Towards Full-area Passivating Contacts for Silicon Surfaces based on Al_2O_3-TiO_x Double Layers

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Abstract — **In order to remove the local openings for contacting PERC Solar cells, one has to introduce passivating contacts. The Al_2O_3-TiO_x double layer stack is an attractive candidate for this purpose. This study will guide a way to enhance the conductivity of those contacts by doping TiO_x with Ta. Additionally, it is shown, that major parts of the stacks are deposited by sputtering. This demonstrates a higher feasibility for industrial applications than atomic layer deposition as reported earlier[1], [2].**

Index Terms – **charge carrier lifetime, contacts, dielectric films, doped titanium oxide, photovoltaic cells, silicon passivation**

I. Introduction

The passivated emitter and rear contact (PERC) solar cell is widely used in industry and its market share increases every year. The state-of-the-art PERC cell is passivated by dielectric materials, like SiN_x and Al_2O_3. They are used for surface passivation of n-type and p-type Si, respectively. Using engineered nanolaminates, it was shown that identical layer stacks can be used for front- and backside passivation [3]. However, in all cases insulating dielectrics are used that need to be opened locally for electrical contact formation. The local metal contacts reduce the efficiency of the solar cell by carrier recombination due to high density of interface states at the openings.

One way to circumvent this drawback is the usage of transparent full area contacts. For example, carrier selective contacts (CSC) are used to reduce the recombination losses while ensuring a good contact resistivity. These contacts extract only one type of carriers (electrons or holes) from the absorber material (e.g. Si) caused by a specific band alignment. Several approaches for CSCs are discussed in literature such as a-Si [4], VO_x, WO_x or MoO_x [5]. CSCs as full-area contacts promise a high efficiency. However, the integration into the PERC process flow is challenging. The thermal instability of amorphous or microcrystalline materials is one of the main limiting factors [3],[4]. Moreover contact concepts based on Si have parasitic photon absorption and are limited in thickness.

Thus, the crucial point of a full area contact is the transparency of the material. Titanium Oxide (TiO_x) is often discussed in literature as an electron-selective contact [6]–[8]. It has a small conduction-band offset ($\Delta E \approx 0.05$ eV) and a large valence-band offset ($\Delta E \approx 2$ eV) to Si. This results in a hole-blocking system. Additionally, it possesses a reasonable band gap of about 3.2 eV [9].

The Al_2O_3-TiO_x double layer on Si is a promising CSC for Si solar cells, because it combines the advantages of both materials [7],[8]. Amorphous Al_2O_3 is established as antireflection coating and passivation on solar cells. Additionally, it is temperature stable up to 400 °C. Dirnstorfer et al. studied Al_2O_3-TiO_x combinations in detail. TiO_x deposited by Atomic Layer Deposition (ALD) with a thickness of 20 nm has 6.7 Ωcm^2 contact resistance [2]. However the lifetime is below 0.1 ms. The combination of both materials in double layers can increase the lifetime by one order of magnitude. The Al_2O_3-interlayer between Si and TiO_x acts as a tunneling layer, similar to the TOPCon concept [4]. Dirnstorfer et al. [2] have further shown, that a 5 nm Al_2O_3-interlayer results in a lifetime of $\tau \approx 1$ ms, however the contact resistance needs to be reduced further.

This study focuses on the improvement of the Al_2O_3-TiO_x double layer stack. The increase of the conductivity of the TiO_x will be addressed by doping with Ta. The substitution of Ti^{4+} with Ta^{5+} in anatase TiO_x leads to a shallow donor with an energy level of 0.01 eV below the conduction band. This furnishes an additional electron with $E_A = 0.01$ eV excitation energy [10]. In this study the TiO_x-layer and the doping are deposited by sputtering, because of its convenience for industrial application. Furthermore, the tuning of the Ta doping concentration is straightforward by co-sputtering Ta from another target together with TiO_x.

II. Experimental Details

The Al_2O_3-TiO_x double layer stack is schematically shown in Fig. 1 a). Al_2O_3 layers with thicknesses $d = 0.5\ldots6$ nm were deposited by thermal ALD (150 °C) using TMA/water processes as described in previous publication [11], [12]. After the Al_2O_3 deposition, a TiO_x layer was sputtered on top to reach a total layer stack thickness of 20 nm. The power density of the DC-plasma at the Ti-target was 6.6 W/cm^2 with 40 sccm Ar- and 4 sccm O_2-flow at a process pressure of $5 \cdot 10^{-3}$ mbar and room temperature. This sputter system enables doping with Ta by igniting an additional plasma at a second target. The RF-plasma power density was varied from $0\ldots1.1$ W/cm^2 to achieve different Ta doping concentrations, which are determined by XPS. It is possible to change the ratio Ta/(Ta+Ti) in a range between 0.02…0.2 with co-sputtering. The inset of Fig. 2 shows the Ta/(Ta+Ti) ratio A depended on the RF-power at the Ta target. The depositing of every films

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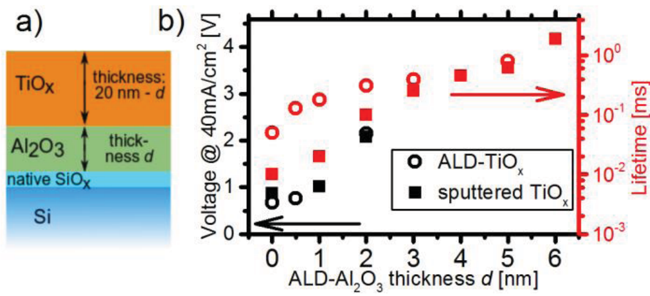

Fig. 1. a) Sketch of the Al_2O_3-TiO_x double layer stack with Al_2O_3 thickness d. The total thickness was 20 nm. b) Minority carrier lifetime (red) and voltage drop at 40 mA/cm^2 (black) vs. Al_2O_3 interlayer thickness d with ALD-TiO_x (open circles) and sputtered TiO_x (solid squares).

was followed by a post deposition anneal (PDA) in forming gas (N_2:H_2 = 9:1) at 350 °C for 10 min.

For lifetime measurements with microwave-detected photoconductivity (MDP), the passivation layers were realized on high purity p-type float-zone Si substrates (250 μm thickness, 1-3 Ωcm) at both sides. Additionally, highly doped p-type Chochralski-Si pieces (< 0.005 Ωcm) were processed just on one side during the same deposition runs. These samples were analyzed by X-ray photoelectron spectroscopy (XPS), grazing incidence X-ray diffraction (GIXRD) and thickness determination with X-ray reflectometry (XRR).

In order to evaluate the resistivity of the contacts, current depended voltage measurements were performed after the thermal evaporation of Al electrodes (≈ 0.1 mm^2). The targeted contact resistance of full-area contacts is less than 0.25 Ωcm^2 in order to keep efficiency of a PERC cell high [13]. This resistance corresponds to a 10 mV voltage drop at 40 mA/cm^2 short-circuit current density of a cell. By using highly doped substrates the measured voltage drop over the entire stack is a good indication for the resistivity of the contact layer.

III. Results and Discussion

Commercially used PERC solar cells require a surface recombination velocity S_{eff} below 100 cm/s to accomplish an efficiency above 20 % [14]. Assuming negligible volume recombination in the high purity pFZ-Wafers with a thickness W = 250 µm, the lower minority lifetime limit is $\tau_{eff} = 0.5 \cdot W/S_{eff}$ = 125 µs [2]. Fig. 1 b) shows the lifetime of an Al_2O_3-TiO_x double layer as a function of the Al_2O_3-interlayer thickness d.

The lifetime measured with pure TiO_x-layers (d = 0 nm) is below the target (125 μs) for both, ALD (≈ 50 μs) and sputtered TiO_x (≈ 10 μs). A 1 nm thick Al_2O_3-interlayer is necessary to achieve 180 µs, if the TiO_x is deposited by ALD. 3 nm Al_2O_3 are needed to exceed the target of $\tau_{eff} \approx$ 125 µs in case of sputtered TiO_x (250 µs). The difference is likely to be caused by sputter damage, which degrades the interface [15], [16]. The minority lifetime for sputtered and ALD-TiO_x is in the same

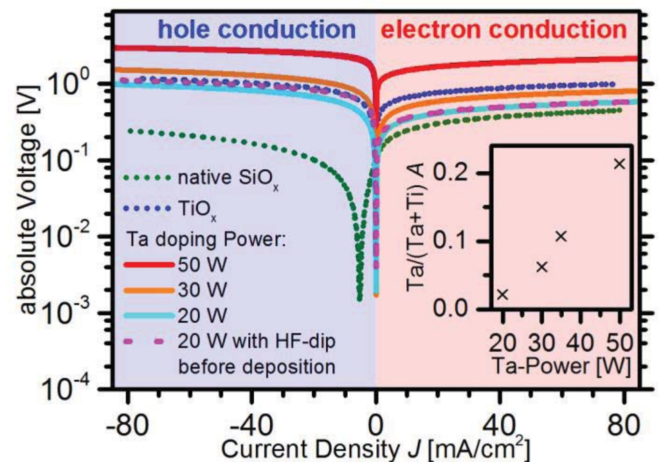

Fig. 2. Voltage vs. Current density measurements of native SiO_x (≈ 1.4 nm) and pure TiO_x, Ta:TiO_x (20 nm thick) with different RF-plasma power at the Ta-target. Inset: Ta/(Ti+Ta)-atom-ratio A vs. RF-plasma power at the Ta-target measured with XPS. Calculation was done with the XPS lines Ta4d and Ti3p.

range for $d \geq$ 3 nm. Probably the thicker Al_2O_3-layer causes a reduction of the sputter damage at the Si interface. A 6 nm Al_2O_3 ALD-layer exceeds 1 ms in both cases ALD-TiO_x and sputtered TiO_x.

However, the voltage drop (Fig. 1 b) for both deposition methods seems to be similar for all investigated thicknesses. The voltage drop over the layer stack with thicknesses d > 2 nm was too high to evaluate. The layer stack broke down electrically, when 40 mA/cm^2 were applied. Pure TiO_x of 20 nm thickness yields the lowest voltage drop of 0.66 V and 0.87 V for ALD and sputtering, respectively. The voltage drop is more than one order of magnitude higher than the target of 10 mV, which corresponds to 0.25 Ωcm^2.

Therefore, the TiO_x conductivity needs to be further increased. This is done via doping by co-sputtering of Ta. Fig. 2 shows current sweeps of differently doped Ta:TiO_x samples compared to pure TiO_x. Despite the usage of p-doped substrates, the voltage drop is slightly higher with negative applied current than with positive applied current. This is due to the hole blocking behavior of TiO_x [8], [9], [17]. At the positive branch (electron conduction), a reduction of the voltage drop was observed with Ta:TiO_x using 20 W and 30 W RF-plasma power at an additional Ta-Target. These correspond to a Ta/(Ta+Ti)-atom-ratio A of 0.02 and 0.06 (inset of Fig. 2). The voltage drop coincidences with the crystallization of TiO_x. After a 350 °C forming gas PDA, sputtered TiO_x with different Ta RF-plasma power formed an anatase phase as measured with GIXRD (see inset of Fig. 3). It shows the characteristic (101) peak of anatase TiO_2 at 2θ = 25.3° for a Ta RF-plasma power between 0 W and 35 W. This corresponds to a ratio A = 0…0.10 (Fig. 2).

A higher ratio $A \approx$ 0.21 (50 W RF-Power) results in a voltage drop, that is even above the voltage drop for pure TiO_x (Fig. 2). Also the characteristic (101) peak is missing for the layer doped

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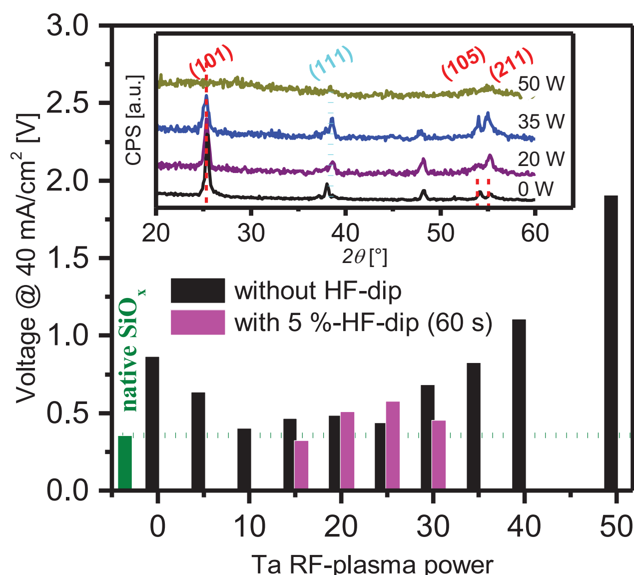

Fig. 3. Extracted voltage drop at 40 mA/cm^2 vs. RF-plasma power at the Ta-target with (purple bars) and without (black bars) 5 %-HF-dip (60 s) before deposition. Native SiOx is shown in green. Inset: GIXRD measurements of pure TiO_x and Ta:TiO_x with different anatase TiO_x planes (red dashed) and the (111)-plane (blue doted) of Al-electrode.

by a 50 W RF-plasma power. This layer is still amorphous after PDA. Probably the solubility limit of Ta in TiO_x is exceeded and an additional TaO_x is formed, which hinders the crystallization and reduces the conductivity of the layer. This result underlines the necessity of crystalline layers for a low voltage drop [10], [18], [19].

Different depositions with various RF-powers exhibit a process window from 10 to 25 W (Fig. 3) to reduce the voltage drop to a minimum of about 0.4 V. This is close to the voltage drop of the Si/SiO_x-layer stack (0.36 V). It indicates that most of the applied voltage drops over the native SiO_x. Supposing a thinner SiO_x leads to a lower voltage drop, the Si substrates were dipped in a 5 %-HF-solution before depositing the TiO_x. The measured voltage drop in Fig. 2 (dashed purple line) shows no decrease compared to the sample without HF-dip. The purple bars in Fig. 3 show HF-dipped samples with different Ta RF-power. There is no significant change observable. Probably part of the SiO_x is reformed during the PDA, which is necessary to form an anatase TiO_x phase [7].

Fig. 4 shows a summary of the performed deposition methods of TiO_x on top of a $d = 2$ nm ALD-Al_2O_3 layer. The ALD-TiO_x layer reaches the highest lifetime (180 µs). The sputter TiO_x and Ta:TiO_x layer (≈ 100 µs) obtain a lifetime slightly below the target of 125 µs. The contact resistance, which is defined by the voltage drop over the Si/SiO_x/Al_2O_3/TiO_x-layer stack (Fig. 1) is similar for the sputtered and the ALD-TiO_x (≈ 50 Ωcm^2). However it is possible to decrease the contact resistance to 40 Ωcm^2 by doping the layer with Ta.

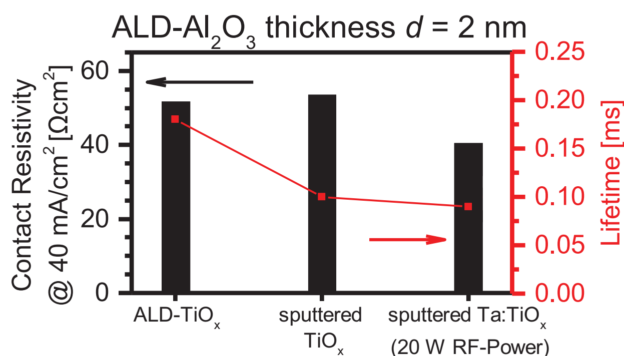

Fig. 4. Contact Resistivity at 40 mA/cm^2 (black bars) and minority carrier lifetime (red bars) of samples with $d = 2$ nm Al_2O_3 deposited by ALD. 18 nm TiO_x was deposited on top by different methods.

IV. Conclusions

In this study carrier selective contacts were realized with Al_2O_3-TiO_x double layers. A comparison between ALD-TiO_x and sputtered TiO_x is presented with focus on contact resistance and minority lifetime. In terms of contact resistivity, there was no difference observable between the deposition methods. However, the lifetime is reduced in case of sputtered TiO_x, probably because of sputter damage. A 3 nm ALD-Al_2O_3 layer reduces this damage. 6 nm Al_2O_3 lead to a lifetime of 1 ms.

The resistivity of the TiO_x can be lowered by doping it with Ta. This was done by a co-sputtering approach. A process window between 10 and 25 W RF-plasma power at an additional Ta-target reduce the voltage drop over the measured Si/SiO_x/Ta:TiO_x layer stack to 0.4 V. The voltage drop over a Si/SiO_x-stack was 0.36 V. Thus, it is likely, that most of the voltage drops over the SiO_x and does not over the Ta:TiO_x.

The Ta:TiO_x (20 W RF-power) lowers the contact resistance of a Si/SiO_x/Al_2O_3/TiO_x-layer stack from 50 to 40 Ωcm^2. However the lifetime is reduced to about 100 μs. In summary, a lowering of the thickness of Al_2O_3 and native SiO_2 is unavoidable. Nevertheless, these experiments show the way to passivating full area contacts and solidifies the claim of Al_2O_3-TiO_x double layers as the material combination of choice.

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