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Vertically Integrated Reconfigurable Nanowire Arrays

Tim Baldauf, André Heinzig, Thomas Mikolajick, *Senior Member, IEEE*, and Walter M. Weber, *Member, IEEE*

***Abstract*— This letter discusses a feasible variant of vertically integrated reconfigurable field effect transistors (RFET) based on top–down nanowires. The structures were studied by 3-D device simulations. Subdividing the structure into two vertical pillars allows a lean technological realization as well as simple access to the electrodes. In addition of enabling p- and n-FET operations like a horizontal RFET, the device delivers higher performance. We show that by the integration of additional vertical pillars and select gates, a higher device functionality and flexibility in interconnection are provided.**

***Index Terms*— Silicon nanowire, nanowire array, reconfigurable logic, CMOS, RFET, functionality enhanced devices, polarity control, SBFET, tunneling, Schottky barrier, vertical, TCAD.**

I. Introduction

THE limited scalability of horizontally integrated metal oxide semiconductor field-effect transistors (MOSFETs) requires reconsideration for future technologies beyond the 7 nm node. For instance, the vertical integration of nanowire as well as fin structures allows to decouple the area scaling from the laterally confined gate pitch [1]–[3]. In addition to the efforts to maintain the scaling rules, beyond CMOS approaches to increase the functionality of integrated circuits are under investigation. In that sense reconfigurable field effect transistors (RFETs) are a possibility to provide enhanced functionality due to a selectable n and p-FET polarity [4]–[7]. RFETs enable programmable logic computing of various logical functions with the same circuit by simply altering a program signal at the transistor level [8]. Thus, regardless of the classical scaling, which can also be applied to the RFET concept, RFETs provide an increase in circuit functionality as well as flexibility at an equal transistor count.

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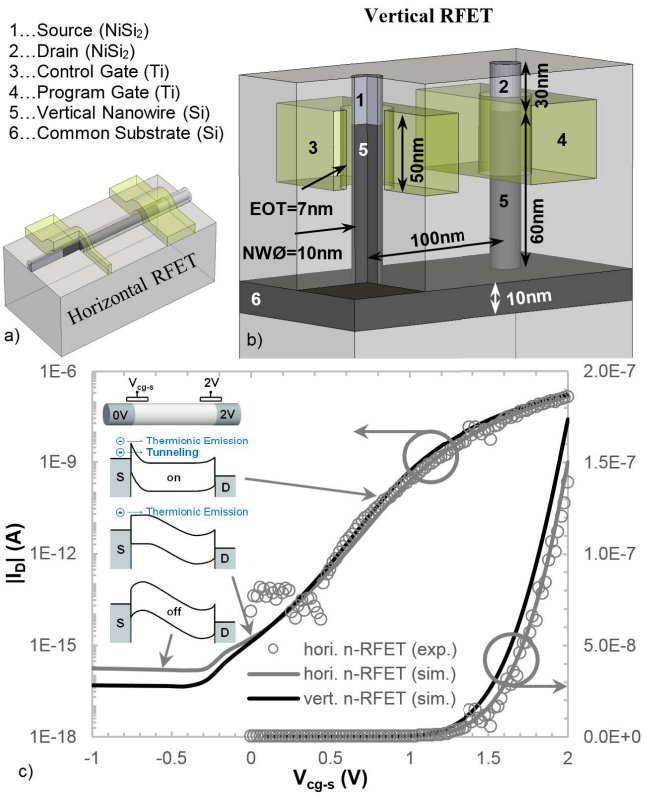

Fig. 1. Comparison of a horizontal and a vertical integrated cylindrical nanowire RFET. a) Schematic view of a horizontal RFET and b) labeled schematic view of a vertical RFET. c) N-type transfer characteristic of both variants compared to the experimental data of a horizontal RFET. The inset illustrates the band structure between source and drain at three regions of the curve.

For instance, in combinational electronics, such as 4-, 6- and 8-bit-adders it has been verified that the transistor count can be reduced by almost 50% by employing RFETs instead of conventional MOSFETs [9]. In addition, complementary XORs can be realized with only 4 RFETs [5], and thus facilitate novel design automation paradigms such as Majority Inverter Graph optimization algorithms [10]. Currently all RFET realizations have been horizontal either with single or stacked nanowires or 2D layers, like shown schematically in Fig. 1a. However, such implementations are demanding in terms of device cell area and reproducible control of silicide length at the source- and drain-electrodes.

This letter shows the concept of a vertically integrated array of nanowires that can both overcome the area and

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contact formation deficiencies of horizontal RFETs. Furthermore, the architecture comprising a multitude of gated access wires sharing a common channel body, opens an additional functional enhancement and extended logic circuit synthesis opportunity. At first, there will be a short introduction of the RFET functionality followed by the explanation of the performance improvement due to the vertical nanowire with a gate all around (GAA) contact geometry. The gate matrix is able to connect and subdivide nanowire terminals, thus enhancing functionality. The presented data are simulated with finite element 3D device simulations by SYNOPSYS Sentaurus and were previously calibrated by experimental data for horizontal devices [6], [11]. The considered geometries are illustrated in Fig. 1b and correspond to the dimensions of the experimental horizontal structure for better comparability between both devices. The used models for carrier transport, barrier tunneling, quantum mechanical confinement, mobility degradation as well as the impact of mechanical stress are the same as described in [6].

II. The Vertical RFET

In analogy to its horizontal counterpart, the vertical RFET consists of two separately gated Schottky junctions representing source and drain (Fig. 1) [4]. While the gate on the drain-side labeled as program gate (4) blocks the unintended charge carriers, the gate on the source-side labeled as control gate (3) switches the device into ON- or OFF-state by the adjustment of the charge carrier transmissibility of the source Schottky junction (as shown by the schematic view of the band diagram in Fig. 1c). The Schottky barriers made of $NiSi_2$-Si are ideally flat and can exhibit atomically sharp interfaces [12]. For the silicidation of the vertical silicon nanowires, an epitaxially controlled $NiSi_2$ process giving flat planar interfaces as described in [13] can for instance be applied to achieve a comparable silicidation depth for all wires. Compared to horizontal $NiSi_2$ encroachment in nanowires, the amount of Ni and the size of the overlapping Ni to Si contact area can be controlled more homogeneously since the surface for Ni deposition is flat (unlike to the case in Fig. 1a). Due to the vertical construction and the top location of source and drain, this temperature- and time-critical process can be performed at the end of the front-end manufacturing process, which provides the advantage of smaller variability and higher device reliability. Following the vertical pillar and gate formation as well as the capping of the top nanowires by chemical mechanical polishing (CMP), the depth of the nickel silicide can be controlled via full consumption of a planar thin Ni layer or formation of epitaxial $NiSi_2$, e.g. by employing ultrathin Ni layers or by Al intermixing [14]. Thus, the gate to Schottky junction alignment is independent of lithography, which itself implies an important reduction of variability.

The channel of the vertical RFET is distinguishably subdivided into the vertical nanowire sections and a common horizontal silicon on insulator (SOI) substrate connecting the vertical nanowires. As for the horizontal RFET, and unlike to conventional MOSFETs, the ungated part between program and control gate plays a subordinate role for the predominantly diffusion-based charge carrier transport and thus for the total device resistance. As the transfer characteristic for the n-type RFETs shows in Fig. 1c, the performance of the vertical device has not been deteriorated by the additional SOI channel section. On the contrary, a slight improved performance could be accomplished due to the enhanced gate coupling of the GAA contact compared to the omega shape one of the horizontal RFETs [11]. In general, the performance of the RFET concept is comparable to other Schottky barrier FETs (SBFET) [15], [16]. A significant benefit of applications with ultra-low power consumption and small activity factor is the large ON/OFF ratio of up to 10^9, which is two orders of magnitude larger than that of state-of-the-art ultra-low power technologies like 22 nm FinFETs [4], [17] and four orders of magnitude larger than that of state-of-the-art vertical nanowire GAA MOSFETs [18]. The scalability of horizontal RFETs with omega gate architecture has been studied in [8] and verified down to 36 nm channel lengths. We expect a slightly improved scalability with the vertical surround gate RFET due to the smaller screening or natural length [19]. In addition, RFET scaling has the advantage to improve the subthreshold swing (tunneling part of the transfer curve) thanks to an increasingly stronger coupling between gate potential and Schottky barrier width. Simulated nanowire RFETs with 7 nm channel thickness and 0.8 nm EOT show a subthreshold swing of approximately 90 mV/dec.

Note, that while applications with doped vertical MOSFETs usually have different drive currents in the forward or backward mode, the vertical RFET provides a high n- and p-current symmetry. However, a prerequisite for this symmetry is a stable and reliable silicidation process of source and drain.

III. The Common Channel

The realization of the channel connection to the common SOI substrate provides elegantly the possibility of producing array structures with a multitude of individually steered vertical nanowires. These can obviously be used as parallel source- and drain contacts so that the entire device can drive more current compared to one with only one source and one drain contact. The resulting current enhancement depends on the arrangement of the wires. In the concrete example of Fig. 2, the most unfavorable case was considered, in which the four wires are connected as a series to the SOI body giving different source to drain distances. SD1 and SD2 are used as drain and SD3 and SD4 as source contacts respectively. The applied contact voltages for the ON-state of the device can be read from the electrostatic potential shown in Fig. 2a. In this arrangement, the total drive current in Fig. 2c is increased by 50% compared to the drive current of a device with only one nanowire for source and drain, respectively. In a more favorable parallel arrangement of source and drain contacts, doubling of the drain current has been verified.

It should be emphasized that the common SOI body opens the opportunity to augment functionality. By coupling potentials to the SOI region, additional potential barriers can be induced to either block electrons or holes. An additional potential barrier gives the advantage of separating or isolating a larger vertical RFET into several smaller sub-devices. In the example of Fig. 2, these potential barriers can be supplied by the crossline contact (CL) in the middle of the device. First, it is set to $+0.8$V, which is in the range of the channel potential of the n-type RFET. As a result, the electrons do not exhibit a blocking potential. In Fig. 3 the crossline potential is set to -0.8V, blocking most of the electrons. As a

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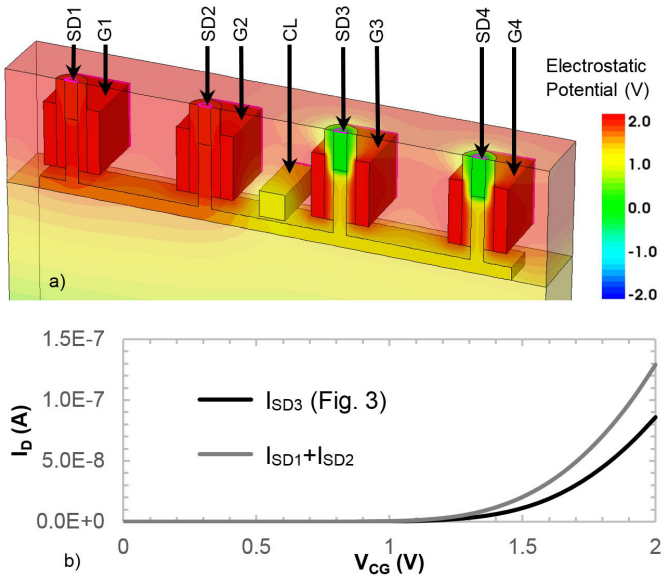

Fig. 2. Electrical characteristic of a vertical integrated RFET structure consisting of four nanowires which are used as source or drain contact (SD) and are surrounded by separate gate contacts (G). A crossline (CL) is located between SD2 and SD3 and has a positive potential which allows an electron flow between all the nanowires. a) Half of the simulated structure with the electrostatic potential for the n-type ON-state. b) Currents of SD1+SD2 compared to the current of SD3 in Fig. 3 as function of the control gate voltage.

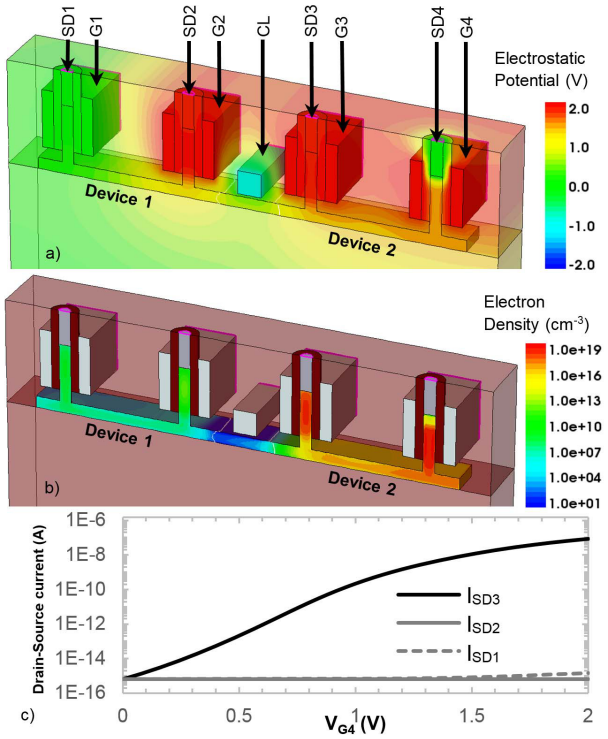

Fig. 3. Electrical characteristic of a vertical integrated RFET structure consisting of four nanowires which are used as source or drain contact (SD) and are surrounded by separate gate contacts (G). A crossline (CL) is located between SD2 and SD3 and separates the structure in two n-type devices. a) and b) show the half of the simulated structure with the electrostatic potential and the electron density, respectively, for the Off-state of device 1 and the ON-state of device 2. c) The currents of SD1, SD2 and SD3 as function of V_{G4}.

consequence the structure is divided into two n-type RFET devices. To demonstrate the successful separation of both n-type configured RFETs, device 1 between SD1 (source) and SD2 (drain) is set into the OFF-state (control gate G1 to 0V) and device 2 between SD3 (drain) and SD4 (source) is set into the ON-state (control gate G4 to 2V). For this scenario, the electron density in the channel region is shown in Fig. 3b. The dark blue color under the crossline exhibits the low-electron region where the potential barrier is located. Fig. 3c shows the total current of contact SD1, SD2 and SD3 as a function of the control gate V_{G4}. The transfer characteristic of device 2 is shown by I_{SD3}. I_{SD1} and I_{SD2} demonstrate the negligible crosstalk between devices 1 and 2. Only the leakage current through SD1 increases slightly due to a weak change of the channel potential of device 1. However, two factors have to be considered to achieve such a good screening. The contacts next to the CL should be used as drains, so the potential of the drain-side program gate keeps the channel potential stable around the vertical nanowire channel of the respective device. With the source contact next to the CL, the drain current (ON-state) of the separated device would be decreased by 18 % compared to the other configuration. However, this impairment strongly depends on the geometry. It is also advisable to use a low-k dielectric between the contacts to reduce parasitic capacitances and to limit the propagation of the CL potential to the desired range. Additionally, multi-terminal devices can be built by steering all gates independently of each other.

It is feasible to configure such a device with four vertically integrated and individually gated Schottky junctions in a way of defining three junctions as source contacts and one junction as drain contact. Thus, parallel transistor networks are efficiently bundled. This can for instance be applied to the parallel operating RFETs of a 3-NAND/3-NOR reconfigurable gate from Fig. 4b in [20]. Importantly, with the use of this approach the 3-NAND/3-NOR gate can be interconnected with the use of only 3 Tracks. Networks of Series transistors can also be efficiently realized by the proposed vertical RFET structure with the use of multiple crosslines. Compared to CMOS where sizing of p- and n- devices is fixed lithographically the *I-V* symmetry in p- and n-type characteristics of RFETs enable flexible reconfiguration of such series networks without affecting the delay. It is anticipated that the benefit of vertical RFETs is more strongly perceivable in circuits with higher complexity. Raitza *et al.* [9] proposed that a 16-bit block adder of horizontal RFETs just needs the half of transistor count compared to optimized CMOS circuits. Also the vertical integration offers the possibility to reduce the total layout area for lager circuits like 32-bit multiplier as described by Bao *et al.* [21].

For enhanced functionality, the CL can be used as control gate of larger devices with several drain and source contacts. Its additional potential controls a thermionic barrier in the device channel like conventional MOSFETs. Thus, with a suitable geometry a steeper subthreshold swing down to 60 mV/dec can be achieved compared to the swing of the control gate.

In summary, we propose a vertically integrated nanowire RFET array with GAA junctions that largely solves the space and contact formation deficiencies of horizontal RFETs. The common channel body of multiple gated wires is successfully combined with an interconnection array matrix enhancing flexibility and functionality of the device at runtime compared to single nanowire RFETs and to conventional MOSFETs.

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