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A 4 - 32 GHz SiGe Multi-Octave Power Amplifier with 20 dBm Peak Power, 18.6 dB Peak Gain and 156 % Power Fractional Bandwidth

Manu Viswambharan Thayyil, Songhui Li, Niko Joram and Frank Ellinger, *Senior Member, IEEE*

***Abstract*—This letter presents the design and characterization results of a multi-octave power amplifier fabricated in a 0.13 µm SiGe-BiCMOS technology. The single stage power amplifier is implemented as the stack of a cascode amplifier combining broadband input matching network with resistive feedback, and a common-base amplifier with base capacitive feedback. Measurement results show that the design delivers a peak saturated output power level of 20.2 dBm, with output 1 dB compression at 19.4 dBm. The measured 3 dB power bandwidth is from 4 GHz to 32 GHz, covering three octaves. The corresponding power fractional bandwidth is 156 %. The measured peak power added efficiency is 20.6 %, and peak small signal gain is 18.6 dB. The fabricated integrated circuit occupies an area of 0.71 mm^2. To compare state-of-the-art multi-octave power amplifiers, the power amplifier figure of merit defined by the international technology roadmap for semiconductors is modified to include power fractional bandwidth and area. To the knowledge of the authors, the presented design achieves the highest figure of merit among multi-octave power amplifiers in a silicon based integrated circuit technology reported in literature.**

***Index Terms*—Power amplifier, broadband matching networks, feedback, SiGe-BiCMOS technology, figure of merit.**

I. Introduction

BANDWIDTH is an important performance parameter along with output power, power added efficiency (PAE) and gain for power amplifiers (PA). Silicon based integrated system applications like positioning and localization radars, imaging systems, and communication transceivers have been instrumental in pushing both the maximum frequency and bandwidth of all components including PAs to microwave, millimeter wave and beyond. To address this demand, several wideband power amplifiers implementations are reported in literature. These include predominantly silicon germanium (SiGe) BiCMOS implementations [1]–[4], while CMOS implementations are catching up [5], [6]. Most PAs reporting a high power fractional bandwidth (PFBW) are based on the distributed amplifier (DA) topology [1], [4], [5], occupying large area, having low gains, often requiring pre-amplifiers when used in a system and having low PAE. Whereas PAs based on other topologies [2], [3], [6] have relatively lower PFBW than DA based PAs.

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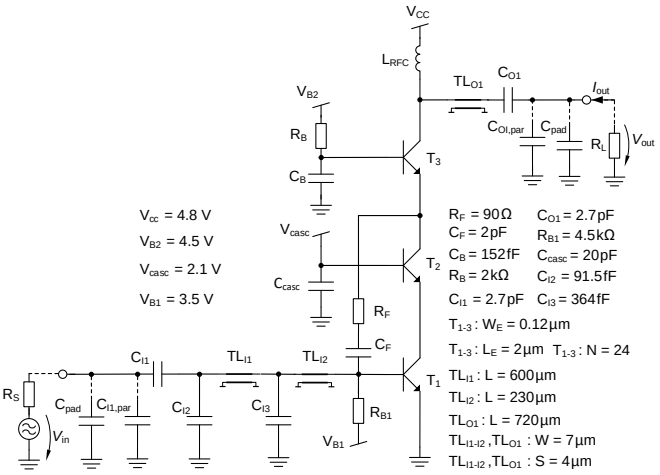

Fig. 1: Circuit schematic of the designed multi-octave PA .

A single stage multi-octave power amplifier (MOPA), completely covering the frequency bands K_u and K, which includes the 24 GHz ISM band and 28 GHz 5G frequency bands, and partially covering the UWB and K_a bands is presented in this letter. The MOPA uses a novel combination of resistive feedback to enable broadband input matching of low-ohmic, highly capacitive input impedances, and transistor stacking for high output power with better output transfer network efficiency across a wide frequency range. The design is optimized to maximize the PFBW and gain, and to minimize the occupied area, while maintaining an output power and PAE comparable to the state-of-the-art in these frequency ranges.

The circuit design of the single gain stage multi-octave PA, including the implementation of matching networks are discussed in Section II. Characterization results and comparison of results with the state-of-the-art are discussed in Section III. Section IV summarizes the letter, highlighting key features of the design and results.

II. Design

The single stage MOPA shown in Fig. 1 is implemented using heterojunction bipolar transistors (HBTs) in a 0.13 µm SiGe-BiCMOS technology with with f_t / f_{max} of 250 GHz / 340 GHz from IHP microelectronics. The design target output power level of 20 dBm corresponds to a peak-to-peak voltage swing $V_{out,pp} \approx 6.3\,V$ on load resistance $R_L = 50\,\Omega$, calculated using $P_{out} = V_{out,pp}^2/(8R_L)$, for

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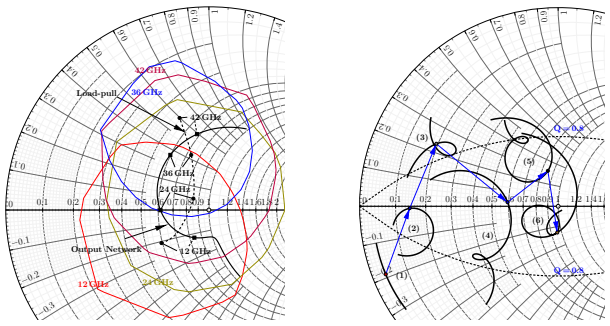
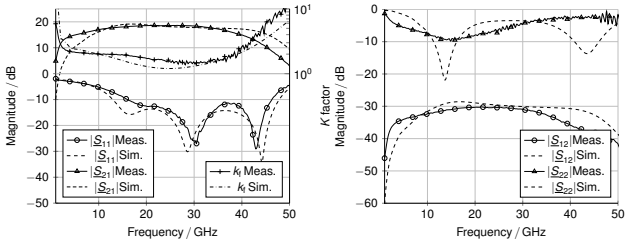
an output network transformation ratio of 1. For a single HBT used in this design, the collector-emitter breakdown voltage when the base is open amounts to $V_{\mathrm{BVCEO}} \approx 1.7\,\mathrm{V}$. However, it can be seen from [7] that, when the base resistance is optimized to lower values, the corresponding breakdown voltage V_{BVCER} is much higher, and close to the collector-base breakdown voltage V_{BVCBO} with open emitter. Using this approach along with technology process documentation, it is determined that base resistance values less than $5\,\mathrm{k\Omega}$, are required for $V_{\mathrm{BVCER}} > 3.5\,\mathrm{V}$. The base resistance values used in the design as shown in Fig. 1 are optimized as a trade-off between breakdown voltage and sensitivity to bias voltage variations. Now using $V_{\mathrm{out,pp}} = n(V_{\mathrm{BVCER}} - V_{\mathrm{knee}})$, where $V_{\mathrm{knee}} \approx 350\,\mathrm{mV}$ is the knee voltage, the number of transistors in the stack is calculated as $n = 2$. This means that a stack of two HBTs, $\mathrm{T}_{2,3}$ is sufficient to generate the required output power to be delivered directly into R_{L}. The common base stage consisting of T_3, base feedback capacitance $C_{\mathrm{B}} \approx 152\,\mathrm{fF}$ and resistance $R_{\mathrm{B}} \approx 2\,\mathrm{k\Omega}$ distributes $V_{\mathrm{out,pp}}$ equally among the HBTs $\mathrm{T}_{2,3}$ using the stacking principle described in [8]. The optimum load required to generate the maximum output power can then be obtained from the load line as $R_{\mathrm{opt}} = V_{\mathrm{out,pp}} \,/\, I_{\mathrm{out,pp}} = 6.3\,\mathrm{V} \,/\, 129\,\mathrm{mA} \approx 49\,\Omega$. To generate the target power with high gain, $\mathrm{T}_{1\text{-}3}$ in Fig. 1 are dimensioned as 24 parallel HBTs with a total emitter area $A_E = 24 \times 0.12\,\mu\mathrm{m} \times 2\,\mu\mathrm{m}$, and biased near the maximum f_{t} current density at $2\,\mathrm{mA}\,/\,\mu\mathrm{m}$. Load-pull simulations are done over the frequency range to obtain the optimum load required to generate the maximum power as shown in Fig. 2(a). The impedance transformation network required to present the optimum load to the collector of T_3 is implemented using the combination of the grounded coplanar waveguide (GCPW) transmission line $\mathrm{TL_{O1}}$ with characteristic impedance $Z_0 = 50\,\Omega$ and length $720\,\mu\mathrm{m}$, the capacitance $C_{\mathrm{O1}} \approx 2\,\mathrm{pF}$, which also functions as a dc block, and the equivalent shunt capacitance formed by the parasitics and pad capacitance $C_{\mathrm{O1,par}} + C_{\mathrm{pad}} \approx 80\,\mathrm{fF}$. The output impedance transformation network is optimized such that, across the frequency range of interest, the MOPA generates an output power within 2 dB of the maximum possible output power that can be generated at each frequency. The corresponding simulated impedance trajectory across the frequency range is shown in Fig. 2(a).

The large HBT emitter area used to generate the required output power results in a very low-ohmic and highly capacitive input impedance, $\underline{Z}_{\mathrm{in}} = R_{\mathrm{in}} - jX_{in} \approx 1.8 - j9.5\,\Omega$ at $f_{\mathrm{c}} = 24\,\mathrm{GHz}$ as shown in curve (1) of Fig. 2(b). The corresponding nodal quality factor $Q_{\mathrm{in}} = \frac{|X_{\mathrm{in}}|}{R_{\mathrm{in}}} = 5.3$, the equivalent parallel resistance $R_{\mathrm{p,in}} = (1 + Q_{\mathrm{in}}^2)Rs \approx 50\,\Omega$, and equivalent parallel capacitance of $C_{\mathrm{p,in}} = 674\,\mathrm{fF}$. The Bode-Fano matching network bandwidth limit [9], for an $|\underline{S}_{11}| = -10\,\mathrm{dB}$ and corresponding input reflection coefficient $|\Gamma|_{\mathrm{max}} = 0.32$, can be then calculated as $f_{\mathrm{BW,limit}} \leq \frac{1}{2R_{\mathrm{p,in}}C_{\mathrm{p,in}}\ln\frac{1}{|\Gamma|_{\mathrm{max}}}} \approx 12.3\,\mathrm{GHz}$. The introduction of the negative feedback resistor R_{F} increases this limit by a factor of 80, making $|\underline{Z}_{\mathrm{in}}|$ predominantly resistive to $\underline{Z}_{\mathrm{in,fb}} \approx 7.3\,\Omega$ as shown in curve (2) of Fig. 2(b). The



(a) (b)

Fig. 2: (a) Optimum load at different frequencies obtained from load-pull simulations, 2 dB load-pull contours and the impedance looking into the output transformation network. (b) Shows the design trajectories for the input matching network.



(a) (b)

Fig. 3: Measured and simulated small signal parameters.

R_{F} required to obtain this $\underline{Z}_{\mathrm{in,fb}}$ can be calculated at f_c as $R_{\mathrm{F}} \approx (1 - \underline{a}_{\mathrm{v}})\,\frac{R_{\mathrm{p,in}}\,\underline{Z}_{\mathrm{in,fb}}}{(R_{\mathrm{p,in}} - \underline{Z}_{\mathrm{in,fb}})} \approx 90\,\Omega$, where the voltage gain of the cascode stage $\underline{a}_{\mathrm{v}}$ has a magnitude $|\underline{a}_{\mathrm{v}}| \approx 10$. The transformation of this Z_{in} to source impedance $R_{\mathrm{s}} = 50\,\Omega$ is done using a two section matching network, confining the impedance transformation trajectory to a $Q = 0.8$ curve and the real axis, as shown in Fig. 2(b). $Q = \frac{f_{\mathrm{C}}}{f_{\mathrm{BW}}} \approx 0.8$ is calculated using $f_{\mathrm{c}} = 24\,\mathrm{GHz}$, and small signal bandwidth $f_{\mathrm{BW}} = 30\,\mathrm{GHz}$. The impedance transformation trajectory in Fig. 2(b) from curve (2) through curves (3), (4) and (5) to R_{s} is implemented using GCPW transmission lines $\mathrm{TL_{I1}}$ and $\mathrm{TL_{I2}}$ with $Z_0 = 50\,\Omega$, capacitors $C_{\mathrm{I1}} = 2.7\,\mathrm{pF}$ $C_{\mathrm{I2}} = 91.5\,\mathrm{fF}$ and $C_{\mathrm{I3}} = 364\,\mathrm{fF}$. $\mathrm{TL_{I1}}$ has a length of $600\,\mu\mathrm{m}$, and $\mathrm{TL_{I2}}$ has a length of $230\,\mu\mathrm{m}$. The parasitic capacitance $C_{\mathrm{I1,par}}$ and C_{pad} are also included in the network. The MOPA is also unconditionally stable across the frequency range from post layout K-factor (K_{f}) simulations and stability circles.

III. Characterization

The inset of Fig. 4 shows the fabricated MOPA IC, occupying an area of $845\,\mu\mathrm{m} \times 845\,\mu\mathrm{m} = 0.71\,\mathrm{mm}^2$ including pads. The bias voltages shown in Fig. 1 are used to set the operating point, and the corresponding bias current measured is 98 mA. S-parameters and large signal parameters as a function of frequency are characterized using a test setup mainly consisting of a R&S 67 GHz vector network analyzer (VNA) ZVA67. S-parameter measurements confirm that the small signal parameters including input matching and

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TABLE I: Comparison with state-of-the-art multi-octave power amplifiers.

Ref.	$f_{\mathrm{u,3dB}}$	PBW_{3dB}	$PFBW$	$P_{\mathrm{L,sat}}$	$P_{\mathrm{L,OP1dB}}$	Peak Gain	Peak PAE	Area	FoM_{MOPA}[a]	Tech.
	(GHz)	(GHz)	(%)	(dBm)	(dBm)	(dB)	(%)	(mm^2)	($\mathrm{W\,GHz}^2/\mathrm{mm}^2$)	
[6]	33	15.0	59	19.5	16	15.2	10.2	0.86	224	0.18 µm CMOS
[1]	40	30.0	120	15.4	11.4	17.1	10	2.00	171	0.18 µm SiGe
[2]	35	10.7	36	11.1	9.6	16.3	55.9	0.72	189	0.18 µm SiGe
[3]	18	13.5	120	23.7	19.5	15.7	31.9	0.73	1476	0.13 µm SiGe
[5]	23.8[b]	22.8[b]	184[b]	16.7	14.5	11.9	10	1.7	44[b]	0.18 µm CMOS
[4]	40	28.0	108	21.5	19.8	13.9	20.1	1.19	1009	0.13 µm SiGe
This	**32**	**29.0**	**156**	**20.2**	**19.4**	**18.6**	**20.6**	**0.71**	**3423**	**0.13 µm SiGe**

[a] $FoM_{\mathrm{MOPA}} = P_{\mathrm{sat}} \cdot G \cdot PAE \cdot f_{\mathrm{u,3\,dB}}^2 \cdot PFBW$ / Area. [b] Power bandwidth not reported, small-signal bandwidth used.

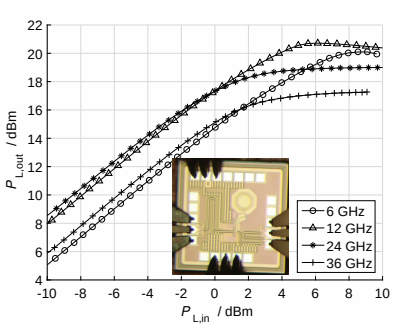
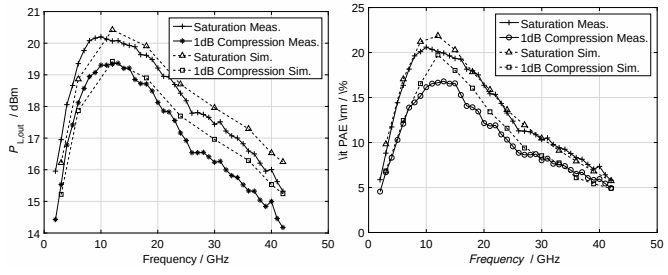


Fig. 4: Measured output power as function of input power levels from −10 dBm to 10 dBm at different frequencies. The fabricated IC occupying an area of $0.71\,\mathrm{mm}^2$ is shown in inset.

gain are in good agreement with simulations as shown in Fig. 3. Also the three characteristic dips due to multi-band input matching network can be clearly seen in the $|\underline{S}_{11}|$ plots in Fig. 3(a). Small signal peak gain is measured as 18.6 dB around 24.6 GHz, and the 3 dB bandwidth is measured as 31.9 GHz from the frequency range of 6.6 GHz to 38.5 GHz.

Input power is swept from −10 dBm to 10 dBm in the 2 GHz to 42 GHz frequency range, and the measured output power as a function of input power for frequencies 6 GHz, 12 GHz, 24 GHz and 36 GHz are shown in Fig. 4. The corresponding



(a) (b)

Fig. 5: Comparison of large signal measurements with simulation. (a) Output power. (b) PAE.

saturated output power level $P_{\mathrm{L,sat}}$ along with output 1 dB compression point $P_{\mathrm{L,OP1dB}}$ are plotted in Fig. 5(a), and the measured PAE is plotted in Fig. 5(b). It can be seen from Fig. 5(a) that the maximum $P_{\mathrm{L,sat}} = 20.2\,\mathrm{dBm}$ and $P_{\mathrm{L,1dB}} = 19.4\,\mathrm{dBm}$ are obtained at a frequency of 10 GHz, and the small-signal gain at 10 GHz is 17 dB from Fig. 3(a). At mid-band, near 24 GHz, $P_{\mathrm{L,sat}} = 18.4\,\mathrm{dBm}$ and $P_{\mathrm{L,OP1dB}} = 17.1\,\mathrm{dBm}$. Also from the data in 5(a), the 3 dB power bandwidth is measured as 29 GHz from the frequency range of 3 GHz to 32 GHz. The measured maximum PAE of the design is 20.6% at 10 GHz, 13.3% at 24 GHz and the minimum of 9.8 % at the 3 dB frequency of 32 GHz. The power fractional bandwidth of a PA [6] is defined as, $PFBW = (PBW_{\mathrm{3dB}} \,/\, f_{\mathrm{c}}) \times 100\,\%$, where $f_{\mathrm{c}} = f_{\mathrm{u,3dB}} - (PBW_{\mathrm{3dB}} \,/\, 2)$, and $f_{\mathrm{u,3dB}}$ is the 3 dB upper cut off frequency. From Fig. 5(a), it can be seen that $PFBW = 156\%$ for the presented MOPA.

Table I shows the comparison with similar state-of-the-art PAs. It can be clearly seen that this work has the best *PFBW*, peak gain and lowest area. A modified international technology roadmap for semiconductors (ITRS) power amplifier figure of merit (FoM) is used to compare PAs in [6]. Here we are incorporating *PFBW* and area into the FoM for better comparison of multi-octave power amplifiers as shown in the footnote [a] of Table I. The $FOM_{\mathrm{MOPA}} \approx 407\,\mathrm{W\,(GHz/mm)}^2$ is the highest when compared to other PAs in Table I.

IV. Conclusion

A single stage integrated multi-octave power amplifier is implemented in a 0.13 µm SiGe-BiCMOS technology using a novel combination of resistive feedback to enable broadband input matching of low-ohmic, highly capacitive input impedances, and transistor stacking for high output power with better output transfer network efficiency across a wide frequency range. Measurement results show a maximum saturated output power level of 20.2 dBm, a peak PAE of 20.6% and a 3 dB power upper cut-off frequency of 32 GHz. To the knowledge of the authors, this design has one of the best reported FOM_{MOPA}, a modified ITRS figure of merit which includes the measured power fractional bandwidth of 156%, peak gain of 18.6 dB and area of $0.71\,\mathrm{mm}^2$.

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