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Exploration of Thin Films for Neuromorphic, Electrofluidic, and Magneto-Plasmonic Applications

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To the Graduate Council:

I am submitting herewith a dissertation written by Walker L. Boldman University of Tennessee Knoxville entitled "Exploration of Thin Films for Neuromorphic, Electrofluidic, and Magneto-Plasmonic Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

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Exploration of Thin Films for Neuromorphic, Electrofluidic, and Magneto-Plasmonic Applications

A Dissertation Presented for the

Doctor of Philosophy

Degree

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Walker Lee Boldman

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ABSTRACT

Due to the limit in computing power arising from the Von Neumann bottleneck, computational devices are being developed that mimic neuro-biological processing in the brain by correlating the device characteristics with the synaptic weight of neurons. We demonstrate a platform that combines ionic liquid gating of amorphous indium gallium zinc oxide (aIGZO) thin film transistors and electrowetting for programmable placement/connectivity of the of the ionic liquid. In this platform, both short term potentiation (STP) and long-term potentiation (LTP) are realized via electrostatic and electrochemical doping of the aIGZO, respectively, and pulsed bias measurements are demonstrated for low power considerations. Using a lithium-based ionic liquid, we demonstrate both potentiation (decrease in device resistance) and depression (increase in device resistance), and propose a 2D platform array that would enable a much higher pixel count via Active Matrix electrowetting. Fabrication and optimization of the aIGZO thin film transistors are then studied and optimized for integration into a 16x16 Active Matrix platform. Poly-silicon transistors are also explored as an alternative to aIGZO, and the behavior of these transistors are compared and contrasted with the aIGZO results.

Bimetallic alloys with large discrepancies in atomic radii and crystal structure typically yield systems that are highly immiscible, even at high temperatures. The Ag_xFe_{1-x} [silver iron] binary system has limited solid and liquid solubility and thus phase separated silver + iron alloys should result. Furthermore, silver has interesting plasmonic properties and iron is a strong ferromagnet, thus magneto-plasmonic nanoparticles/films should result

due to their phase separation. We have leveraged a combinatorial sputter deposition to synthesize thin films with a large Ag_xFe_{1-x} ($0.19 < x < 0.84$) phase space to correlate the composition and structure to the optical and magnetic properties for both as-deposited and annealed compositions.

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CHAPTER 1 - DEVELOPMENT OF THIN FILM TRANSISTORS FOR APPLICATION IN ACTIVE MATRIX ELECTROWETTING

Motivation and History

The development of thin film transistors (TFTs) started with the research of P.K. Weimer at RCA Laboratories in the 1960s [1]. His work stemmed from MOSFET development done by Brody, Lilienfeld, and Heil, where a three-terminal (source, drain, and gate) operated transistor was introduced [2], [3]. While they were originally developed to be used as a cheap logic source, it was the pairing of TFTs with the liquid crystal display in 1968 that caused the TFT to emerge as an important device technology [4]. Since then, TFTs have been applied to electronic displays such as computer screens, TVs, and phones, and are being developed for use in transparent, flexible, and wearable displays. Researchers around the globe have sought to improve device characteristics while striving to make TFTs smaller, thinner, cheaper, and faster.

Materials studied for the TFT semiconducting active layer includes silicon, metal oxide semiconductors, and polymers/organic semiconductor materials [5]–[10]. Before the 1970s, various materials were used as TFT active layers, with the most prevalent and explored being an evaporated cadmium sulfide (CdS) [11]. However, in 1979, LeComber proposed a structure based on a hydrogenated amorphous silicon (a-Si:H), desirable due to its high uniformity and on/off ratio (see Figure 1.1) [12]. Since then, a majority of TFTs used in modern consumer items use Si as the active layer, both in the a-Si:H form [13] and in a polycrystalline form (poly-Si) [14]. However, a recent need has arisen in

industry for the development of low to room-temperature fabricated TFTs for application in transparent and/or flexible displays. For this reason, work has been done in the development of amorphous Indium Gallium Zinc Oxide (aIGZO) TFTs, as they have high transparency (>80%), a field effect mobility on the order of 10-50 cm^2/Vs, and a relatively easy fabrication process [10], [15]. In this dissertation, we focus on the development and fabrication of poly-Si and aIGZO TFTs for the use in driving an Active Matrix Electrowetting lab-on-a-chip platform.

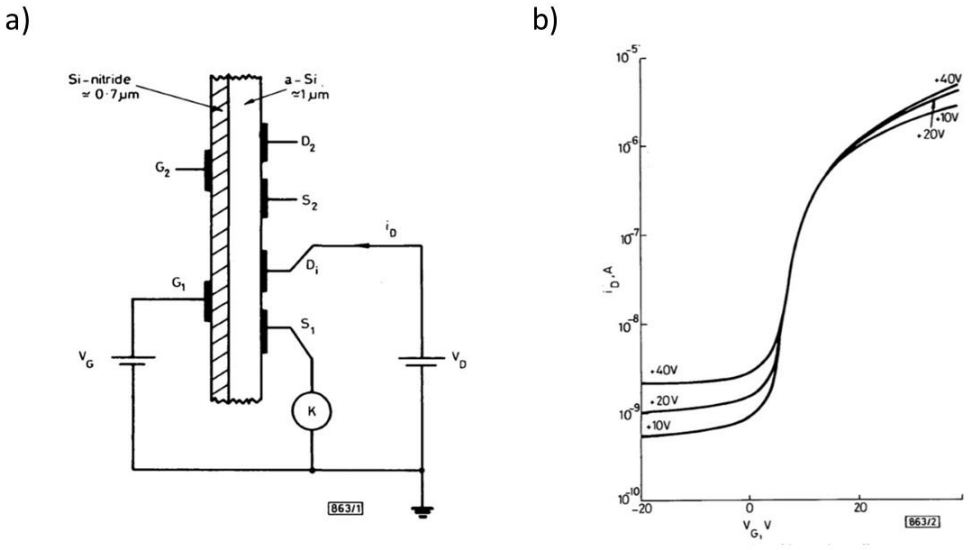


Figure 1.1. (a) Schematic diagram illustrating the design of the a-Si TFT and (b) the associated transfer characteristics (drain current I_d plotted logarithmically against gate voltage V_g for the given values of drain voltage V_d). Reproduced from [12].

TFT Operation and Structure

TFTs are a form of a field effect transistor (FET) that are fabricated by depositing thin layers of a semiconducting active layer, dielectric insulator, and metallic contacts over a non-conducting substrate. Metallic contact is made directly to the active layer via source and drain lines, sometimes mediated through a thin contact adhesion layer. After insulation of the active layer, a third line is patterned (the gate) that will influence the carrier concentration in the active layer via an induced bias. Figure 1.2 shows the band diagram for an n-type TFT under varying gate biases [16]. If a voltage is applied across the source/drain contacts without the presence of a gate bias, the device is highly resistive, or in the OFF state, as the device is in equilibrium. If a negative bias is applied to the gate (or a positive bias in the case of a p-type device), electrons would be repelled from the active channel, further inhibiting conduction across the region. However, if a positive bias is applied, electrons are attracted to the channel, resulting in a much lower state of resistance, thus turning the device ON.

In the development of TFTs, there are several structure types to consider, each with varying advantages depending on platform integration and fabrication process. Figure 1.3 details several of the more commonly used structures, including normal staggered (a), inverted staggered (b), bottom gate (c), and top gate (d). Classification of normal or inverted staggered is dependent on the ordering of the source/drain lines relative to the active layer. Patterning the active layer on top of the source/drain lines (normal staggered) can lead to issues in making ohmic contact between the active layer and electrodes, depending on the thickness of the active layer and the type of materials

used. More importantly, this structure could not be used for the development of poly-Si TFTs, as the crystallization temperature of Si is well above the melting point for most metals used as source/drain electrodes [17]. For this reason, the inverted staggered structure is more common, though issues can still arise in making ohmic contact depending on the source/drain thickness, as well as active layer degradation during the etch process of electrodes.

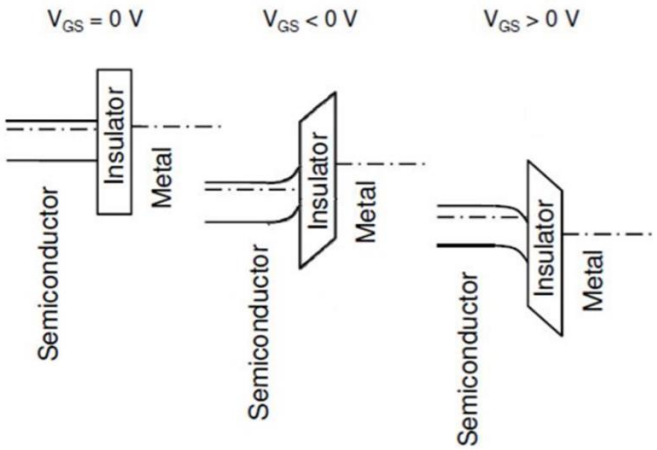


Figure 1.2: Energy band diagrams as viewed through the gate for several biasing conditions: equilibrium ($V_{gs} = 0$ V), $V_{gs} < 0$ V, and $V_{gs} > 0$ V. Reproduced from [16].

Classification of top and bottom gate is dependent on the ordering of the gate line relative to the active layer. Again, for the development of poly-Si TFTs, the bottom gate structure could generally not be used. However, for most metal-oxide and polymer TFTs,

the bottom gate structure is preferred in order to minimize TFT degradation during gate etching/patterning. In this dissertation, we will focus on the inverted staggered top gate structure for the poly-Si TFTs and the inverted staggered bottom gate structure for the aIGZO TFTs.

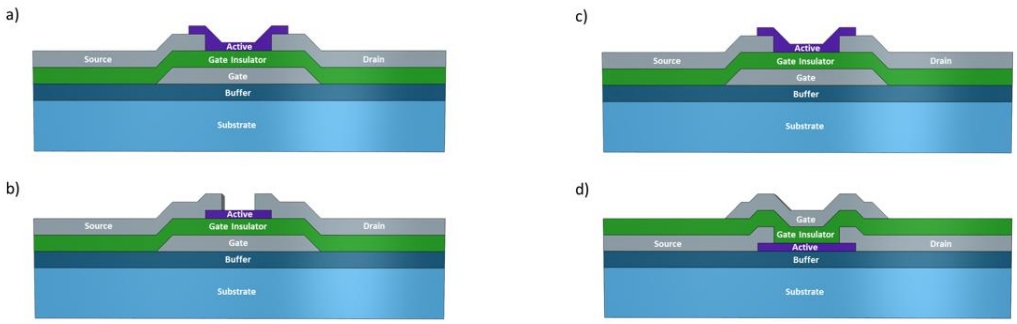


Figure 1.3: Cross-sectional diagrams of TFT structure types. (a) Normal staggered, (b) inverted staggered, (c) bottom gate, and (d) top gate.

Electrical Characterization of TFTs

In order to properly understand how a TFT functions and what parameters affect its performance, it can be helpful to delve into the general electrical characteristics of the device. Several important factors to consider are the subthreshold swing, threshold voltage (V_{th}), on/off ratio, and channel field effect mobility. A “simplified” version of the

current-voltage equations is presented in [18], where the relation between voltage and current are divided into three sections: the exponential, linear and the saturation regimes (see Figure 1.4 for graphical representation). A brief mathematical description of the linear and saturation regimes follows.

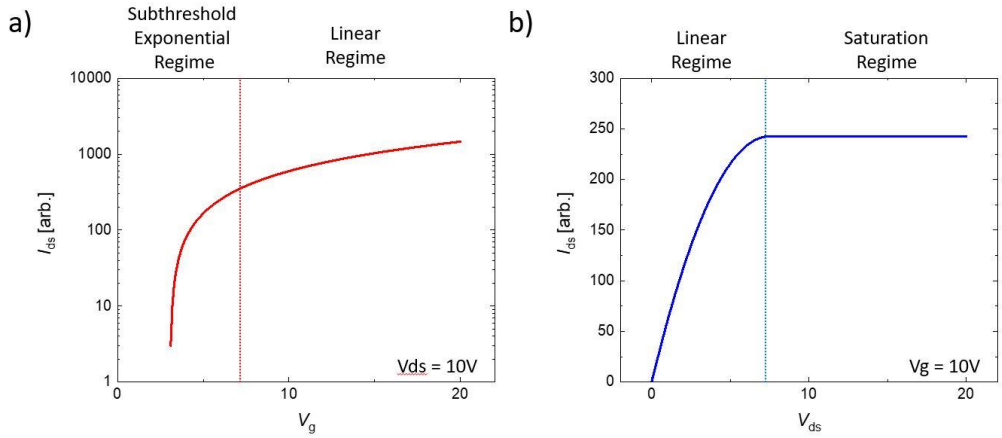


Figure 1.4: Graphical representation illustrating the linear, saturation, and exponential regimes in (a) transfer curve and (b) output curve.

Linear Regime

Defined where the source/drain voltage (V_{ds}) is less than the difference between the gate voltage (V_g) and threshold voltage ($V_{ds} < V_g - V_{th}$), the TFT current is determined to be given by

$$I_{ds} = C_{SiO_2}\mu_n \frac{W}{L}\left[\left(V_g - V_{TH}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right],$$

where C_{SiO2} is the capacitance of the gate insulator, μ_n is the field effect mobility, and W/L is the width to length ratio of the channel region. Here, mobility can be estimated using the equation

$$\mu_{AVG}(V_g) = \frac{LG_D^{LIN}(V_g)}{WC(V_g - V_{th})},$$

where G_D^{LIN} is the output conductance defined in the linear region as

$$G_D^{LIN}(V_g) = \left.\frac{I_d(V_g)}{V_{ds}}\right|_{V_{ds}\to 0}.$$

Threshold voltage is calculated in the linear regime, though the precise definition varies from source to source. However, one of the simplest and most widely used methods is to plot a straight line through the linear regime where the slope reaches a maximum, and then extrapolate that line through the x-axis (V_g).

Subthreshold gate swing (S.S.) is defined as the voltage required to increase the drain current by a factor of 10, as shown in the equation

$$S.S. = \frac{dV_g}{d\log_{10}(I_{ds})}.$$

For an optimal device, this should be less than 1 V/decade, and typical MOSFETs used in industry today have a value of around 70 mV/decade [19]. One major inhibitor of S.S. is trapped charges at the source/drain and active layer interface, which can greatly reduce device performance and switching speed. To counter this, promoting a pristine interface between layers was explored, as will be discussed in detail later.

Saturation Regime

Defined where the source/drain voltage is greater than the difference between the gate voltage and threshold voltage ($V_{ds} > V_g - V_{th}$), the current-voltage equation simplifies to

$$I_{ds} = \frac{1}{2} C_{SiO_2} \mu_n \frac{W}{L} (V_g - V_{TH})^2.$$

Graphically, the device has reached saturation when the current across the active layer cannot be increased as a function of further increasing gate voltage. Here, the important factor is the on/off current ratio, or

$$On/Off\ Ratio = \frac{I_d\,(on)}{I_d\,(off)}.$$

For an optimal device, this value should be greater than 10^6, with most industry MOSFETS being around $10^8 – 10^{10}$.

Electrowetting

Electrowetting on dielectric (EWOD) is a process that uses an applied electric field to modify the interface energy and wetting properties of a surface [20]; it has been used in many areas, including biosensing and other bio applications [21], [22], microlenses [23], fibre optics [24], and various display technologies [25]. When an applied electric field is applied to an electrode with an electrolyte droplet on top of it (and an adjacent electrode), the surface energy of the electrolyte/solid interface decreases, which increases the area of the droplet and the edges of the droplet proceed toward the neighboring electrode. This phenomenon is dependent on the various surface tensions of the system, the capacitance

of the interface, and the applied voltage to the system, and is governed by the Young-Lippmann equation, $\gamma\cos(\theta) = \gamma_{SV} - \gamma_{SL} + 1/2CV^2$, where θ is the wetting angle, γ_{SV} is the surface tension between the substrate and air (or oil), γ between the conductive liquid and air (or oil), γ_{SL} between the solid and conductive liquid, C is the capacitance per unit area, and V is the applied voltage (Figure 1.5). By directionally changing the contact angle, electrowetting can be used for droplet actuation/manipulation across a series of insulated electrodes, as illustrated in Figure 1.6. Control of droplet motion has opened the door for Lab on Chip [10], microscale chemical experiments [26], protein extraction [27], and even has allowed for some novel device platforms, such as a microscale conveyer system [28].

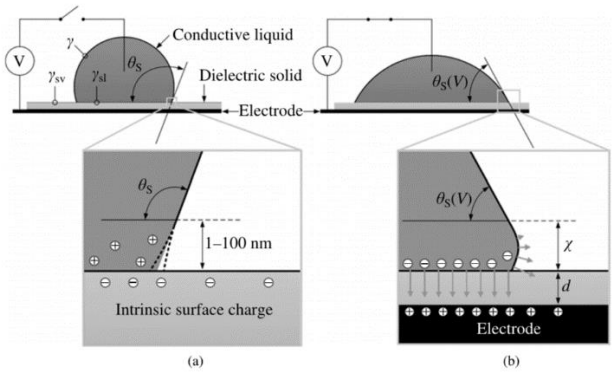


Figure 1.5**:** Schematic showing contact angle change of conductive liquid with (a) no voltage, and (b) under an applied voltage. Note that in (b) X is on the order of d, which is around 100 nm in many EWOD devices today. Reproduced from [20].

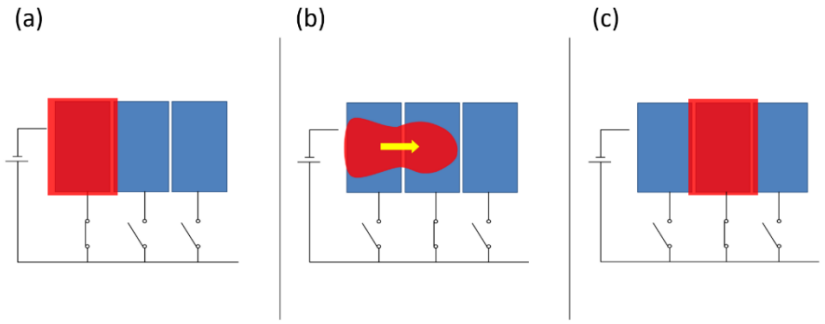


Figure 1.6: Schematic of droplet actuation. (a) voltage is applied to left pixel, causing the droplet to conform to the pixel's shape. (b) when a voltage is applied to the adjacent pixel, the contact angle of the conductive liquid changes, causing actuation across the pixel, until (c) the droplet covers the surface area of the applied voltage [image courtesy of Joo Hyon Noh].

Droplet actuation can be driven passively, where each electrode in the system is connected to a voltage supply and controlled separately, or actively by a process known as Active Matrix addressing. Active Matrix (AM) addressing uses thin film transistors (TFTs) to drive pixels via a row-column addressing scheme. Large scale passive matrix addressing can become very complicated to fabricate and difficult to control, which makes implementation of large-scale arrays unwieldy. Using AM addressing, an array of M x N pixels can be individually controlled by using only M + N electrodes, allowing a much higher pixel count while simplifying the fabrication and driving process as well. To this end, work has been done by several groups, including Noh et. al [10] and B. Hadwen et. al [29].

In [10], a 5x5 AM electrowetting array (Figure 1.7) was fabricated using thin film techniques, and low voltage electrowetting of ink was demonstrated. Electrical analysis of electrowetting signals was also conducted, and the optimal pulsing frequency and pulse width for effective AM electrowetting was determined based on the electrical properties of the TFT driving the pixels, the material type and thickness of the inter-dielectric layer, and applied gate voltage. A similar, but much larger scale device was developed by B. Hadwen et. al [29], where are 64x64 AM EWOD platform was used to perform actuation, splitting/merging, mixing, and impedance measurement of biological assays (Figure 1.8). AM electrowetting has also been used for driving liquid crystal displays [30].

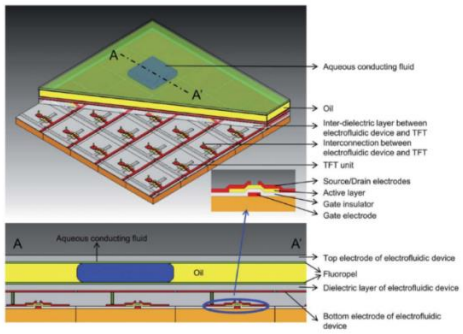


Figure 1.7: Schematic and cross-section of a 5x5 Active Matrix (AM) electrofludic device. In this device, each electrowetting pixel is controlled by a thin film transistor (TFT), which allows 25 pixels to be driven using only 10 electrodes. Reproduced from [10].

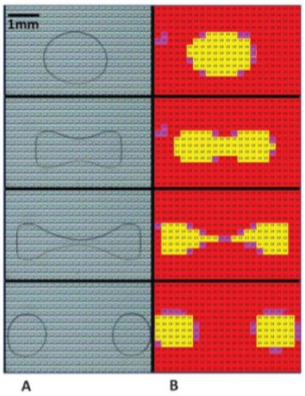


Figure 1.8**:** Droplet manipulation on the device, showing the splitting of a PBS droplet (550 nL) containing 0.1% Tween 20. a) Images, arranged vertically, were taken approximately 0.5 s apart. b) The corresponding portion of the impedance sensor images. Reproduced from [29].

Development of TFTs for Active Matrix Electrowetting Platform Application

For the application of TFTs in active matrix (AM) electrowetting, one of the most important factors to consider in the development of a TFT is its behavior as a series resistor in a voltage divider circuit (Figure 1.9). During the addressing of an AM electrowetting pixel, a pulsed voltage is applied across the source electrode of the desired pixel to be addressed. If this pulse is synchronized with a pulsed voltage across the gate electrode, then the pixel is turned "on," and the voltage is dropped across the drain electrode, or the "pixel." If, however, the source and gate voltages pulses are not in sync, then the pixel remains "off," and the voltage is dropped across the TFT. This total

resistance of the two series resistors is dependent on the resistance of both the TFT and the pixel,

$$R_{Total} = R_{TFT} + R_{Pixel}.$$

Here, R_{TFT} has two states, R_{ON} and R_{OFF}, corresponding to a pixel being turned on and off, respectively, and the voltage applied across the two series resistors will be dropped across the resistor with higher resistance. This voltage drop can be calculated by taking the applied voltage (V_{DS}) and multiplying it by the resistance ratio of the TFT to the total resistance, R_{Total}. For example, the voltage drop across the TFT in the on state is given by the equation

$$TFT\ Voltage\ Drop = V_D * \frac{R_{TFT}\ (on)}{R_{Total}}.$$

It is fundamental then that there be a clear distinction between the ON and OFF states at the pixel in order to promote electrowetting. In other words, the voltage applied across a TFT in the OFF state must be dropped across the TFT, and the voltage applied across a TFT in the ON state must be dropped across the electrowetting dielectric pixel. This can be achieved by modifying the electrical properties of the TFT such that the on and off state resistance envelope the electrowetting pixel resistance, namely through the materials selection and the active channel width/length ratio. In this dissertation, we focus on the development and improvement of both aIGZO and poly-Si as material selection, and how altering physical properties of these materials and devices affect their performance.

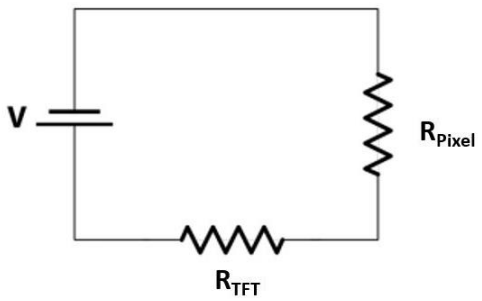


Figure 1.9: Series resistance in one AM electrowetting pixel, where the applied voltage (V) across a pixel is distributed between the resistance of the TFT (R_{TFT}) and the resistance of the drain electrode of the pixel itself (R_{Pixel}).

aIGZO TFT Materials Selection and Process Flow

For the fabrication of the aIGZO transistors, an inverted staggered bottom gate structure (Figure 1.3b) was chosen, and the devices were fabricated on 4" P/B <1-0-0> single side polished silicon wafers with a thermally grown 500 nm buffer oxide layer. Figure 1.10 and 1.11 show a modeled cross-section of a fabricated TFT and finished device, respectively.

Bottom Gate

For the bottom gate (Figure 1.10a), 150 nm of chromium was sublimated onto the wafer via electron-beam evaporation. Chromium was chosen as a suitable gate material due to its conductivity, thermal stability, and its high selectivity during fluorine plasma etching during via etching. Patterning of the chromium layer was achieved by optical

lithography and wet etching. For the deposition of the lithographic patterning layer, a photoresist primer was first spun onto the wafer at 3000 RPM for 45 seconds, followed by spin-coating of a positive photoresist SPR 2.1, also spun at 3000 RPM for 45 seconds. The wafer was then prebaked at 115 ºC for 60 seconds and allowed to cool. The wafer was then exposed at 90 mJ/cm^2 (~3.2 seconds) through an optical chrome mask and post baked at 115ºC for 60 seconds. After cooling, the wafer was developed in CD-26A for 60-90 seconds and inspected optically to ensure full development. This lithographic process is used multiple times throughout TFT fabrication and will be referred to as "patterned lithographically" to consolidate the process flow description. To wet etch the chrome, a diluted ceric ammonium nitrate and acetic acid mixture (22% $Ce(NH_4)_2(NO_3)_6$ + 9% CH_3COOH + 69% H_2O) was used, where the wafer was allowed to be fully immersed in the etchant until visibly fully etched (~3 minutes). Using a wet etch process is advantageous to a lift-off method for the bottom gate patterning as wet etching is an isotropic process, i.e., the etchant is non-directional. Because of this, sloped sidewalls were created, which allows for excellent step coverage of the gate dielectric and active layers. After the etchant was rinsed off, the wafer was sonicated in acetone for 5 minutes to strip the photoresist and clean the wafer.

Gate Insulator

Silicon dioxide (SiO_2) was chosen as our gate dielectric material (Figure 1.10b), as it has been widely used in many TFT devices and has good electrical characteristics, and performs well as an aIGZO gate insulator [10], [15]. For our devices, 100 nm of SiO_2 was deposited via plasma enhanced chemical vapor deposition (PECVD) under the

following conditions: 1000mTorr working pressure, 20 W RF power, 350 ºC working temperature, and a gas flow of 5% SiH_4 – Ar/N_2O (85/157 sccm). Under these conditions, deposition rate was calculated to be 69 nm/minute. While SiO_2 serves as the primary material chosen as a gate insulator, other materials (including Al_2O_3, HfO2, and SiN_x) are also explored in this chapter, as will be detailed later.

Semiconductor

As detailed earlier, a recent need has arisen in the semiconductor industry for a low to room temperature fabricated, transparent to semi-transparent semiconductor material for application in transparent, flexible, and wearable displays. Amorphous materials especially show promise in this field, due to their processing temperatures and high uniformity of device characteristics. However, field effect mobility of amorphous materials such as a-Si:H is extremely low, as it is limited by hopping between localized tail-states and strongly directed sp^3 orbitals [31]. However, amorphous metal-oxide materials (such as aIGZO) have been shown to have much higher mobility due to the formation of ns orbitals, where n is the principal quantum number 4-5. These orbitals create conduction paths through metal-oxide-metal bonds, as detailed in [32]. Because of this, and due to its transparent nature, several metal-oxides semiconductors, and in particular, aIGZO, have been studied and developed for application in display technologies. Table 1.1 details the electrical characteristics of several different types of active layer materials (including aIGZO), as well as the relative ease of fabrication. For the reasons listed above, and in this table, we have chosen to develop aIGZO TFTs for the application of AM electrowetting. Deposition of the aIGZO films (Figure 1.10c) was

carried out via magnetron reactive sputtering of a pressed powder 2” diameter aIGZO ($In_2O_3Ga_2O_3ZnO$=1:1:1) target in an Ar and O_2 gas mixture. The working pressure during sputtering was 5 mTorr with a 10% flow of O_2, and 80 W was applied via an rf power supply. The sputter rate at these conditions was found to be 1.4 nm/min, and a total of 50 nm was deposited. Patterning of the aIGZO films was done via photolithography and lift-off.

Table 1.1: Various electrical and physical properties of several frequently used active layers, demonstrating the benefits of aIGZO for AM TFT consideration. Reproduced from [15].

	Metal Oxide (a-IGZO)	a-Si	poly-Si	Polymer Organic
Field Effect Mobility (cm^2/Vs)	10~50	0.5~1	30~300	Up to 0.1
Process Temperature (℃)	<350℃	~350℃	>450℃	<150℃
Transparency (%)	>80	<20	<20	>80
Uniformity	Good	Good	Fair	Medium
Reliability	Low → High	Low	Medium/High	Low
Fabrication Difficulty	Easy	Easy	Difficult	Easy
(# of Mask layer)	5	5	(7~10)	(4~5)

Source/Drain Electrodes

While chromium was used as a bottom gate material and has shown good electrical behavior, it was not used here as source/drain electrode material. One necessary requirement for a properly functioning TFT is that it display a fast switching time, typically in the microsecond timeframe [16]. One inhibitor of this switching time is contact resistance between the active layer (here, aIGZO) and the source/drain electrodes. For this reason, a multilayer of titanium and gold (Figure 1.10d) was chosen, as titanium has been shown to promote contact adhesion and lower contact resistance [33], and gold is an excellent conductor and can thus support high switching speeds. 10 nm of titanium was sublimated via electron-beam evaporation, followed by 80 nm of gold, and then another layer of 10 nm thick titanium. All three layers were deposited without breaking vacuum to promote adhesion and to prevent oxidation/contamination of the gold. Patterning of the source/drain electrodes were done via photolithography and lift-off.

Gate Electrode Via Opening

In order to enable electrical characterization of the TFTs, via holes were etched in the SiO_2 insulator layer to allow probe contact. The patterning of this etch layer was done via photolithography and lift-off, and the etching of the contact hole was carried out in an RIE dry etch using an SF_6 + Ar gas chemistry.

Activation of IGZO

Typically, stoichiometric as-deposited IGZO is resistive, and requires an activation step in order to promote semiconducting behavior. The most commonly used

and simplest method is annealing, though there has been work done towards room-temperature activation for application in flexible substrates [34], [35]. For our TFTs, activation was achieved via annealing of the wafer for 1 hour at 200 ºC in ambient atmosphere.

At this point, electrical characterization of the fabricated pre-passivated TFTs can be carried out using a LabView program that sends and receives electronic signals to and from two Keithley 2400 source meters, the results of which are detailed and discussed later.

Passivation

In order to protect the TFTs against degradation, exposure to post processing procedures, and to allow the TFTs to be used in an active matrix electrowetting array, 100 nm of SiO_2 (Figure 1.10e) is deposited on top of the TFTs via atomic layer deposition (ALD). ALD deposited SiO_2 is advantageous to PECVD deposited SiO_2 due to its conformality, allowing for full step coverage and mitigating electrical breakdown of underlying layers.

Gate and Source/Drain Electrode Via Opening

To open the source/drain contact regions and to re-open up the gate contact region, an RIE dry plasma etch is again utilized, following the same procedure and patterning as described above for the gate contact via; namely, the etching of the contact hole was carried out in an RIE dry etch using an SF_6 + Ar gas chemistry.

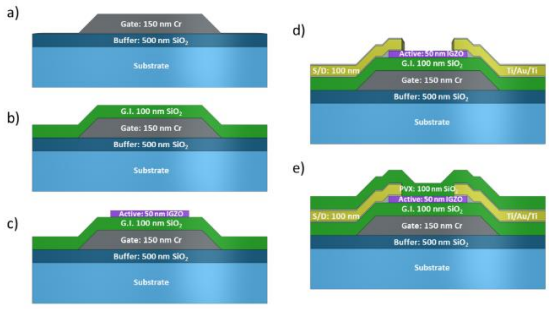


Figure 1.10: 2D cross-section detailing the process flow for aIGZO unit TFT. Here, 150 nm Cr was deposited as a bottom gate (a), 100 nm SiO_2 as a gate insulator (b), 50 nm of sputtered aIGZO as the active layer (c), 100 nm of e-beam evaporated Ti/Au/Ti as source/drain electrodes (d), and 100nm of SiO_2 as a passivation layer (e).

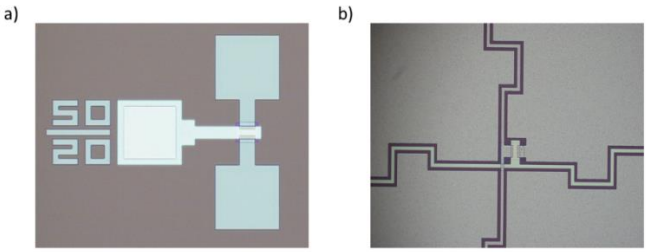


Figure 1.11: Optical micrograph of unit TFT with active layer width/length ratio of 50/20 µm (a), and incorporation of TFT into an active matrix EW platform.

Integration of IGZO TFT into 16x16 Active Matrix Electrowetting Array

Fabrication of a 16x16 Active Matrix Electrowetting array follows the flow described above, with only a few modifications. As detailed earlier, electrowetting consists of a bottom device and a top plate. For the bottom device, 150 nm chromium was deposited and patterned into row electrodes (gate) and passivated with 100 nm SiO_2. This passivation of the row electrodes also acts as the gate insulator. 50 nm aIGZO is then deposited as the TFT active layer. Next, 100 nm of Ti/Au/Ti is evaporated and patterned into source/drain TFT contacts and column electrodes in the EW array. In the EW array, a TFT is fabricated at the bottom left corner of each EW pixel such that the drain electrode of the TFT connects directly to the EW pixel. 100 nm SiO_2 is the deposited as the TFT passivation layer and electrowetting dielectric. Via holes are then opened to the unit TFT electrodes as well as the row/column electrode lines so that the device can be addressed. The array is then dip-coated in a hydrophobic solution (Fluoropel 1610V with 10 wt. % Fluoropel 1601V), allowed to dry in atmosphere for 1 hour, then baked at 175 ºC for 1 hour. For the top plate, 50 nm of ITO was sputtered onto a glass slide via a 3" $In_2O_3SnO_2$ target at 5 mTorr Ar working pressure with 30 W power. This top plate is then coated in a hydrophobic layer as described above. For the electrowetting process, ~80 µm spacers were used to separate the top and bottom plate, and a red ink (10 wt. % pigment with .01 wt. % sodium lauryl sulfate) EW droplet and an insulating oil (OS-30 Dow Corning) were infiltrated between the two plates.

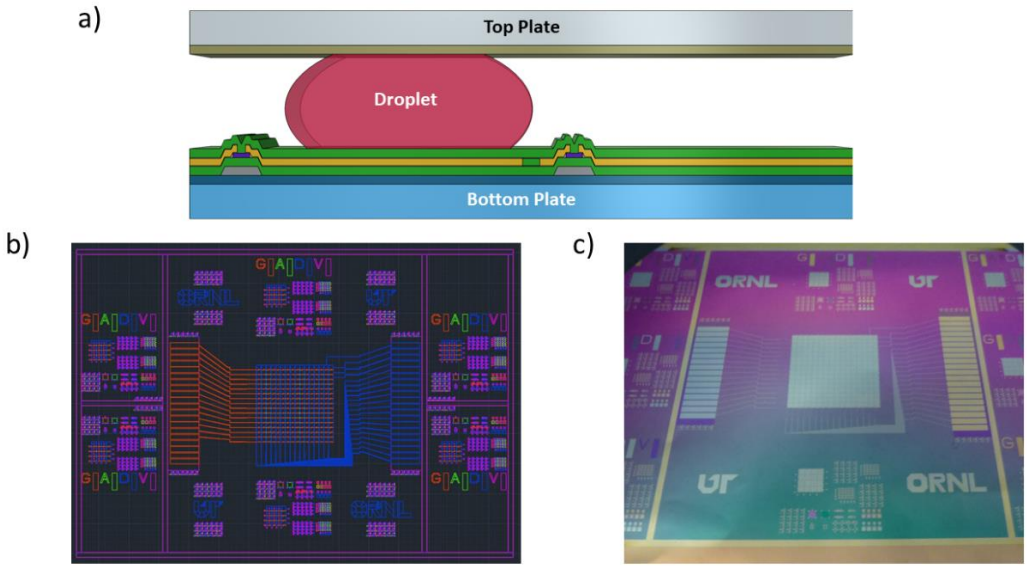


Figure 1.12: (a) 2D Cross-sectional schematic of EW configuration. (b) CAD design snapshot and (c) photograph of full 16x16 Active Matrix bottom plate.

TFT Electrical Measurements

Once fabrication of the device is complete, electrical measurements of TFTs around the device are taken to verify that the platform is functioning as desired. Figure 1.13 outlines these electrical measurements. A transfer curve of a typical TFT is taken (Figure 1.13a) to demonstrate switching of the device, and to measure the on/off ratio and the maximum on current for a given gate voltage. For the IGZO devices, gate voltage (V_g) is typically swept from -10 to 20 volts for incremental values of source/drain voltage (V_{ds}), with V_{TH} found to be ~3 V. Output curves are also taken (1.13b), where V_{ds} is swept from

0 to 20 V for incremental values of V_g, which shows saturation voltages as well as maximum on-current for a given source/drain voltage. This information then allows us to tune our AM parameters to ensure optimal driving parameters. To ensure consistent behavior across the 16x16 platform, TFT transfer measurements are taken at various points surrounding the EW platform (1.13c).

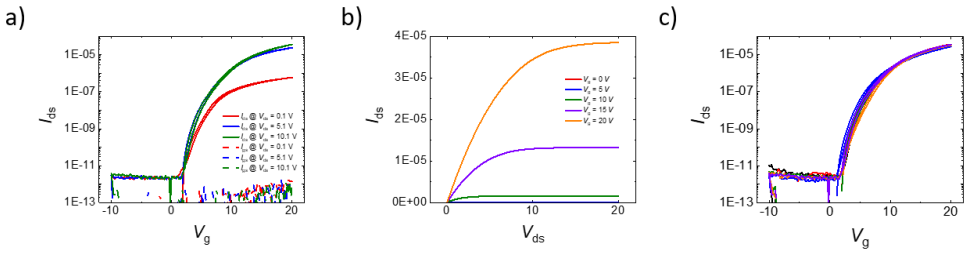


Figure 1.13: (a) Transfer curve of testing TFT (w/l ratio: 50/20) taken at V_{ds} = 0.1 V, 5.1 V, and 10.1 V. (b) Output curve of testing TFT for incremental Vg, and (c) six transfer measurements taken from six TFT structures located around the periphery of the EW platform.

Electrowetting Pixel Electrical Measurements

These electrical measurements determine if the device is capable of successful Active Matrix EW. As mentioned earlier, the integration of a TFT at each EW pixel creates a series resistance, and the way a voltage applied across this series is distributed depends

on the electrical characteristics of the TFT and EW dielectric in question. The resistance across the TFT depends upon gate biasing, and both the OFF state (V_g = 0 V) and the ON state (I_{ds} at V_g = ON, 20 V in this case) can be calculated by rearranging Ohms law

$$R = I/V,$$

where V is the applied voltage, *I* is the current measured, and *R* is the resistance. The resistance across the EW pixel is nominally a fixed value for a given voltage and was determined experimentally. 100 nm of ALD deposited SiO_2 was grown on top of a silicon wafer, and 100 nm of Ti/Au was then electron-beam evaporated and patterned into electrodes via lithography and lift-off, as illustrated in Figure 1.14a. Then, using the Si wafer as the one electrode, a series of I-V measurements were taken through the oxide, where the applied voltage was swept from 0 – 100 V (1.14b). Results show oxide breakdown around 75 – 80 V, which is well below the EW operating voltage (typically 30-50 V). In the range of 20-45 V and based upon the EW pixel dimension of 9.2×10^{-7} m^2, the resistance of the ALD oxide was found to be 13 M-ohms.

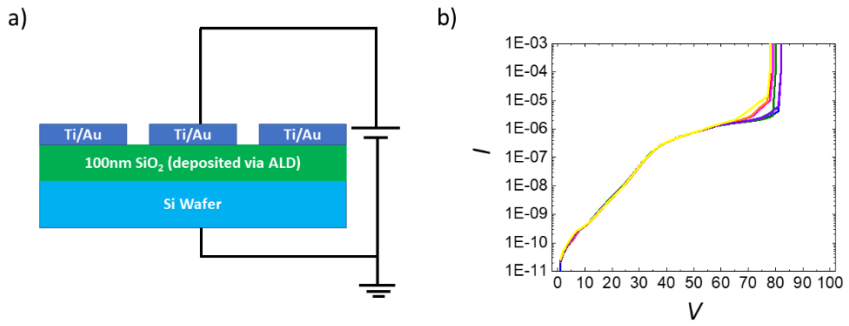


Figure 1.14: (a) 2D cross-sectional schematic demonstrating experimental setup, and (b) nine I-V measurements swept from 0 – 100 V taken across a 4” Si wafer.

If the TFT measured is too resistive, then the addressed EW pixel would not be able to turn ON, as the applied voltage would be dropped mostly across the TFT, even when under a positive gate bias. On the other hand, if the TFT is too conductive in the OFF state, then individual addressing of a single column would not be possible, as the voltage applied across a column would be dropped across the pixels, and not the TFT. It is therefore crucial to the development of Active Matrix EW that the driving TFTs display both a highly resistive OFF state (I_{ds} at V_g = 0 V) and a highly conductive ON state. Figure 1.15 plots percentage voltage drop at the TFT and at the EW pixel for various measured current/resistance values, where the ON current relates to voltage dropped across the pixel, and the OFF current relates to voltage dropped across the TFT. Here, the assumed EW pixel resistance is 2.6×10^7 ohms. As stated earlier, these results are dependent on channel width/length/thickness, applied voltage, dielectric material, etc.

Hydrophobic Layer Improvements

Another crucial component to successful electrowetting is a thin, uniform, and robust hydrophobic layer. The film needs to be robust, both resisting breakdown while under high electric fields, and maintaining hydrophobicity after aging or repeated use. At the same time, the film needs to be as thin as possible in order to promote a capacitance on the EW pixel, as most hydrophobic layers have low dielectric constants of ~2. There are

many factors that can affect the hydrophobic layer, including the material/materials used [36]–[41], the temperature, temperature ramp speed, and time that the solvent is baked [42]–[44], and the method by which the solvent is applied [10], [28], [45]–[47].

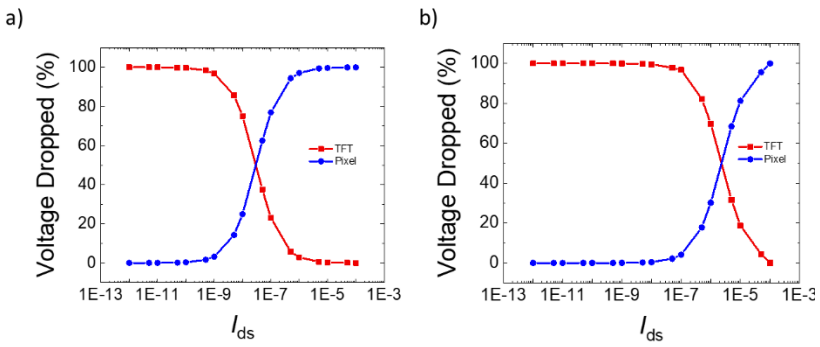


Figure 1.15: Plot demonstrating percentage voltage drop across the TFT-EW series resistors and its dependence on measured TFT current. Here, the EW pixel resistance for (a) is 1 giga-ohm and (b) is 26 megaohms. For both (a) and (b), a theoretical 30 V was applied across the series resistor.

Previously, a dip-coated layer of fluoropel was applied to the platform, was allowed to air dry for an hour, then baked at 180 ºC for one hour. The measured thickness was ~50 nm, and initially displayed good hydrophobicity. However, during electrowetting over an array of electrodes, the hydrophobic layer showed signs of non-uniformity and degradation, which caused the droplet to “stick” to areas where the hydrophobic coating

was thinner/non-existent. Figure 1.16 shows a series of snapshots taken of an EW video, which demonstrates the sticking of the red ink to the platform that wasn't fully coated in fluoropel. In this EW demonstration, a droplet was dispensed onto the bottom left side of the platform and immersed in oil (a). Then, using Active Matrix addressing, the droplet was actuated down (b). Because of the size of the droplet, all actuation addressing was done in a 2x2 pixel fashion in order to better control droplet motion. As is shown in image (b), the top right area of the droplet sticks to the bottom platform, and thus is not actuated towards the addressed pixels. Further downward addressing (c) resulted only in elongating the droplet and failed to move from the degraded area. Actuation to the left (d) and right (e) gave similar results.

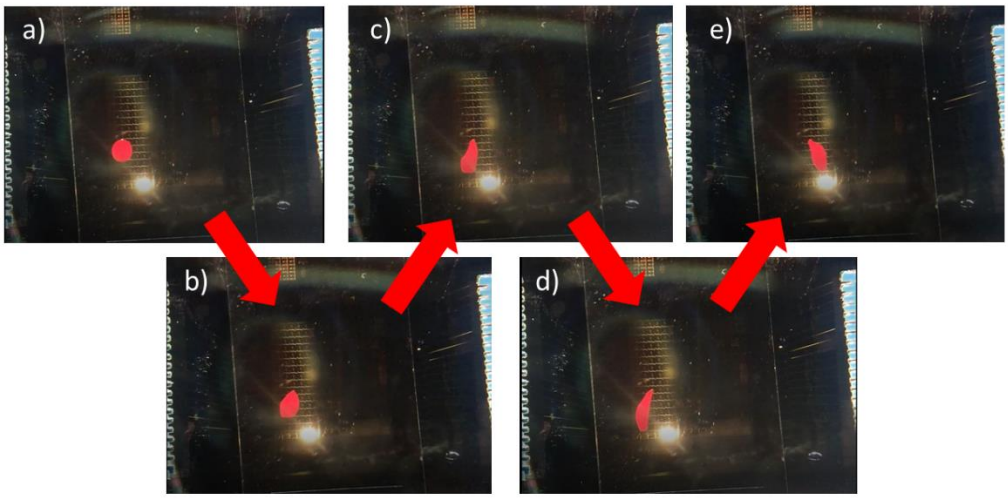


Figure 1.16: Snapshots of Active Matrix EW (a-e) demonstrating failure in hydrophobic layer.

To prevent further failure due to hydrophobic breakdown or other related issues, several alternative hydrophobic layers that have been successfully demonstrated in literature were explored for application toward our Active Matrix EW platform, including a spin-coated Teflon [48], spin-coated fluoropel [39], SU-8 [49], parylene [50], and an evaporated chlorotrimethylsilane monolayer [51]. To test the durability, robustness, hydrophobicity, and necessary driving voltages for each layer, a simple 1x8 EW pixel array was fabricated by sputtering 150 nm of chromium onto a silicon wafer with 500 nm SiO_2 buffer oxide (see Figure XX in ionic liquid EW platform for an optical image of the platform). The chromium was patterned into electrodes via lithography and lift-off, and passivated using 100 nm of ALD deposited SiO_2. For each device, a top plate with 50 nm of sputtered ITO was used and coated with the respective hydrophobic layer used for each study.

While parylene has been shown to be highly robust, easy to deposit, and often acts as both a hydrophobic layer and dielectric, the film thickness required to exhibit good EW behavior is often > 500 nm, as the deposition of parylene involves the measuring out and weighing of a solid, granular material. For our study, .5 g of parylene – C was weighed out and loaded into a parylene coating chamber, where the parylene was then vaporized and pyrolized, which cleaves the dimer gas into a monomeric form. This gas was then deposited uniformly on the ITO top plate and Active Matrix EW platform, and the final film thickness was measured to be ~400 nm. Because of the thickness deposited, successful EW of an ink required > 80 V DC, which is above both the TFT tolerance and

the dielectric failure of the ALD oxide. For this reason, parylene was abandoned as a viable alternative.

SU-8, an epoxy-based negative photoresist, was abandoned for similar reasons. While uniform films of < 100 nm can be reliably and repeatably deposited, these thinner films aren't nearly as hydrophobic as the explored alternatives, and thus still require high voltages in order to demonstrate successful actuation.

Chlorotrimethylsilane, or $(CH_3)_3SiCl$, is a colorless organosilicon compound, and is stable in the absence of water. When exposed to air, it will evaporate and form a superhydrophobic monolayer on any nearby surfaces. This method was explored for application to the Active Matrix EW platform, as a monolayer hydrophobic layer would both increase device capacitance and lower the required voltage necessary to drive EW actuation. However, during the EW demonstration, this layer reacted chemically with the water present in the ink droplet, as is shown in Figure 1.17 and as expected by the chemical equation

$$2\,(CH_3)_3SiCl + H_2O \rightarrow (CH_3)_3Si - O - Si(CH_3)_3 + 2HCl.$$

Figure 1.17: Hydrophobic layer breakdown due to hydrolysis of ink droplet and chlorotrimethylsilane monolayer.

Spin-coated Teflon has been shown to have good thickness control via spin speed, high reliability and hydrophobicity, and good uniformity across a 4" wafer. For our study, Teflon AF 1600 was dispensed onto the substrate, spun at 90 RPM for 10 seconds, and then at 900 RPM for 60 seconds. The substrate was then baked at 115 ºC for 15 minutes, 165 ºC for 15 minutes, and then 350 ºC for 30 minutes. During electrowetting, the droplet showed no signs of clinging to certain pixels or areas and achieved excellent actuation at low voltages. The hydrophobic layer showed no signs of degradation or breakdown, even after 20 cycles of droplet actuation. An electrowetting actuation speed test as a function of applied voltage is shown in detail in Chapter 2 of this dissertation.

Recovery and Control of Electrical Characteristics via Annealing

While optimal Active Matrix EW is dependent on a certain narrow range of TFT ON/OFF currents, as-deposited IGZO rarely falls within these bounds. Typically, an as-deposited sputtered film is resistive, and an annealing process is used to drive oxygen atoms out of the film, making the film semiconducting. However, the original state of the film, and thus the changes induced in the film, can be influenced by a wide variety of factors such as: age and quality of the sputter target, O_2 flow during sputtering, cleanliness of target shield and chimney, target voltage and current, and others. Some of these factors are non-controllable by the user and can thus introduce randomness into the final device results. However, we can at least partially maintain device characteristics across fabrication runs by controlling the device annealing process.

Here, we show two different fabrication runs where the final device characteristics were non-ideal, as the ON current was below that required to induce voltage drop across

the pixel in the ON state (refer to Figure 1.15). These devices were both fabricated according to the methods described above, with the exception that neither of these runs were passivated, but the final electrical characteristics (Figures 1.18 and 1.19) differed greatly from that of the previous run (Figure 1.13).

In Figure 1.18, we demonstrate control of device characteristics by annealing in atmosphere at 250 ºC for 2, 4, and 8 hours. For the 8-hour anneal, we see an increase in the ON current by over 2.5 orders of magnitude. However, hysteresis in the device characteristics were also increased, as well as a shift of V_{TH} to negative voltages and a substantial increase in the OFF current as well.

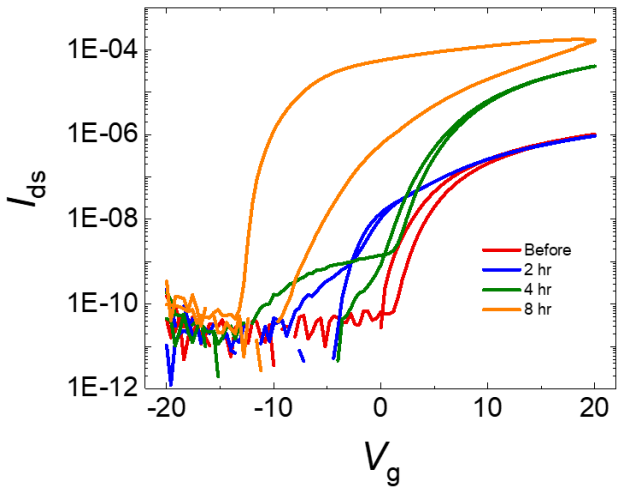


Figure 1.18: Transfer curves of IGZO TFT before annealing and after 2, 4, and 8 hours of annealing in atmosphere at 250 ºC.

Figure 1.19 shows device characteristics after 1, 4, and 9 hours after annealing at 250 ºC, and demonstrates a shift in the ON current of 3 orders of magnitude, and a shift in V_{TH} from 11 V to -5 V, pre-passivation. However, after 100 nm of SiO_2 was deposited via ALD and the devices were measured again, and there was a positive shift in V_{TH} and a slight decrease in the ON current as well.

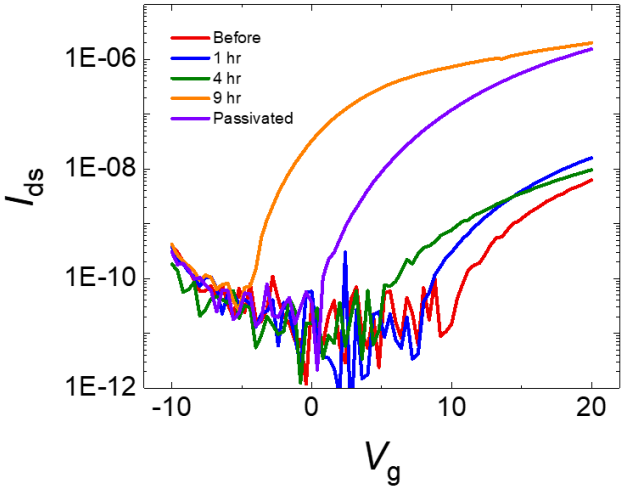


Figure 1.19: Transfer curves of IGZO TFT before annealing, and after 1,4, and 9 hours of annealing in atmosphere at 250 ºC, as well as a transfer curve taken after 100 nm SiO_2 passivation.

High-K Dielectric Passivation Study

Active Matrix addressing differs from Passive Matrix Addressing in that, rather than applying a constant voltage to the pixel to be addressed, a timed pulse is applied, with the voltage frequency dependent on the device characteristics and hardware limitations. The duty cycle is dependent on the number of rows in the platform, in this case, 1/16. In between cycles, the addressed pixel acts as a capacitor, storing the applied voltage until the next pulse cycle. Because of this, it is crucial that the pixel dielectric, the passivation layer, display fast switching time and a high capacitance. Capacitance is governed in a system by the equation

$$C = k\varepsilon A/d,$$

where C is capacitance, k is the dielectric constant of the insulator, ε is the permittivity of space, A is the area of the capacitor, and d is the thickness. In order to promote higher capacitance, the parameters that can be changed are 1) an increase in pixel size, 2) a decrease in passivation dielectric thickness, and 3) an insulator with a higher dielectric constant. While an increase in pixel area could be explored, due to the high pixel count involved and the desire to keep device size at a minimum to increase functionality, the necessary increase in pixel size would quickly become impractical. Decreasing passivation thickness could also not be explored due to issues in pixel step coverage, leaky dielectrics, and conformality issues. Because of this, hafnium dioxide was chosen for possible application for usage in Active Matrix EW, as the dielectric constant is 4-6 times higher than that of SiO_2 [52], and was recently explored for application to IGZO TFTs [53].

For this study, two wafers were processed together as described in the process flow, with one wafer passivated in 100 nm ALD deposited SiO_2 and the other passivated with 100 nm of ALD deposited HfO_2. TFT characteristics were measured before and after passivation (Figure 1.20). While the HfO_2 passivated devices showed slightly better characteristics after passivation, both sets of devices showed a significant decrease in the ON current and an increase in both hysteresis and V_{TH}.

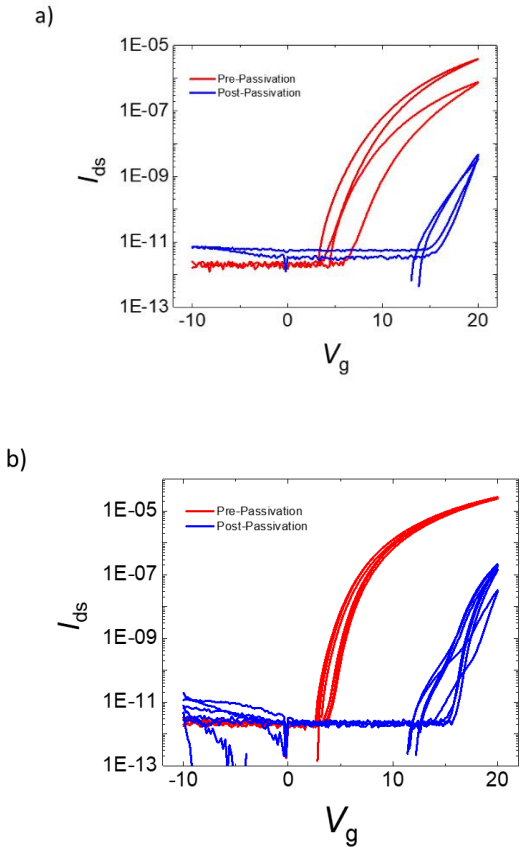


Figure 1.20: Transfer curves of IGZO TFTs with (a) 100 nm SiO_2 and (b) 100 nm of HfO_2, taken pre-passivation (red) and post-passivation (blue).

Passive Electrowetting on Sputtered Aluminum Pixels

In an attempt to decrease surface roughness of the EW pixel and to decrease contact resistance between the IGZO active layer and the source/drain contacts, an Active Matrix EW platform was fabricated with 150nm chromium back gate, 100 nm PECVD deposited SiO_2 gate insulator, 50 nm IGZO active layer, 100 nm of sputtered aluminum, and 100 nm of ALD deposited SiO_2. By using aluminum source/drain electrodes, a chemical wet etch could be used to pattern the electrodes, thus creating a sloped step interface at the pixel electrode boundaries, which should promote better EW actuation and prevent leakage through the dielectric. However, the aluminum etchant used during the source/drain patterning reacted chemically with the IGZO active layer, resulting in breakdown and etching of the active layer (Figure 1.21a). Another platform was fabricated similarly with 100nm of sputtered chromium as the source/drain layer and etched with a chromium etchant as described in the process flow, and optical images showed no visible breakdown of the IGZO active layer. However, during electrical measurements, the IGZO layer would short, causing electrical breakdown in the active layer and device failure (Figure 1.21b).

Because of the leaky passivation layer, Active Matrix addressing was not achieved due to a lack of capacitance over the EW pixels. However, using Passive Matrix addressing, actuation and droplet driving was possible. Passive Matrix addressing uses a constant DC voltage to address the desired pixels one at a time, rather than sending a pulsed voltage across the entire rows in sequence. In doing so, droplet actuation is no longer dependent on the capacitance of the dielectric, but rather only signal strength

(applied voltage) and the hydrophobicity of the platform. To demonstrate this, an EW platform was fabricated by depositing 150 nm Cr on a Si wafer with 500 nm SiO_2 buffer oxide, and patterning into a back gate via a wet etch process. 100 nm of PECVD SiO_2 was deposited as a gate insulator, and 50 nm of aIGZO was sputter deposited and patterned into a TFT active layer via lift-off. 100 nm of sputtered Al was deposited and patterned into source/drain electrodes via lift-off, and the device was passivated with 100 nm of ALD SiO_2.

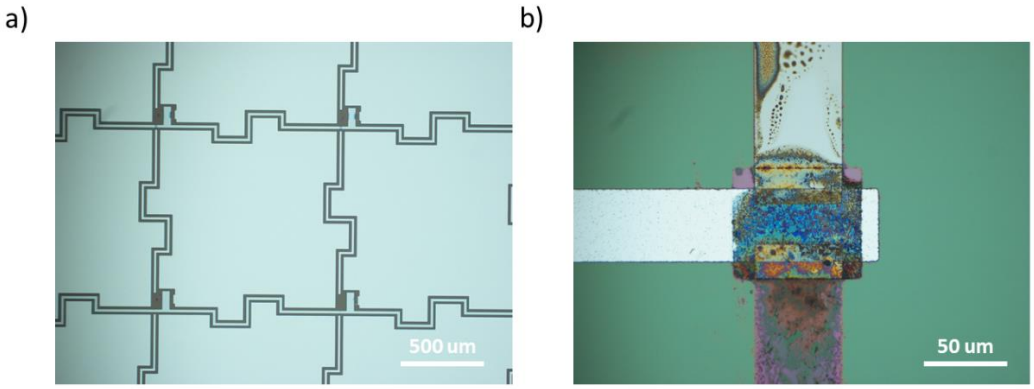


Figure 1.21: (a) Micrograph of Active Matrix EW platform, showing physical degradation of IGZO active layer after etching of aluminum electrodes. (b) Breakdown of IGZO TFT after electrical measurements were taken with wet-etched chromium source/drain electrodes.

After opening up the electrode contacts via an RIE plasma etch, the platform and an ITO coated top plate were both spin-coated in Teflon 1600 AF and cured as described above. The bottom platform and the ITO top plate were then separated with 80 μm microscope slides, and a yellow pigmented ink was infiltrated between the plates and was then surrounded in Dow Corning OS-30 oil. Then, starting at the bottom left corner of the 16x16 array, the yellow droplet was driven across the EW platform by individually addressing each pixel with 30 V applied to the gate electrode and 35 V applied to the source electrode through the commonly grounded ITO top plate. Figure 1.22 shows an image of the fabricated 16x16 array, where each pixel is highlighted in either green to signify successful EW or red to signify failure. Of the 256 pixels, 239 were able to successfully electrowet and drive the droplet, and the 17 failed pixels are attributed to unsuccessful patterning of an electrode line during the fabrication process.

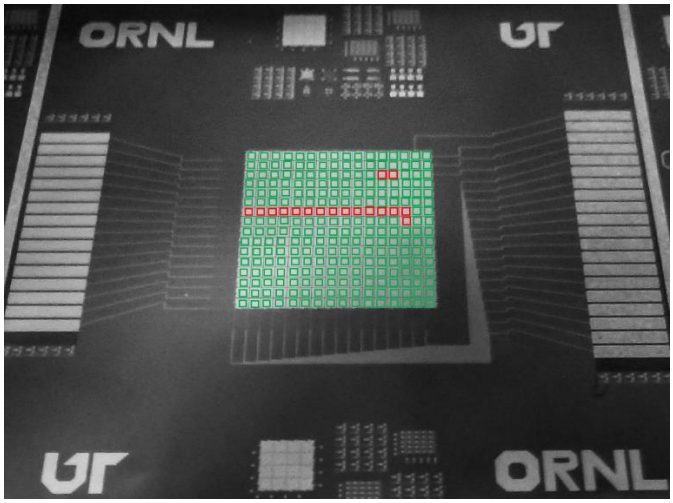


Figure 1.22: Photograph of fabricated 16x16 EW array, with each EW pixel highlighted in green (successful droplet actuation) or red (failed droplet actuation).

aIGZO Conclusion

Due to inconsistent device characteristics after fabrication, physical degradation of the IGZO active layer during etching of the source/drain layer and dampening of the electrical characteristics of the TFTs after passivation, IGZO was deemed to be ill-suited for development of TFTs for Active Matrix EW applications. Instead, our development of IGZO TFTs shifted to application of these TFTs into a programmable elecrofluidic neuromorphic platform, which will be discussed in Chapter 2.

Poly-Crystalline Silicon TFT Materials Selection and Process Flow

For the fabrication of the poly-crystalline silicon (poly-Si) TFTs, an inverted top gate structure (Figure 1.3d) was implemented, as the silicon active layer growth and activation temperature reaches > 900 ºC, which is above the melting temperature of most metals used for source, drain, and gate electrodes. These poly-Si TFTs were fabricated on 4" p-type (boron doped) <1-0-0> Si wafers with 100 nm of thermally grown buffer oxide. Figures 1.23 and 1.24 show a 2D cross-section of a fabricated poly-Si TFT and micrographs of the finished TFT structures, respectively.

Semiconductor

Due to its high carrier mobility, uniformity, and reliability, polycrystalline Silicon (poly-Si) can be used as the semiconductor layer in AM TFTs that require fast switching speeds and high applied voltages [54]. The limiting factor behind the application of poly-Si in electronic display technology lies in the high annealing temperature (>900 ºC)

necessary to form the polycrystalline grains. To this end, studies have been done showing low-temperature (< 500 ºC) formation of poly-Si via excimer laser annealing [55], metal-induced lateral crystallization [56], and others. In this dissertation, however, we grow on silicon wafers, so low temperature processing is not a requirement; thus, we show that, by using a top gate inverted staggered structure, we can grow poly-Si by via low pressure chemical vapor deposition (LPCVD) for application towards AM electrowetting TFTs.

For this study, two sets of poly-Si semiconductor active layers were grown at different thicknesses, in order to study the electrical characteristics' dependence on thickness. In the first set, 200 nm of intrinsic poly-Si was grown via LPCVD. In order to promote better source/drain electrode contact, a 50 nm layer of n-type Si was then grown on top of the intrinsic Si. This Si bilayer was then patterned into TFT active structures via an RIE plasma etch, and a channel etch was performed via the same process to create the active channel region. To reduce surface step height in the EW platform, a second set of wafers was fabricated with 50 nm of intrinsic Si was grown via the same process, 15 nm of n-type Si grown on top. Patterning of the active layer and channel were carried out in the same manner as above.

Activation of Poly-Crystalline Silicon

In order to further activate the LPCVD grown Si, a rapid thermal process (RTP) annealing was performed in order to promote further grain growth. Here, the silicon device wafer was loaded into an RTP chamber at room temperature, pumped down to $1x10^{-5}$ Torr, and then flooded with a nitrogen gas and held at 10 mTorr. The chamber temperature was then ramped to 950 ºC at 1.5 ºC/second and held at 950 ºC for 30

minutes. The wafer was then allowed to cool to room temperature and removed from the chamber.

Source/Drain Electrodes

Unlike the sputtered IGZO, poly-Si does not react when exposed to an aluminum wet etch, so aluminum was chosen as the source/drain material. However, to further reduce contact resistance at the source/drain and active layer interface, a sputtered aluminum doped with silicon was used. To deposit the aluminum, a 3" silicon-doped aluminum target (Al/Si, 99/1 wt%) was sputtered at 100 W at a working pressure of 3 mTorr. The sputtering rate was found to be 15 nm/min, and a total of 300 nm was deposited for the first wafer set (250 nm active layer) and 75 nm for the second (65 nm active layer). The source/drain electrodes were then patterned via lithography and a wet-etch bath in Al etchant. For the Active Matrix EW platform, since the drain electrode connects directly to the EW pixel, patterning the EW pixels via a wet-etch process rather than a lift-off method (as was done with the IGZO EW platform) created sloped pixel edges, which should promote EW actuation and better passivation step coverage.

Gate Insulator

As PECVD deposited SiO_2 performed well as a gate insulator for IGZO TFTs and was characterized previously, it was used as the insulator material for the poly-Si TFTs as well. As before, 100 nm was deposited via PECVD under the same working conditions as described in the IGZO TFT process flow. Note that because an inverted top gate structure was chosen, the gate insulator layer also acts as the EW pixel passivation/dielectric layer.

Gate Electrode

As the silicon-doped Al showed desirable electrical performance as a source/drain electrode and because it was able to be patterned via a wet-etch process with high selectivity to the underlying SiO_2, sputtered silicon-doped Al was also used as the gate electrode. Due to the selected fabrication structure, the Active Matrix EW gate lines run on top of the passivation layer, rather than underneath. Because of this, patterning the gate electrodes with a wet-etch process to create sloped sidewalls is necessary in order to promote droplet actuation over the gate lines. Deposition and patterning of the gate electrodes followed the same process flow as described above, but with 75 nm of silicon-doped Al being used for both wafer sets and patterned via wet-etch as described above.

Gate Electrode Passivation

Because the gate electrode lines were deposited and patterned on top of the passivation layer, another layer of insulating SiO_2 is necessary to insulate the gate electrodes. To this end, another 100 nm of PECVD SiO_2 was deposited as described above. To promote capacitance at the EW pixel, an RIE plasma etch was then used to etch out 100 of the 200 nm SiO_2 over each pixel area, though this step was later abandoned as it was shown to introduce leakage through the device.

Gate and Source/Drain Electrode Via Opening

In order to make metallic contact with the source, drain, and gate electrodes for electrical and EW testing, an RIE plasma etch was implemented to etch VIAs through the insulating layer, as is described in the IGZO process flow. At this point, electrical

characterization of the fabricated TFTs can be carried out using a LabView program that sends and receives electronic signals to and from two Keithley 2400 Source meters, the results of which are detailed and discussed later.

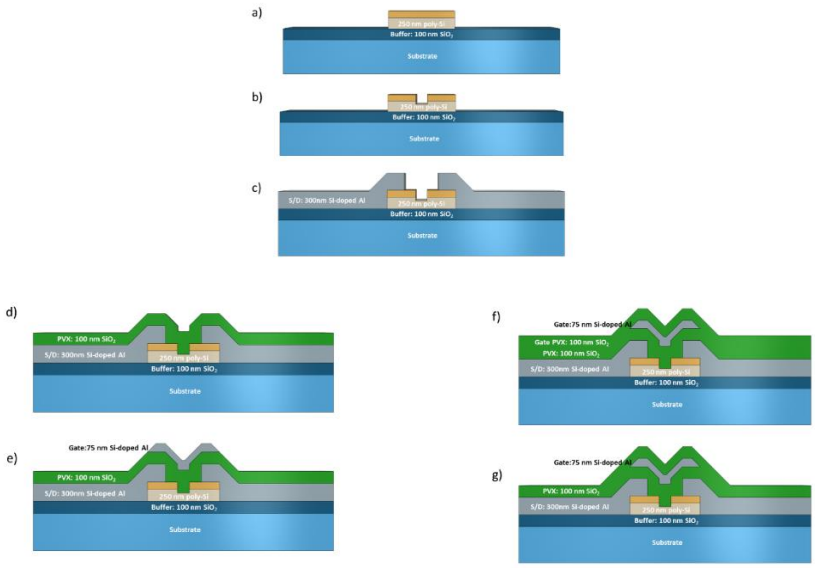


Figure 1.23: 2D cross-section model detailing fabrication process flow of poly-Si TFT, where 250 nm of poly-Si is grown (a) and patterned (b) as the active layer, 300 nm of silicon-doped Al was deposited as source/drain electrodes (c), 100 nm SiO_2 as the gate insulator (d), 75 nm of silicon-doped Al as the top gate (e), 100 nm of SiO_2 as the gate passivation (f), and finished TFT after 100 nm SiO_2 is etched away from the source/drain region (g).

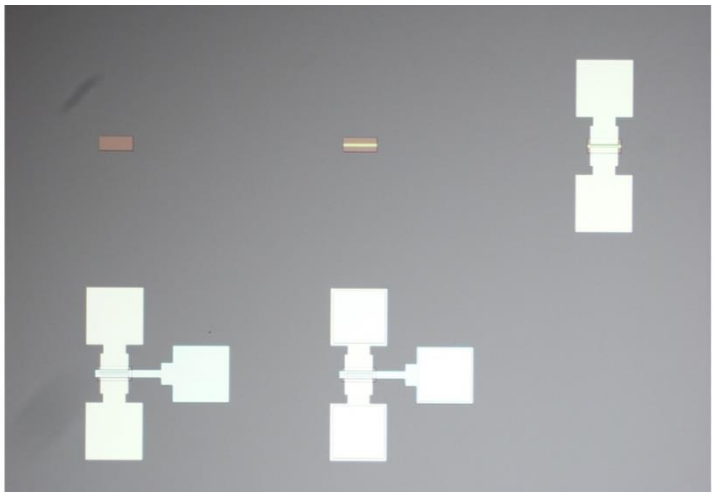


Figure 1.24: Optical image of poly-Si TFT during fabrication process. Deposition and patterning of active layer (top left), etching of active layer channel (top middle), deposition and patterning of source/drain electrodes (top right), deposition and patterning of gate electrode (bottom left), and etching of electrode VIAs (bottom middle). Channel length/width ratio is 10/100 µm.

Channel Width/Length and RTP Activation Study

For the development of the previously discussed IGZO TFTs, the channel dimensions and structure had already been decided upon based on work done by Joo Hyon [10] and Jiyong [15]. However, channel dimensions and structure for the poly-Si TFTs varied widely from source to source, and was dependent on silicon growth time, temperature, pressure, number of wafers processed at a time, and grain size, as well as activation method, time, and temperature. Because of this, a mask set was designed with an array of TFTs, with the channel width and length both ranging from 10 to 100 µm. The goal of

this experiment was to develop a channel length/width that satisfied the series resistance rule such that the voltage applied would be dropped across the TFT in the OFF state and dropped across the EW pixel in the ON state, as was discussed previously (Figure 1.15).

Fabrication of the TFTs followed that described in the process flow above, with the 250 nm active layer thickness being chosen. To measure the electrical properties of these devices, fabrication was only carried out to the deposition and patterning of the source/drain electrodes, and the silicon wafer was used to gate the TFTs. This was done because we were unsure as of yet as to the possible effects the top gate and gate insulator would play on the active layer and channel. Figure 1.25 outlines transfer characteristics taken from various channel width/length dimensions. Overall the devices showed minimal gate leakage (dashed lines), on/off switching under both a negative and positive gate bias (V_{ds} = 10.1 V). However, out of the TFT dimensions analyzed, we encountered one of two problems. First, for the longer, narrow TFTs (50-20 and 50-50) or the wider TFTs with longer channels (100-20 and 100-50), the OFF current of the device was satisfactory, but the ON current was limited. However, the shorter, wide TFTs (100-5 and 100-10) as well as the narrower TFT with a shorter length (50-10), the issue was quite the opposite, where we achieved a higher ON current, but saw a much higher OFF current as well. Both of these issues would inhibit Active Matrix EW.

Increasing the ON current was achieved simply by increasing the applied voltage to the TFT. To induce EW actuation of a standard yellow ink droplet, > 20 V needs to be applied, as is detailed further in Chapter 2. However, increasing the applied voltage would also induce a higher OFF state. To enable higher voltages to be applied while still

maintaining a low OFF state, TFTs were fabricated according to the methods describe above, but without any RTP annealing. This absence of a high-temperature activation step would result in smaller grain size, which in principle should increase device resistance, resulting in a lower OFF state. This is demonstrated in Figure 1.26, where transfer curves of the same channel lengths/widths of those in Figure 1.25 are taken, where V_{ds} is again 10.1 V. These poly-Si TFTs fabricated without an RTP activation step have an OFF current suitable for Active Matrix EW, and the improvement of the ON current is achieved by increasing the applied source/drain voltage and by increasing the channel width, as will be detailed later.

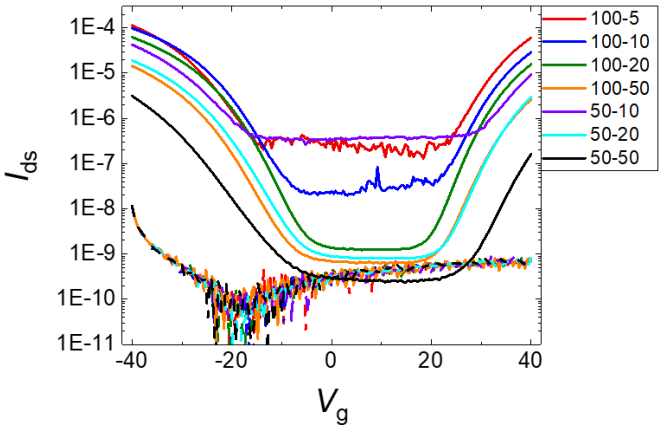


Figure 1.25: Silicon wafer-gated transfer curves for various active layer channel width/length ratios. V_{ds} = 10.1 V. The dashed lines are the measured source-to-gate leakage currents.

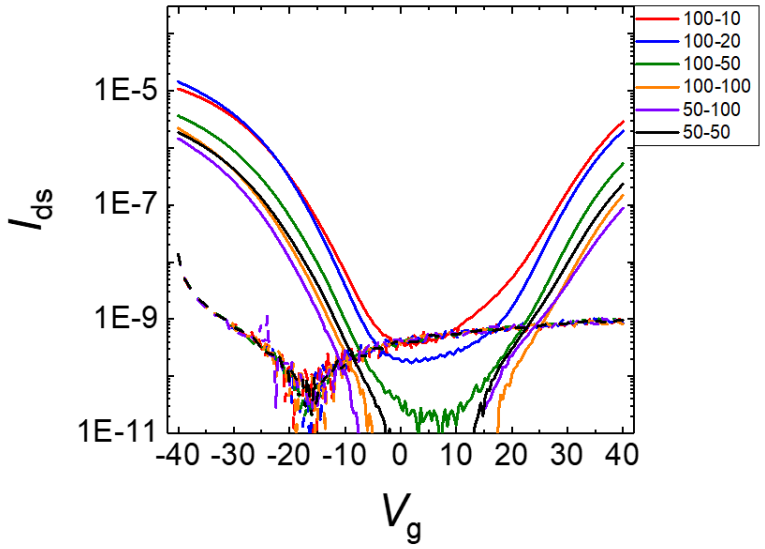


Figure 1.26: Silicon wafer-gated transfer curves for various channel length/width ratios fabricated without an RTP annealing. V_{ds} = 10.1 V. The dashed lines indicated gate leakage.

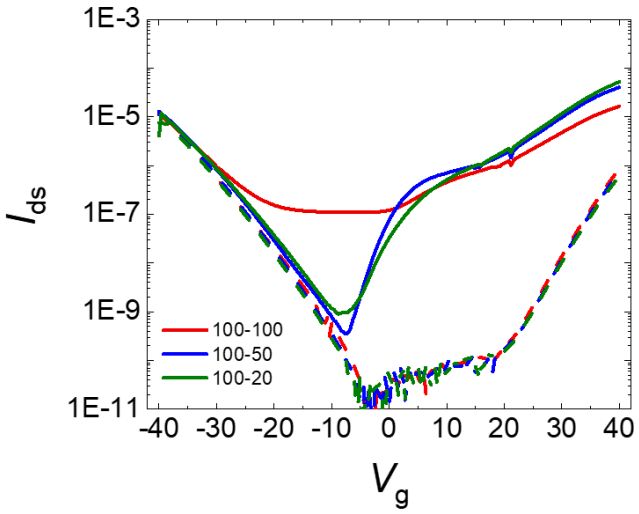
High-K Dielectric Poly-Si TFT Fabrication and Characterization

In order to decrease device switching time and to increase device capacitance, several high-k dielectric devices were fabricated and studied, including silicon nitride (SiN_x) and hafnium oxide (HfO_2). To fabricate the devices, 72 nm of poly-Si (54 nm of intrinsic Si and 18 nm of n-type Si) was patterned into TFT active layers with a 30 nm channel thickness on silicon wafers with 100 nm of thermally grown SiO_2 buffer oxide. Source/drain contacts were deposited via sputtering of 140nm Si-doped Al and patterned via lithography and a wet etch. For the gate dielectrics, 100 nm of SiN_x was deposited via

PECVD for one wafer, and 80 nm of HfO_2 was deposited via ALD on the other. Top gate electrodes were deposited via sputtering of 140 nm of Si-doped Al and patterned via a wet etch, and electrode VIAs were opened with an RIE sputter etch. Both wafers were then annealed at 200 ºC for 1 hour in vacuum (< $1x10^{-6}$ Torr) to promote contact adhesion.

While both devices showed both an increase in ON current and faster switching times, neither device was found to be suitable for Active Matrix EW due to other issues. For the SiN_x gated devices (Figure 1.27a), the deposited PECVD nitride was found to be extremely porous and leaky, resulting in a higher OFF current, erratic switching behavior, and very high gate leakage (indicated by the dashed lines). Both the high OFF current and the high gate leakage would inhibit accurate addressing of EW pixels, and thus would was not pursued as a viable option. For the HfO_2 gated devices (Figure 1.27b), the deposited ALD oxide had excellent conformality, resulting in very low leakage and fast switching times. However, the threshold voltage shifted from 10 V for SiO_2 gated devices (Figure 1.26) to -25 V, resulting in a much higher OFF current, which again, would greatly inhibit Active Matrix EW. It should also be noted that physical device failure was observed at V_g > 30 V. For these reasons, 100 nm of PECVD deposited SiO_2 was chosen as the most suitable dielectric for Active Matrix EW TFT application.

a)



b)

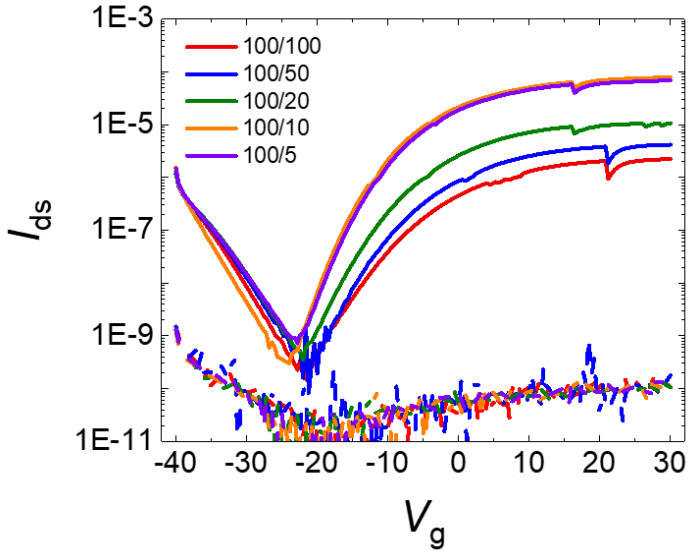


Figure 1.27: Top-gated SiN_x (a) and HfO_2 (b) poly-Si TFTs for various channel length/width ratios. V_{ds} = 10.1 V. The dashed lines indicate gate leakage.

Optimization of Poly-Si TFTs for Active Matrix EW

After optimization of the TFT materials and fabrication process, a detailed study was carried out in order to optimize TFT dimensions and layouts. In order to further increase the ON state current, TFT channel width was increased to up to 500 µm with TFT widths of 100, 150, 200, 300, and 500 µm, and channel length was decreased to 5 µm.

To fabricate the devices, 60 nm of poly-Si (48 nm of intrinsic Si and 12 nm of n-type Si) was patterned into TFT active layers with a 10 nm channel thickness on silicon wafers with 100 nm of thermally grown SiO_2 buffer oxide. Source/drain contacts were deposited via sputtering of 140nm Si-doped Al and patterned via lithography and a wet etch. 100 nm of PECVD SiO_2 was then deposited as a gate dielectric, and top gate electrodes were deposited via sputtering of 140 nm of Si-doped Al and patterned via a wet etch, and electrode VIAs were opened with an RIE sputter etch. The wafer was then annealed at 400 ºC for 30 minutes in vacuum (< $1x10^{-6}$ Torr). Transfer curves were then run at V_{ds} = 10.1 V and V_{ds} = 40 V in order to calculate voltage drop during Active Matrix EW.

Source/Drain and Gate Electrode Overlap

In order to understand the effects of parasitic capacitance (capacitance between the source/drain and gate electrodes) in the TFTS, an array of TFTs was designed with where the horizontal spacing between the source/drain and the gate electrodes were designed with a 10 µm overlap (Figure 1.28a), no overlap (1.28b) and a 10 µm gap (1.28c). This parasitic capacitance can limit ON current and lower the subthreshold swing, resulting in a slower switching time [18]. This effect can be seen in Figure 1.29a (V_{ds} = 10.1 V) and 1.29b (V_{ds} = 40.1 V), where, as the electrodes are moved from overlapping to a flush

configuration, both the ON current and the subthreshold swing increases. When the electrodes are further separated from a flush configuration to a gap, there is no further improvement in device behavior. Transfer curves were taken for several channel width/length ratios, including 100/5 (red), 150/5 (blue), 200/5 (green), and 300/5 (orange).

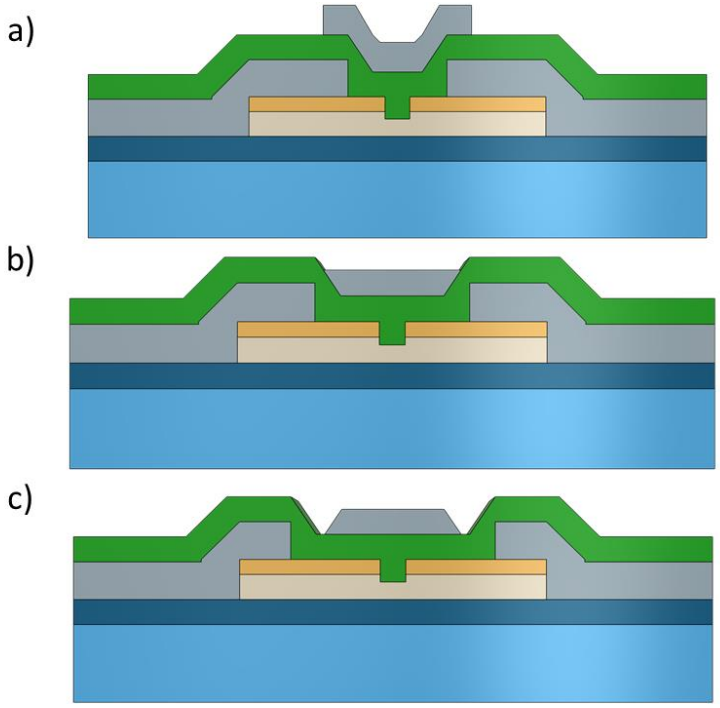


Figure 1.28: 2D cross-sections of Poly-Si TFTs, where the horizontal overlap between the source/drain and gate electrodes are (a) overlapped by 10 µm, (b) flush, and (c) separated by 10 µm.

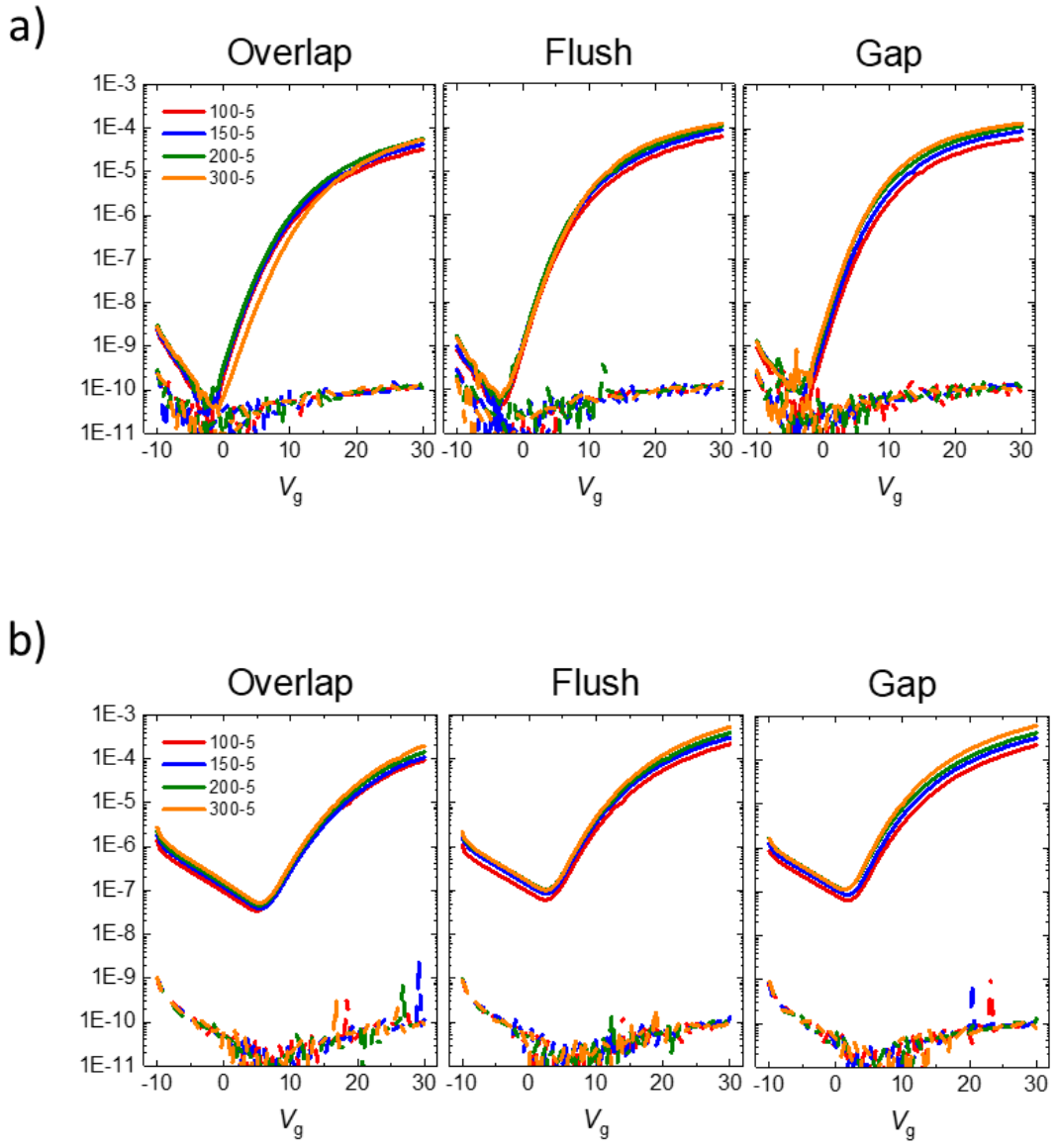


Figure 1.29: Transfer curves detailing shift in ON current and increase in subthreshold swing as horizontal spacing between source/drain and gate electrodes increases from overlap (10 µm overlap) to flush (no overlap) to gap (10 µm separation). V_{ds} for (a) was 10.1 V and (b) was 40.1 V.

Gate Electrode and Active Channel Region Overlap

To understand the role that the gate line width plays in the electrical characteristics, an array of poly-Si TFTs were designed such that the width of the gate line relative to the active channel varied from a 10 µm overlap (Figure 1.30a), a 1 µm overlap (1.30b) and no overlap (1.30c). Increasing the gate width relative to the active channel would promote gating of the n-type Si contact layer, increasing subthreshold swing, which would increase switching speed. This is seen in Figure 1.31, where, as the gate line is increased from flush to a 1 µm overlap, the subthreshold swing increases. Further increasing this overlap from 1 to 10 µm both increases the switching speed and the ON current for both low (V_{ds} = 10.1 V, 1.31a) and high (V_{ds} = 40.1 V, 1.31b) voltages. Transfer curves were taken for several channel width/length ratios, including 100/5 (red), 150/5 (blue), 200/5 (green), and 300/5 (orange).

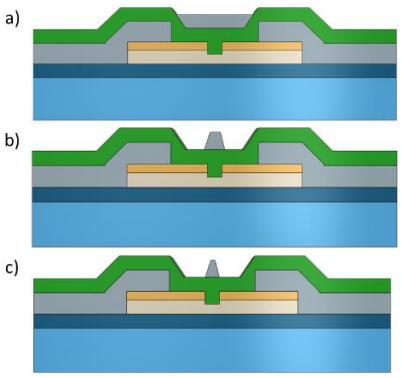


Figure 1.30: 2D cross-sections of Poly-Si TFTs, where the gate width relative to the active channel region (a) overlaps by 10 µm, (b) overlaps by 1 µm, and (c) is equal to the channel width.

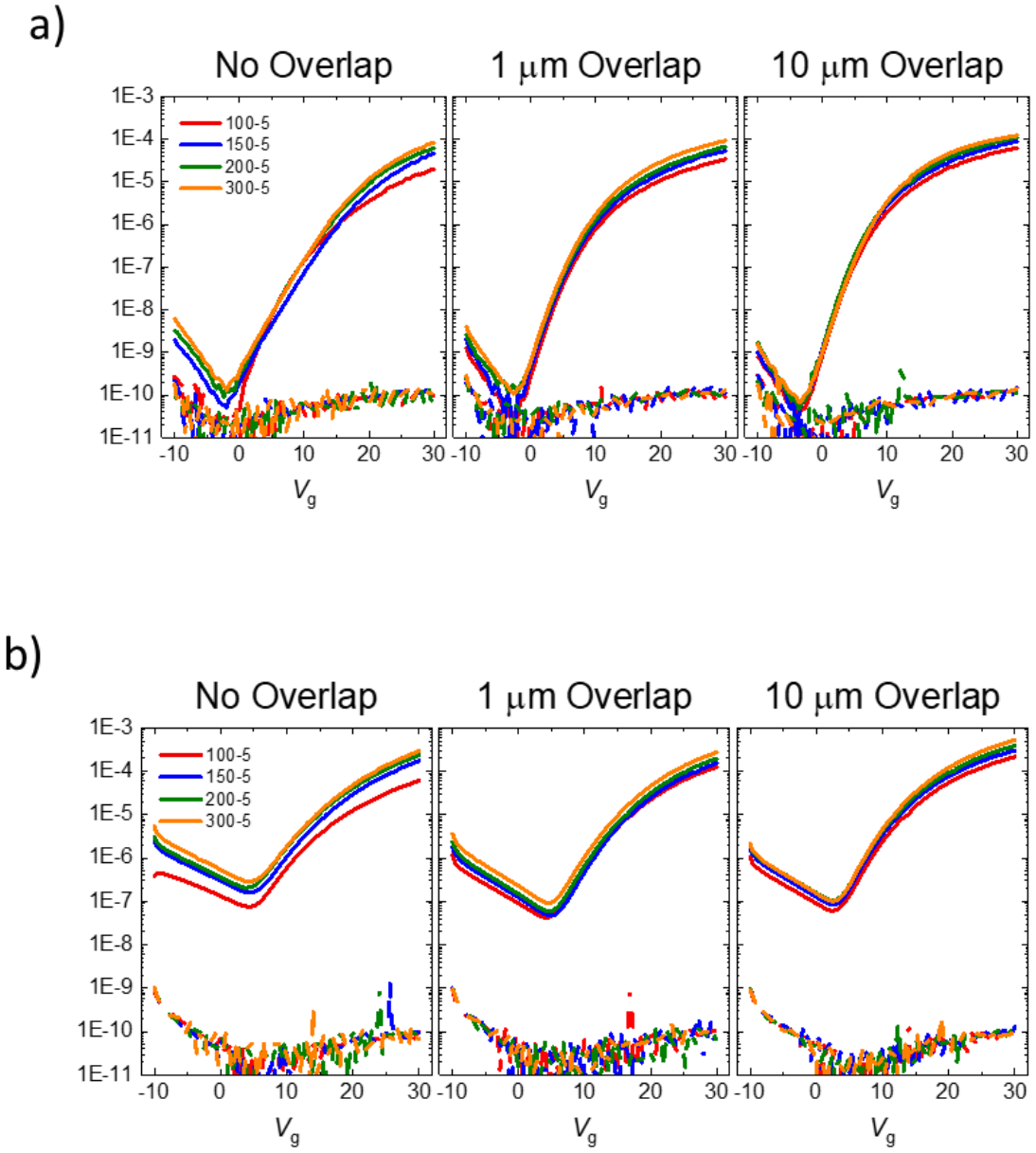


Figure 1.31: Transfer curves detailing increase in subthreshold swing as gate electrode width increases from equal to active channel width, 1 μm overlap, and 10 μm overlap. V_{ds} for (a) was 10.1 V and (b) was 40.1 V.

4x4 Active Matrix EW Pixel Analysis Array

While most electrical characterization of the Active Matrix EW is done via fabricated periphery TFTs (see Figure 1.12), characterization of the EW array itself was necessary in order to troubleshoot and improve device design. To this end, a 4x4 array of EW pixel was fabricated (Figure 1.32) so that electrical characterization could be done on a probe station, rather than Arduino driven. VIA holes were also etched into the center of each EW pad so that transfer characteristics and device leakage could also be tested. To fabricate the devices, 60 nm of poly-Si (48 nm of intrinsic Si and 12 nm of n-type Si) was patterned into TFT active layers with a 32 nm channel thickness on silicon wafers with 100 nm of thermally grown SiO_2 buffer oxide. Active channel width/length ratio was chosen to be 300/5 based electrical results shown in the previous section. Source/drain contacts were deposited via sputtering of 140nm Si-doped Al and patterned via lithography and a wet etch. 100 nm of PECVD SiO_2 was then deposited as a gate dielectric, and top gate electrodes were deposited via sputtering of 140 nm of Si-doped Al and patterned via a wet etch, and electrode VIAs were opened with an RIE sputter etch. The wafer was then annealed at 400 ºC for 30 minutes in vacuum ($< 1x10^{-6}$ Torr).

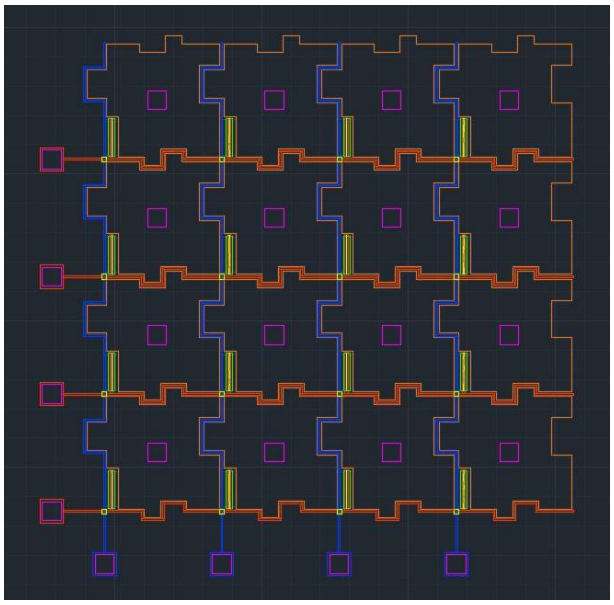


Figure 1.32: Snapshot of 4x4 EW troubleshooting array with VIA openings (purple boxes) in the center of each pixel.

In this troubleshooting array, several tests were done to determine the validity of the Active Matrix design and fabrication. First, a series of transfer curves was taken across the array to determine uniformity, as fabrication flaws, dust/photoresist/metal particles, or design faults could result in voltage drop across either the source/drain or gate lines. Figure 1.33 shows transfer curves taken across the 4x4 array (V_{ds} = 30.1 V), starting at the bottom left corner and working at a diagonal to the top right corner. While there is slight variation across the array, the EW behavior of the array would not be affected by these discrepancies. In order to determine the uniformity across a full 16x16 array, 4 of these fabricated troubleshooting arrays could be situated at the corners of the

full array, and uniformity across these 4 arrays would indicate uniformity across the EW platform.

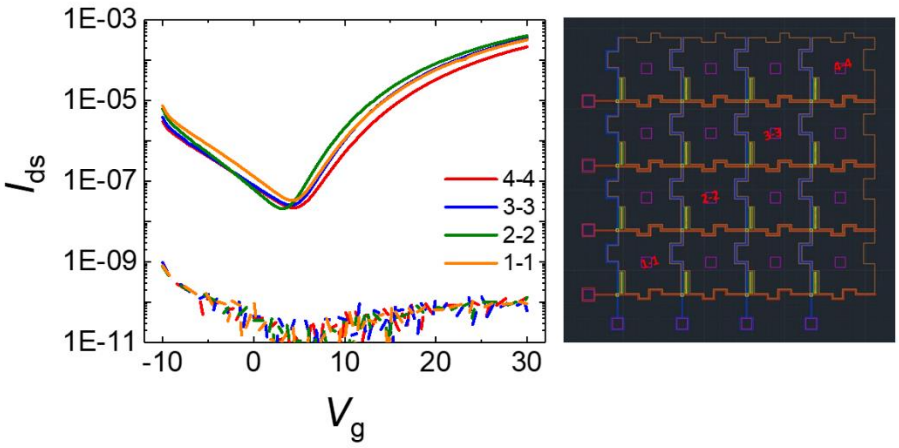


Figure 1.33: Transfer measurements from four EW pixel (shown on right) detailing platform uniformity. V_{ds} = 30.1 V.

In the fabricated Active Matrix EW platform, the source/drain and gates electrodes overlap at each pixel corner, resulting in 256 overlap locations. Each of these overlap areas could result in voltage shorting due to poor step coverage, a leaky or porous dielectric, or parasitic capacitance. In order to affirm that there is no crosstalk or current leakage across this array, a series of two probe measurements were taken at various points in the troubleshooting array (Figure 1.34). In this experiment, each combination pairing of source, gate, and drain electrodes was analyzed by applying a 10 V voltage

across the pair for 100 seconds while measuring current (I_{ds}). Note that values below $1x10^{-11}$ amps are beyond the instrument sensitivity used, and are thus not plotted. From the results plotted, it is evident that there is no crosstalk or leakage across the EW platform.

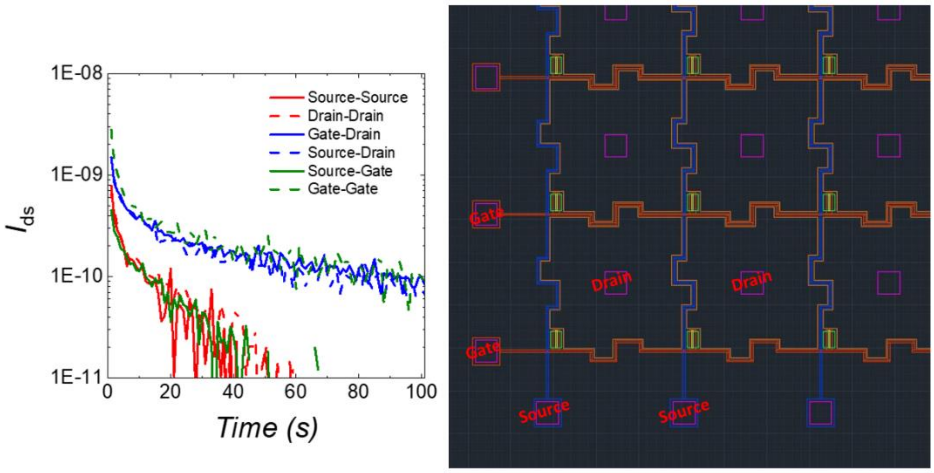


Figure 1.34: I-V measurements taken from each two probe combination of source, drain, and gate VIAs.

Active Matrix Electrowetting

After electrical analysis and characterization of the EW platform, Active Matrix addressing and droplet actuation was attempted on a full16x16 array. The Active Matrix EW platform was fabricated in the same manner as the 4x4 array described, and a glass

slide with 50 nm of sputtered ITO was fabricated as a top plate. Both the EW platform and the ITO top plate were then dip-coated in fluoropel, allowed to dry in ambient for one hour, and then baked at 175 ºC in ambient for one hour. The bottom platform and top plate were separated with 80 µm spacers, and an OS-Corning 30 insulting oil was infiltrated in the gap (see Figure 1.12a). To drive the platform, a software program (Figure 1.35a) developed by collaborators at UC Riverside sends signals to an Arduino board (b), which translates those signals to 5 V pulses, which are sent to a breadboard (c). These pulses are then amplified to the desired EW voltage by two Keithley 2400 source meters (d) and are applied to the EW platform (e).

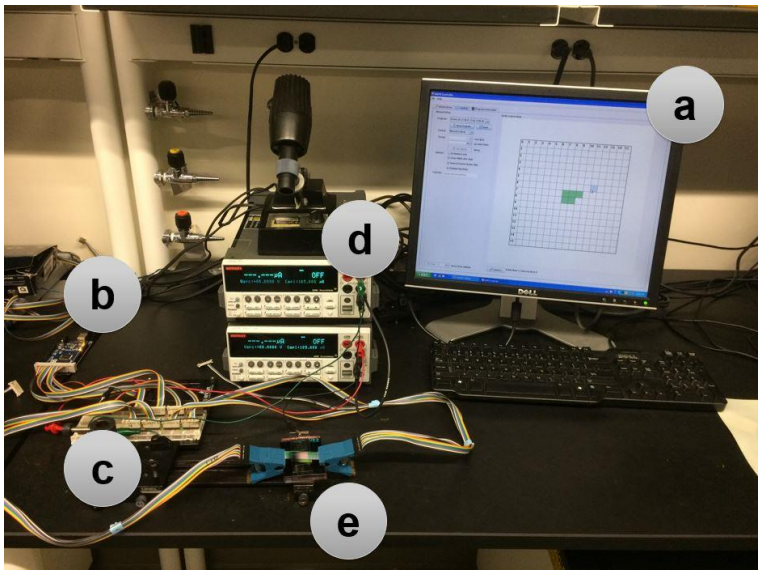


Figure 1.35: Photograph of electrowetting setup, incluidng (a) Active Matrix EW driving software, (b) Arduino board, (c) breadboard, (d) Keithley 2400 source meters, and (e) fabricated 16x16 Active Matrix EW platform.

This Active Matrix EW setup was then run with 40 V applied to the source electrode and 30 V applied to the gate electrode. The source and gate pulse widths where measured to be 100 μs. While droplet actuation was controllable across the columns, row control was not. This is due to the method by which the software drives the Active Matrix addressing.

In a completely OFF state, the desired gate ON voltage is cycled through the gate lines, while all 16 source lines are off. To turn ON a pixel, an applied source ON voltage pulse is synchronized with the appropriate gate line pulse. This synced voltage pulse enables droplet electrowetting, as the applied voltage is dropped across the EW pixel for the addressed pixel and the TFT for the non-addressed pixels.

However, this addressing control is dependent on the proper voltage drop distribution. As discussed earlier, each EW pixel functions as a series resistor, where the applied voltage is divided between the TFT and the EW pixel dielectric, and the voltage percentage seen on the EW pixel is dependent on the on/off state of the TFT and the resistivity of the dielectric. Figure 1.36 shows the transfer characteristics of four TFTs located in the periphery of the 16x16 Active Matrix EW platform, as well as the voltage drop divider taken from Figure 1.15a. Despite the discrepancy in uniformity across the platform, even the lowest ON current of $1x10^{-6}$ amps (1.36a) is capable of successful Active Matrix driving, with 97% of the voltage being dropped across the pixel (1.36b). The issue, however, lies in the OFF current as, at $V_g = 0$ V, only 23% of the applied V_{ds} is dropped across the TFT. Hence, the applied V_{ds} is seen across the entire addressed column regardless of which pixels are being addressed/not addressed. Because of this,

actuation of the droplet across the rows is not controllable. This is shown in Figure 1.37, where a yellow ink droplet (10 wt. % pigment with .01 wt. % sodium lauryl sulfate) is driven from left to right, but only the 3rd row is addressed. Despite this, the ink droplet shifts between rows independent of addressing, as is indicated by the red up/down arrows.

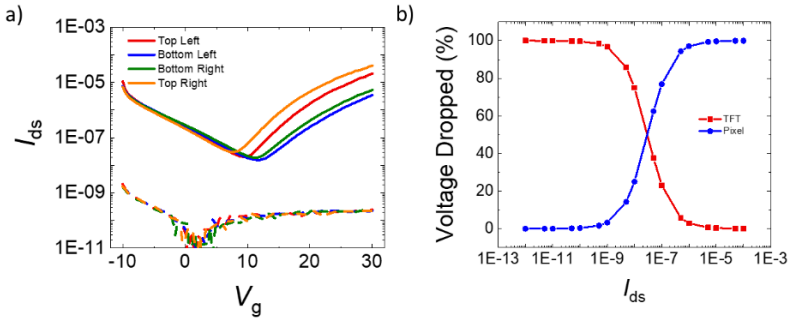


Figure 1.36: (a) Transfer characteristics of unit TFTs taken at the periphery of the 16x16 Active Matrix EW platform, showing unifomrity across platform. V_{ds} = 40 V. (b) Plot demonstrating percentage voltage drop across the TFT-EW series resistors and its dependence on measured TFT current with a measured pixel resistance of ~1 gigaohm.

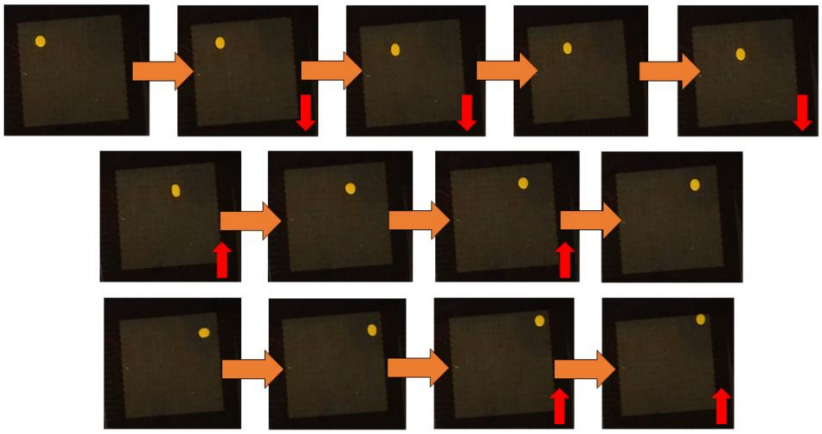


Figure 1.37: Series of photographs showing independent row shifting during Active Matrix electrowetting from left to right. Row shifting is indicated by red up/down arrow. For Active Matrix addressing, V_g = 30 V, V_{ds} = 40 V, and voltage pulse width = 100 µs.

Poly-crystalline Silicon Conclusion

In order to achieve Active Matrix EW across the entire 16x16 platform, further work would need to be done demonstrating tunability and control of the pixel resistance to complement the TFT ON/OFF resistances. This could be done by controlling passivation thickness, deposition method (ALD, PECVD, etc.), materials selection (SiO_2, HfO_2, Al_2O_3, etc.), and others. Further work is also needed in improving the LPCVD poly-Si growth process in order to successfully replicate device electrical characteristics.

CHAPTER 2 - PROGRAMMABLE ELECTRODLUIDICS FOR IONIC LIQUID BASED NEUROMORPHIC PLATFORM

A version of this chapter was originally published by Walker L. Boldman, Cheng Zhang, Thomas Z. Ward, Dayrl P. Briggs, Bernadeta R. Srijanto, Philip Brisk, and Philip D. Rack

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Background

Ionic liquid (IL) gating of metal oxide semiconductor devices has been studied extensively because of the intriguing properties of the electric double layer at the IL/solid interface. This electric double layer generates an extremely high electric field and induces large carrier densities at its interface. This generated electric field has been used to electrostatically tune the electrical and/or magnetic properties of certain materials, such as VO_2 [57], ZnO [58], Bi_2Se_3 [59], amorphous IGZO [35], few layer graphene [60], and others. When this electric field is applied over an extended amount of time, electrochemical doping can occur via ion extraction or intercalation of ions out/in of the semiconducting layer, respectively. Electrochemical doping of oxygen has been observed in materials such as WO_3 [61] and IGZO [34], and doping of hydrogen or hydroxyl ions via a hydrated ionic liquid has been seen in ZnO [62], MoO_x [63], and WO_3 [64], among others. Ionic liquid gating has also been used to induce superconductivity in various thin

films such as MoS_2 [65], $KTaO_3$ [66], and $SrTiO_3$ [67], and has been used to modulate optical properties of certain perovskite materials [68].

Ionic liquid gating is being explored as a possible neuromorphic computing platform, which attempts to mimic neuro-biological retention and retrieval of information. Neuromorphic computing attempts to overcome the Von Neumann bottleneck, which limits conventional computing power due to an inability to both fetch instructions and perform data operations at the same time. Neuromorphic computing attempts to overcome this by introducing massive parallelism of neuronal mimics [63], [69] and by attempting to store multiple bits per element [70]. Recently, Yang et. al [71] investigated ionic liquid gated MoO_x to mimic synaptic behavior, as shown in Figure 2.1. In their findings, they observe both potentiation and depression of current (Figure 2.1e and f) and demonstrate short and long term plasticity.

Electrowetting of Ionic Liquids

Ionic liquids (IL) have been extensively studied for their intriguing properties of the electric double layer formed at their liquid/solid interface. This electric double layer has been used for electric field gating of many materials, as we will see later. These liquids have effectively zero vapor pressure, good thermal and chemical stability, and are non-flammable [72]. The electrowetting properties of these ILs (also known as "ionic salts") have also been studied [72]–[74] and show promising manipulation and actuation. Figure 2.2 illustrates the electrowetting characteristics of several ILs [63] and Table 2.1

details the structure and electrowetting properties of several leading ILs in the literature today [74].

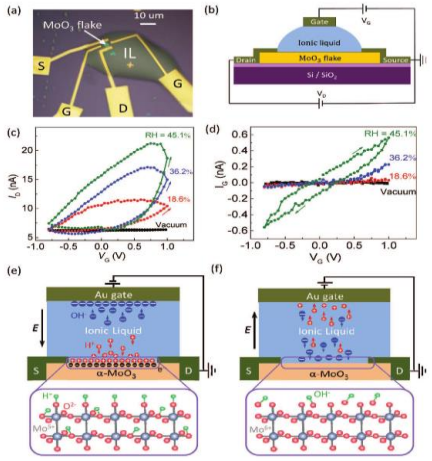

Figure 2.1: I-V (a) The optical image of the quasi-2D α -MoO_3 based three-terminal synaptic device. (b) The schematic illustration of the device structure and measurement setup. A small dc voltage (V_{ds} = 50 mV) was applied between the source and drain electrodes, and the corresponding drain current (I_d) was measured. The gate voltage (V_g) was directly applied on the gate electrode and the corresponding gate current (I_g) was also monitored. (c,d) The I_d and I_g dependence of the gate voltage, respectively, under different relative humidity conditions (vacuum, 18.6%, 36.2%, 45.1%). (e) Schematic of the transistor structure corresponding to the positive gate voltage application. (f) Schematic of the transistor structure corresponding to the negative gate voltage application. The protons are extracted and desorbed from the α -MoO_3 channel surface with the accumulation of hydroxyls, resulting in the channel conductance decrease back to the initial state. Reproduced from [71].

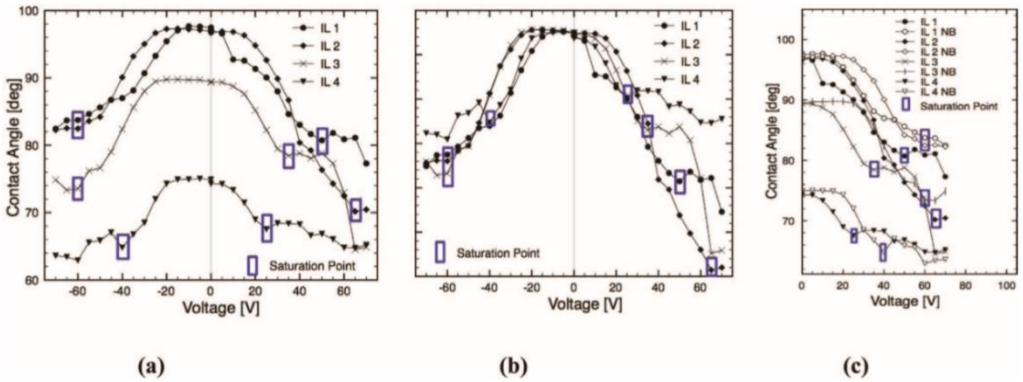

Figure 2.2: Example electrowetting curves of four chosen ILs. (a) Electrowetting curves of ILs 1-4. (b) Curves overlaid normal to the maximum contact angle value. (c) Folded curves, showing asymmetry in electrowetting. Reproduced from [73].

Table 2.1: Properties of several chosen ionic liquids, including: molecular volume (V_m), Ion Pair Diameter (d_m), Viscosity (η), Surface tension (γ), and static advancing (θ_A) and Receding (θ_R) contact Angles at 0 V. Reproduced from [73].

Ionic liquid	Abbrev	Structure	v_m nm^3	d_m nm	η mPa·s	γ mN/m	θ_A^0 °	θ_R^0 °
1-butyl-3-methylimidazolium tetrafluoroborate	[BMIM] BF_4		0.31	0.68	112	43.8	93	90
1-butyl-3-methylimidazolium hexafluorophosphate	[BMIM] PF_6		0.34	0.7	250	46.3	92	90
1-butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide	[BMIM] NTf_2		0.49	0.79	55	33.3	73	72
1-hexal-3-methylimidazolium bis(trifluoromethylsulfonyl)imide	[HMIM] NTf_2		0.54	0.85	80	31.3	72	69
1-octyl-3-methylimidazolium tetrafluoroborate	[OMIM] BF_4		0.42	0.75	330	33.5	80	77

Materials and Methods

In this study, we combined the electrical tuning of a TFT active layer with a pixelated electrowetting on dielectric (EWOD) array as a programmable neuromorphic device platform. Figure 2.3 overviews the device architecture. As shown in in Figure 2.3a, the device architecture consisted of a top and bottom plate. The bottom plate contains a 2D array of pixels, where each pixel contained an integrated dual gate thin film transistor and an electrowetting on dielectric electrode. The top plate is a pixelated electrode array, which acts as the top gate for the long-term potentiation of the device. The aIGZO thin film transistor array was integrated co-planar with a simple electrowetting array and both were fabricated on a silicon substrate with a 500 nm silicon oxide insulating layer. A 150 nm thick chromium back gate and co-planar electrowetting electrode was sputter deposited onto a 500 nm SiO_2 coated silicon wafer and then was lithographically patterned and wet etched with a Cr wet etch solution ($9\%(NH_4)2Ce(NO_4)_6 + 6\%(HClO_4) + H_2O$). A 100 nm SiO_2 gate dielectric and electrowetting insulator was deposited via plasma enhanced chemical vapor deposition (PECVD). The 50 nm a-IGZO active layer was rf magnetron sputter deposited at room temperature using an In_2O_3:Ga_2O_3:ZnO mixed and pressed powder target with a 1:1:1 mol % ratio, and patterned by lift-off. The rf sputtering power was 80 W and the sputtering pressure was 5 mTorr with a 10:1 mixing ratio of argon:oxygen at a fixed total flow rate of 25 SCCM. 10/80 nm Ti/Au source and drain electrodes were deposited by e-beam evaporation and patterned by lift-off. To achieve eletrowetting of the IL, ~ 400 nm

of TeflonAF 1600 was spin coated at 900 rpm for 60 seconds, and baked at 115 ºC for 15 minutes, 165 ºC for 15 minutes, and then 315 ºC for 30 minutes.

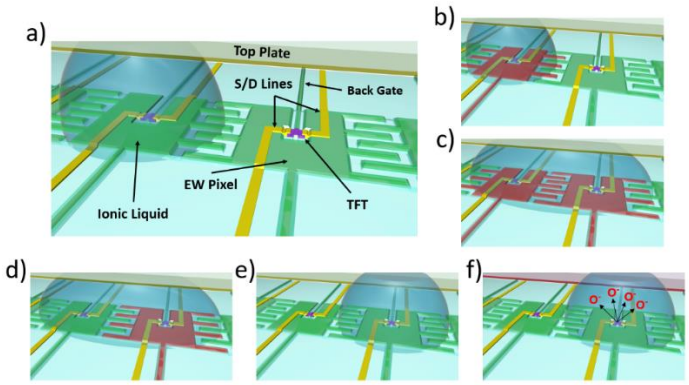

Figure 2.3: 1) (a) Schematic of Programmable Electrofluidic Neuromorphic device, with critical components labeled. (b-e) Schematic illustration demonstrating the electrofluidic control of the IL. In (b), the ionic liquid is present initially over the left pixel and is electrofluidically transferred to the neighboring right pixel by initially actuating the left pixel, which decreases the surface energy and causes the IL to spread. Next, (c) the neighboring right pixel is actuated, which causes the IL to selectively spread to this pixel. The left pixel is then turned off (d), which increases the surface energy, and thus the ionic liquid migrates over to the right pixel. After movement to this pixel, the right pixel is then turned off (e), which completes the cycle. Short term plasticity is realized when a transistor is measured with IL present on the pixel. Long term plasticity is realized by applying a bias on the ionic liquid via the top plate (f), which electrochemically alters the composition of the material by extracting oxygen ions, permanently altering its electrical resistance.

A key feature of the device is the programmability of the IL network over the 2D pixel array via electrowetting. As illustrated in Figure 2.3b–e, electrowetting of the IL was accomplished via activating the (b) left pixel, which contained the IL, and thus inducing a lowering of the hydrophobicity of the IL, which caused spreading. (c) By activating the right pixel, spreading was directed to this pixel. After the IL had spread to this right pixel, the left pixel was turned off (d), thus increasing the hydrophobicity, which caused the drop to dewet from the left pixel. Clearly, any neuromorphic application will require long-term electrowetting stability. Interestingly, while many electrowetting lab-on-chip applications have been proposed, relatively little work has been devoted to studying long-term stability of these devices. In a study done by Dhindsa et al., a study was done with a dip-coated fluoropel layer where over 300 cycles were achieved without any significant change to the contact angle or degradation of the hydrophobic layer [75]. Similarly, work done by Mibus and Zangari showed that, for a TaOx/spin coated Cytop insulator/hydrophobic layer stack, stable electrowetting of up to 350 cycles was achieved at a 20 V bias [76]; however, severe degradation occurred at 25 V applied bias. As will be demonstrated, the presence of the IL on the aIGZO active layer changed the transfer characteristics and thus realized STP. LTP was realized by applying a top gate bias (f) to the IL, which electrochemically extracted/intercalated ions out/into the active layer and changed the electrical properties of the aIGZO.

Constant Bias Results

Figure 2.4a shows back gate transfer characteristics with and without the presence of IL on the active layer, which illustrates that STP (volatile memory) was realized via

electrowetting the IL over the desired aIGZO TFT pixel. Note: Current values below 1e-14 amps were truncated due to instrument sensitivity. For this experiment, diethylmethyl (2-methoxyethyl) ammonium bis(trifluoromethyl sulfonyl)imide (DEME) was chosen as the ionic liquid. The TFT transfer characteristics changed dramatically, as noted by an ~580× increase in the I_{ds} when V_g was equal to zero. This electrostatic effect was only present while the IL/solid interface was formed, and could thus be combined with electrowetting of the IL to create a programmable STP device. Combining this effect with an active matrix array of transistors [10], [29] could result in a neuromorphic platform that could be scaled to very high pixel counts.

Non-volatile memory, or LTP, was induced by electrochemically altering the chemical composition in the active layer via a positive top gate bias. To characterize this LTP effect, Figure 2.4b–d illustrates a series of electrical measurements taken on the IGZO active layer. For this experiment, both DEME and LiClO–PEO were used. DEME electrochemically dopes the IGZO active layer by extracting oxygen ions under a positive gate bias, and thus decreasing the device resistance. The electrochemical effect of the DEME is permanent but, unlike several other oxide materials, is non-reversible. To create a device capable of both potentiation (decrease in device resistance) and depression (increase in device resistance), the electrostatic and electrochemical effects of DEME were compared to another ionic liquid, LiClO–PEO. Rather than extracting oxygen, LiClO–PEO intercalates (positive gate bias) or extracts (negative gate bias) lithium ions into the near surface region of the aIGZO active layer, which in turn decreases or increases device resistance, respectively [77]–[79]. To demonstrate the LTP, after the

ionic liquid is actuated over the pixel, a top gate bias of +2 V was applied to the IL/active layer for various time intervals (10, 10, 30, 50, and 100 s) for a total of 200 s (Figure 2.5). Figure 2.4b,c show the back gate transfer characteristics for the DEME and LiClO–PEO ILs (respectively) measured in between each time interval, where the ILs induce higher conductance in the aIGZO channels. After a cumulative bias time of 200 s, a negative bias ($V_g = -2$ V) was applied to both devices, indicated by the dashed line in Figure 2.4b,c; note that the DEME channel inexplicably continued to decrease the channel resistance, whereas the −2 V bias for the LiClO-PEO IL increased the channel resistance. To demonstrate the purely electrochemical change, Figure 2.4d illustrates the currents at $V_g = 0$ V for each transfer measurement plotted as a function of top gate bias time and normalized with respect to the current at zero gate voltage before biasing (note that off state current for the DEME is much lower than that of the LiClO–PEO). For both ILs, the electrochemical effect of positive biasing tended to saturate after 100 s. TFT resistance under DEME biasing changed by over two orders of magnitude in under a minute, promoting fast writing/programming time in a neuromorphic device. While the electrochemical effect of the DEME was much more pronounced, applying a negative bias further decreases device resistance; the LiClO–PEO IL, however, when biased at −2 V, increased the resistance and thus demonstrated reversible transport modulation.

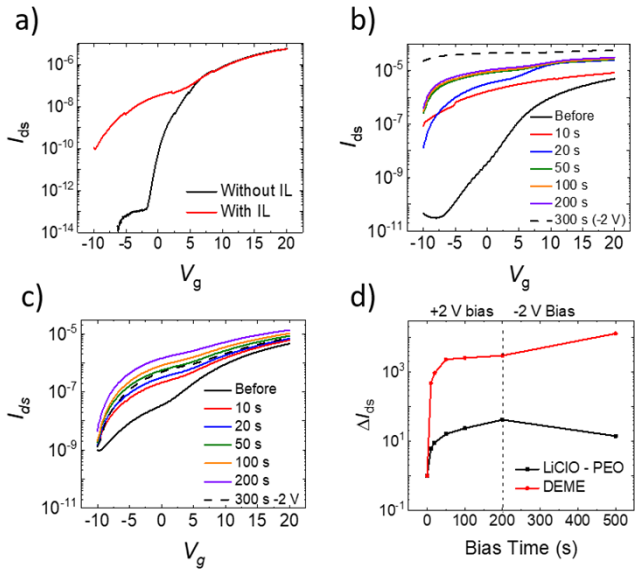

Figure 2.4: (a) Back gate transfer characteristics of a thin film transistor (TFT) pixel both with and without the presence of the DEME ionic liquid. After electrowetting the ionic liquid over the TFT pixel, the transfer characteristics shifts due to the presence of the IL. (b,c) illustrates the back gate transfer characteristics after each IL bias time, which demonstrates the electrochemical long-term potentiation (LTP) due to biasing of DEME and LiClO–PEO, respectively. After a cumulative 200 s positive bias, a −2 V bias for 300 s was then applied to both ILs in an attempt to reverse the characteristics; note only the LiClO–PEO IL exhibits some recovery of the high-resistance state. The I_{ds} at zero gate voltage as a function of IL biasing is shown in figure (d) as a function of cumulative bias time. In (a–d), V_{ds} was 1 V.

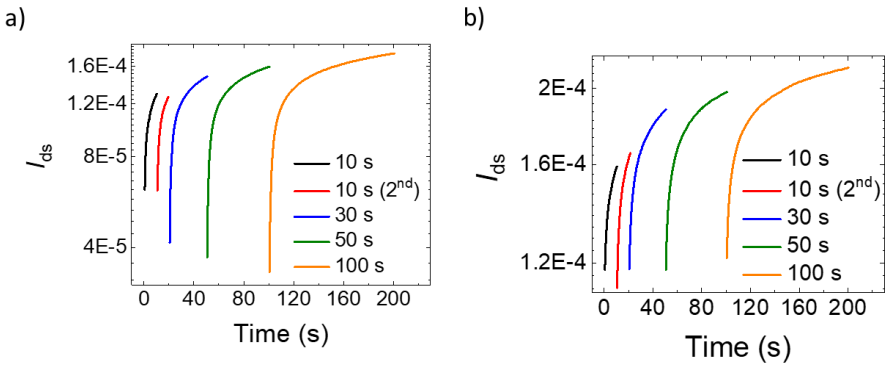

Figure 2.5: I_{ds} as a function of cumulative bias time for a) LiClO – PEO and b) DEME.

Pulsed Bias Results

Since low power computation is a significant driving force for neuromorphic computing, we explored short pulse biasing with the DEME IL. Figure 2.6a illustrates three series +2 V 50 ms gate bias pulses (15, 50, and 100 pulses, respectively) where the I_{ds} (V_{ds} = 1 V) was measured during the IL gate bias. Figure 2.6b is a magnified view of seven pulses of the 100-pulse series. The electrostatic IL effect was clear as the on-current increased over six orders of magnitude. To measure a residual electrochemical effect, after each series of pulses, I_{ds} was allowed to decay to a pseudo-saturation point, allowing any remnant electrostatic effect to decay. Figure 2.6c is a plot of I_{ds} after each pulse series, which illustrates that the change in remnant current increased with an increase in the number of pulses. Figure 2.6d shows the remnant I_{ds} current measured two

seconds after each pulse, demonstrating a permanent and incremental decrease in the channel resistance.

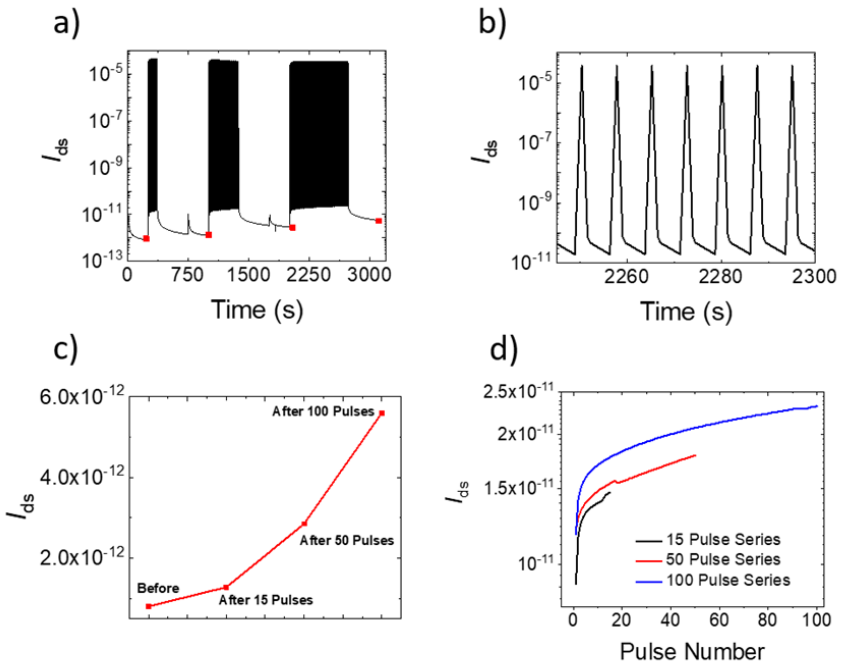

Figure 2.6: (a) I_{ds} as a function of time for a series of +2 V, 50 ms top gate pulses (15, 50, and 100, respectively) applied to the active layer. (b) Magnified view of seven pulsed cycles from (a). (c) Remnant I_{ds} values (red squares in (a)) after each pulse series, where the relaxation time after the last pulse was 630 s. To illustrate the cumulative effect of each +2 V 50 ms bias pulse, the I_{ds} versus pulse number is plotted for each series after a relaxation time of 2 s per pulse. In (a–d), V_{ds} was 1 V.

Platform Programmability

The proposed programmability of the neuromorphic platform was realized via electrowetting of the IL. Electrowetting has been used in the development of Lab on a Chip [75], [78], [79], flexible and transparent displays [22], as an aid in medical and chemical analysis [21], [27], and novel device concepts, such as an aerosol sampler [80] and a micro conveyor system [28]. The electrowetting of the IL is governed by the Young-Lippmann equation, $\gamma_{LG}\cos(\theta) = \gamma_{SG} - \gamma_{SL} + (1/2)CV^2$, where θ is the wetting angle, γ_{SG} is the surface tension between the substrate and air (or oil), γ_{LG} between the IL and air (or oil), γ_{SL} between the solid and IL, C is the capacitance per unit area, and V is the applied electric voltage. As the capacitance of the electrowetting dielectric is critical to the performance, we used a 100 nm SiO_2 electrowetting dielectric with a specific capacitance of 39.4 pF/cm^2. The electrowetting behavior of many different ionic liquids have been observed, with voltages required to achieve electrowetting ranging from 25 to 190 V [72], [74]. The contact angle saturation in ionic liquids have been studied [74], and the voltage range for saturation is shown to be 40 to 70 V. In an optimized neuromorphic platform, low-voltage electrowetting would be critical for low-power consumption, and thus contact angle saturation should not limit device functionality. Furthermore, to lower the EW voltage, nanostructured EW electrodes could also be employed to enhance the hydrophobicity. Thus, we characterized the basic electrowetting characteristics of DEME via a series of actuation tests of the IL (relative to a standard yellow ink) as a function of increasing voltage (Figure 2.7e). Movement speed of the DEME and a yellow ink (Cab-O-JET 270 Yellow Colorant) were captured on a DSLR video camera, and the time

needed for the IL droplet to move across one pad (2 mm) was recorded. To ensure that the results were repeatable and reliable, each droplet was moved left and right two times (four movements), with the time recorded being the average of these measurements.

To combine the electrowetting platform with the TFT pixel array, a transparent top electrode plate was patterned via indium tin oxide (ITO) sputtering and lift-off. This top plate acts as a common ground during EW actuation of IL droplet, and as the programmable IL gate electrode during biasing. To form a channel, a DEME reservoir was dispensed onto the electrowetting platform via a micropipette next to the electrowetting array, as shown in Figure 2.7a. Subsequently, the electrowetting pixels 1–8 were progressively activated by applying a 20 V bias to each pixel. Figure 2.7b is a still image of the early stage channel formation, where just EWP1 was biased. Figure 2.7 shows the channel formation after the first five pixels had been activated, which took approximately 10 s for the viscous IL to cover. Full channel formation, Figure 2.7d, took approximately 24 s; however, channel retention was only maintained for as long as the bias was applied. Similarly, agile droplet motion is also achievable via sequential pixel biasing, as schematically illustrated in Figure 2.8 and demonstrated in Figure 2.7f–h. Initial actuation/biasing of the original IL pixel (Figure 2.7f) caused the drop to spread and directed spreading was accomplished by simultaneously addressing the appropriate neighboring pixels (g). After the droplet spread over both pixels, de-activating the original pixel (h) caused the drop to dewet from the original pixel. Full 2D channel formation and droplet motion was possible, leading to a deterministic pattern of the IL on the pixelated array.

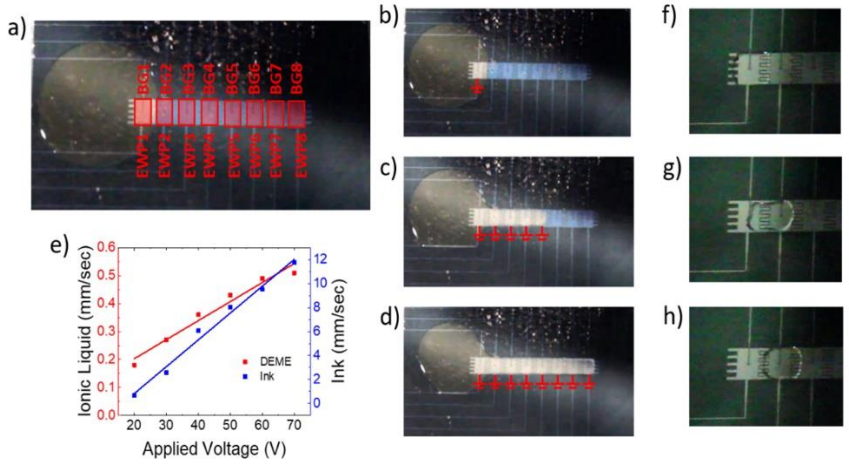

Figure 2.7: (a) Photograph of programmable electrofluidic neuromorphic device with the circular ionic liquid reservoir shown to the left (slight yellow tint) of the 1D electrowetting array. Overlaid in (a) are the rectangular pixels and the labels for the back gate contact lines (BG 1 - 8) and electrowetting pixel contact lines (EWP 1 – 8). (b) Channel formation with only EWP1 turned on. (c) Channel formation after EWP1–5 have been powered (10 s) and (d) channel formation of IL after all EWP1 – EWP8 are powered (24 s). Electrowetting voltage in (b–d) and (f–h) was 20 V. (e) Plot of electrowetting speeds of DEME compared to a standard aqueous based yellow ink as a function of applied voltage. (f–h) illustrate IL droplet motion, similar to schematically illustrated in Figure 2.8 (see text for details).

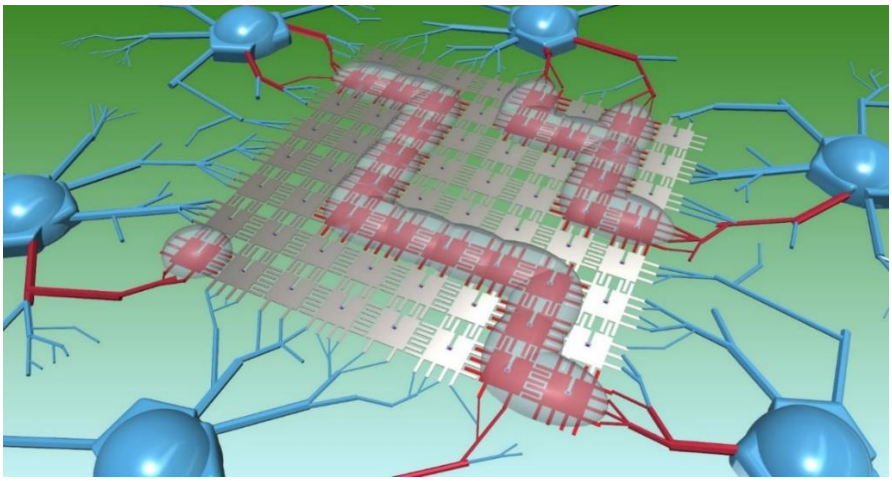

Figure 2.8: Conceptual model of a 2D array programmable electrofluidic neuromorphic device capable of multi-pixel biasing. Here, three ionic liquid droplets are shaped via electrowetting into user defined channels, allowing specific chosen pixels (highlighted in red) to be programmed.

Conclusion

In conclusion, by mimicking the neuro-biological processing via an ionic liquid neuromorphic platform, we demonstrated both short- and long-term potentiation, as well as reversibility of the device resistance. Short-term potentiation was achieved by electrowetting the IL over the desired TFT/TFTs, and long-term potentiation was achieved by electrochemically doping the TFT. We showed successful doping of the aIGZO via oxygen extraction using DEME, and reversible intercalation of lithium ions using LiClO–PEO. Short pulsed biasing was performed as a way to minimize power. IL

channel formation and droplet mobility were both demonstrated and characterized in order to move towards a multi-pixel biasing scheme.

CHAPTER 3 - COMBINATORIAL THIN FILM SPUTTERING FOR RAPID MATERIALS DISCOVERY

Motivation and History

Most traditional alloys are based on one principal element, and have been around for thousands of years. These principal elements have different alloying materials added to improve specific properties of the alloy, thus creating a family of alloys around a principal element. Notable alloys introduced through this method include bronze, steel, wrought iron, brass, and many others. While these alloys are extremely beneficial to the modern world, they are limited simply by the number of elements in the periodic table. If, however, alloys with more than just one or two principal elements opens up a vast number of possibilities. This was first explored in 1995 [81], and was coined as a 'high entropy alloy' (HEA). Other recent names include multiple principle element alloys (MPEA), or concentrated solid solutions (CSS).

HEAs are defined as any alloy with five or more principal elements, though there are many four-element HEAs that have been explored as well [82]–[84]. Each principal element should have at least a 5 at.% concentration, though additional elements with less than 5% can be added as well. When these elements are mixed together, instead of precipitating out into several different phases (as one might expect), the alloy remains in a solid solution. This solution exhibits a very high entropy of mixing, which leads to a very low Gibbs free energy, according to the equation $G = H - TS$, where G is Gibbs free energy, H is enthalpy, T is the temperature, and S is entropy. This unique

composition leads to many beneficial materials properties, including high strength [83], wear resistance [85], corrosion [86] and oxidation resistance [87], high-temperature strength [88], and others.

Traditionally, multicomponent films (including HEAs) are deposited via the sputtering from a mixed HEA target that has been processed to meet the desired composition. This single target is loaded into a sputter chamber and the film is then sputtered onto the desired substrates. While this method is easy and straight-forward, there are downsides, as these targets are often expensive, can take several months to fabricate and ship, and offer no tunability/variation in atomic composition.

Alternatively, multicomponent films can be co-sputtered from multiple single element targets. This requires a sputter chamber capable of co-sputtering, as well as forehand knowledge of the sputtering parameters of each individual target. However, the advantages of co-sputtering include the ability to tune/modify atomic composition and a vastly increased library of alloys available.

In our specific sputter chamber, up to four targets can be sputtered co-sputtered (Figure 3.1). If the substrate is rotated during deposition, a uniform film is deposited across the substrate. If, however, the substrate is not rotated, then a compositional gradient is deposited across the substrate, with the atomic concentrations depending on the number of targets, applied power, target tilt, and position on the substrate, etc.

Figure 3.1: photograph of sputter chamber during sputtering of a HEA via four sputter guns (bottom) aimed towards a substrate (top).

Computational Modeling of Co-Sputtering

In order to better understand and predict the effects of co-sputtering from individual targets, a computational model was developed that could predict substrate composition across a 100 mm diameter substrate. This model is capable of predicting composition at any given point on the substrate based on the sputtering rates of individual sputtering sources, as well as determining the necessary sputter rates to achieve any given atomic composition.

For this model, each of the four sputter guns is modeled as an individual Knudson surface source, where the sputtering flux per unit area is given by the equation

$$\frac{d\overline{M_s}}{dA_s} = \frac{\overline{M_T}(n+1)cos^n\varphi\ cos\theta}{2\pi r^2}$$

Where dM_s/dA_s is the mass deposited per unit area and M_T is the total sputtered mass from the target. Here, φ is the angle between the target surface normal and a line extending from the center of the target to a given point on the substrate surface (Figure 3.2). n is the degree of flux forward peaking, and has been determined experimentally to be ~12 [89], mostly due to the targets being positioned inside stainless steel chimneys in order to prevent cross-contamination (see Figure 3.1). As the targets are not angled such that the target normal line is not parallel to the substrate normal line, θ is introduced, and is defined as the angle between the substrate surface normal and a line extending from the center of the target surface to a given point on the substrate surface. *r* is the distance from the center of the target to a given point on the substrate surface.

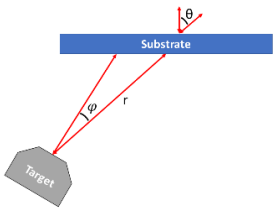

Figure 3.2: A schematic illustrating the geometry of the sputtering gun and substrate.

Physical Parameters

Physical chamber measurements that affect the sputtering conditions include the distance between targets, the tilt angle of the targets, the vertical distance between the targets and the substrate, and the substrate size. In our specific sputtering system (AJA ATC 2000-F), the sputter guns are spaced 25 cm apart 15 cm below the substrate holder, as represented in Figure 3.3. While the spacings of the guns are fixed, the sputter flux can be adjusted by either changing the substrate height or by changing the tilt of the sputter guns (indicated by α in Figure 3.3b). To demonstrate how these parameters effect the sputtered films, a simple model was created that simulated sputtering from a single target. The total thickness sputtered (both absolute and normalized) is plotted as a function of substrate position for both varying target tilt angle (Figure 3.4) and substrate height (Figure 3.5). In modeling of co-sputtered alloys, the substrate height is set to 15 cm, and the tilt angle is set to 32.7°, where a tilt of 0° corresponds to the sputter guns pointed straight up. As the model treats each sputter gun as an individual source, the user can set the tilt of each gun independently in order to greater increase/decrease the effects of that gun in the overall composition.

Once the sputter rates of each element are determined, then both the atomic percent and atomic weight percent of any co-sputtered alloy can be determined given the atomic mass and density of the sputtered materials. For convenience, a table of these values have been preloaded into the model, allowing the user to simply select from the list of available materials. Alternatively, the user can input a new element by manually

entering in the atomic mass and density when prompted by the model. The complete code can be found in the Appendix for reference.

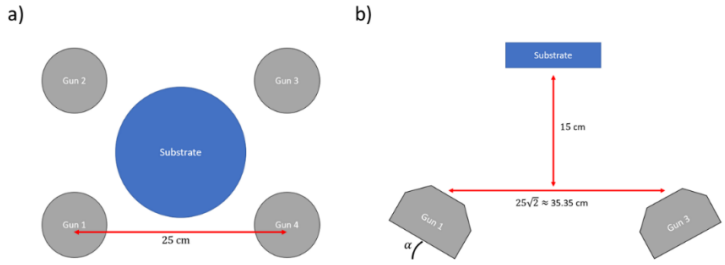

Figure 3.3: Schematic detailing a top-down (a) and side view (b) of the AJA ATC 2000-F sputtering chamber.

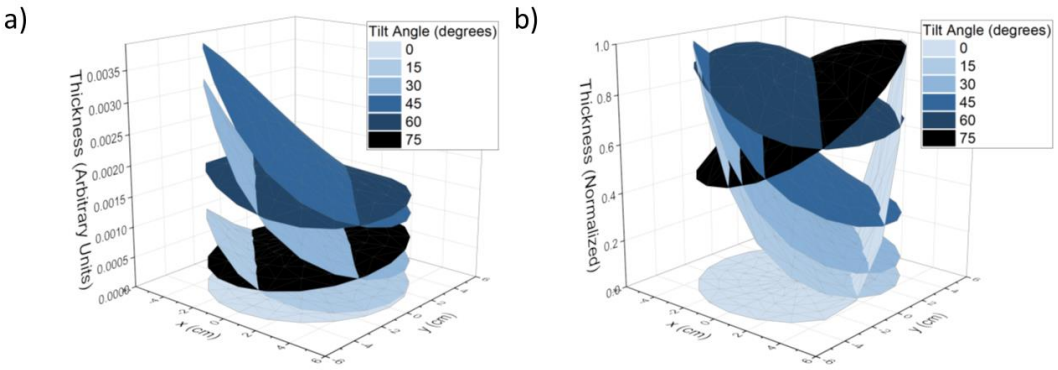

Figure 3.4: Thickness mapping over an 100 mm wafer as a function of sputtering gun tilt angle. Here, thickness is mapped in absolute arbitrary units (a) and normalized to maximum thickness (b).

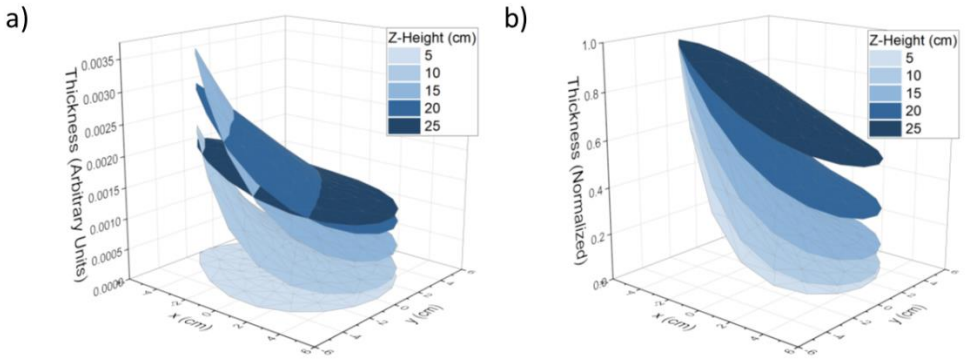

Figure 3.5: Thickness mapping over an 100 mm wafer a function of substrate height. Here, thickness is mapped in absolute arbitrary units (a) and normalized to maximum thickness (b).

Once the sputter rates of each element are determined, then both the atomic percent and atomic weight percent of any co-sputtered alloy can be determined given the atomic mass and density of the sputtered materials. For convenience, a table of these values have been preloaded into the model, allowing the user to simply select from the list of available materials. Alternatively, the user can input a new element by manually entering in the atomic mass and density when prompted by the model. The complete code can be found in the Appendix for reference.

Two-Element Modeling

In order to validate the model, several two-element alloys were selected from experimental work carried out previously in our AJA sputter system, including a Au-Al alloy [90] and a Au-Ni alloy [91]. Atomic compositions of these alloys were determined via EDS and plotted against computational estimation, as shown in Figure 3.6. For both alloys, the composition across the wafer diameter was estimated by tuning the sputter rates in the model such that the composition in the center position (0,0) matched the composition determined experimentally. Also included in the modeling of the Au-Ni (3.6a) alloy are composition estimations for a peak forwarding value (n) of 6 and 18, demonstrating both good agreement of n = 12 and proper behavior of the flux gradient as n increases.

Once the atomic weight percent gradient is known, a total thickness gradient can also be calculated across the 100 mm wafer. Experimentally, the most straightforward method of measuring a thickness gradient is to cut the wafer along the direction to be measured and then take a series of SEM cross-sectional images. Not only does this result in destruction of the wafer, but also limits the user to one direction along the wafer, so a series of multiple cuts would have to be taken in order to obtain a full 2D mapping. Another alternative would be to measure atomic composition across the entire wafer (a both tedious and time-consuming process) and calculate the thickness according to the atomic composition, mass, and density of the materials sputtered. With this model, however, a 2D mapping of thickness across the entire 100 mm wafer can be estimated using nothing more than the calculated sputter rates of each material, as well as the

materials properties. Figure 3.6 plots the total thickness across a 100 mm wafer for the Au-Ni alloy referenced above.

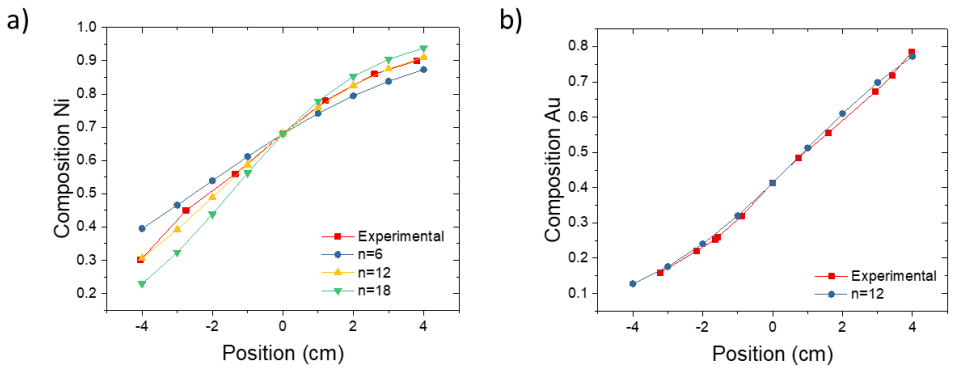

Figure 3.6: Atomic composition plots for a Au-Ni alloy (a) and a Au-Al alloy (b) plotted against computational estimation. In both a and b, the computational value of the center position was fit to match the experimental value.

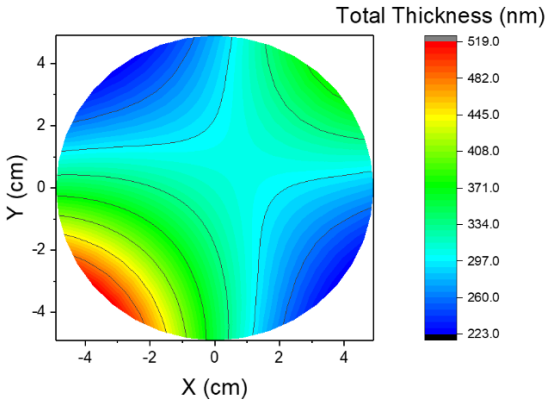

Figure 3.7: Thickness gradient of a Au-Ni alloy mapped across a 100 mm wafer.

To verify computational thickness against experimental, two samples were prepared with sputtered copper, one sputtered via magnetic sputtering, and the other sputtered via magnetron sputtering. Note that for magnetic versus magnetron sputtering, the flux profile should not change, but rather only the sputtering rate.

Each sample was sputtered for 30 minutes, with 100 W applied to the magnetron sample, and 200 W to the magnetic sample. The samples were not rotated during sputtering in order to achieve a thickness gradient across the sample that could be used to verify the sputtering model (Figure 3.5 shows a normalized thickness profile for a 4" diameter sample). After sputtering, the samples were cut parallel to the gradient and imaged via SEM imaging. Since the sputter rates were not previously determined, the sputtering model was zeroed by inputting the actual thickess at the sample center, which, if rotated, would produce a uniform sputtering rate across the sample. Figure 3.8 plots the contrasted thicknesses of the experimental results against the sputtering model for both magnetron and magnetic sputtering, and shows them to be in good agreement.

CoCrCuFeNi HEA

In this study, a five-element HEA consisting of cobalt, chromium, copper, iron, and nickel was sputtered for a group at the Oak Ridge National Laboratory. Since more than four elements were desired, a single 50 mm diameter target consisting of 1:1:1:1:1 CoCrCuFeNi was ordered and sputtered onto various substrates, including a 100 mm wafer, quartz glass slides, NaCl salt substrates, and TEM grids.

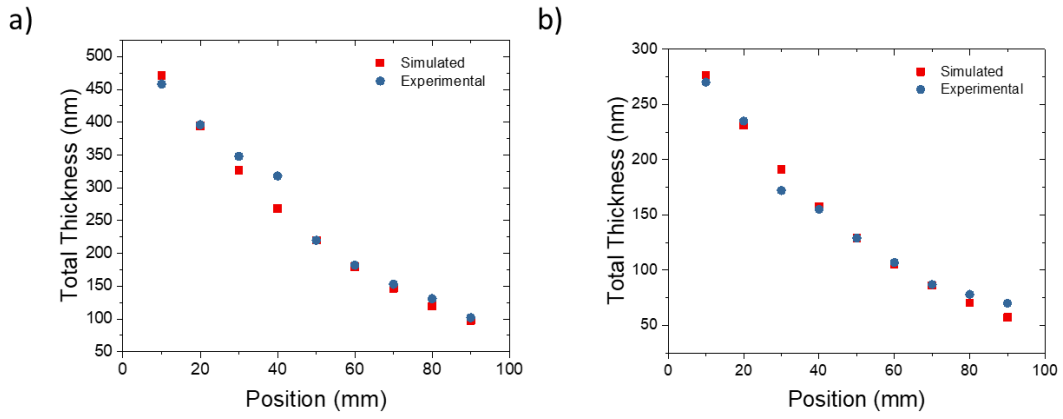

Figure 3.8: Total thickness plots contrasting simulated results against experimental results for both the magnetron sputtered sample (a) and the magnetic sputtered sample (b).

CoCrCuFeNi HEA

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These films (with thicknesses of 70 nm and 1000 nm) were deposited using a DC power supply at 200 W with an Ar flow rate of 25 sccm through a throttle valve setting to

equilibrate the system at 5 mTorr. Grain growth and phase stability of these films were then studied via both thermal and irradiation induced crystallization [92].

CrMnNiFe HEA

Methods

In this study, a HEA consisting of chromium, manganese, nickel, and iron was sputter deposited and characterized for study of its magnetic and thermal properties. This alloy was co-sputtered from four individual targets, and sputter rates were chosen and tuned so the atomic ratio of the HEA composition in the center of the substrate would be 1:1:1:1. Table 3.1 details the power and voltage applied to each target during sputtering. However, due to plasma rate limits during the co-sputtering, the final HEA composition deviated from the desired composition, as shown in Figure 3.8. 50 nm of the HEA was sputtered on a 100 mm silicon wafer with 100 nm of thermally grown SiO_2, and a second wafer was prepared as above with 300 nm of the HEA. Sputtering was carried with an original base pressure of $1x10^{-7}$ Torr, a working pressure of 5 mTorr, and an Ar gas flow rate of 25 sccm. The atomic ratio of the HEA elements at each of 17 points shown in Figure 3.8 (spaced 2 cm apart) was determined by energy dispersive x-ray spectroscopy (EDS), and scanning electron microscopy (SEM) images were taken as well (Figure 3.9).

Four-Element Modeling

Once the sputter rates of the four individual elements are determined, the co-sputtering process is simulated and compared to the experimental results. The modeled

results include the relative error between experimental and modeled composition (Figure 3.10), and a 3D plot of the total thickness across the 100 mm wafer (Figure 3.11).

Table 3.1: Sputtering conditions for HEA deposition. Total sputter rate was calculated to be 2.27 nm/min.

	Cr	**Mn**	**Ni**	**Fe**
Power (W)	30	33	11	175
Voltage (V)	244	144	112	1070

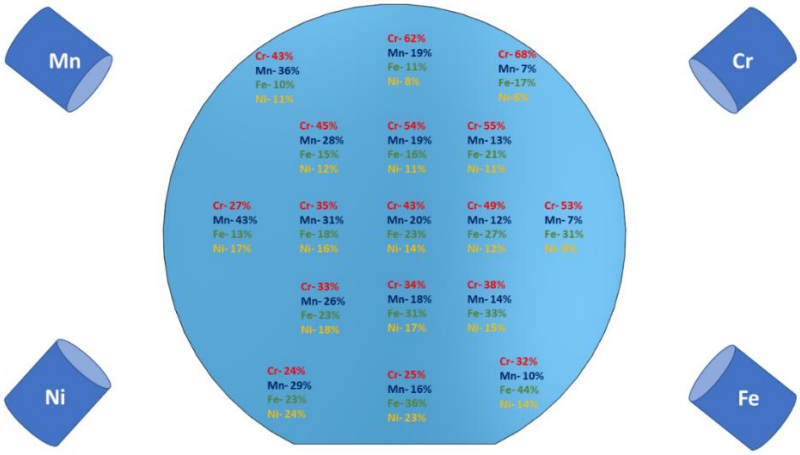

Figure 3.9: Atomic percentage mapping of the NiMnCrFe HEA across an 100 mm wafer.

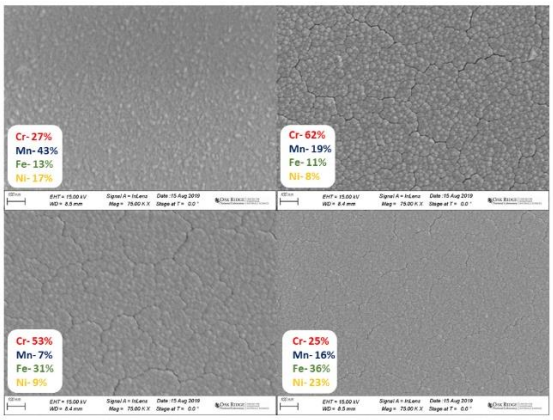

Figure 3.10: SEM images taken at various alloy compositions of the FeMnCrNi HEA.

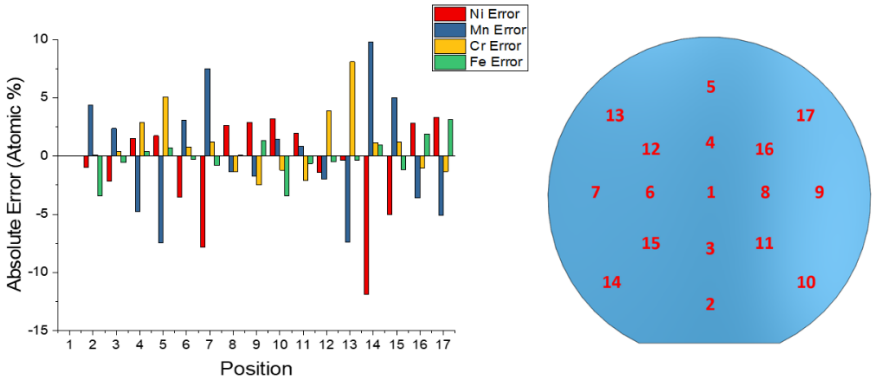

Figure 3.11: Bar graph illustrating absolute error of the CrMnNiFe HEA between EDS determined atomic composition and computationally modeled atomic compostion for each of the 17 positions shown on the 100 mm wafer schematic (right).

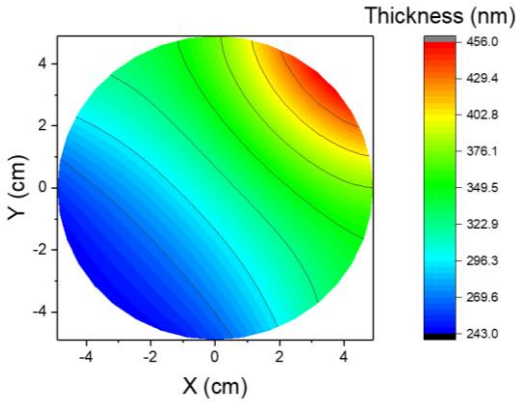

Figure 3.12: 2D projection of the CrMnNiFe HEA thickness.

TiZrHfW HEA

Methods

In this study, a HEA consisting of titanium, zirconium, hafnium, and tungsten was sputter deposited and characterized for study of its crystallization properties during thermal and laser irradiation. This alloy was co-sputtered from four individual targets, and sputter rates were chosen and tuned so the atomic ratio of the HEA composition in the center of the substrate would be 1:1:1:1. Table 3.2 details the power and voltage applied to each target during sputtering. However, due to plasma rate limits during the co-sputtering, the final HEA composition deviated slightly, as shown in Figure 3.12. Two wafers were sputtered, one with 1 µm of the HEA was sputtered on a 100 mm silicon wafer with substrate rotation (to obtain a uniform composition and thickness across the

entire wafer) and one with 1 µm of the HEA sputtered without substrate rotation. As above, the atomic composition of each of the 17 points shown in Figure 3.14 was determined via EDS.

Table 3.2: Sputtering conditions for HEA deposition. Total sputter rate was calculated to be 6 nm/min.

	Ti	**Zr**	**Hf**	**W**
Power (W)	46	100	47	208
Voltage (V)	320	303	163	700

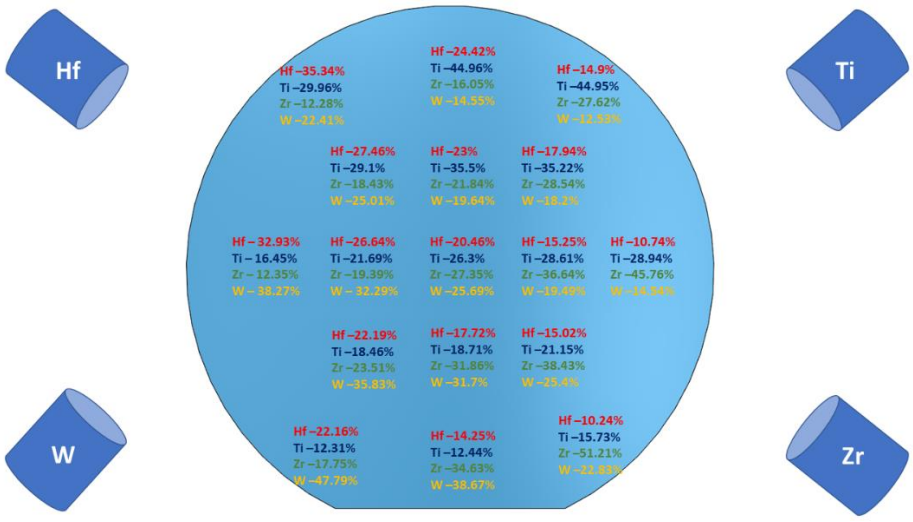

Figure 3.13: Atomic percentage mapping of the TiZrHfW HEA across an 100 mm wafer.

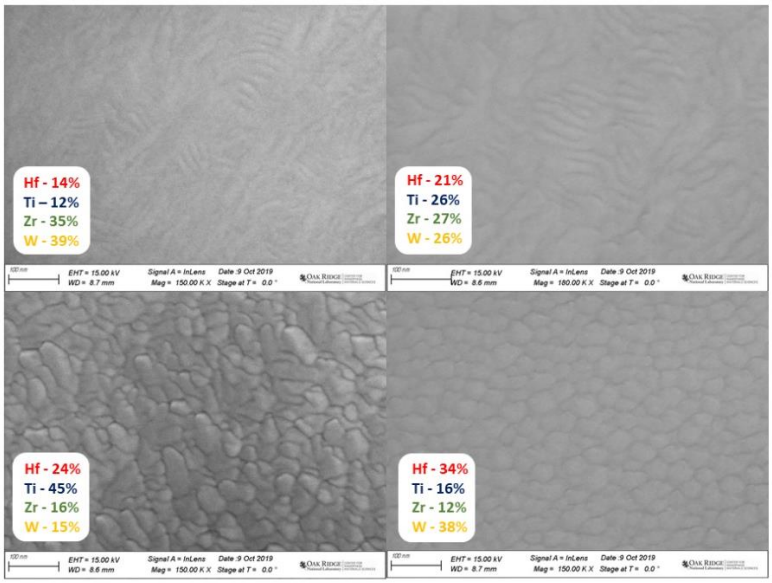

Figure 3.14: SEM images taken at various alloy compositions of the TiZzHfW HEA.

Four-Element Modeling

For this study, 50 nm of HEA was sputtered on a 4" silicon wafer with 100 nm of thermally grown SiO_2, and a second wafer was prepared as above, but with 300 nm of HEA. Sputtering was carried out at a base pressure of $1x10^{-7}$ Torr, a working pressure of 5 mTorr, and an Ar gas flow rate of 25 sccm. The atomic ratio of the HEA elements at each of the 17 points was determined by energy dispersive spectroscopy (EDS), and scanning electron microscopy (SEM) images were taken as well (Figure 3.14).

Once the sputter rates of the four individual elements are determined, the co-sputtering process is simulated and compared to the experimental results. The modeled results include the relative error between experimental and modeled composition (Figure 3.14),

and a 3D plot of the total thickness across the 100 mm wafer (Figure 3.15). The variance in wafer thickness of ~120 nm can be explained by comparing the density of the four elements sputtered. The aim of this study was to have the atomic % ratio (note: *not* weight % ratio) of the center position 1:1:1:1. However, the difference in densities between the four elements is substantial, with a factor of ~5 between the least (zirconium) and most (tungsten) dense materials.

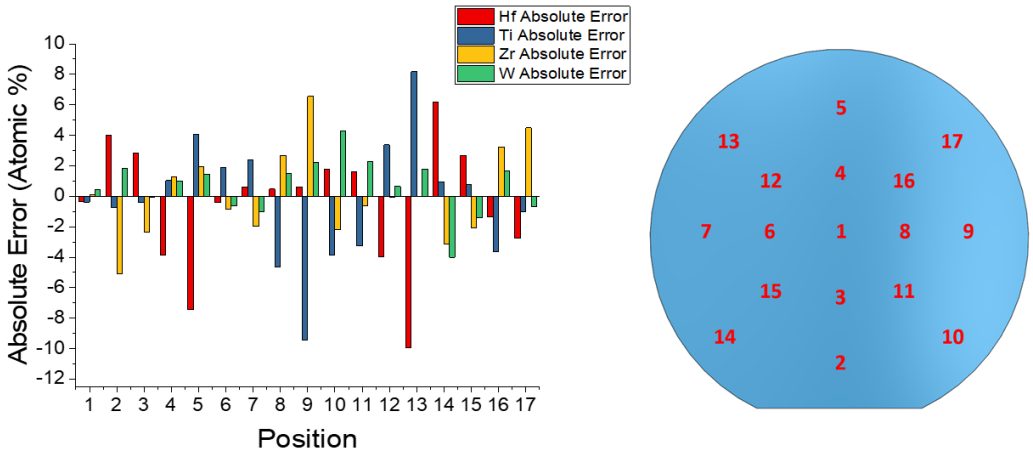

Figure 3.15: Bar graph illustrating absolute error of the TiZrHfW HEA between EDS determined atomic composition and computationally modeled atomic compostion for each of the 17 positions shown on the 100 mm wafer schematic (right).

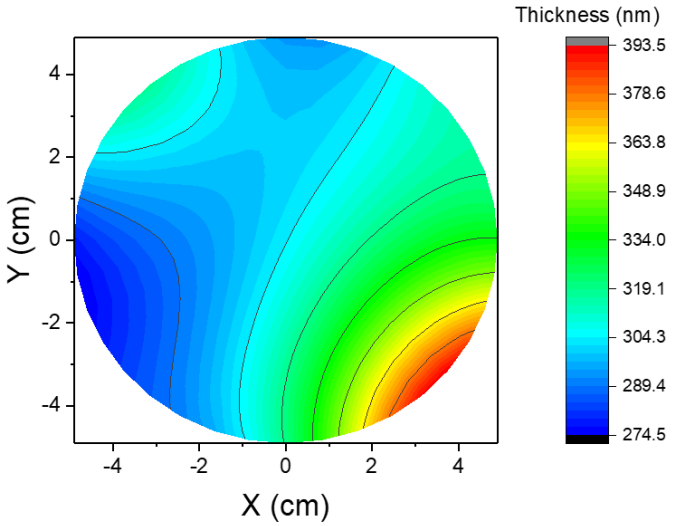

Figure 3.16: 2D projection of the TiZrHfW HEA thickness.

Exploring the composition and phase separation and structure of AgFe alloys for magneto-optical applications

Bimetallic systems have been studied for a wide variety of functional applications, including plasmonics [93]–[95], surface-enhanced Raman scattering [96], biomedicine [97]–[99], and others. Fe-based binary alloys are of particular interest for their structural and outstanding magnetic properties with large magnetization [100], [101]. Further, the combination of a magnetic Fe compound, $Fe_{3-x}O_4$, with a plasmonic metal (Au), has been shown to produce magneto-plasmonic bi-functionality [98], [99], [102], [103]. Magneto-optical materials with ferromagnetic/superparamagnetic and plasmonic properties have been explored for dual magnetic imaging and photothermal cancer therapies as well as

magnetically enhanced photothermal therapy [97], [99], [103], [104]. As an alternative to Au, Ag possesses a greater plasmonic quality factor, while also being immiscible with Fe. Fe and Ag have different crystal structures (BCC vs FCC), as well as a large discrepancy in atomic radii (140 pm vs 160 pm), causing the system to be immiscible, even in the liquid phase up to 4800 K. Sputter deposition, however, has successfully proven to be an effective method of obtaining metastable alloys which can extend the solubility limits [105]. Early work exploring this binary system by Takao *et al.* involved co-evaporation and magnetic measurement of a $Ag_{0.5}Fe_{0.5}$ system, showing changes in coercivity as a function of heat treatment [106]. Later work included Mössbauer spectroscopy of evaporated $Ag_{0.99}Fe_{0.01}$ and $Ag_{0.7}Fe_{0.3}$ alloys, detailing alloy formation of nanocrystalline grains [107], [108], as well as work detailing a shift in magnetic moment and lattice size across the Ag-Fe phase diagram [105]. Notably, the vapor quenched films demonstrated composition regions with all FCC (Ag-rich), all BCC (Fe-Rich) and mixed phases with supersaturated compositions. The magnetic influence of Fe and its atomic volume in various binary systems, including $Ag_{0.5}Fe_{0.5}$, has also been calculated [109]. In this paper, we systematically investigate the optical properties, magnetic properties, and crystal structure of the Ag_xFe_{1-x} alloy system sputtered across a wide range of phase space ($0.19 < x < 0.84$) in the metastable as-deposited and phase-separated annealed form.

Materials and Methods

In this study, 300 nm of Ag_xFe_{1-x} films were deposited via RF magnetron sputtering, where the Ag and Fe were co-sputtered from elemental targets in order to control the composition and to induce a compositional gradient. Sputtering was carried out at a base

pressure of $1x10^{-7}$ Torr, a working pressure of 5 mTorr with an Ar gas flow rate of 25 sccm. The powers applied to the Ag and Fe targets were 30 W and 140 W, respectively, which yield similar sputtering rates of 2 nm/min. The substrate, a 25 × 100 mm [100] polished Si wafer strip, was oriented such that one end was positioned near the Ag sputter target, and the other near the Fe sputter target (see diagram in Figure 3.17), thus creating a composition gradient across the wafer, where one end is Ag-rich, and the other Fe-rich.

Energy Dispersive X-ray Spectroscopy

To determine the compositions of the samples, a series of Energy Dispersive X-ray Spectroscopy (EDS) scans were performed along the composition gradient in 10 mm increments using a Carl Zeiss EVO SEM. The atomic composition for the sample, Figure 3.17, shows a relatively linear gradient of 0.86 at%/mm across the wafer with an approximately equiatomic composition at the wafer center.

X-ray Diffraction

X-ray diffraction (XRD) and phase identification was carried out using a Malvern Panalytical X'Pert3 MRD in a grazing incidence geometry, illuminating a 4 × 9 mm region. The substrate was oriented such that the long axis of the x-ray beam was perpendicular to the composition gradient, with the 4 mm beam width capturing a compositional range of ≈ 3.4 at.%. The incident angle was fixed at 12° and the detector angle was swept from 25° to 90°. Measurements were taken on both the as-deposited sample as well as a sample that was annealed at 873 K under vacuum for 1 hour.

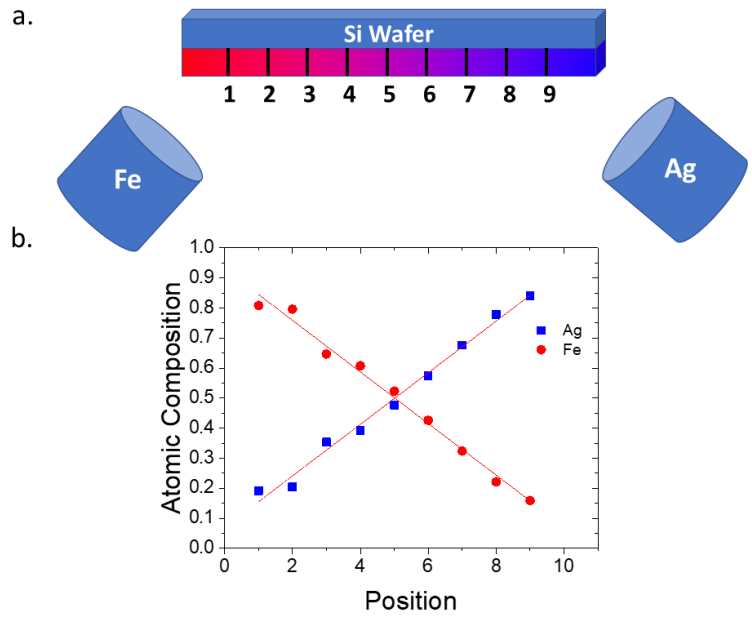

Figure 3.17: a) Schematic illustrating the location of the sputtering targets and the sample positions. b) Measured EDS composition as a function of position and linear fit to the data relative to position. Sample size is 25 × 100 mm, with 10 mm between each position in both (a) and (b).

TEM

In-situ grain growth and phase separation experiments were performed by depositing a 20 nm thick film of $Ag_{0.5}Fe_{0.5}$ on a transmission electron microscope (TEM) membrane, then using a monochromated Carl Zeiss LIBRA 200 MC (S)TEM equipped with a laser delivery system (Waviks Inc.) to photothermally heat the sample [110]. The operating voltage was set to 200 kV and TEM bright field and high angle annular dark field

(HAADF) scanning transmission electron micrographs (STEM) images were collected at 10 kX and 30 kX magnification. Selected area electron diffraction (SAED) patterns were also collected using a 5 μm aperture and radially averaged and normalized as described previously [91].

Electron energy loss spectroscopy (EELS)

STEM EELS was conducted on a Zeiss Libra TEM with an accelerating voltage of 200 keV, a convergence semi-angle of 0 mrad, and a collection semi-angle of 100 mrad. For data acquisition, a 0.5 μm monochromator slit with a dispersion of 30 meV per channel was used. The spectrum image was collected using a 29 x 23 grid of 4.4 nm square pixels and a dwell time of 0.02 s.

Ellipsometry

To measure the complex dielectric function, a J.A. Woolam M-2000U variable-angle spectroscopic ellipsometer was used, and data were collected in an energy range of 1.24 – 5.06 eV. No dispersion model was used to fit the results, as no suitable model for polycrystalline alloy films exists due to the complex phase structure, crystalline size, and energy band composition. Instead, Re(ε) and Im(ε) were obtained via point-by-point fitting of the calculated data.

Magnetometry

Magnetometry measurements were performed using a vibrating sample magnetometer (VSM) at temperatures between 1.9 K and 400 K. Temperature dependent magnetization (M-T) measurements in field cooled regime were performed by heating the

sample to 400 K, applying a static 5 mT magnetic field, then cooling to 1.9 K while measuring the magnetization. The sample was then heated back to 400 K, a static magnetic field of 8.5 T was applied, and the sample was cooled to 1.9 K. Major hysteresis loops were recorded by measuring the magnetization versus magnetic field, M-H, at fixed temperatures. Measurements were performed on ten samples – five compositions, each as-deposited and annealed. The results were normalized to the volume of the measured films.

Results and Discussion

In order to better correlate atomic composition and thickness to the structural and optical properties of these alloys, a computational model was developed to estimate the film composition and thickness as a function of position across the 100 mm diameter substrate. This model is capable of predicting the atomic composition at any point on the substrate based on the sputtering rates of the individual sputtering sources, their material properties, as well as the necessary angular distribution of species emanating from the target.

For this model, each of the four sputter guns in this deposition system is modeled as an individual Knudson surface source, where the sputtering flux per unit area is given by the equation

$$\frac{d\overline{M_s}}{dA_s} = \frac{\overline{M_T}(n+1)cos^n\varphi\ cos\theta}{2\pi r^2}$$

Where dM_s/dA_s is the mass deposited per unit area and M_T is the total sputtered mass from the target. Here, φ is the angle between the target surface normal and a line extending from the center of the target to a given point on the substrate surface, n is the degree of flux forward peaking, and has been determined experimentally to be ≈12 [89], due to the targets being positioned inside 50 mm tall stainless steel chimneys in order to minmize cross-contamination. As the targets are not perpendicular to the substrate, θ is introduced, and is defined as the angle between the substrate surface normal and a line extending from the center of the target surface to a given point on the substrate surface. Finally, *r* is the distance from the center of the target to a given point on the substrate surface.

The computational estimates of the substrate composition and thickness are shown in Figure 3.18, with a dashed box indicating sample substrate and orientation relative to whole 100 mm diameter wafer. The results of Figure 3.18a and the EDS results in Figure 3.17 show good agreement.

As silver and iron are immiscible at room temperature, thermodynamically we expect the alloy to be phase-separated. Figure 3.19 illustrates the FCC-derived [111] XRD peaks as a function of position for (a) the as-deposited and (b) annealed film. In the as-deposited samples, as the Fe concentration increases, the Ag [111] peak shifts to a higher 2θ values, indicating a decrease in lattice size. The atomic radius of silver is 160 pm and the lattice parameter of FCC silver is 0.409 nm, whereas the atomic radius of iron is 140 pm and the lattice parameter of BCC iron is 0.2856 nm. The persistence of the (111) peak across virtually all compositions and the decrease in the lattice parameter suggests that the

smaller iron atoms substitutionally occupy the silver lattice positions, forming a metastable solid solution in the alpha (FCC) configuration. The amount of iron in this alpha phase can be calculated assuming Vegard's Law based on the atomic radii, as plotted in (c). Up to ≈12% of Fe is accommodated in the silver lattice, which is supersaturated relative to the room temperature thermodynamically limited (<1%) miscibility of Fe in Ag. After annealing, the (111) diffraction peak maintains a constant position over the composition range, indicating the out-diffusion of the supersaturated Fe and phase separation into nearly pure Fe and Ag phases. This is further explored in the TEM section.

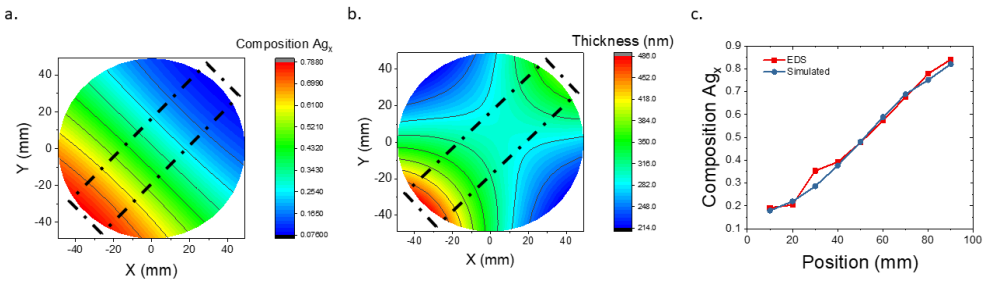

Figure 3.18: 2D projection map of (a) Ag composition (x) in the Ag_xFe_{1-x}, (b) total thickness, and (c) plot comparing experimental Ag EDS composition and calculated Ag composition versus position on the substrate. Both maps are plotted for a 100 mm diameter wafer, with a dashed area indicating the 25 ×100 mm sample region.

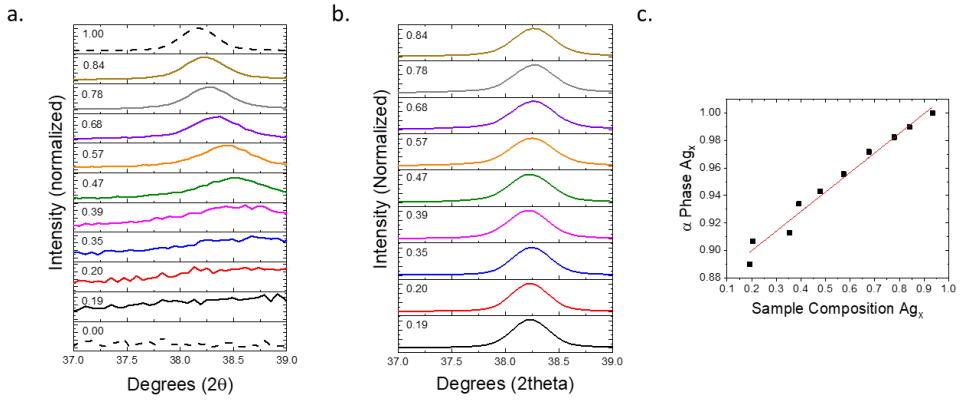

Figure 3.19: Plot of the Ag [111] XRD peak, both as-deposited (a) and after annealing (b). For both (a) and (b), the peaks are labeled as a function of Ag sample composition as determined by EDS, as shown in Figure 3.17. The atomic composition of the as-deposited Ag peak in (a) is plotted in (c) also as a function of Ag sample composition. In (a), the dashed lines indicate XRD taken from reference samples.

The as-deposited films demonstrate a continuous shift in the dielectric constant as the film composition varies from iron rich to silver-rich, as shown in Figure 3.20. Not surprisingly, as the silver concentration is increased, the localized surface plasmon resonance (LSPR) quality factor (Q), which measures the suitability of an alloy as a plasmonic material, increases significantly (Fig. 3.20 c and d). Additionally, the peak in the Q factor over the spectroscopic range measured shifts to higher energy side with increasing silver concentration. In the silver-rich region, Re(ε) has a large negative value and a small Im(ε) value, demonstrating good low-energy plasmonic behavior.

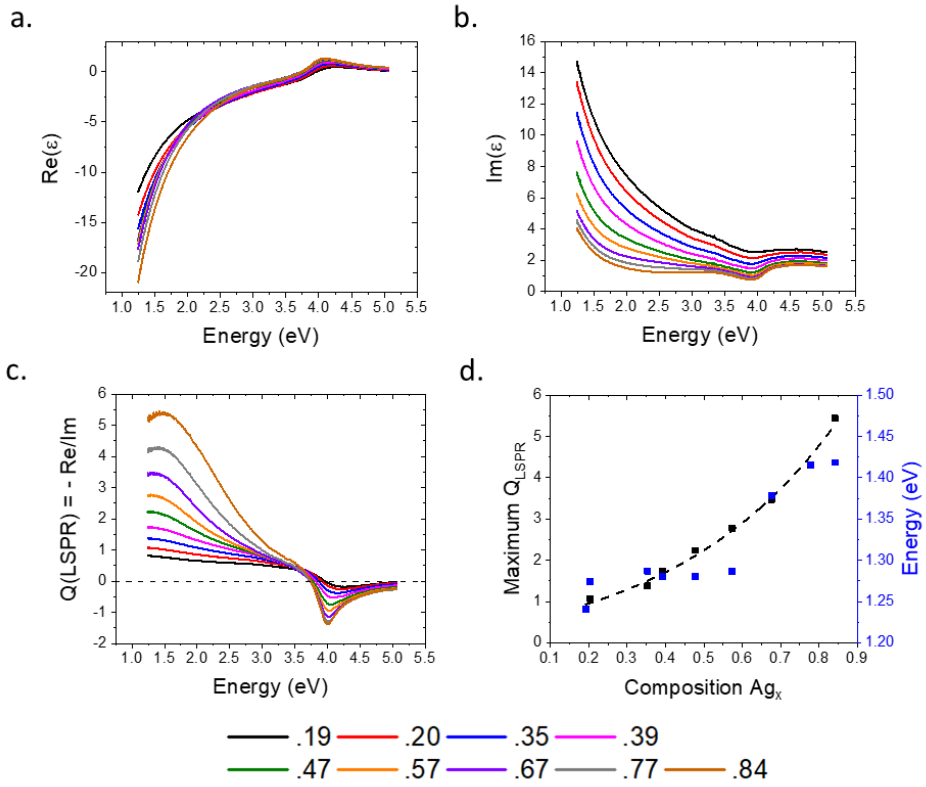

Figure 3.20: real (a) and imaginary (b) parts of the dielectric function for the annealed films, (c) corresponding Q_{LSPR} factors, and (d) maximum Q_{LSPR} and peak energy as a function of sample composition. Panels a-c are plotted for the different of Ag concentrations, as shown in the legend.

To verify and characterize the phase separation, scanning electron microscopy (SEM) images were taken before and after annealing of the samples, where images were taken every 10 mm. Before annealing, the AgFe films are nanogranular across the sample gradient with very little phase contrast, as shown in Figure 3.21. The grain size increases linearly as the composition shifts from iron-rich to silver-rich (Figure 3.21 m), which is

explained by silver's higher melting temperature and larger crystal structure. After annealing for 1 hour at 873 K in vacuum, the Ag and Fe phase separate, and grain growth is induced. On the iron-rich side (positions 1- 4), the grain size stays roughly the same size as the as-deposited film (35-45 nm in diameter), but the Ag (lighter) and Fe (darker) separate and form distinct grains throughout the film. Once the film reaches an equiatomic composition, larger grain sizes are observed, forming Fe rich and Ag rich regions. Moving towards the Ag rich side (positions 6-9), the Fe grains become smaller as the phase fraction decreases, forming islands in the semi-continuous Ag film. Excess silver also starts to precipitate out of the film, creating particles as large as 2 μm in diameter.

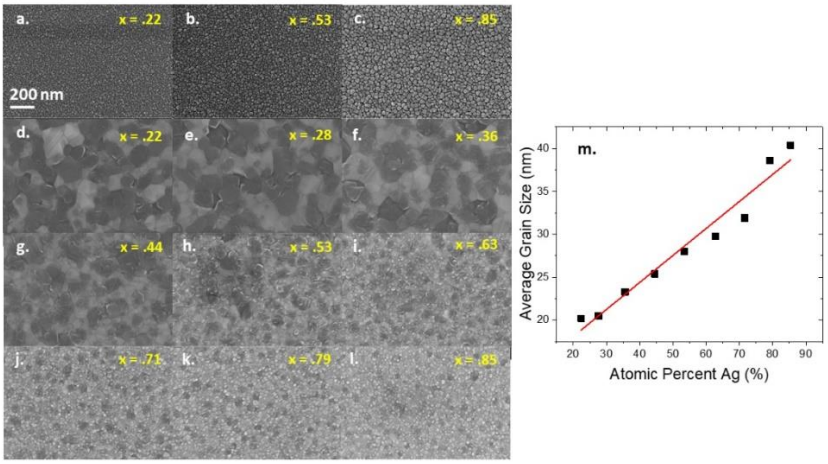

Figure 3.21: SEM images of the as-deposited Ag_xFe_{1-x} film (a-c); SEM images of the Ag_xFe_{1-x} film annealed at 873 °C for 1 hour under vacuum (d-l); (m) average grain size (diameter) in the as-deposited sample as a function of Ag composition. In a-l, the scale bar (bottom left of a) is 200 nm and applies to all the SEM images.

To further explore the grain growth and phase separation in the Ag-Fe alloy, a 20 nm thick $Ag_{0.5}Fe_{0.5}$ film was sputtered onto a 20 nm SiO_2 TEM membrane then imaged after *in-situ* laser annealing. To induce grain growth and phase separation, the pulsed laser was focused at the TEM grid for five minutes at ≈ 25 mW, 200 µs at 100 Hz (2% duty cycle). The laser spot has an approximately Gaussian profile with a $1/e^2$ radius of ≈ 3.7 µm. Images were taken near the laser center every minute during the laser exposure). Subsequent to the laser exposure/heat treatment, TEM images, STEM images, and SAED patterns were taken every 1.5 µm up to 12 µm moving radially out from the spot center representing different annealing temperatures.

Figure 3.24 a-c illustrate a finite element thermal simulation based on the as-deposited index of refraction, as estimated via the spectroscopic ellipsometry and averaged physical properties of Ag and Fe. As shown in Fig. 3.24a, the model predicts that the center of the beam reaches a steady-state maximum temperature of 1180 K in 55 µs and the peak temperature logically drops (b), to where the position 12 µm from the spot center reaches ≈ 560 K (c), well below the annealing temperature explored in the larger sample (873 K). Based on the ≈150 µs time at steady state per pulse, the cumulative annealing time at the maximal temperature is only 4.5 s (30000 pulses).

A wide view image of the illuminated area is shown in d and highlights the position-dependent changes in the microstructure; the vector illustrating the sequence of images in e - m are shown as a yellow arrow. At the peak center (0 and 1.5 µm, e and f), solid state dewetting has occurred and nanoparticles result. The very center contains all spherical particles and the SAED pattern suggests that silver has preferentially evaporated due to its

higher vapor pressure. This dewetting is shown in greater detail in Figure 3.22, where it is observed that, as the film dewets, a large (several micron) hole forms in the center of the laser spot. Because of this phenomenon, much of the energy in the center of the beam passes through the membrane rather than coupling to the deposited alloy, which in turn effects the annealing temperature of the film. To better understand these effects, several additional simulations were run with varied hole sizes, as shown in Figure 3.23.

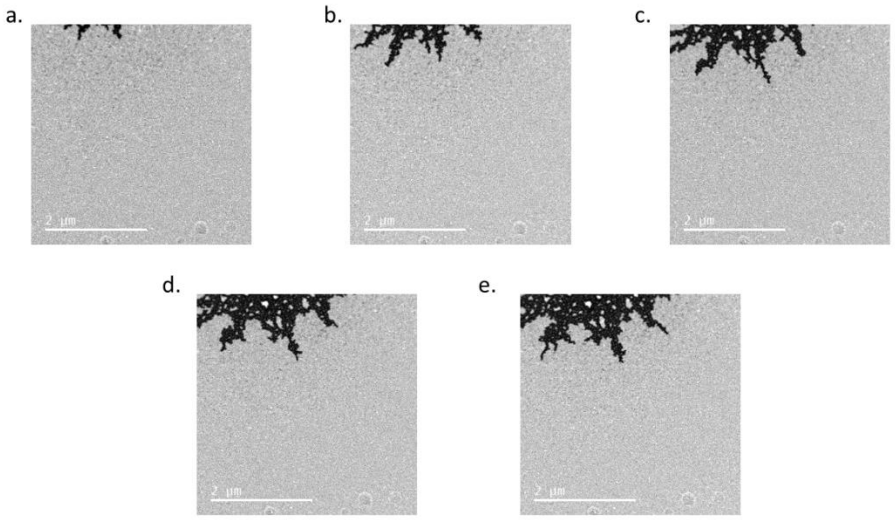

Figure 3.22: TEM images taken near the laser center after 1 (a), 2 (b), 3 (c), 4 (d), and 5 (e) minutes of laser heating in the TEM

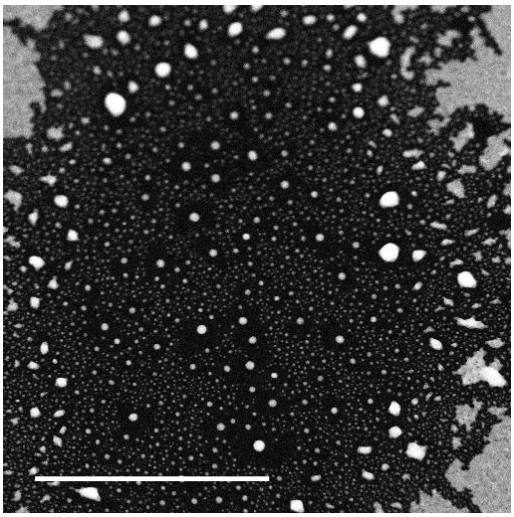

Figure 3.23: TEM image taken in the center of the laser spot after the 5-minute laser exposure illustrating the dewetting/hole formation.

At the 1.5 μm position (Fig. 3.24f), bi-metallic nanoparticles are evident where small Fe nanoparticles decorate larger silver cores and some small Fe-Ag Janus nanoparticles exist. At 3.0 μm and 4.5 μm (g and h) partial dewetting is observed, and in the film regions, small scale phase separation and grain growth occurs. At radii > 4.5 μm (i-m) dewetting does not occur and the degree of phase separation and grain growth decreases with increasing radius, eventually resembling the as-deposited condition at 12 μm. Interestingly, at ≈ 9 μm, corresponding to an annealing temperature of ≈ 650 K, large (several hundred nm) silver nanoparticles precipitate where the continuous films are nanogranular.

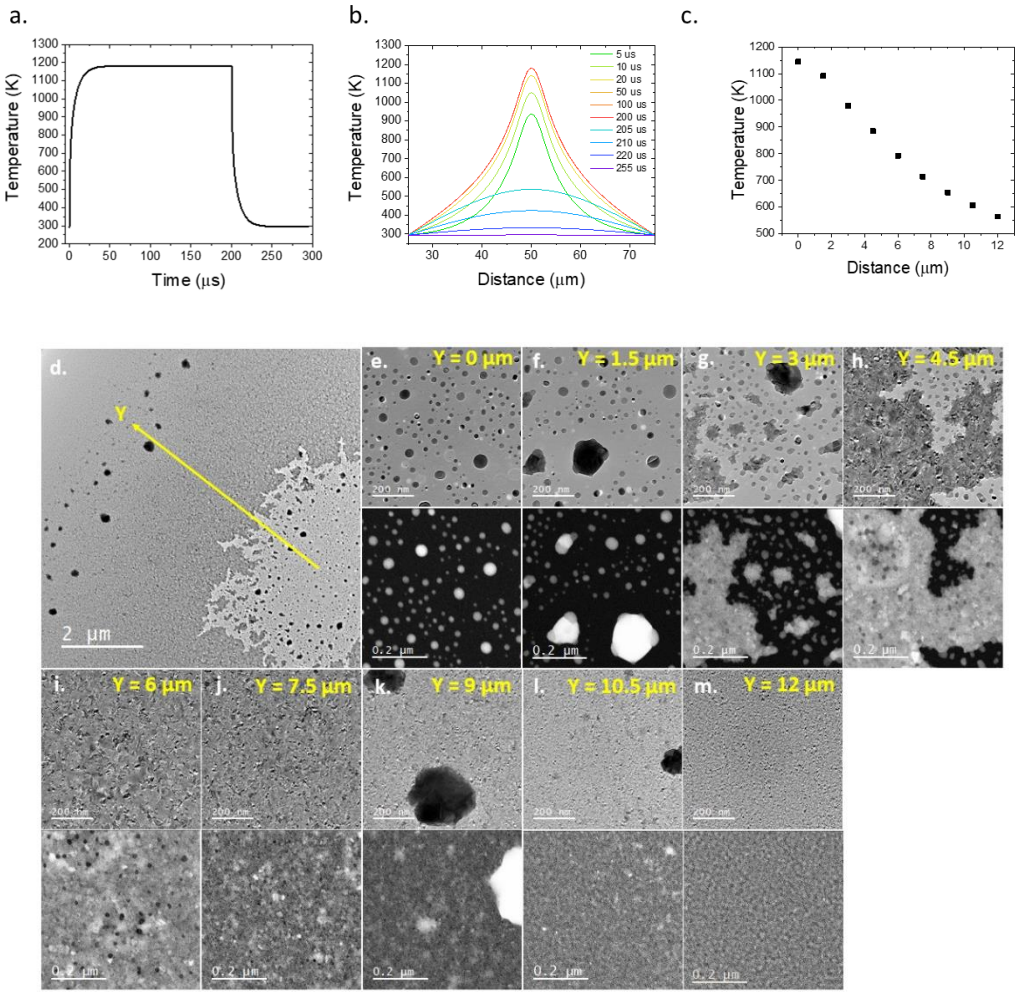

Figure 3.24: (a) Time-temperature plot from a finite element photothermal simulation of a 20 nm thick $Ag_{0.5}Fe_{0.5}$ film on a 20 nm SiO_2 membrane exposed to a 25-mW laser. (b) Simulated surface temperature versus laser spot position for various times illustrating the spatial and temporal temperature evolution for a 25 mW power and 200 μs pulse width. (c) Plot correlating position of images taken in (e-m) to the relative annealing temperature, as shown in (b). (d) Micrograph overview of laser spot, with close up images taken 1.5 μm apart in (e-m). For each set of images, the bright field TEM image is above, and the HAADF STEM image is below.

In agreement with the results shown in Figure 3.24, the SAED shows that phase separation increases with increasing photothermal heating, as shown in Figure 3.25. SAED measurements towards the center of the laser spot (Fig. 3.25 a), indicate phase separation, as demonstrated by the shift to lower wavenumber of the Ag peak, and the shift to higher wavenumber of the Fe peak. Using the simulated laser conditions above, we can then correlate the shift in the Ag and Fe peaks to a necessary annealing temperature required to induce this shift, and shown in Fig. 3.25 b-c. Note that the SAED measurements could not be performed at < 3 μm from the center of the laser spot due to diffraction overexposure.

During the in-situ laser heating STEM experiments, phase separated nanoparticles were formed on the suspended membranes. Particles very similar to these have been described as "Nano-fried-eggs," and are characterized by a FCC crystalized silver region surrounded by amorphous iron regions [111]. Low-loss EELS was used to measure the plasmonic spectrum of these nanoparticles. Figure 3.26a shows the STEM image for one of these particles (a silver central region with two iron regions at the poles) and its associated EELS spectrum images b-d at various loss energies. For better visualization, the outline of the nanoparticle is superimposed over the spectrum images in black. In the Fe phase at the tips of the elongated nanoparticle, the bulk surface plasmon peaks can be clearly seen at 2.62 eV (b), as well as for another particle at the top of the image. A dipole peak associated with an ≈ 40 nm central Ag region is also observed at 3.05 eV (c), and is in good agreement with previous work on dewet silver nanoparticles of [112]. Finally, the silver bulk surface plasmon peak is observed at ≈3.50 eV (d).

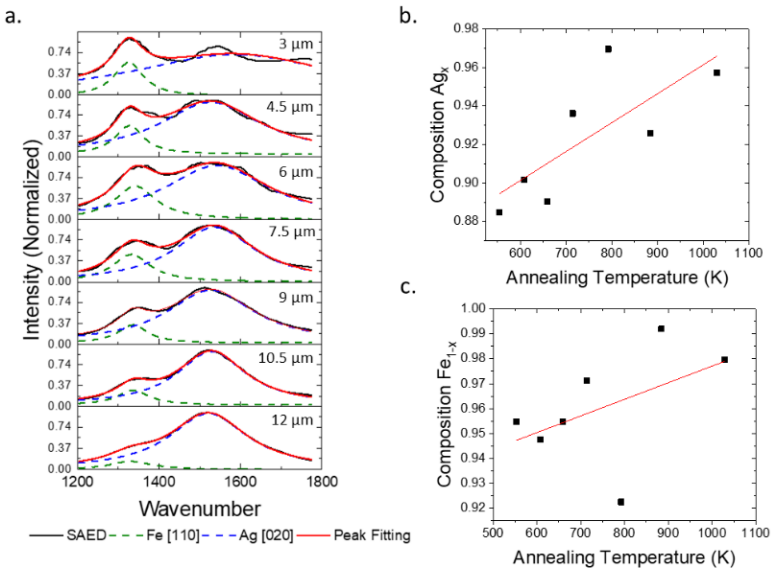

Figure 3.25: (a) Radially averaged and normalized selected area electron diffraction patterns and fitted Ag and Fe peaks as a function of distance from the center of the laser spot, as shown in Figure 6 d. Composition of the Fe BCC [110] peak (b) and the Ag FCC [020] peak (c) plotted as a function of annealing temperature determined from Figure 3.24 c.

As demonstrated in figure 3.26 (a), various nanoparticle sizes and shapes were generated via the photothermal heating of the thin film. We envision that nanoparticle arrays of various sizes and compositions can be made via pulsed laser induced dewetting (PLID) [113]. The phase fraction of Ag and Ni can be controlled by the original thin film composition and the average particle size can be controlled by the thin film thickness. Furthermore, precise hierarchical one [114] and two [115] dimensional nanoparticle arrays

can also be achieved. Thus, as we recently demonstrated in the Ag_xNi_{1-x} system [116], the dipolar plasmonic energy can be tuned by the resultant Ag nanoparticle volume and the magnetic moment per nanoparticle tuned by the Fe volume.

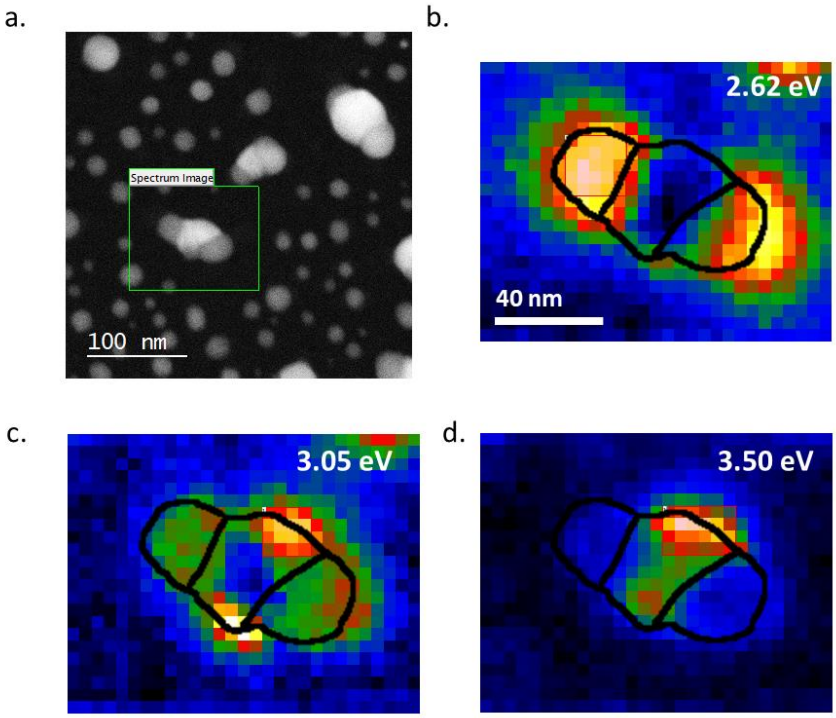

Figure 3.26: (a) HAADF STEM image of an Ag-Ni nanoparticle, and associated EELS spectrum images for the (b) Fe bulk surface plasmon peak, (c) the Ag dipole peak, and (d) the Ag bulk surface plasmon peak. For a-c, the scale bar (shown in the bottom right corner of b) is 40 nm.

The saturation magnetization for five compositions between 15 at.% Fe and 78 at.% Fe, both annealed and as-deposited, were measured at 1.9 K and are tabulated in Figure 3.27a. These results show a non-linear increase in the total moment approaching the Fe-rich samples, which does not change significantly with annealing. The non-linearity suggests that there may be some non-ferromagnetic ordering. Magnetization versus temperature measurements, shown in Figure 3.27b, support this claim. Samples with 78 at.% Fe, 65 at.% Fe, and 50 at.% Fe show a distinct drop in the magnetization when cooling below 120 K, suggesting the onset of a new magnetic ordering. The M-T plots for the 30 at.% Fe and 15 at.% Fe do not have this drop. These plots all show a protracted shallow curve, suggesting that the Curie temperature, T_C, is well above 400 K, which is consistent for Fe – which has a T_C of 1043 K.

Magnetic hysteresis loops measured below 120 K show an enhanced loop width (e.g. coercivity) and a shift along the field axis away from center (e.g. loop bias). These effects are well known and correspond to exchange bias, which results from the coupling between a ferromagnet and an antiferromagnet [117]. This suggests that the FeAg has an antiferromagnetic phase with a Néel temperature of ≈120 K, as suggested by the M-T plots. After annealing, the hysteresis loops measured above 120 K show an increased coercivity. This is likely due to pinning of the domain walls by Ag precipitates. Below 100 K the annealed loops also show an increase in the coercivity, albeit much smaller than the as-deposited sample, and also show no loop bias. This is likely a consequence of the phase separation, which reduces the antiferromagnetic phase fraction by precipitating separate Fe

and Ag regions and decreases the contact boundary between the ferromagnetic and antiferromagnetic regions.

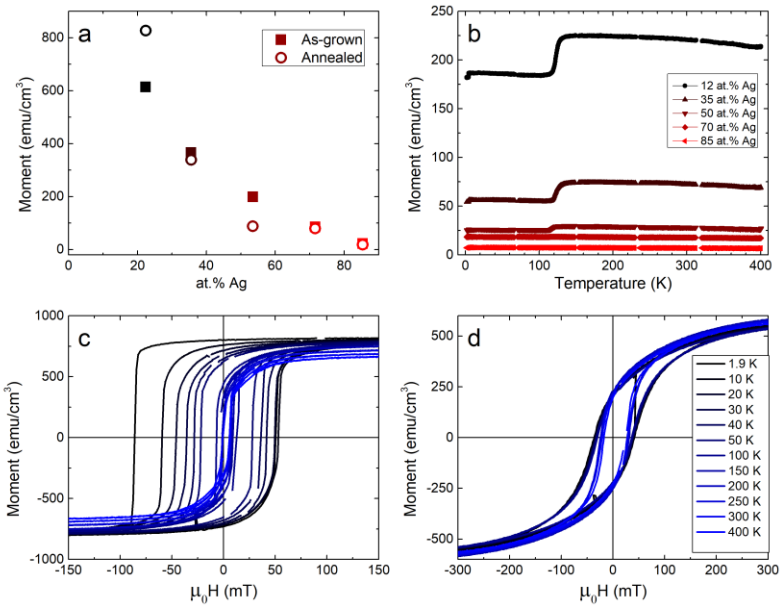

Figure 3.27: (a) Saturation magnetization versus composition, (b) M-T curves from the annealed samples, and major hysteresis loops for the 78 at.% Fe sample (c) as-deposited and (d) after annealing.

Conclusion

In conclusion, we have demonstrated that fast quenching in sputter deposited Ag_xFe_{1-x} results in a metastable supersaturated Ag-rich solid solution. Annealing of the films at 873 K for 1 hour was sufficient for the solid solution to phase separate into the

equilibrium Ag and Ni phases. The composition of the Ag_xFe_{1-x} alloy for both as deposited and annealed samples were analyzed via EDS, showing a silver gradient ranging from ($0.19 < x < 0.84$), allowing for the rapid characterization of the structural, optical and magnetic properties of the Ag_xFe_{1-x} system. The structural properties were characterized via SEM and TEM imaging, XRD, and SAED. The SEM and TEM imaging revealed no contrast in the as-deposited film, consistent with a nanogranular supersaturated solid solution. The annealed films revealed clear phase contrast indicative of the Ag and Ni phase separation. XRD and SAED patterns confirmed the observed phase separation in the annealed films. The optical properties were characterized via spectroscopic ellipsometry, and confirmed the expected decrease in the LSPR Q factor as the silver concentration increased. STEM of an annealed film resulted in phase separated Ag-Ni nanoparticles and the plasmonic properties were correlated via low-loss EELS. Finally, the magnetic behaviors of the films were analyzed by studying M-T and M-H measurements taken via a VSM and revealed a non-linear increase in the total moment approaching the Fe-rich samples, which suggests that there may be some non-ferromagnetic ordering. Magnetic hysteresis loops measured as a function of temperature revealed exchange bias below 120 K, which suggests that the Ag_xFe_{1-x} has an antiferromagnetic phase with a Néel temperature of ≈120 K. Thus, the demonstrated magnetic and plasmonic properties of phase-separated Ag_xFe_{1-x} alloys have promise in magnetoplasmonic applications such as combined magnetic resonance imaging and magnetically enhanced photothermal cancer therapy.

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APPENDIX

```
clear all;

ElementLibrary;

n = 12; %peak forwarding factor
gundistance = 25; %distance between guns in sputter chamber
avagadro = 6.02e+23; %constant

disp('Default gun tilt is 32.7 degrees'); %option to alter gun tilt
tiltoption = input('Would you like to alter sputter gun tilt? y/n  ','s');
if tiltoption == 'y'
   tilt1 = input('Enter tilt of gun 1 (degrees):  ');
    tilt2 = input('Enter tilt of gun 2 (degrees):  ');
     tilt3 = input('Enter tilt of gun 3 (degrees):  ');
      tilt4 = input('Enter tilt of gun 4 (degrees):  ');
else
   tilt1 = 32.7;
   tilt2 = 32.7;
   tilt3 = 32.7;
   tilt4 = 32.7;
end

disp('Default substrate height is 15 cm'); %option to alter substrate height
heightoption = input('Would you like to alter the substrate height? y/n  ','s');
if heightoption == 'y'
   zheight = input('Enter substrate height (cm):  ');
else
   zheight = 15;
end

disp('Enter the name or abbreviation of each target (e.g. Gold or Au) from the element
library, or enter 0 to input atomic weight and density manually');
disp('If sputtering with less than 4 targets, simply add in placeholder elements on empty
guns and set sputter rate to 0');
element1 = input('Enter element of gun 1:  '); % gun 1 element
if element1 == 0
   mass1 = input('Enter atomic mass in amu:  ');
   density1 = input('Enter atomic density in g/cm^3:  ');
else
   mass1 = element1(1,1);
   density1 = element1(1,2);
end

element2 = input('Enter element of gun 2:  '); % gun 2 element
```

```
if element2 == 0
   mass2 = input('Enter atomic mass in amu:  ');
   density2 = input('Enter atomic density in g/cm^3:  ');
else
   mass2 = element2(1,1);
   density2 = element2(1,2);
end

element3 = input('Enter element of gun 3:  '); % gun 3 element
if element3 == 0
   mass3 = input('Enter atomic mass in amu:  ');
   density3 = input('Enter atomic density in g/cm^3:  ');
else
   mass3 = element3(1,1);
   density3 = element3(1,2);
end

element4 = input('Enter element of gun 4:  '); % gun 4 element
if element4 == 0
   mass4 = input('Enter atomic mass in amu:  ');
   density4 = input('Enter atomic density in g/cm^3:  ');
else
   mass4 = element4(1,1);
   density4 = element4(1,2);
end

dm1 = density1/mass1;
dm2 = density2/mass2;
dm3 = density3/mass3;
dm4 = density4/mass4;
%enter sputter rates for each gun

sputterrate1 = input('Enter sputter rate for gun 1 in nm/min: ');
sputterrate2 = input('Enter sputter rate for gun 2 in nm/min: ');
sputterrate3 = input('Enter sputter rate for gun 3 in nm/min: ');
sputterrate4 = input('Enter sputter rate for gun 4 in nm/min: ');

%total sputter time (minutes)
time = input('Enter total sputter time in min  ');

radiusincrement = input('Enter radial increment in cm  '); %define points on wafer
thetaincrement = input('Enter theta increment in degrees  '); %define points on wafer
disp('Open file labeled "resultsfinal" for thickness and atomic % plots');
```

```
disp('For gradients from guns opposite each other, open files "gradient1to3" or
"gradient2to4"');


v1start = [-gundistance/2, -gundistance/2, -zheight]; %sputter gun locations
v2start =  [-gundistance/2, gundistance/2, -zheight];
v3start =  [gundistance/2, gundistance/2, -zheight];
v4start =  [gundistance/2, -gundistance/2, -zheight];

finalangle1 = (90-tilt1); %sputter gun tilts (90 being straight up, 0 being horizontal)
finalangle2 = (90-tilt2);
finalangle3 = (90-tilt3);
finalangle4 = (90-tilt4);
diagonalgundistance = gundistance*sqrt(2);

if finalangle1 == 90 %takes care of gun pointing straight up
   radialfinalposition1 = gundistance*sqrt(2);
else
   radialfinalposition1 = (diagonalgundistance/2) - (zheight/tan(finalangle1*pi/180));
end

if finalangle2 == 90 %takes care of gun pointing straight up
   radialfinalposition2 = gundistance*sqrt(2);
else
   radialfinalposition2 = (diagonalgundistance/2) - (zheight/tan(finalangle2*pi/180));
end

if finalangle3 == 90 %takes care of gun pointing straight up
   radialfinalposition3 = gundistance*sqrt(2);
else
   radialfinalposition3 = (diagonalgundistance/2) - (zheight/tan(finalangle3*pi/180));
end

if finalangle4 == 90 %takes care of gun pointing straight up
   radialfinalposition4 = gundistance*sqrt(2);
else
   radialfinalposition4 = (diagonalgundistance/2) - (zheight/tan(finalangle4*pi/180));
end


position1 = radialfinalposition1/sqrt(2);
position2 = radialfinalposition2/sqrt(2);
position3 = radialfinalposition3/sqrt(2);
position4 = radialfinalposition4/sqrt(2);
```

```
v1final = [-position1 -position1 0]; %define point that sputter gun vector contacts
substrate
v2final = [-position2 position2 0];
v3final = [position3 position3 0];
v4final = [position4 -position4 0];

thetatotal = 360/thetaincrement;
k=1;
l=1;

for i=1:1:5/radiusincrement %two for loops that will sweep through wafer points
   for j=1:1:thetatotal
   r(i,j) = (i-1)*radiusincrement;
   theta(i,j) = (j-1)*thetaincrement;

   x(i,j) = r(i,j).*cos(theta(i,j).*pi/180);
   y(i,j) = r(i,j).*sin(theta(i,j).*pi/180);
   point = [x(i,j) y(i,j) 0];
   pointcenter = [0 0 0];


   target1norm(i,j) = norm(v1final - v1start);
   target2norm(i,j) = norm(v2final - v2start);
   target3norm(i,j) = norm(v3final - v3start);
   target4norm(i,j) = norm(v4final - v4start);

   target1normcenter = norm(v1final - v1start); %determinecenter
   target2normcenter = norm(v2final - v2start);
   target3normcenter = norm(v3final - v3start);
   target4normcenter = norm(v4final - v4start);

   r1(i,j) = norm(point - v1start);
   r2(i,j) = norm(point - v2start);
   r3(i,j) = norm(point - v3start);
   r4(i,j) = norm(point - v4start);

   r1center = norm(pointcenter - v1start);
   r2center = norm(pointcenter - v2start);
   r3center = norm(pointcenter - v3start);
   r4center = norm(pointcenter - v4start);

   thetafinal1(i,j) = acos(dot((v1final-v1start),(point-v1start))/(target1norm(i,j)*r1(i,j)));
```

```
   thetafinal2(i,j) = acos(dot((v2final-v2start),(point-v2start))/(target2norm(i,j)*r2(i,j)));
   thetafinal3(i,j) = acos(dot((v3final-v3start),(point-v3start))/(target3norm(i,j)*r3(i,j)));
   thetafinal4(i,j) = acos(dot((v4final-v4start),(point-v4start))/(target4norm(i,j)*r4(i,j)));

   thetafinal1center = acos(dot((v1final-v1start),(pointcenter-
v1start))/(target1normcenter*r1center));
   thetafinal2center = acos(dot((v2final-v2start),(pointcenter-
v2start))/(target2normcenter*r2center));
   thetafinal3center = acos(dot((v3final-v3start),(pointcenter-
v3start))/(target3normcenter*r3center));
   thetafinal4center = acos(dot((v4final-v4start),(pointcenter-
v4start))/(target4normcenter*r4center));

   phivector = [0 0 1];
   phinorm = norm(phivector);

   phi1(i,j) = acos(dot(point - v1start, phivector)/(phinorm*r1(i,j)));
   phi2(i,j) = acos(dot(point - v2start, phivector)/(phinorm*r2(i,j)));
   phi3(i,j) = acos(dot(point - v3start, phivector)/(phinorm*r3(i,j)));
   phi4(i,j) = acos(dot(point - v4start, phivector)/(phinorm*r4(i,j)));

   phi1center = acos(dot(pointcenter - v1start, phivector)/(phinorm*r1center));
   phi2center = acos(dot(pointcenter - v2start, phivector)/(phinorm*r2center));
   phi3center = acos(dot(pointcenter - v3start, phivector)/(phinorm*r3center));
   phi4center = acos(dot(pointcenter - v4start, phivector)/(phinorm*r4center));

   comp1(i,j) =
sputterrate1*(n+1)*(cos(thetafinal1(i,j)))^n*cos(phi1(i,j))/(2*pi*r1(i,j)^2);
   comp2(i,j) =
sputterrate2*(n+1)*(cos(thetafinal2(i,j)))^n*cos(phi2(i,j))/(2*pi*r2(i,j)^2);
   comp3(i,j) =
sputterrate3*(n+1)*(cos(thetafinal3(i,j)))^n*cos(phi3(i,j))/(2*pi*r3(i,j)^2);
   comp4(i,j) =
sputterrate4*(n+1)*(cos(thetafinal4(i,j)))^n*cos(phi4(i,j))/(2*pi*r4(i,j)^2);

   comp1center =
sputterrate1*(n+1)*(cos(thetafinal1center))^n*cos(phi1center)/(2*pi*r1center^2);
   comp2center =
sputterrate2*(n+1)*(cos(thetafinal2center))^n*cos(phi2center)/(2*pi*r2center^2);
   comp3center =
sputterrate3*(n+1)*(cos(thetafinal3center))^n*cos(phi3center)/(2*pi*r3center^2);
   comp4center =
sputterrate4*(n+1)*(cos(thetafinal4center))^n*cos(phi4center)/(2*pi*r4center^2);
```

```
    if sputterrate1 == 0 factor1(i,j) = comp1(i,j)*0;
  else factor1(i,j) = comp1(i,j)/(comp1center);
    end
    if sputterrate2 == 0 factor2(i,j) = comp2(i,j)*0;
  else factor2(i,j) = comp2(i,j)/(comp2center);
    end
    if sputterrate3 == 0 factor3(i,j) = comp3(i,j)*0;
  else factor3(i,j) = comp3(i,j)/(comp3center);
    end
    if sputterrate4 == 0 factor4(i,j) = comp4(i,j)*0;
  else factor4(i,j) = comp4(i,j)/(comp4center);
    end


  volume1 = sputterrate1*time*1e-7; %assumes an area of 1cm^2
  volume2 = sputterrate2*time*1e-7;
  volume3 = sputterrate3*time*1e-7;
  volume4 = sputterrate4*time*1e-7;

  atomic1(i,j) = density1/(mass1/avagadro)*volume1*factor1(i,j);
  atomic2(i,j) = density2/(mass2/avagadro)*volume2*factor2(i,j);
  atomic3(i,j) = density3/(mass3/avagadro)*volume3*factor3(i,j);
  atomic4(i,j) = density4/(mass4/avagadro)*volume4*factor4(i,j);


  atomicpercent1(i,j) =
atomic1(i,j)/(atomic1(i,j)+atomic2(i,j)+atomic3(i,j)+atomic4(i,j));
  atomicpercent2(i,j) =
atomic2(i,j)/(atomic1(i,j)+atomic2(i,j)+atomic3(i,j)+atomic4(i,j));
  atomicpercent3(i,j) =
atomic3(i,j)/(atomic1(i,j)+atomic2(i,j)+atomic3(i,j)+atomic4(i,j));
  atomicpercent4(i,j) =
atomic4(i,j)/(atomic1(i,j)+atomic2(i,j)+atomic3(i,j)+atomic4(i,j));
  end
  end

atomic1plot = reshape(atomic1',[],1);
atomic2plot = reshape(atomic2',[],1);
atomic3plot = reshape(atomic3',[],1);
atomic4plot = reshape(atomic4',[],1);

thickness1 = time*factor1*sputterrate1;
thickness2 = sputterrate2*time*factor2;
thickness3 = time*factor3*sputterrate3;
```

```
thickness4 = sputterrate4*time*factor4;

thickness1plot = reshape(thickness1',[],1);
thickness2plot = reshape(thickness2',[],1);
thickness3plot = reshape(thickness3',[],1);
thickness4plot = reshape(thickness4',[],1);


totalthickness = thickness1+thickness2+thickness3+thickness4;
%%creates set of points along gun to gun lines for 2 element gradient
%%estimation
   for a=1:1:5/radiusincrement %two for loops that will sweep through wafer points
   for b=1:1:thetatotal
   r2(a,b) = (a-1)*radiusincrement;
   theta2(a,b) = (b-1)*thetaincrement;
   x2(a,b) = r2(a,b).*cos(theta2(a,b).*pi/180);
   y2(a,b) = r2(a,b).*sin(theta2(a,b).*pi/180);
   point = [x2(a,b) y2(a,b) 0];
   if abs(point(1)-point(2))<=(1e-10)
   gradient1to3(k,1)=x(a,b);
   gradient1to3(k,2)=y(a,b);
   gradient1to3(k,3)=atomicpercent1(a,b);
   gradient1to3(k,4)=atomicpercent2(a,b);
   gradient1to3(k,5)=atomicpercent3(a,b);
   gradient1to3(k,6)=atomicpercent4(a,b);
   gradient1to3(k,7)=totalthickness(a,b);
   k=k+1;
   end
   if abs(point(1)+point(2))<=(1e-10)
   gradient2to4(l,1)=x(a,b);
   gradient2to4(l,2)=y(a,b);
   gradient2to4(l,3)=atomicpercent1(a,b);
   gradient2to4(l,4)=atomicpercent2(a,b);
   gradient2to4(l,5)=atomicpercent3(a,b);
   gradient2to4(l,6)=atomicpercent4(a,b);
   gradient2to4(l,7)=totalthickness(a,b);
   l=l+1;
   end


   end
   end
%%reshsape results for easy plotting in external program
```

```
xplot = reshape(x',[],1);
yplot = reshape(y',[],1);
factor1plot = reshape(factor1',[],1);
factor2plot = reshape(factor2',[],1);
factor3plot = reshape(factor3',[],1);
factor4plot = reshape(factor4',[],1);
percent1plot = reshape(atomicpercent1',[],1);
percent2plot = reshape(atomicpercent2',[],1);
percent3plot = reshape(atomicpercent3',[],1);
percent4plot = reshape(atomicpercent4',[],1);
comp1plot = reshape(comp1',[],1);
comp2plot = reshape(comp2',[],1);
comp3plot = reshape(comp3',[],1);
comp4plot = reshape(comp4',[],1);
thickness1plot = reshape(thickness1',[],1);
thickness2plot = reshape(thickness2',[],1);
thickness3plot = reshape(thickness3',[],1);
thickness4plot = reshape(thickness4',[],1);
totalthicknessplot = reshape(totalthickness',[],1);


%%creates final table of results for easy access and plotting
percenttable =[xplot yplot percent1plot percent2plot percent3plot percent4plot
thickness1plot, thickness2plot,thickness3plot,thickness4plot, totalthicknessplot];
colNames =
{'x','y','gun1atomic%','gun2atomic%','gun3atomic%','gun4atomic%','thickness1','thicknes
s2','thickness3','thickness4','totalthickness'};
totalthicknesstable = unique([xplot yplot totalthicknessplot],'rows');
resultstable = array2table(percenttable, 'VariableNames',colNames);
resultsfinal = unique(resultstable,'rows');
```

VITA

Walker Lee Boldman was born on June 26th of 1994. He attended College of the Ozarks, where he graduated in 2016 with a B.S. in Mathematics and a B.A. in Music. He then attended the University of Tennessee Knoxville, where he received his Master's in Material Science Engineering in 2018 and his Ph.D. in Materials Science Engineering in 2020. He currently lives in Knoxville, Tennessee with his wife and daughter.