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Enhanced performance of 19 single gate MOSFET with high permittivity dielectric material

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ABSTRACT

In this research, the performance of the 19 nm single gate MOSFET is enhanced through the implementation of the high permittivity dielectric material. The MOSFET scaling trends necessities in device dimensions can be satisfied through the implementation of the high-K dielectric materials in place of the SiO2. Therefore, the 19 nm n-channel MOSFET device with different High-K dielectric materials are implemented and its performance improvement has also been analysed. Virtual fabrication is exercised through ATHENA module from Silvaco TCAD tool. Meanwhile, the device characteristic was utilized by using an ATLAS module. The aforementioned materials have also been simulated and compared with the conventional gate oxide SiO2 for the same structure. At the end, the results have proved that Titanium oxide (TiO2) device is the best dielectric material with a combination of metal gate Tungsten Silicides (WSix). The drive current (ION) of this device (WSix/TiO2) is 587.6 µA/um at 0.534 V of threshold voltage (VTH) as opposed to the targeted 0.530 V predicted, as well as a relatively low IOFF that is obtained at 1.92 pA/µm. This ION value meets the minimum requirement predicted by International Technology Roadmap for Semiconductor (ITRS) 2013 prediction for low performance (LP) technology.

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1. INTRODUCTION

With new technologies, numerous industries rely heavily on a manufacturing of smaller, faster, cheaper and decent quality of the MOSFET and such increment in global competition have caused the modern industries to have to acclimate and improve their manufacturing process to be more effectual and competitive by developing a further compact sized products and therefore forcing the advanced technologies to scale down the MOSFET into nanoscale. Theoretically, the device performance has been improved as both incremental is analysed in the gate capacitance (Cg) and thereby drive current, as thickness of the silicon dioxide (SiO2) gate dielectric is gradually reduced. However, scaling the SiO2 further below the 2 nm gate layer thickness may upshot in a hefty increase of the leakage current (IOFF) and short channel effect due to incremental in tunnelling that increases power consumption whilst reducing the reliability of the device. In order to overcome this problem, scholars are concentrating on the metal gate with high-K materials that is capable to be incorporated in MOSFET flow [1]. Despite that, there are several high-K materials that holds dielectric constant that is either too low or high for which may not be an appropriate of choice for alternative gate dielectric [2]. Therefore, substituting the SiO2 with high-K materials permits an amplification of gate capacitance. This is due to that the high-K dielectric materials are widely accepted as a better approach for

the gate dielectric of the MOSFET. That said, previous works from various sources have purposed the combination of high-K and metal gate on MOSFET devices [3-10]. A higher dielectric constant material is introduced to replace SiO2 which allows thicker dielectric to be deposited to reduce leakage without electrical thickness penalties [11-12]. Commonly, a substantial sum of studies has been issued on the prediction of leakage current and leakage power by numerous researchers, along with the study on the performance of high-K materials [13-18]. High dielectric constant, large band gap with favorable band alignment, low interface state density and good thermal stability are amongst the best characteristics to have for the gate dielectric. Among the high-K materials that could have either too low or high dielectric constant may not be appropriate for the use on alternative gate dielectric.

In this project, the fundamental understanding of the physical and the electrical characteristics of the 19 nm gate length NMOS device containing high dielectric constant will be investigated. Simulation based fabrications have also been implemented in previous studies [18-20]. For this project, the performance of high-K dielectric Titanium Oxide (TiO2) will be compared with SiO2 as gate dielectric via simulation with Silvaco TCAD tool. Besides, design nanoscale of NMOS transistor device using ATLAS module in generating the current-voltage (I-V) Characteristic, structure and the value of threshold voltage. The simulation study of nanoscale n-channel MOSFET device using various high-K materials such as Hafnium Oxide (HfO2), Aluminum trioxide (Al2O3), Titanium Oxide (TiO2) and Lanthanum oxide (La2O3) is studied. Besides, the effect of high-K dielectrics on the electrical characteristics such as threshold voltage (VTH), drive current (ION) and leakage current (IOFF) has been critically reviewed. After investigation of various high-K dielectrics, it has been observed that WSix/TiO2 device has an excellent capability of enhancing the device performance with the suppression of short channel effects (SCEs).

2. MATERIALS AND METHOD

2.1. Virtual Fabrication Process

The virtual fabrication of the 19 nm NMOS device is materialized using Silvaco TCAD tool through the ATHENA simulator for process simulation before ATLAS is used for device simulation in obtaining the ID-VGS and ID-VDS for the device [18]. An orientation of <100> and p-type (boron doped) silicon wafers are used in this study where by silicon (Si) is added as a primary substrate before a layer of Silicon Oxide (SiO2) being deposited. 7x1014atom/cm3 of boron is then injected. P-well oxidation is then obtained through developing 200 Å oxide at 970oC that is exercised as mask for p-well implantation process. 3.75x1012 atom/cm3 of boron dose is implanted before trenching process and the oxide is grown in dry oxygen at 812oC. The field oxide is also used in defining source and drain in subsequent diffusion. That being said, gate oxide produces better oxide as well as thinner compared to the field oxide. Subsequently, beryllium difluoride (BF2) is applied in the channel region to amend the threshold voltage. Low dosage is performed on the VTH due to that a slight modification made on the gate concentration is proven to be sufficient for the VTH adjustment to achieve within the targeted value predicted by the ITRS 2013 [21].

High-K dielectric materials are then deposited using HfO2 and TiO2 with gate oxide thickness is size-adjusted as this is so that it achieves the equivalent oxide thickness (EOT) with SiO2 through the device electrical characteristics analysis. The length adjustment is also scaled at 19 nm that is equivalent to the transistor's gate legth before boron is implanted on the n-well active area for the alteration process to the VTH. Afterwords, the Titanium Silicide (TiSix) and Tungsten Silicides (WSix) are set down on the top of each high-K materials (HfO2 and TiO2). Figure 1 shows the 19 nm structure after high-K dielectric material is deposited. The optimum performance for the 19 nm NMOS device can be obtain following 2.18x1013 atom/cm3 of indium is doped in the halo implantation process that implanted a p-type impurity ion prior to the formation of lightly doped n-channel source/drain areas. Effectively, the short channel effect is reduced through a formation of halo structure [22-23]. Afterwards the layer Si3N4 is formed on the surface of silicon and polysilicon after the nitride deposition for which is called sidewall spacer that is then used as mask in source/drain implantation.

Meanwhile, the source/drain implantation is exercised by implanting 9.67x1013 atom/cm3 of arsenic to build a profoundly n-type doped region in the p-type substrate in order to warrant the current flow is smoothening in the 19 nm device. The deposition of boron phosphor silicate glass (BPSG) is then added to work as a pre-metal dielectric (PMD) for which is the first layer consigned on the surface of the wafer. BPSG for which is a silicate glass type includes the additives of 1x1016 atom/cm3 of boron, 1x1016 atom/cm3 of phosphor and 1x1016 atom/cm3 of arsenic after oxide is deposited at 100 nm of thickness. The likes of silicate glass for instance PSG and boron phosilicate glass are common in semiconductor device fabrication [24]. Next, the source/drain contact patterning is then managed to enable current flow between source and drain before compensate implantation is carried out as to minimize side capacitance.

The 19 nm NMOS structure was connected with aluminium metal followed by deposited the second aluminium layer on the uppermost of the intel-metal dielectric (IMD) whereby the metallization is the electrically interconnected metal layers between the diversed device structures fabricated on the substrate. Further to that, the contact is developed as unwanted aluminium is etched. That being said, Aluminium etching is extremely exothermic thus the under-etched resist mask causes local heating, if no agitation is performed. In addition to that, the extra xide on the wafer is discarded by applying chemical mechanical polishing (CMP). Once the 19 nm NMOS device is constructed with ATHENA simulator, the simulator is then purposed to stimulate the ID-VGS and ID-VDS for the MOSFET device. Figure 1 shows one of the 19 nm NMOS structure device with high–K dielectric and metal gate as well as the results obtained as in Table 1.

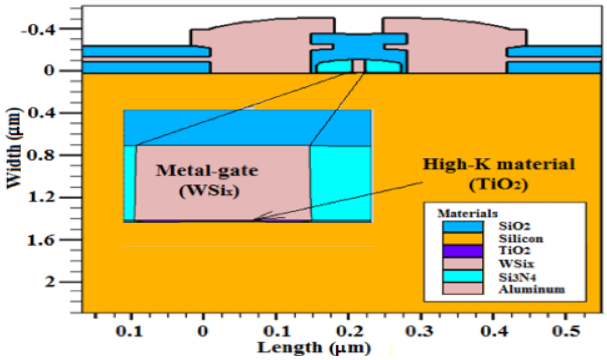

Figure 1. Effects of selecting different switching under dynamic condition

Table 1. Output Responses of the Device Characteristics for 19 Nm NMOS Device Using Sio2 and Polysilicon

Parameters	SiO_2/Poly	ITRS 2013 prediction [21]
Threshold voltage (V), V_{TH}	0.536	0.530
Drive current (µA/µm), I_{ON}	169	>422
Leakage current (pA/µm), I_{OFF}	4.5	<20
I_{ON}/I_{OFF} ($\times 10^6$)	37.55	21.10
Subthreshold voltage (mV/dec), SS	121	70~100

2.2. Election of High-K Material and Metal Gate

Numerous high-K materials have been examined at the present time such as hafnium dioxide (HfO2) and titanium dioxide (TiO2). However the band alignment for TiO2 is at 0.4eV is not favorable despite its high dieletric constant propery of k~85. On the other hand hafnium oxide has the average dielectric constant property of k~25 with high band gap at 4.3eV. That being said, the performance for the all high-K material with titanium silicides and tungsten silicides are studied.

Replacing polysilicon gate materials with metal is observed to have eliminate compatibility issues between the high-K dielectric and poly electrode [18]. When the titanium dioxide and titanium silicide (TiSix) is applied as the respective high-K dielectric and metal gate, the value of the VTH obtained is at 0.530 V which precisely and is within the range ±12.7% from the ITRS 2013 values predicted for the year 2017 that is 0.530 V [21].

In contra to the results obtained using the TiO2 and TiSix, the VTH value is achieved at 0.535 V when hafnium dioxide (HfO2) is used as high-K along with TiSix remained as the metal gate. Changes are also made on the metal gate whereby the tungsten silicide (WSix) is used in place of the TiSix. When the TiO2 is used in the structure as high-K dielectric material along with WSix as the metal gate, the value of the VTH is at 0.534 V. Meanwhile as it the high-K material is replaced with HfO2, the VTH value is then acquired at 0.534 V as well. That being said, both TiO2 and HfO2 when using the WSix are still in the ITRS 2013 prediction for the year 2017 when VTH is predicted at 0.530±12.7% V [21].

3. RESULTS AND ANALYSIS

Voltage threshold (VTH), Drain current (ION), leakage current (IOFF), ION/IOFF ratio and Subthreshold Voltage (SS) are the parameters chosen in determining the performance of the high-K dielectric

materials and metal gates combination in the NMOS device designed. The ION values resulted from the simulation shows larger values obtained (587.6µA/µm) as opposed to estimated values (456µA/µm) for a device that has WSix as metal gate whereas the simulation results for IOFF are lower (1.92pA/µm) than forecasted value (20pA/µm) is also from the device that has WSix as metal gate. The decent performance of design MOSFET is when IOFF equal to zero ampere and higher of ION value [2].

Hence, it is concluded that both high-K materials are attuned with metal gate and compatible with device transistor. Based on the ID-VGS overlay of each devices with different high-K dielectric aterials and metal gates in Figure 2, the results of the device characteristics for the Poly-Si/SiO2 device, the WSix/HfO2 device, WSix/TiO2 device, TiSix/HfO2 device and TiSix/TiO2 device are shown in Table 2.

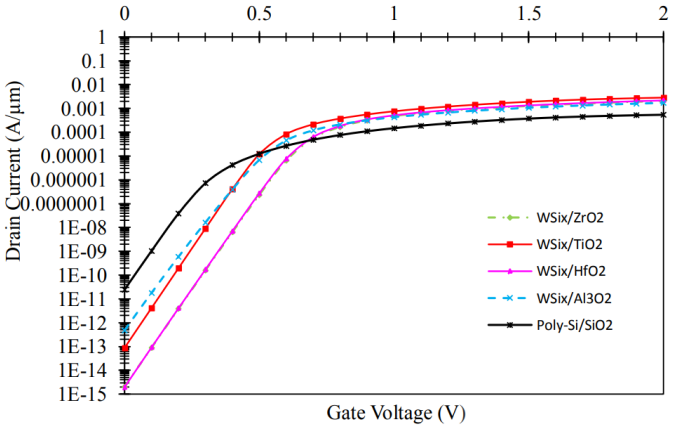

Figure 2. The ID–VGS overlay each device with different materials of high-K and metal gate

Table 2. Results of Electrical Characteristic for Device

Parameters	Device					ITRS 2013 prediction for 2017 [24]
	SiO_2/Poly	High-K/metal gate				
		HfO_2/WSi_x	TiO_2/WSi_x	$HfO_2/TiSi_x$	$TiO_2/TiSi_x$	
V_{TH} (V)	0.536	0.534	0.534	0.535	0.530	0.530
I_{ON} (µA/µm)	169	578.8	587.6	383.0	388.4	> 422
I_{OFF} (pA/µm)	4.5	5.1	1.9	66.9	92.4	< 20
I_{ON}/I_{OFF} (x 10^6)	37.6	113.2	306.0	5.72	4.2	21.10

It is observed that the WSix/TiO2 device has produced the highest value of the ratio of ION/IOFF, which is 306.06x106. In fact, all the device characteristics of WSix/TiO2 based device were observed to be better than the others. The device is apposite for low power application because it shows the higher ION and IOFF ratio in the subthreshold region of operation [25]. It is discovered as the best choice material as the gate dielectric for metal gate TiSix is HfO2 as this is due to the fact that it provides the best result through high dielectric constant, high band-gap and band offsets with silicon, aside from decent scalability and low leakage current. Besides, the sufficient barrier height is also obtainable due to the heat of formation and bandgap for HfO2 is 271 Kcal/mol and 5.68eV respectively and is high enough. HfO2 is thermodynamically stable with silicon substrate, high dielectric constant (~25), impurity diffusion resistance due to its high density (9.68g/cm3), along with similar lattice parameter to that of Si with a small lattice misfit (<5%) [2].

Meanwhile, TiO2 is the best dielectric material for metal gate WSix. The TiO2/WSix device gives the better result since the silicides has less resistance, decent process compatibility with Si, has little or no electromigration, easy to dry etch and decent contacts to other materials [26]. Based on results from Table 2, it is analyzaed that the TiO2/WSix device has the highest drain current which is at 587.6 µA/µm as opposed to HfO2/WSix which is at 578.8 µA/µm as shown in Figure 3. Hence from these figures, it is observed that the ION is proportional to the permittivity of high-K dielectric materials. Based on the comaprisons between TiO2/TiSix and HfO2/TiSix, as well as between TiO2/WSix and HfO2/WSix, improvement is observed for ION value when TiO2 is used as a gate dielectric. The ION value is observed to be increased when a higher permittivity of high-K dielectrics is applied as the gate insulator due to the decrement in depletion as there is less boron penetration when a higher permittivity of high-K dielectric is applied [25].

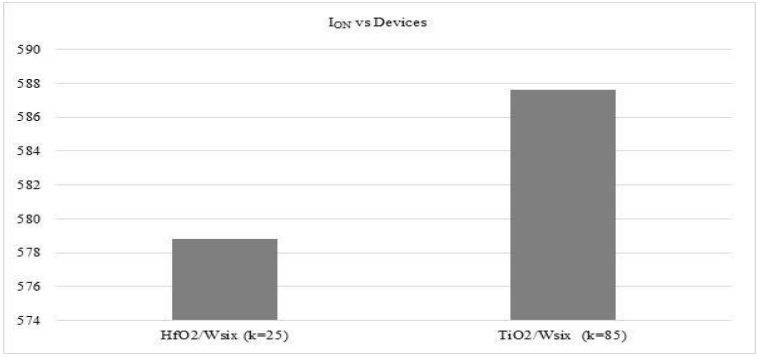

Figure 3. ION for HfO2 and TiO2 dielectrics with metal gate WSix

4. CONCLUSION

The fabrication of MOSFET challenges in nanometer regime can be overcome through the application of high-K dielectric material with metal gate in place of SiO2 and polysilicon. The application of TiO2 and HfO2 along with TiSix and WSix has proven to have significantly improve the structure's electrical characteristics due to the properties of high-K dielectric materials that holds higher permittivity for which improves the ION due to a reduction in depletion from low boron penetration occurred. Hence, TiO2/WSix combination has proved to provide the best performance to the device due to its lowest leakage current at 1.92 pA/µm and also its highest drain produced at 587.6 µA/µm. Comparatively, the TiO2/WSix has improved the results by 87.712% based on the ION/IOFF ratio produced in comparison to the initial structure that is using the SiO2/Polysilicon. However, further improvement can be made whereby the results can be improvised through statistical method implementation. Based on the results obtained, the electrical characteristics of this device meet the requirement of low performance technology predicted by International Technology Roadmap Semiconductor 2013 for the year 2017.

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