MODELING OF THE OUTPUT AND TRANSFER CHARACTERISTICS OF GRAPHENE FIELD-EFFECT TRANSISTORS

BY

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THESIS

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ABSTRACT

This thesis presents a model that provides the output and transfer characteristics of graphene field-effect transistors by using the charge-control model for the current, based on the solution of the Boltzmann equation in the field-dependent relaxation time approximation. Closed expressions for the conductance, transconductance, and saturation voltage are derived. The results are in good agreement with the experimental data of Meric et al. [*Nature Nanotechnology*, vol. 3, p. 684, 2008] without assuming carrier density-dependent velocity saturation.

ACKNOWLEDGMENTS

Thank you to my wife and family for the unconditional support and encouragement. Thanks to my classmate and cubicle partner, Anuj Girdhar, for helpful discussions and welcome distractions. Thank you to the University of Illinois Graduate College for awarding me a teaching assistantship to ease my financial burden. Most of all, thank you to my professor and adviser, Dr. Jean-Pierre Leburton, for providing me with the required knowledge to complete this project and for the many hours spent deriving equations on white boards.

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LIST OF SYMBOLS

C_{back}	back gate capacitance
C_{top}	top gate capacitance
E	elementary charge
$f(k)$	carrier distribution function
F	electric field
F_c	critical electric field
g_{ds}	small signal drain-source conductance
g_m^{sat}	small signal transconductance at saturation
$\hbar$	Planck’s constant
I_d	drain current
$\vec{k}$	momentum vector
k_B	Boltzmann’s constant
k_F	Fermi momentum vector
L	top gate length
μ_0	mobility
p	hole concentration
p_0	equilibrium hole concentration
R_{ds}	drain-source resistance
R_s	source resistance (located on both sides of top gate)
$\tau(p)$	relaxation time
T_e	electronic temperature
V_0	device threshold voltage

V_c	critical voltage
v_F	Fermi velocity
V_{g0}	voltage difference between top gate voltage and threshold voltage
V_{gback}	back gate voltage
V_{gback}^0	back gate voltage at the Dirac point
V_{gtop}	top gate voltage
V_{gtop}^0	top gate voltage at the Dirac point
v_{sat}	saturation velocity
W	device width

CHAPTER 1

INTRODUCTION

1.1 GRAPHENE

In recent years, graphene has emerged as a novel monolayer material with exotic physical properties [1], [2] for applications in high performance electronic devices [3], [4]. Its potential was most notably recognized when the 2010 Nobel Prize in Physics was awarded to Novoselov and Geim for their experiments with the material. Graphene consists of a single atomic layer of sp^2-bonded carbon atoms arranged in a 2-D honeycomb lattice as shown in Figure 1. This results in a linear relation between the charge carrier energy E and the 2-D wave vector k given by $E = \hbar v_F k$, where $v_F \sim 10^8$ cm/s is the Fermi velocity and $\hbar$ is the reduced Planck constant. Additionally, the bandgap is reduced to a single point (Dirac point) as shown in Figure 2. In this framework all carriers behave like massless fermions and have a velocity with the same absolute value that is one order of magnitude larger than in conventional III-V materials [7], making graphene a promising candidate for high-speed nanoelectronics.

1.2 GRAPHENE FIELD-EFFECT TRANSISTORS

Recently, graphene field-effect transistors (GFETs) were successfully fabricated and exhibited *I-V* characteristics similar to conventional silicon MOS transistors [3]. Low-field mobilities were, however, strongly degraded by the presence of coulombic space charge in the neighboring oxides, whereas nonlinearities in the *I-V* characteristics were interpreted as caused by carrier velocity saturation for which the value would depend on the carrier concentration induced by gate voltages in the 2-D graphene monolayer.

The goal of this thesis is to provide a charge-control model for GFETs that does not require the assumption of carrier density-dependent saturation velocity to reproduce the experimental characteristics. This model also provides closed form analytic expressions for the saturation voltage, conductance, and transconductance of the device.

1.3 FIGURES

Figure 1. Schematic of a graphene layer [5].

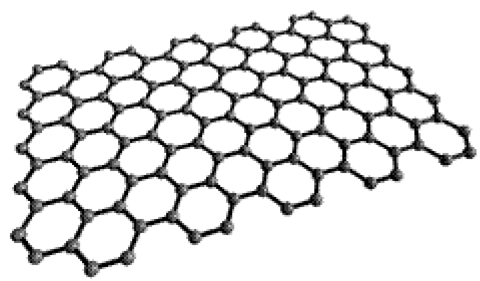
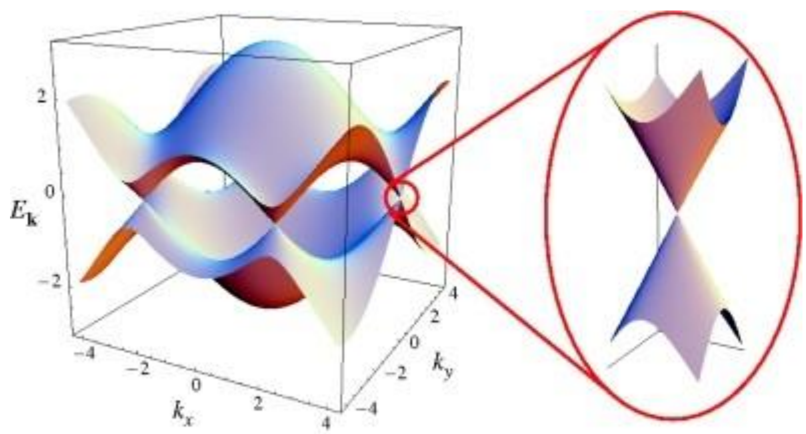


Figure 2. E-k diagram for graphene with an enlarged portion showing the zero bandgap and linear relation near the Dirac point [6].



CHAPTER 2

EXPERIMENTAL SETUP

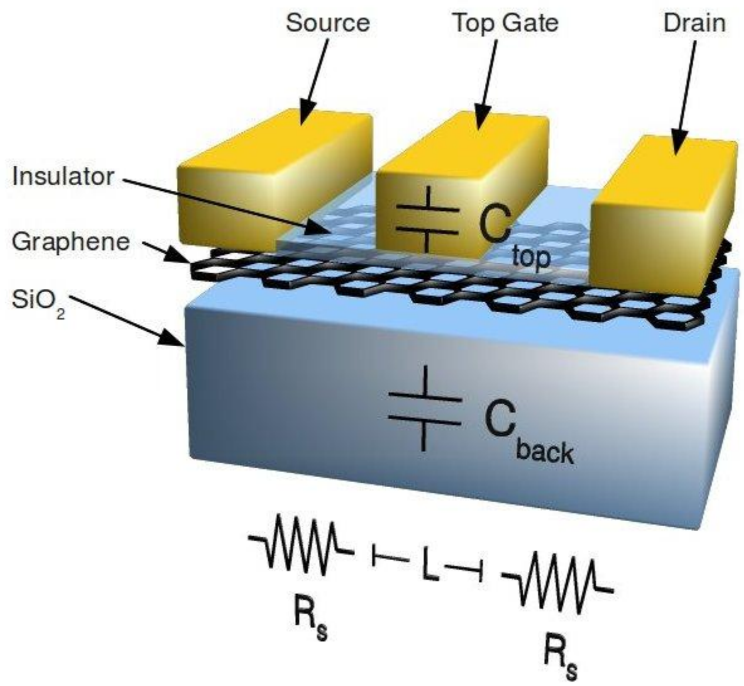
2.1 DEVICE DESCRIPTION

Figure 3 shows a schematic of the GFET, where the graphene monolayer sits on a thick SiO_2 layer with capacitance C_{back} on top of a back gate. By varying the back gate voltage V_{gback}, one can control the source and drain resistance R_s at the same time as the channel threshold voltage. A top gate of length L, separated from the graphene monolayer by a thinner oxide with capacitance C_{top}, controls the carriers in the channel with V_{gtop}. For the sake of comparison with the experiment, we will only consider p-channel device operation, but our model is valid for n-channel operation as well.

All experimental data was obtained using a device with a width of 2.1 µm, a source-drain separation of 3 µm, and a top gate length of 1 µm. Additionally, the top and back gate capacitances were measured to be approximately 552 nF/cm^2 and 12 nF/cm^2, respectively. Results are provided for two constant back gate voltages using either V_{gback} = −40 V (p-type source/drain) or V_{gback} = +40 V (n-type source/drain).

2.2 FIGURES

Figure 3. Schematic of a GFET.



CHAPTER 3

MODEL

3.1 MATHEMATICAL DERIVATIONS

In order to model the transport characteristics of the GFET, the carrier distribution function is split into its even and odd parts so $f\left(\vec{k}\right) = f_{even}\left(\vec{k}\right) + f_{odd}\left(\vec{k}\right)$. Then, it is well known that in the presence of randomizing collisions, and even in high fields, the Boltzmann transport equation can be written as [8]

$$\frac{eF}{\hbar}\frac{\partial}{\partial k_x} f_{even}\left(\vec{k}\right) = -\frac{1}{\tau_{tot}\left(k\right)} f_{odd}\left(\vec{k}\right) \tag{1}$$

with $\frac{1}{\tau_{tot}\left(k\right)} = \sum_i \frac{1}{\tau_i\left(k\right)}$ and the i-index indicates a particular scattering mechanism. *F* is the electric field. In the presence of strong inter-carrier scattering for high carrier concentration, the even part of the distribution is thermalized at an electronic temperature T_e, and reads

$$f_{even}\left(\vec{k}\right) = \frac{1}{1 + \exp\left[\frac{\hbar v_F\left(k - k_F\right)}{k_B T_e}\right]} \tag{2}$$

where $k_F = k_F\left(x\right)$ defines the carrier concentration along the channel. In p-channel, the current can be calculated as

$$\vec{I} = \frac{4e}{L}\sum_{\vec{k}} \vec{v}\left(\vec{k}\right) f_{odd}\left(\vec{k}\right) \tag{3}$$

where L is the channel length, and the factor 4 accounts for the spin and the twofold degeneracy of the Dirac point [1]. Here, $v(\vec{k}) = v_F(\cos\theta, \sin\theta)$ and θ is the angle between the electric field and the vector $\vec{k}$. Then for $\hbar v_F k_F \gg k_B T_e$ one can approximate $\frac{\partial}{\partial k_x} f_{even}\left(\vec{k}\right)$ by a delta function centered around k_F as shown in Figure 4. After integration, and given $k_F = \sqrt{\pi p}$ [9] [1], the hole current in a 2-D graphene layer reads

$$I = W\frac{2e^2}{h} F v_F \tau\left(p\right)\sqrt{\pi p} \tag{4}$$

where W is the graphene layer width, p is the hole concentration, and $\tau(p)$ is the relaxation time (inverse scattering rate) for a particular carrier concentration p. In the high field regime, we assume $\tau\left(p\right) = \tau_{lf}\big/\left(1 + F/F_c\right)$ where F_c is the critical field for the onset of high energy collisions such as remote phonons [10], $\tau_{lf}\left(p\right) = \tau_0\sqrt{p/N_i}$ is the low field relaxation time dominated by scattering with charged impurities with density N_i [9], and τ_0 is a time constant. By setting $\mu_0 = \left(e/\hbar\right) v_F \tau_0 \sqrt{p/N_i}$, one recovers the conventional current expression

$$I = Wepv(F) \tag{5}$$

with $v(F) = \mu_0 F\big/\left(1 + F/F_c\right)$, where the low field conductance $\sigma_{lf} \propto p$, as observed experimentally [1], [9].

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[1] Here, it is assumed carrier energies are low enough so that the linear energy dispersion holds, since the maximum voltage drop along the channel is < 3 V, accounting for the source and drain regions, well within the linearity region.

In the charge-control model, close to the Dirac point, one can use the mass action law [11] to get

$$p(x) = \frac{Q(x)}{2e} + \sqrt{\left(\frac{Q(x)}{2e}\right)^2 + p_0^2} \tag{6}$$

where p_0 is the minimum sheet carrier concentration [9] and $Q(x)$ is the electric charge density along the channel from source to drain given by $Q(x) = -C_{top}\left[V_{g0} - V(x)\right]$ in the gradual channel approximation [12]. Here, $V_{g0} = V_{gtop} - V_0$ where V_0 is the threshold voltage of the GFET and is defined as [3]

$$V_0 = V_{gtop}^0 + \frac{C_{back}}{C_{top}}\left(V_{gback}^0 - V_{gback}\right) \tag{7}$$

where V_{gtop}^0 and V_{gback}^0 designate the top and back gate voltages at the Dirac point, respectively. However, for $\frac{Q(x)}{2e} \gg p_0$, which is the case for all bias conditions considered in this analysis, one can write

$$p(x) = \frac{Q(x)}{e}. \tag{8}$$

By integrating the current equation (5) from source to drain as in conventional MOS devices [12], and by taking into account the series resistance R_s at the source and drain [3], one gets

$$I_d = \frac{W\mu_0 V_c}{2LC_{top}\left(\left|V_{ds}\right| - 2\left|I_d\right|R_s + V_c\right)}\left[Q(L)^2 - Q(0)^2\right] \tag{9}$$

where $Q(L) = -C_{top}\left(V_{g0} - V_{ds} - |I_d| R_s\right)$ and $Q(0) = -C_{top}(V_{g0} + |I_d| R_s)$. Solving for I_d, one obtains a closed expression for the drain current

$$I_d = \frac{1}{4R_s}\left[V_{ds} - V_c + I_0 R_s + \sqrt{(V_{ds} - V_c + I_0 R_s)^2 - 4 I_0 R_s V_{ds}}\right] \tag{10}$$

where V_{ds} is the drain-source voltage, $I_0 = 2(W/L)\mu_0 V_c C_{top}\left(V_{gtop} - V_0 - V_{ds}/2\right)$, and $V_c = F_c L$.

From here, the low drain-source bias conductance is readily calculated by taking the derivative of the current expression (10) with respect to V_{ds} as V_{ds} goes to zero. One gets

$$g_{ds}(V_{ds} \to 0) = \frac{-V_{g0}}{\left|2R_s V_{g0} - R_c V_c\right|} \tag{11}$$

where $1/R_c = (W/L)\mu_0 C_{top} V_c$, so that $R_c V_c$ is independent of V_c, as is the conductance at low drain bias. The low drain-source bias resistance reads

$$R_{ds} = \frac{1}{g_{ds}} = 2R_s - \frac{R_c V_c}{V_{g0}} \tag{12}$$

which establishes a linear relation between $1/g_{ds}$ and $1/V_{g0}$ with a slope given by $R_c V_c$ (inversely proportional to the mobility) and an asymptotic conductance value for large V_{g0} reaching $2R_s$.

In the same context, one obtains the expression for the drain-source saturation voltage as a function of the top gate voltage V_{g0} by solving for V_{ds} after setting the derivative of the current (10) with respect to V_{ds} equal to zero that yields

$$V_{ds(sat)}=\frac{2\gamma V_{g0}}{1+\gamma}+\frac{1-\gamma}{(1+\gamma)^2}\left[V_c-\sqrt{V_c^2-2(1+\gamma)V_cV_{g0}}\right] \tag{13}$$

with $\gamma=R_s/R_c$. Substituting the drain-source saturation voltage (13) into the current equation (10) leads to the expression of the saturation drain current as a function of the top gate voltage that reads

$$I_{d(sat)}=\frac{\gamma}{R_s(1+\gamma)^2}\left[-V_c+(1+\gamma)V_{g0}+\sqrt{V_c^2-2(1+\gamma)V_cV_{g0}}\right]. \tag{14}$$

By taking the derivative of the saturation current with respect to the top gate voltage, one derives the expression for the transconductance at saturation,

$$g_m^{sat}=\frac{1}{R_s+R_c}\left[1-\frac{1}{\sqrt{1-2(1+\gamma)V_{g0}/V_c}}\right]. \tag{15}$$

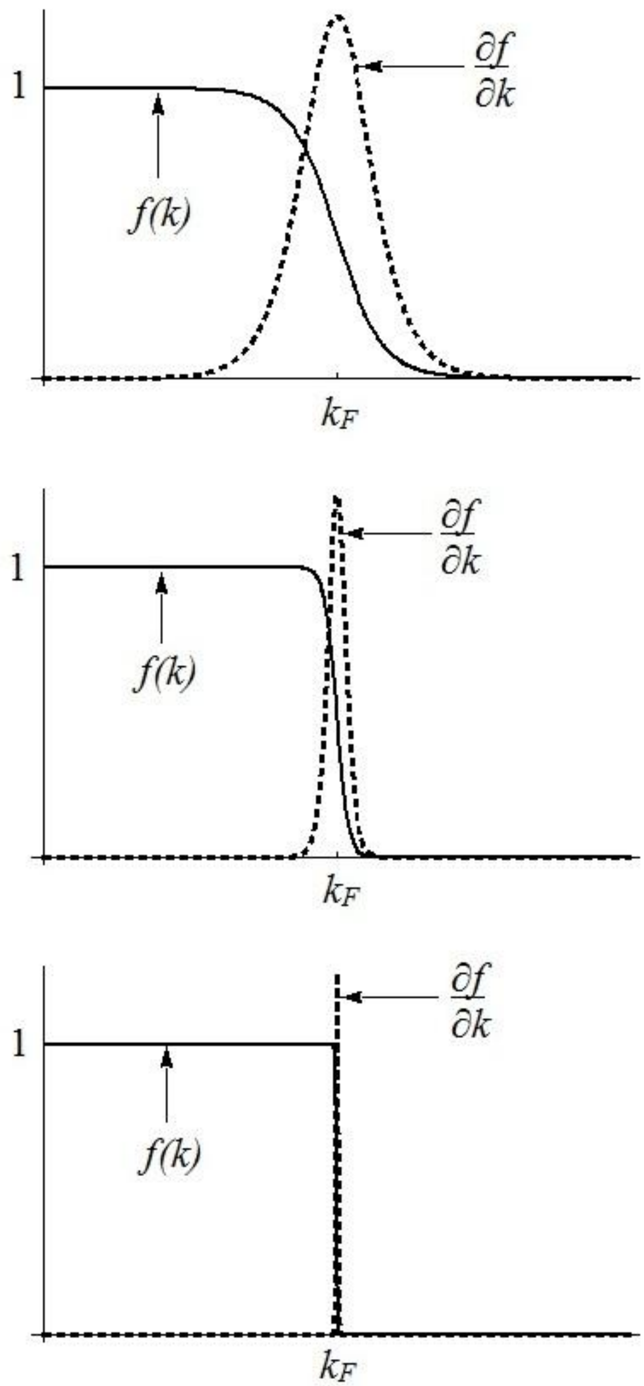
Additionally, the expression for the electric potential as a function of position along the channel length can be derived from the current equation (10) and is given by

$$V(x)=V_{g0}-V_i+\sqrt{(V_{g0}-V_i-I_dR_s)^2+\frac{2I_dx}{W\mu_0C_{top}}} \tag{16}$$

where $V_i=I_d/(W\mu_0F_cC_{top})$ and the source is located at *x* = 0.

3.2 FIGURES

Figure 4. Graphical demonstration of how $\frac{\partial}{\partial k} f_{even}\left(\vec{k}\right)$ approaches a delta function for $\hbar v_F k_F \gg k_B T_e$.



CHAPTER 4

RESULTS

This section will present the results for the case of V_{gback} = −40 V (V_0 = 2.36 V) and of V_{gback} = +40 V (V_0 = 0.64 V). In the former, the source and drain regions of the GFET are p-type, while in the latter, they are n-type; notice that both threshold voltages are positive, and in both cases the top gate is biased negatively to form a p-channel.

4.1 V_{gback} = −40 V

Figure 5 shows the plots of both the low-bias conductance g_{ds} as a function of the top gate voltage, and the low-bias resistance R_{ds} as a function of the inverse of the top gate voltage in the device configuration investigated in [3]. In Figure 5(a), the solid curve is calculated from (11) with the mobility μ_0 = 550 $cm^2/(V{\cdot}s)$ and source resistance R_s = 700 Ω as explicitly given in [3], which gives good agreement with the experimental data close to the minimum conductance, but underestimates the former by about 20% at high top gate bias. The dashed curve is the best fit of (11) with the experimental conductance with μ_0 = 600 $cm^2/(V{\cdot}s)$ and R_s = 500 Ω, which indicates that the discrepancy with the previous data is essentially due to a different value of the source resistance. In Figure 5(b), one can see that the experimental resistance values display a linear relation with $1/V_{g0}$ in agreement with (12). While their mobilities have similar values (within 10%), both theoretical curves are shifted from one another by the different values of the source resistance R_s.

Figure 6(a) displays the *I-V* characteristics of the GFET for V_{gback} = −40 V. An excellent agreement between experiment and theory (10) is obtained with μ_0 = 700 $cm^2/(V{\cdot}s)$, R_s = 800 Ω, and V_c = 0.45 V for all gate biases, which provides the right current values for high (negative) V_{ds}. This mobility value is 25% higher than Meric's fitted values [μ_0 = 550 $cm^2/(V{\cdot}s)$], while the source resistance is within 15% of the measured ones [3]. The up-kick in the drain current attributed to ambipolar transport for V_{gtop} = 0 V is simulated by a phenomenological current term proportional to $\left(V_{ds}/V_{ds(sat)}-1\right)^2$ [13]. For comparison, the current is also plotted with the parameter values (μ_0 = 600 $cm^2/(V{\cdot}s)$ and R_s = 500 Ω) that best fit the conductance characteristics in Figure 5, and for which V_c = 0.5 V (F_c = 5 kV/cm) is used for all gate biases, which gives the right current values at V_{ds} = −3 V, but overestimates the current at high (negative) gate and intermediate source-drain biases. The discrepancy between the two sets of fitting parameters are within the 15 to 25% range, which is not really excessive and may be due to the fact that in the case of the conductance fit, the experimental data are obtained for very low bias, whereas in the case of the *I-V* fit, the mobility μ_0 and source resistance R_s values account for *intermediate* source-drain biases. These latter biases describe different transport processes (warm holes) with the onset of remote phonon scattering [10] at intermediate fields rather than low-bias transport limited only by impurity scattering [9].

Figure 6(b) shows the carrier concentration (left axis) and electric potential (right axis) at the saturation onset (V_{ds} = $V_{ds(sat)}$) as functions of position along the channel length with the source located at x = 0. One can observe that the channel never experiences pinch-off since the carrier concentration never reaches the minimum sheet carrier concentration given by p_0 = 0.5 x 10^{12} cm^{-2}. Therefore, it is believed the current up-kick at high source-drain bias for V_{gtop} = 0 V may be due to effects other than electron injection from the drain side, such as impact ionization with carrier multiplication for instance [13].

4.2 V_{gback} = +40 V

Figure 7 shows the comparison between theoretical and experimental results for both the p-channel conductance and resistances. In Figure 7(a), the solid curve is obtained from (11) with the parameters (μ_0 = 1200 cm^2/(V·s), R_s = 1200 Ω) given in [3], while the dashed curve uses μ_0 = 400 cm^2/(V·s) and R_s = 1000 Ω to fit the experimental data, which again display the linear relation predicted in (12) for the resistance as seen in Figure 7(b). Here, the discrepancy between the two sets of values for the fitting parameters is more dramatic since it affects both the slope (mobility) and to a less extent the asymptotic value of the source resistance.

Figure 8(a) shows the *I-V* characteristics of the GFET for V_{gback} = +40 V. Here the best fit is obtained with μ_0 = 1200 cm^2/(V·s), R_s = 1500 Ω, and V_c = 1.5 V (F_c = 15 kV/cm) for all gate biases, which are also close to Meric's values [3], but significantly different from the best conductance fit in Figure 6 that underestimates (overestimates) the current at low (high) (negative) gate bias. This high value for F_c compared to the GFET configuration with V_{gback} = −40 V is indicative of the higher saturation voltage for similar channel concentrations (indeed, the curves for V_{gtop} = −1.8 V and −2.8 V with V_{gback} = +40 V, on the one hand, and V_{gtop} = 0 V and −1.5 V with V_{gback} = −40 V, on the other hand, have similar charges at the source), while the higher source resistance provides lower current than for V_{gback} = −40 V, despite the higher mobility.

Figure 8(b) shows the carrier concentration and electric potential at the saturation onset ($V_{ds} = V_{ds(sat)}$) as functions of position along the channel length for the different gate biases. From a general standpoint, carrier concentrations are lower than for the case with V_{gback} = −40 V because of the lower threshold voltage (V_0 = 0.64 V instead of V_0 = 2.36 V). Again, it can be seen that the channel never experiences pinch-off since the carrier concentration never reaches the minimum sheet carrier concentration.

4.3 TRANSFER CHARACTERISTICS

In Figure 9, the drain-source saturation voltage is plotted as a function of gate bias (13) for the two GFET configurations. The vertical bars on the plot represent the approximate range of the saturation drain-source voltage obtained from the experimental plots [3]. One notices the excellent agreement between theory and experiment, especially for the V_{gback} = −40 V condition, whereas the discrepancy for the V_{gback} = +40 V configuration is due to the uncertainty in ascertaining the experimental values that fall out of the figure. One also notices the steeper variation of the saturation voltage in the latter case compared to the former case, which is reflected in the larger value of the critical fields to reproduce the experimental data.

In Figure 10, the saturation current is plotted as a function of the top gate voltage (14). For the case V_{gback} = −40 V, the extraction of the experimental values of the saturation current is straightforward, except for high top gate biases for which the current has not saturated (see Figure 6(a)), and shows an excellent agreement with this model. For the case V_{gback} = +40 V, the bars are estimates of experimental values because the current does not saturate for all values of V_{gtop} over the range of the source-drain voltage (see Figure 8(a)). For both V_{gback}, it can be seen that the relationship between the saturation current and top gate voltage is linear, and an excellent agreement between theory and experiment is obtained with discrepancies occurring at low top gate biases.

Also displayed is the profile of the transconductance at saturation as a function of top gate voltage (15) in Figure 11. One notices that for V_{gback} = +40 V, g_m^{sat} is much more drastically affected by the variation of the top gate voltage than for the V_{gback} = −40 V condition. This is due to the V_c term in (15) since the critical field, and consequently the critical voltage, is much larger when V_{gback} = +40 V.

4.4 FIGURES

Figure 5. (a) Small-signal source-drain conductance g_{ds} as a function of the top gate voltage minus the threshold voltage V_{g0}. (b) Small-signal source-drain resistance R_{ds} as a function of the inverse of the top gate voltage minus the threshold voltage $1/V_{g0}$ for V_{gback} = −40 V.

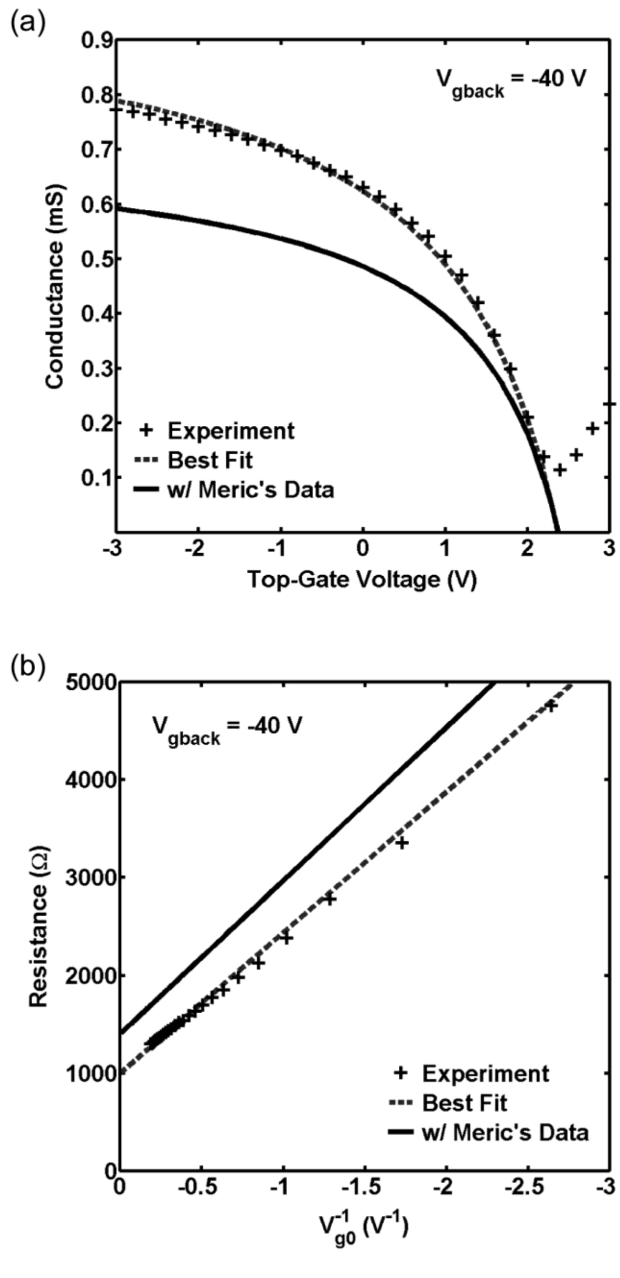


Figure 6. (a) Drain current I_d as a function of drain-source voltage V_{ds} and (b) hole concentration (left axis) and electric potential (right axis) for $V_{ds} = V_{ds(sat)}$ as functions of position along the channel length (source is on the left) for $V_{gback} = -40$ V; $V_{gtop} = 0$ V, -1.5 V, -1.9 V and -3 V (from bottom to top).

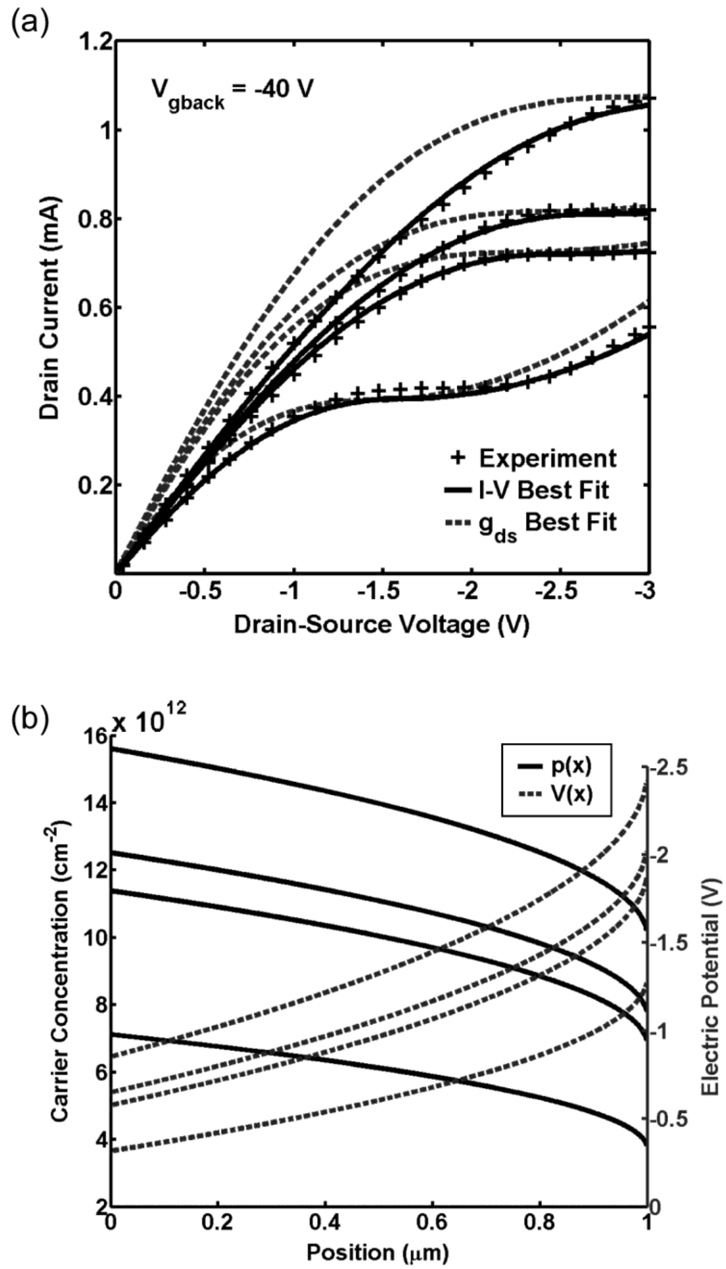
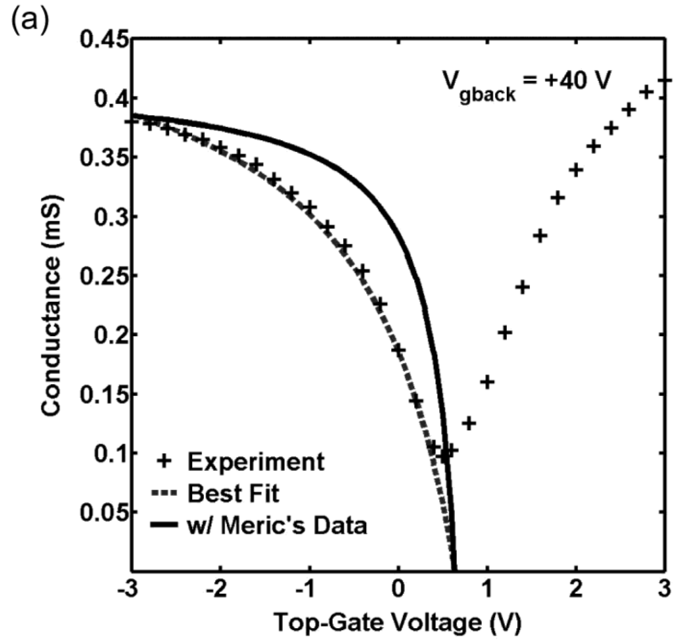


Figure 7. (a) Small-signal source-drain conductance g_{ds} as a function of the top gate voltage minus the threshold voltage V_{g0}. (b) Small-signal source-drain resistance R_{ds} as a function of the inverse of the top gate voltage minus the threshold voltage $1/V_{g0}$ for V_{gback} = +40 V.



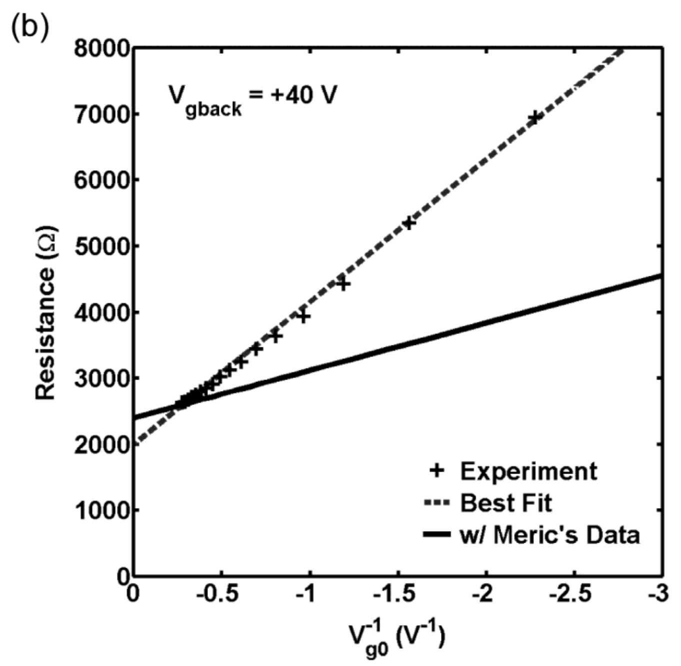


Figure 8. (a) Drain current I_d as a function of drain-source voltage V_{ds} and (b) hole concentration (left axis) and electric potential (right axis) for $V_{ds} = V_{ds(sat)}$ as functions of position along the channel length (source is on the left) for V_{gback} = +40 V; V_{gtop} = −0.8 V, −1.3 V, −1.8 V, −2.3 V and −2.8 V (from bottom to top).

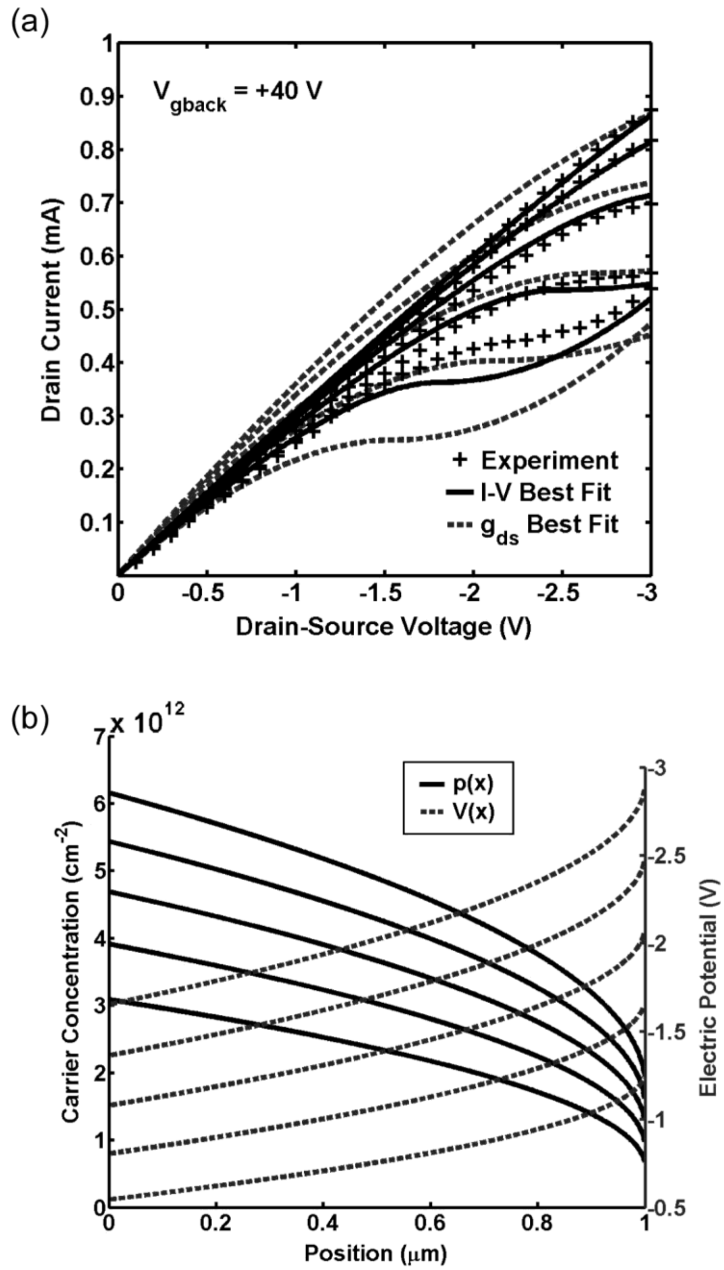


Figure 9. Calculated drain-source voltage $V_{ds(sat)}$ as a function of the top gate voltage V_{gtop} for two V_{gback} biases. The bars are estimated values from the experimental data [3].

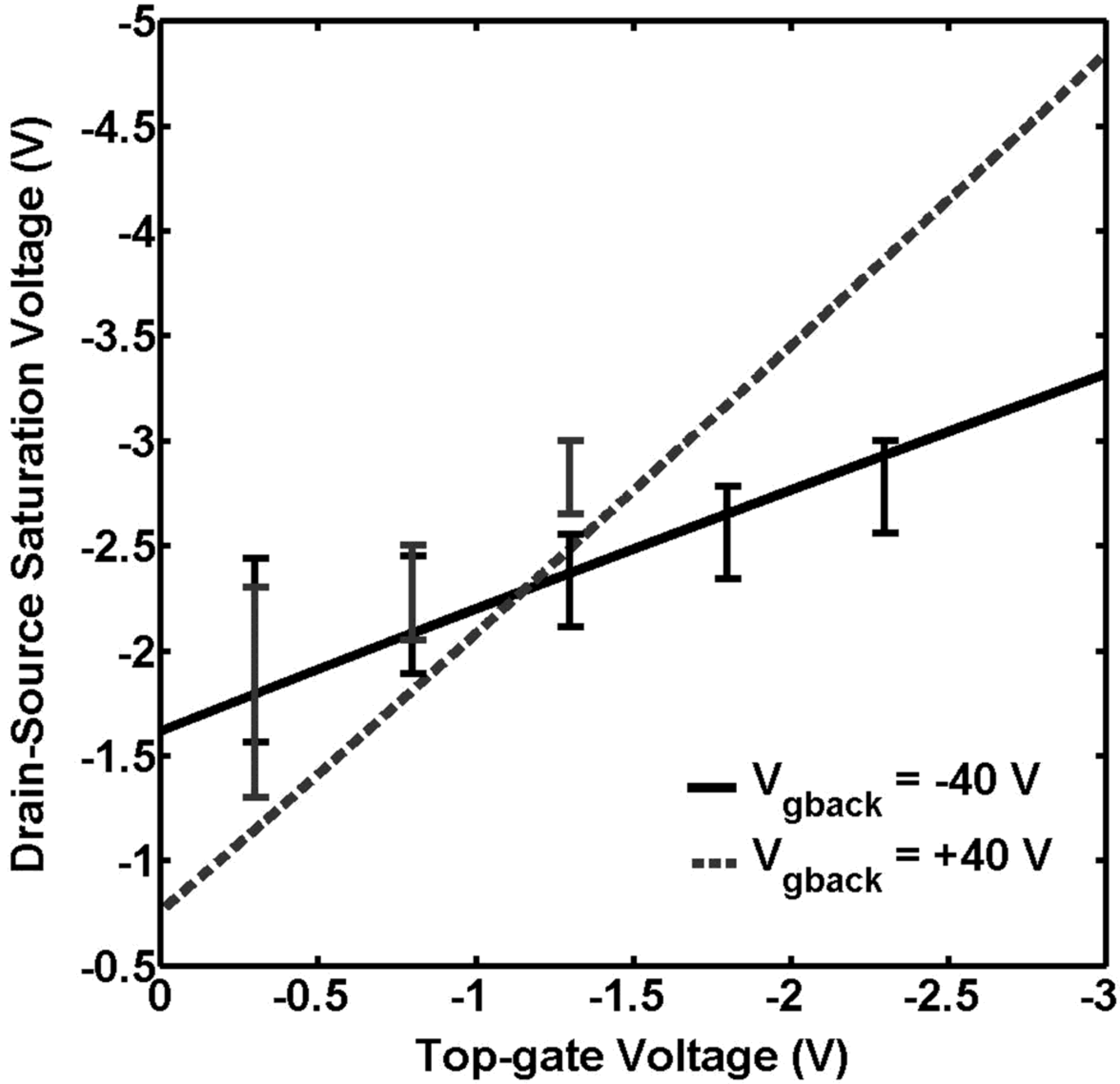


Figure 10. Calculated saturation current $I_{d(sat)}$ as a function of the top gate voltage V_{gtop} for two V_{gback} biases. Crosses (+) and bars (I) are estimated from the experimental data [3].

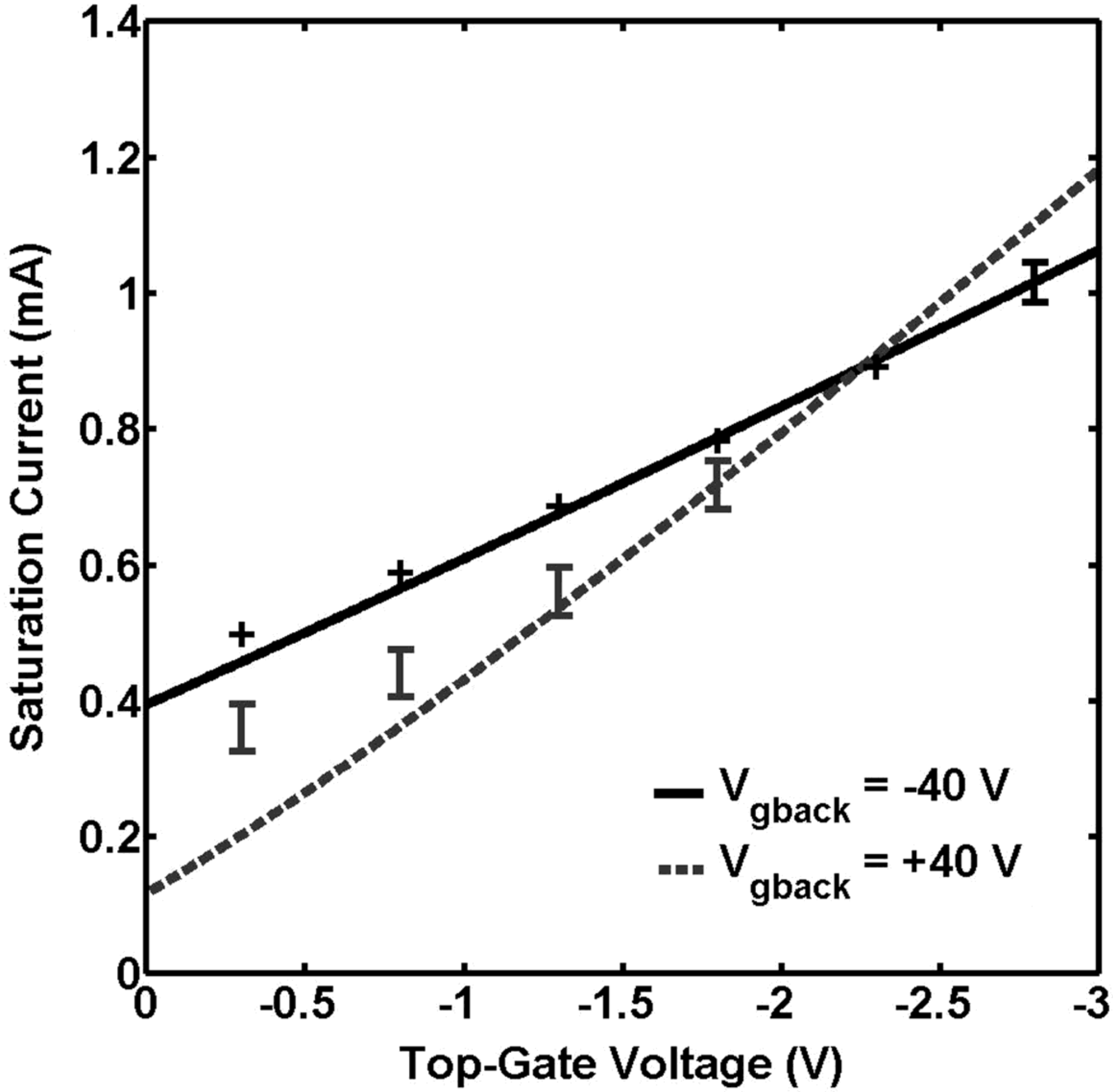
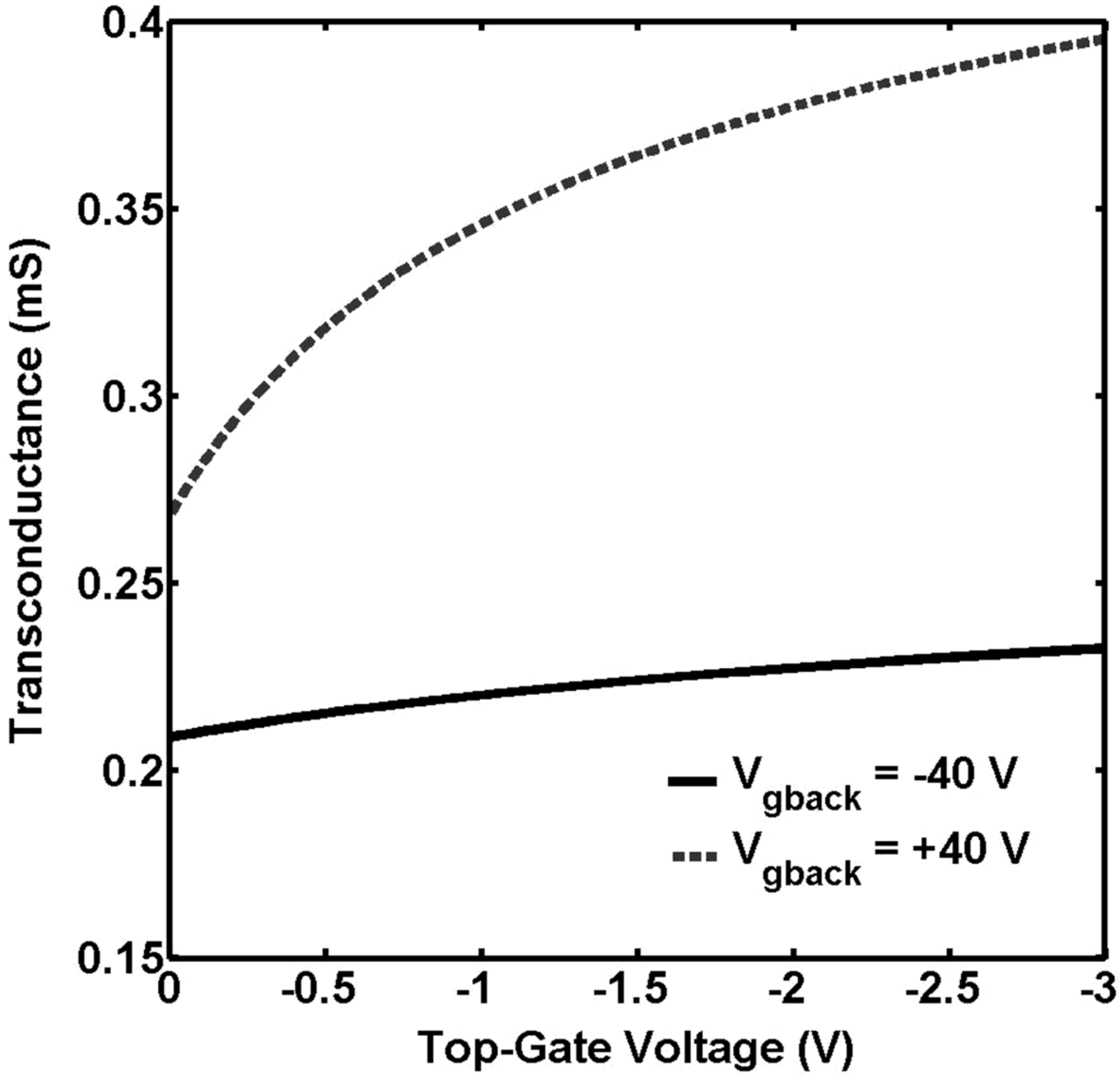


Figure 11. Calculated transconductance at saturation g_m^{sat} as a function of the top gate voltage V_{gtop} for two V_{gback} biases.



CHAPTER 5

DISCUSSION AND CONCLUSIONS

This thesis provides a coherent model for the output and transfer characteristics of GFETs with two back-gate bias configurations, for which the source and drain contacts are either p- or n-type. For unipolar transport, closed form expressions are obtained for the current, low drain bias conductance, transconductance at saturation, saturation voltages, saturation currents, and potential along the channel, which rely on three parameters, i.e., low-field carrier mobility, source-drain resistance, and critical field for the high-energy carrier scattering, to reproduce the experimental *I-V* characteristics for each back-gate condition. In particular, a linear dependence of the low-field resistance versus inverse gate voltage is predicted, which is quantitatively confirmed, while a discrepancy is pointed out between the parameter values used for the g_{ds}-V_{g0} plots and the *I-V* characteristics, especially for positive back gate voltage, which has not been resolved so far. However the predicted quasi-linear dependence between saturation voltage and gate voltage is well confirmed experimentally.

It should be emphasized that this model relies on only one F_c parameter to describe the current at high drain biases for all top gate biases, which according to the velocity field relation *v(F)* implies a single saturation velocity v_{sat} = 3.2 x 10^6 cm/s (1.8 x 10^7 cm/s) for V_{gback} = −40 V (+40 V), unlike Meric's model that requires a concentration dependent saturation velocity to fit the experimental data. In this respect, one should notice that close analysis of the source-drain field profile indicates that the maximum fields achieved in the highest drain biases are only a few times the critical field values F_c, which is far from achieving saturation. It is, therefore, quite possible that the velocity-field relation acquires a lower slope due to remote phonon scattering rather than saturating [14].

Finally, it should be pointed out that this approach is based on the charge-control model in which 1-D analysis is valid for wide devices so that size effects due to confinement are negligible. The device is also "well tempered" and the drain-to-gate voltage ratio is small enough so that the gradual channel approximation is valid. Indeed, detailed analysis of the charge-control model indicates that even for the lowest (negative) top gate bias, i.e., V_{gtop} = 0 V (−0.8 V) for V_{gback} = −40 V (+40 V), the channel never reaches pinch-off, which suggests that the current increase at high drain biases may be due to other causes than electron injection [13]. For shorter gate lengths or higher drain biases, non-linearity in the energy dispersion [15] should be included, as well as carrier multiplication by impact ionization [13].

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