INTEGRATION OF ALIGNED ARRAYS OF SINGLE-WALLED CARBON NANOTUBES IN ELECTRONIC DEVICES

BY

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DISSERTATION

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ABSTRACT

Aligned arrays of single-walled carbon nanotubes (SWNTs) are an attractive format for macroelectronics and RF analog electronics with exceptional electrical, mechanical and optical properties. Unlike isolated SWNT, the presence of many SWNTs in the aligned arrays increases the current output and statistical averaging in many SWNTs is expected to reduce the device to device variations. The SWNTs in aligned arrays do not intersect one another, unlike in networks of SWNTs. Hence, tube/tube contacts, which limit the transport in SWNT networks due to tunneling barriers or electrostatic screening at the contacts to prevent effective gate modulation at those specific points, are absent.

Nonetheless, challenges still remain for these aligned arrays of SWNTs before their successful integration into electronic devices for large scale commercial use. The main challenges include (1) selective elimination of m-SWNTs, (2) increasing the density of SWNTs, (3) achieving electronic uniformity across devices fabricated and (4) understanding their mode of operation and the role of contacts in their operation.

In this dissertation, I present a study that aims to tackle the 3rd and 4th challenges aforementioned. We integrated these arrays of SWNT thin films into field effect transistors to study the electronic uniformity of the devices. We examined the effect of variation in density and diameter distributions of the aligned arrays of SWNTs on the variation in the electrical performance of the transistors. We also analyzed the properties of the contacts at the SWNT/metal interface. We found Pd to be a good Ohmic contact and Ca to be a Schottky contact to the aligned arrays of SWNTs and went on to fabricate Schottky diodes. Using these Schottky diodes, we demonstrated light emitting diodes with aligned arrays of SWNTs which could be used in novel applications that require solid state and nano-scale infra-red emitters. Work done to selectively eliminate m-SWNTs (1st challenge) via selective laser ablation is also archived in this dissertation.

These results represent important steps in understanding the device performance of transistors and Schottky diodes based on aligned arrays of SWNTs; which may have a large impact in large area RF analog electronics.

ACKNOWLEDGEMENTS

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CHAPTER 1:

INTRODUCTION

The main objective of my doctoral research is to study the integration of thin films of aligned arrays of single-walled carbon nanotubes (SWNT) into field effect transistors and diodes. We examined the effect of variation in density and diameter distributions of the aligned arrays of SWNTs on the scatter in the electrical performance of the transistors based on these thin films and analyzed the properties of the contacts at the SWNT/metal interface in these transistors. We found Pd to be a good Ohmic contact and Ca to be a Schottky contact to the aligned arrays of SWNTs and went on to fabricate Schottky diodes. We studied the theoretical and experimental aspects of these Schottky diodes based on aligned arrays of SWNTs and found that a simple physical model, taking into account the basic physics of current rectification, can adequately describe the devices. Using these Schottky diodes, we demonstrated light emitting diodes which could be used in novel applications that require solid state and nano-scale infra-red emitters.

1.1 Introduction to Carbon Nanotubes

SWNTs can be perceived as rolled-up cylinders of graphene sheets. The way a graphene sheet is rolled up is represented by a pair of indices (n,m), as shown in Figure 1.1. This pair of indices determines the chirality and diameter of a SWNT which in turn determines the bandgap as well as the mobility of the SWNT [1,2]. SWNTs are an interesting class of materials to study because of their exceptional electrical [1,2] and optical properties [3]. Semiconducting SWNTs have been considered for use as the active channels in field effect transistors and diodes due to their high mobility (up to 10,000cm^2/Vs)[2] while metallic SWNTs, for use as transparent metal contacts because of their low resistivity [4-6], optical transparency and high current carrying capability (up to 10^9A/cm^2) [7].

Two promising areas of potential application are flexible macroelectronics and RF analog electronics. Flexible macroelectronics, involving large scale electronics beyond the size of a semiconductor wafer, demands materials and processes to be cost effective,

flexible and portable. Applications include rollable displays, printable solar cells or other novel applications that require large scale electronics on non-conventional substrates. SWNTs with their very high mobility [2], mechanical flexibility [8-10] and the ability to deposit solution-based SWNTs directly on polymeric substrates or transfer printed from conventional substrates to other forms of substrates make them attractive for flexible macroelectronics applications. Aligned arrays of SWNTs, which have low intrinsic capacitance and high linearity, have been considered for use in RF analog electronics. Transistors based on aligned arrays of SWNTs have been demonstrated to be able to operate up to GHz frequency with further improvements possible via device optimization, increasing the density of the SWNTs and selectively eliminating the m-SWNTs [11-14].

Transistors based on a single semiconducting SWNT have been demonstrated. They are found to display high mobility (up to 10,000cm^2/Vs) [2], high transconductance (up to 3mS/μm) [15] and high on/off ratio (up to ~10^6) [15]. However, these single SWNTs are difficult to integrate into devices as one needs to know precisely where the single SWNTs are in order to deposit contacts on them. Furthermore, these single SWNTs have different chirality, resulting in non uniformity of electrical performance in devices fabricated. Finally, transistors based on single SWNTs have low current output. The obvious solution of which is to grow thin films of SWNTs.

Thin films of SWNTs can be grown in two different formats: random network or aligned arrays. Scanning electron micrographs of random network of SWNTs and aligned arrays of SWNTs are shown in figure 1.2a and 1.2b respectively. As evident in figure 1.2, there are many tube-tube contacts in the random network which are absent in the aligned arrays. These tube/tube contacts limit the transport in SWNT networks due to tunneling barriers or electrostatic screening at the contacts to prevent effective gate modulation at those specific points [16]. Hence, aligned arrays of SWNTs display superior electrical performance relative to random network of SWNTs, which is essential for RF applications [17,18].

1.2 Alignment in Aligned Arrays of Single-walled Carbon Nanotubes

Carbon nanotubes can be synthesized via arc-discharge [19], laser ablation [20] or chemical vapor deposition (CVD). The first two methods of synthesis mentioned above are difficult to integrate into devices because the alignment and location of the nanotubes cannot be well controlled. On the other hand, CVD growth of carbon nanotube films provides excellent control over alignment and location of nanotubes.

The driving force for alignment in CVD can arise from electrical fields [21,22], laminar flow of feeding gas [23-25] or anisotropic interactions between SWNTs and single crystalline substrates [26-28]. Electric fields induce torques on growing SWNTs to align them [21,22] while laminar flow of the feed gas in CVD growth of SWNTs aligns them [23-25]. SWNTs grown on certain single crystalline substrates (e.g. sapphire and quartz) interact anisotropically, resulting in aligned arrays of SWNTs. In one study, the authors present combined theoretical and experimental studies of alignment of SWNTs on different orientations of quartz [28]. They find that there is an angle dependent van der Waals interaction between the SWNTs and substrate and SWNTs preferentially grow in the directions that minimize the Lennard-Jones potential energy (figure 1.3). These directions correspond to the directions of molecular scale topological grooves on the substrate. They also find that while surface roughness and any small surface relief are not crucial, the crystalline quality of the surface is extremely important. Hence, aligned arrays of SWNTs can be reproducibly grown with very high degrees of alignment on single crystalline substrates.

1.3 Nanotube Field Effect Transistors and Diodes

1.3.1 Nanotube Field Effect Transistors

After the formation of SWNT thin films, transistors or diodes can be fabricated. Single semiconducting-SWNT transistors have been examined and found to be Schottky transistors if a Schottky barrier exits between small diameter SWNTs and the metal electrode [28-32]. On the other hand, ohmic contacts [33,34] have been formed when palladium electrodes are contacted to s-SWNTs which have larger diameters. As current output from a single SWNT transistor is very small, thin films of SWNTs are essential to increase the current output. Thin films of SWNTs can also potentially decrease the device to device variations present in single tube transistors via statistical averaging.

Studies have shown that despite the high mobility of a transistor made from a single semiconducting SWNT (up to 10,000cm^2/Vs) [2], a transistor made from a network of SWNTs has a significantly lower mobility (~80cm^2/Vs) [35]. This has been attributed to the tube-tube junction resistance and the screening effect between tubes which limit the charge transport in the network of tubes. On the other hand, transistors which active conducting channel is aligned arrays of SWNTs are found to retain the high mobility as in a single SWNT transistor.

Figure 1.4a shows the schematic illustration of a top gated field effect transistor which active conducting channel is aligned arrays of SWNTs. Typical source and drain electrodes used are high work function metals, palladium or gold. Hafnium dioxide is deposited to form the dielectric between the gate electrode and SWNT array. A typical transfer curve from a transistor with palladium source and drain electrodes is shown in figure 1.4b. The transistor is predominantly p-type behaving as the Fermi level of high work function metal electrodes used is closer to the valence band. By applying a negative gate bias, the conduction and valence bands are bent upwards. Thus, the tunneling barrier between the palladium source and the valence band is narrowed, enabling holes to tunnel through the Schottky barrier easily. As the holes start to accumulate in the SWNTs, it becomes increasingly difficult for the holes to tunnel into the SWNTs. Hence, the increase in current with gate bias decreases and eventually saturates.

1.3.2 Nanotube Diodes

Besides nanotube transistors, nanotube diodes have been fabricated and examined. Two types of SWNT diodes have been studied; namely p-n junction diodes [36-38] and Schottky diodes [39]. P-n junction diodes can be formed by various means.

A commonly used method is electrostatic doping [36]. This is achieved by using a split-gate geometry. One part of the SWNT is gated p type while the other part is gated n type. The area between these two parts of the SWNT which is not gated forms an intrinsic region. This results in a p-i-n diode which does not suffer from severe reverse leakage. Another technique to form a p-n diode is via chemical doping [38]. One side of the junction is doped by a p-type dopant, tetracyanoquinodimethane (TCNQ) while the other side is doped by a n-type dopant, polyethylenimine (PEI).

The Schottky barrier formed at the SWNT-metal electrode interface is determined by both the diameter of the SWNT (which determines the bandgap of the SWNT) and the work function of the metal electrode used. Aluminum and titanium have been found to form Schottky contacts with SWNTs and have been used in Schottky diodes [39]. Palladium or gold is usually used to form an Ohmic contact for the other electrode in the diode.

1.4 Construction of this Thesis

Chapter 1 provides the outline of the thesis and provides background information about SWNTs and thin film type electronics.

Chapter 2 presents the statistical analysis of the electrical performance variability in transistors that use aligned arrays of single walled carbon nanotubes. We find that when we increase the number of SWNTs in a transistor with aligned arrays of SWNTs, the scatter in the on current, maximum transconductance, threshold voltage and off current of the devices do not decrease as rapidly as we expect based on statistical averaging. This is because of (1) the variation in the number of SWNTs in the transistors fabricated with the aligned arrays of SWNTs and (2) the different statistical distributions of diameter for different transistors having the same channel width.

Chapter 3 reports the intrinsic performance variability in aligned array SWNT field effect transistors. Using measured diameter distributions, detailed numerical simulations are performed to demonstrate that the diameter distribution of SWNTs in field effect transistors using aligned array of SWNTs plays a dominant role in the fluctuation of the electrical performance of the device at short channel length. This fluctuation in electrical performance ranges from the fluctuation in on current to that in device modulation.

Chapter 4 reports scaling properties in transistors that use aligned arrays of single walled carbon nanotubes. Using the transmission line model, the dependence of device properties on channel length are studied, to reveal the role of contact and channel resistance in the operation. Two systems are examined; one with palladium electrodes and the other with gold electrodes.

Chapter 5 demonstrates near-infrared electroluminescence from ambipolar, electrolyte-gated arrays of SWNTs. Numerous emission spots corresponding to individual SWNTs in the array are observed. When the electron and hole accumulation zones determined by the applied gate and source-drain voltages meet, these spots will emit light. The movement of emission spots with gate voltage yields information about the relative band gaps, contact resistance, defects, and interaction between carbon nanotubes within the array.

Chapter 6 presents theoretical and experimental studies of Schottky diodes that use aligned arrays of single walled carbon nanotubes. A simple physical model, taking into account the basic physics of current rectification, can adequately describe both the single-tube and array devices.

Chapter 7 demonstrates light emitting Schottky diodes based on aligned arrays of SWNTs. Electroluminescence was observed from Schottky-diode structure based on Ca and Pd asymmetric contacts. Light emission occurs spatially near the Ca/Al contact under forward biased condition. Both the current and the emission intensity increases linearly with the voltage beyond a certain threshold voltage, but the emission onset is higher. The spectral peaks observed are broad with the FWHM ranging from 80meV to 120meV. Further understanding of the causes for differences in threshold voltage for current and light emission and peak broadening is expected to be achieved through ongoing modeling. The light emission is mainly due to electron hole recombination near the Schottky contact, while impact excitation and black body radiation (BBR) may be the causes of light emission at higher voltages.

Chapter 8 archives work done to selectively remove m-SWNTs via laser ablation. This is very challenging because of the varying diameter distribution of SWNTs across the substrate which results in inconsistent electrical performance of transistors based on selectively ablated SWNTs. In addition, to achieve transistors with very high I_{on} / I_{off} ratio, very small proportion of m-SWNTs are allowed to be present. This is very difficult to achieve as not all m-SWNTs absorb the same wavelength of light very effectively. Some s-SWNTs also absorb at the same wavelength of light as certain m-SWNTs, which results in undesired ablation and / or degradation of s-SWNTs too.

Chapter 9 summarizes the results of our studies and discusses possible future work in this field.

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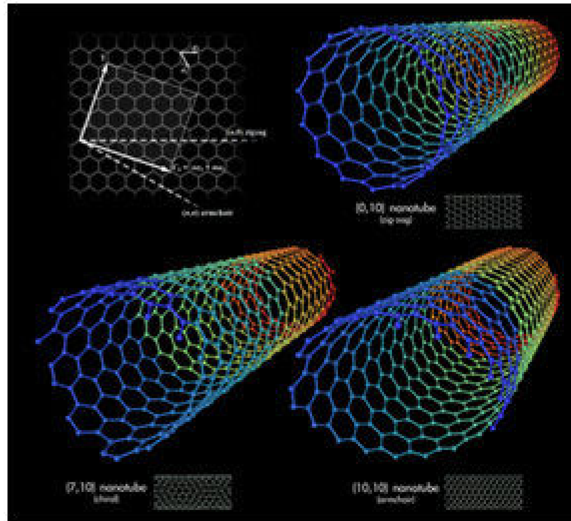
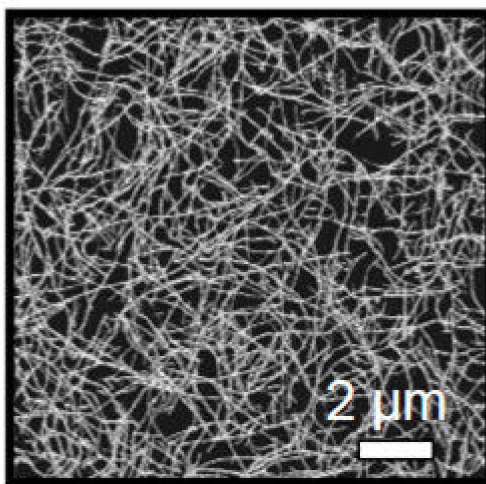
1.6 Figures



http://www.nanoscienceworks.org/Members/siebo/657pxtypes_of_carbon_nanotubes.png/view

Figure 1.1 Single layers of graphene sheets are rolled up to form various kinds of carbon nanotubes.

a.



b.

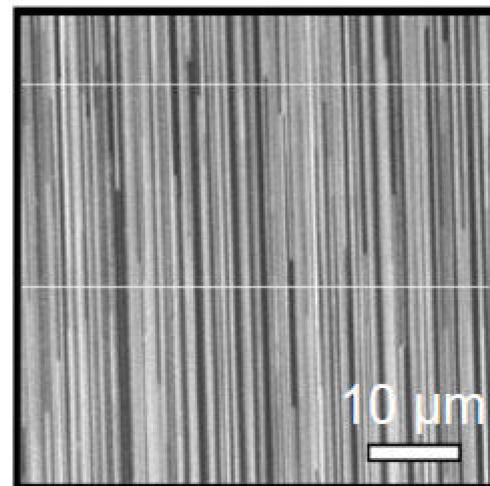


Figure 1.2 Random networks (a) and aligned arrays (b) of SWNTs grown via chemical vapor deposition.

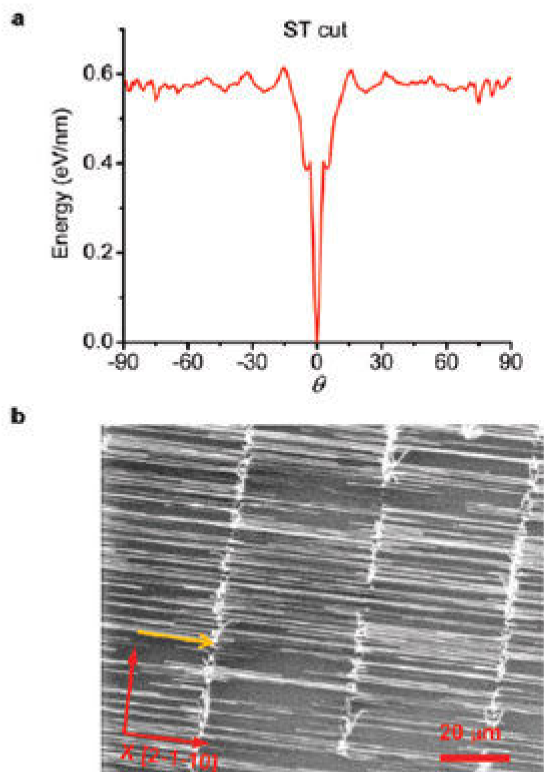
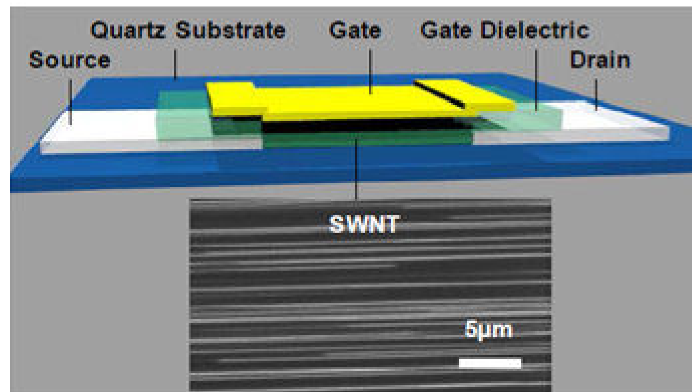


Figure 1.3 Interaction energy between a SWNT and ST cut quartz, as a function of orientation angle, and experimental results. (a) Energy map for a SWNT with radius 0.6 nm on quartz. The results show a single preferred orientation, at 0°. (b) SEM image of experimental results, showing behavior consistent with theory. The orange arrow indicates the flow direction. In a typical case such as this one, more than 99.91% of the total lengths of the SWNTs lie along the preferred direction, not including the regions where the catalyst particles are located. Reproduced with permission from Ref. [26]. Copyright 2009 American Chemical Society.

a.



b.

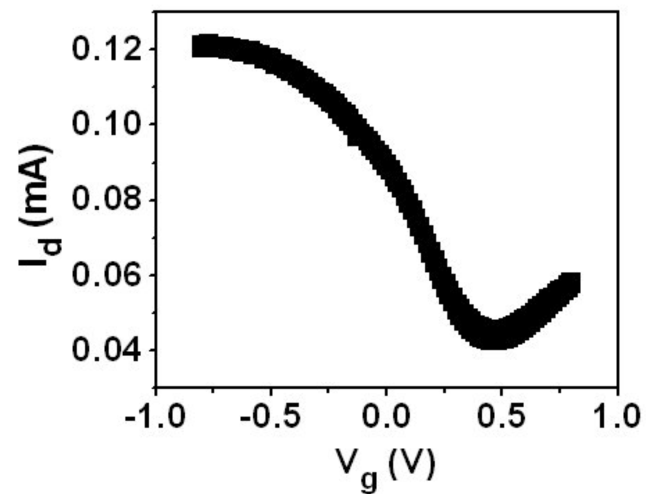


Figure 1.4 (a) Schematic illustration of a top gated thin film transistor. Bottom image shows a SEM image of an aligned array of SWNTs. (b) Transfer curve of an aligned array SWNT thin film transistor. In this case, the channel width is 400μm and the channel length is 5μm. Tube density is 4SWNTs/μm. Metal electrodes used are palladium.

CHAPTER 2:

STATISTICAL ANALYSIS OF THE ELECTRICAL PERFORMANCE VARIABILITY IN TRANSISTORS THAT USE ALIGNED ARRAYS OF SINGLE WALLED CARBON NANOTUBES

2.1 Introduction

Transistors based on single semiconducting single walled carbon nanotubes (SWNTs) have been demonstrated. These devices are found to have high mobility up to 10,000cm^2/Vs, [1] high transconductance up to 3mS/µm [2] and high on/off ratio, ~10^6. [2] This generates an interest in studying SWNTs for use in electronic devices. However, these test structures based on single SWNTs have low current output and non-uniformity in electrical performance because of the variation in diameter and chirality of SWNTs grown. [3,4] Hence, for practical use of SWNTs in transistors, thin films of SWNTs containing SWNTs of a certain high density are more attractive because the current output will be higher and statistical averaging can result in more uniform electrical performance.

Transistors based on thin film of random SWNT networks have demonstrated attractive device performance [5] and thus, been considered as alternative semiconducting materials for use in flexible electronics [6] or transparent electronics. [7] On the other hand, transistors based on aligned arrays of SWNTs have superior electrical performance than its random counterpart, which makes aligned array SWNT transistors to be attractive in applications with high demand requirements such as RF analog electronics. [8-10] However, integration of such aligned SWNT arrays in transistors for large scale commercial use requires them to be uniform in electrical performance. Our measurement of transistors based on aligned arrays of SWNTs (schematically shown in Figure 2.1a) indicates considerable variation in its I-V characteristics (Figure 2.1b).

Our previous work [11] has indicated that variation in the on current of transistors based on aligned array of SWNTs can be attributed to variation in the diameter distribution of SWNTs. However, we did not consider the effect of SWNT density variation in the arrays, which can also potentially contribute to additional variation [12]. Reference 12 also claims that in devices with many SWNTs, the variation contributed by

the diameter distribution is strongly diminished by statistical averaging. This contradicts with our previous study. Our earlier analysis was limited because we only considered the effect of diameter of SWNT on the Schottky barrier height at the SWNT-metal electrode interface. However, at relatively long channel lengths (> a few μm), the on current of a SWNT can instead be limited by its channel conductance instead of contact conductance. This is especially true for SWNTs with large diameters (hence small bandgap and small Schottky barrier at the SWNT-metal electrode interface). Furthermore, the contribution of SWNTs with large diameters to the overall on current of a transistor based on aligned array of SWNTs is more significant because SWNTs with larger diameters carry more current. Similarly, a previous study from another group (reference 3) has also considered the effect of contact conductance only but not channel conductance, which we will consider in this work.

This chapter seeks to examine the extent of statistical averaging in reducing the device to device variations in transistors based on aligned arrays of SWNTs very thoroughly. In this study, we fabricate and characterize field-effect transistors consisting of a single SWNT (single-SWNT FETs). Using these single-SWNT FETs as the basis, we simulate transistors consisting of aligned arrays of SWNTs (array-SWNT FETs). Later, we compare the I-V characteristics and the extracted on current and maximum transconductance of these simulated array-SWNT FETs to those of fabricated array-SWNT FETs. Our analysis suggests that the variations in fabricated array-SWNT FETs do not reduce as $1/\sqrt{n}$ (central limit theorem) as we would expect, where n is the number of SWNTs in array-SWNT FETs. We attribute these inconsistencies to the variations in spatial density and diameter distribution of SWNTs across the wafer.

In addition, we also study in detail the dependence of the on current, maximum transconductance and threshold voltage of single semiconducting SWNT (s-SWNT) devices on the diameter of the SWNTs. The variation in on current and maximum transconductance can be attributed to variations in diameter. The threshold voltage has also previously been attributed to the diameter only [13]. However, we show that the SWNT threshold voltage statistics should consider the contributions from extrinsic factors, e.g. the variations in defect density across the wafer [14,15,16]. These results

provide key insights into the causes of variations in transistors and directions to eliminate these variations in future.

2.2 Methods for Fabricating Single and Array SWNT FETs

Figure 2.1a shows a schematic illustration of a transistor that uses aligned arrays of single walled carbon nanotubes (SWNTs) or a single SWNT as the semiconducting material. A scanning electron microscope (SEM) image of an aligned array of SWNTs is also shown below for illustration. To fabricate aligned array SWNT FETs, aligned SWNTs are grown via chemical vapor deposition (CVD) on ST (stable temperature) cut quartz substrate, using procedures described elsewhere. [15,16] Next, we define source and drain electrodes (60 nm Pd/ 2 nm Ti) by photolithography and lift-off and etch SWNT outside the channel regions (defined by channel length and width). The channel length of the fabricated transistors is ~10µm. A layer of ~35nm spin-coated and heat-treated Spin-On Glass (SOG) and a layer of ~20nm ALD-grown hafnium oxide (HfO_2) are deposited on top of the contacts and SWNTs, forming the gate dielectrics. This is followed by a gate electrode (Au (60 nm)/ Ti (2 nm)) deposition, which is again defined by photolithography and liftoff to complete the transistors.

Fabrication of single SWNT FETs follows a similar process. However, we etch all but a small width of 1.5µm, thus resulting in FETs with a small number of SWNTs. The devices are examined using SEM and the FETs with a single SWNT are selected. As a purely stochastic process, resultant yield of single SWNT FETs is low, ~3%.

2.3 Characteristics of Single SWNT FETs

Understanding of the statistics of an array SWNT FET requires us to comprehend the characteristics of its basic building block, i.e. the characteristics of single SWNT itself. So far, several studies [1, 11, 14, 17-24] have characterized single SWNT FETs and examined the effect of SWNT diameter and source/drain metal electrodes on their I-V properties. These studies have identified the following key features of SWNT FETs:

- SWNT FETs with Pd source/drain electrodes have p-type properties.
- Small diameter SWNT has large bandgap and p-type conduction in the corresponding FET is dictated by the Schottky barrier near the source/drain electrode.

- On the other hand, large diameter SWNT has small bandgap and the corresponding FET has no Schottky barrier near the source/drain electrode. Hence, p-type conduction in these FETs is dictated by the intrinsic properties of SWNT channel.
- P-type conduction in large diameter SWNT FET indicates linear relationship between the channel conductance and diameter (which also corresponds to a quadratic relationship between the effective mobility and diameter).
- The magnitude of conductance and effective mobility of SWNT FET strongly depends on its surrounding environment.

In this section, we study the properties of our fabricated SWNT FETs, estimate the conventional electrical parameters of SWNT FETs (like threshold voltage, maximum transconductance, ON current, etc.) and identify their dependence on SWNT diameter. In addition, we develop a simple model explaining the diameter dependence of SWNT FETs electrical parameters. In consistency with literature, we identify that most of the electrical parameters (except threshold voltage) of SWNT FETs can solely be explained by understanding their diameter dependence. Therefore, knowledge of diameter distribution and SWNT density distribution across the wafer is sufficient to study the performance statistics (except threshold voltage) of array SWNT FETs (see section 2.4.3 for details). We show that the variation of threshold voltage of SWNT FETs depends weakly on diameter and (presumably) depends on extrinsic factors like interface defect density, metal workfunction [25-27], etc. Such understanding of the SWNT's performance variation with diameter, along with the information related to diameter distribution and SWNT density distribution across the wafer, enables us to explain the statistics of array SWNT FETs, as discussed in section 2.4.

2.3.1 Measurement of Single SWNT FET

Figure 2.2a shows a SEM image of a single SWNT contacted to two metal electrodes to the right and left of the image, before depositing the gate dielectric and metal gate to complete the single SWNT FET. Figure 2.2b and 2.2c show typical transfer curves of transistors based on a single semiconducting SWNT (s-SWNT) and a single quasi metallic SWNT (m-SWNT), respectively, measured with the source grounded, the

drain held at a bias of -0.05 V, and the gate bias (V_G) swept between ±1.5V. The single s-SWNT devices have high ON/OFF ratio = I_{ON}/I_{OFF} (here, the ON current I_{ON} is considered as the I_D at V_G = -1.5V and OFF current I_{OFF} is considered as the minimum I_D) and show predominantly p-type behavior. On the other hand, single quasi m-SWNT devices have very small gate modulation (ON/OFF ratio of < 100) and show ambipolar behavior (with a smaller n type tail). Small gate modulation of quasi m-SWNT devices are not totally unexpected and have been reported previously. [28-29] This phenomenon has been attributed to the Mott insulating state in m-SWNTs [28] or the strain induced bandgap in m-SWNTs [29]. The difference in electrical properties of quasi m-SWNT FETs and s-SWNT FETs is more clearly visible in Figure 2.2d, where we plot I_{OFF} vs I_{ON} for all the 45 single (quasi metallic and semiconducting) SWNT FETs measured. The symbols representing the quasi m-SWNT FETs (having ON/OFF ratio < 100) are in the shaded maroon region, while the symbols representing the s-SWNT devices (having ON/OFF ratio > 100) are in the shaded blue region. The single s-SWNT FETs have I_{OFF} that are orders of magnitude smaller than most of the single m-SWNT FETs. Note that the measured I_{OFF} of s-SWNT devices are limited at ~0.1-1pA, which is due to the Agilient parametric analyzer's current resolution limit. Actual I_{OFF} of s-SWNT FETs may be significantly lower than this measured pA current.

2.3.2 Modeling of s-SWNT FET

Figure 2.3a replots the I-V characteristics of 25 measured s-SWNT FETs (having ON/OFF ratio >100). Here, we model the s-SWNT I-V characteristics and check if the variation in electrical parameters of s-SWNT is due to variation in diameter. We simulate the I-V characteristics of s-SWNT at small drain bias by determining the source-to-drain conductance (G_{DS}) of s-SWNT FET, as a combination of contact conductance (G_C) and s-SWNT channel conductance (G_{CNT}). Later on, we calculate the drain current, I_D, at a particular gate voltage, $V_G = E_{Fi} + Q/C_G$, using $I_D = G_{DS}*V_{DS}$, where V_{DS} is the drain voltage, $E_{Fi} = E_i – E_F$, E_i is the intrinsic Fermi level of s-SWNT (*i.e.*, the mid-gap energy level), E_F is the Fermi energy level in the s-SWNT, C_G is the gate capacitance, and Q is the charge density that is expressed as

$$Q = -q\int_{-\infty}^{\infty} dE * sign(E) * v(E) * f(sign(E) * (E - E_{Fi})) \quad (1)$$

where $v(E) = \frac{4}{\pi \hbar v_F} \frac{|E| u(E - E_{Fi})}{\sqrt{E^2 - E_{Fi}{}^2}}$ [30-33], *v(E)* is the density of states in the s-SWNT, *f(sign(E)*(E-E$_{Fi}$))* is the Fermi distribution in the s-SWNT, u(E) is the unit step function, and sign(E) is the sign of energy level E.

Once, we calculate E_{Fi}, hence V_G, for a particular value of Q, we can estimate G_{DS} using

$$G_{DS} = G_{DS,e} + G_{DS,h} = (G_{CNT,e}{}^{-1} + G_{C,e}{}^{-1})^{-1} + (G_{CNT,h}{}^{-1} + G_{C,h}{}^{-1})^{-1} \quad (2)$$

where G_{CNT} within single sub-band approximation is expressed as [1],

$$G_{CNT,e(h)} = \frac{4q^2}{h} \frac{\tau_0 v_0}{L} \frac{[|Q_{e(h)}|/V_A]^2}{1 + [|Q_{e(h)}|/V_A]^2} \quad (3)$$

where $V_A = \frac{8q}{3\pi d}$, q is the electron charge, h is Planck's constant, L is channel length, $\tau_0{}^{-1}$ is the scattering rate in the SWNT channel at Fermi velocity, v_0. Following the expression for acoustic phonon scattering rate in [1], we express the scattering rate using, $\tau_0{}^{-1} = \alpha \frac{T}{d}$, where T is the temperature in °K, and α is the scattering coefficient. d is the diameter of the SWNT and $Q_{e(h)}$ is the electron (hole) density within SWNT channel and can be calculated as

$$Q_e = -q\int_{0}^{\infty} dE * sign(E) * v(E) * f(sign(E) * (E - E_{Fi}))$$

$$Q_h = -q\int_{\infty}^{0} dE * sign(E) * v(E) * f(sign(E) * (E - E_{Fi}))$$

(4)

Calculation of G_{DS} in equation (2) also requires us to obtain G_C, which is considered as a multiplication of G_{C0} (the contact conductance for large s-SWNT diameter and large V_G, so that carriers can be injected barrier-free from contact into

SWNT) and contact Transmission probability T_C; i.e. $G_C = G_{C0}T_C$ with $T_C = T_{therm} + T_{SB} + T_{BTBT}$. The transmission probability through the contact has contributions from

(1) thermionic emission (T_{therm}). T_{therm} is expressed as $exp(-E_{barrier}/kT)$; where $E_{barrier}$ is the thermal barrier for carrier injection from contact into the channel,

(2) Schottky barrier tunneling (T_{SB}). T_{SB} is expressed as where k_z is parallel momentum related to the E-k relationship in CNT [33] at distance z from the contact into the channel,

(3) band to band tunneling (T_{BTBT}). T_{BTBT} is expressed as $\exp(-E_G{}^2 / q\hbar v_0 F_z)$ [34], where E_G is the bandgap of CNT, F_z is the electric field at the location of band to band tunneling.

Following the approach summarized above, we calculate I_D-V_G of s-SWNTs for various diameters (figure 2.3b) using $v_0 = 8\times10^5$ m/s, α = 80m/K-s, G_{c0} = 1/28kΩ [1], T = 300 ^{0}K. The simulated transfer curves match closely with the measured transfer curves in Figure 2.3a. With these parameters, our simulation suggests a diameter range of 0.5-1.5nm for the measured transfer characteristics of Figure 2.3a. Note that the required value of scattering parameter α, for matching the I-V characteristics using a reasonable diameter range of 0.5-1.5nm, is much larger than the ones reported in [1,24,35]. This can be due to the existence of more scattering in our samples. Next, we calculate $I_{ON} \equiv I_D@V_G-V_T=-1V$, maximum transconductance ($g_{m,\max} = \max\left(\partial I_D/\partial V_G\right)$) and V_T (defined as V_G for $I_{D,max}/100$) of single s-SWNT devices and plot them in figure 2.3c, 2.3d and 2.3e, respectively. I_{ON} vs diameter relationship of Figure 2.3c suggests a non-linear increase of I_{ON} at smaller diameter, where $T_C < 1$. At larger diameter, $T_C \sim 1$ and the source-to-drain conduction is mostly limited by the CNT channel and hence, $I_{ON} \sim \tau_0^{-1} \sim d$ [1]. $g_{m,max}$ vs diameter relationship of Figure 2.3d suggests a non-linear relationship at smaller diameter (where, $T_C < 1$) and $g_{m,max}$ ~ SWNT mobility ~ d^2 [1] relationship at larger diameter, where $T_C \sim 1$. Note that the diameter threshold for observing a change in the electrical-parameter vs diameter as we move from the $T_C < 1$ to $T_C \sim 1$ region (in Figure 2.3c and 2.3d) depends on CNT work-function (Φ_{CNT}), V_G-V_T, and contact work-function (Φ_C) used in the simulation. In general, the diameter threshold is smaller for larger V_G-V_T and smaller (Φ_C - Φ_{CNT}). Figure 2.3e shows V_T vs diameter relationship for

single s-SWNT transistors. This relationship mainly depends on the definition of V_T being used. Since V_T is defined as the V_G for $I_D = I_{D,max}/100$, at smaller diameter or larger SWNT bandgap (when $T_C < 1$), the non-linear conduction is dictated by the Schottky barrier at the contact and hence V_T increases rapidly with diameter. At larger diameter (when $T_C \sim 1$), Schottky barrier height reduces to zero and the linear increase in $I_{D,max}$ with diameter also results in a corresponding increase of V_T.

2.4 Statistics of Array SWNT FETs

Our knowledge of s-SWNT electrical parameters and their diameter dependence enables us to estimate the statistics of array SWNT FETs by following the algorithm that is presented in Figure 2.4 for studying the ON current statistics (one can follow similar algorithm with appropriate changes for other electrical parameters) and hence compare with array SWNT FET measurements. This allows us to understand the extent of statistical averaging in reducing the device to device variations in array-SWNT FETs. The input to our algorithm is the diameter distribution and the SWNT density distribution across the wafer, which is known from measurements (see section 2.4.1 and Figure 2.5). For simulating an array SWNT FET having a nominal number of <n> SWNT,

1. We either randomly choose n from a (presumed) normal distribution of SWNT having mean <n>, or choose n = <n>.

2. At the same time, we also choose a diameter distribution for the same array SWNT FETs that has a mean and standard deviation of the diameter. Such mean and standard deviation are either randomly chosen from the values measured in Figure 2.5b-c or kept the same for the entire set of array SWNT FETs.

3. Choice of a particular diameter distribution, along with the diameter dependence of electrical parameters (as shown in Figure 2.3c-e), enables us to obtain the distribution of electrical parameters (one such example is shown in Figure 2.6).

4. Later, we choose n values of electrical parameters from the distribution and appropriately sum them for estimating the electrical parameters of an array SWNT FET.

For simulating a different array SWNT FET, we repeat the same steps as mentioned above.

2.4.1 Diameter and Density Distributions

Simulation of array SWNT FET statistics uses the SWNT density distribution and diameter distribution across the wafer as an input. Therefore, we measure these values across the wafer and summarize them in Figure 2.5. Figure 2.5a show the measured SWNT density distribution (via Atomic Force Microscopy AFM) on a substrate for a scanned area of 20µm (normal to the alignment direction of SWNT) X 1.25 µm (parallel to the alignment direction of SWNT), which has average SWNT $\langle n \rangle = 13$ and standard deviation of 69% of $\langle n \rangle$. The SWNT density can vary significantly even though the separation between two distributions is only 200µm. Therefore, our simulation of array SWNT FET statistics should consider different n for different array SWNT FETs. Similarly, wide variation in the mean and standard deviation of the diameter distribution at different locations of the substrate (for the same scan area) is also observed in Figure 2.5b and 2.5c, respectively. Figure 2.5d shows a representative diameter distribution for a wider scanned area. The distribution is better fitted (have less sum of squares error) using a log-normal distribution compared to a Poisson distribution. Therefore, we determine the variation of log-normal distribution parameters across the wafer. In simulating different array SWNT FETs, we either randomly choose log-normal distribution parameters within the measured range (see Figures 2.8d and 2.8f) or keep the log-normal distribution parameters fixed to a measured value (see Figures 2.7b, 2.7c, 2.7e, 2.8a, and 2.8b).

2.4.2 Distribution of s-SWNT Electrical Parameters

Once we obtain the dependence of s-SWNT electrical parameters on diameter (Figure 2.3c-e), we can use a particular diameter distribution to estimate the distribution of s-SWNT parameters for that diameter distribution. Later, we compare the simulated distribution of s-SWNT electrical parameters with the ones obtained from single s-SWNT FET measurements. We fit a representative statistics of diameter (inset of Figure 2.6a) using log-normal distribution and hence use Figure 2.3c to estimate the distribution of $I_{ON} \equiv I_D@V_G\text{-}V_T\text{=-}1V$ (Figure 2.6a). Simulated distribution agrees reasonably well I_{ON} distribution of Figure 2.6b, which has been derived from Figure 2.3a. We also perform similar simulation of $g_{m,max}$ and $V_T - \langle V_T \rangle$ distributions, as shown in Figure 2.6c and

2.6e, respectively and compare them with the measurements of Figure 2.6d and 2.6f, respectively. However, unlike the I_{ON} and $g_{m,max}$ distribution, measured $V_T - <V_T>$ distribution shows inconsistency with the simulated distribution. Therefore, diameter distribution of s-SWNTs may not be the main factor that controls the measured variations in $V_T - <V_T>$. Instead, the variation in $V_T - <V_T>$ is expected to originate from extrinsic factors, such as variations in oxide/interface defects at the SWNT/gate dielectric interface and/or variation in metal-gate workfunction. The shape of the V_T distribution will therefore reflect the variation of these extrinsic factors in our fabricated FETs.

2.4.3 Comparing simulated and measured array-SWNT FETs

Once we have estimated the distribution of electrical performance parameters or I-V characteristics as a whole (for a particular diameter distribution, chosen from a set), we can simulate statistical distribution of electrical parameters or I-V characteristics for an array SWNT FET. To perform this for a particular array SWNT FET having a nominal number of <n> SWNT, we either choose n = <n> ('fixed n' simulation) or choose n from the expected SWNT density distribution with mean <n> ('variable n' simulation). Next, we randomly select n values of electrical parameters like I_{ON} ($I_{ON,i=1\ldots n}$) from the distribution like Figure 2.6a. Then for estimating the ON current for the simulated array SWNT FET (I_{ARRAY}), we sum $I_{ON,i}$ and thus calculate $I_{ARRAY} = \sum_{i=1}^{n} I_{ON,i}$. On the other hand, for estimating maximum transconductance (g_{ARRAY}) and threshold voltage ($V_{T,ARRAY}$) for simulated array SWNT FET, we sum the randomly selected n I-V characteristics (I-V_i) to obtain I-V characteristics of array SWNT FET (I-V_{ARRAY}). From I-V_{ARRAY}, we can estimate g_{ARRAY} and $V_{T,ARRAY}$. For simulating a different array SWNT FET, we either choose the same n = <n> for 'fixed n' simulation or choose a different n from the SWNT density distribution for 'variable n' simulation. Input diameter distribution to our simulator can either be considered as fixed (as done in Figures 2.7b, 2.7c, 2.7e, 2.8a, and 2.8b) or variable (as done in Figures 2.8d and 2.8f).

After repeating the calculation for a number of array SWNT FETs having same <n>, we can estimate the statistics of electrical parameters like I_{ARRAY}, g_{ARRAY}, $V_{T,ARRAY}$ for the array SWNT FETs. Let us now understand the effect of the experimentally

observed distribution of SWNT density and diameter on the statistics of array SWNT FET's electrical parameters. We add the effect of one distribution at a time for studying the I_{ARRAY} statistics in detail and later extend our analysis for other SWNT FET's electrical parameters.

First, we consider the case for no variation in SWNT density (*i.e.*, $n = \langle n \rangle$) and input diameter distribution for array SWNT FET. Using this approach, we simulate the $I_{ARRAY}/\langle n \rangle$ (Figure 2.7a) and observe gradual narrowing of the distribution with increasing $\langle n \rangle$. Following the central limit theorem, the normalized standard deviation of $I_{ARRAY}/\langle n \rangle$ distribution, ($\sigma_n/\sigma_1(I_{ARRAY})$), reduces as $1/\sqrt{\langle n \rangle}$ (Figure 2.7b). Estimation of $\sigma_n/\sigma_1(I_{ARRAY})$ of measured array SWNT FET suggests significant deviation from the $1/\sqrt{\langle n \rangle}$ relationship (Figure 2.7c). This indicates the necessity to consider the variation in SWNT density and input diameter distribution for understanding the statistics of array SWNT FETs.

Next, we consider the effect of variation in mean $I_{ARRAY}/\langle n \rangle$ on the statistics of array SWNT FETs. Considering that the mean of any distribution is related to the standard deviation (for example, $\mu \sim \sigma^2$ for the Poisson distribution), a systematic variation in mean $I_{ARRAY}/\langle n \rangle$ might enable us to explain the deviation from $1/\sqrt{\langle n \rangle}$ in Figure 2.7c. Therefore, we determine the statistics of $I_{ARRAY}/\langle n \rangle$ for all array SWNT FETs and observe Log-normal distribution to better fit (with smaller sum of square error) the $I_{ARRAY}/\langle n \rangle$, compared to a Poisson distribution (Figure 2.7d). However, since Poisson distribution has a simple relationship of $\mu \sim \sigma^2$ and has reasonable fitting for the array SWNT FET statistics, we use $\mu \sim \sigma^2$ in the rest of our analysis for compensating the disparity of $\mu_{n,I}$ (see the inset of Figure 2.7e) in our array transistors. Therefore, scaling $1/\sqrt{\langle n \rangle}$ with $\sqrt{(\mu_n/\mu_1)_{EXP}}$ (obtained from measurement) enables us to capture the effect of variation in mean $I_{ARRAY}/\langle n \rangle$. Figure 2.7e suggests that such scaling of $1/\sqrt{\langle n \rangle}$ (which is consistent with simple statistical simulation of Figure 2.7a-b) cannot explain the measured $\sigma_n/\sigma_1(I_{ARRAY})$ of Figure 2.7c.

Later, we consider the effect of SWNT density variation on the statistics of array SWNT FET. Our simulation (Figure 2.8a) suggests that the consideration of SWNT density variation (variable n simulation) causes deviation from $1/\sqrt{\langle n \rangle}$, when we use $I_{ARRAY}/\langle n \rangle$ for calculating $\sigma_n/\sigma_1(I_{ARRAY})$. However, a calculation of $\sigma_n/\sigma_1(I_{ARRAY})$ using

I_{ARRAY}/n (*i.e.*, calculating average ON current carried by a SWNT in array SWNT FET by dividing with the respective n, rather than $\langle n \rangle$, for that array SWNT FET) eliminates the effect of SWNT density variation from the statistics of array SWNT FETs (Figure 2.8b). Simulated $\sigma_n/\sigma_1(I_{ARRAY})$ for array SWNT FETs that considers the effect of SWNT density variation suggests negligible deviation from $1/\sqrt{\langle n \rangle}$, when I_{ARRAY}/n is used for calculating $\sigma_n/\sigma_1(I_{ARRAY})$. However, similar calculation of measured $\sigma_n/\sigma_1(I_{ARRAY})$ using I_{ARRAY}/n still shows significant deviation from the $1/\sqrt{\langle n \rangle}$ relationship (Figure 2.8c). This enables us to conclude that we still need to consider the effect of diameter distribution in calculating $\sigma_n/\sigma_1(I_{ARRAY})$, which mainly dictates the statistics of array SWNT FETs.

Finally, we consider the effect of both variations in SWNT density and diameter distribution for explaining the statistics of array SWNT FETs. Figure 2.8d suggests that the inclusion of variation in diameter distribution from one array SWNT to another (but having same $\langle n \rangle$) is crucial for explaining the experiment. Since there is disparity in the chosen diameter distribution from one simulation run to another, we obtain a range of $\sigma_n/\sigma_1(I_{ARRAY})$ for the array SWNT FETs of size $\langle n \rangle$. Experimental data shown in Figure 2.8c falls within this range of $\sigma_n/\sigma_1(I_{ARRAY})$ and hence show excellent consistency with simulation. Similar to the analysis of I_{ARRAY}, our measurement of $\sigma_n/\sigma_1(g_{ARRAY})$ also reflects deviation from $1/\sqrt{\langle n \rangle}$ scaling, as shown in Figure 2.8e. This deviation can also be attributed to the wafer-level diameter distribution, as simulated in Figure 2.8f.

Note that our simulation of array-SWNT FET does not consider the effect of metallic-SWNTs in calculating the array-SWNT FET statistics; however, the measurements of array SWNT FETs have contribution from metallic-SWNTs and hence have much smaller ON/OFF ratio, as shown in Figure 2.1b. In spite of such differences, our statistical analysis nicely reflects the effect of statistical averaging in large $\langle n \rangle$ array SWNT FETs and the effect of variation in SWNT density and diameter distribution across the wafer. Inclusion of the effect of metallic-SWNTs should make the comparison between theory and experiment more meaningful, but will not change the essential features of array-SWNT FET statistics.

Since our theoretical analysis does not take into account the conduction through metallic SWNTs, we do not follow the same approach (as we used for analyzing I_{ARRAY} and g_{ARRAY}) for statistical analysis of two other array-SWNT FET parameters, namely

gate voltage at minimum drain current ($V_{G,min}$) and minimum drain current (I_{MIN}). Statistics of these parameters are mainly related to the statistics of metallic SWNTs within the array-SWNT FET and shows slight deviation from $1/\langle n \rangle$. Our ultimate effort in commercializing SWNT electronics is to eliminate the metallic SWNTs, hence we restrain ourselves from the statistical analysis of $V_{G,min}$ and I_{MIN}.

2.5 Conclusions

We examine the variation in on current, maximum transconductance and threshold voltage of single s-SWNT FETs and find that we can attribute the variation in on current and maximum transconductance to variation in diameter distributions of SWNTs. The variation in threshold voltage of single s-SWNT transistors may be more influenced by other extrinsic factors such as variation in interface defects or gate metal workfunction. Next, we study the extent of statistical averaging in reducing the device to device variations in array-SWNT FETs. We simulate the electrical parameters of array-SWNT FETs and hence compare it with measurements of similar parameters. We find that although there is smaller device to device variation as the number of SWNTs in array FETs increases, the decrease in device to device variation does not follow the expected $1/\sqrt{n}$ relation (according to central limit theorem) because of the non-uniformity of the density and diameter distributions across the wafer. Therefore, it is essential to control the uniformity of the density and diameter distributions of array-SWNT FETs to achieve devices with uniform electrical properties via well engineered processing, which is essential for large scale commercial use of such FETs. Clever circuit design is also another technique that has been suggested to help reduce the effects of variations in arrays of SWNTs. [12]

2.6 References

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2.7 Figures

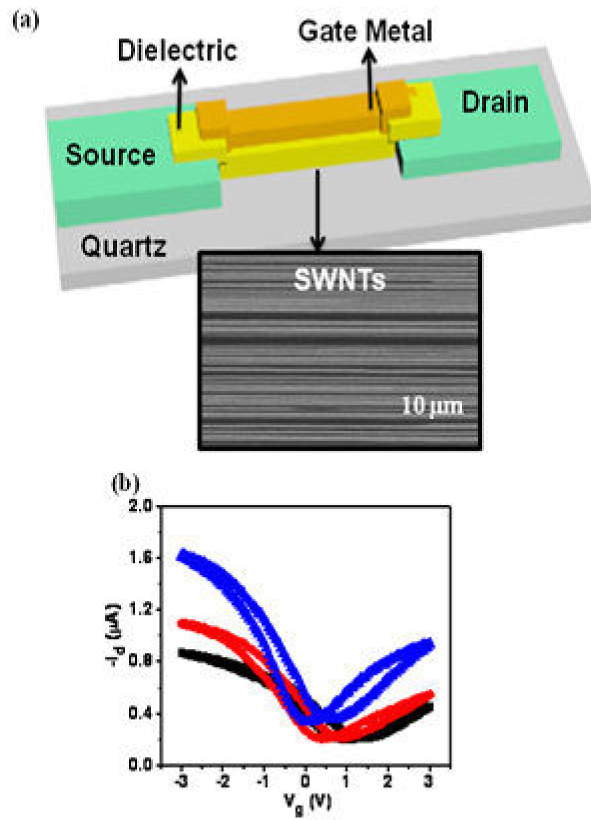

Figure 2.1: (a) Schematic illustration of a transistor based on single walled carbon nanotubes (SWNTs). A scanning electron microscope (SEM) image of the aligned arrays of SWNTs is shown below the illustration. (b) Transfer curves of array SWNT FETs with nominally 10 SWNTs.

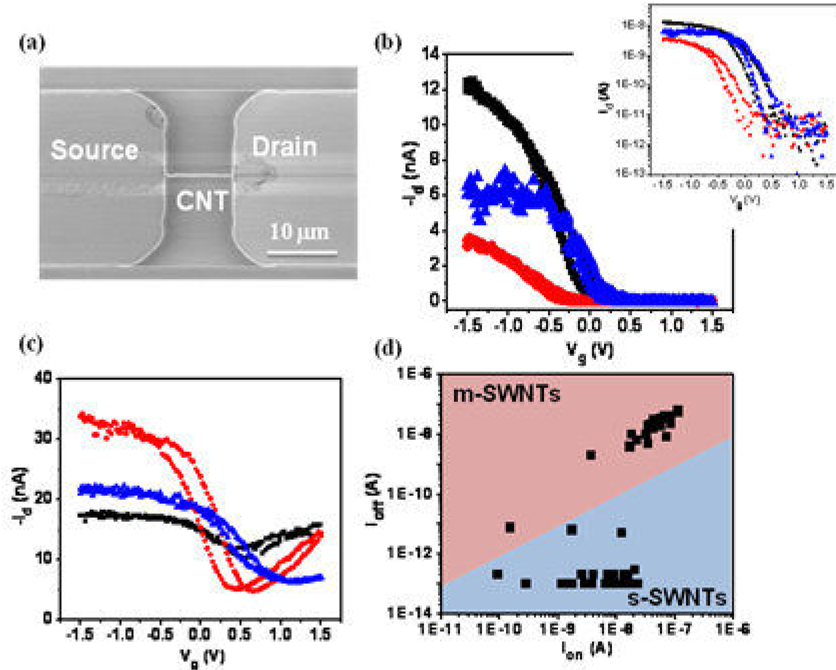

Figure 2.2: (a) SEM image of a single SWNT contacted to two metal electrodes (source and drain) on the left and right of the image. (b) Transfer curves of representative single semiconducting SWNT (s-SWNT) devices at V_{ds} = -0.05V. Inset shows the transfer curve in semilog-y scale. (c) Transfer curves of representative single metallic SWNT (m-SWNT) devices at V_{ds} = -0.05V. (d) Distribution of measured I_{on} and I_{off} of single SWNT devices. Symbols representing m-SWNTs are in the area shaded maroon with $I_{on}/I_{off} < 100$ and symbols representing s-SWNTs are in the area shaded blue with $I_{on}/I_{off} > 100$.

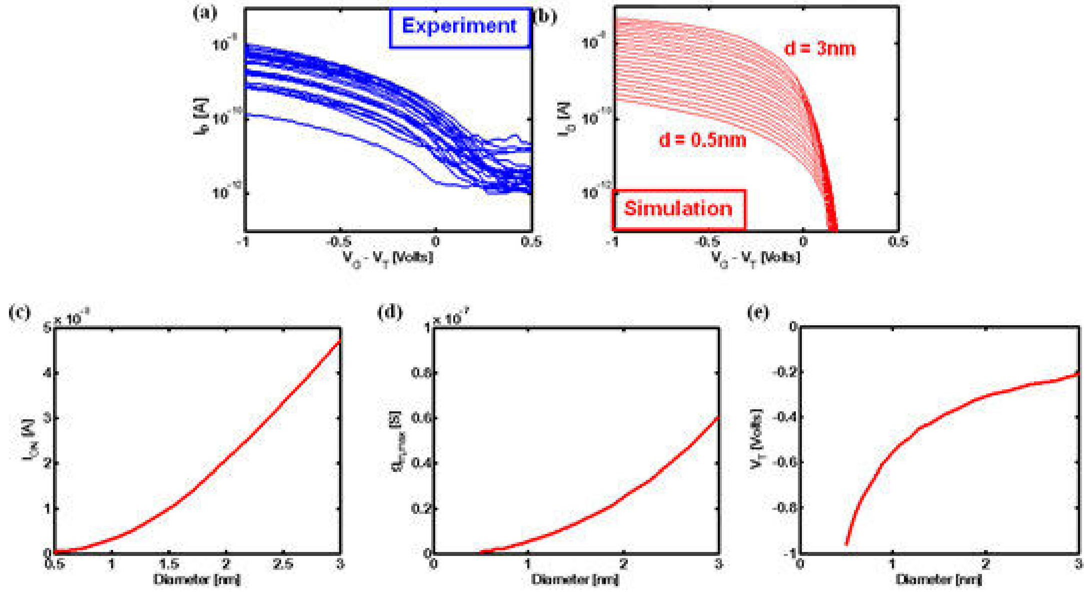

Figure 2.3: (a) Measured transfer characteristics of single s-SWNT transistors. (b) Simulated transfer curves of single s-SWNT transistors having a diameter range of 0.5nm and 3nm. (c) Drain current when V_G-V_T = -1V (I_{ON}) as a function of diameter for single s-SWNT transistors. I_{ON} increases super-linearly at smaller diameters and increases linearly at larger diameters. (d) Maximum transconductance ($g_{m,max}$) as a function of diameter for single s-SWNT transistors. $g_{m,max}$ increases non-linearly with diameter. (e) Threshold voltage (V_T) as a function of diameter for single s-SWNT transistors. V_T increases rapidly at smaller diameters and less rapidly at larger diameters. Here V_T is defined as the V_G at which I_D= $I_{ON,max}$/100.

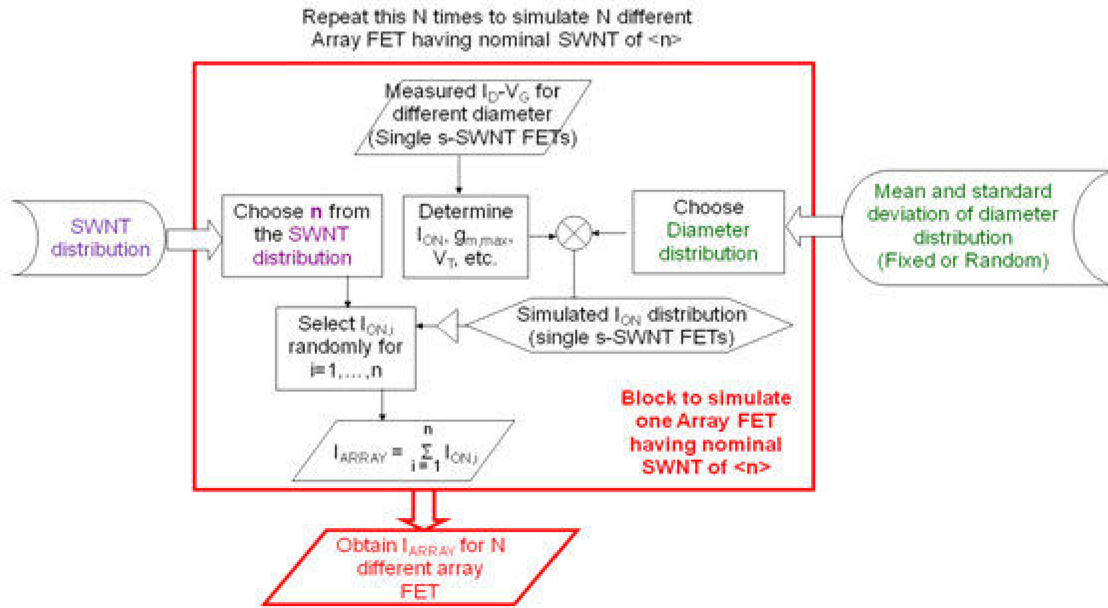

Figure 2.4: Flowchart for simulating ON current distribution for N different array SWNT FET having nominal SWNT of <n>.

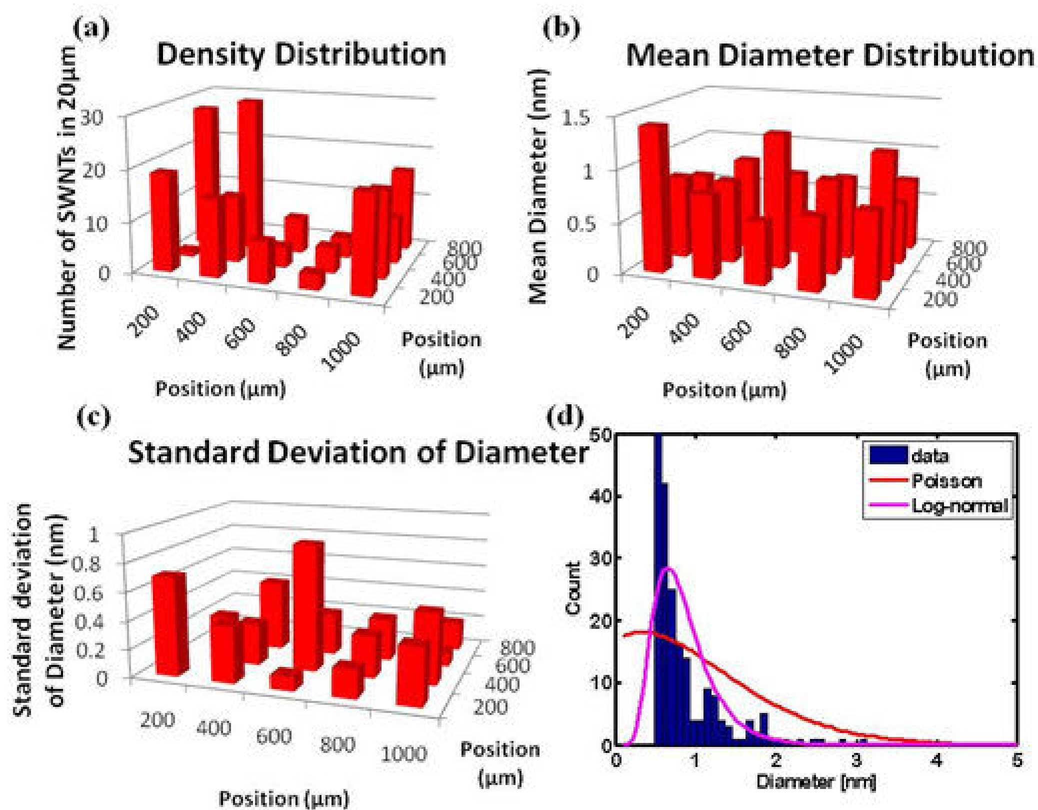

Figure 2.5: (a) Spatial distribution of the density of aligned arrays of SWNTs over an area of a substrate. Scanned area via AFM: 20µm (normal to the alignment direction of SWNT) X 1.25µm (parallel to the alignment direction of SWNT); Mean SWNT, <n> = 13. The x and y axes show the spatial locations where the distributions were measured. (b) Spatial distribution of the mean diameter of aligned arrays of SWNTs over an area of a substrate. Scanned area = 20x1.25µm. (c) Spatial distribution of the standard deviation of the diameter distribution of aligned arrays of SWNTs over an area of a substrate. Scanned area = 20x1.25µm. (d) A representative diameter distribution of SWNTs measured by AFM. The distribution is better fitted using a log-normal distribution (magenta line) compared to a Poisson distribution (red line).

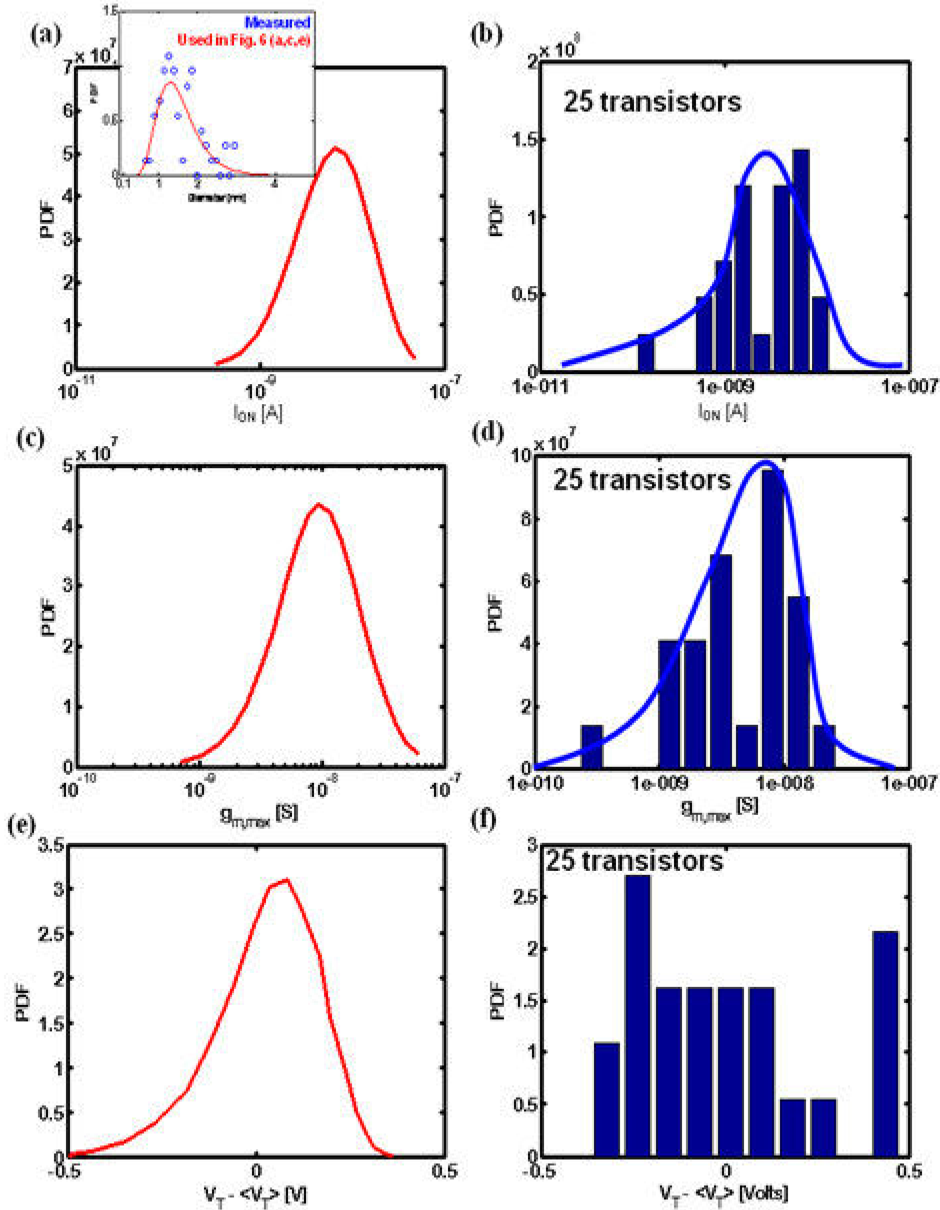

Figure 2.6: (a) Distribution of simulated I_{ON} for single s-SWNT transistors using the diameter distribution shown in the inset. (b) Distribution of measured I_{ON} for single s-SWNT transistors. Blue line acts as guide to the eye only. (c) Distribution of simulated $g_{m,max}$ for single s-SWNT transistors using the diameter distribution shown in the inset of Figure 2.6a. (d) Distribution of measured $g_{m,max}$ for single s-SWNT transistors. Blue line acts as guide to the eye. (e) Distribution of simulated V_T - $\langle V_T \rangle$ for single s-SWNT transistors using the diameter distribution in the inset of Figure 2.6a. (f) Distribution of measured V_T - $\langle V_T \rangle$ for single s-SWNT transistors. Here, $\langle V_T \rangle$ is the mean V_T of all the single s-SWNT transistors.

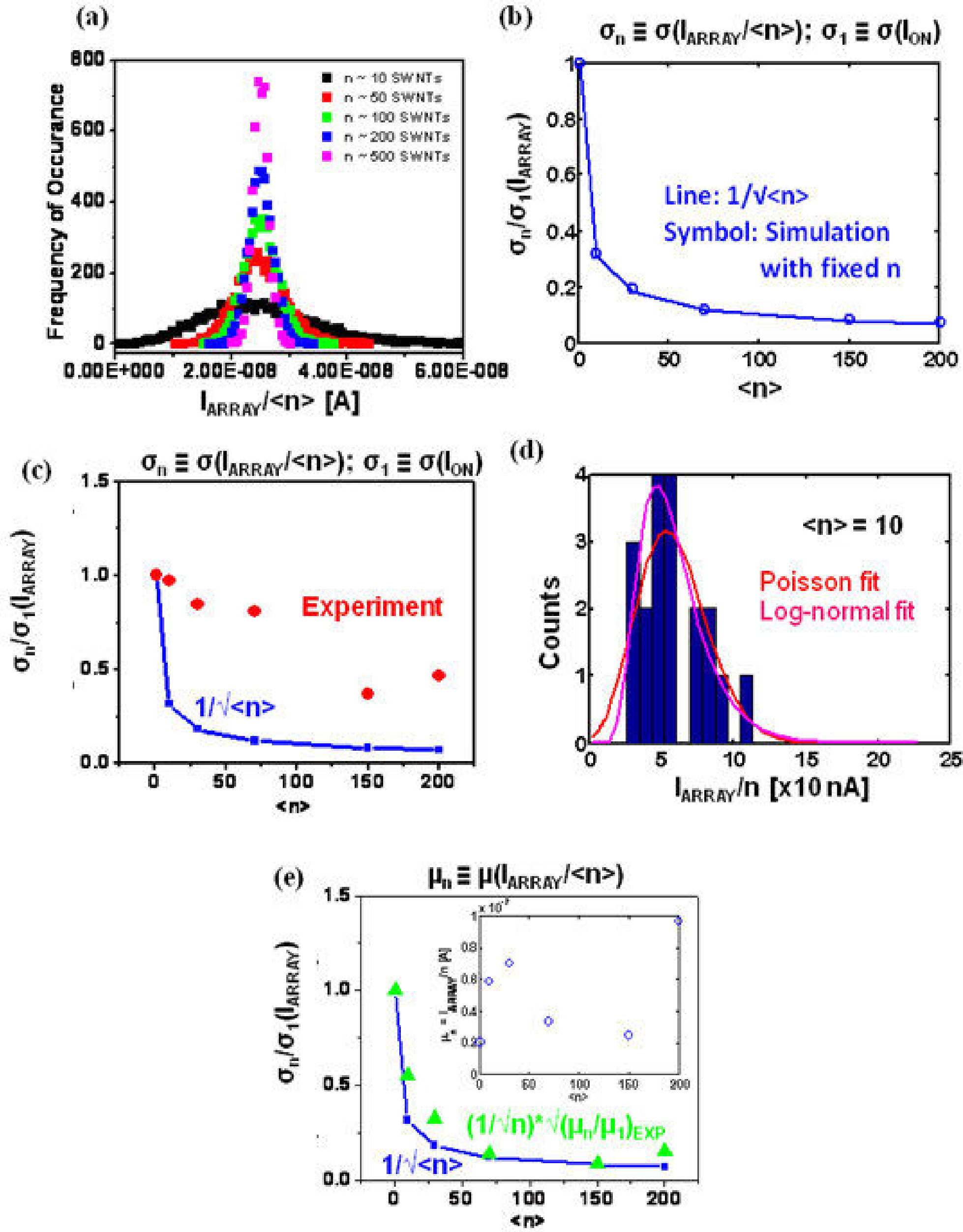

Figure 2.7: (a) Distribution of I_{ARRAY}/n at V_G-V_T = -1V in simulated array transistors (single SWNT FET of Figure 2.2 are used as basis), where there are n = 10, 50, 100, 200 and 500 SWNTs in the array FETs, represented by the black, red, green, blue and magenta symbols respectively. (b) Normalized standard deviation of I_{ARRAY}/n at V_G-V_T = -1V, $\sigma_n/\sigma_1(I_{ARRAY})$, as a function of n in the simulated array transistor. In the simulation,

Figure 2.7 (continued): n is fixed ($n = <n>$) for each of the array-SWNT FET. $\sigma_n/\sigma_1(I_{ARRAY})$ follows a $1/\sqrt{n}$ scaling, as expected in any statistical samples. Here, the transistors for any n are considered to have same I_{ARRAY}/n and $\sigma_n \equiv \sigma(I_{ARRAY}/n)$, $\sigma_1 \equiv \sigma(I_{ON})$. (c) $\sigma_n/\sigma_1(I_{ARRAY})$ of measured array transistors as a function of $<n>$. The experiment deviates significantly from the $1/\sqrt{n}$ relationship. Here, $\sigma_n \equiv \sigma(I_{ARRAY}/<n>)$ and $\sigma_1 \equiv \sigma(I_{ON})$. Therefore, for a particular n, the array-SWNT FET does not have same number of SWNT and diameter distribution, as assumed in this simulation. (d) Histogram of measured I_{ARRAY}/n for $<n> = 10$ (blue column bars). Measured distribution matches well with a Log-normal distribution (magenta line) than a Poisson distribution (red line). (e) There is significant deviation of mean I_{ARRAY}/n, $\mu(I_{ARRAY}/n)$, in our transistors (inset). We scale $1/\sqrt{n}$ (which is similar to the standard deviation of part b) using $\sqrt{(\mu_n/\mu_1)}$ (where, $\mu_n \equiv \mu(I_{ARRAY}/n)$ and $\mu_1 \equiv \mu(I_{ON})$) to capture the effect of mean I_{ARRAY} variation (green symbols). Here, we use the Poisson relationship of $\mu \sim \sigma^2$ for scaling the normalized standard deviation of part b. Consideration of disparity in mean I_{ON} causes deviation from the $1/\sqrt{n}$ relationship. However, such deviation from $1/\sqrt{n}$ is not comparable to the deviation observed in part c.

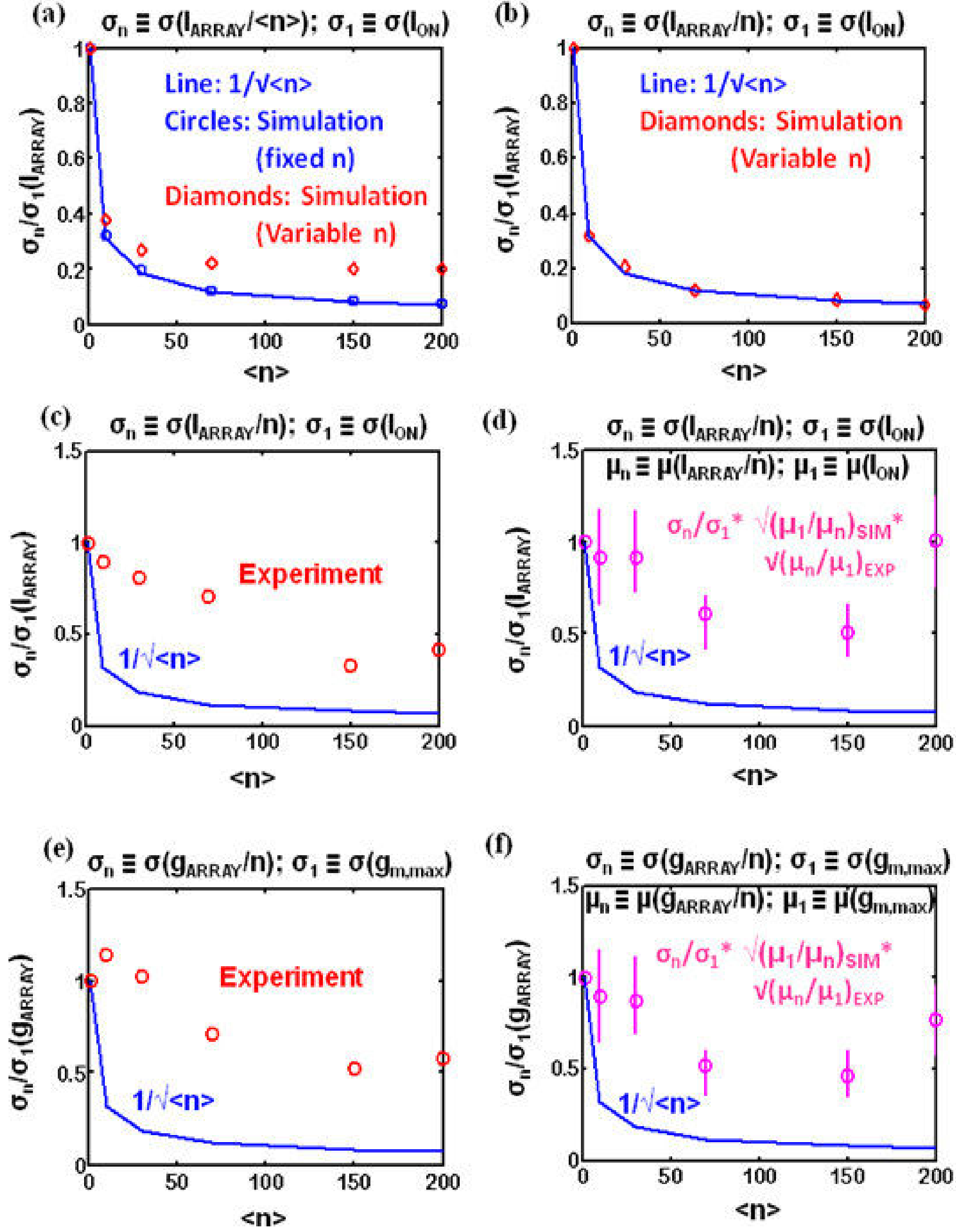

Figure 2.8: (a) $\sigma_n/\sigma_1(I_{ARRAY})$ of simulated array transistors as a function of <n>, where σ_n indicates the standard deviation of I_{ARRAY}/<n>. Blue square symbols consider no variation of n in array SWNT FET and is consistent with $1/\sqrt{n}$. Red diamond symbols

Figure 2.8 (continued): consider variation of n in array SWNT FET and deviates from $1/\sqrt{n}$. (b) $\sigma_n/\sigma_1(I_{ARRAY})$ of simulated array transistors as a function of $\langle n \rangle$, where σ_n indicates the standard deviation of I_{ARRAY}/n. Simulation results (red diamond symbols) are consistent with $1/\sqrt{n}$ (blue line), which suggests that the calculation of σ_n using I_{ARRAY}/n (rather than using $I_{ARRAY}/\langle n \rangle$, as in part a) can eliminate the effect of n variation in array SWNT FET. (c) $\sigma_n/\sigma_1(I_{ARRAY})$ of measured array transistors (red symbols) as a function of $\langle n \rangle$. Measurement still deviates from $1/\sqrt{n}$ relationship (blue line), even when the σ_n is calculate using I_{ARRAY}/n. (d) $\sigma_n/\sigma_1(I_{ARRAY})$ of simulated array SWNT FET (magenta symbols) as a function of $\langle n \rangle$. Simulation considers the effect of density distribution (like part b), wide range of diameter distribution (like Figure 2.5b,c), and μ_n variation (like the inset of Figure 2.7e) across the wafer. The $1/\sqrt{n}$ relation is also shown in blue. (e) Normalized standard deviation of the maximum transconductance (g_{ARRAY}) per SWNT of measured array transistors $\sigma_n/\sigma_1(g_{ARRAY})$ (where, σ_n is the standard deviation of g_{ARRAY}/n of array SWNT FET, and σ_1 is the standard deviation of $g_{m,max}$ for single SWNT FET) of measured array transistors (red symbols) as a function of $\langle n \rangle$. Measurement deviates from $1/\sqrt{n}$ relationship (blue line). (f) $\sigma_n/\sigma_1(g_{ARRAY})$ of simulated array SWNT FET (magenta symbols) as a function of $\langle n \rangle$. Simulation considers the effect of density distribution (like part b), wide range of diameter distribution (like Figure 2.5b,c), and μ_n variation (like the inset of Figure 2.7e) across the wafer. The $1/\sqrt{n}$ relation is also shown in blue.

CHAPTER 3:

INTRINSIC PERFORMANCE VARIABILITY IN ALIGNED-ARRAY CARBON NANOTUBE FIELD EFFECT TRANSISTORS

This chapter was accepted as "Intrinsic Performance Variability in Aligned-Array CNT Field Effect Transistors, S. Salamat, **X. Ho**, J.A. Rogers and M.A. Alam, *IEEE Transactions on Nanotechnology,* PP(99), 1 (2010)" Reproduced with permissions from the journal.

3.1 Introduction

As CNT-nanonet technology explores niche applications in micro [1-5] and macroelectronics [6-10], it is increasingly important to create transistors with nominally uniform characteristics as the basis for large scale circuit integration. Studies based on single tube CNFET have shown that among various transistor parameters, control of tube diameter is most critical, because diameter dictates bandgap and injection barriers, and these two parameters in turn dictate (exponentially) the I-V characteristics of a transistor [11]. The question is: Does diameter distribution play an equally important role in multi-tube transistors or does the self-averaging, over various tube diameters, obviate the problem? It is well known that in long channel nanonet transistors, the sensitivity of the I-V characteristics on tube diameter is suppressed as electrons percolate through an 'ensemble-averaged' network of tubes with various diameters [7,12]. In short channel aligned-array CNFETs, however, such "path-averaging" may be absent and distribution of CNT parameters (e.g., diameter, mobility, etc.) could be directly reflected in the I-V characteristics. In principle, therefore, short-channel directly-bridging CNFETs using similar device geometries could exhibit significant variation in the on current, especially for ultra-scaled transistors appropriate for high-frequency operation. While the role of the metal/nanotube contact and its effect on device performance for FET with single CNT has been studied by many groups [11, 13-16], the effect of diameter distribution (of CNT array) on FET performance parameters (e.g., I_{on}, V_T, R_d, and I_{on}/I_{off}), especially in the presence of metallic-CNTs, has not been considered. In this paper, we use measured

diameter distribution and transistor characteristics along with systematic theoretical simulations to demonstrate that, of all the parameters, intrinsic process-induced diameter distribution would continue to play a dominant role in dictating the performance of short channel CNT transistors, even if the channel length was scaled to the ballistic limit. Given typical diameter distribution, we find that (i) only a fraction of the tubes carry most of the current (i.e., larger diameter nanotubes, despite being relatively small percentage of the total number of tubes, carry a significant amount of current [d_{CNT}~$1/E_g$]) and (ii) depending on the contact material (source/drain), a fraction of the semiconducting tubes behave essentially like metallic tubes (from Off-state to On-state) and must be removed for good I_{on}/I_{off} ratio.

3.2 Fabrication of Nanotube Arrays and Devices

As shown in the Fig. 3.1, the thin-film transistors (TFTs) used in this study are based on perfectly aligned parallel array of single walled carbon nanotubes (SWNTs) as the channel material. The SWNTs were grown directly into such configuration via chemical vapor deposition (CVD) on a specially prepared quartz substrate, using the procedures described in our earlier work [17]. The devices studied here used Palladium (Pd) for source and drain electrodes. Layers of hafnium oxide (HfO_2) deposited on top of the resulting structure formed the gate dielectric (94±7 nm). Gold (Au) was used as the gate electrode. The gate was aligned to the channel and it overlapped significantly with both the source and the drain (by ~20 μ m). To study the transport characteristics, we fabricated 6 samples for each channel length of 3, 4, 5 and 8 μm (a total of 24 devices). The widths (W) of all the transistors were kept constant at 400 μ m.

Fig. 3.2 shows typical transfer curves of one sample of each channel length. Consistent with the previous reports [14], these Pd contacted devices exhibited predominantly p-type characteristics.

Remarkably, however, even though all the devices were processed in parallel and used the same metallization scheme, Fig. 3.3 shows that even for samples with the same channel length, the devices exhibited significant variations in the I_{on}, V_T and R_d. Here, I_{on}

is defined as drain current (I_d) at maximum applied gate bias (V_g) of -0.8V, V_T is defined as the gate bias (V_g) at which I_d is minimum [18] (This definition is different from that of MOSFET, wherein V_T is traditionally defined by taking the point of maximum slope on I_d-V_g curve (or linear transconductance) and V_T is extracted by the intercept of the tangent through the point [19]), and R_d is the device resistance given by $R_d=V_{ds}/I_{on}$ and it includes the resistance of semiconducting as well as metallic tubes. Given that the ratio of metallic-CNTs (m-CNTs) to semiconducting-CNTs (s-CNTs) is ~1:2, we associate I_{off} with transport through m-CNTs, and the difference of I_{on} and I_{off} with transport through semiconducting tubes. The average resistance of each semiconducting tube can be calculated as $R_s = N_s x V_{ds}/(I_{on}-I_{off})$ where N_s is the number of semiconducting tubes per device (determined from the density measurements of CNTs making up the transistor) and V_{ds} is the applied drain bias.

Figs. 3.3a and b summarize the observed fluctuations in the average resistance of semiconducting tubes for various channel lengths, measured at threshold and in saturation. These variations were present for all channel lengths (3, 4, 5 and 8 μ m), and were particularly large around V_T (Fig. 3.3a).

These results immediately bring into focus a number of issues regarding the variability in transistors' performance. It is conceivable that at longer channel lengths, extrinsic factors like mobility fluctuation, variability in the number of tubes able to bridge the source and the drain, length dependent scaling of defects along the tube, etc. can potentially increase device-to-device fluctuation. However, as the devices are scaled down to 3μm or less, surprisingly the *relative* fluctuation in resistance remains almost independent of channel length (see Fig. 3.6), suggesting the possibility that this fluctuation may not be averaged out even at ultra-scaled, quasi-ballistic channel lengths (< 300nm) [14] relevant for high-speed electronic applications. While fluctuation at the longer channel lengths may be amplified by extrinsic variability, there appears to be an irreducible intrinsic variability present in all array-based CNT transistors.

The discussion above leads one to the hypothesis that the distribution of diameters of CNTs may be the source of this variability and may play a more important role than is

commonly appreciated. To verify this proposition, we first measured the diameter distributions of as grown CVD SWNTs (before defining channel lengths and depositing gate dielectric) of four different samples using AFM (see Fig. 3.4). The diameters of CNTs were determined by measuring the height difference between top of CNT and substrate next to it (quartz) and approximately 600 measurements were taken to reduce statistical error. Fig. 2.4 shows that some of the CNTs have diameter ~0.4nm. These very low values may reflect the resolution limit of our AFM setup. Nonetheless, the fraction of such tubes ($d_{CNT} \leqslant$ 0.4nm) is very small and given their large E_g, these CNTs would have very little effect on device characteristics (I_{on}, R_d etc). Also noted in the Fig. 2.4 is that CVD grown tubes exhibit a wide range of diameter distribution that cannot be represented by a simple distribution function, let alone by an average value [20]. In general, the exact shape of the diameter distribution would depend on the CNT growth technique and device processing details. For typical ranges of diameter distributions, the spread in transistors' characteristics can be significant – as discussed below.

3.3 Modeling of the Effect of Diameter Distribution on I-V Characteristics

Although I-V characteristics of CNFETs resemble that of a conventional MOSFET, however, the underlying physics of the two transistors is very different. Contacts in the conventional MOSFET are ohmic, but owing to the difficulty in making an ohmic contact in CNFETs, the transport through CNFETs is thought to be dominated by SB at the (contact) metal/CNT interface [1,15,21-23]. For short channel CNFETs, experiments have shown that the metal-CNT contacts limit the current flow through CNT and determine the electrical characteristics of the device [21]. The SB at metal/CNT interface, however, is a function of the metal work function and CNT diameter (or, equivalently E_g). If the metal work function is fixed, the diameter of CNT dictates the nature of the contact, i.e., Schottky barrier or ohmic. In essence, if metal-CNT combination is such that the metal Fermi level contacts CNT inside the valence band (or conduction band), the contact will be ohmic; alternatively if the metal Fermi level contacts CNT inside the bandgap, the contact will be SB. Many researchers have shown Pd to make an excellent ohmic contact with carbon nanotubes [14,24]. Since our devices

have aligned network of CNTs with wide range of diameter distribution, *some of the CNTs are likely to form SB while remaining will make ohmic contact*.

The electronics structure of SWNTs strongly depends on their diameter and chirality [25]. The work function of SWNTs (Φ_{CNT}) would therefore, be differentdepending on the structure of CNT. Many studies have been conducted on the work functions of SWNTs [26,27] and the values reported vary slightly depending on the method used for measurement. We used work function for nanotube Φ_{CNT} = 4.7eV [28]. Since the bandgap (E_g) of CNT depends on the reciprocal of CNT diameter (d_{CNT}) [29,30] , we calculated the E_g for each CNT using the relationship [31]

$$E_g = 2|t|a_{c-c} / d_{CNT}. \quad (1)$$

An overlap integral value of |t|=2.7eV is used in this study [29,31], and with carbon to carbon bond length a_{c-c}=0.144nm, the above expression simplifies to

$$E_g = 0.78\text{eV} / d_{CNT}. \quad (2)$$

With Φ_{CNT} = 4.7eV and Φ_{Pd} = 5.1eV [11,14], the barrier for holes (Φ_P) is calculated using analytical expression

$$\Phi_P = (\Phi_{CNT} + E_g/2) - \Phi_m \quad (3)$$

This relationship suggests that there would be no hole barrier (i.e., Φ_P=0) for CNTs with diameter equal to 1nm; $d_{CNT} \sim 1.0$nm (E_g = 0.8eV) and there would be a positive SB (Φ_P) for holes for all nanotubes with diameters less than 1nm; $d_{CNT} < 1.0$nm ($E_g >$ 0.8eV±3kT). As seen in Fig. 3.4, in our devices there are many CNTs with diameter smaller than 1nm. Hence, the transport in these CNTs will be dominated by SB. For all the CNT with diameter larger than 1nm; $d_{CNT} > 1.0$nm ($E_g <$ 0.8eV±3kT), there is no barrier for holes and metal/CNT contact will essentially be ohmic.

Given the barrier for holes (and electrons), metal and CNT work functions and other parameters (drain/gate bias, oxide thickness, etc.), we can now calculate the current through the transistor using self-consistent numerical simulations [32]. As discussed previously, in order to isolate the *intrinsic* effect of diameter distribution from other *extrinsic* effects, like charge trapping and mobility variation, (that might add to the drain current fluctuation in long channel transistors), we focus on ballistic transport in very

short channel transistor (100 nm) that is exclusively affected by contact metal and the diameter distribution of the tubes. Briefly, our numerical simulations involve solution of quantum transport equations (the standard NEGF formulation) self-consistently with Poisson equation. Details of the simulation model have been discussed elsewhere [33].

Due to nearly ballistic nature of transport in short channel CNFETs [14], the transistor performance is dictated by the SBs at the metal/nanotube interface and the s-CNTs resistance (R_s) can be approximated by the contact resistance (R_c). For the long channel lengths (3, 4, 5, and 8 μm), where transport is scattering dominated and is also affected by extrinsic factors, we calculate the total resistance R_s by using the expression; $R_s = R_c + \rho L_c$, where R_c is the ballistic contact resistance, ρ is the resistivity of semiconducting tubes (determined from the slope of the experimental measurements of R_s-vs-L_c), and L_c is the channel length (3, 4, 5 or 8μm). Figs. 3.5a&b show that large variations in the resistance R_s are expected from the intrinsic variation in the diameter distribution - and these variations are comparable to those observed in the experiments [see Figs. 3.3a&b]. Figs. 3.6a&b, on the other hand, show the comparison of simulation result and experimental values of normalized resistances R_s (normalized with respect to averages). Black lines in the plot show the expected variability in Rs, as obtained from simulations, whereas the red circles show the measured experimental variations (measured at threshold and in saturation). The experimental variability is found within the extents of the intrinsic variation limits established by simulation results. Obviously, as discussed above, there are additional sources of extrinsic variability at longer channel devices.

Noting the simulation results of Fig. 3.5 and Fig. 3.6 and comparing with the observed experimental variations (Fig. 3.3), we conclude that even for long channel transistors – where other extrinsic effects like increase in defect density, charge trapping etc. may play a significant role – the effect of diameter distribution is still significant. And therefore a key conclusion of this paper is that unless the diameter distribution of the semiconducting tube is controlled, large scale integration of the transistors based on this technology would be difficult.

Apart from fluctuation in the drain-current, Fig. 3.7 demonstrates another important consequence of the diameter distribution in ultra-scaled quasi-ballistic CNFET transistors that in aligned array CNFETs, only a small fraction of the semiconducting CNTs with diameter 1.0nm<d_{CNT}<2.2nm is capable of giving a good Ion/Ioff ratio, and the rest must be eliminated for good transistors' performance. For d>2.2 nm, the Ion/Ioff ratio is poor for the following reason: The metal Fermi level contacts large-diameter CNTs deep inside the valance band and the channel conductance (from off-state to on-state) changes very little with gate bias. Therefore, even though these large diameter (small E_g) tubes carry significant amount of on current, there is essentially no SB available to suppress the current during off-state. Such tubes therefore have poor Ion/Ioff ratio that is not appropriate for digital logic operation. On the other hand for very small diameter tubes with d_{CNT}<1.0nm, the barrier-height is too large for any significant contribution to the on current and the off current. These tubes are essentially electrically inactive and while they contribute to physical density, their contribution to electrical performance is negligible.

In fact, for the given diameter distribution shown in Fig. 3.4, only ~40% of s-CNTs carry most of the current through the device and ~60% carry insignificant current due to large bandgap (or Schottky barrier). Of these 40% s-CNTs with high on-state current, ~50% have Ion/Ioff ⩾ 500, while the bandgap of the remaining tubes are too small to be turned off effectively. Therefore, the performance of the device is dictated by ~20% of the total s-CNTs that have substantial current and good on/off ratio (Ion/Ioff⩾500). On the other hand, if the Ion/Ioff~200 is sufficient for specific applications, the percentage of performance determining s-CNTs rises to ~30%. Since 2 out of 3 SWNTs are semiconducting, therefore, eventually only about 15-20% of the tubes that have good on/off ratio, are useful for directly bridging transistors. *In sum, increasing tube density without corresponding control over the diameter distribution may cause unacceptable level of fluctuation in on current and threshold voltage, as well as poor on/off ratio.*

While the conclusion above is based on CNFETs with Pd as source/drain contact material, we have also fabricated transistors with gold (Au) metallization scheme. These

Au contacted CNFETs exhibited ambipolar characteristics, contrary to P-type behavior of Pd contacted devices. The detailed analysis of these Au contacted transistors is underway and will be published elsewhere; however, the fluctuations in the devices' characteristics, having similar channel lengths and operating under similar conditions, are quite similar and can be understood in the same theoretical framework.

3.4 Conclusion

Our analysis of the effects of diameter distribution on the performance of aligned array CNT transistors shows that the control over diameter distribution is critically important process parameter for attaining high performance transistors and circuits with characteristics rivaling those of state-of-the art Si technology. Aligned network CNFETs are desirable to gain higher drive current, large active areas and to resolve inherent 'impedance mismatch' problems for high frequency applications (quantum of resistance~25kΩ, typical of nanodevices and characteristics impedance of free space ~377Ω) [34,35]. Of late, p-type and n-type single and aligned network nanotube FETs have been fabricated and logic gates have been demonstrated [36-38], therefore, reproducibility in device current becomes essential before such applications are realized and promising results are achieved. Can the diameter distribution of CNTs be easily controlled? Of the various techniques to control diameter distribution discussed in the literature, pre-sorting by density differentiation seems effective in producing tubes of diameter 1.2-1.6 nm [39]. Fig. 3.7 suggests that the ideal diameter distribution for high on current and on/off ratio should be confined to 1.2-2.1 nm; however, tubes of 1.2-1.6 nm diameter would give reasonable performance as well. Since it is difficult to align solution-processed nanotubes for high performance transistor applications, the integration of presorted tubes for use in the aligned arrays remains an open problem. Perhaps the most effective route of controlling diameter for aligned array CNFETs would come within the CVD process where the initial size-distribution of the catalysts are controlled by self-assembly technique. The problem of device-to-device fluctuation could also be addressed if long tubes are shared among various transistors, so that regardless the diameter distribution, their device-to-device fluctuation is eliminated. This approach

would restrict transistor layout, however such layout rules are now routine in silicon ICs [40] and have been found not to have significant effect on transistors' performance or area-penalty.

3.5 References

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3.6 Figures

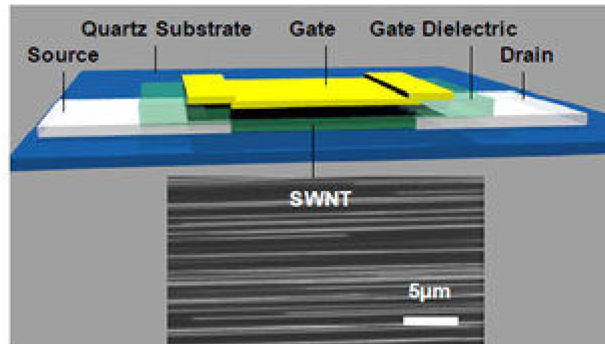

Figure 3.1. Schematic illustration of thin-film transistor (TFT) with perfectly aligned parallel array of SWNTs. Lower portion of the figure shows the scanning electron micrograph of a representative CNT array.

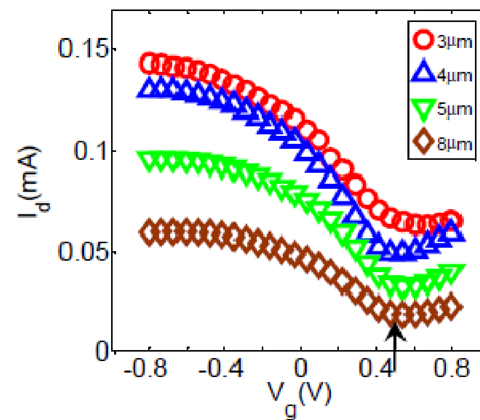

Figure 3.2. Transfer curves of devices for channel lengths of 3, 4, 5 and 8µm. Measurements were taken with the source grounded and the drain held at a bias of -0.01 V. Gate bias was swept between ±0.8V. Upward arrow on the bottom curve (corresponding to channel length of 8 µm) indicates V_T of this device.

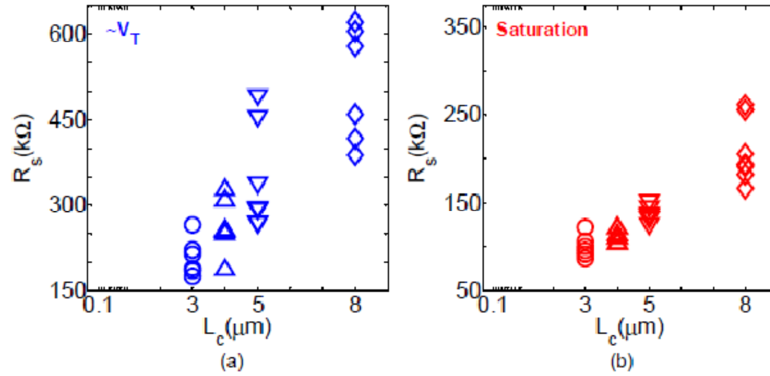

Figure 3.3. (a) Resistance variations in the the semiconducting tubes measured at threshold voltage. (b) Resistance variations in the semiconducting tubes measured in saturation. All the devices had same contact material and the applied biases (gate/drain). Nonetheless, significant variations in resistance Rs were present for all channel lengths and were particularly large near V_T.

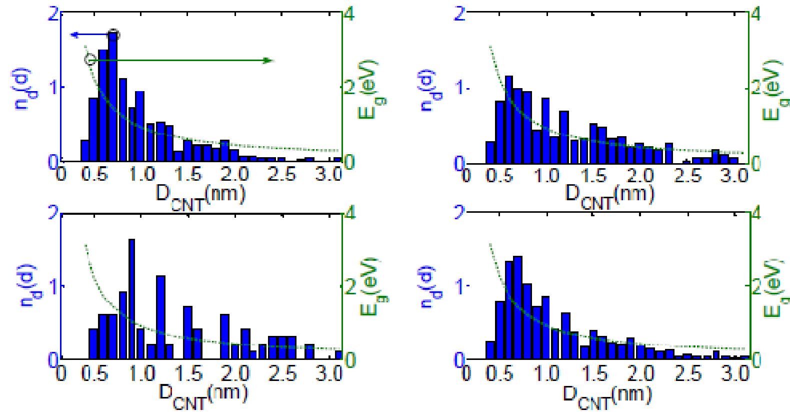

Figure 3.4. Normalized diameter distributions for four samples. These measurements correspond to different thin film transistors that use perfectly aligned array of single-wall carbon nanotubes for the channel. The measurements were taken using AFM, on as grown CVD tubes before defining the channel lengths and depositing the gate dielectric. We determined the diameter by measuring the height difference between the top of the CNT and the area just next to the CNT (i.e., quartz). The number of tubes on each device were different so the data has been normalized to highlight the general shape of diameter distribution in the CNFETs.

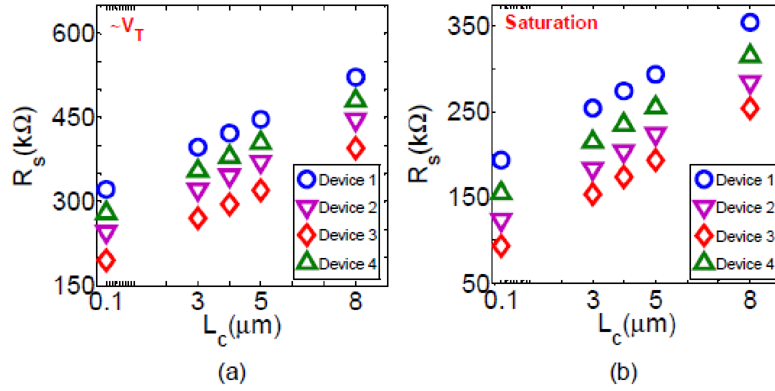

Figure 3.5. Simulation results for resistance variations resulting from diameter distributions of CNTs (in the aligned array CNFETs) for the four devices are shown above. (a) Resistance variations at threshold voltage. (b) Resistance variations in saturation. Resistance of CNT is calculated as R=Rc + ρ Lc, where Rc is contact resistance of CNT (calculated assuming the ballistic transport with the given Schottky barrier height) and ρ is the resistivity of the CNT, extracted from the slope of Rs-vs-Lc measurements and Lc is the channel length.

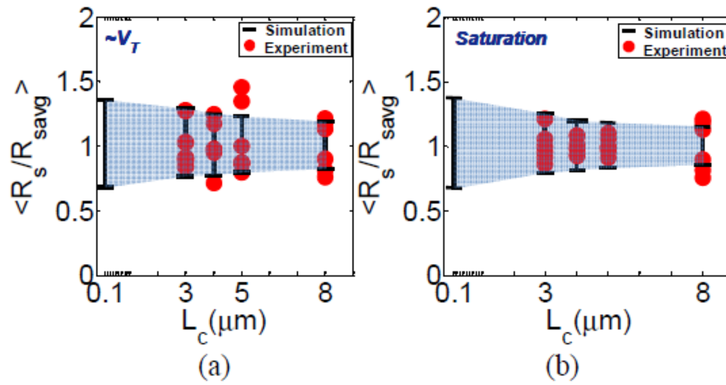

Figure 3.6. Normalized Rs variability observed in simulations and experiments (a) Rs variability at threshold voltage. (b) Rs variability in saturation. Rs has been normalized with respect to average. Lines (black) shows the spread of normalized Rs and dots (red) show the experimental values. As seen in the figure, most of the experimental data falls within the extents of simulations (supposed to be originating from diameter distribution).

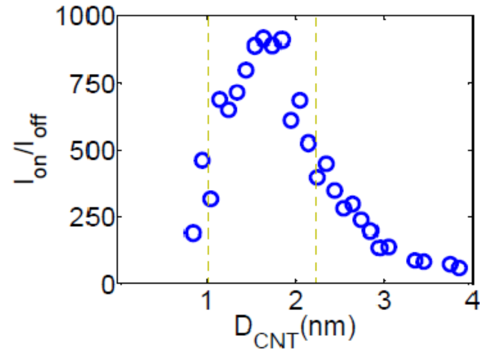

Figure 3.7. Simulation results for the Ion/Ioff as function of diameter of CNTs. Maximum Ion/Ioff is only ~1000, due to small drain bias Vds = -0.01V, in these simulations (Ion is drain current corresponding to the gate bias of -0.8V).

CHAPTER 4

SCALING PROPERTIES IN TRANSISTORS THAT USE ALIGNED ARRAYS OF SINGLE WALLED CARBON NANOTUBES

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4.1 Introduction

Submonolayer aligned arrays or random networks of single walled carbon nanotubes (SWNTs) represent attractive semiconductor materials for effective, thin film type transistors (TFTs) [1] partly because the mobilities of individual SWNTs have been shown to be up to 10,000 cm2/Vs, [2] and possibly higher, significantly exceeding that of silicon. Arrays or networks of SWNTs provide a scalable way to exploit these properties, as well as their excellent mechanical and thermal characteristics. In the case of long channel TFTs that use networks of SWNTs, scaling studies show clearly that the device operation is based on field modulation of the properties of the channel; the role of the contacts is experimentally negligible for channel lengths that are large compared to the average lengths of the SWNTs. Attractive device-level properties that can be obtained with networks create interest in their use as alternatives to other thin film materials for flexible electronics [3], flat panel electronics and related systems. Arrays provide much better performance than networks, thereby creating opportunities in analog electronics [4,5] and other areas where the requirements can be demanding. In the case of arrays, it is known that the contacts can greatly influence device operation [1,4,6-8], just as with transistor test structures based on individual SWNTs [9-11]. In the present paper, we study the dependence of device parameters in array based transistors on channel length in the micron range, for cases where the source and drain electrodes consist of Pd and Au. The results indicate that, for arrays with a range of diameters centered at ~1.2 nm, the contacts contribute significant, but largely gate-independent resistance in the case of Pd

and gate dependent behavior in the case of Au. The results provide key insights into the behavior of the devices, the scaling of their properties and directions for future work.

4.2 Methods

Figure 4.1a shows a schematic illustration of a TFT that uses a 'perfectly' aligned parallel array of single walled carbon nanotubes (SWNTs) for the semiconductor and a scanning electron microscope (SEM) image of an array representative of the type used here. The SWNTs were grown directly into such configurations via chemical vapor deposition (CVD) on an ST (stable temperature) cut quartz substrate, using procedures described elsewhere. [12] The devices studied here used two different metallization schemes for the source and drain electrodes, both defined by photolithography and liftoff directly on the arrays. In one case, the metal was Pd (30 nm) / Ti (1 nm); in the other it was Au (30 nm)/ Ti (1 nm). Layers of hafnium oxide (HfO2) deposited on top of the resulting structures formed the gate dielectrics (94±7 nm in the case of Pd/Ti; 128±3 nm in the case of Au/Ti). Gate electrodes (Au (30 nm)/ Ti (2 nm)) aligned to the channels, but significantly overlapping (by ~20 μm) both the source and drain, were defined by photolithography and liftoff to complete the devices.

4.3 Results and Discussions

Figure 4.1d and 4.1e show typical transfer curves of devices with Pd and Au electrodes, respectively, measured with the source grounded, the drain held at a bias of -0.01 V, and the gate bias swept between ±0.8V. The Pd devices display predominantly p-type behavior while the Au transistors show ambipolar characteristics, both with only small levels of hysteresis. This outcome is consistent with the lower work function of Au and reduced barrier for electron injection, compared to Pd. The densities of the arrays (measured in tubes per micron of lateral distance across the channel) were 4±0.5 SWNTs/μm for Pd and 2±0.5 SWNTs/μm for Au, as determined by the average of SEM measurements at various spots across the surface of the substrate. Figure 4.1b shows a typical diameter distribution of the SWNTs. The diameters are critically important to the behavior of the devices, as the bandgaps of the SWNTs and their mobilities depend strongly on this parameter [2,13]. Also, experimental studies of test structures that use

individual SWNTs indicate that Schottky barriers at the contacts and threshold behavior vary strongly with diameter [11]. Statistical averaging associated with the arrays reduces but does not eliminate variability in device properties associated with slightly different diameter distributions of the incorporated SWNTs, as confirmed by theoretical studies on arrays with different diameter distributions [14]. To minimize the influence of such effects, we separately analyzed collections of devices that exhibited minimum current outputs at similar gate voltages, such as those presented in Fig. 4.1d and 4.1e, as a proxy for similar diameter distributions and contact properties. This procedure also, at the same time, removes device to device variations that can be caused by other effects, such as different amounts of residual charge in or near the channel. Figure 4.1f and 4.1g plot the combinations of channel lengths and gate voltages at minimum current, for Pd and Au devices respectively. The devices that form the focus of the results presented in the following are highlighted in red, where the minimum current voltage for the Pd and Au devices are ~0.43 V and ~0.13 V, respectively. Separate analysis was also performed on two other clusters of devices, as highlighted in blue and green in Fig. 4.1f and 4.1g. Summaries of results for analysis of these collections of devices, which we will refer to as blue and green clusters of devices, are also provided. In all of the following, we assume that the ratio of m-SWNTs to s-SWNTs is 1:2 and that ~80% of all of these SWNTs bridge the source and drain [4].

We analyzed the behavior using a simple equivalent circuit model, as shown in Fig. 4.1c, in which we assume diffusive transport in the channel. We refer to the number of semiconducting (s-SWNT) and metallic (m-SWNT) tubes bridging the source and drain as N_s and N_m. The resistance of a given tube, with index i, is $R_s^{(i)}$ and $R_m^{(i)}$, for a s-SWNT and a m-SWNT, respectively. As measured in the TFT structure, the resistance of each SWNT has two components: (i) a contact resistance ($R_{c,s}^{(i)}$ and $R_{c,m}^{(i)}$ for a s-SWNT and a m-SWNT, respectively) at the source and the drain electrodes and (ii) a channel resistance determined by the product of the channel length, L_c, and the resistivity (i.e. resistance per unit length), $\rho_s^{(i)}$ and $\rho_m^{(i)}$, of a s-SWNT and a m-SWNT respectively. The resistances of the transport pathways associated with each of the tubes add in parallel, due to the array geometry. The total resistance of the TFT device (R_{tot}), then, can be

written as the following, where the dependencies on gate voltage (V_g) are indicated explicitly:

$$\frac{1}{R_{tot}(V_g)} = \sum_{i=1}^{N_s} \frac{1}{R_s^{(i)}(V_g)} + \sum_{i=1}^{N_m} \frac{1}{R_m^{(i)}} = N_s \overline{G}_s(V_g) + N_m \overline{G}_m \quad (1)$$

The quantities $\overline{G}_s(V_g)$ and $\overline{G}_m$ are the average conductances associated with the s-SWNTs and m-SWNTs and their contacts to the source/drain electrodes, respectively, with

$$R_m^{(i)} = \frac{1}{G_m^{(i)}} = R_{c,m}^{(i)} + \rho_m^{(i)} L_c = \frac{1}{G_{c,m}^{(i)}} + \frac{L_c}{\sigma_m^{(i)}} \quad (2)$$

and

$$R_s^{(i)}(V_g) = \frac{1}{G_s^{(i)}(V_g)} = R_{c,s}^{(i)}(V_g) + \rho_s^{(i)}(V_g) L_c = \frac{1}{G_{c,s}^{(i)}(V_g)} + \frac{L_c}{\sigma_s^{(i)}(V_g)} \quad (3)$$

Where the G values are the corresponding conductances and σ are the conductivities. As indicated in these equations, the analysis assumes that only $\rho_m^{(i)}$ and $R_{c,m}^{(i)}$ are independent of V_g. We note, however, that it is well known that even nominally m-SWNTs can often be modulated by an applied field, due possibly to defects or other non-ideal aspects [15].

Using these expressions, intrinsic properties can be extracted from the electrical properties and their dependence on L_c. First, we associate the minimum current (I_{off}) extracted from the transfer curves with transport, approximately, through the m-SWNTs. We refer to the resistance at this minimum as the off-state resistance, R_{off}. Using Ohm's law, we can write:

$$\frac{1}{R_{off}} = \frac{I_{off}}{V_d} = \sum_{i=1}^{N_m} \frac{1}{R_m^{(i)}} = N_m \overline{G}_m \quad (4)$$

where V_d is the drain bias (-0.01 V). Next, we associate the difference between current measured at a given V_g, $I_{on}(V_g)$ and I_{off}, which we refer to as $I_{on\text{-}off}$, with transport through the s-SWNT. Again, using Ohm's law,

$$\frac{1}{R_{on-off}} = \frac{I_{on-off}}{V_d} = \sum_{i=1}^{N_s} \frac{1}{R_s^{(i)}(V_g)} = N_s \overline{G}_s\left(V_g\right) \qquad (5)$$

Figure 4.2a and 4.2b show the dependence of $1/\overline{G}_s\left(V_g\right)$ and $1/\overline{G}_m$ of transistors with palladium electrodes on L_c, respectively. The extracted $\frac{1}{\overline{G}_{c,m}}$ for the m-SWNTs is small, ~20 ± 5 kΩ, comparable to values from earlier reports (~14 kΩ) [16,17] and between values obtained from analysis of the blue (not fitted to a finite value within statistical accuracy) and green (~56 kΩ) clusters of Pd devices. The extracted value of 1/ $\overline{\sigma_m}$ is 24 ± 5 kΩ/μm, which lies between previous reports of devices of this type (~80 kΩ/μm),[4] and values reported for individual tube devices (~6 kΩ/μm) [18,19]. Likewise, $1/\overline{\sigma_m}$ from similar analysis on the different clusters of devices are also in this range (~45 kΩ/μm for blue; ~20 kΩ/μm for green). According to Eq. (3), linear fits to the data 1/ $\overline{G}_s\left(V_g\right)$ vs L_c yield the inverse of the average conductances of the contacts from the intercepts and the inverse of the average conductivities from the slopes. Figure 4.2c and 4.2d plot the dependence of $1/\overline{G}_{c,s}$ and $1/\overline{\sigma_s}$, as a function of V_g, respectively. The results show that $1/\overline{G}_{c,s}$ is ~50 ± 20 kΩ, with no significant dependence on V_g, to within experimental uncertainties. This result is quantitatively similar to previous studies of individual tube devices with similar diameters and metallization (~32 kΩ) [20]. Analysis of blue and green Pd devices yields $1/\overline{G}_{c,s}$ values of ~0 ± 10 kΩ and ~50 ± 20 kΩ, respectively. In neither case is the contact resistance significantly modulated by V_g.

The data of Fig. 3.2d show clearly that $1/\overline{\sigma_s}$ is modulated strongly by V_g. This dependence can be used to extract the average intrinsic mobility, $\overline{\mu_i}$. and the average threshold voltage, $\overline{V_t}$, of the s-SWNTs from the slope and the intercept of a plot of average sheet conductance ($\frac{\Delta L_c}{\Delta R_{on-off} W}$) versus V_g (Fig. 3.2e). In particular, in the linear region, where $V_d << V_g$, it can be shown that

$$\frac{\Delta L_c}{\Delta R_{on-off} W} = (\overline{\mu_i} C_w) V_g - \overline{\mu_i} C_w \overline{V_t} \qquad (6)$$

where C_w is the specific capacitance per unit area of the TFT device, and W is the channel width of the device. The specific capacitance per unit area of the TFT device for an infinite array of parallel SWNTs with uniform spacing $1/D$ that includes the effects of electrostatic screening and fringing fields is given by:

$$C_w = \frac{D}{C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_s}\log\frac{\sinh(2\pi t D)}{\pi R D}} \qquad (7)$$

where C_Q^{-1} is the quantum capacitance [21] ($4\cdot10^{-10}$ F·m^{-1}), R is the radius of the SWNTs, t is the distance to the gate electrode, ε_s is the dielectric constant of the surface/interface where we place the SWNTs[4] and D is the density of the SWNTs. The dielectric constant in the quartz/SWNT/HfO_2 sandwich structure is $\varepsilon_s = (\varepsilon_{SiO2}+\varepsilon_{HfO2})/2 = (4+16)/2 = 10$. If we take D as corresponding only to the contribution of the s-SWNTs, then we find that $\overline{\mu_i}$ ~5700 cm^2/Vs, which is in the same range as average values reported previously in array and single tube devices [2,4,7,22] and between those determined from analysis of blue (~2300 cm^2/Vs) and green (~10,000 cm^2/Vs) devices. The same analysis yields $\overline{V_t}$ = 0.50 ± 0.05 V.

Similar analysis was performed on transistors that use Au for source and drain metallization, as shown in Fig. 3.3. Comparable to the Pd case, the red cluster of Au devices yield $\frac{1}{G_{c,m}}$ = ~ 20 ± 10 kΩ and $\frac{1}{\sigma_m}$ = ~30 ± 5 kΩ/µm. The extracted values of the $\frac{1}{G_{c,m}}$ and the $\frac{1}{\sigma_m}$ for the other clusters of Au devices are ~50 ± 10 kΩ (blue) and ~20 ± 5 kΩ (green), and ~20 ± 5 kΩ / µm and ~30 ± 5 kΩ / µm respectively. The s-SWNTs in the p-channel branch, on the other hand, show different behavior. In particular, for Au, $\frac{1}{G_{c,s}}$ is, unlike Pd, dependent on V_g. The magnitude increases systematically from ~180 kΩ to ~240 kΩ as V_g increases from -0.44V to -0.24V. Qualitatively, this behavior is

also observed in the blue cluster of Au devices, but not clearly evident in the green devices. Throughout this range, the values are considerably larger than those in the Pd cases. The lower work function of Au and its poorer wetting on SWNTs compared to Pd might explain these differences. These values are also about an order of magnitude larger than single tube devices reported (~10 – 30 kΩ), for diameters of ~ 3 nm and pure Au electrodes [23]. These differences might be caused by different processing conditions, which are known to be extremely important to the behavior of the contacts. The intrinsic mobility of the s-SWNTs extracted from analysis of Au devices is ~3700 cm^2/Vs, comparable to that in the Pd devices. This value is also similar to the values obtained from analysis of the other clusters of devices (i.e. ~2500 cm^2/Vs for blue; ~2100 cm^2/Vs for green). The threshold voltage from this analysis is 0.10 ± 0.05 V. The response in the n channel regime operation shows a similar trend. First, the inverse of the average conductance of the contact shows systematic dependence on V_g, decreasing from ~650 kΩ to ~450 kΩ as V_g increases from 0.36V to 0.48V (Fig. 3.4b). Similar results are obtained from analysis of other clusters of devices. We speculate that these behaviors result from the larger Schottky barrier for electrons than holes. The intrinsic mobility observed for electrons is ~4100 cm^2/Vs, similar to that for holes and not too dissimilar from results for the other clusters of Au devices (3600 cm^2/Vs for blue; 1600 cm^2/Vs for green). The threshold voltage from this analysis is 0.2 ± 0.1 V.

4.4 Conclusions

In conclusion, systematic studies of channel length scaling in SWNT array transistors show that Pd provides an ohmic contact to the arrays, with little dependence of resistance on gate voltage. Operation in this case is dominated by modulation of the channel resistance by the gate. Devices with Au, on the other hand, show behavior indicative of gate modulation of both the channel and the contacts, particularly in the n channel branch. In most cases, quantitative values for the inferred mobilities, SWNT resistances and contact behaviors are in the same range as those reported previously in single tube test structures and, for certain parameters, in array devices.

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4.6 Figures

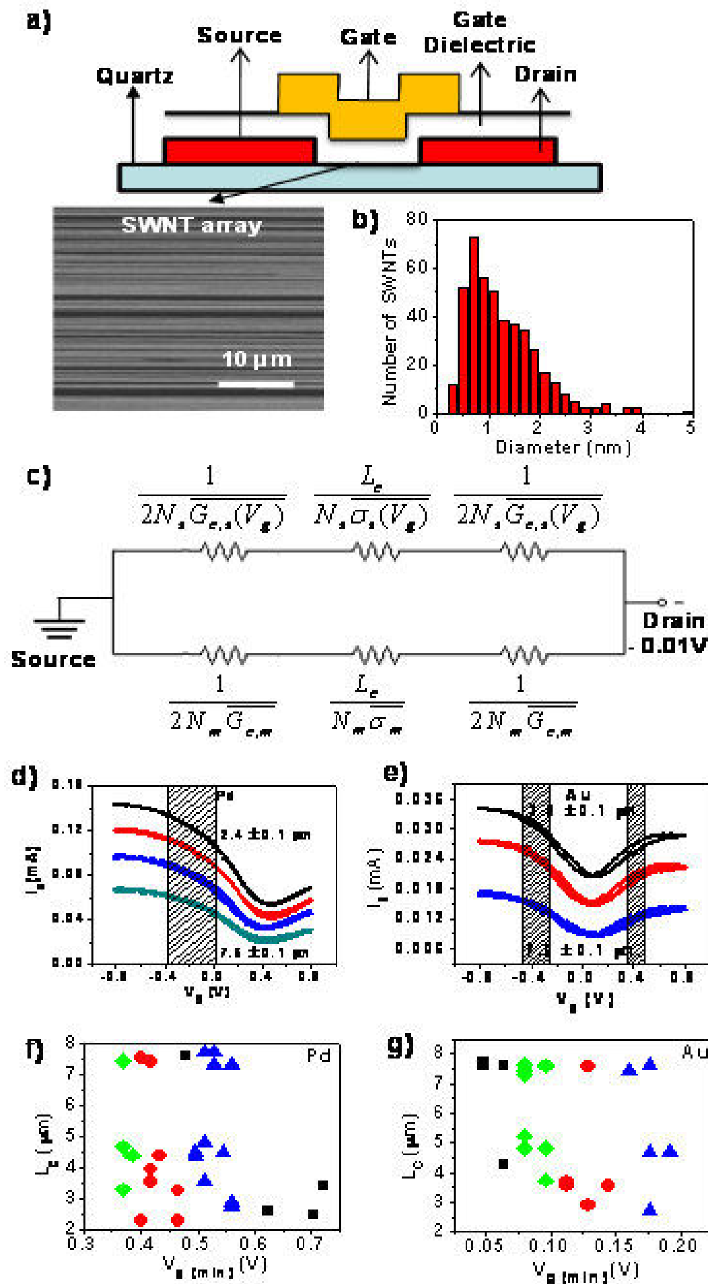

Figure 4.1. (a) Schematic illustration of a single walled carbon nanotube (SWNT) array transistor with an SEM image of a representative array in the frame below. (b) Typical

Figure 4.1 (continued): diameter distribution of SWNTs measured by AFM. (c) Equivalent circuit model for a device with channel length L_c, showing the resistances contributed by the inverse of the average conductances of the contacts to the semiconducting and metallic SWNTs (i.e. $\frac{1}{G_{c,s}}$ and $\frac{1}{G_{c,m}}$, respectively) and their role in transport through the channel (i.e. $\frac{L_c}{\sigma_s}$ and $\frac{L_c}{\sigma_m}$). The number of s-SWNT and m-SWNT is N_s and N_m , respectively. Representative transfer curves of (d) Pd and (e) Au electrode devices with channel width (W) = 400 µm at V_d = -0.01V. The channel lengths of the Pd devices are 2.4 ± 0.1 µm (black symbols), 3.7 ± 0.3 µm (red symbols), 4.4 ± 0.1 µm (blue symbols) and 7.5 ± 0.1µm (green symbols) from top to bottom. The channel lengths of the Au devices are 2.9 ± 0.1 µm (black symbols), 3.7 ± 0.1 µm (red symbols) and 7.6 ± 0.1 µm (blue symbols) from top to bottom. The highlighted regions show the range of V_g values that were analyzed. The bottom frames show combinations of L_c and gate voltages at minimum current ($V_{g(min)}$), for (f) Pd and (g) Au devices. The devices that form the focus of the analysis are shown in red. Two other clusters of devices, indicated in blue and green, were also analyzed.

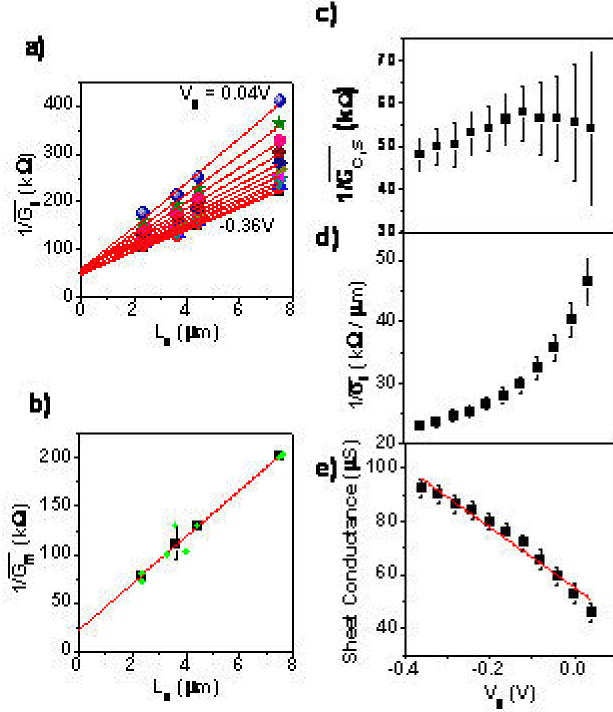

Figure 4.2. Channel length scaling and extracted intrinsic properties of Pd devices. (a) The inverse of the average conductance of an s-SWNT ($\frac{1}{\overline{G_s}}$) as a function of channel length (L_c) at gate voltages (V_g) of 0.04V (blue circles), 0V (green stars), -0.04V (pink hexagons), -0.08V (brown pentagons), -0.12V (blue diamonds), -0.16V (light green triangles), -0.20V (pink triangles), -0.24V (dark green triangles), -0.28V (blue triangles), -0.32V (red circles) and -0.36V (black squares) from top to bottom. (b) The inverse of the average conductance of an m-SWNT ($\frac{1}{\overline{G_m}}$) as a function of channel length. The black squares with error bars represent the average of individual devices (green circles). (c) Inverse of the average conductance of the contact of the s-SWNT ($\frac{1}{\overline{G_{c,s}}}$) extracted from the intercept in (a) as a function of gate voltage. (d) Inverse of the average conductivity of the s-SWNT ($\frac{1}{\overline{\sigma_s}}$) extracted from the slope in (a) as a function of gate voltage. (e) Sheet conductance of the s-SWNT as a function of gate voltage.

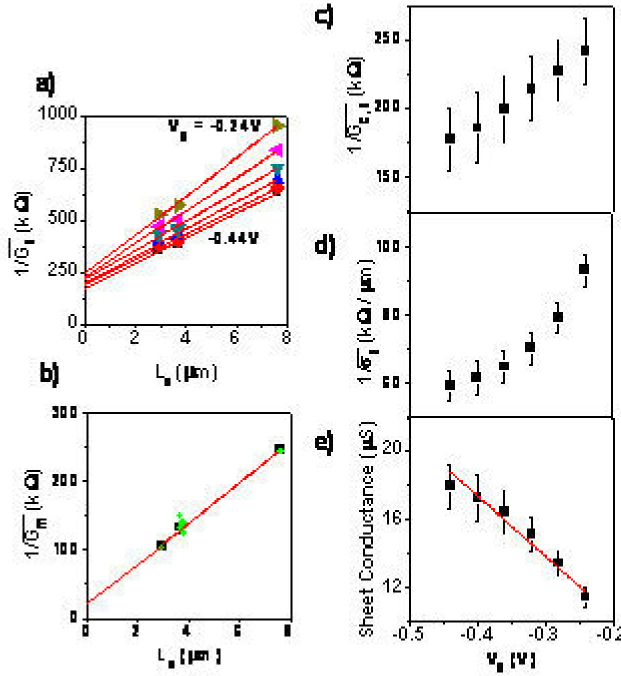

Figure 4.3. Channel length scaling and extracted intrinsic properties of the m-SWNT and s-SWNT in the p-channel branch of the gold electrode devices. (a) The inverse of the average conductance of the s-SWNT ($\frac{1}{\overline{G_s}}$) as a function of channel length (L_c) at gate voltages (V_g) of -0.24V (light green triangles), -0.28V (pink triangles), -0.32V (dark green triangles), -0.36V (blue triangles), -0.40V (red circles), and -0.44V (black squares) from top to bottom. (b) The inverse of the average conductance of a m-SWNT ($\frac{1}{\overline{G_m}}$) as a function of channel length. The black squares with error bars represent the average of individual devices (green circles). (c) The inverse of the average conductance of the contact of the s-SWNT ($\frac{1}{\overline{G_{c,s}}}$) extracted from the intercept in (a) as a function of gate voltage. (d) The inverse of average channel conductivity of the s-SWNT ($\frac{1}{\overline{\sigma_s}}$) extracted from the slope in (a) as a function of gate voltage. (e) Sheet conductance of the s-SWNT as a function of gate voltage.

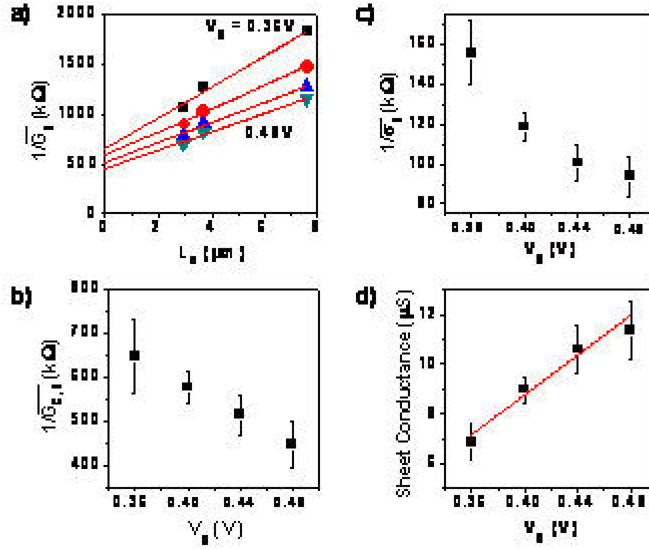

Figure 4.4. Channel length scaling and extracted intrinsic properties of the s-SWNT in the n-channel branch of the gold electrode devices. (a) The inverse of the average conductance of a s-SWNT ($\frac{1}{\overline{G_s}}$) as a function of channel length (L_c) at gate voltages (V_g) of 0.36V (black squares), 0.40V (red circles), 0.44V (blue triangles) and 0.48V (green triangles) from top to bottom. (b) The inverse of average conductance of the contact of the s-SWNT ($\frac{1}{\overline{G_{c,s}}}$) extracted from the intercept in (a) as a function of gate voltage. (c) The inverse of average channel conductivity ($\frac{1}{\overline{\sigma_s}}$) of the s-SWNT extracted from the slope in (a) as a function of gate voltage. (d) Sheet conductance of the s-SWNT as a function of gate voltage.

CHAPTER 5

ELECTROLUMINESCENCE FROM ELECTROLYTE-GATED CARBON NANOTUBE FIELD-EFFECT TRANSISTORS

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5.1 Introduction

In recent years, field-effect transistors (FET) based on single-walled carbon nanotubes (SWNT) have been shown to exhibit a range of interesting optoelectronic effects. [1] In particular, near-infrared electroluminescence (EL) was demonstrated for ambipolar and unipolar field effect transistors that used either random networks of SWNTs or individual SWNTs. [2-6] In these devices, excitons resulted from the recombination of holes and electrons that were injected from the source and drain electrodes, respectively. However, external quantum efficiencies were generally low (10^{-7} to 10^{-6} photons per electron), [4,5] and many nanotube FETs suffered from current hysteresis due to the presence of water under ambient conditions and the high voltages required for sufficient injection of holes and electrons. [3,7,8] Because nanotubes with large diameters (›1.5 nm) and small band gaps have the lowest injection barriers for both carrier types, [9] they are best suited for ambipolar FETs, and thus electroluminescence is usually observed at wavelengths around 1.8 to 2 µm. [4-6]

In order to make light-emitting carbon nanotube FETs interesting for applications, their device properties have to be improved significantly. Major objectives are minimization of applied voltages and current hysteresis, device uniformity and reproducibility, for example, by statistical averaging over many nanotubes, and optimization of electroluminescence efficiency in the optical telecommunications window by shifting emission toward shorter wavelengths and avoiding quenching caused by metallic nanotubes and substrate effects.

Here we present near-infrared light emission from electrolyte-gated ambipolar field-effect transistors with large scale, parallel arrays of carbon nanotubes grown by chemical vapor deposition (CVD) on quartz substrates. Two aspects of these devices are significant, compared to previous light emitting nanotube transistors. First, we use high quality, nearly perfectly linear, aligned arrays of SWNTs that have been shown to yield transistors with excellent performance characteristics, high levels of reproducibility in wafer-scale arrays, and demonstrated applications in radio frequency electronics and other integrated systems. [10,11] These arrays provide a multitude of light sources with potential for high overall output. They also offer reproducible properties due to statistical averaging effects owing to the large numbers of tubes in the channel without the drawback of uncontrolled energy transfer and quenching by metallic tubes associated with dense random arrays of SWNT. They are significant for basic scientific study because emission from large numbers of tubes can be evaluated in a single device under identical conditions, thereby allowing systematic investigations of emission properties depending on tube diameter, chirality, and other characteristics. Disadvantages of these thin film-like arrays are the presence of metallic nanotubes that cause large off currents and reduce overall efficiency and the inability to determine individual current-voltage characteristics and threshold voltages of the carbon nanotubes in the array.

The other important feature of the light-emitting FETs introduced here is that they use electrolyte gating as a way to achieve high charge carrier densities with drastically reduced gate and source-drain voltages while avoiding current hysteresis, as demonstrated previously in carbon nanotube and organic field-effect transistors. [12-15] In these devices, the gate dielectric is replaced by an electrolyte, for example, imidazoliumbased ionic liquid gels or LiClO4 dissolved in poly(ethyleneglycol) (PEG). When a negative voltage is applied, positive cations are attracted to and negative anions are repelled from the gate electrode. The cations form an electric double layer at the gate/electrolyte interface, while the anions do the same at the carbon nanotube/electrolyte interface, where they induce accumulation of holes in the nanotube. The bulk electrolyte remains charge-neutral so that almost all of the applied potential is dropped across these electric double layers, which leads to an extremely high effective gate capacitance of tens of $\mu F \cdot cm^{-2}$ and thus high charge carrier densities. Changing the gate voltage causes the

ion distribution to re-adjust with diffusion-limited rates. This redistribution avoids charge trapping and associated hysteresis that occur in oxide dielectrics. The strong gate coupling provided by the electrolyte enables efficient charge injection, due to sharp bending of the valence and conduction band at the metal/nanotube interface and thus enhanced tunneling through the thin Schottky barrier. In this manner, both holes and electrons can be efficiently injected even into carbon nanotubes with relatively small diameters (*i.e.*, large band gaps) and under ambient conditions. Simultaneous injection of both charge carriers leads to coexisting hole, and electron accumulation zones along the nanotube and light emission take place at the point where the opposite charge carriers meet and recombine. The position of the recombination zone is determined by the gate and source-drain voltages and thus the local potential along the nanotubes. [3,16,17] We note that electroluminescence from electrolyte-gated SWNTs is particularly interesting because metal ions can quench nanotube luminescence. [18] Here positive (*e.g.*, Li^+) and negative (*e.g.*, $ClO4^-$) ions are accumulated closely (Debye length ~ 0.1 nm) around the nanotubes, and strong quenching might be expected.

Our device structure allows us to study the effect of the dielectric environment on charge transport in and emission from carbon nanotubes. As a quasi-one dimensional object, the medium surrounding the nanotube has a strong influence on emission wavelength, peak width, and photoluminescence yield. [19,20] Increasing the dielectric constant ε leads to increased exciton screening and thus a decreased exciton binding energy. Simultaneously, the self-energy correction causes a red shift of emission that is larger than the blue shift associated with the reduced binding energy. [21,22] As charge screening increases with the dielectric constant of the surrounding medium, interband transitions (blue-shifted with respect to the exciton) become stronger and eventually dominate according to theory. [20] This has not yet been observed for photoluminescence from carbon nanotubes due to the strong luminescence quenching of nanotubes on solid substrates. [19,23,24] For electroluminescence, these limitations are less strict because very large numbers of excitons can be generated and thus light detection from individual nanotubes remains possible despite low efficiencies. For example, a small contribution of interband emission was recently assigned to unipolar impact excitation electroluminescence. [25,26] A very high ε dielectric that could lead to interband

transitions is TiO2 (ε = 60-80). However, TiO2 is not very suitable as a thin gate dielectric on its own due to its relatively small band gap and thus high leakage. We will show that adding a thin layer (few nm) of TiO2 or HfO2 (ε ~ 25) to the electrolyte-gated carbon nanotube FETs allows us to significantly increase the dielectric constant of the nanotube environment without drastically altering the overall device and emission characteristics.

5.2 Methods

We fabricated devices as shown in Figure 5.1a on double-side polished quartz wafers (ST-cut) whose annealed surface templates dense (1-10 SWNT/μm) and highly aligned growth of single-walled carbon nanotubes (see scanning electron micrograph, inset Figure 5.1a) from prepatterned submonolayer iron catalyst lines as described previously. [42] Evaporation and lift-off of Ti (1-2 nm)/Pd (30-40nm) gave source and drain electrodes with channel lengths (*L*) of 5-15 μm and channel widths (*W)* of 150 and 250 μm. Oxide buffer layers were deposited by electron beam evaporation (TiO2, thickness 7 nm) or by atomic layer deposition (HfO2, at 120 °C with alternating pulses (50 cycles) of tetrakis(dimethylamido)hafnium(IV) precursor (0.06 s) and H2O (0.6 s)). To complete the devices, a piece of polydimethylsiloxane (PDMS) elastomer with a trench was placed over the source and drain electrodes, so that the trench allowed access to the channel area while the larger parts of the electrodes were in conformal contact with the PDMS to reduce gate leakage. The trench was filled with the electrolyte, for example, polyethylene glycol methyl ether (PEG, Aldrich): $LiClO_4 \cdot 3H_2O$ (weight ratio 12:1) or the ionic liquid 1-butyl-3-methylimidazolium octyl sulfate (Aldrich). A PtIr wire immersed in the electrolyte acted as the gate electrode. Two Keithley 2400 source meters applied voltage to the gate and drain, while the source was grounded, and acquired current-voltage characteristics of the completed transistors. A near-infrared objective (Olympus LMPL 100xIR, NA = 0.8) collected light emitted through the quartz substrate (thickness 500 μm). The image was focused onto the entrance slit of a spectrometer (Acton SP150, focal length 15 cm) that enabled direct imaging with a mirror and spectral resolution with a grating (150 grooves/mm, blaze 1250 nm). A liquid nitrogen cooled InGaAs camera (Princeton Instruments 2D-OMA V) acquired images and spectra during

voltage sweeps synchronized *via* a Labview interface. Each image was exposed and accumulated over a total of 60 s.

5.3 Results and Discussions

Figure 5.1a shows a schematic of the electrolyte-gated nanotube FET and the electroluminescence measurement setup. We fabricated aligned carbon nanotube transistors on quartz substrates with Ti/Pd source-drain electrodes (see inset Figure 5.1a) and a liquid electrolyte contacted with a PtIr wire as the gate electrode. Figure 5.1b,c shows current-voltage characteristics of nanotube array field-effect transistors gated *via* an electrolyte of either PEG:LiClO4 or the ionic liquid 1-butyl-3-methylimidazolium octyl sulfate ($[BMIM]^+[octOSO3]^-$). In both cases, ambipolar charge transport is evident for very low gate (Vg) and source-drain (V_{ds}) voltages with negligible hysteresis despite the very slow gate voltage sweep rate. Such extended bias stress typically leads to strong hysteresis in devices that use conventional oxide gate dielectrics. The limited gate modulation of the source-drain current (Ids) is partially due to the ambipolar nature of the transport (*i.e.*, the hole and electron accumulation ranges overlap so that the channel is never in depletion) and to the presence of metallic nanotubes in the arrays. The point of minimum current roughly follows the expected Vg=Vds/2 dependence for ambipolar FETs with threshold voltages near zero. [27] Effective peak mobilities for holes and electrons were calculated to range between 600 and 1200 cm2 V^{-1} s^{-1} using $\mu = (\delta I_{ds}/\delta V_g) \cdot (L/(W \cdot V_{ds} \cdot C))$, with channel width W and channel length L. The devices capacitance C is determined using the quantum capacitance of a carbon nanotube with one sub-band occupied ($C_q = 4 \times 10^{-10}$ F · m^{-1}) [28] and the density of the nanotube array $\delta N/\delta W$ =5-10 μm^{-1} minus the metallic tubes: $\delta N/\delta W$ = 3-7 μm^{-1} (N is the number of nanotubes in the channel) with Cq · $\delta N/\delta W$ = 0.12 - 0.28 μF · cm^{-2}. The effective capacitance of the electrolyte (C_{el} > 10 μF · cm^{-2}) is orders of magnitude larger than the quantum capacitance of the array so that the total capacitance ($1/C = 1/C_{el} + 1/C_q$) is dominated by the latter.

The average maximum conductance per nanotube (including metallic SWNT) is on the order of 0.04 e^2/h (for L = 10 μm), which is comparable to values reported by Zhou *et al.* for nanotubes with diameters of 1.5 nm. [29] This value is within the average

diameter distribution of the nanotube arrays determined by atomic force microscopy (AFM) and Raman spectroscopy.

We note that, although imidazolium-based ionic liquids can disperse carbon nanotubes through weak van der Waals interactions, [30] we did not find evidence that the nanotubes become detached from the quartz surface when 1-butyl-3-methylimidazolium octyl sulfate is used as the electrolyte. Nevertheless, due to its comparatively large electrochemical operating window, we used PEG:$LiClO_4$ as the electrolyte for all experiments described in the following.

We observe light emission from electrolyte gated carbon nanotube array transistors for a range of gate voltages, as a collection of emission spots, each of which corresponds to an individual nanotube in the array, as shown in Figure 5.2a. These emission spots appear to be nearly diffraction-limited with an isotropic full width at half-maximum of about 1.5 μm. For a source-drain voltage of -2.4 V, light emission appears at the source electrode for positive or small negative gate voltages (*e.g.*, for $V_g = 0$). Under these bias conditions, electrons accumulate over the entire length of the channel and hole injection at the source leads to recombination and emission along the edge of the electrode visible as a string of light spots. As the gate voltage shifts toward more negative values, the hole accumulation layer extends further away from the source. The point of charge recombination and emission for each nanotube shifts more into the channel and moves with decreasing gate voltage toward the drain (*e.g.*, V_g=-1.2 V in Figure 5.2a). The reverse movement takes place when the gate voltage increases again.

Figure 5.2b shows a composite image of emission from the device in Figure 5.2a. This image is created by assigning to each pixel the highest brightness value detected during the entire voltage sweep. In this way, traces of exciton recombination along the nanotubes become visible as well as apparently disconnected emission spots. The number of emission traces in Figure 5.2a is significantly smaller than one would expect from the nanotube density determined by SEM and AFM. One third of the nanotubes are metallic and do not emit light. The observed movement of emission spots and increased brightness close to the contacts exclude the possibility of emission from metallic tubes due to Joule heating. [31] The diameter distribution of the aligned nanotubes indicates that the majority emits at wavelengths longer than 1600 nm that are not detected by our InGaAs

camera, which could account for the small number of observable emission spots compared to the density of aligned nanotubes estimated by SEM.

The average current density in these devices is on the order of 1-5 μA per nanotube. The distribution of current within the ensemble of nanotubes is determined by the conductance and contact resistance of metallic and semiconducting nanotubes with different diameters. The on-state conductance of semiconducting nanotubes is similar to that of metallic ones and increases linearly with nanotube diameter. [29,32] Higher injection barriers for larger band gap nanotubes and thus higher contact resistance further reduce the number of charges going through these nanotubes. Although this effect should be lower in electrolyte-gated devices compared to those with thick oxide dielectrics, it is likely to still play a role. We assume that these factors shift the distribution of current density toward large diameter nanotubes and thus decrease the probability of observing emission from smaller diameter nanotubes that emit within our detection range. Energy transfer to metallic or smaller band gap nanotubes [33] should not be a significant problem because nanotubes grown on quartz are almost perfectly aligned in parallel, and only very few of them form bundles or intersect with each other compared to random networks.

Devices with aligned arrays of SWNTs enable imaging of electroluminescence from many different nanotubes at a time and thus highlight the distribution of possible defects and emission efficiencies. Examples of position and intensity *versus* gate voltage plots are shown in Figure 5.2c. The movement of these light spots is reproducible for several voltage sweeps, and overall emission intensity increases with increasing source-drain voltage. It is evident from Figure 5.2a,c that emission spots associated with individual nanotubes reach different positions along the channel for the same gate and source-drain voltage. We attribute these variations to the distribution of diameters and chiralities of nanotubes in the array resulting in different injection barriers and thus voltage drops at the contacts. [9]

In a simplified picture, we can assume diffusive transport and use the gradual channel approximation as shown by Tersoff *et al.* [16] to find the dependence of the emission spot position x_0 (as distance from drain) on V_g and V_{ds} including constant voltage drops at the source ($V_{C,s}$) and drain ($V_{C,d}$) electrodes to be

$$\frac{x_0}{L} = \frac{(V_{ds} - V_{C,d} - V_g)^2}{(V_{C,s} - V_g)^2 + (V_{ds} - V_{C,d} - V_g)^2} \quad (1)$$

In the ambipolar regime, there is an overall voltage drop equal to the band gap due to the crossover from electron to hole conduction. Therefore $V_{C,s}$ and $V_{C,d}$ cannot be smaller than the Schottky barrier heights for holes and electrons, respectively. The emission zone moves from the source to the drain electrode within a gate voltage range of $V_{ds} = (V_{C,s} + V_{C,d})$. [16] This suggests that the larger voltage drops at the contacts with wide band gap (*i.e.*, small diameter) nanotubes should lead to a more rapid change of the emission zone position with gate voltage compared to small band gap (*i.e.*, large diameter) nanotubes. The difference between the voltage drop at the source and that at the drain electrode, the work function of Pd being closer to the SWNT valence band than the conduction band, should only cause an overall Vg shift of the curve compared to symmetric injection barriers. Absolute values of hole and electron mobility do not have an impact on the movement of the emission zone provided that their ratio is close to unity, as is the case for our devices. According to this model, relative differences in motion of emission spots with gate voltage can be attributed to different voltage drops at the contacts and thus to different nanotube band gaps. This simple picture is complicated by the unknown gate voltage dependence of contact resistance and thus voltage drop at the contacts and the influence of electrolyte gating on it.

In order to study the light emission from carbon nanotubes embedded in high ε dielectrics, we deposited thin layers of HfO2 (5 nm by atomic layer deposition, ε ~ 25, C_{HfO2} = 4.4 μF · cm^{-2}) and TiO_2 (7 nm by electron beam evaporation, ε ~ 60, C_{TiO2} = 7.6μF · cm^{-2}) on top of the aligned carbon nanotubes as a buffer dielectric after the source/drain electrodes were patterned and before the device was completed as described earlier with the electrolyte and gate electrode. The capacitance of these thin buffer layers is still much higher than the quantum capacitance of the nanotubes, so that the overall efficiency of gating is not significantly decreased. Moreover, leakage through the electrolyte is greatly reduced, and device stability at higher voltages improved due to the separation of the source/drain electrodes from the electrolyte. The advantages of using electrolyte gating instead of a thin oxide as the only dielectric are simplified fabrication,

high device yield, and reduction of leakage and dielectric breakdown especially for a high ε dielectric such as TiO_2 with a small band gap.

Figure 5.3a,b shows current-voltage characteristics of nanotube FETs with buffer layers of HfO_2 and TiO_2, respectively. They are overall similar to those of purely electrolyte-gated devices except for a threshold shift. In both cases, the transfer curves are shifted toward more positive gate voltages, which could indicate p-doping that occurred during the oxide deposition process or an increased contact resistance for electrons due to the additional dielectric. Despite this, we observe electroluminescence from these devices in a similar fashion as without the buffer layers. Examples are shown in Figure 5.3c (HfO_2) and Figure 5.4 (TiO_2). The same movement of emission spots from the source to the drain electrode takes place, and the intensity of emission from the individual nanotubes increases with source-drain voltage.

Again, using an array of nanotubes allows for observing emission from a range of nanotubes with different band gaps and possibly defects within a single device under uniform bias conditions. Panels 1 and 2 in Figure 5.3d show the position of light emission with changing gate voltage for two nanotubes. In panel 1, the emission zone moves from the source to the drain electrode over a gate voltage range of 1.3 V for a source-drain voltage of -2.8 V. This gives us a direct estimate of the voltage drop at the contacts because this voltage range equals $V_{ds} - (V_{C,s} + V_{C,d})$. The total voltage drop is 1.5 V, which is larger than any possible band gap of a nanotube in the array, based on the measured diameter distribution, but significantly smaller than values found for ambipolar FETs with small band gap nanotubes on SiO_2 dielectrics (5-6 V).16 FETs without any buffer layer (see Figure 5.2c), and those with TiO_2 as the buffer dielectric (see Figure 4) exhibit similar contact-induced voltage drops. This is direct evidence that electrolyte gating significantly reduces contact resistance in carbon nanotube field-effect transistors. In Figure 5.3d, panel 2, the progression of emission zone position with gate voltage is much steeper than that in panel 1. A voltage difference of only 1 V covers the entire channel length. The overall voltage drop at the contacts therefore amounts to about 1.8 V, indicating that this nanotube has a larger band gap than the one in panel 1.

Besides emission from nanotubes with different band gaps, we observe emission traces that do not extend all the way across the channel but are confined to part of the

channel, as shown in Figure 5.3d, panels 3 and 4. Various explanations are possible. A nanotube could change its chirality along the channel [19,34] and may emit outside the detection range from that point on. Alternatively, it could join a bundle, which would lead to energy transfer to smaller band gap nanotubes. Panel 4 in Figure 5.3d could be explained either way because emission disappears for more negative gate voltages before reoccurring at the same position when the voltage sweep is reversed. Another possible scenario for a shortened emission trace is the intersection of the emitting nanotube with a metallic nanotube and thus shorting out of the rest of the channel. The metallic nanotube then acts as an electrode itself. This could be the case in Figure 5.3d, panel 3, because here emission is continuous for the entire gate voltage sweep similar to a nanotube FET with shorter channel length.

Furthermore, we occasionally observe apparently disconnected emission spots within the channel region (see Figure 5.3c) that move little or not at all. Some of these emission spots emerge, move slightly, and disappear again with changing gate voltage. These could originate from short segments of nanotubes that are emissive within the detection range. Others that are stationary could result from defects that can cause impact excitation and thus bright localized emission. [25,35]

In order to estimate the electroluminescence efficiency of electrolyte-gated SWNT-FETs, we need to correlate source-drain current with emission intensity. This can only be done for the entire device including the metallic and small band gap semiconducting nanotubes. As the gate voltage changes and thus alters the conductivity of the semiconducting SWNT, the distribution of current density among the ensemble of nanotubes is expected to change, as well. Figure 5.5 shows source-drain current and light output *versus* gate voltage characteristics for a purely electrolyte-gated FET and for one with a TiO2 buffer layer. Due to the high source-drain bias (2-3 V) necessary to achieve detectable electroluminescence, the current modulation is small. For the FET without a buffer dielectric in Figure 5.5b, the emission intensity increases with decreasing gate voltage as more and more emission spots appear and move through the channel until they have reached the drain electrode and vanish as injection of electrons diminishes. For the device with a TiO2 buffer layer, the total electroluminescence intensity remains relatively unchanged throughout the gate voltage sweep (Figure 5.5e), although emission from

individual SWNT appears strongest close to the electrodes (see Figure 5.4). This may be explained by a broadening of the spectrum near the contacts and thus more photons within the detection range. [3] Alternatively, the increase of emission at the contacts could be a result of the lower mobility and thus higher concentration of carriers in the high field region near the contact as suggested by McGuire *et al*. [36]

In both cases, the maximum emission intensity increases superlinearly with V_{ds} (Figure 5.5c,f), while I_{ds} increases more or less linearly. An exponential dependence of intensity on V_{ds}, which fits the data well, has previously been associated with impact excitation that is more efficient than ambipolar emission. [1,35,37] Although emission close to the electrodes (especially the source) is more intense than within the channel and increases more with V_{ds}, it is not stationary as one would expect for impact excitation [35] but vanishes when voltage conditions become more unipolar. Enhanced injection through the Schottky barrier at higher V_{ds} and thus larger carrier densities could also explain the observed V_{ds} dependence of the integrated emission intensity. This should also lead to higher source-drain currents, which may not show in the overall current-voltage characteristics due to the metallic nanotubes.

We estimate the effective external efficiency for devices with and without oxide buffers to be about 10^{-10} to 10^{-9} photons/electron. This is significantly lower than efficiencies found for ambipolar nanotube electroluminescence in previous studies. [4,5] We are, however, limited in detection to the wavelength range of 800 to 1600 nm. The diameter distribution of the CVD grown SWNT is centered around 1.7 nm (corresponding to an emission wavelength of 2 _m), and only about 10-15% of all nanotubes is expected to emit within the detection range. Spectral resolution of a number of emission spots (Figure 5.6a-d) reveals that most of them represent only the high-energy tail of emission peaks beyond 1600 nm. This prevents a detailed analysis of the influence of the dielectric surrounding on the spectral distribution as well as correlation of emission behavior with nanotube diameter and band gap at this point. For very few emission spots, we could resolve a whole emission peak (Figure 5.6f). The width at half maximum of these peaks varied between 50 and 100nm (27-59 meV), which is significantly broader than

photoluminescence peaks from CVD-grown suspended nanotubes (10-15 meV) [38] but similar to electroluminescence from other long channel devices (25 meV) [4] and narrower than those from short channel nanotube FETs (80-100 meV). [5,39] Assuming this peak width range to be similar for all nanotubes regardless of diameter and taking into account the brightness of those emission spots for which only the high-energy tail of the spectrum was detected, we can estimate that the overall efficiency of these devices is much higher than 10^{-9} photons/electron. This is further supported by the fact that nanotubes with smaller band gaps exhibit more efficient carrier injection and higher mobilities and thus allow for higher current densities than nanotubes with larger band gaps and thus shorter emission wavelengths. Nevertheless, the differences of efficiency between FETs with and without dielectric buffer layers are within the margin of error of detection and device-to-device fluctuations. We thus conclude that emission from carbon nanotubes in direct contact with the electrolyte is not drastically more or less quenched than that from nanotubes embedded in an oxide.

5.4 Conclusions

In conclusion, we demonstrated near-infrared light emission from ambipolar electrolyte-gated field-effect transistors with dense parallel arrays of carbon nanotubes at exceptionally low gate and source-drain voltage and with minimal current hysteresis. The dependence of emission spot position and brightness on the applied voltages yielded information about the relative band gap, possible defects, and interactions of carbon nanotubes in the array and confirmed that electrolyte gating leads to low contact resistance for both charge carriers. Nanotube FETs using thin layers of HfO_2 or TiO_2 as high ε buffer dielectrics showed similar current-voltage and emission characteristics, opening a convenient way to study the influence of different dielectric media on carbon nanotube excitons. The estimated nanotube electroluminescence efficiencies did not significantly depend on the surrounding medium but were lower than previously reported values for ambipolar nanotube FETs on Si/SiO_2. [4,5] The demonstrated device structure is versatile and easy to fabricate with high yields. While the liquid electrolyte can be washed off for further analysis of the nanotubes, solid electrolytes could be employed for other applications. Increasing the ratio of semiconducting to metallic nanotubes and

better control over the chirality and diameter distribution [40,41] will further improve device performance and electroluminescence yield of these nearinfrared light-emitting FETs.

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5.6 Figures

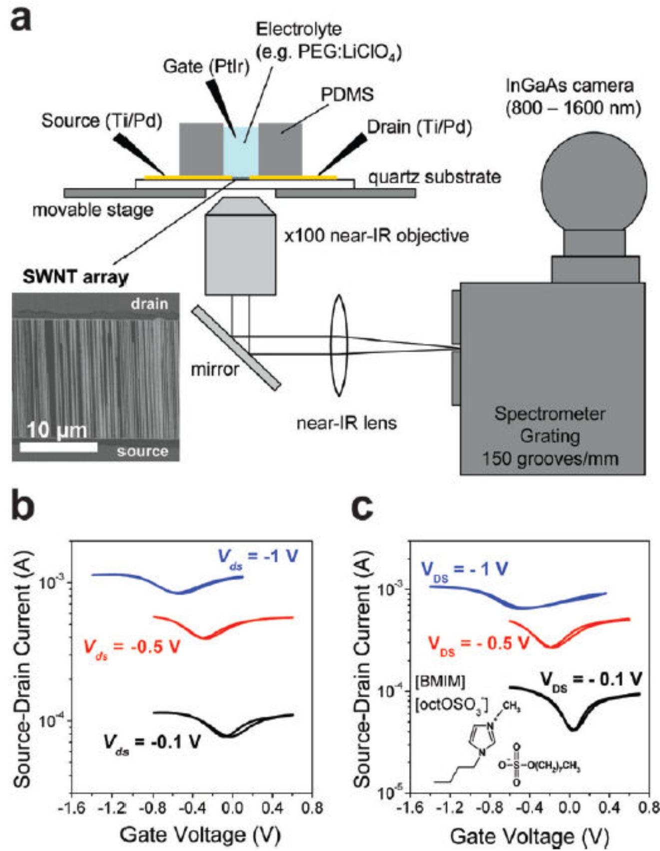

Figure 5.1. (a) Schematic illustration of device structure of an electrolyte-gated ambipolar carbon nanotube field-effect transistor and experimental setup for detection of near-infrared electroluminescence. FETs consist of an array of highly aligned single-walled carbon nanotubes on a double-side polished quartz wafer (thickness 500 µm) contacted with Ti/Pd source/drain electrodes (inset: scanning electron micrograph (SEM)). Emitted light is collected through the quartz substrate by a microscope objective and imaged onto a liquid nitrogen cooled InGaAs focal plane array. (b) Current-voltage characteristics of electrolyte-gated carbon nanotube FET with PEG:LiClO4 electrolyte (channel length L = 10 µm, channel width W = 150 µm). (c) Current-voltage characteristics of electrolyte-gated carbon nanotube FET with ionic liquid, $[BMIM]^+[octOSO3]^-$, electrolyte (channel length L = 10 µm, channel width W= 150 µm). In both cases, the gate voltage was scanned at 5 mV/s.

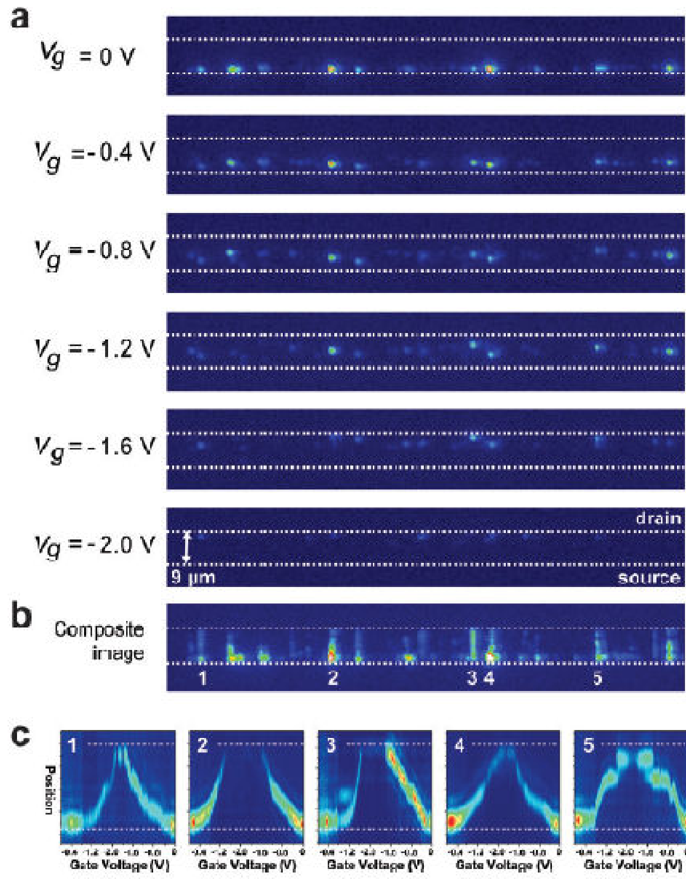

Figure 5.2. (a) False-color intensity images of electroluminescence from electrolyte (PEG:$LiClO_4$)-gated array of SWNT (L = 9 µm, W = 250µm) for source-drain voltage V_{ds} = -2.4 V and different gate voltages (V_g). The white, dashed lines indicate the edges of the source and drain electrodes. (b) Composite image of light emission for entire gate voltage sweep illustrating the emission traces of individual nanotubes along the channel. (c) Position/intensity *versus* gate voltage maps for selected nanotubes in (b).

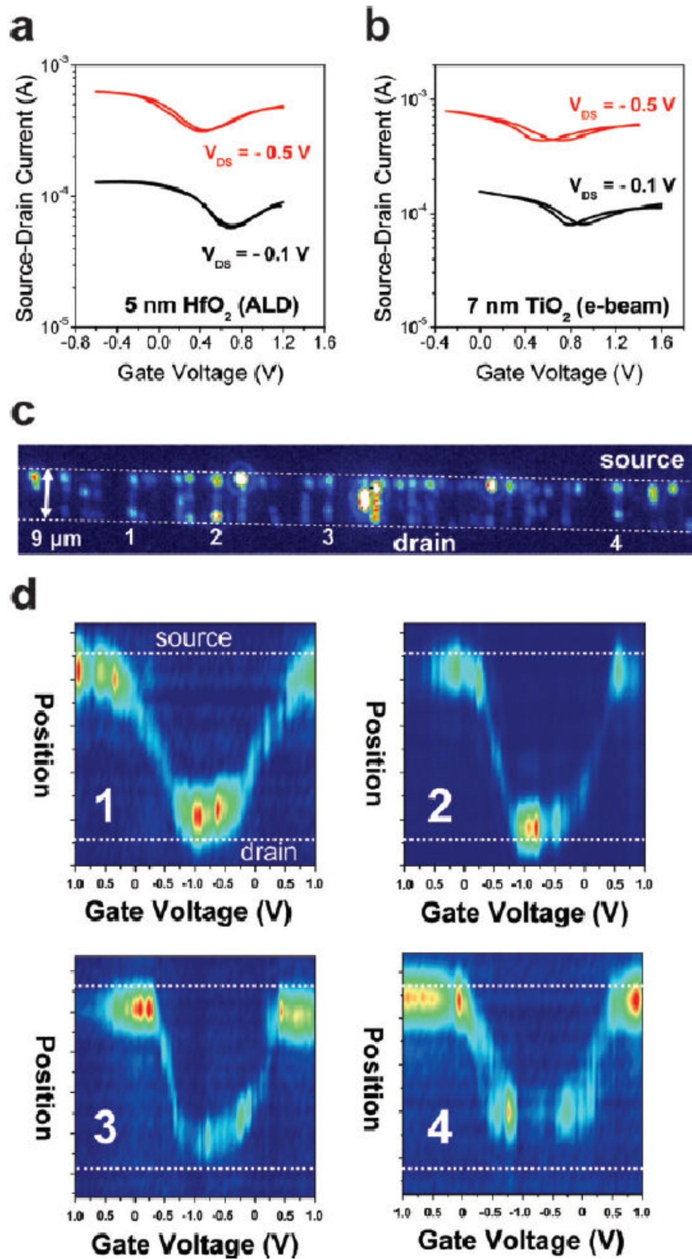

Figure 5.3. (a) Current voltage characteristics of electrolyte-gated SWNT-FET with additional 5 nm HfO_2 (ALD) buffer dielectric (L = 8 µm, W = 150 µm) and (b) 7 nm TiO_2 (e-beam) buffer dielectric (L = 8 µm, W = 150 µm). (c) Composite image of light emission for forward and reverse gate voltage sweep (V_g = 1.0 to -1.0 V, V_{ds} = -2.8 V) of electrolyte-gated FET of aligned carbon nanotubes (L = 9 µm, W = 250 µm) with a 5 nm buffer layer of HfO_2. (d) Position/intensity *versus* gate voltage maps for selected carbon nanotubes (1-4) in (c).

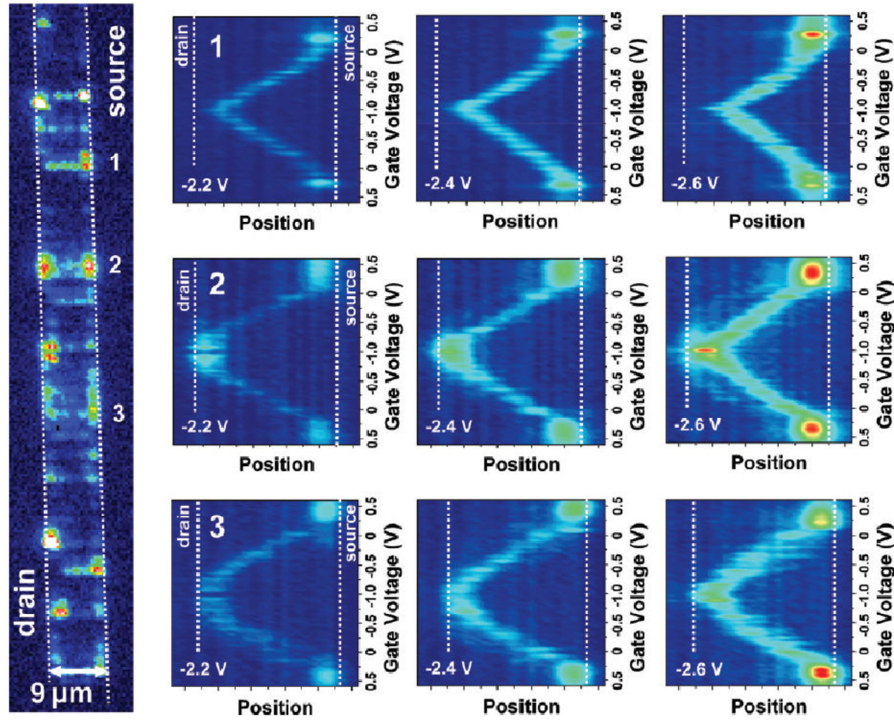

Figure 5.4. Left: composite image of light emission for forward and reverse gate voltage sweep (V_g = 0.6 to -1.0 V, V_{ds} = -2.4 V) of electrolyte-gated FET with aligned arrays of carbon nanotubes (L = 9 µm, W = 250 µm) and a buffer layer of 7nm TiO_2. Right: position/intensity *versus* gate voltage plots of selected nanotubes (1-3) and their evolution with source-drain voltage (-2.2 to -2.6 V).

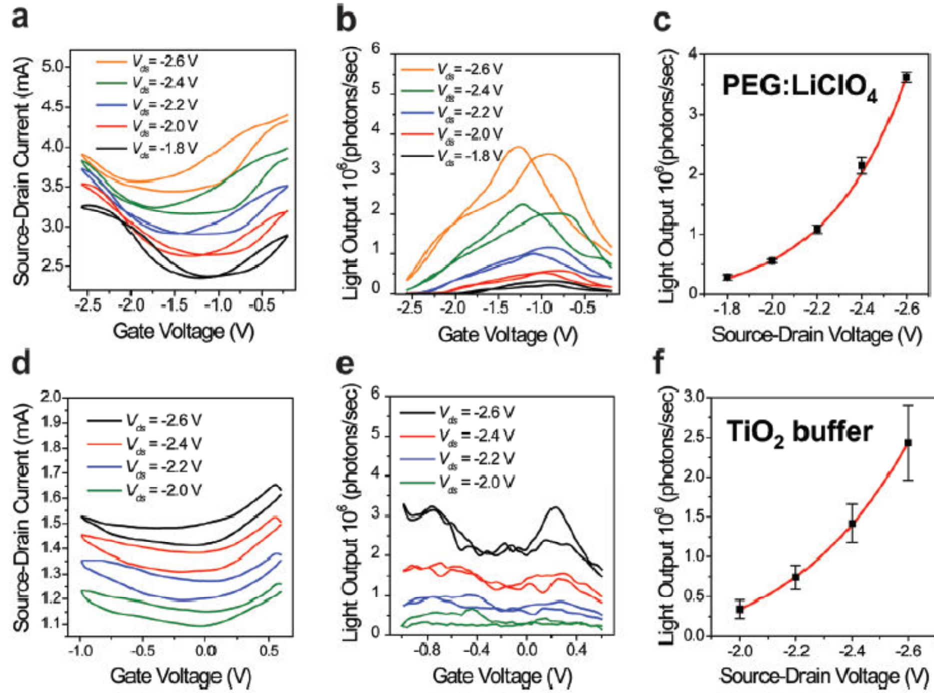

Figure 5.5. (a) Current-voltage characteristics of a SWNT-FET with PEG:LiClO$_4$ electrolyte (L = 6 μm, W = 150 μm). (b) Concurrent light output *versus* gate voltage for this device over the wavelength range of 800 to 1600 nm. (c) Average maximum light output (squares, error bars indicate maximum and minimum values) *versus* source-drain voltage and single exponential fit (red line). (d) Current-voltage and light output (e) *versus* gate voltage characteristics of an electrolyte-gated SWNTFET (L = 9 μm, W = 250 μm) with TiO2 buffer dielectric (7 nm). (f) Average maximum light output (squares, error bars indicate maximum and minimum values) *versus* source-drain voltage for this device and single exponential fit (red line).

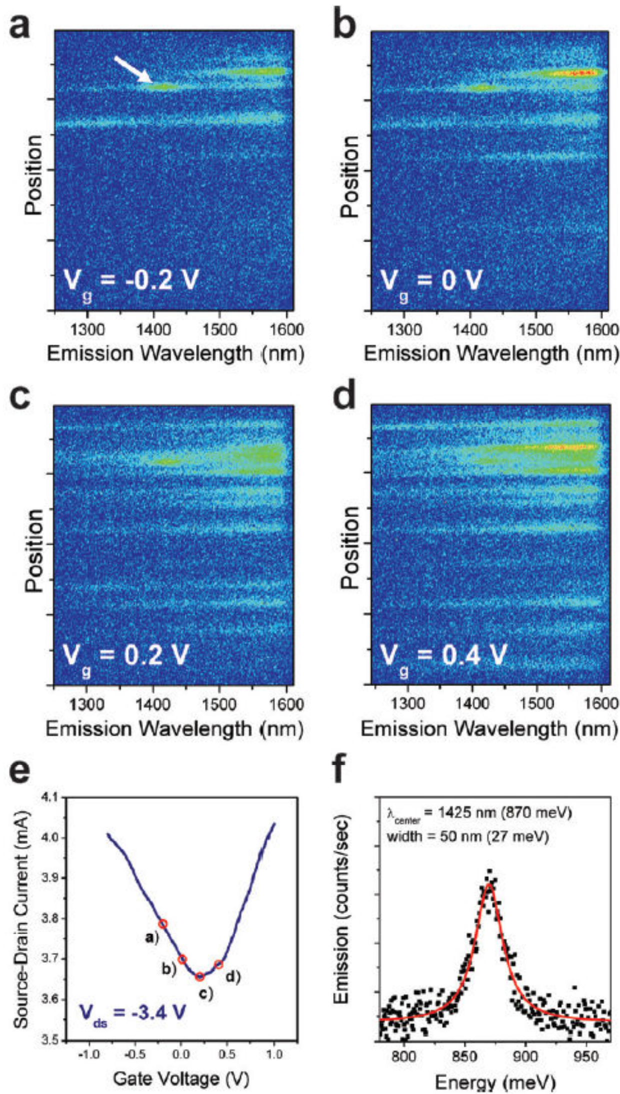

Figure 5.6. (a-d) Electroluminescence spectra of electrolyte-gated array of carbon nanotubes with 5 nm HfO_2 buffer layer (V_{ds} = -3.4 V, L = 6 μm, W = 250 μm). The spectrometer slit (perpendicular to nanotube orientation, parallel to electrode edge, slit width 200 μm) was positioned so that only emission from the middle of the channel was dispersed. The InGaAs camera sensitivity cutoff is at 1600 nm. (e) Current-voltage characteristics of device in (a)-(d). Circles indicate voltage conditions for each spectrum. (f) Resolved emission spectrum for emission spot indicated by white arrow in (a). Lorentzian peak fit (after subtraction of background) gives a peak center λ_{center} of 1425 nm (870 meV) and full width at half-maximum (fwhm) of 50 nm (27 meV).

CHAPTER 6

COMPLEMENTARY THEORETICAL AND EXPERIMENTAL STUDY OF SCHOTTKY DIODES THAT USE ALIGNED ARRAYS OF SINGLE WALLED CARBON NANOTUBES

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6.1 Introduction

Since the earliest days of work on semiconductor devices, diodes have played critically important roles. Theories of p-n Schottky diodes [1,2] laid the foundations for understanding bi-polar transistor operation and contact phenomena at the metal/semiconductor interface. Even though the diode itself is not a main element of modern digital electronics, the physics of the diode structure is essential for many applications, including in optoelectronics [3]. Nanoscale diodes have been already demonstrated with carbon-based nano-materials, such as graphene and individual nanotubes [4-14]. The work presented here focuses on diode structures made of parallel nanotube arrays, their rectification properties and the physics of their electronic transport. The array format is advantageous because they deliver much larger currents than a single-tube device and have less noise, enabling them to operate at high-frequency as we have demonstrated extensively in transistors, amplifiers and even fully integrated transistor radios [15-18]. In addition, arrays provide a natural path toward large scale integration, in which the spatial position and electronic properties of any given tube in the array are not critically important; the large numbers of tubes that contribute to operation of a given device yield statistical averaging effects that can provide good device-to-device uniformity in properties. In currently achievable, as-grown arrays, both semiconducting and metallic species are present, thus making the physics of diode operation more complex than that given by the textbook equations [19]. In this Letter, we combine

experiments with a compact model for device behavior to reveal key aspects. Below we present a clear physical interpretation for the transport experiments with nanotube array diodes as well as for similarly fabricated individual tube diodes. This outcome allows us to extract the average device parameters and correlate them to the physical properties of individual tubes.

6.2 Results and Discussions

We start by considering Schottky diodes based on single semiconducting-SWNTs (s-SWNTs) and resistors based on single metallic-SWNTs (m-SWNTs). Figure 6.1a shows a schematic illustration of such devices. For these cases, as well as the array devices described next, we grew perfectly aligned parallel arrays of SWNTs via chemical vapor deposition (CVD) on a ST (stable temperature) cut quartz, using procedures described elsewhere [20,21]. Electrodes defined by photolithography and liftoff were deposited directly on the arrays. One electrode was Pd(30nm)/Ti(1nm), providing the Ohmic contact [22-24] and the other electrode was Al(30nm)/Ca(3nm), providing the Schottky contact [9,25] to the s-SWNTs. The channel lengths and channel widths were ~10μm and ~15μm, respectively. Narrow stripes (~1μm wide) of photoresist (AZ5214) defined via photolithography protected selected areas of SWNTs before we placed the substrate into a Reactive Ion Etcher (RIE) to oxygen etch unwanted SWNTs. This process increases the chance of obtaining a single SWNT per device by decreasing the number of SWNTs that bridge the metal electrodes and it also electrically isolates neighboring devices. A Scanning Electron Microscope (SEM) was used to determine the number of tubes in each device, after electrical characterization using a Parameter Analyzer (Agilent 4156A).

Parts b and c of figure 6.1 show typical current-voltage (I-V) curves of single m-SWNT resistors and single s-SWNT diodes, respectively, measured with the Al/Ca electrode grounded and the Pd electrode swept between ±2V. The I-V curves of the single m-SWNT resistors are linear while those of the single s-SWNT diodes display rectification at reverse bias, as might be expected. In an ideal diode structure, thermionic current, I_d, follows a simple exponential dependence on the drive voltage, V_d:

$I_d = I_o(\exp[eV_d / nk_B T] - 1)$ where I_o and n are the reverse saturation current and non-ideality factor respectively, e and k_B are electron charge and Boltzmann constant respectively and k_BT/e is the temperature in Volts. None of our devices shows this simple I-V curve, which is consistent with other studies [5,6,10-13,26]. However, we propose a physical model that can adequately describe the behavior. Our devices have channel lengths that exceed the length of the diode junction itself. Thus, the total voltage drop across the whole device is distributed between the junction and the rest of the channel. In addition, we find that a non-negligible current can flow at reverse bias. In multiple tube diodes this current is due to the shunt represented by the m-SWNTs. Since all tubes contribute to the total current in parallel, we derive the analytical expression for the I-V curve as:

$$I_d = \frac{V_d}{R_m} + I_o\left(\exp\left[\frac{e(V_d - I_d R_c)}{nk_B T}\right] - 1\right) = \frac{V_d}{R_m} + \frac{nk_B T}{eR_c}\varpi\left(\frac{eI_o R_c}{nk_B T}\exp\left[\frac{e(V_d + I_o R_c)}{nk_B T}\right]\right) - I_o \quad (1)$$

Here the expression in the middle is still an implicit function of I_d and must be further solved for V_d. Because the solution is not available in elementary functions, we apply the product-log function to the expression on the right hand side [27]: $y = \varpi(x)$ defined such that $x = y\log(y)$. The first term V_d/R_m is due to the metallic shunt, with R_m corresponding to a characteristic leakage resistance. R_c represents a characteristic resistance of the physical diode. I_oR_c is therefore the voltage drop at the SWNT channel and electrodes, except for that of the junction itself. The junction is characterized by the single parameter I_o. Thus the model has three fitting parameters, besides the ratio $(n k_BT/e)$ which we assume is fixed at a given temperature $T=300K$ and $n=1$ (thus we neglect the trap recombination below). Eq.(1) corresponds to the equivalent circuit shown in figure 6.1d.

The slope at reverse bias is determined by the R_m term. I_o can be dropped here because of its negligible numerical value. This result implies that in our devices the leakage is not due to the thermionic current through the diode junction itself (i.e., the upper path in the equivalent circuit of figure 6.1d is shut-off at $V_d << 0$. We provide full proof next.) For array devices, the slope of the reverse bias wing is very close to linear and unambiguously yields R_m for m-SWNTs. This resistance is an order of magnitude

higher than that for Pd-Pd contacted field effect transistors (FETs) [28] as obtained from known contact resistance and channel resistivity of similarly grown m-SWNTs, the measured channel length and width and estimated number of tubes in the array diode. We attribute this difference to the lower quality of the Ca contact, due at least partly to its poor wetting properties on SWNTs [9,25] and to the higher drain bias applied in the diodes here (up to -2V) compared to that (-0.01 V) used in the transistors in previous work on related transistor devices [28].

At high positive bias, the diode structure is fully open and the physics is also simple: the equivalent circuit contains only R_m and R_c. Theoretically, the product-log function saturates at large arguments: $\varpi(x) \to \log(x) + \dots$. As a result, Eq.(1) reduces to: $I_d \approx \frac{V_d}{R_m} + \frac{V_d}{R_c} - \frac{nk_B T}{eR_c}\log\left(\frac{V_d + I_o R_c}{I_o R_c}\right)$. Thus, the linear slope of the high-bias I-V curve gives us the total device conductance: $\frac{1}{R_{tot}} = \frac{1}{R_m} + \frac{1}{R_c}$. The current cut-off, the point where the linear part of the I-V curve crosses the ordinate axis, with the logarithmic accuracy, is given by: $\frac{nk_B T}{eR_c}\log\left(\frac{nk_B T}{eI_o R_c}\right)$. In this manner, I_o and R_c can be extracted.

For example, figure 6.1e shows the current for single s-SWNT diodes, plotted on a log-scale. The measured leakage current at reverse bias allows us to determine $R_m \sim 1\text{-}40$ GΩ; the linear currents at high forward bias yield $R_c \sim 1\text{-}50$ MΩ, with $I_o \sim$fA or smaller. This observation proves post factum that the leakage current is not due to I_o. We note that at large V_d the diode junction is open and has almost zero resistance. Thus, very little voltage drops at the junction $V_c \sim (n\, k_B T/e) \log(n\, k_B T/eI_o R_c) \sim 0.1\text{-}0.3$ V. The rest of the drop is due to Ohmic losses at the s-SWNT channel and electrodes, except for that of the junction itself. The extracted model parameter R_c is about an order of magnitude higher than similarly fabricated FET devices [28] which we speculate is due to the lower quality of the Ca contact and the higher drain bias applied in the diodes here compared to that applied in previously studied transistors [28], similar to the case of m-SWNT devices. At small bias $V \ll V_c$, the junction resistance becomes very high, on the order of $nk_B T/eI_o \sim$TΩ. In this regime, almost all voltage drops at the junction, and not in the channel or electrodes. The resistance increases further at reverse bias, which must

essentially shut off thermionic conduction through the ideal diode. In a real system we always observe leakage. The origin of the leakage for SWNT devices is unknown. Zener tunneling through the Schottky contact and thermal generation in the field region of the small bandgap SWNTs (<1eV) could explain the leakage current [6,8].

Figure 6.1f shows the rectification (i.e. current at maximum positive bias of 2V divided by the absolute value of the current at minimum bias of -2V) as a function of the current at 2V for the various single m-SWNT resistors and single s-SWNT diodes. The rectification of the single m-SWNT resistors is about 1 while that of the single s-SWNT diodes could be as large as 10^4. We emphasize that according to our analysis, this result is not limited by the internal physical properties of the material. Instead, the rectification, as in other current SWNT devices, is substantially limited by the channel resistance. We conclude that short channel devices should achieve much better rectification and lower resistance.

Having established physical parameters of single SWNT devices, we proceed to analysis of the arrays. Figure 6.2a,b show a schematic illustration of a Schottky diode based on perfectly aligned arrays of SWNTs and an SEM image of an array representative of the type used here. These array diodes were fabricated in a manner similar to the single SWNT devices mentioned earlier but the patterned photoresist covered the entire diodes to protect all SWNTs within the diodes during the etching process. The channel lengths and channel widths of these devices were ~10µm and ~250µm, respectively. The densities of the arrays (measured in SWNTs per micrometer of lateral distance across the channel) were 1 ± 0.5 SWNTs/µm, as determined by the average of SEM measurements at various spots across the surface of the quartz substrate. As a result, if we assume that the ratio of m-SWNTs to s-SWNTs is 1:2, then there are approximately ~83 m-SWNTs and ~167 s-SWNTs in each array SWNT diode. Figure 6.2c shows the diameter distribution of the SWNTs in the arrays, as determined by AFM measurements. The diameter of the SWNTs ranges from ~0.5nm to ~1.7 nm with single counts for tubes with diameters up to 4.8nm which we assume are small bundles of SWNTs. The majority of the SWNTs have diameters between 1.0 and 1.2nm.

Array SWNT diodes were measured with the Al/Ca electrode grounded and the Pd electrode swept between ±2V. A small rectification (~1.5) is observed in these array SWNT diodes. This result is consistent with the significant population of SWNTs that are m-SWNT and act as shunt channels. Assuming that most of the leakage in reverse bias is due to these m-SWNT shunts, and then extracting the s-SWNT channel resistance at large forward bias as explained before, we can fit the array data. Next we compare the currents flowing through the m- and s-SWNTs throughout the range of biases. At reverse bias, m-SWNTs always dominate while at forward bias, we observe two cases (as shown in figure 6.2d,e). In figure 5.2d, the s-SWNTs resistance is approximately half of the m-SWNTs, which is reasonable assuming the ratio of s-SWNTs to m-SWNTs to be about 2:1. On the other hand, in figure 6.2e, these resistances are about the same, which may be due to stronger scattering at the contacts and/or in the channels of s-SWNTs [29-31]. Assuming that our single-SWNT device measurements have sampled sufficiently the random distribution of the SWNT channels in the array devices, we compare in figure 6.2f the experimental array IV curve and the one composed from an average m-SWNT and average s-SWNT IV curves weighted with their abundances in the arrays.

We can increase the rectification in the array devices by electrically breaking down most of the m-SWNTs. After applying V_d~30V, the I-V curve of the device shown in figure 6.3a demonstrates irreversible changes (compare to figure 6.3b before breakdown). Analysis of the device before and after the high-bias sweep indicates that current contributed by both m-SWNTs and s-SWNTs have decreased. However, the metallic-shunt resistance has increased much more significantly as shown in figure 5c. Thus, we speculate that we were able to burn preferentially m-SWNTs, to yield an array diode with good rectification. $\frac{R_m}{R_c}+1$, which also corresponds to the rectification ratio, increased from 1.6 to 29.3 after breakdown. After we applied even more significant bias sweep up to 50V, the s-SWNT channels also break down, and both resistances further increased to yield low ratios (figure 6.3c).

6.3 Conclusions

In conclusion, we present theoretical and experimental studies of diodes based on parallel arrays of SWNTs. A simple physical model takes into account basic physics of current rectification and explains the data. Our analysis is equally applicable to single-tube and array devices though we stress that some aspects of the charge carrier transport need further study, for example, the origin of the SWNT leakage current requires special attention. We show that for as grown array diodes, the rectification ratio, that is the maximum-to-minimum-current-ratio, is low due to the presence of m-SWNT shunts. These tubes can be eliminated in a single voltage sweep resulting in a high rectification array device. Further analysis shows that the channel resistance, and not the intrinsic nanotube diode properties, ultimately limits the rectification. Shorter devices may demonstrate even better performance, with some potential to serve in ultra-miniaturized circuits.

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6.5 Figures

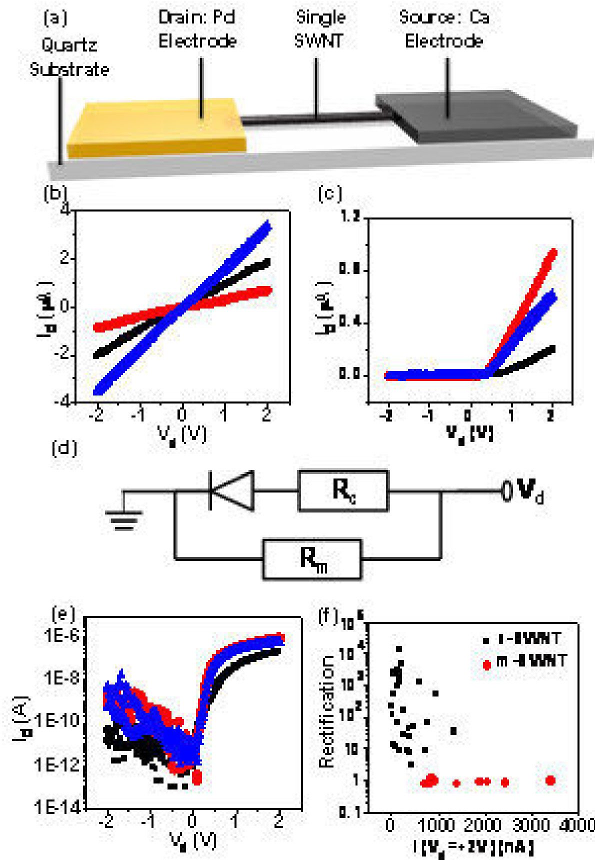

Figure 6.1. (a) Schematic illustration of a single single-walled carbon nanotube (SWNT) device. A single SWNT is contacted on one end by a palladium electrode and by a calcium electrode on the other end. (b) Three representative I-V curves (black, red and blue curves) of three single metallic-SWNT (m-SWNT) resistors. (c) Three representative I-V curves (black, red and blue curves) of three single semiconducting-SWNT (s-SWNT) diodes. (d) Equivalent circuit model of a non-ideal diode and a leakage via a parallel channel. *Rc* represents the Pd contact and channel resistance in series with the diode and *Rm* represents the shunt resistance that contributes to the leakage current. (e) Same I-V curves (black, red and blue curves) as in part (c) shown in log 10 scale. (f) Rectification (i.e. current at V_d=+2V divided by absolute value of current at V_d=-2V) as a function of the current at V_d=+2V for single s-SWNT diodes (black squares) and single m-SWNT resistors (red circles).

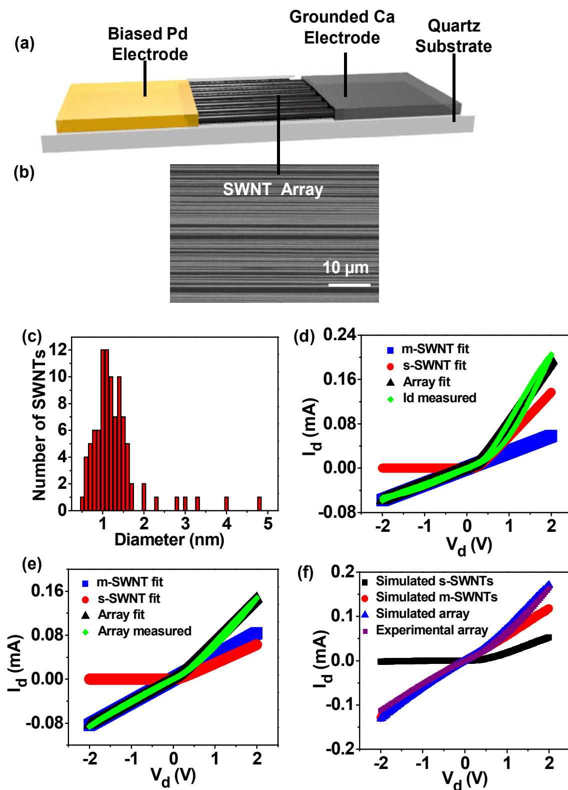

Figure 6.2. (a) Schematic illustration of a Schottky diode based on perfectly aligned arrays of SWNTs with an analogous design that in figure 6.1(a). (b) A SEM image of a representative array of SWNTs is shown in the frame below. (c) Diameter distribution of the SWNTs in the perfectly aligned arrays of SWNTs. (d) I-V curve of an array diode: model (black curve), including the current of the s-SWNTs (red curve) in the array is approximately twice that of the m-SWNTs (blue curve), and the corresponding measured data (green curve). (e) I-V curve of an array diode: model (black curve), including the current of the s-SWNTs (red curve) in the array is about the same as that of the m-SWNTs (blue curve), and the corresponding measured data (green curve). (f) Average current contributed by s-SWNTs (black curve) and m-SWNTs (red curve) in an array diode interpolated from the current of single SWNT devices. Blue curve represents the total average current of the array diode. The purple curve is the I-V curve of a measured array diode.

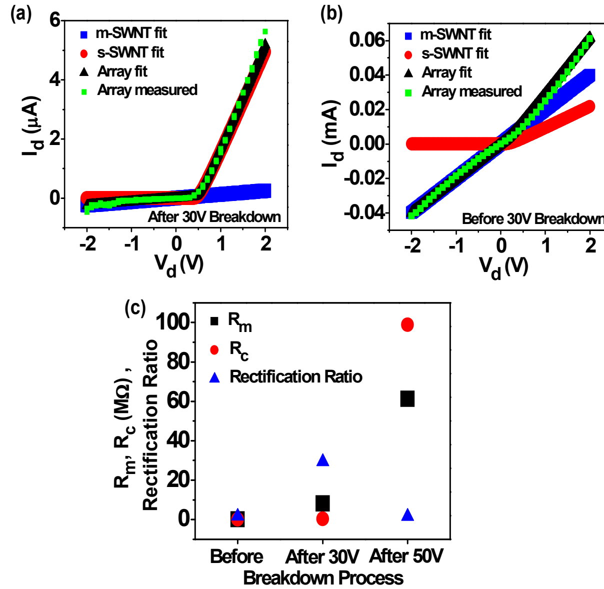

Figure 6.3. (a) I-V curve of an array diode after electrical breakdown by driving the device to V_d=30V: model (black curve), the current of the m-SWNTs (blue curve) is significantly lower than the s-SWNTs (red curve), and the corresponding measured data (green curve). (b) I-V curve of the same array diode as in part (a) before electrical breakdown: model (black curve) with its s-SWNTs (red curve) and m-SWNTs (blue curve) components and the corresponding measured data (green curve). (c) Plots comparing the values of R_m (black square symbols), R_c (red circle symbols) and rectification ratio (blue square symbols) before breakdown, after driving the device to V_d=30V and after driving the device to V_d=50V.

CHAPTER 7:

ELECTROLUMINESCENCE FROM SCHOTTKY DIODES THAT USE ALIGNED ARRAYS OF SINGLE WALLED CARBON NANOTUBES

7.1 Introduction

The electroluminescence (EL) properties of single-walled carbon nanotubes (SWNTs) have attracted wide interest because they can be potentially used to fabricate flexible nano-scale light sources with tunable wavelength. [1,2] Their fabrication is also compatible with the semiconductor technology. In particular, EL from SWNT based light emitting diodes (LEDs), with structures of either field effect transistors (FETs) [3-10] or p-n junctions [11], has been extensively investigated. For the FET based LEDs, EL happens in the ambipolar conduction regime, where electrons and holes simultaneously injected from the contacts recombine in the CNT channel. [3-7] EL also occurs in the unipolar conduction regime through impact excitation, in which case the excess energy of hot carriers generates electron-hole pairs which subsequently recombine radiatively. [9,10] For the p-n junction based LED, p (holes) and n (electrons) regions are formed by electrostatic doping through two split gates. [11] Unlike the FET case where very high drain-source voltages are used in order to inject electrons and holes from the contacts, the p-n junction can independently control the current injection from the p and n regions therefore operating under nearly flat band-condition, resulting in highly efficient and thresholdless LED. On the other hand, however, the p-n junction structure increases the complexity of fabrication and operation because of the additional top gates. It also works effectively only at relatively low current which limits the light output.

Schottky diode is another type of structure suitable for optoelectronics. It is extremely convenient to fabricate because additional doping is not required. Schottky diodes are also two terminal devices which are easy to operate. Previously, the electrical properties of SWNTs based Schottky diodes have been well studied. [12-15] Until recently, Sheng Wang et.al investigated the EL properties from single-SWNT based diodes with Sc-Pd asymmetric contacts. [16] They observed the light emission from the forward biased diodes, which had a narrow emission peak in the spectrum with a full width at half-maximum (FWHM) of about 30meV. However, the spatially resolved EL

image was lacking and the explanation for high threshold voltage/current was somewhat ambiguous.

Here, the electroluminescence from Schottky diode that used aligned arrays of SWNTs is measured. Aligned arrays of SWNTs have the advantages of easy scaling and integration. Since the arrays are ensembles of individual tubes, they can provide device-to-device uniformity by averaging away the differences between tubes. The arrays can also sustain large current therefore having large output. More importantly, aligned arrays of SWNTs are beneficial for the study of basic device properties in a statistical way. Since they consist of various independent individuals, arrays should be able to show us important information on how the EL properties are affected by different factors, like the diameters, defects, contact resistances and interaction between SWNTs. Using the previous Schottky-diode structure based on Ca and Pd asymmetric contacts [12], we found that light emission happens spatially near the Ca/Al contact under forward biased condition. Both the current and the emission intensity increases linearly with the voltage beyond a certain threshold voltage, but the emission onset is larger. This is somehow surprising because we expected the two threshold voltages to be the same. The spectral peaks are broad with the FWHM ranging from 80meV to 120meV, which is much larger than Sheng Wang et.al.'s results. [16] The light emission is mainly due to electron hole recombination [3-7,17-19] near the Schottky contact, while impact excitation [9,10] and black body radiation (BBR) [19-21] may also contribute to the light emission at higher voltages. Development of a model to explain the EL process is ongoing.

7.2 Methods

The upper inset of figure 7.1 shows the device geometry of the Schottky diode and the lower right inset of figure1 is the SEM image of the device. We started by growing perfectly aligned arrays of SWNTs on transparent quartz substrates via chemical vapor deposition (CVD). [22,23] Electrode contacts were defined on the SWNT arrays through photolithography, followed by the metal deposition and the lift-off process. We deposited Ti/Pd (0.2nm/40nm) on one side to form the Ohmic contact and Ca/Al (5nm/30nm) on the other side to form the Schottky contact. The channel length and

channel width was about 10um and 250um, respectively. Detailed process procedures can be found in previous work on Schottky diode [12].

7.3 Results and Discussions

During the operation of the diodes, Ca/Al electrode was grounded and Pd electrode was biased. The IV characteristic of the Schottky diodes in figure 7.1 shows asymmetric conduction between forward bias and reverse bias. This asymmetric current reveals the fact that there are both semiconducting SWNTs and metallic SWNTs in the arrays. The semiconducting SWNTs work as rectifying diodes, with almost no current at reverse bias, and current superlinearly increasing with voltage at low forward bias. Eventually the current increases linearly with voltage after the threshold (~0.5V) because of the series resistance contributed by the SWNT channel. The metallic SWNTs are just shunt resistors, with equal conduction at forward and reverse biases. Combining contributions both from semiconducting and metallic SWNTs, the IV curve shows slight rectification behavior, as shown in figure 7.1.

We used a liquid nitrogen cooled InGaAs infrared camera to collect the light from the back of the transparent quartz. Figure 7.2a to figure 7.2d show the light emission images when the devices were forward biased (Ca/Al electrode grounded and Pd electrode positively biased). The light emission consists of emission spots from individual SWNTs, appearing from ~3V and getting brighter as the voltage is increased. These emission spots are localized at the SWNT-Ca Schottky contact. The Pd contact is dark and highlighted by dotted white lines for clarification. Since the diffraction limit of the IR camera is about ~1.5um and the density of the arrays is about 1~2 SWNTs/µm, we estimate that each emission spot corresponds to one or two SWNTs. Figure 7.2e and 7.2f show the overall light intensity-voltage curve and current-voltage curve, respectively. Both the light emission and current conduction show linear dependence on the voltage after a certain threshold. However, the threshold voltage for light emission is about 2~3V, which is higher than the current threshold voltage at about 0.5V.

There are three possible mechanisms responsible for the light emission, which are radiative recombination from excitons formed by injected electrons and holes (electron hole recombination) [3-7], and recombination from excitons formed from impact

excitation (IE) [9,10], and black-body radiation (BBR) from joule heating [18-21]. In order to clarify the light emission mechanism for the Schottky diodes, we further fabricated and tested the electroluminescence from a hybrid device structure. Figure 7.3a and 7.3b show the schematic illustration of such a structure and its SEM image, respectively. The hybrid structure consists of three two terminal devices: Ca-Ca (left channel), Ca-Pd (middle channel) and Pd-Pd (right channel). The channel length here is about 20um. We connected the Ca/Al electrode to the Pd electrode as shown in figure 7.3a for easy probing.

During light emission collection, the Ca and Pd electrodes on the left in figure 7.3a were biased and the Ca and Pd electrodes on the right were grounded. Figure 7.3c to Figure 7.3h show the spatially resolved EL images for different applied voltages. The polarity and the edge of the electrode are marked in the figures for easy identification. At relatively low bias (figure 7.3c to figure 7.3f), we saw the light emission spots localized at the lower potential contact side for the Ca-Ca devices (i.e. the grounded side when positively biased and the biased side when negatively biased), and the light emission happened near the Ca contact for the Ca-Pd devices when positively biased. For the Pd-Pd devices, we only detected several random emission spots in the channel or near the contact at relatively high voltage (figure 7.3g and figure 7.3h).

Black body radiation from hot SWNTs by joule heating can be ruled out because the emission spots are not located in the channel but at the contact. [18,20] The contact region should be colder than the channel because of additional heat dissipation through the metal electrode. [24] Moreover, the Pt wire calibration we performed shows that the IR camera starts to detect BBR emission around 120 degree celsius. The light emission threshold voltages for the Schottky diodes are about 2.5V~4V. For our long-channel-length devices at a voltage of 2.5V~4V, the temperature hardly rises to the IR camera detectable range. However, at higher voltage and hence higher temperature, the BBR effect appeared in the Pd-Pd device (Figure 7.3g and 7.3h), when the channel started to emit light.

Impact excitation happens when the excess energy of hot carriers transfers to the valence electrons and generates excitons which decay radiatively. [8-10] Therefore, it is more likely to happen at the high field region. [3,18] The reverse biased Schottky contact

has higher field than the forward biased case, but there is no emission from the reverse biased contact. This phenomenon indicates that impact excitation is not the origin of the EL. Moreover, the light intensity should increase exponentially with electrical field during impact excitation**.** [9,25] However, the intensity of the emission spots from the forward biased Schottky contact increased linearly with the voltage, as shown in figure 3i. At high voltage, impact excitation can happen, and the intensity increases superlinearly with voltage beyond the threshold voltage (Figure 7.3i and j).

The light emission from the hybrid devices suggests that the EL is due to the radiative recombination of excitons formed when the minority carriers (electrons) inject from Ca contact and recombine with the majority carriers (holes) in the channel.

We finally investigated the EL spectra of the Schottky diode. A spectrometer with a grating (150 grooves/mm, blaze 1250 nm) was placed before the IR camera to disperse the incoming light. Figure 7.4a shows the spectrally resolved EL image, in which each bright line corresponds to an emission spot in the right picture. We found that most of the lines show a tail like spectrum, only a few of them can be resolved as full peaks. This is because the dispersion range of the spectrometer is from 1200nm (0.78eV) to 1600nm (1.04eV), and the diameters of the SWNTs are mostly in the range of 0.5nm to 1.7nm (corresponding to energy gap from 0.53eV to 1.6eV). Therefore, only a small proportion of semiconducting SWNTs is expected to emit within this window while most of their emission peaks are beyond 1600nm. All the peaks that we observed showed broad FWHM ranging from 80meV to 120meV. Figure 7.4b shows the evolution of a typical EL spectrum with a fully resolved peak (Peak 3 identified in figure 7.4a) under several voltages. The FWHM ~ 120meV and its location at ~0.83eV did not change during the evolution. We also note that the peak intensity scales linearly with voltage beyond the onset, as shown in Figure 7.4c.

The FWHM (~80meV to 120meV) of the peaks in the spectra of our Schottky diodes are comparable with that of network SWNT-FETs (~80meV) [18] and short channel SWNT-FETs (~150meV) [17], but are significantly larger than that of the long channel ambipolar SWNT-FETs (~25meV) [17], SWNT based p-n junction (~35meV) [11] and Sc-Pd short channel diodes (~30meV) [16] reported recently. Previous work attributed the broadening of the peak to the high electrical field. The carriers get high

energy in the high electrical field, and are not able to relax before recombination, resulting in the mixture of exciton and continuum states [25]. Our detected peaks have relatively high threshold voltages, which may induce a high field near the contact and result in peak broadening. Since most of the peaks are out of detection range, it is possible that some of them with low threshold voltage can show narrow emission peaks. Hence, we do not exclude the possibility of finding narrow peaks. Other groups have also attributed peak broadening to phonon broadening [11] and Auger recombination [11,19,25]. Development of a model to explain the peak broadening is ongoing.

7.4 Conclusions

In conclusion, we observe electroluminescence from Schottky-diode structure based on Ca and Pd asymmetric contacts. Light emission occurs spatially near the Ca/Al contact under forward biased condition. Both the current and the emission intensity increases linearly with the voltage beyond a certain threshold voltage, but the emission onset is higher. Modeling is still ongoing to understand the difference in threshold voltage for current and emission intensity. The spectral peaks observed are broad with the FWHM ranging from 80meV to 120meV. Further understanding of the cause for peak broadening is also expected to be achieved through ongoing modeling. The light emission is mainly due to electron hole recombination near the Schottky contact, while impact excitation and black body radiation (BBR) may be involved at higher voltage. The light emitting Schottky diodes demonstrated are easy to fabricate and operate. Further improvements to the diodes can be made by increasing the ratio of s-SWNT to m-SWNT and better control over the chirality and diameter distribution, [26-28] which will improve the electroluminescence yield and uniformity of these near infrared light-emitting diodes.

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7.6 Figures

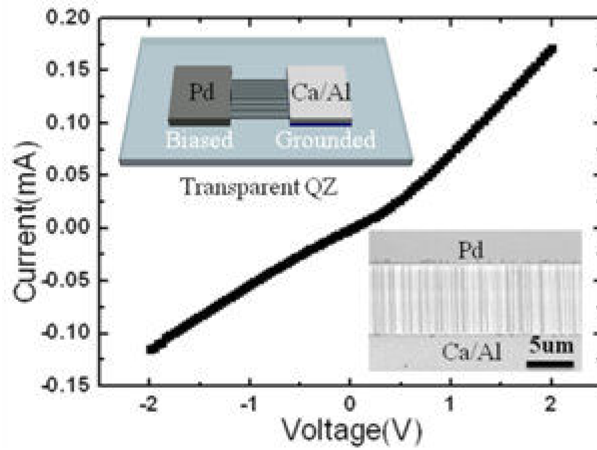

Figure 7.1 IV characteristic of Schottky diodes based on perfectly aligned arrays of SWNTs. There are both s-SWNTs and m-SWNTs in the arrays. The asymmetric current between forward (0.17mA at 2V) and reversed bias (-0.11mA at -2V) is due to the rectification of s-SWNTs, while the m-SWNTs only behave as shunt resistors. Upper left inset is the schematic illustration of the Schottky diodes, with one contact formed by using Ca/Al (Schottky Contact) and the other by Pd (Ohmic Contact). Lower right inset is the SEM image of such devices.

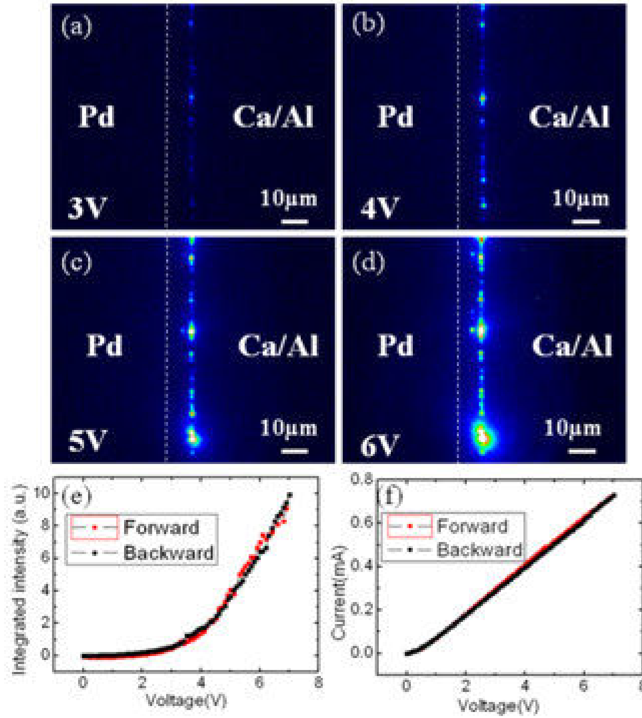

Figure 7.2 (a)-(d) False-color images of infrared emission from Schottky diodes based on aligned arrays of SWNTs at different forward biases. Light emission is located at the Ca/Al contact (Grounded). The white dotted line is used to help identify the Pd contact (Biased). The InGaAs camera has a spatial resolution of about 2um and a sensitivity cutoff at 1600nm. (e) Integrated intensity versus voltage show linear dependence after the onset (about 4V). The devices are forward driven from 0V to 7V with a 0.1V step and then driven backwards. The total data collection time is about 2.5 hours. (f) Current-Voltage characteristic of the Schottky diodes during light emission. The current has a linear dependence on the voltage after the onset at about 0.5V.

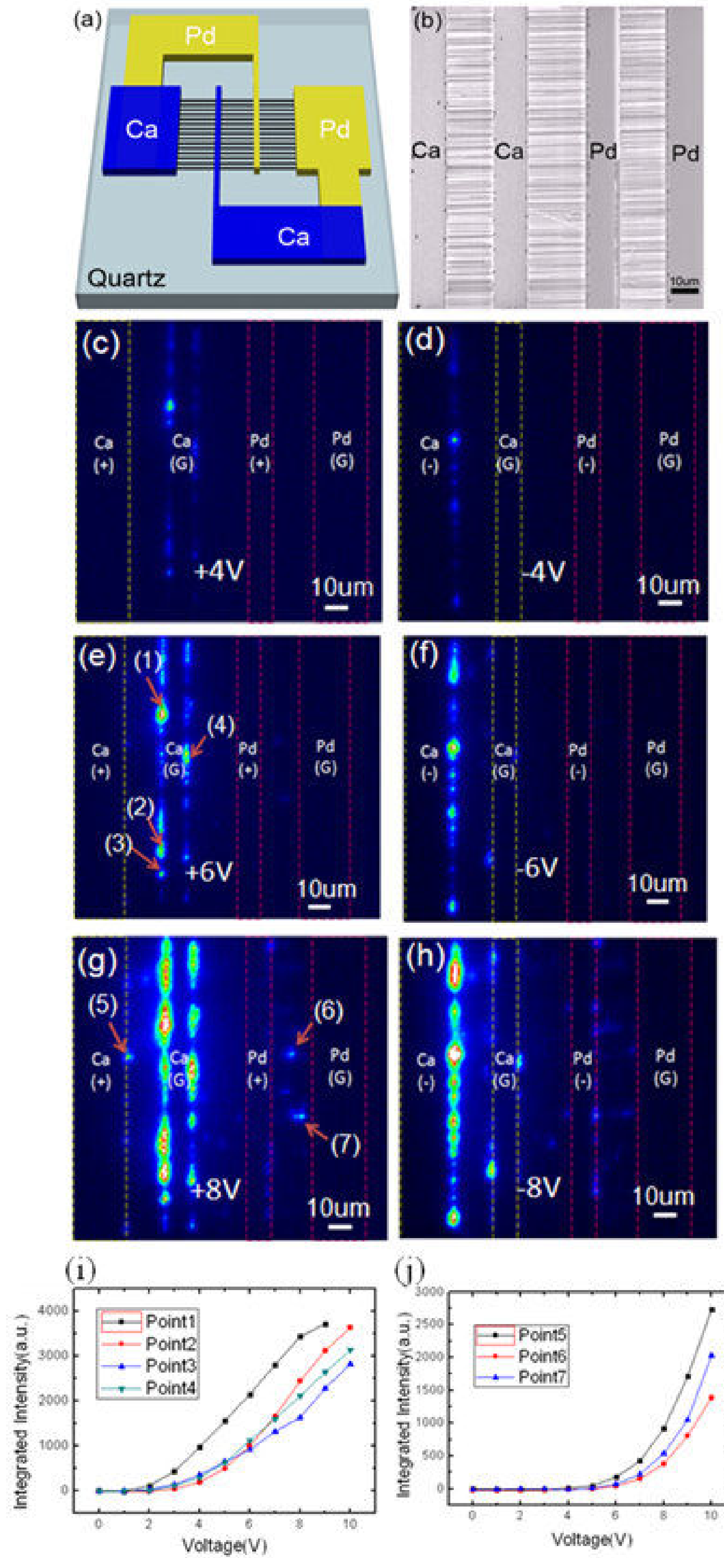

Figure 7.3 (a) Schematic illustration of the hybrid structure which consists of three two terminal devices: Ca-Ca(left channel), Ca-Pd(middle channel) and Pd-Pd(right channel). Figure 7.3 (continued) (b) SEM picture of the hybrid devices shows perfectly aligned

Figure 7.3 (continued): arrays of SWNTs across the channel. (c)-(h) Infrared light emission from the hybrid devices under different bias conditions. (c)(e)(g) light emission at positively biased condition at 4V, 6V and 8V, respectively. (d)(f)(h) light emission at negatively biased condition at -4V, -6V and -8V, respectively. Most of the light emission occurs at the Ca contact with lower electrical potential. Only under high bias, light spots start to appear inside or at the edge of the Pd-Pd channel. (i) Light emission intensity versus voltage for point 1 to point 4, which are identified in part (e), these light emission spots are located at forward biased Schottky contact. (recombination). (j) Light emission intensity versus voltage for point 5 to point 7, which are identified in part (g), these light emission spots are located at reverse biased Schottky contact (point 5) or inside the channel (point 6 and point 7). (impact excitation)

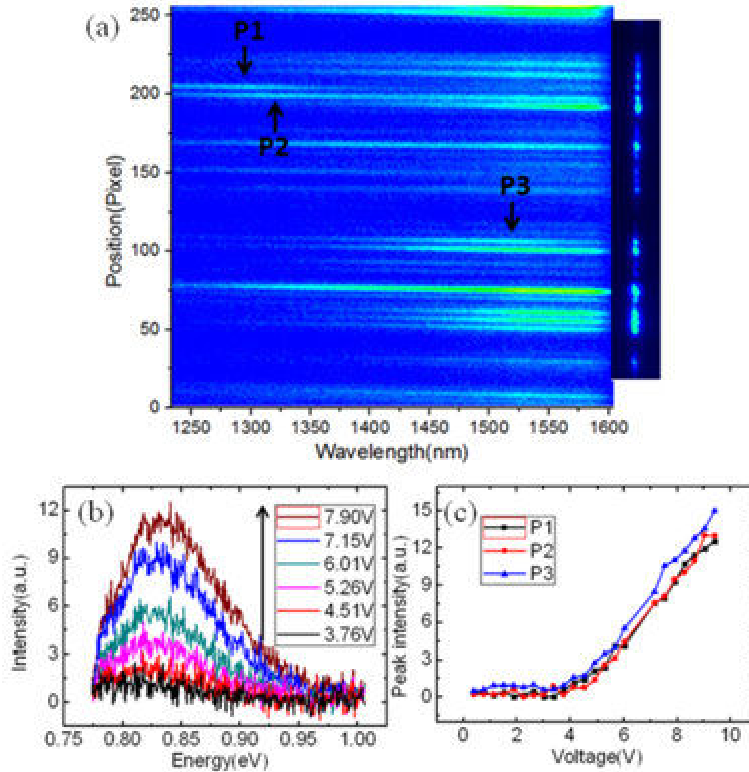

Figure 7.4 (a) Electroluminescence spectra of the Schottky diodes (at 6V). The horizontal axis represents spectrally resolved wavelength and the vertical axis represents spatially resolved position. Each line in the spectra corresponds to a emission spot shown in the right image (b) Spectrum (P3) evolution with voltage, the peak position (at 0.84eV) and FWHM(about 120meV) stays almost the same during the increase of the applied voltage. (c) Peak intensity versus voltage for spectrum peak---P1, P2 and P3, respectively (marked in part (a)). The intensity scales linearly with voltage once after the onset at about 4V.

CHAPTER 8:

SELECTIVE ELIMINATION OF METALLIC SINGLE WALLED CARBON NANOTUBES VIA SELECTIVE LASER ABLATION

8.1 Introduction

Transistors based on single semiconducting single walled carbon nanotubes (SWNTs) are found to have high mobility up to 10,000cm^2/Vs, [1] high transconductance up to 3mS/μm [2] and high on/off ratio, ~10^6. [2] These attractive electrical properties generate an interest in studying SWNTs for use in electronic devices. However, single SWNTs have low current output and have a one-third chance to be a metallic SWNT which cannot be well modulated by the gate in a transistor. Hence, for practical use of SWNTs in transistors, thin films of semiconducting SWNTs (s-SWNTs) are more attractive because the current output will be higher and the absence of metallic SWNTs (m-SWNTs) results in transistors that can be well modulated by the gate. Thin films of SWNTs can come in two formats: random network and aligned array. Transistors based on random network of SWNTs can have high gate modulation despite the presence of m-SWNTs so long as the electrical path between the source and drain has at least one s-SWNT which will determine if that electrical path can be completely turned off when the transistor is at an "off" state. [3,4] Devices based on random network of SWNTs have been considered as alternative semiconducting materials for use in flexible electronics [4] or transparent electronics. [5] However, the tube/tube contacts in random network of SWNTs limit the transport in SWNT networks due to tunneling barriers or electrostatic screening at the contacts to prevent effective gate modulation at those specific points. [6] SWNTs in devices based on aligned arrays of SWNTs, on the other hand, bridge directly between the source and drain and have superior electrical performance, making them attractive in applications with high demand requirements such as RF analog electronics. [7-9] However, the presence of any m-SWNTs can result in leakage current during the "off" state of a transistor based on aligned arrays of SWNTs. Presence of m-SWNTs in RF analog devices contribute to parasitic capacitance which will lower the frequency at which the devices can be operated.

Various methods have been considered to obtain just s-SWNTs [10]: remove m-SWNTs [11-16] or separate m-SWNTs and s-SWNTs [17,18] or grow preferentially s-SWNTs only [19,20]. The techniques to remove m-SWNTs, such as chemical functionalization [11-14] or electrical burnout [15,16], usually breaks down or degrades the s-SWNTs too; resulting in a large decrease in the on current (I_{on}) of the transistors. Separating m-SWNTs and s-SWNTs via density differentiation has been found to be effective but is applicable for solution SWNTs only [17,18]. Solution SWNTs tend to be less pristine and have more defects than SWNTs grown via chemical vapor deposition (CVD) and hence they have poorer electrical properties. [18] Techniques to grow preferentially s-SWNTs have not been very effective as a significant portion of the SWNTs grown are still m-SWNTs. [19,20]

This chapter archives work done to selectively remove m-SWNTs via laser ablation. The Kataura plot relates the energy of the bandgap of a SWNT to its diameter (Figure 1a). A SWNT of a certain diameter can be either metallic M or semiconducting S. It can have several band gaps, conventionally labeled as S_{11}, S_{22}, M_{11}, M_{22}, etc. The S_{nn}, represented by the black symbols, are the bandgaps for semiconducting SWNTs while M_{nn}, represented by the red symbols, are the bandgaps for metallic SWNTs. Hence each SWNT can absorb light of certain energy (or wavelength) better than other energies. Groups have also reported observing absorption and emission from SWNTs and correlating it to their diameters and chiralities [21,22]. A group also reports of preferential destruction of m-SWNTs by laser irradiation using a selected wavelength [23]. Nonetheless, they report that it is difficult to eliminate all the m-SWNTs in the random network of SWNTs.

In our study, we used a 532nm laser to ablate aligned arrays of SWNTs. The green horizontal line in figure 1a shows the energy level of the 532nm laser. It coincides with the bandgap energy of m-SWNTs between ~1 and ~1.3nm and s-SWNTs between ~1.5 and ~2nm and ~0.7nm. Figure 1b shows four different diameter distributions of the SWNTs on four different spots of the same substrate. The diameter distributions can vary significantly across the substrate which can result in inconsistent ablation results from device to device. Majority of the SWNTs are smaller than 1.5nm, so there will not be many s-SWNTs between ~1.5nm and ~2nm removed. s-SWNTs that are as small as

0.7nm carry very little current, so the contribution from them is small. Hence, laser ablation using 532nm laser looks promising. However, we observe from our studies that transistors, based on SWNTs that have undergone selective laser ablation, do not have very high on to off current ratio (I_{on} / I_{off} ratio). This is possibly because the m-SWNTs at other diameters besides ~1 to ~1.3nm do not absorb the 532nm laser energy very effectively and thus are not ablated. These m-SWNTs can contribute to a significant amount of leakage current, resulting in transistors with low I_{on} / I_{off} ratio. If a higher laser power was used to ablate these m-SWNTs, more s-SWNTs will be ablated too, resulting in very low current output.

8.2 Methods

Figure 2 shows the experimental setup. A microchip laser emitting pulsed laser beam at a frequency of 7kHz is used. The pulse width is 1ns. The polarizing beam splitter splits the incoming beam from the laser, allowing light that is polarized along the long axis of the SWNTs to be transmitted. The aluminum beam shutter, placed in the path of the beam, has various thicknesses on different parts of it and allows a controlled fraction of the beam to pass through. A 10x microscope objective is used to focus the laser beam onto the substrate with SWNTs, which is on a moveable stage, to achieve high intensity.

By varying the thickness of the aluminum on the beam shutter, various powers of light is used to ablate the SWNTs. The SWNTs are ablated by varying degrees as shown in figure 3. The SEM images show that the SWNTs are ablated by a little in the bottom right SEM, ablated more in the bottom centre SEM and completely ablated in the bottom left SEM. The intensities used were 0.6, 0.7 and 1.0MW/mm^2 respectively.

Using these selectively ablated aligned arrays of SWNTs as the semiconducting material, we fabricated transistors as shown in figure 4a. The source and drain electrodes, both defined by photolithography and liftoff on the arrays were Pd (30 nm) / Ti (2 nm). A layer of hafnium oxide (HfO_2) was deposited on top of these structures next, forming the gate dielectrics. Finally, gate electrodes (Au (30 nm)/ Ti (2 nm)) were defined by photolithography and liftoff.

8.3 Results and Discussions

Figure 4b and 4c show the transfer curves of transistors based on the ablated aligned arrays of SWNTs. The transistor in figure 4b has low I_{on} / I_{off} ratio (~5) and high on current (I_{on} ~ 2mA at V_g = -2V) as many SWNTs were not ablated when low power of light was used. Meanwhile, the transistor in figure 4c has higher I_{on} / I_{off} ratio (~100) and lower on current (I_{on} ~ 0.01mA at V_g = -2V) as many SWNTs were ablated when high power of light was used.

Figure 5a shows the I_{on} / I_{off} ratio (y-axis on the left), represented by the black symbols, and I_{on} (y-axis on the right), represented by red symbols, as a function of laser power. The higher the power of the laser beam used for ablation, more m-SWNTs and some s-SWNTs will be ablated; resulting in higher I_{on} / I_{off} ratio but lower I_{on}. The results shown in figure 5a are not repeatable. This is because there is a strong dependence of light absorption on the diameter of the SWNT as discussed earlier and the diameter distribution of SWNTs that we grow is not well controlled.

A possible reason why it is difficult to achieve transistors with very high I_{on} / I_{off} ratio up to 10^3 or 10^4 is that a very small proportion of m-SWNTs are allowed to be in such transistors. Panels b, c and d of figure 5 show the distribution of I_{on} , I_{off} and I_{on} / I_{off} ratio distributions of 5000 devices with 1000 SWNTs which the fraction of semiconducting SWNTs are 0 (cross symbols), 0.67 (open circle symbols), 0.9 (dot symbols) and 1 (triangle symbols) respectively. These distributions are simulated distributions based on 139 single SWNT transistors fabricated and measured. By randomly picking out a certain number of s-SWNTs and m-SWNTs with replacement and summing up their transfer curves, transfer curves of array devices can be simulated. The I_{on} and I_{off} can then be extracted from these transfer curves. The I_{on} / I_{off} ratio can be calculated from the extracted I_{on} and I_{off}. As the fraction of s-SWNTs in the array increases from zero to one, both the I_{on} and I_{off} decrease. The I_{off} only decreases to negligibly small value when the fraction of s-SWNTs is one. When the fraction of s-SWNTs is 0.9, there is still a substantial I_{off}. Hence, when the fraction of s-SWNTs is 0.9, a low I_{on} / I_{off} ratio (~15) is obtained. Only when the fraction of s-SWNTs is one, does the I_{on} / I_{off} ratio increases to very high values above 10^4. In the transistors based on highly

ablated SWNTs where the I_{on} / I_{off} ratio is ~ 100, the fraction of s-SWNTs can be more than 0.9. Hence, achieving transistors with high I_{on} / I_{off} ratio is very challenging.

8.4 Conclusions

In conclusion, selective ablation of m-SWNTs in aligned arrays of SWNTs is very challenging because of the varying diameter distribution of SWNTs across the substrate and across batches of SWNTs grown. This results in inconsistent electrical performance of transistors based on SWNTs that have undergone selective laser ablation. In addition, to achieve transistors with very high I_{on} / I_{off} ratio, very small proportion of m-SWNTs are allowed to be present. This is very difficult to achieve as not all m-SWNTs absorb the same wavelength of light very effectively. Some s-SWNTs also absorb at the same wavelength of light as certain m-SWNTs, which results in undesired ablation and / or degradation of s-SWNTs too. Hence, further work to grow SWNTs with a narrow distribution is essential. Many groups have reported that the catalyst size, which can be controlled by catalyst pre-treatment, determines the diameter of SWNTs. [24-26] Nonetheless, it remains a challenge to control the catalyst size very precisely, which will yield a very narrow diameter distribution of SWNTs. Further work in this area will be valuable.

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8.6 Figures

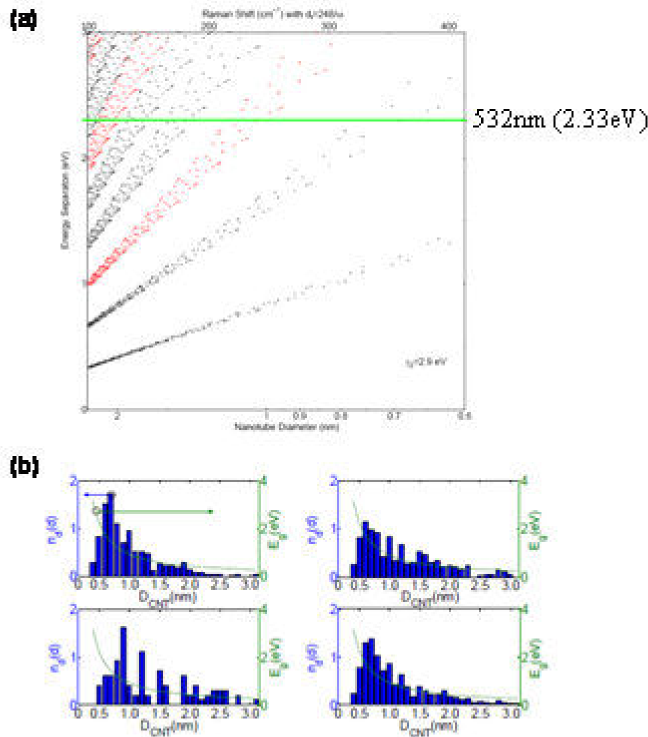

Figure 8.1: (a) Kataura plot relating the energy of the band gap in a carbon nanotube to its diameter. A nanotube of certain diameter can be either metallic M or semiconducting S. It can have several band gaps, conventionally labeled as S_{11}, S_{22}, M_{11}, M_{22}, etc. The S_{nn}, represented by the black symbols, are the bandgaps for semiconducting nanotubes while M_{nn} , represented by the red symbols, are the bandgaps for metallic nanotubes. The green horizontal line shows the energy level of the 532nm laser. (b) Normalized diameter distributions of aligned arrays of single walled carbon nanotubes (SWNTs) on four different spots of a substrate, measured using atomic force microscope (AFM).

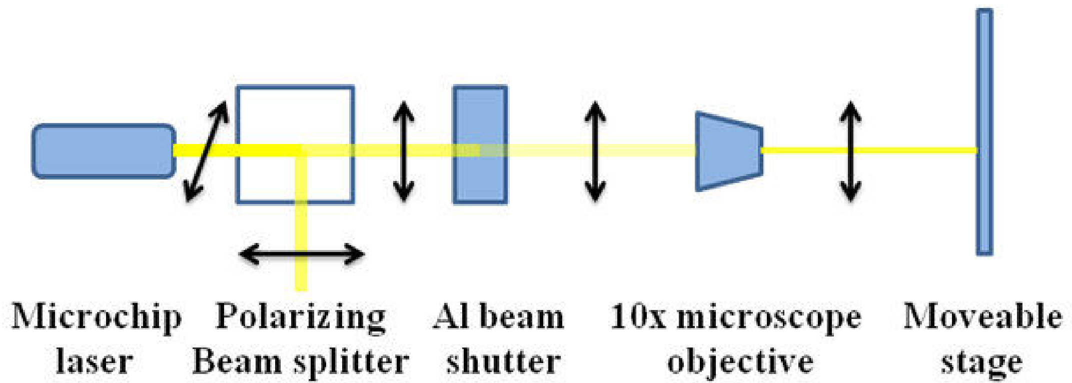

Figure 8.2: Experimental setup. Microchip laser used emits pulsed laser beam at a frequency of 7kHz. The pulse width is 1ns. The polarizing beam splitter splits the beam, allowing light that is polarized along the long axis of the SWNTs to be transmitted. The aluminum beam shutter has various thickness on different parts of it and allows a controlled fraction of light to pass through. The 10x microscope objective is used to focus the laser beam onto the substrate with SWNTs, which is on a moveable stage, to achieve high intensity.

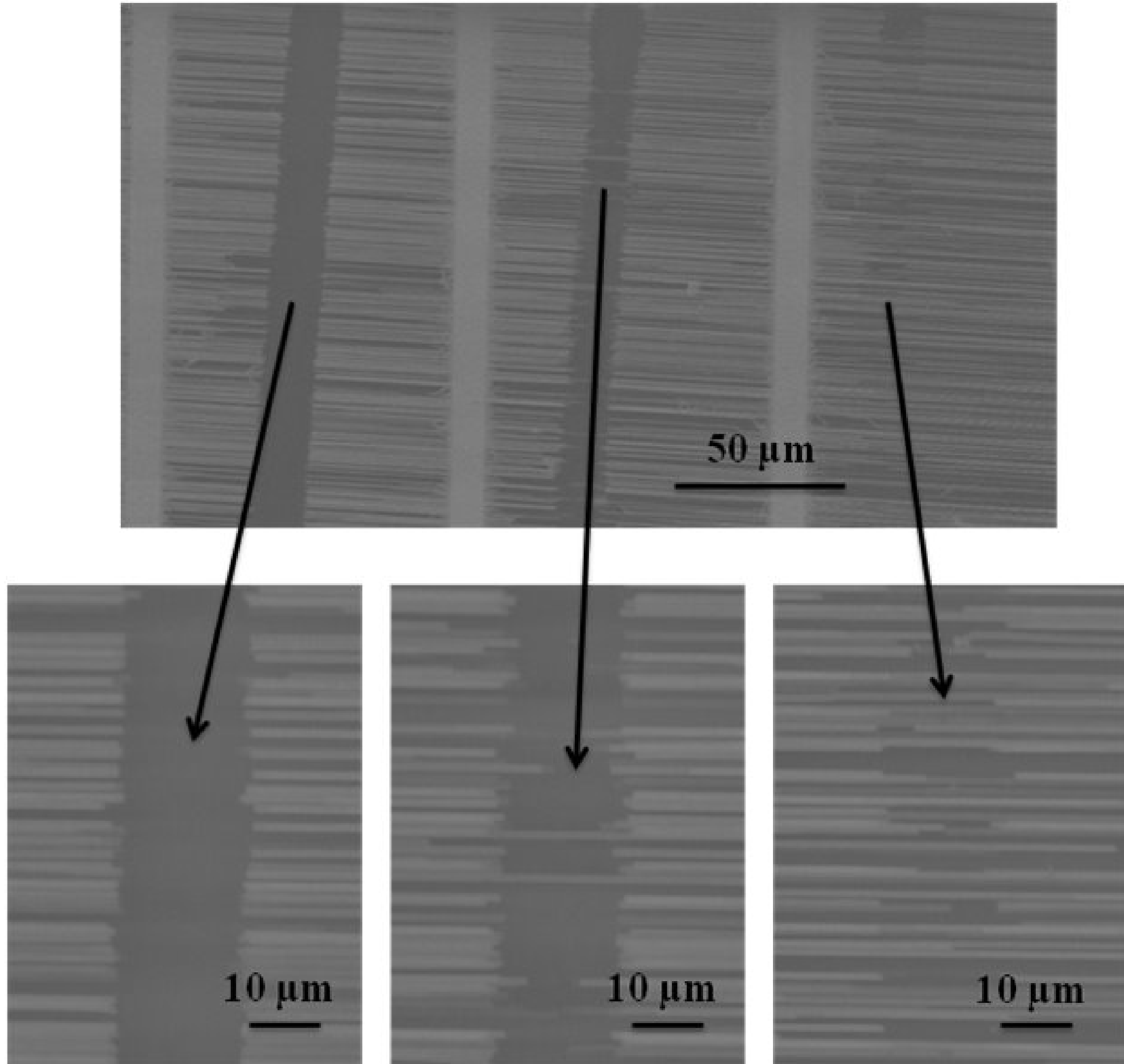

Figure 8.3: Scanning electron microscope (SEM) images of SWNTs ablated by various degrees. The power of light that is transmitted to the substrate can be changed by varying the thickness of the Al beam shutter. Hence, the SWNTs are ablated by different extents. To ablate the SWNTs in the image on the left, centre and right, $1.0 MW/mm^2$, $0.7 MW/mm^2$ and $0.6 MW/mm^2$ intensity of light was required respectively.

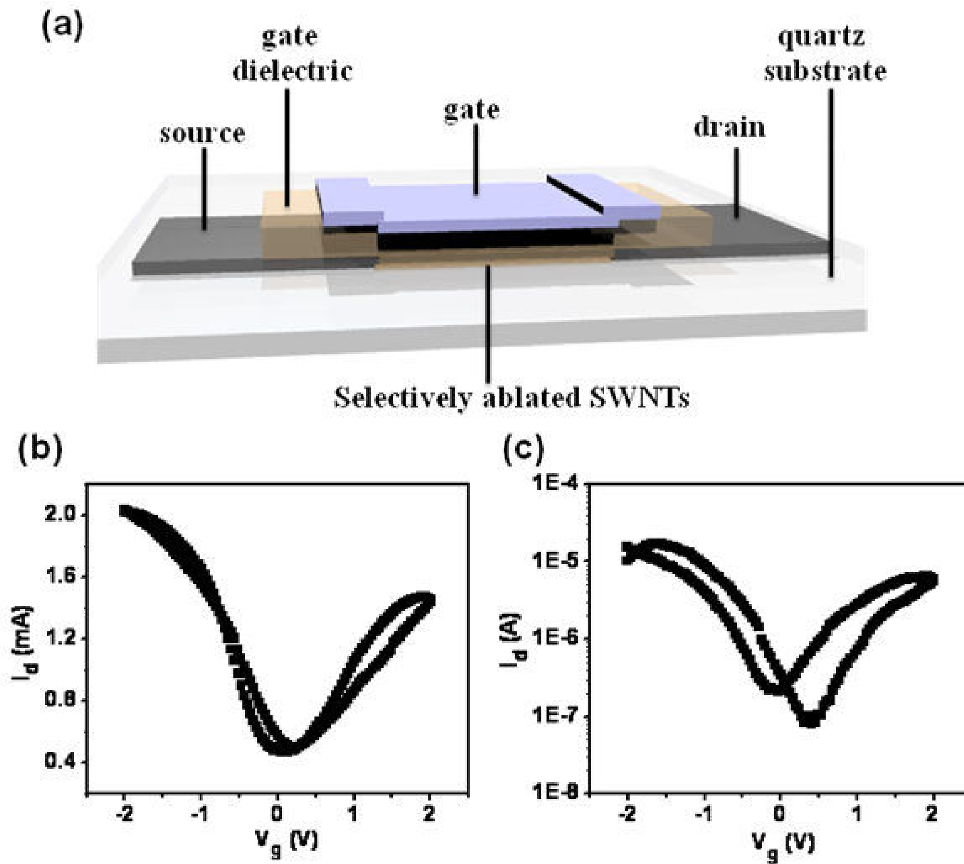

Figure 8.4: (a) Schematic illustration of a transistor based on the selectively ablated aligned arrays of single-walled carbon nanotubes (SWNTs). (b) Transfer curve of a transistor with low gate modulation and high current where V_s = -0.5V. (c) Transfer curve of a transistor with higher gate modulation and low current where V_s = -0.5V.

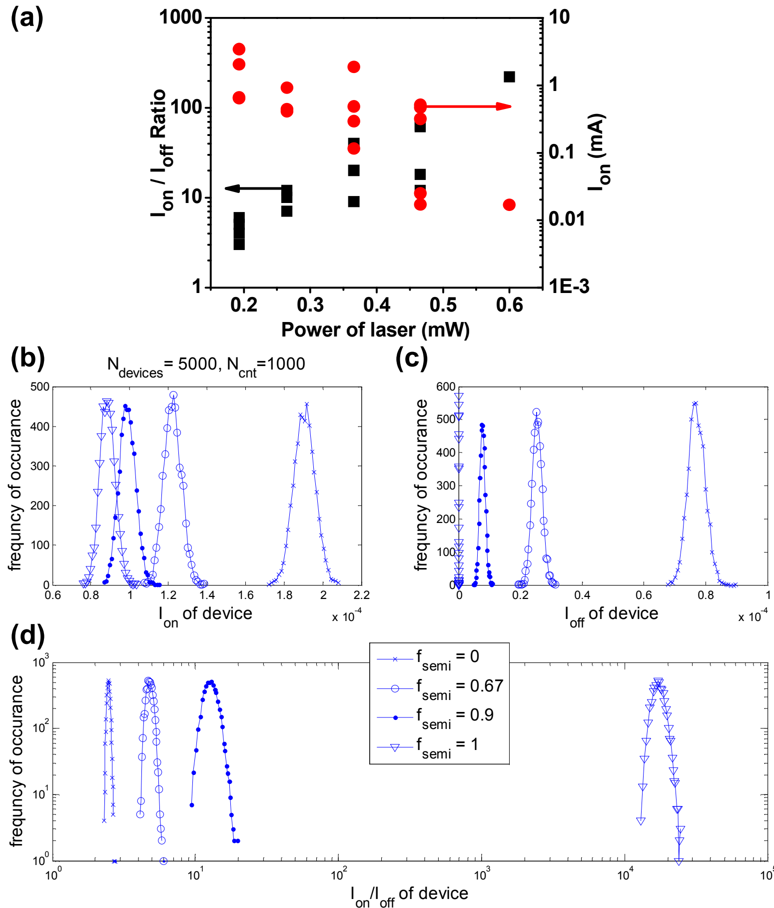

Figure 8.5: (a) I_{on} / I_{off} ratio (y-axis on the left) as a function of laser power, represented by black symbols. I_{on} (y-axis on the right) as a function of laser power, represented by red symbols. (b) I_{on} distribution of 5000 devices with 1000 SWNTs which the fraction of semiconducting SWNTs are 0 (cross symbols), 0.67 (open circle symbols), 0.9 (dot symbols) and 1 (triangle symbols). (c) I_{off} distribution of 5000 devices with 1000 SWNTs which the fraction of semiconducting SWNTs are 0 (cross symbols), 0.67 (open circle symbols), 0.9 (dot symbols) and 1 (triangle symbols). (d) I_{on} / I_{off} ratio distribution of 5000 devices with 1000 SWNTs which the fraction of semiconducting SWNTs are 0 (cross symbols), 0.67 (open circle symbols), 0.9 (dot symbols) and 1 (triangle symbols).

CHAPTER 9:

CONCLUSIONS AND OUTLOOK

9.1 Conclusions and Outlook

Transistors based on single semiconducting single-walled carbon nanotubes (SWNTs) have been demonstrated. They are found to have high mobility (10,000 cm2/Vs) [1], high transconductance (up to 3mS/μm) [2] and high on/off ratio (~10^6) [2]. However, for practical applications of SWNT based devices, thin films of SWNTs are more feasible because of their higher current output and easier integration into devices than transistors based on single SWNTs. Statistical averaging in thin films of SWNTs is also expected to decrease the device to device variations in electrical performance. There are two main types of thin films of SWNTs: random network and aligned arrays.

For applications requiring exceptionally high performance such as RF analog electronics [3,4], aligned arrays of SWNTs are preferred over random network of SWNTs. The SWNTs in aligned arrays do not intersect one another, unlike in networks of SWNTs. Hence, tube/tube contacts, which limit the transport in SWNT networks due to tunneling barriers or electrostatic screening at the contacts to prevent effective gate modulation at those specific points, are absent [5].

Nonetheless, challenges still remain for these aligned arrays of SWNTs before their successful integration into electronic devices for large scale commercial use. The main challenges include (1) selective elimination of m-SWNTs, (2) increasing the density of SWNTs, (3) achieving electronic uniformity across devices fabricated and (4) understanding their mode of operation and the role of contacts in their operation.

This thesis has examined the first, third and fourth challenges aforementioned in detail. We find that as the SWNTs bridge directly between the source and drain of a device using aligned arrays of SWNTs, the presence of metallic-SWNTs (m-SWNTs) results in a high leakage current which makes the device unsuitable for logic applications. In RF analog devices, the presence of m-SWNTs contributes to parasitic capacitance that decreases the frequency at which the devices can operate. The control of the density and diameter distribution of the array SWNTs are also very crucial as is evident from chapter 2. The large variation in density and diameter distribution of array SWNTs results in

significant device to device variations even when there is a large number of SWNTs in an array device. Hence for the successful implementation of devices based on arrays of SWNTs, elimination of m-SWNTs and better control of the density and diameter distribution of SWNTs are essential.

Elimination of m-SWNTs has been extensively investigated by various groups. In an assembly of SWNTs, approximately one-third of them are m-SWNTs and the remaining two-third are semiconducting-SWNTs (s-SWNTs). There have been various techniques employed to either eliminate the m-SWNTs after they are grown [6-8] or to grow predominantly s-SWNTs films [9]. All these techniques have their own varying degrees of success to overcome the problem of the presence of m-SWNTs. However no one method is able to produce purely s-SWNTs films which SWNT structure is pristine and of high quality. Hence, there is still a need to develop a technique that can effectively produce films of high quality s-SWNTs.

Attempts to control the diameter distribution of SWNTs have also been studied by various groups. It has been reported that diameter distributions and possibly chiralities of SWNTs can be influenced by the size [10-15] and composition [16-19] of catalysts used in the CVD growth of SWNTs. Success in eliminating m-SWNTs and controlling density and diameter distributions of SWNTs will lead to the path of integrating a dense array of small diameter distribution of s-SWNTs in devices which are of very uniform and excellent electrical performance.

9.2 References

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