# Study of multi-channel wideband receiver architectures.

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# Contribution à l'étude des architectures de récepteurs large bande multi-canaux

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# Summary

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# Résumé

Cette thèse est le fruit d'un partenariat entre la BL TVFE de NXP Semiconductors à Caen et l'ESIEE à Paris dans le cadre d'une thèse CIFRE. Le but est d'apporter une solution qui permette la réception simultanée de plusieurs canaux pour le câble.
L'émission de la télévision est caractérisée par l'utilisation de larges canaux fréquentiels. Ainsi, la transmission de plusieurs canaux pour la télévision implique un spectre d'autant plus large. Une fonction *tuner* est actuellement directement implémentée sur la carte principale grâce à une solution totalement intégrée que sont les *Silicon Tuners*. NXP est l'un des leaders dans ce domaine. Cependant, c'est la réception simultanée de plusieurs flux de données qui sera la clé des produits du futur, pour la réception de la télévision par câble, satellite et par voie terrestre. C'est une caractéristique nécessaire pour avoir la possibilité de regarder une chaîne et d'en enregistrer une autre en même temps, ou la fonction Picture in Picture (PiP) par exemple. La tendance actuelle est de pouvoir recevoir plusieurs types de données grâce à un récepteur unique, une passerelle domestique (*Home Gateway*).

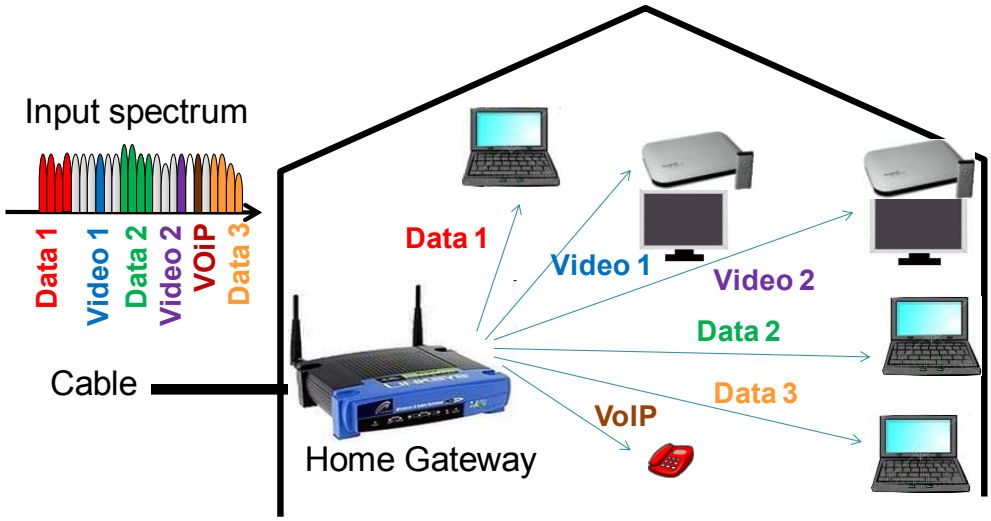


**Fig. 1 - Passerelle domestique**

Ceci implique la réception simultanée de plusieurs canaux situés aléatoirement dans toute la bande ou dans une partie de la bande RF. Pour recevoir ces canaux en même temps, il faut soit numériser toute la bande, soit implémenter autant de tuners de que chaînes que l'on souhaite recevoir. Le spectre correspondant à cette application s'étend de 50MHz à 1GHz et un cas d'usage serait de recevoir simultanément jusqu'à 16 canaux de 6MHz. Il est évident que l'implémentation de 16 tuners intégrés serait très coûteuse en termes de prix et de consommation. Il est donc crucial de rechercher des solutions qui permettent de numériser toute la bande de 1GHz. Pour réaliser une numérisation très large bande et très haute fréquence, un échantillonnage RF sera effectué le plus tôt possible dans la chaîne de réception, ce qui va limiter les composants RF et permettre une flexibilité au niveau de la sélection de l'information pertinente dans le domaine numérique (radio logicielle ou cognitive).
Cette recherche de flexibilité a un coût, notamment au niveau du Convertisseur Analogique-Numérique (CAN), point bloquant de la chaîne de réception, qui doit convertir une très large bande, à très haute fréquence (>2Gsps), avec une forte précision (>10 bits).
En effet, les performances des CAN classiques sont insuffisantes pour ce type de numérisation. Il est difficile d'avoir simultanément une vitesse élevée et une forte résolution.

La figure ci-dessous présentée dans la partie 1, montre les performances que nous souhaitons obtenir par rapport à un bref état de l'art des CAN classiques.

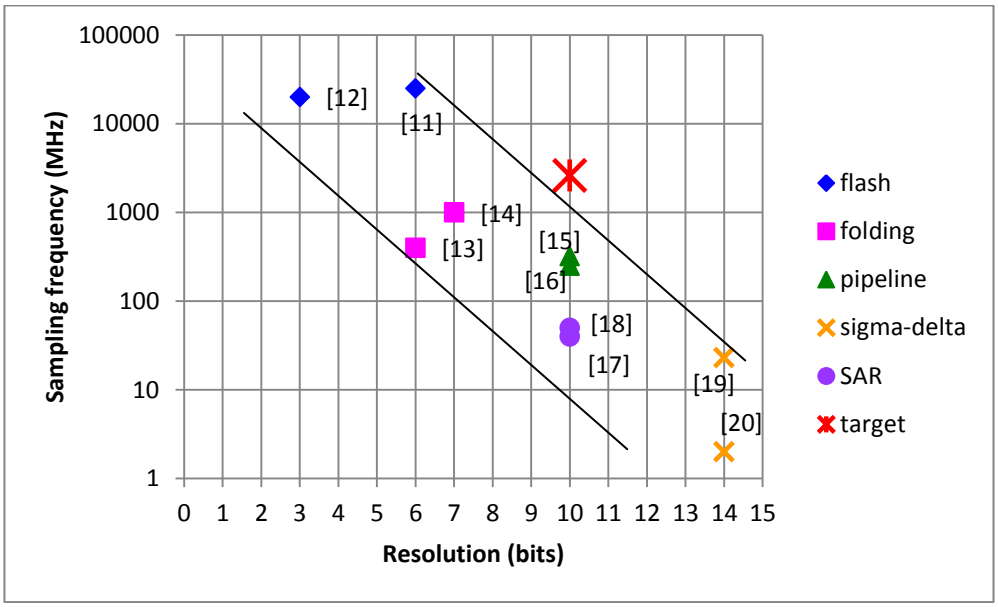


**Fig. 2 - Exemple d'état de l'art des CANs**

D'après la littérature, les architectures parallèles semblent être une bonne solution à ce problème, comme l'entrelacement temporel et les bancs de filtres hybrides [1], présentés dans l'état de l'art de la partie 2. Une autre piste que nous proposons est de réduire les contraintes en divisant le spectre d'entrée en sous-bandes qui peuvent contenir un ou plusieurs canaux. Pour ce faire, il suffirait d'associer un banc de filtres analogiques et un banc de CANs. Une étude de cette architecture est réalisée dans la Partie 3 du manuscrit, ainsi que de plusieurs architectures utilisant différentes méthodes d'échantillonnage, comme l'échantillonnage passe-bande et l'échantillonnage complexe. L'échantillonnage passe-bande n'est pas adapté à notre cas car nous montrons qu'il faudrait découper notre spectre d'entrée large-bande en plus de 20 sous-bandes, ce qui aurait un coût non négligeable. En revanche, l'échantillonnage complexe permet de réduire la fréquence d'échantillonnage par deux, ce qui est avantageux dans une application large-bande. Il faut évaluer le coût des filtres polyphases ajoutés ainsi que du nombre de CANs qui est doublé. Une telle solution, basée sur l'utilisation des signaux analytiques et d'une conversion de fréquence semble intéressante, comme représenté sur la figure suivante :

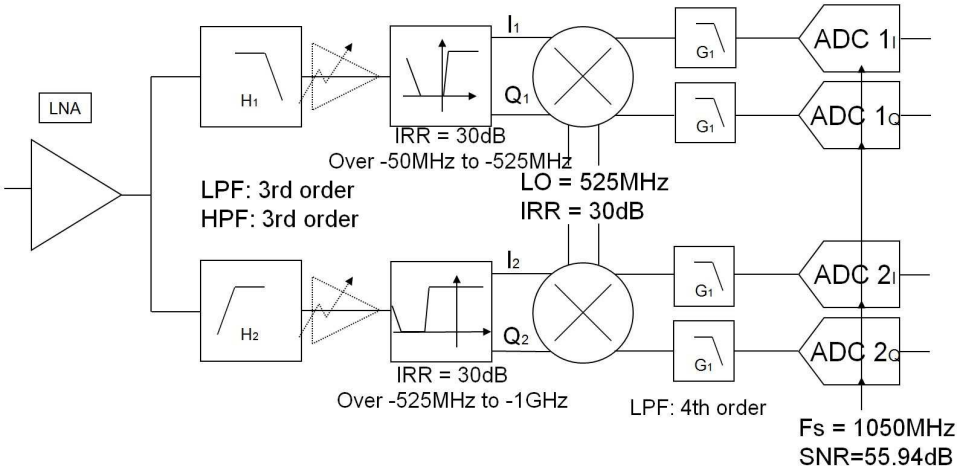


**Fig. 3- Architecture proposée**

La fréquence d'échantillonnage est unique et commune à tous les CANs. Elle est également le double de la fréquence des oscillateurs locaux, ce qui simplifie la génération des fréquences. Le banc de filtres analogiques est composé de simples filtres elliptiques d'ordre 3, et les filtres polyphases ont des spécifications que l'on retrouve dans l'état de l'art. Cependant, la question du coût de cette architecture se pose et nous avons donc proposé d'introduire une fonction de coût générale qui relie la surface et la consommation, afin de comparer l'architecture proposée avec un CAN large-bande très haute performance, proche de nos spécifications. Ceci a été présenté à EuMW [2]. L'un des avantages de cette architecture est que tous les composants sont réalisables, même les CANs, et qu'il est possible d'éteindre des sous-bandes pour diminuer la consommation. Cette solution est intéressante pour le moment mais n'est pas compétitive en termes de consommation et de surface.
Nous proposons une alternative dans la partie 4, avec les Bancs de Filtres Hybrides (BFH). Nous étudions cette architecture, en gardant à l'esprit la faisabilité de la solution. Nous avons choisi un BFH à deux voies, avec un filtre analogique passe-bas et un passe-haut de type Butterworth et d'ordre 3 afin de limiter leurs coûts.

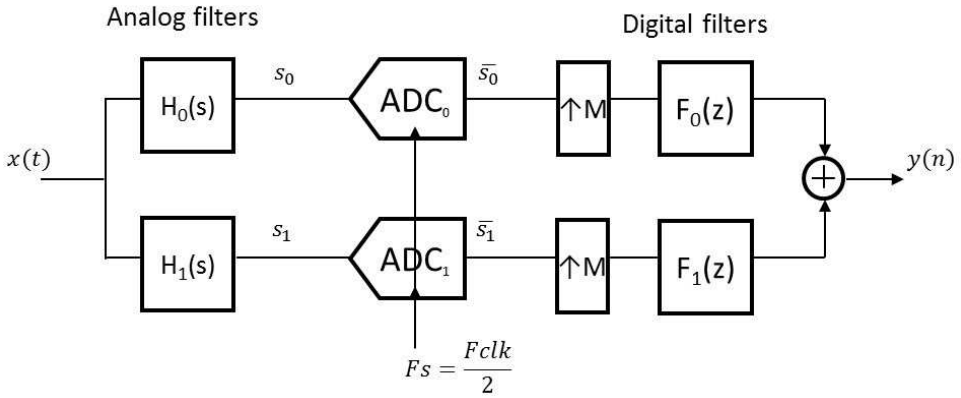


**Fig. 4 - BFH à 2 voies**

La fréquence d'échantillonnage des CANs est $Fs = \frac{Fclk}{2}$ et le système est régi par les équations suivantes :

$$Y\left(e^{j\omega Tclk}\right) = G_{TF}(j\omega).X(j\omega) + G_{AF}(j\omega).X\left(j\omega - j\frac{\pi}{Tclk}\right)$$

$$G_{TF}(j\omega) = H_0(j\omega).F_0\left(e^{j\omega Tclk}\right) + H_1(j\omega).F_1\left(e^{j\omega Tclk}\right)$$

$$G_{AF}(j\omega) = H_0\left(j\omega - j\frac{\pi}{Tclk}\right).F_0\left(e^{j\omega Tclk}\right) + H_1\left(j\omega - j\frac{\pi}{Tclk}\right).F_1\left(e^{j\omega Tclk}\right),$$

où $X(j\omega)$ et $Y\left(e^{j\omega Tclk}\right)$ sont les transformées de Fourier de l'entrée $x(t)$ et de la sortie $y(n)$ du système. $G_{TF}$ et $G_{AF}$ sont les fonctions de transfert et de repliement, respectivement.
Le but de cette architecture est de numériser l'entrée $x(t)$, tel que l'on ait la sortie :

$$Y\left(e^{j\omega Tclk}\right) = K \times X(j\omega),$$

à un gain et un déphasage linéaire près.
Pour cela, nous souhaitons avoir une fonction de transfert $G_{TF}$ constante, ou même égale à 1, et une fonction de repliement $G_{AF}$ nulle. Ceci dépend bien entendu du choix des filtres analogiques et numériques.

Nous proposons un nouvel algorithme d'optimisation des filtres numériques, dits de synthèse, qui utilise à la fois les méthodes de Nelder-Mead et minimax, ainsi qu'une stratégie de perturbation pour éviter les minima locaux. Le critère $J$ à minimiser est ainsi :

$$J(F_0, F_1) = (|G_{TF}(j\omega)| - 1)^2 + \beta |G_{AF}(j\omega)|^2,$$

où $\beta$ est un coefficient qui donne plus d'importance à la réjection du repliement, qui est la plus difficile à minimiser. Le schéma de principe de cet algorithme est indiqué ci-dessous :

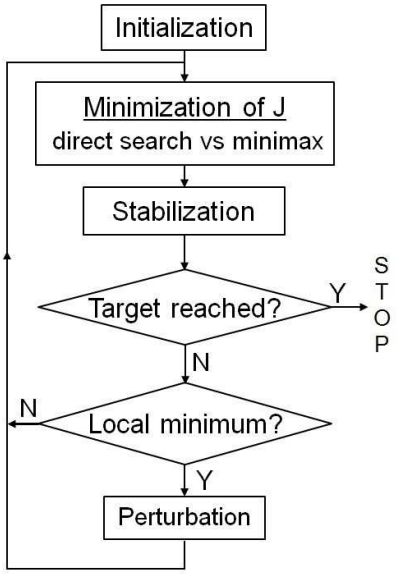


**Fig. 5 - Algorithme d'optimisation**

Nous nous sommes également intéressé au problème de la calibration, c'est-à-dire l'identification des filtres analogiques réels, et nous mettons en évidence l'impact de l'identification et des erreurs de mesure sur les performances de l'architecture. Ces résultats ont été présentés à Newcas [3]. Enfin, nous nous sommes attaché à réaliser un prototype d'une solution à base de BFH. Cette réalisation physique démontre la faisabilité de ce concept de réjection de repliement mais confirme aussi la sensibilité de cette architecture aux imperfections analogiques (ECCTD [4]).

Pour cela, une carte avec deux CANs qui travaillent chacun à 75Msps et une carte avec un FPGA ont été utilisées, et les deux filtres analogiques ont été implémentés sur une troisième carte. Les mesures ont été réalisées sur une bande spectrale plus basses fréquences, pour s'adapter aux contraintes matérielles, mais cela permet tout de même de prouver le concept.

Dans l'exemple ci-dessous, une sinusoïde de fréquence 36MHz est appliquée à l'entrée. Une raie correspondant au repliement est attendue à la fréquence 39MHz, à cause du sous-échantillonnage local. Celle-ci se trouve atténuée de plus de 75dB, ce qui correspond à l'objectif que nous nous étions fixé.

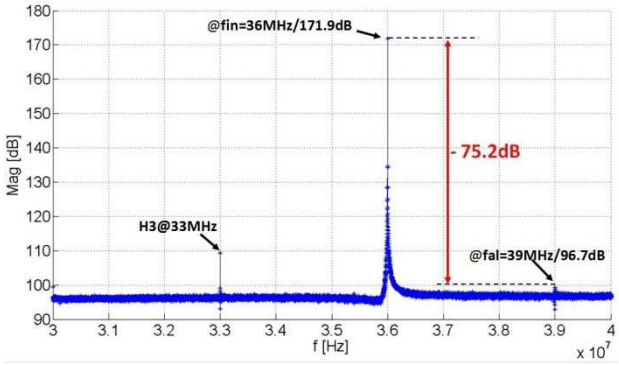


**Fig. 6 - Module de la FFT (en dB) après reconstruction**

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Le travail technique de cette thèse a débuté par l'étude des architectures présentées dans la partie 3, basées sur un banc de filtres analogiques et d'un banc de CAN, puisque nous n'avons pas trouvé cette architecture dans la littérature. Cette étude, en sus de la familiarisation avec le contexte et la littérature, a duré environ un an. L'étude des BFH a également duré environ un an, et a précédé la réalisation du prototype, qui a quant à elle pris environ neuf mois. Il nous paraissait très important de conclure par une réalisation démontrant que les objectifs, en termes de performances, pouvaient être obtenus. Ceci s'est révélé techniquement très ardu et la rédaction n'a pas pu être terminée dans les temps. J'ai commencé une nouvelle aventure dans une start-up quelques jours à peine après la fin officielle de ma thèse. Notre premier projet était très important pour la survie de l'entreprise et a occupé une part très conséquente de mon temps cette année, ce qui a retardé encore l'achèvement de ce mémoire. Ce manuscrit termine donc ce travail de thèse.

# 1 Introduction

This thesis is a partnership between the BL TVFE of NXP Semiconductors in Caen and ESIEE Paris. Its goal is to provide a solution to multi-channel reception for cable network.
TV broadcasting is characterized by the use of wideband channels to transmit a large amount of information. Hence, multiple TV channels transmission requires a broadband spectrum. A tuner function is needed to select the desired channel among a large range of frequency for the demodulation. The tuner function is now implemented directly on the main board thanks to fully integrated solution, so-called Silicon Tuner. NXP are one of the leaders in this domain. Yet, multi-stream reception is a key point for future products in cable modem, terrestrial and satellite TV. This is a required feature for watch-and-record, picture-in-picture, or bonded channel applications... Another trend is the reception of different types of data using a unique receiver, called home gateway, as shown in Fig.1. 1.

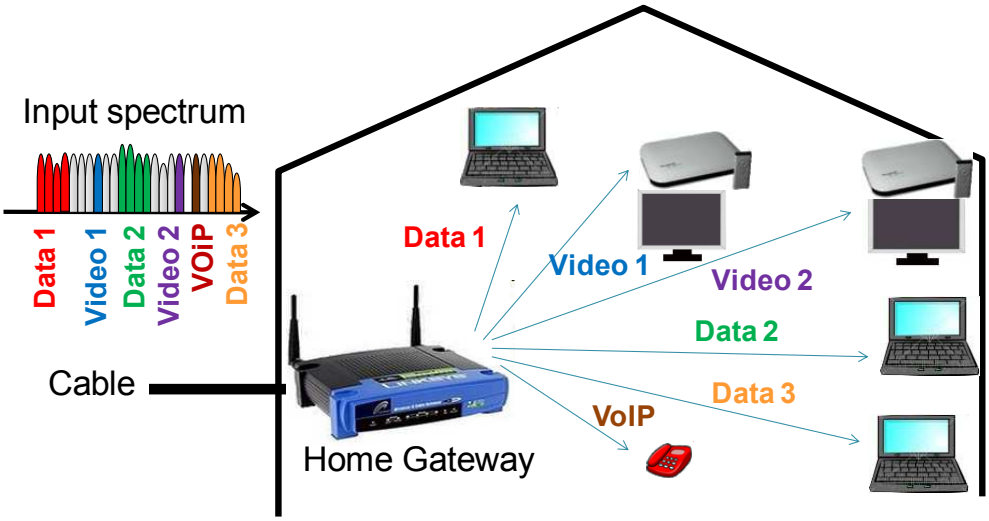


**Fig.1. 1 - Home Gateway**

This implies simultaneous reception of several channels located anywhere on the whole band or partial RF band. The simultaneous reception supposes either the digitization of the whole band or the use of as many tuners as wanted channels. The spectrum of interest spreads from 50MHz to 1GHz, and one might want to simultaneously receive up to 16 channels of 6MHz. Of course, using for instance 16 tuners Integrated Circuits for receiving 16 channels will be severely over-killing in terms of cost and power. Therefore it is of particular importance to investigate solutions for the complete digitization of the 1GHz input spectrum.
Broadband digitization is a foreseen direction in RF sampling architecture: the whole RF band is sampled very early in the signal path. This reduces RF hardware, allows most of the processing to be done in digital domain, thus facilitates reconfigurability by software (Software Radio).

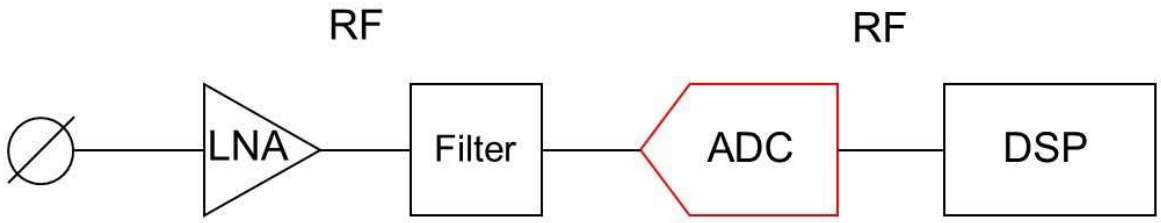


**Fig.1. 2 - RF sampling architecture**

However, this puts tough requirements on the Analog-to-Digital Converter (ADC): the wide signal bandwidth requires a high sampling rate (>2Gsps) ), while the lack of RF selectivity and the non-uniform input power spectral density (PSD) leads to high dynamic range requirement (>10bits).

The current Analog-to-Digital Converters architectures are not adapted to such an application. Flash ADCs, pipeline ADCs, Successive Approximation Register (SAR) ADCs and ΣΔ ADCs are either high speed or high resolution. According to the literature, parallel structures for ADCs are a key for the design of high-speed, high-resolution data converters. Time-interleaving (TI), Hybrid Filter Banks (HFB) are potential architectures [1]. Another possible way to cope with this problem is to divide the issues by splitting the spectrum into subbands. This architecture is called RFFB and consists of a bank of analog filters and a bank of ADCs. A study is proposed in Part 3, where we also propose and evaluate several architectures using different sampling methods such as bandpass sampling and complex sampling. A solution based on analytic signals and downconversion is promising. Then we introduce a general cost function that links surface and power consumption, in order to compare the proposed architecture with a wideband ADC close to our targets. This work has been presented at EuMW [2]. This architecture has the major advantage that all the components are feasible, even the ADCs, and it is possible to switch-off subbands to save power. It could be a good solution at the present time but it is not competitive in terms of power consumption and surface. An alternative is proposed in Part 4, where we study Hybrid Filter Banks. It is interesting to discover this architecture with realization feasibility in mind. This is why we select a 2-channel HFB with a $3^{rd}$-order Butterworth lowpass filter and a $3^{rd}$-order Butterworth highpass filter as low-cost analog filters. We present an original procedure for the optimization of the synthesis filters, which combines direct simplex search, minimax methods and a perturbation strategy to avoid local minima. We also address the calibration of the device, namely the identification of the actual analog filters, and highlight the impact of the identification and of measurement errors on the overall performances. This work has been presented at Newcas [3]. Finally, a physical realization proves the concept of aliasing rejection and confirms the parallel architecture sensitivity to analog mismatches. (ECCTD [4]).

We have started with the study of RFFB, because we have not found this architecture in the literature. This lasted around one year. Then the theoretical work on HFB preceeded the realization. It took around one year, and around 9 months respectively. The aim was to reach our targets and it was so challenging that the manuscript could not be finished on time. A few days and a conference later, I started a new adventure in another company, a start-up. Our first project was crucial for our survival and I spent much time on it this year. This manuscript ends this adventure.

We continue this introduction with a brief presentation of the context of cable networks, which highlights the main figures and the objectives of our work.

## 1.1 Cable network

### 1.1.1 Description (standards)

There are two main standards related to cable network, DOCSIS 3.0 [8] and SCTE40 [9], that meet the requirements of ITUJ83.B [10]. The main parameters that are necessary for the specification of our application are summarized in Table 1. 1:

**Table 1. 1 - Parameters for cable network**

| Parameters | Condition | DOCSIS | SCTE40 | Unit |
|---|---|---|---|---|
| RF channels freq range | | 108-1002 | 54-864 | MHz |
| Min level per channel | 64QAM | -15 | -15 | dBmV |
| Min level per channel | 256QAM | -15 | -12 | dBmV |
| Max level per channel | 64QAM | +15 | +15 | dBmV |
| Max level per channel | 256QAM | +15 | +15 | dBmV |
| Channel bandwidth | | 6 | 6 | MHz |
| Symbol rate | 64QAM | 5.06 | 5.06 | Msps |
| Symbol rate | 256QAM | 5.36 | 5.36 | Msps |
| Es/N0 | At output of the receiver for 64QAM | ≈ 23.5 | | dB |
| Es/N0 | At output of the receiver for 256QAM | ≈ 29 | | dB |
| D/U | 64QAM wanted channel | -10 | -21 | dB |
| D/U | 256QAM wanted channel | -10 | -11 | dB |

### 1.1.2 Signals

Some notions are defined in the following so as to introduce the specifications of the selected test case presented in 1.1.3.

#### *1.1.2.1 $Es/N0$*

$Es/N0$ is the SNR per channel wanted at the output of the ADC to be able to demodulate the channel. $Es/N0$ depends on the modulation of the channel and we can find its value in Table 1. 1.

Unlike the $SNRnyquist$ that is defined in the Nyquist band, i.e. from DC to $\frac{Fs}{2}$, it is defined in a single channel (6MHz):

$$\frac{Es}{N0} = \frac{Wanted\ channel}{noise_{6MHz}} \tag{1.1}$$

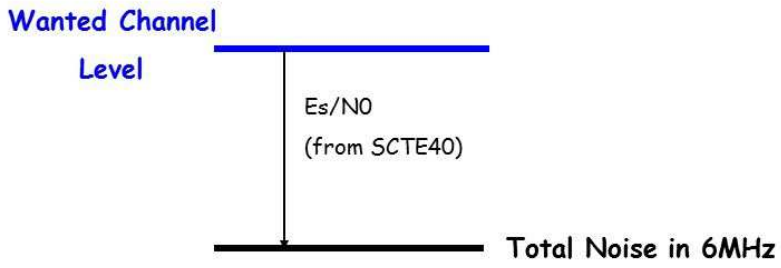


**Fig.1. 3 - Es/N0**

For now, we need to define the SNR per channel at the output of the ADC. We have to specify a margin to take into account the imperfections of the ADC.

#### *1.1.2.2 Margin*

We choose the Implementation Loss, $IL$, and calculate the corresponding Margin with the formula of APPENDIX A:

$$Margin = IL - 10\log\left(10^{\frac{IL}{10}} - 1\right). \quad (1.2)$$

Given that $IL = 2.2dB$, $Margin = 4dB$.

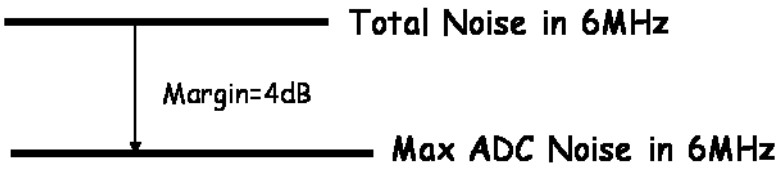


**Fig.1. 4 - Margin**

#### *1.1.2.3 Total Desired to Undesired power ratio D/Utot*

In cable network, the 6MHz wanted channel is located in a much wider band. The total power of the spectrum, $P_{tot\_dBuV}$, is calculated as follows. The power level of the wanted channel, $P_{desired\_dBuV}$, can be determined using its relation in the standard with the adjacent undesired channel. Thus, we have the total desired to undesired power ration, $D/U_{tot}$.

$$D/U_{tot} = P_{desired\_dBuV} - P_{tot\_dBuV}. \quad (1.3)$$

##### 1.1.2.3.1 Calculation of total power of the spectrum

We consider the following spectrum. It is composed of $M$ blocks. For each one, we know the number of channels $N_k$ per block and the power of one channel, $V_{k\_dB\mu V}$. The aim of this section is to calculate the total power of the whole spectrum, $P_{dB\mu V}$.

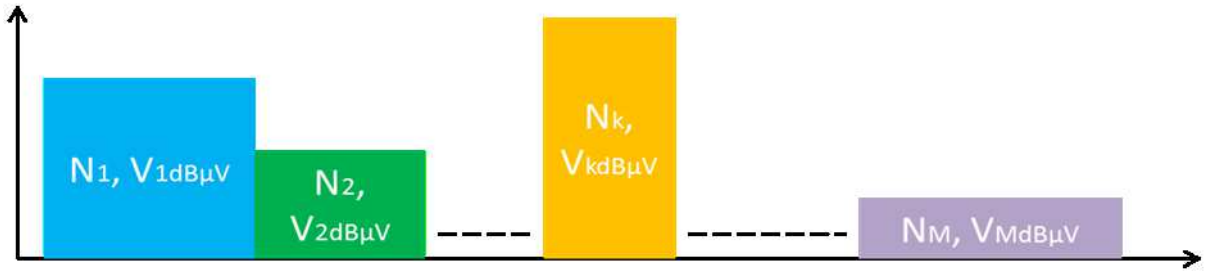


**Fig.1. 5 - Spectrum with *M* blocks**

We compute the total power of block $k$, $v_{k\_tot}$ given the number of channels $N_k$ and the the power of each channel $v_k$, in linear scale:

$$v_{k\_tot} = N_k \times v_k \tag{1.4}$$

This is equivalent to the following equation, where $V_{k\_dB\mu V}$ and $V_{k\_dB\mu V\_tot}$ are the power of one channel in dB and the total power of block $k$ in dB, respectively:

$$10^{\left(\frac{V_{k\_tot\_dB\mu V}}{10}\right)} = N_k \times 10^{\left(\frac{V_{k\_dB\mu V}}{10}\right)} \tag{1.5}$$

$$V_{k\_tot\_dB\mu V} = 10\log(N_k) + V_{k\_dB\mu V} \tag{1.6}$$

The total power of the whole spectrum $p_{tot}$ is the sum of the total power of each block $v_{k\_tot}$, in linear, as follows:

$$p_{tot} = \sum_{k=1}^{M} v_{k\_tot} \tag{1.7}$$

It is of course equivalent to the following equation, where $P_{tot\_dB\mu V}$ and $V_{k\_tot\_dB\mu V}$ are the power of the whole spectrum in dB and the total power of block $k$ in dB, respectively:

$$10^{\left(\frac{P_{tot\_dB\mu V}}{10}\right)} = \sum_{k=1}^{M} 10^{\left(\frac{V_{k\_tot\_dB\mu V}}{10}\right)} \tag{1.8}$$

$$P_{tot\_dB\mu V} = 10\log\left(\sum_{k=1}^{M} N_k \times 10^{\left(\frac{V_{k\_dB\mu V}}{10}\right)}\right). \tag{1.9}$$

Now, let us consider a uniform flat spectrum, composed of $N$ channels, each of them with a power $V_{dB\mu V}$, as depicted in Fig.1. 6.


**Fig.1. 6 - Spectrum with one block**

In this case, (1.9) becomes:

$$P_{tot\_dB\mu V} = 10\log\left(N \times 10^{\left(\frac{V_{dB\mu V}}{10}\right)}\right) \tag{1.10}$$

$$P_{tot\_dB\mu V} = 10\log(N) + V_{dB\mu V} \tag{1.11}$$

### 1.1.2.3.2 Power of desired channel


**Fig.1. 7 - *D/U***

According to the standards, we know that the worst case of $D/U$ Ratio depends on the type of modulation of the desired and the undesired channels. Thus, we can determine the power of the Desired channel, $P_{desired\_dB\mu V}$, from the knowledge of the power of an adjacent channel, i.e. $V_{k\_dB\mu V}$ defined in 1.1.2.3.1, depending on the location of the wanted channel.

$$D/U = P_{desired\_dB\mu V} - V_{k\_dB\mu V} \quad (1.12)$$

$$P_{desired\_dB\mu V} = V_{k\_dB\mu V} + D/U \quad (1.13)$$

### *1.1.2.4 Crest factor*

Crest Factor, $CF$, is a value that links the peak value and the root mean square value of a signal as follows:

$$CF = 10\log\left(\frac{{V_{peak}}^2}{{V_{rms}}^2}\right), \quad (1.14)$$

where $V$ is the signal magnitude.
For Multi-QAM modulations, $CF$ is estimated to be 15dB, according to our simulations.

### *1.1.2.5 Backoff*

Given that we reach the full-scale, backoff is null.

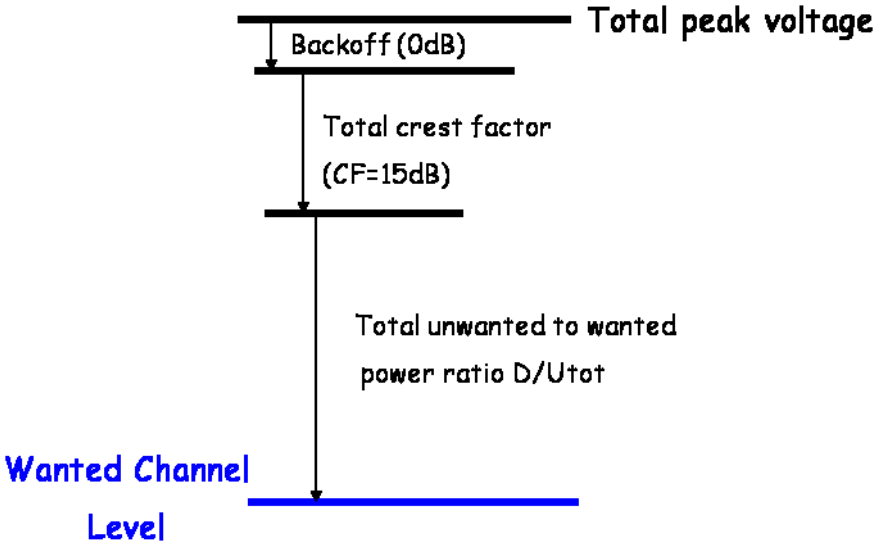


**Fig.1. 8 -Wanted channel in the whole spectrum**

### *1.1.2.6 Symbol Rate*

The symbol rate, $SR$, is different from the channel bandwidth, $chBW$, and they are linked as follows:

$$SR = \frac{chBW}{1+\alpha} \quad (1.15)$$

Where α is the roll-off factor.
Fig.1. 9 highlights this difference:

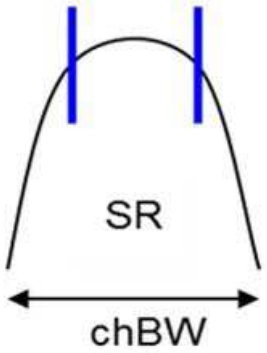


**Fig.1. 9 - Symbol Rate versus channel bandwidth**

The symbol rate depends on the modulation of the channel and is defined in ITU J.83.

### 1.1.3 Selected Test Case

This section presents the selected test case and explains the choices made on the input spectrum and the specifications of the wanted channel. Then, the most important values are calculated.

There are two main standards related to cable network, SCTE40 and DOCSIS 3.0, presented in 1.1.1. SCTE40 transmits a signal from 54MHz to 864MHz, whereas DOCSIS 3.0 transmits a signal from 111MHz to 1002MHz. To cover both, we choose to consider an input spectrum from $f_{min} = 50MHz$ to $f_{max} = 1GHz$.
Our target is US, thus each channel has 6MHz-bandwidth, $chBW$. We can calculate $N$, the number of channels as follows:

$$N = \frac{f_{max} - f_{min}}{chBW}, \tag{1.16}$$

$$N = \frac{1.10^9 - 50.10^6}{6.10^6} \approx 158. \tag{1.17}$$

Using the standard, we know that the power per channel is between -15dBm and 15dBm, i.e. between 45dBµV and 75dBµV. We choose the mean value: 60dBµV. We consider that the input spectrum is flat on the whole bandwidth. The possible tilt that reduces the power of channels at high frequencies can be compensated by adding an equalizer in the architecture.
We are now able to calculate the total power of the input spectrum, $P_{tot\_dBuV}$.
As $N = 158$ and $V_{dB\mu V} = 60dB\mu V$, (1.11) gives $P_{tot\_dB\mu V} = 10\log(158) + 60 \approx 82dB\mu V$

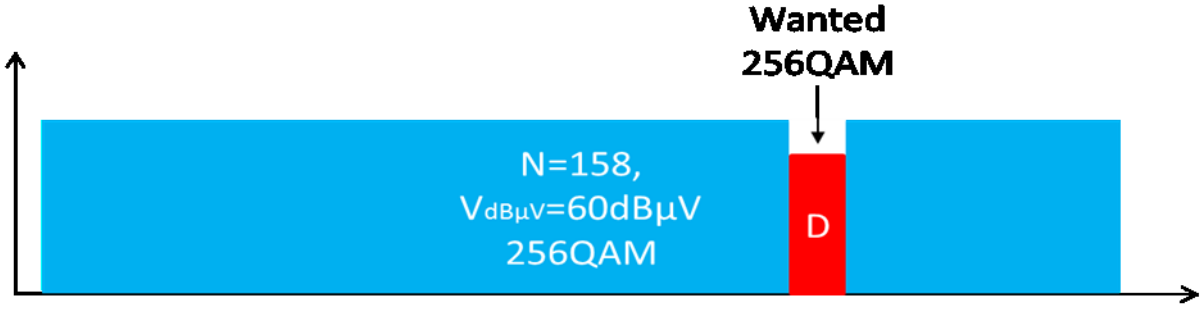


**Fig.1. 10 - Input spectrum**

As analog signals are becoming obsolete, we assume that the spectrum will be composed of digital channels, 256QAM for example. The wanted channel is also 256QAM. Fig.1. 10 sums up the hypotheses on the wanted signal and the input spectrum.
The power ratio of the Desired to the adjacent undesired channel, $D/U$, in the worst case, is not indicated for this example in SCTE40. It is possible to evaluate it using the standard values.
The desired and the undesired signals are 256QAM with a nominal level of -5dBc. In the worst case, the wanted signal will be at its weakest level, 6dB below nominal level which itself may be -2dB below -5dBc (-5-2-6= -13dBc), and the unwanted will be at its strongest level, 6dB above nominal, which itself may be 2dB above -5dBc (-5+2+6=3dBc). Thus, the undesired 256QAM signal is 16dB stronger than the desired 256QAM signal in the worst case. As a reasonable value, we choose $D/U = -11dB$.
Given that the level of the adjacent is 60dBµV, the wanted channel's level, $P_{desired\_dBuV}$, is 49dBµV ($60 - 11 = 49dB\mu V$).

As a consequence, (1.3) gives $D/U_{tot} \approx 49 - 82 \approx -33dB$.

The choice of 256QAM implies that $Es/N0$ should be 29dB and that the symbol rate, $SR$, is 5.36Msym/s, that corresponds to a roll-off factor of 0.12.

Table 1. 2 summarizes the values that will be used to specify the ADC Signal-to-Noise ratio (SNR) on the Nyquist band (see 1.3.2).

**Table 1. 2 - Recap table**

| | |
|---|---|
| Frequency range | 50MHz→ 1GHz |
| Channel BW | 6MHz |
| Number of channels | 158 |
| Power per channel | 60dBµV |
| Modulation Wanted | 256QAM |
| Modulation Unwanted | 256QAM |
| Es/N0 | 29dB |
| Margin | 4dB |
| D/U | -11dB |
| D/Utot | -33dB |
| CF | 15dB |
| Backoff | 0dB |
| SR | 5.36Msym/s |

## 1.2 Applications

TV broadcasting is characterized by the use of wideband channels to transmit a large amount of information. Hence, multiple TV channels transmission requires a broadband spectrum. A tuner function is needed to select the desired channel among a large range of frequency for the demodulation. The tuner function is now implemented directly on the main board thanks to fully integrated solution, so-called Silicon Tuner. NXP semiconductor has demonstrated the feasibility of Silicon tuner solution currently in mass-production and is the leader in this field.
Multi-stream reception is a key point for future products in cable modem. This implies simultaneous reception of several channels located anywhere on the whole or partial RF band.

The first part of this section briefly presents the architecture of a single tuner for cable modem and the second part introduces the constraints associated to multi-channel reception.

### 1.2.1 Single cable tuner

NXP Semiconductors are the leaders in Silicon Tuners.
We know how to receive only one channel.
The global architecture is depicted on Fig.1. 11. The principle is to select the wanted channel located anywhere in the whole spectrum, with a bandpass filter (Fig.1. 12), to down-convert it near DC with a mixer and to filter harmonics with a lowpass filter (Fig.1. 13). Then, the wanted channel is converted from analog to digital with an ADC, and it is demodulated using a DSP.

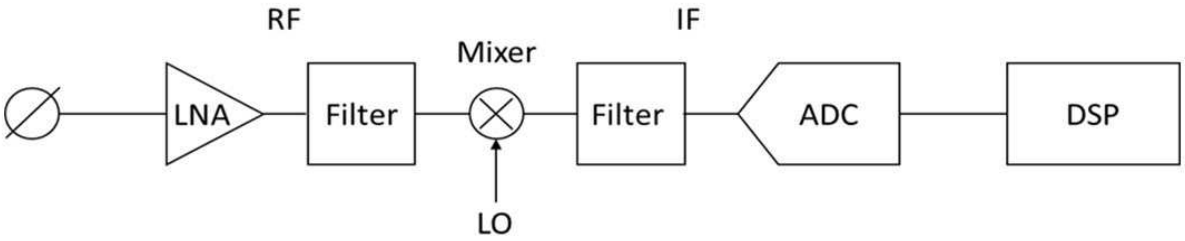


**Fig.1. 11 - Common and simplified receiver architecture**

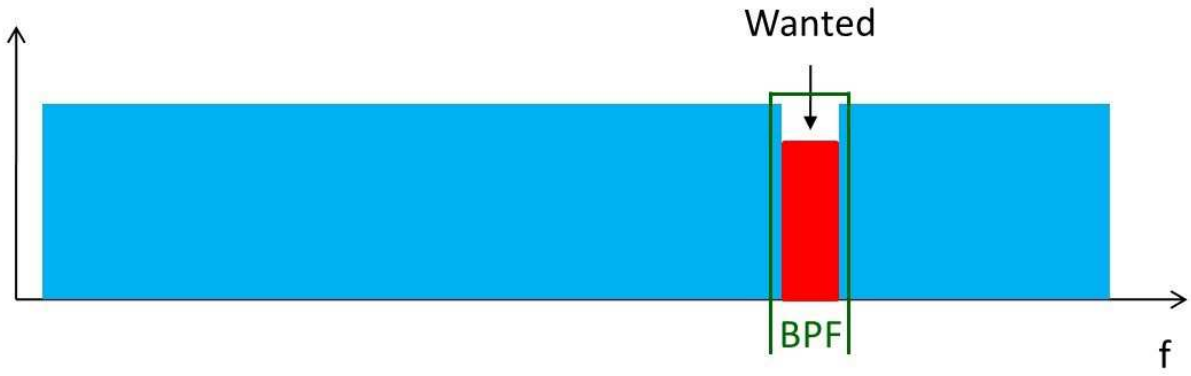


**Fig.1. 12 - Selection of the wanted channel with BPF**


**Fig.1. 13 - Wanted channel after mixing and LPF**

In this case, the ADC requirements are quite light, since the bandwidth to convert is narrow.

### 1.2.2 Multi-channel reception

To receive several channels simultaneously, we can obviously imagine having a tuner per channel (Fig.1. 14).

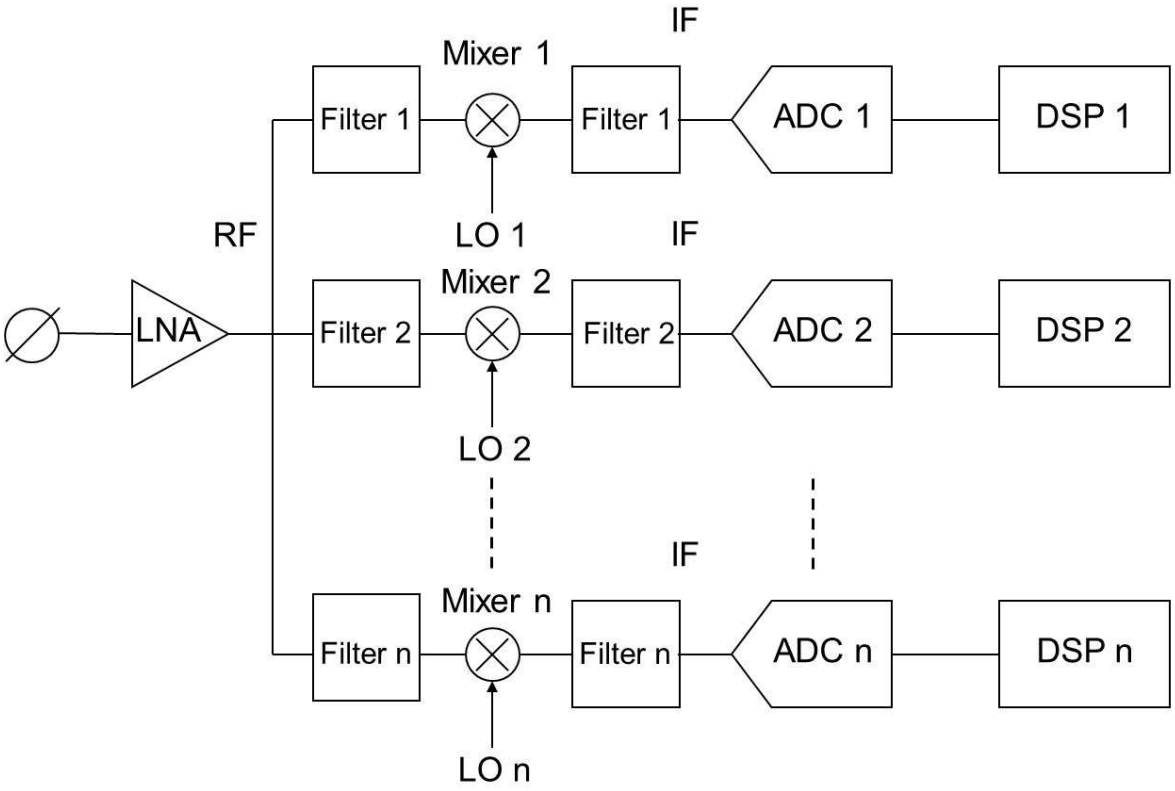


**Fig.1. 14 - M multiple common receivers in parallel**

Yet, this solution is overkilling in terms of cost and power.
Today, one foreseen direction is RF sampling architecture: whole RF band is sampled very early in the signal path, as shown on Fig.1. 15. This reduces RF hardware, allows most of the processing (mixing, filtering) to be done in digital domain, thus facilitates reconfigurability by software (Software Radio). ADC becomes the bottleneck of such architecture, because it needs to be broadband and must cope with the whole input dynamic range. The following section derives the specifications of this ADC according to the selected test case in 1.1.3.

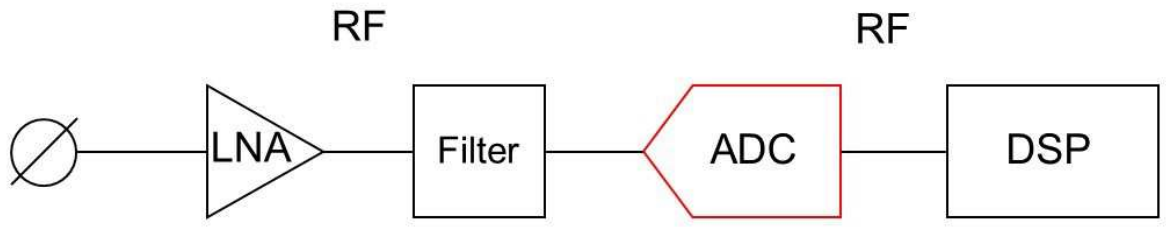


**Fig.1. 15 - Full-spectrum receiver**

## 1.3 ADC specifications

An ADC is specified by its sampling rate, $Fclk$, and the SNR in the Nyquist band, $SNRnyquist$.

### 1.3.1 Sampling rate

In general, the sampling rate should be chosen so as to fulfill the Shannon's condition to avoid aliasing. According to the selected test case, the sampling rate should be greater than 2Gsps. Moreover, to avoid MoCA, we choose $Fclk = 2.6Gsps$.

### 1.3.2 SNR on the Nyquist band

$SNRnyquist$ is the signal-to-noise ratio defined on the Nyquist band with a full-scale input sinus.

In 1.1.2, we have calculated the ADC noise in 6MHz. We need to define the noise in the Nyquist band.
The oversampling gain, $OG$, links noise in two different bandwidths, $\frac{Fs}{2}$ and $SR$:

$$OG = 10\log\left(\frac{Fs}{2 \times SR}\right), \tag{1.18}$$

where $FS = 2.6GHz$ and $SR = 5.36Mbits/s$, according to the previous sections.

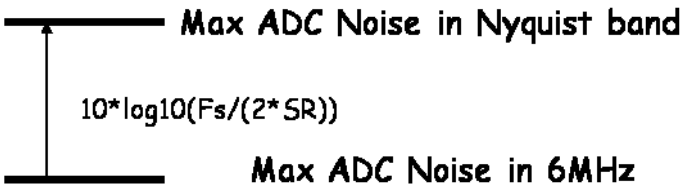


**Fig.1. 16 - Oversampling gain**

Here is the corresponding level diagram:

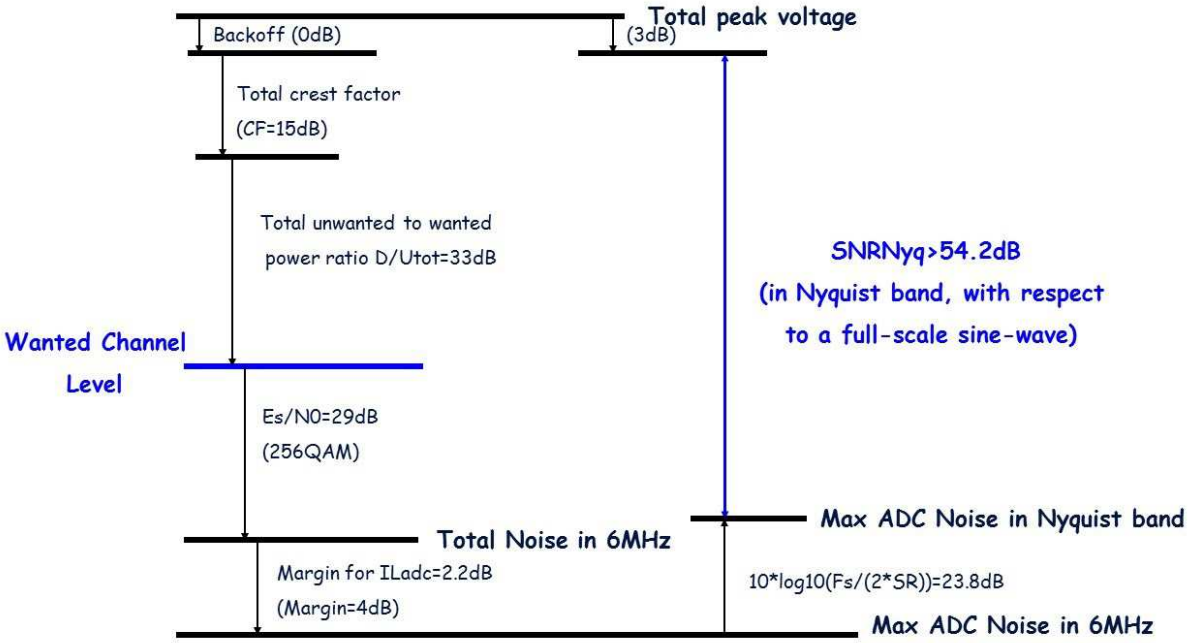


**Fig.1. 17 - Level diagram**

From Fig.1. 17, we deduce equation (1.19) and the minimum required SNR in Nyquist band for this ADC working at 2.6GHz, that is around 55dB, according to the selected test case.

$$SNR_{nyquist} = Backoff + CF + D/U_{tot} + Es/N0 + Margin - 10\log\left(\frac{Fs}{2 \times SR}\right) - 3 \qquad (1.19)$$

## 1.4 Conclusion

In the context of multi-channel reception for cable modem, broadband digitization is the major issue and, thus, the ADC is the bottleneck of architecture of RF sampling. We have specified an ADC that should be working at 2.6GHz, with a required SNR greater than 55dB to be able to digitize the selected input spectrum, which is really challenging. This input spectrum has been chosen to meet the requirements of the standards SCTE40 and DOCSIS 3.0.

# 2 State-of-the-art

In the introduction, we have specified the ADC that is the bottleneck of the receiver in case of multi-channel reception. According to the selected test case, we need an ADC working at 2.6GHz with a minimum required SNR of 55dB. As shown in the following section that sketches the state-of-the-art of stand alone ADCs, it is really challenging. Then, we will see that parallel architectures seem to be necessary to reach the ADC requirements, as the constraints on each subband ADC can be relaxed. Finally, some sampling methods are recalled such as bandpass sampling and complex sampling since they are solutions that reduce the sampling frequency below the Nyquist rate in particular conditions.

## 2.1 Stand-alone ADC

There are several types of ADCs, the most famous being flash, folding, pipeline, sigma-delta and SAR. They can be classified as in Fig.2. 1 regarding their speed, i.e. input signal bandwidth, and their resolution, i.e. the number of bits needed to convert the signal from analog to digital. Therefore, we have the following graph:

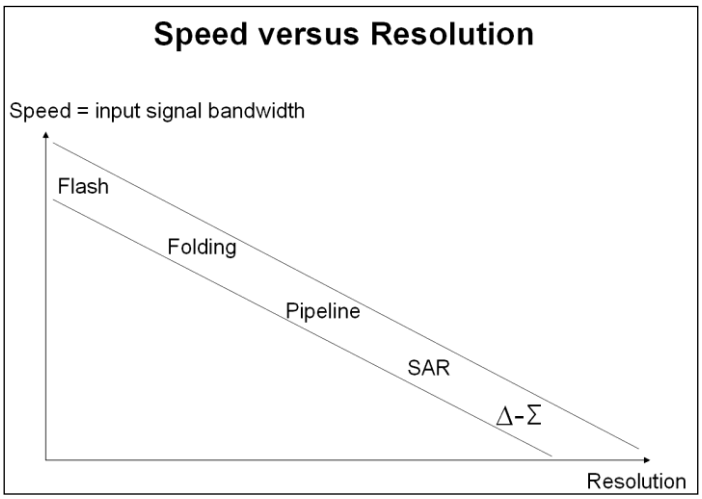


**Fig.2. 1 - Trade-off of ADCs**

### 2.1.1 Flash

#### *2.1.1.1 Architecture*

Flash ADCs (sometimes called “parallel” ADCs) are typically high-speed, low resolution. Flash ADC is the fastest architecture available. A flash ADC is made up of a large bank of comparators. An N-bit flash ADC consists of $2^N$ resistors and $2^N$-1 comparators. So the number of comparators goes up by a factor of 2 for every extra bit of resolution. This leads to high power consumption. In addition, the capacitive load seen by the sample-and-hold is quite high. Fig.2. 2 shows the architecture of a 3-bit Flash ADC, thus with 8 resistors and 7 comparators.

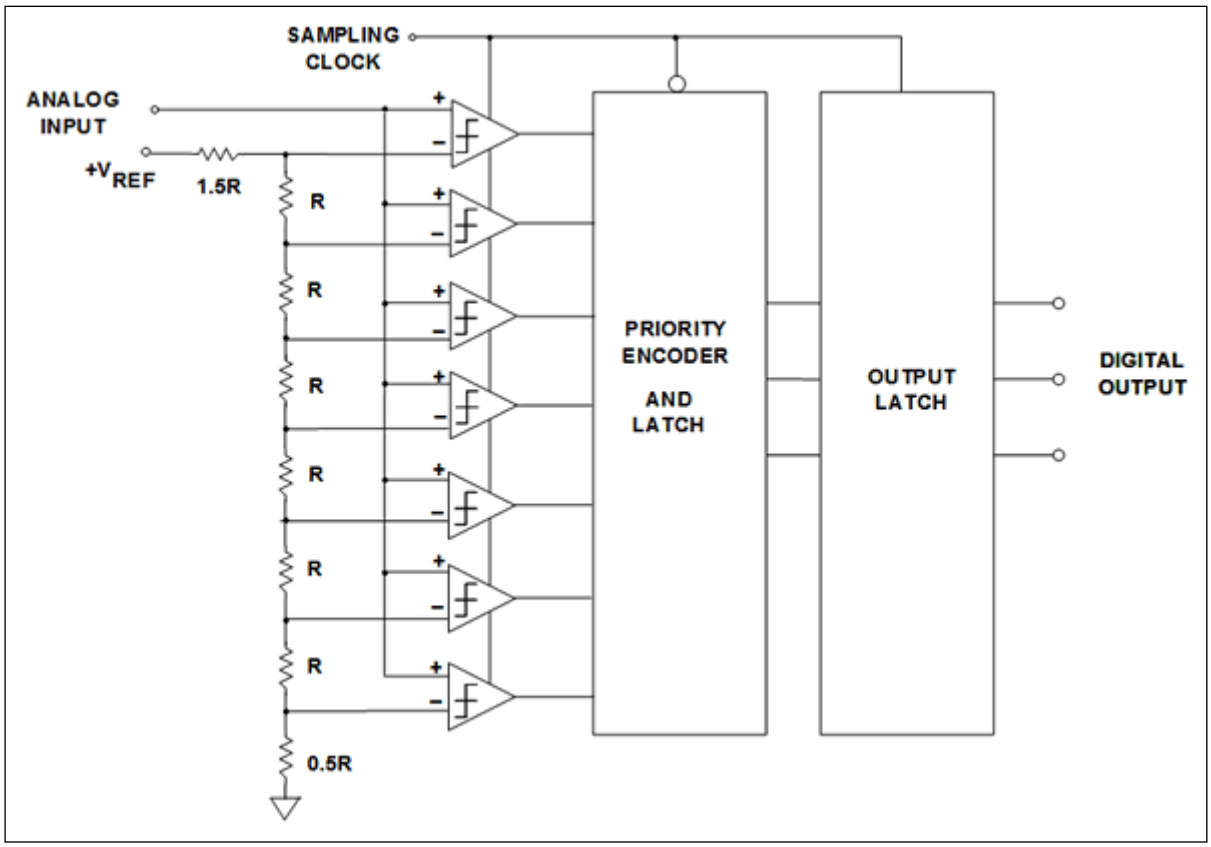


**Fig.2. 2 - 3-bit Flash ADC architecture**

#### *2.1.1.2 Principle*

Each comparator has a reference voltage from the resistor string which is 1 LSB higher than that of the one below in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The $2^N$-1 comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a "thermometer" code. Since $2^N$-1 data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.

#### *2.1.1.3 State-of-the-art*

For example, we find in the literature a 6-bit flash ADC working at 25Gsps in 90nm CMOS [11], or even a 3-bit flash ADC working at 20Gsps in 65nm CMOS [12].

### 2.1.2 Folding

#### *2.1.2.1 Architecture*

Folding ADCs have approximately the same architecture as flash ADCs. They consume less power than flash, as depicted on Fig.2. 3.

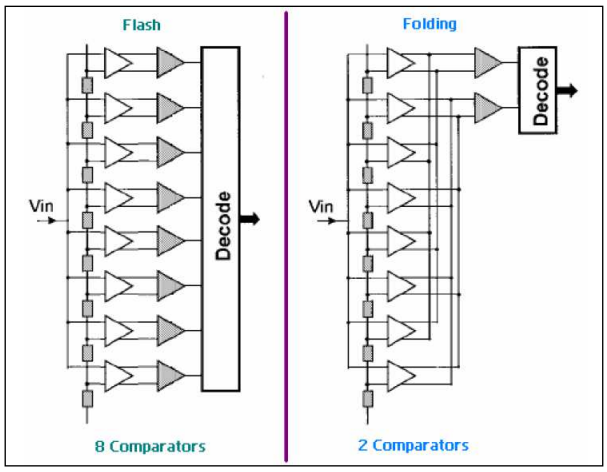


**Fig.2. 3 - Flash versus Folding**

The architecture of a folding analog-to-digital converter system for an 8-bit ADC is shown on Fig.2. 4:

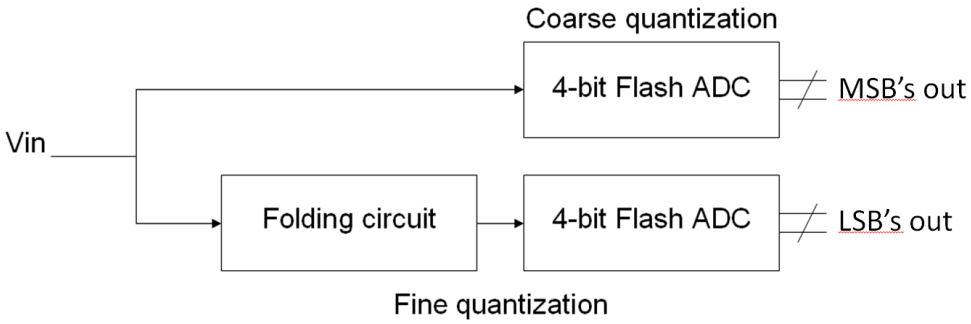


**Fig.2. 4 - Folding architecture**

There are a fine quantization for LSBs and a coarse quantization for MSBs. The fine quantization is done by a 4-bit Flash ADC preceeded by a folding circuit, whereas the coarse quantization is done by a 4-bit Flash ADC, in this example.

### *2.1.2.2 Principle*

The most significant bits are determined by the coarse quantizer, which determines the number of time a signal is folded. The fine bits are determined by the fine quantizer which converts the pre-processed "folded" signal into the fine code. In this way it is possible to obtain an 8-bit resolution with only 30 comparators (4-bit coarse plus 4-bit fine), instead of 255 comparators for a Flash ADC. The low component count results in a small die area, while more power can be spent into the system to extend the bandwidth of the comparator and folding stages resulting in a higher sampling speed and a larger analog input bandwidth. On the other hand, a reduction in power can be obtained when sampling rate and analog input bandwidth are fixed.
On Fig.2. 5, there are the input signal (top) and the corresponding output signal of the folding stage (bottom) as a function of time. The result of the operation is an output signal with a frequency that is a multiple of the input frequency.

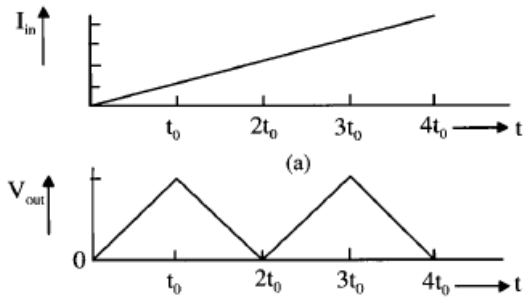


**Fig.2. 5 - Folding principle**

#### *2.1.2.3 State-of-the-art*

For example, we find in the literature a 6-bit folding ADC working at 400Msps in 90nm CMOS [13] or even a 7-bit folding ADC working at 1Gsps in 65nm CMOS [14].

### 2.1.3 Pipeline

#### *2.1.3.1 Architecture*

Pipelined ADCs are typically medium-speed, high resolution.
A pipelined ADC employs a cascaded structure in which each stage works on one to a few bits (of successive samples) concurrently. Although it cannot work very fast (~100Msps), it does not consume much.
The pipelined ADC had its origins in the sub-ranging architecture. Fig.2. 6 shows an example of pipeline architecture:

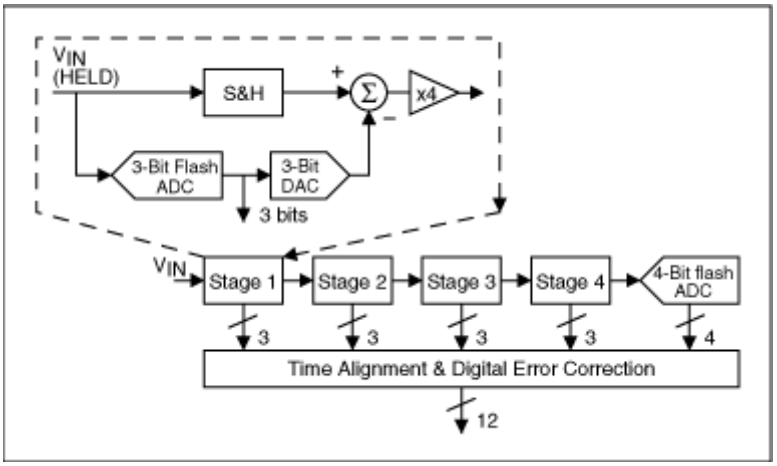


**Fig.2. 6 - Pipeline architecture**

#### *2.1.3.2 Principle*

The input is first converted by a simple 3-bits flash ADC. The digital value is converted back in analog format by a 3-bit DAC and subtracted from the input, this gives a residue. The residue is multiplied to get the full range, and then converted by as second flash.
In Fig.2. 6, the analog input, $V_{IN}$, is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to three bits. The 3-bit output is then fed to a 3-bit DAC (accurate to about 12 bits), and the analog output is subtracted from the input.

This "residue" is then gained up by a factor of four and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing three bits per stage until it reaches the 4-bit flash ADC, which resolves the last 4LSB bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput.

#### *2.1.3.3 State-of-the-art*

For example, we find in the literature a 10-bit pipeline ADC working at 320Msps in 90nm CMOS [15] or even a 10-bit pipeline ADC working at 250Msps in 90nm CMOS [16].

### 2.1.4 SAR

SAR means Successive Approximation Register. They represent the majority of the ADC market for medium to high resolution ADCs. Yet, they do not work very fast. As it only needs 1 comparator for N bits, power consumption is very low.

#### *2.1.4.1 Architecture*

A SAR ADC consists of a track-and-hold, a comparator, an n-bit DAC and SAR logic.

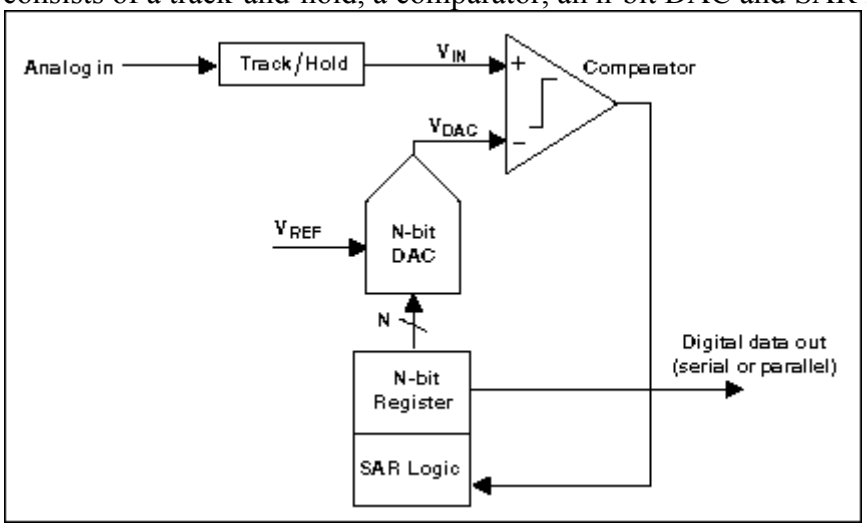


**Fig.2. 7 - SAR structure**

#### *2.1.4.2 Principle*

The basic principle of a SAR ADC is to convert the input voltage by successively approaching it (binary search algorithm).
First of all, the analog input voltage $V_{IN}$ is held on a track-and-hold. To implement the binary search algorithm, the N-bit register is first set to midscale (FS/2). This forces the DAC output $V_{DAC}$ to be $V_{REF}/2$, where $V_{REF}$ is the reference voltage provided to the ADC. A comparison is then performed to determine if $V_{IN}$ is less than or greater than $V_{DAC}$. If $V_{IN}$ is greater than $V_{DAC}$, the comparator output is logic high or '1' and the MSB of the N-bit register remains at '1'. Conversely, if $V_{IN}$ is less than $V_{DAC}$, the comparator output is logic low and MSB of the register is cleared to logic '0'. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the

LSB. Once this is done, the conversion is complete, and the N-bit digital word is available in the register.

Fig.2. 8 shows an example of a 4-bit conversion. The y-axis (and the bold line in the figure) represents the DAC output voltage. In the example, the first comparison shows that $V_{IN} < V_{DAC}$. Thus bit 3 is set to '0'. The DAC is then set to $(0100)_2$ and the second comparison is then performed. As $V_{IN} > V_{DAC}$, bit 2 remains at '1'. The DAC is then set to $(0110)_2$, and the third comparison is performed. Bit 1 is set to '0', and the DAC is then set to $(0101)_2$ for the final comparison. Finally, bit 0 remains at '1' because $V_{IN} > V_{DAC}$.

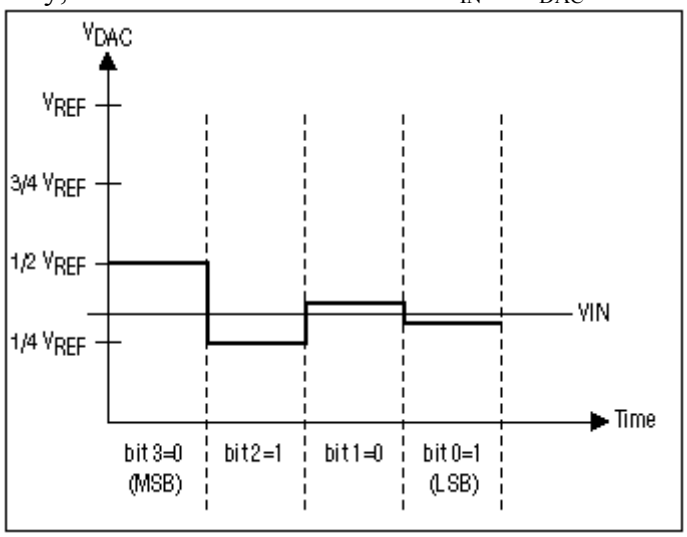


**Fig.2. 8 - SAR operation (4-bit ADC example)**

Notice that four comparison periods are required for a 4-bit ADC. Generally speaking, an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. This explains why these types of ADCs are power- and space-efficient.

#### *2.1.4.3 State-of-the-art*

For example, we find in the literature a 10-bit SAR ADC working at 40Msps in 0.13µm CMOS [17] or even a 10-bit SAR ADC working at 50Msps in 90nm CMOS [18].

### 2.1.5 ΣΔ

Traditional sigma-delta type converters have limited bandwidth, whereas they reach high resolution and they do not consume much.

#### *2.1.5.1 Architecture*

A sigma-delta ADC consists of an integrator, an n-bit flash ADC, an n-bit DAC, a digital filter and a decimator. Fig.2. 9 shows an example of a sigma-delta ADC.

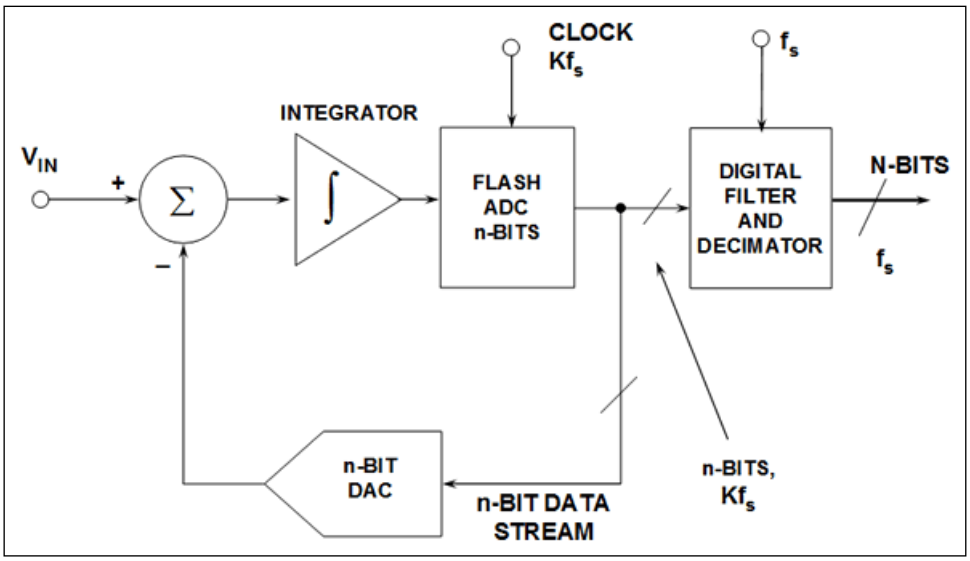


**Fig.2. 9 - Multi-bit sigma-delta ADC**

### *2.1.5.2 Principle*

Assume a dc input at $V_{IN}$. The integrator is constantly ramping up or down. The output of the comparator is fed back through an n-bit DAC to the summing input. The negative feedback loop from the comparator output through the n-bit DAC back to the summing point will force the average dc voltage to be equal to $V_{IN}$. This implies that the average DAC output voltage must equal the input voltage $V_{IN}$. The average DAC output voltage is controlled by the ones-density in the data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

### *2.1.5.3 State-of-the-art*

For example, we find in the literature a 14-bit sigma-delta ADC working at 23Msps in 90nm CMOS [19] or even a 14-bit sigma-delta ADC working at 2Msps in 0.18µm CMOS [20].

## 2.1.6 Conclusion

Fig.2. 10 depicts the few references of ADCs we have just mentioned. We can notice that it looks like Fig.2. 1. We also see that the targeted ADC (red star) is faster and/or with a better resolution than these ADCs.
The solution to reach the requirements of the targeted ADC is to use parallel architectures.

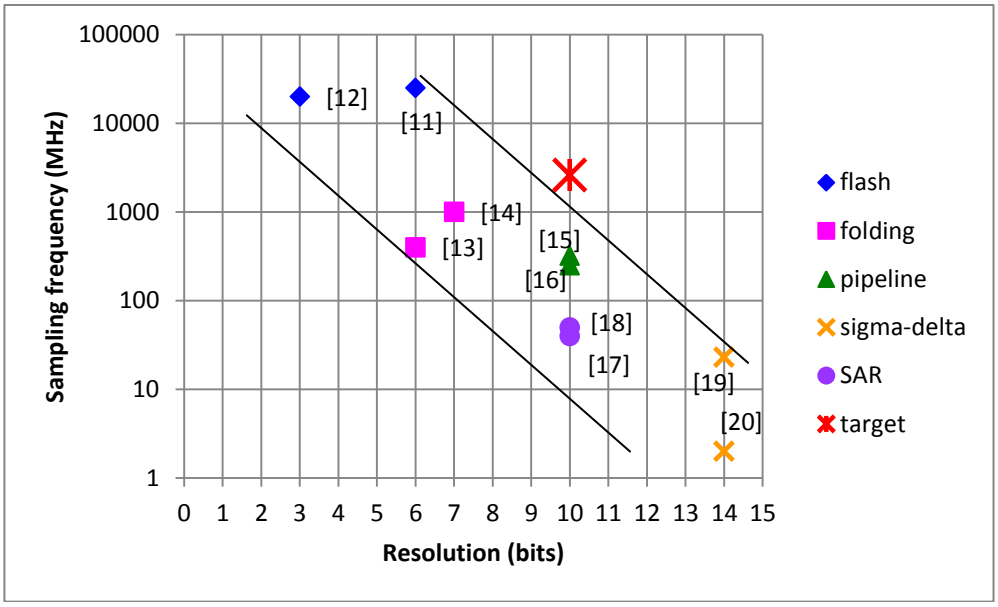


**Fig.2. 10 - Example of state-of-the-art of ADCs**

## 2.2 Parallel structures

Parallel architectures seem to be a solution to broadband digitization. In literature, we find structures such as Fig.2. 11:

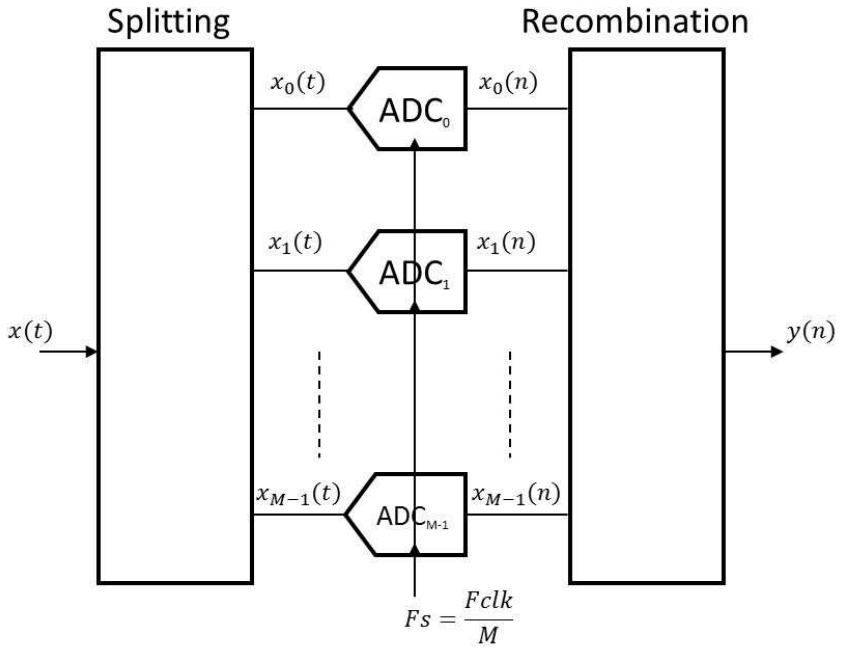


**Fig.2. 11 - Parallel architecture**

We wish to digitize the input signal x(t) at the global sampling rate $Fclk$. The analog input signal is split into M subbands $x_m(t), m \in \{0, \dots, M-1\}$. Then each subband signal is converted at $Fs = \frac{Fclk}{M}$ by the subband ADCs. Finally, the undersampled signals, $x_m(n), m \in \{0, \dots, M-1\}$ are recombined in such a way that the digital output $y(n)$ is equivalent to the analog input $x(t)$, sampled at $Fclk$. Thus, the constraints on the subband ADCs are reduced compared to a single high-performance ADC.

Two main parallel architectures will be described in the following sections: time-interleaving and hybrid filter banks. Parallel sigma-delta are not studied here ([21], [22], [23]).

### 2.2.1 Time-Interleaving

The first studied and the most famous parallel architecture is time-interleaving [24], [25]. Fig.2. 12 depicts the architecture.

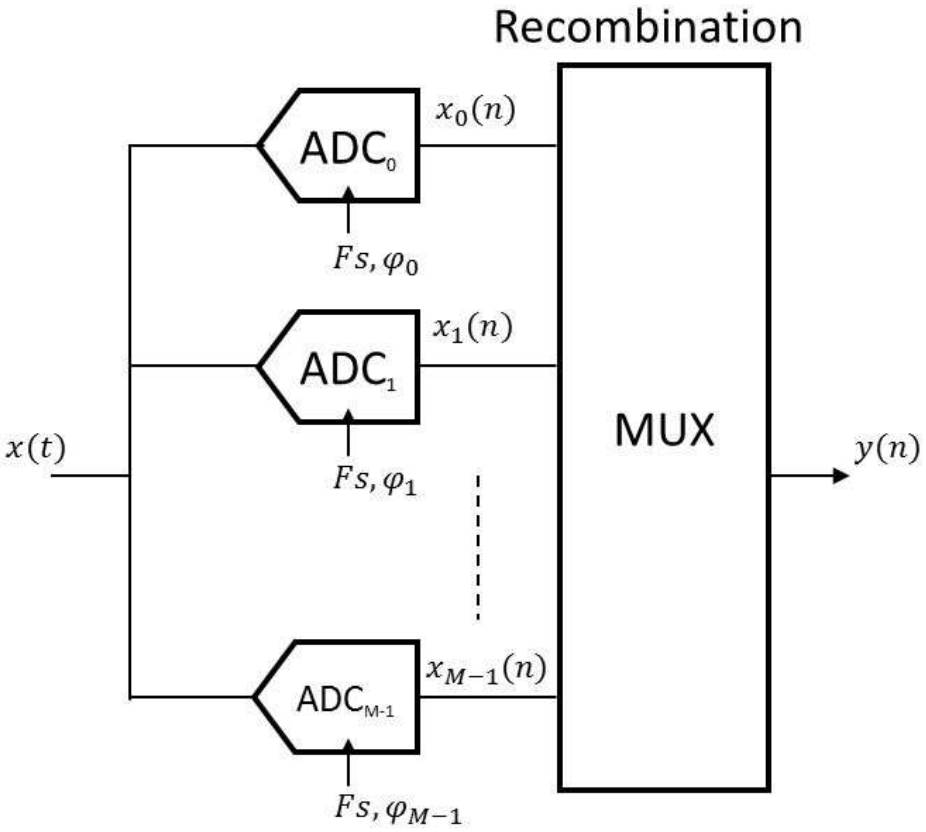


**Fig.2. 12 - Time-interleaving architecture**

There are M ADCs in parallel so each ADC works at $Fs = \frac{Fclk}{M}$, as explained before. Thus the ADCs sample at the same sampling rate but at different instants, $\varphi_m = m\frac{2\pi}{M}, m \in \{0, \dots, M-1\}$, because of phase shifting from one branch to another, as depicted on Fig.2. 13. Then, after sampling, a multiplexer recombines the samples to have the output signal. The global resolution is theoretically equivalent to the resolution of each sub-ADC.

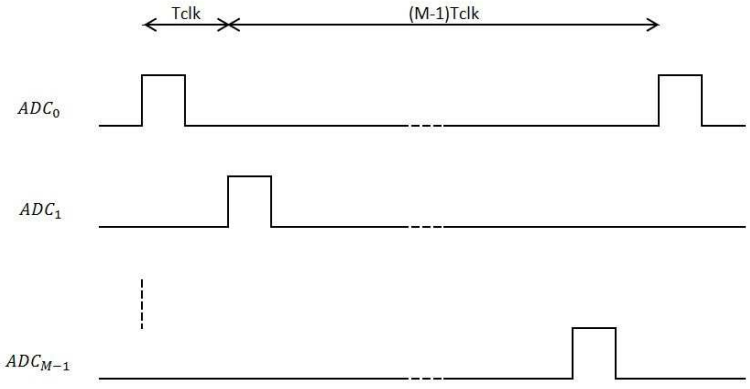


**Fig.2. 13 - Chronogram**

So the global sampling rate is $Fclk$. Fig.2. 14 represents the time-interleaving architecture in the general framework of parallel architecture.

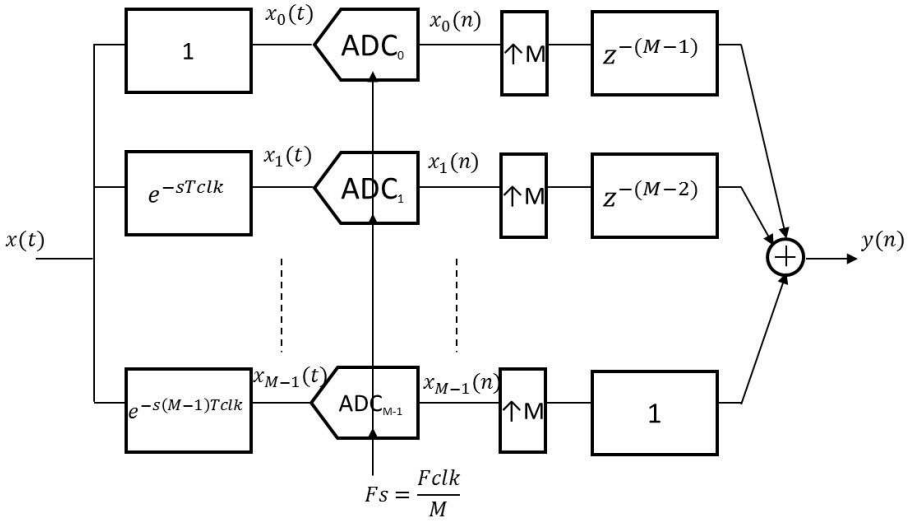


**Fig.2. 14 - Principle of time-interleaving**

In practice, the quantizers are different from each other. There are four types of errors: offset errors, gain errors, phase errors and timing errors. Some methods have been proposed to correct these errors in [25], [26], [27].

NXP Semiconductors is working on this architecture and has reached high-performance such as a SNDR of 48.5dB with a sampling rate of 2.6 Gsps [28]. There are 64 SAR ADCs in parallel, each ADC working at around 40Msps.

### 2.2.2 Spectral decomposition: HFB

We can split the input spectrum into several subbands thanks to analog filters, called analysis bank. Then, each subband signal is sampled thanks to subband ADCs that work at a lower sampling rate than the global sampling rate. Upmixers and digital filters composed the synthesis bank and finally, the subbands are recombined. This architecture is called Hybrid Filter Banks (HFB) and can be implemented with either discrete-time or continuous-time analog filters.

#### *2.2.2.1 Discrete-time Hybrid Filter Banks*

Fig.2. 15 depicts a discrete-time Hybrid Filter Bank (DT-HFB).

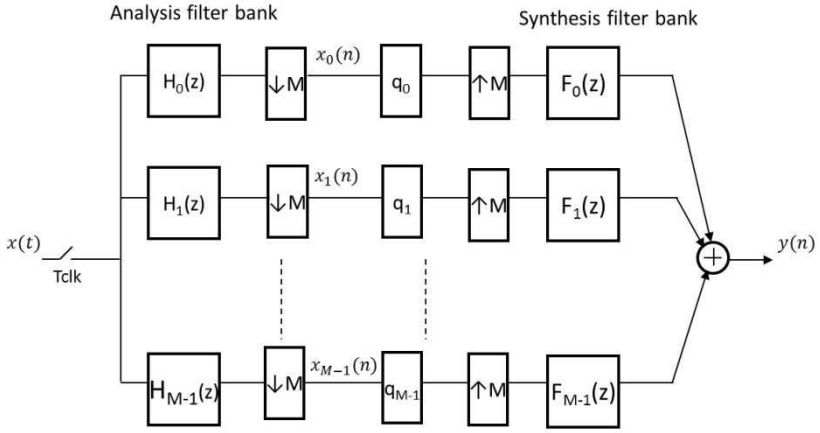


**Fig.2. 15 - Discrete-time Hybrid Filter Banks**

We suppose that the input signal $x(t)$ is bandlimited. The analysis bank is composed of discrete-time analog filters $H_0(z)$, $H_1(z)$,…, $H_{M-1}(z)$, such as switched-capacitors. The input signal $x(t)$ is first sampled and then filtered by discrete analog filters $H_0(z)$, $H_1(z)$,…, $H_{M-1}(z)$. Then, the signals $x_0(n)$, $x_1(n)$,…, $x_{M-1}(n)$ are downsampled and quantified at the sampling rate $Fs = \frac{Fclk}{M}$, where $Fclk$ is the global sampling rate and M is the number of subbands. After that, the individual signals are up-sampled and filtered by the digital filters $F_0(z)$, $F_1(z)$,…, $F_{M-1}(z)$. Finally, the signals are added and the digital output $y(n)$ is a digital equivalent to the analog input signal.
The advantage of the discrete-time HFB is that the switched-capacitors filters can be implemented with a very good precision, compared to continuous-time analog filters. A disadvantage of this structure is that the sampling of the input signal $x(t)$ should be done at the global sampling rate, which is very high in our applications. Another limitation of the discrete-time filters is their maximum frequency.
DT-HFB has been studied in [29] for the first time. The impact of quantization at the output of DT-HFB-based ADC has been studied in [30]. An analysis of the impact of analog imperfections on the DT-HFB performances has been proposed in [31] or [32].

### *2.2.2.2 Continuous-time Hybrid Filter Banks*

Fig.2. 16 depicts a continuous-time Hybrid Filter Bank (CT-HFB).

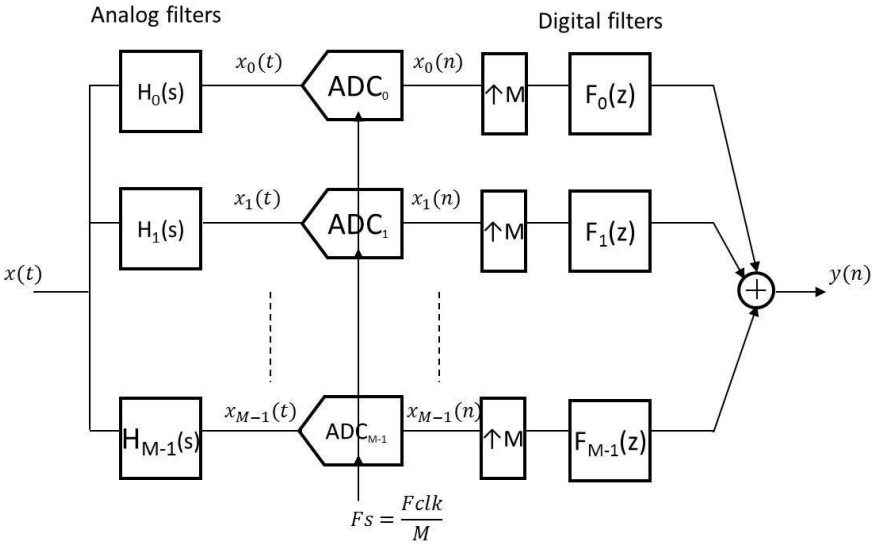


**Fig.2. 16 - Continuous-time Hybrid Filter Bank**

This structure has been proposed in [33]. In this case, the analog input signal is directly decomposed by the continuous-time analog filters $H_0(s)$, $H_1(s)$,…, $H_{M-1}(s)$. We suppose that $x(t)$ is bandlimited. Then, the M filtered signals are sampled at a sampling rate $Fs = \frac{Fclk}{M}$, where $Fclk$ is the global sampling rate and M is the number of subbands. This differs from the case of DT-HFB where the input signal had to be sampled at the global sampling rate. After that, the digital signals $x_0(n)$, $x_1(n)$,…, $x_{M-1}(n)$ are quantified, upsampled and filtered by the digital filters $F_0(z)$, $F_1(z)$,…, $F_{M-1}(z)$. Finally, the output results from the addition of the signals at the output of the digital filters. We choose the analog filters $H_m(s)$ and the digital filters $F_m(s)$ such that the output $y(n)$ is as close as possible to the analog input signal.

The advantage of this architecture with continuous-time analog filters is that we can work at high frequencies, compared to switched-capacitors. The major disadvantage is the sensitivity to realization errors, compared to discrete-time filters.
Many articles on continuous-time hybrid filter banks have been issued. A frequency analysis of HFB can be found in [34], [35] and [36]. Many synthesis methods for 2-channel HFB have been proposed in [34], [37], [38], [39], [40], [41]. Synthesis methods for more than 2 subbands are in [36], [42], [43].
In [44] and [45], ideal transfer functions of analog filters have been calculated from a discrete-time HFB. Quantization noise is studied in [34]. An analysis of mismatches between the subband ADCs is proposed in [34], [36] and [46]. Some design techniques have been patented by Velazquez [47], [48], [49].
[50], [51], [52], [53], [54], [55] [56] are Supélec's contributions to synthesis methods with realization constraints. There are some examples of 8-channel HFB.

### 2.2.3 Conclusion

As Time-Interleaving architectures are well-covered in literature, we will focus on HFB in Part 4. Yet, there is another intuitive architecture that does not appear in literature. It consists in splitting the input spectrum into subbands and simply converting the subbands. We propose a study of this architecture in Part 3. In this part, we will need many sampling methods. They are recalled in the following section.

## 2.3 Sampling

ADCs have two functions: sampling and quantizing. In this section, we focus on sampling that is the process of going from continuous-time signals to discrete-time signals.
Fig.2. 17 shows a sampler that samples the continuous-time signal $x(t)$ at the sampling period $Ts$.

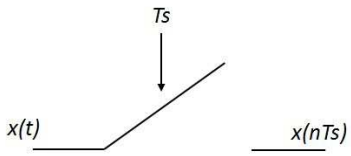


**Fig.2. 17 - Sampler**

### 2.3.1 Introduction

Ideal sampling process does not cause any information loss, provided the Shannon condition is fulfilled.
A real signal, from $Fmin$ to $Fmax$, with a bandwidth $B$, must be sampled at a rate $Fs$ chosen to avoid aliasing:

$$Fs > 2Fmax, \tag{2.1}$$

$Fs = 2Fmax$ is called the Nyquist rate. In case of a baseband signal, we have $Fmax = B$, so (2.1) is equivalent to:

$$Fs > 2B \tag{2.2}$$

Yet, for some applications we prefer having a sampling rate much greater than the Nyquist rate. Indeed, oversampling could be useful to relax the anti-aliasing filter, or decrease the white noises (quantization, kT/C…) density in the wanted channel bandwidth by spreading these noises over a wider bandwidth.

### 2.3.2 Bandpass sampling

Bandpass sampling is applied to bandpass signals. It can downconvert a signal without any mixer.

#### *2.3.2.1 Bandpass sampling of a bandpass signal*

In [57], the theory of bandpass sampling is explained. We consider a bandpass signal as follows:

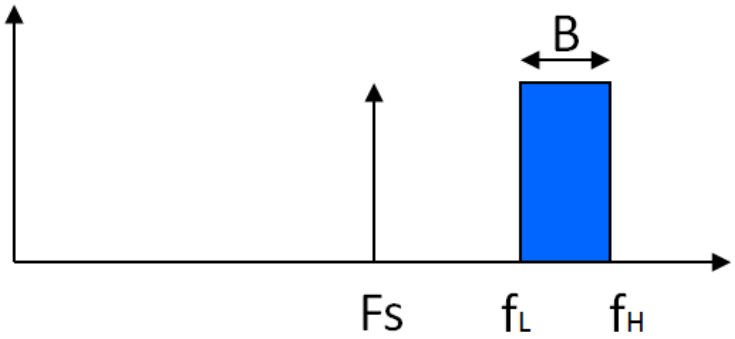


**Fig.2. 18 - Bandpass signal description**

The bandpass signal is located between $f_L$ and $f_H$. Its bandwidth is $B$. $Fs$ is the sampling rate. We notice that $Fs$ is lower than $f_L$. Yet, $Fs$ should be carefully chosen to avoid aliasing.

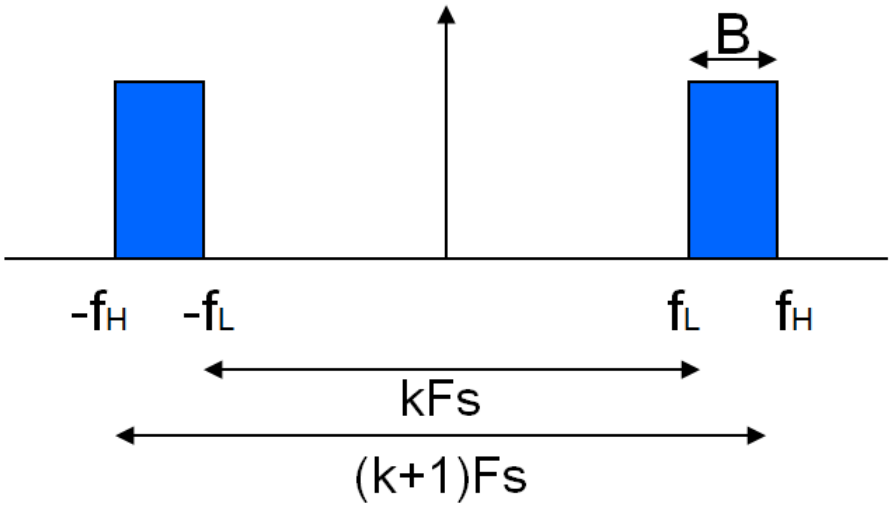


**Fig.2. 19 - Bandpass sampling**

Sampling rates should fulfill the following equations:

$$-f_L + kFs \leq f_L \quad (2.3)$$

$$-f_H + (k+1)Fs \geq f_H \quad (2.4)$$

$$Fs \leq \frac{2f_L}{k} \quad (2.5)$$

$$Fs \geq \frac{2f_H}{k+1} \tag{2.6}$$

$$\frac{2f_H}{k+1} \leq Fs \leq \frac{2f_L}{k} \tag{2.7}$$

We notice that (2.7) is equivalent to Shannon's theorem for k = 0:

$$2f_H \leq Fs \tag{2.8}$$

From (2.7), we can determine allowed and disallowed bands for $Fs$. Indeed, each allowed band has a width $B_{a,k}$ that depends on k:

$$B_{a,k} = \frac{2f_L}{k} - \frac{2f_H}{k+1} \tag{2.9}$$

$$B_{a,k} = \frac{2}{k(k+1)}(f_L - kB) \tag{2.10}$$

Thanks to (2.10), we see that (2.7) is true while k respects:

$$k \leq floor\left(\frac{f_L}{B}\right) \tag{2.11}$$

Furthermore, we can evaluate the bandwidth $B_{d,k}$ of disallowed bands that also depends on k:

$$B_{d,k} = \frac{2f_H}{k+1} - \frac{2f_L}{k+1} \tag{2.12}$$

$$B_{d,k} = \frac{2}{k+1}B \tag{2.13}$$

Fig.2. 20 gives an example of allowed and disallowed bands for $Fs$.

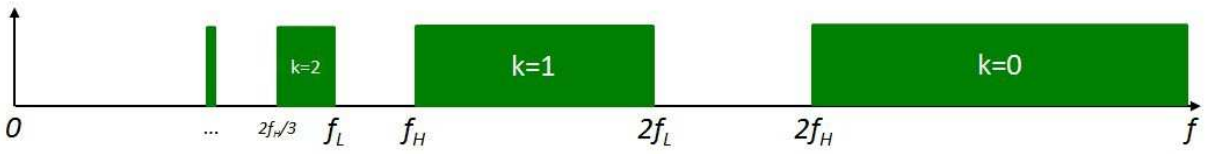


**Fig.2. 20 - Allowed (green) and disabled bands**

### *2.3.2.2 Bandpass sampling of contiguous spectra*

Bandpass sampling could also be applied to a bandpass signal that is adjacent to other unwanted signals, as in [58] where a shift of the desired subband is proposed so that there is no need for RF bandpass filters at the front-end.

Let's introduce the notation and adapt them to our case:

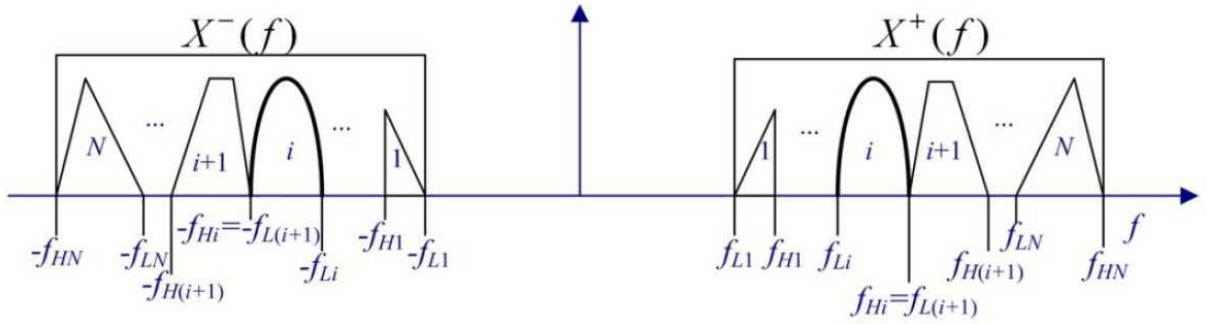


**Fig.2. 21 - Contiguous spectra of a set of N RF signals from [58]**

As explained in [58], we consider a set of N RF signals and the i[th] one is located between $f_{Li}$ Hz and $f_{Hi}$ Hz with a bandwidth of $B_i = f_{Hi} - f_{Li}$, where i =1,2…N. The i[th] RF signals can be

denoted as $X_i^+(f)$ and negative spectrum $X_i^-(f)$, where i =1,2….N. As a whole, these N RF signals can be denoted as $X(f)$, with the positive spectrum $X^+(f)$ and negative spectrum $X^-(f)$. For the sake of simplicity, assume that the spectrums of these multiple RF signals are contiguous, i.e. $f_{L(i+1)} = f_{Hi}$, where i = 1,2…N -1, as depicted in Fig.2. 21.
In our case, we have M contiguous RF signals: the M subbands. $X(f)$ corresponds to the whole input spectrum, so $f_{L1} = 50MHz$, $f_{HN} = 1GHz$ and $W = f_{HN} - f_{L1} = 950MHz$. As we consider M subbands with equal bandwidths, we have:

$$B_i = B = \frac{W}{M} \tag{2.14}$$

Fig.2. 22 depicts the spectrums of the N RF signals and their replicas after sampling.

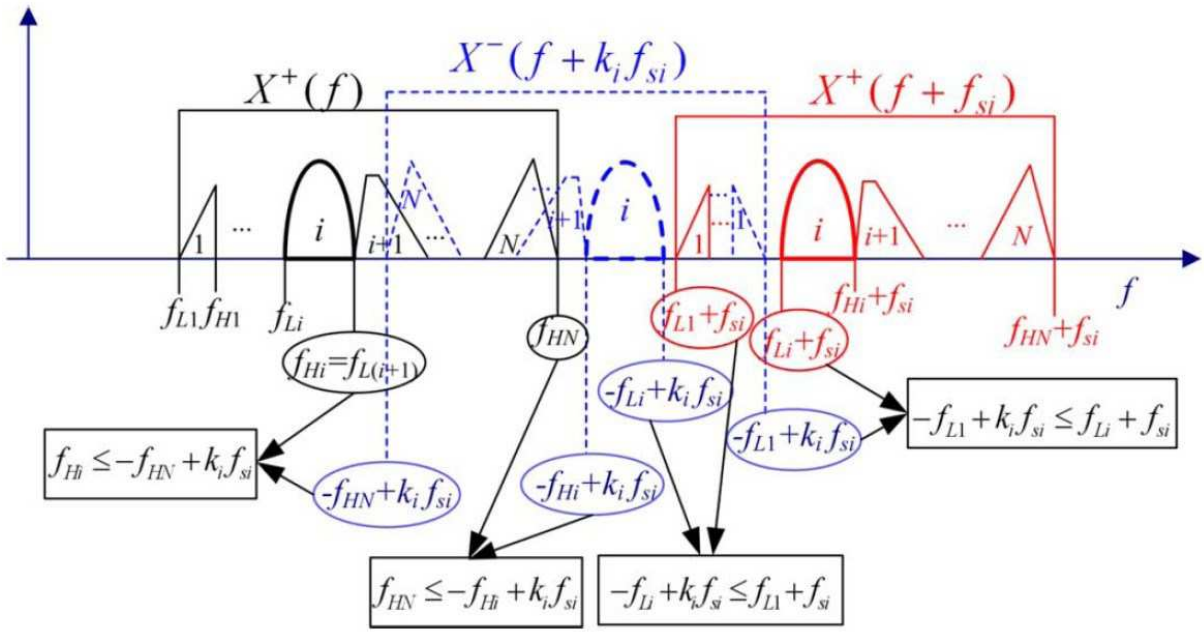


**Fig.2. 22 - Spectra of the N RF signals and their replicas after sampling from [58]**

To cause no aliasing, we should fulfill the following conditions:

$$-f_{Hi} + k_i f_{si} \geq f_{HN} \tag{2.15}$$
$$-f_{Li} + k_i f_{si} \leq f_{L1} + f_{si} \tag{2.16}$$

In [58], one also defines:

$$n_i = floor\left(\frac{f_{HN} + f_{Hi}}{W + B_i}\right) \tag{2.17}$$

And the minimum valid sampling frequency for the i[th] RF signal is given by:

$$f_{si} = \frac{f_{HN} + f_{Hi}}{n_i} \tag{2.18}$$

So, the higher $n_i$, the lower $f_{si}$.
We have thus a method to reduce the sampling rate for bandpass signals.

### 2.3.3 Complex sampling

#### *2.3.3.1 Euler equations*

We recall here the expression of a cosinus and a sinus at the frequency $f_0$:

$$\cos 2\pi f_0 t = \frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} \tag{2.19}$$

$$\sin 2\pi f_0 t = \frac{e^{j2\pi f_0 t} - e^{-j2\pi f_0 t}}{2j} = j\frac{e^{-j2\pi f_0 t}}{2} - j\frac{e^{j2\pi f_0 t}}{2} \tag{2.20}$$

Fig.2. 23 depicts the corresponding plots ((2.19) and (2.20)), in both time and frequency domain:

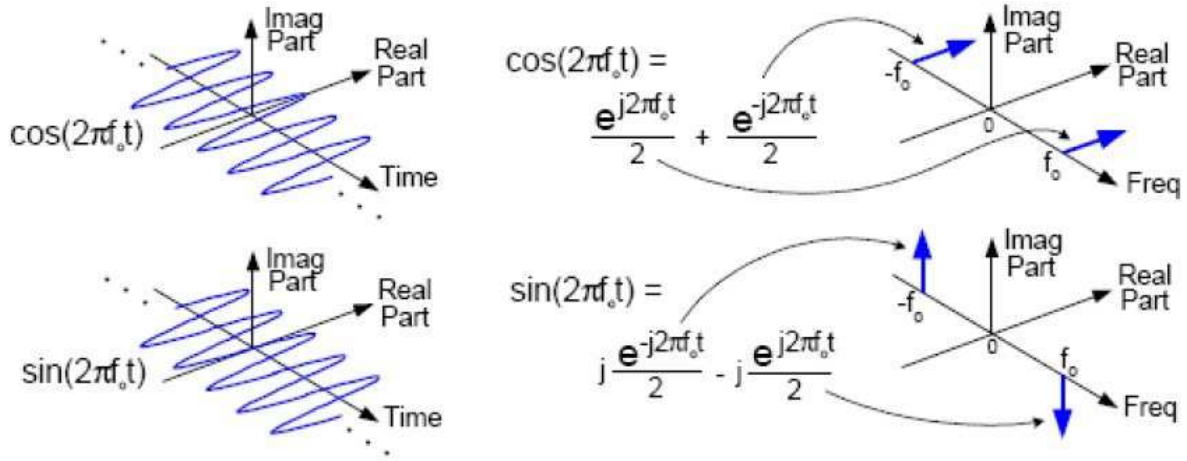


**Fig.2. 23 - Representation of sinus and cosinus in time and frequency domain**

If we multiply the sinus by $j$, that is equivalent to shift by $\frac{\pi}{2}$, we have:

$$j \sin 2\pi f_0 t = \frac{e^{j2\pi f_0 t} - e^{-j2\pi f_0 t}}{2} \tag{2.21}$$

Then, we find the Euler's equation by adding (2.19) and (2.21):

$$\cos 2\pi f_0 t + j \sin 2\pi f_0 t = e^{j2\pi f_0 t} \tag{2.22}$$

Fig.2. 24 depicts the corresponding plots in frequency domain:

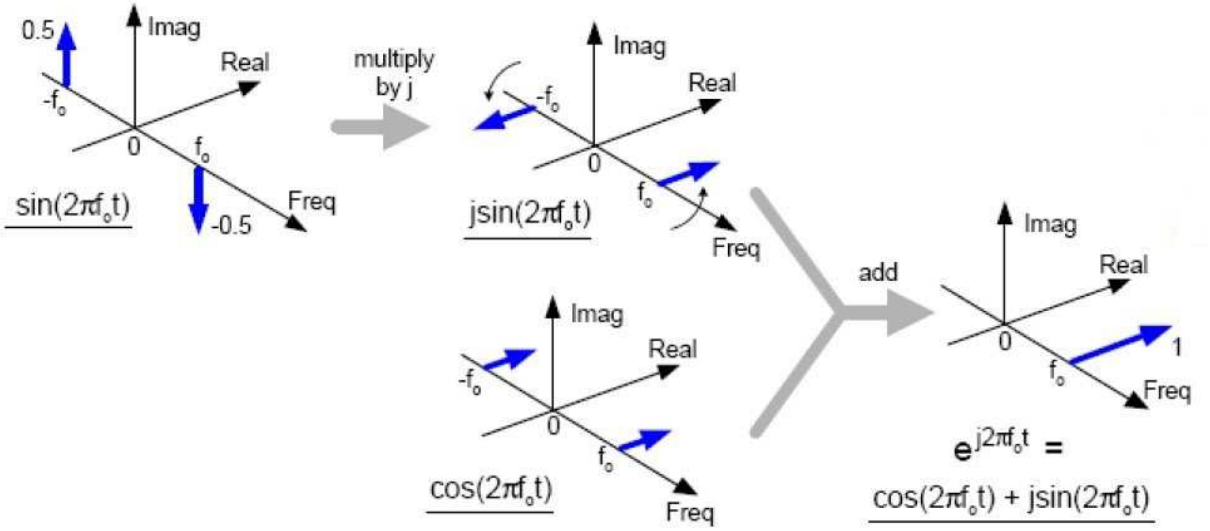


**Fig.2. 24 - Representation of Euler's equation in frequency domain**

In other words, in complex domain, it is possible to avoid negative frequencies.
In our example, the input signal is real, thus its spectrum is symmetric, as depicted in Fig.2. 25:

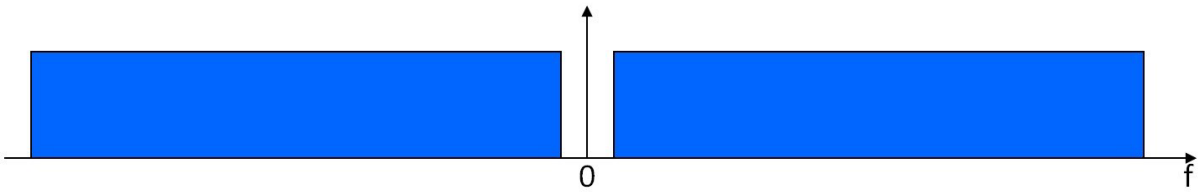


**Fig.2. 25 - Real input spectrum**

The corresponding graph with a complex input spectrum is depicted in Fig.2. 26:

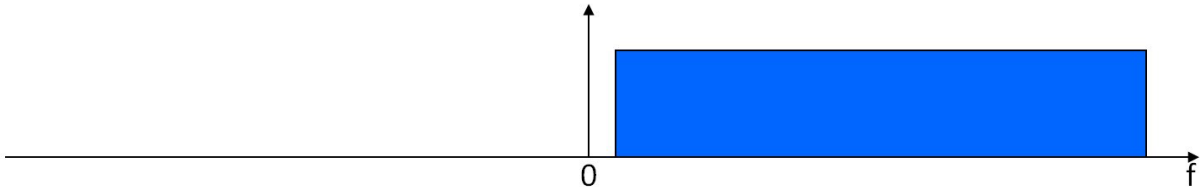


**Fig.2. 26 - Complex input spectrum**

### *2.3.3.2 Hilbert transform*

A signal which has no negative frequency components is called an analytic signal.
The real-to-complex transformation is called the Hilbert transformation.
A filter can be constructed which shifts each sinusoidal component by a quarter cycle. This is called a Hilbert transform filter, such as, for example, Passive Polyphase Filters (PPF) that suppress or at least, attenuate much negative frequencies. This type of filters will be mentioned in Part 3.
So, when a real signal $x(t)$ and its Hilbert transform $y(t) = Ht(x)$ are used to form a new complex signal $z(t) = x(t) + jy(t)$, the signal $z(t)$ is the (complex) analytic signal corresponding to the real signal $x(t)$.
As an example, if we have:

$$x(t) = Acos(2\pi f_0 t), \quad (2.23)$$

then

$$y(t) = Ht\big(x(t)\big) = Asin(2\pi f_0 t) \quad (2.24)$$

and

$$z(t) = x(t) + jy(t) = Ae^{j2\pi f_0 t}. \quad (2.25)$$

We find the Euler's equation again.
Fig.2. 27 shows the block diagram for complex sampling with the Hilbert filter and two ADCs.

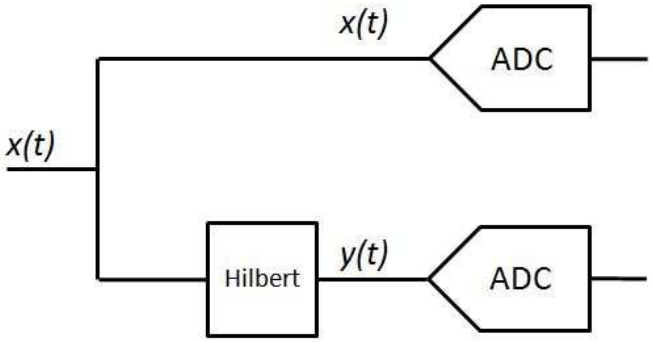


**Fig.2. 27 - Block diagram for complex sampling**

Thus, thanks to filters as polyphase filters, negative frequencies can be suppressed. This has obviously an impact on the choice of the sampling rate.

#### *2.3.3.3 Shannon's theorem*

As mentioned in 2.3.1, (2.1), Shannon's theorem for a real signal is:

$$Fs > 2Fmax$$

This sampling rate is chosen to avoid aliasing. Indeed, sampling is equivalent to replicate the pattern every multiple of Fs. In case of a real signal, the pattern is composed of positive frequencies and negative frequencies. So, we should choose Fs such that the negative frequencies do not recover the positive frequencies. In case of an analytic signal, there are no negative frequencies and thus, Shannon's condition could be reformulated as:

$$Fs > B \tag{2.26}$$

where $B$ is the bandwidth.
(2.26) is very interesting for wideband input signals since the constraint on the sampling rate is relaxed, but at the cost of doubling the number of channels. We notice that the value of $Fmax$ is not important here, thus this formula is valid wherever the input spectrum is located in the spectrum. We will see in Part 3 that this property is very interesting.

### 2.3.4 Conclusion

In this section, we have recalled many methods of sampling, particularly bandpass sampling and complex sampling. These methods will be used in Part 3.

## 2.4 Conclusion

Parallel architectures have been presented and Hybrid Filter Banks will be developed in Part 4. However, there is an other intuitive architecture that does not appear in literature. It consists in splitting the input spectrum into subbands and simply converting the subbands. We propose a study of this architecture in Part 3, where bandpass sampling and complex sampling will be used to reduce the sampling rate of the ADCs.

# 3 Study of RF Filter Banks (RFFB)

The aim of this part is to study an architecture simply composed of a bank of analog filters and a bank of ADCs. We call this architecture RF Filter Banks (RFFB). This is a kind of parallel architecture that is not described in literature but is, though, very intuitive. To cope with the problem of broadband digitization, we propose here to split the input spectrum into subbands with analog filters and then to convert each subband with an ADC. Compared to HFB, this simply corresponds to the analysis part. This architecture will be studied with real signals and analytic signals. Finally, we give a comparison of this architecture with a reference ADC.

## 3.1 RFFB

Fig.3. 1 shows the RFFB architecture. In this study, we do take into account neither the LNA nor the possible equalizer as it is valid for all the following architectures. So, as a shortcut, we will use "input spectrum" instead of "LNA output". As depicted on the following picture, the input spectrum is split into M subbands thanks to analog filters such that they cover the whole band. A study of these analog filters is proposed later and we consider bandpass filters on the figure. We suppose that the ADCs are driven by a Full-Scale signal thanks to RF AGCs.

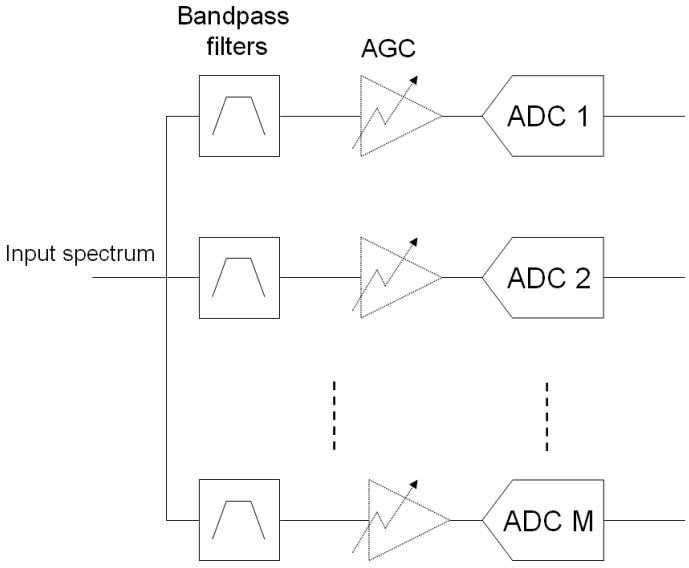


**Fig.3. 1 - RFFB architecture**

This study mainly focuses on the performances of the ADCs in order to relax their constraints. First, we will study the roles of the analog filters and their influence on the requirements of ADCs. We will apply different methods so as to reduce the sampling rate and evaluate the trade-off with the complexity of the filters. Then, analytic signals will be considered and a solution will be proposed.

### 3.1.1 Analog filters

Analog filters have two main functions: reject power and attenuate aliasing. First, we will define and see the impact of power rejection, particularly the reduction of the requirement on SNR. Then, we will specify aliasing rejection and with this in mind, we will choose the best type of filters among the most famous ones such as Butterworth, Elliptic and Chebyshev.

#### *3.1.1.1 Power rejection*

##### 3.1.1.1.1 Definition

A signal that is selected by a bandpass filter looses power. For instance, Fig.3. 2 shows the difference between the input spectrum and the spectrum after filtering. $P_{want,in}$ is the power of the wanted signal and $P_{tot,in}$ is the power of the total spectrum, before filtering. $P_{want,out}$ and $P_{tot,out}$ are the power of the wanted and total spectrum respectively, after filtering. As the input spectrum is flat, the output spectrum takes the shape of the bandpass filter. The signal power decreases when passing through the filter. We consider that the gain in the passband is not 0dB, thus the wanted signal would be attenuated and $P_{want,out} \neq P_{want,in}$.

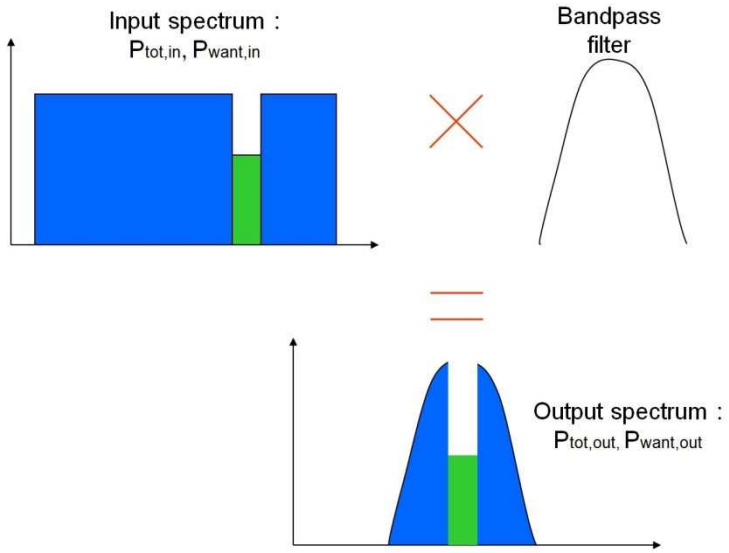


**Fig.3. 2 - Power rejection**

Power rejection, $RejPow$, is defined as the difference between the power at input and power after filtering:

$$RejPow = \left(P_{tot,in} - P_{tot,out}\right) - \left(P_{want,in} - P_{want,out}\right) \quad (3.1)$$

As defined in the introduction, the Desired to total Undesired power ratio is:

$$D/U_{tot} = P_{want} - P_{tot}$$

Thus

$$RejPow = (D/U_{tot})_{out} - (D/U_{tot})_{in} \quad (3.2)$$

$RejPow$ is a negative value. Let us see the relations between power rejection and the other parameters.

#### 3.1.1.1.2 Relations between parameters

Let us recall here the equation (1.19), that is valid for the equivalent single Nyquist ADC, as seen in the introduction:

$$SNR_{Nyquist} = D/U_{tot} - 10\log\left(\frac{Fclk}{2 \times SR}\right) + C$$

Where $C$ is reasonably considered as a constant value that is:

$$C = Backoff + CF + Es/N0 + Margin - 3 \quad (3.3)$$

But we have added analog filters to reject power. We assume that the M filters are identical with the same power rejection.
Then (1.19) becomes:

$$SNR_k = (D/U_{tot})_{out} - 10\log\left(\frac{Fs}{2 \times SR}\right) + C \quad (3.4)$$

where $SNR_k$ is the SNR per branch, $Fs$ is the sampling rate of the bank of ADCs.
Thus, subtracting (3.4) by (1.19) gives:

$$SNR_k - SNR_{Nyquist} = (D/U_{tot})_{out} - (D/U_{tot})_{in} - 10\log\left(\frac{Fs}{2 \times SR}\right) + 10\log\left(\frac{Fclk}{2 \times SR}\right) \quad (3.5)$$

$$SNR_k = SNR_{Nyquist} + RejPow + 10\log\left(\frac{Fclk}{Fs}\right) \quad (3.6)$$

From (3.6), we can plot the relations between the parameters.
On the one hand, we assume that $Fs = Fclk$, i.e. that each ADC works at the Nyquist frequency, thus we have a linear relation between SNR and power rejection. SNR required per branch is less than $SNR_{Nyquist}$. In Fig.3. 3, we set $SNR_{Nyquist} = 55dB$. On the other hand, we assume that it is possible to have a unique sampling rate for each subband ADC such that it is a fraction of the global sampling rate, as for parallel architectures:

$$Fs = \frac{Fclk}{M} \quad (3.7)$$

To see the impact of sampling rate reduction, we consider $SNR_k = SNR_{Nyquist}$ and (3.6) becomes:

$$RejPow = -10\log M \quad (3.8)$$

Fig.3. 3 and Fig.3. 4 show the theoretical evolution of SNR per branch (3.9) and M (3.10) with respect to power rejection, given that the analog filters are identical.

$$SNR_k = SNR_{Nyquist} + RejPow \quad (3.9)$$

$$M = 10^{-\left(\frac{RejPow}{10}\right)} \quad (3.10)$$

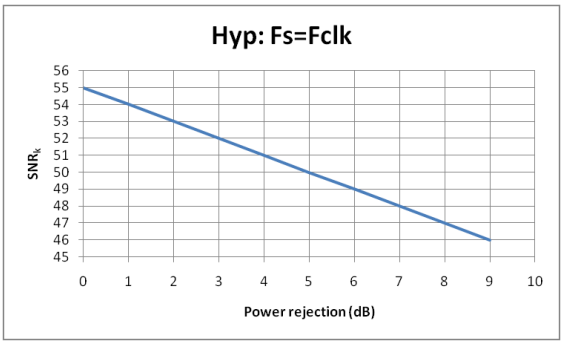


**Fig.3. 3 - $SNR_k$ versus power rejection**

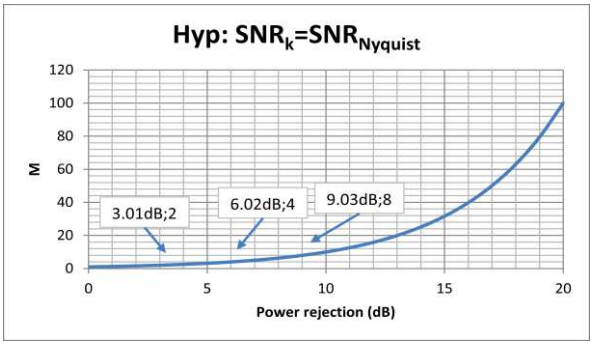


**Fig.3. 4 - M versus power rejection**

We notice that if we want a gain of 20dB on SNR per branch, $SNR_k$, compared to $SNR_{Nyquist}$, we need more than 100 filters ! This is clearly out of our scope because of the corresponding area. Thus, our study focuses only on 2, 4 or even 8 subbands.

### *3.1.1.2 Aliasing rejection*

#### 3.1.1.2.1 Aliasing

Aliasing is a defect due to sampling, as reminded in the introduction. The alias replica could cover the wanted channel and could interfere with the wanted information, if Nyquist's theorem is not fulfilled.
The alias location is predictable since it depends on the Nyquist frequency, which is half the sampling rate, as shown on Fig.3. 5.

#### 3.1.1.2.2 Aliasing rejection

To minimize aliasing impact, we should attenuate the alias subband.
Fig.3. 5.a. shows the input spectrum in blue with the wanted channel in green. After sampling at $Fs$, the wanted channel is recovered by the aliasing, as depicted on Fig.3. 5.b. This implies that the information contained in the wanted channel is lost. One of the solutions when considering the same sampling rate is to add a filter that will attenuate the alias that falls in the wanted channel as shown on Fig.3. 5.c and d.

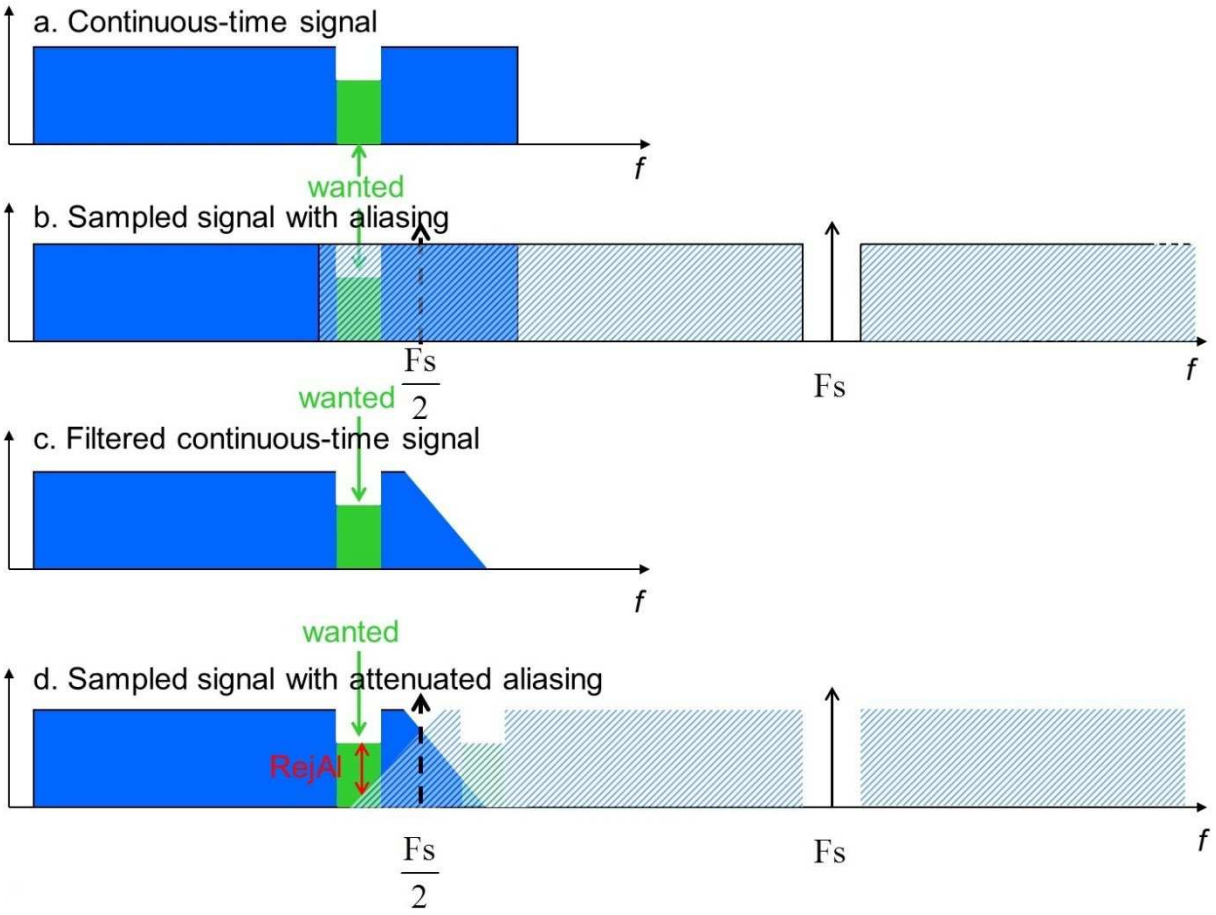


**Fig.3. 5 - Aliasing rejection**

Aliasing rejection is the attenuation of the replica that is required so that it is possible to demodulate the wanted channel. It depends on Es/N0, as shown on the level diagram Fig.3. 6.

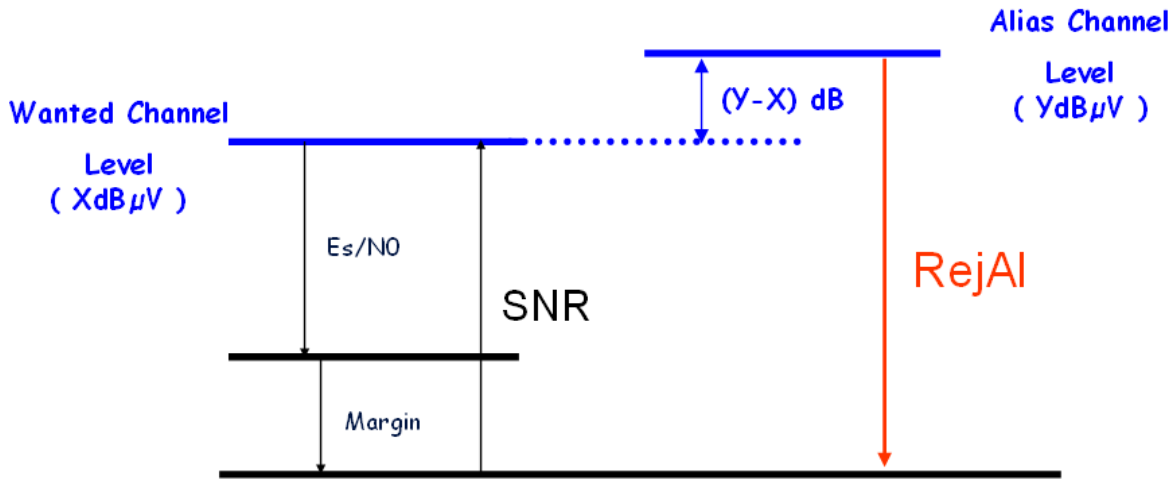


**Fig.3. 6 - Level diagram with wanted and alias channels**

So, aliasing rejection $RejAl$ should be:

$$RejAl = -\left(SNR_{Al} + (Y - X)\right) \tag{3.11}$$

In our case, modulation of the wanted channel is 256QAM so the SNR per channel wanted at the output is Es/N0=29dB. We choose $IL_{Al} = 0.2dB$ and we can calculate the corresponding margin thanks to the formula of APPENDIX A:

$$Margin_{Al} = IL_{Al} - 10\log\left(10^{\frac{IL_{Al}}{10}} - 1\right) \quad (3.12)$$

Thus $Margin_{Al} \approx 13dB$

And

$$SNR_{Al} = \frac{Es}{N0} + Margin_{Al} \quad (3.13)$$

So that $SNR_{Al} \approx 29 + 13 \approx 42dB$

As we have a flat spectrum, we know that the wanted channel level is 11dB lower than the alias channel level in the worst case, as seen in the introduction.Thus, $Y - X = 11dB$.

Therefore, we have $RejAl \approx -(42 + 11) \approx -53dB$

We consider an additional security margin, and then require an aliasing rejection of more than 60dB.

Aliasing could be avoided by choosing a sampling rate that fulfills Nyquist's theorem. Otherwise, aliasing rejection could be performed by filters that could attenuate the replicas. We study different analog filters to find the most suitable type of filters.

### *3.1.1.3 Choice of analog filters*

A filter is specified by its type, its order and its power rejection. Four types have been studied: Butterworth, Elliptic, Chebyshev type I and Chebyshev type II. Given the number of subbands M (2, 4 or 8) and the order, we compare power rejections of all types of filters. These should be as close as possible to theory and be almost constant over the whole band: 50MHz to 1GHz.

#### 3.1.1.3.1 Presentation of the filters

Standard filters are Butterworth, Elliptic, Chebyshev I and Chebyshev II filters. An example of a 3rd-order filter of each type is shown on Fig.3. 7.

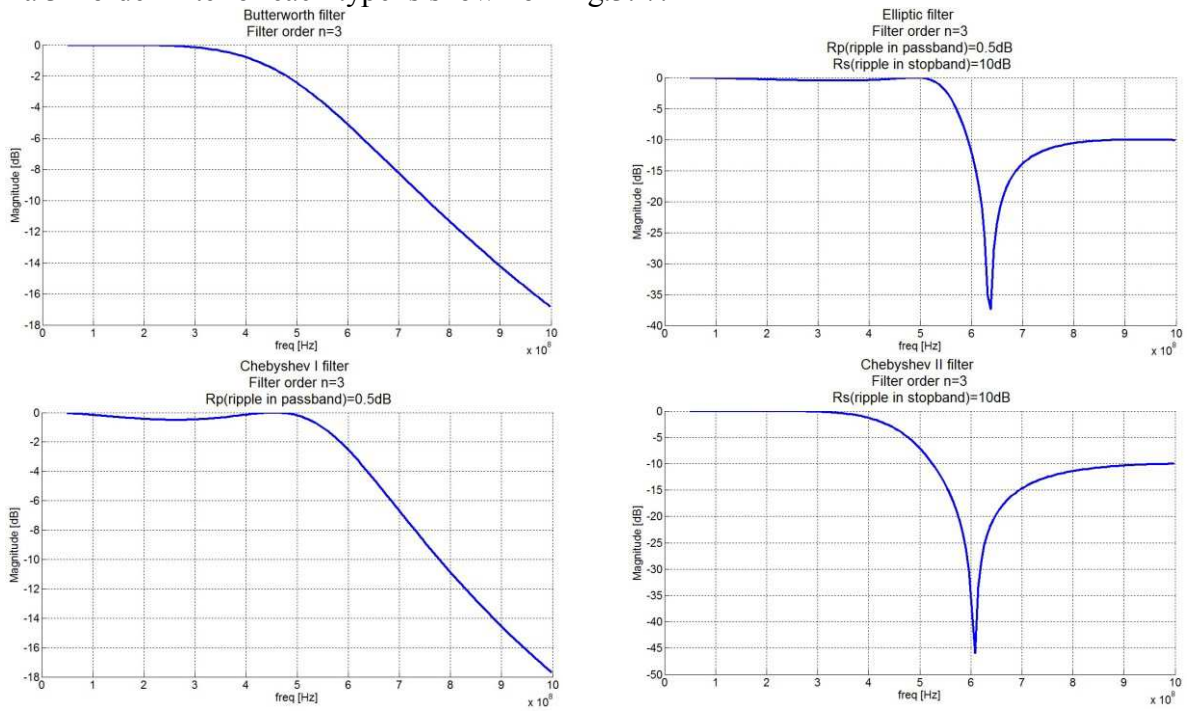


**Fig.3. 7 - Examples of 3rd-order filters**

Table 3. 1 summarizes the main characteristics of the filters. Sharpness is important for aliasing rejection. Ripple is also a parameter that should be carefully chosen. It could decrease the level of the wanted channel in passband, and then degrade the SNR per channel. We can tolerate a ripple of 0.5dB in the passband. As we want to reject aliasing by 60dB, the ripple in the stopband should be at least 60dB.

**Table 3. 1 - Comparison of the different types of filters**

| Filter type | Sharpness | Ripple |
|---|---|---|
| Butterworth | * | No |
| Elliptic | *** | Passband and stopband |
| Chebyshev I | ** | Passband |
| Chebyshev II | | Stopband |

Elliptic filters with a ripple in the passband, $Rp$, less than 0.5dB and with a ripple in the stopband, $Rs$, of at least 60dB seem to fit with our requirements. Fig.3. 8 depicts Elliptic filters for different orders. It is obvious that aliasing will be attenuated by 60dB for frequencies greater than the stopband frequency, and that this frequency decreases as the filter order increases.

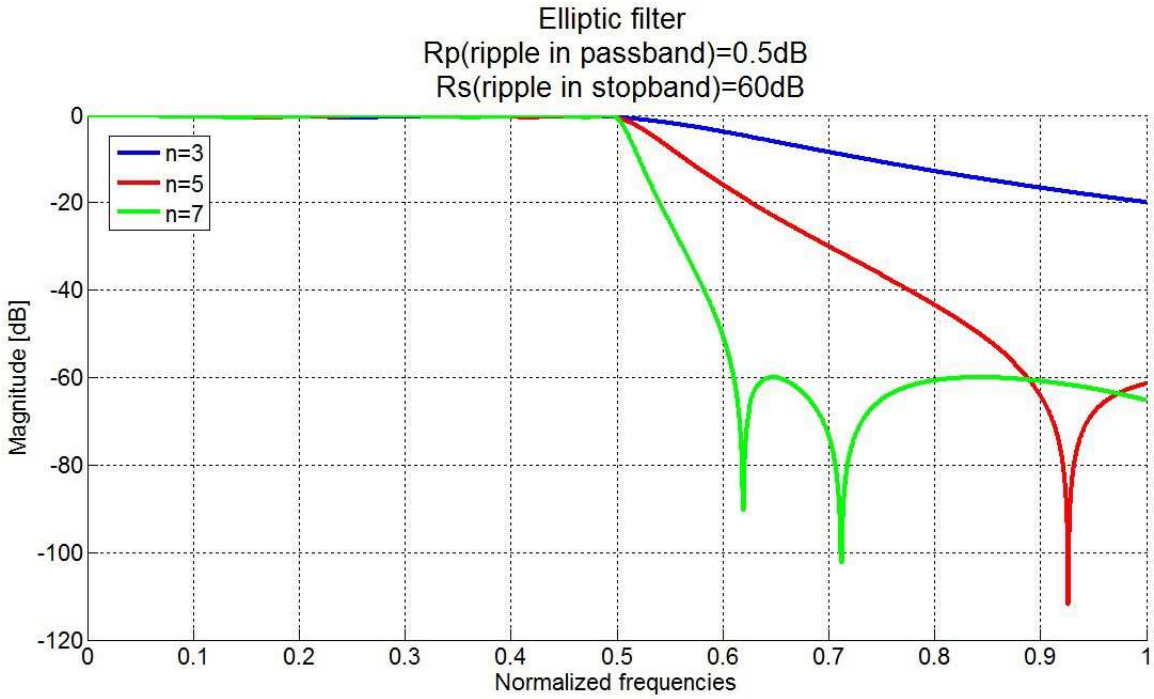


**Fig.3. 8 - Elliptic filters**

We can calculate power rejection, $RejPow$, given that the input spectrum is flat, using (3.1). Table 3. 2 shows power rejection versus the filter order. We have chosen the cutoff frequencies of the filters such that the input subband is divided into two equal subbands (M=2). We notice that the value of power rejection is slightly lower than the 3dB theoretical one, which would be obtained with an ideal brickwall filter.

**Table 3. 2 - Power rejection versus elliptic filter order**

| n | \|RejPow\| |
|---|---|
| 3 | 2,31 |
| 5 | 2,98 |
| 7 | 3,17 |
| ∞ | 3,02 |

This value will be useful to determine the required SNR, thanks to (3.6).

#### 3.1.1.3.2 Application to subband splitting

There are many ways to split the total band into M subbands:

a) M bandpass filters (BPF)
b) 1 LPF + (M-1) BPF
c) 1 LPF + (M-2) BPF + 1 HPF

It seems that the solution c. is the best for our application. Indeed, the first solution could be the more intuitive and selective, but BPFs require more components than LPFs. The solution b. uses a LPF since it costs less than a BPF and there is no power between 0 and 50MHz. It also seems to solve the issue of MoCA at high frequencies (see the introduction). Yet, we could also filter MoCA before subband splitting by using a unique filter, and thus, use a HPF instead for the last subband, as proposed in solution c.
Transfer responses should be quite flat, even at the transition bands. Indeed, if the wanted channel is in a transition band, it should not be attenuated, to guarantee a sufficient SNR. So, we look at the power rejection of the crosspoints

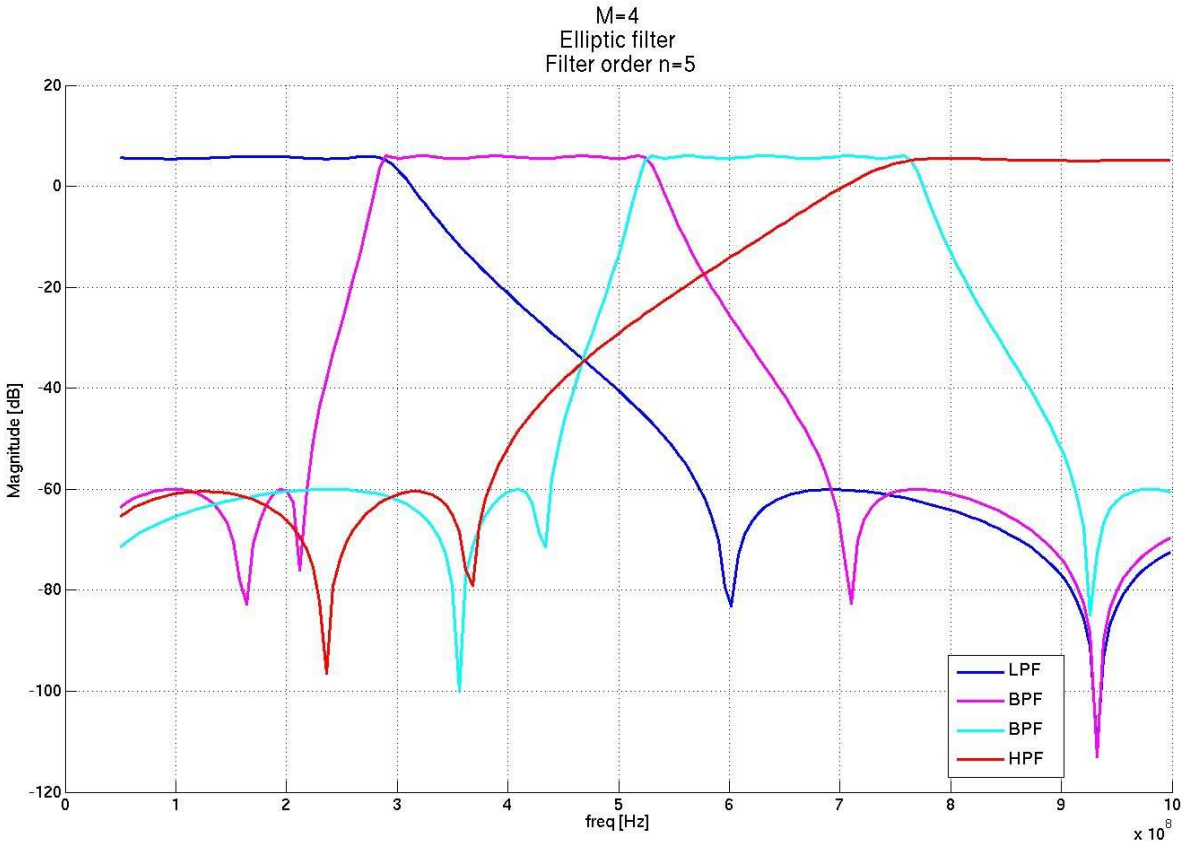


**Fig.3. 9 - Splitting in 4 subbands with 5th-order Elliptic filters**

Fig.3. 9 shows that the whole band from 50MHz to 1GHz is completely covered with a minimum of ripple, even at the transition subbands.

### 3.1.2 Choice of the sampling rate of subband ADCs: Fs

The goal of this section is to identify the optimum sampling rates for each subband. For cost consideration, there is a strong interest in minimizing the number of different VCOs. Therefore, we will seek for the minimum number of unrelated clock frequencies.

We remind here Shannon's theorem, as in (2.1):

$$Fs \geq 2Fmax$$

On Fig.3. 10, we check that aliasing does not fall on the wanted spectrum, with $\frac{Fs}{2} \geq Fmax$ .

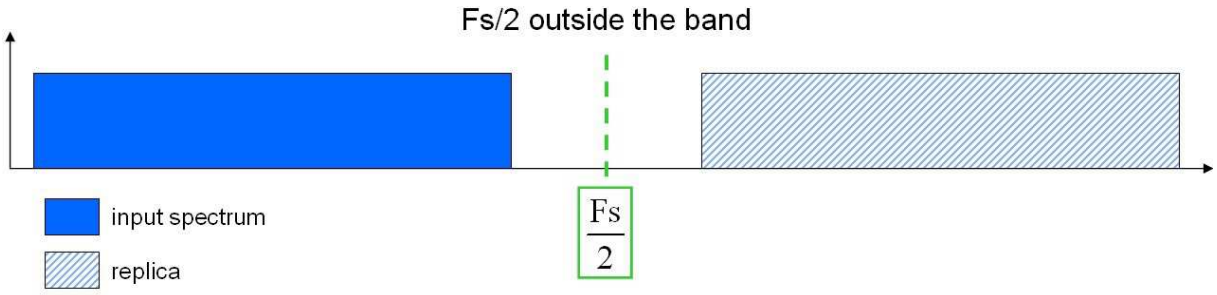


**Fig.3. 10 - Case of non-aliasing**

Now, we try to have a unique sampling rate below the Nyquist rate. So we reduce $Fs$. Fig.3. 11 depicts a case where Shannon's theorem is not respected anymore. Even with an ideal filter, a sampling rate corresponding to this case cannot be used since the channel in which Fs/2 falls would be lost because of auto-aliasing. Auto-aliasing means that the channel is polluted by itself. Thus, this sampling rate is not adapted for (at least) one subband and therefore, it cannot be chosen as the unique sampling rate.

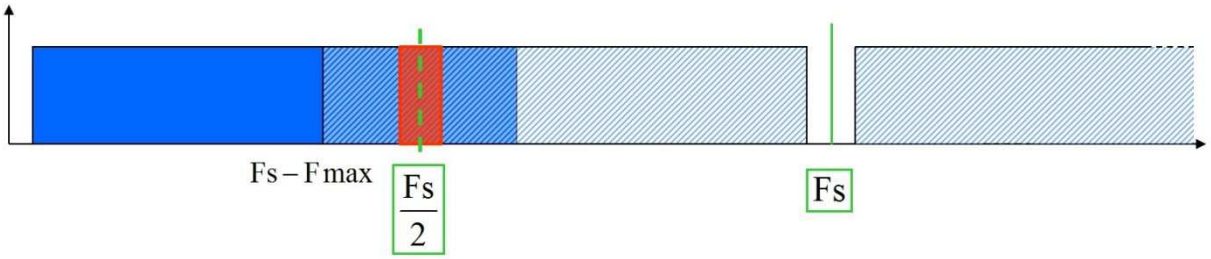


**Fig.3. 11 - Case of partial aliasing**

Yet, we notice that a part of the band is not aliased. This property could be interesting and will be studied later.
To conclude, it is not possible to have a unique sampling rate below the Nyquist rate. Yet, we note that the required SNR per branch is still lower than the global SNR thanks to power rejection.

Therefore, assuming that several sampling rates could be used, we study three different methods to reduce the sampling rate:

a) Splitting into M subbands + Nyquist's theorem

Splitting the input spectrum into M subbands reduces the maximum frequency considered for calculating the minimum Fs, except for the $M^{th}$ subband. Indeed, considering M equal subbands, the maximum frequency of the $k^{th}$ subband will be:

$$Fmax_k = Fmin + k\frac{Fmax - Fmin}{M} \quad (3.14)$$

Thus, we can calculate the minimum allowed sampling rate for each subband:

$$Fs_k \geq 2Fmax_k \quad (3.15)$$

$$Fs_k \geq 2\left(Fmin + k\frac{Fmax - Fmin}{M}\right) \tag{3.16}$$

Table 3. 3 shows the minimum theoretical sampling frequencies that respects Shannon's theorem, after splitting.

**Table 3. 3 - Minimum sampling rate allowed after splitting, with respect to Shannon's theorem**

| M | Subband n° | Bandwidth (Hz) | Fsmin (Hz) |
|---|---|---|---|
| 2 | 1 | 50M → 525M | 1.05M |
| | 2 | 525M → 1G | 2G |
| 4 | 1 | 50M → 287.5M | 575M |
| | 2 | 287.5M → 525M | 1.05G |
| | 3 | 525M → 762.5M | 1.525G |
| | 4 | 762.5M → 1G | 2G |
| 8 | 1 | 50M → 168.75M | 337.5M |
| | 2 | 168.75M → 287.5M | 575M |
| | 3 | 287.5M → 406.25M | 812.5M |
| | 4 | 406.25M → 525M | 1.05G |
| | 5 | 525M → 643.75M | 1.2875G |
| | 6 | 643.75M → 762.5M | 1.525G |
| | 7 | 762.5M → 881.25M | 1.7625G |
| | 8 | 881.25M → 1G | 2G |

For the first subbands, the minimum sampling rates are much lower than the Nyquist rate. Yet, if we consider only this solution, there are as many different sampling frequencies as subbands, which is not an optimal solution.
We notice that the minimum sampling rate for the last subband is 2GHz, which is as high as the sampling rate chosen without splitting.
Practically, the sampling rates cannot be chosen as low as the theoretical one because it would imply ideal filters, i.e. brickwall filters. The sampling frequencies have to be a bit higher than the minimum theoretical value such that the filters could reject aliasing by at least 60dB. Obviously, there is a trade-off between the sampling rate and the complexity of the filter. The lower the sampling rate, the higher the filter orders.

b) Bandpass sampling without filtering

The method of bandpass sampling has been presented in Part 2.
Fig.3. 12 summarizes the notations.

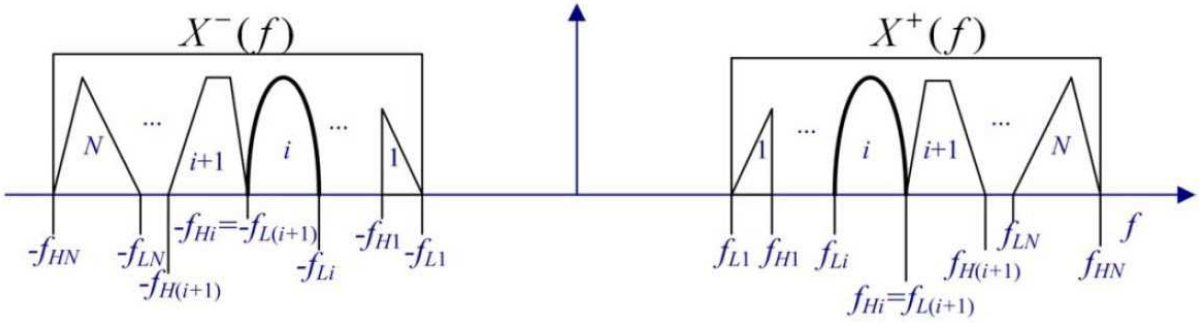


**Fig.3. 12 - Contiguous spectra of a set of N RF signals from [58]**

In our case, we have M contiguous RF signals: the M subbands. $X(f)$ corresponds to the whole input spectrum, so $f_{L1} = 50MHz$, $f_{HN} = 1GHz$ and $W = f_{HN} - f_{L1} = 950MHz$.

As we consider M subbands with equal bandwidths, we have:

$$B_i = B = \frac{W}{M}. \tag{3.17}$$

We have seen ([58], (2.18) and (2.17)) that the choice of the sampling rate for the i[th] subband was defined as:

$$f_{si} = \frac{f_{HN} + f_{Hi}}{n_i}$$

with

$$n_i = floor\left(\frac{f_{HN} + f_{Hi}}{W + B_i}\right)$$

So, the higher $n_i$, the lower $f_{si}$.
Let us see which $n_i$ we can reach.
We know that considering contiguous subbands implies: $f_{Hi} = f_{L(i+1)}$, thus $f_{Hi} = f_{L1} + iB_i$.
From (3.17), we have:

$$f_{Hi} = f_{L1} + i\frac{W}{M} \tag{3.18}$$

Equation (3.18) reported in (2.17) gives:

$$n_i = floor\left(\frac{f_{HN} + f_{L1} + i\frac{W}{M}}{W + \frac{W}{M}}\right). \tag{3.19}$$

We easily see that $n_i$ is max for i = M, so (3.17) becomes:

$$n_{max} = floor\left(\frac{f_{HN} + f_{L1} + W}{W + \frac{W}{M}}\right). \tag{3.20}$$

Now, to have $n_{max}$= 2, we should have:

$$2 \leq \frac{f_{HN} + f_{L1} + W}{W + \frac{W}{M_2}} < 3, \tag{3.21}$$

which leads to:

$$M_2 \geq \frac{W}{f_{L1}}. \tag{3.22}$$

Therefore $M_2 \geq \frac{950M}{50M} = 19$.
So to have $n_i$= 2, we should split the input spectrum into 19 subbands. As implementing 19 subbands is very expensive in terms of surface, we only consider the case where $n_i$= 1, and thus (2.18) gives:

$$f_{si} = f_{HN} + f_{Hi} \tag{3.23}$$

We notice that $f_{si} \geq f_{HN} = 1GHz$, i.e. that we cannot have a sampling rate lower than 1GHz. What is more, as we have, by definition, $f_{Hi} \leq f_{HN}$, then it implies that $2f_{Hi} \leq f_{HN} + f_{Hi} = f_{si}$, which is Shannon's theorem. In other words, in our case, bandpass sampling without filtering is a method that cannot be used to reduce the sampling rate because it is equivalent to Shannon's theorem.
Table 3. 4 shows the minimum sampling rate allowed for each subband.

**Table 3. 4 - Minimum sampling rate allowed after splitting, in case of bandpass sampling without filtering**

| M | Subband n° | Bandwidth (Hz) | Fsmin (GHz) |
|---|---|---|---|
| 2 | 1 | 50M → 525M | 1.525 |
| | 2 | 525M → 1G | 2 |
| 4 | 1 | 50M → 287.5M | 1.2875 |
| | 2 | 287.5M → 525M | 1.525 |
| | 3 | 525M → 762.5M | 1.7625 |
| | 4 | 762.5M → 1G | 2 |
| 8 | 1 | 50M → 168.75M | 1.16875 |
| | 2 | 168.75M → 287.5M | 1.2875 |
| | 3 | 287.5M → 406.25M | 1.40625 |
| | 4 | 406.25M → 525M | 1.525 |
| | 5 | 525M → 643.75M | 1.64375 |
| | 6 | 643.75M → 762.5M | 1.7625 |
| | 7 | 762.5M → 881.25M | 1.88125 |
| | 8 | 881.25M → 1G | 2 |

c) Bandpass sampling after filtering

Bandpass sampling theory has been described in Part 2.
It is possible to downconvert a bandpass signal without a mixer. The bandpass signals are the M subbands obtained after filtering. We have seen that the sampling rate $Fs$ should be carefully chosen, in an allowed band, given by (2.7):

$$\frac{2f_H}{k+1} \leq Fs \leq \frac{2f_L}{k}$$

**Table 3. 5 - Allowed bandwidth for Fs versus k**

| k | Inequations |
|---|---|
| 0 | $2f_H \leq Fs \leq \infty$ |
| 1 | $f_H \leq Fs \leq 2f_L$ |
| 2 | $\frac{2}{3}f_H \leq Fs \leq f_L$ |
| 3 | $\frac{1}{2}f_H \leq Fs \leq \frac{2}{3}f_L$ |
| 4 | $\frac{2}{5}f_H \leq Fs \leq \frac{1}{2}f_L$ |
| 5 | $\frac{1}{3}f_H \leq Fs \leq \frac{2}{5}f_L$ |
| 6 | $\frac{2}{7}f_H \leq Fs \leq \frac{1}{3}f_L$ |
| 7 | $\frac{1}{4}f_H \leq Fs \leq \frac{2}{7}f_L$ |

From (2.11), we can calculate the maximum k for which the inequality is valid:

$$k \leq floor\left(\frac{f_L}{B}\right)$$

Table 3. 6 calculates the maximum value of k, given equation (2.11).

**Table 3. 6 - Validity of inequality**

| M | Subband n° | $f_L$ | B | $k_{max}$ |
|---|---|---|---|---|
| 2 | 1 | 50 | 475 | 0 |
| | 2 | 525 | 475 | 1 |
| 4 | 1 | 50 | 237,5 | 0 |
| | 2 | 287,5 | 237,5 | 1 |
| | 3 | 525 | 237,5 | 2 |
| | 4 | 762,5 | 237,5 | 3 |
| 8 | 1 | 50 | 118,5 | 0 |
| | 2 | 168,5 | 119 | 1 |
| | 3 | 287,5 | 118,75 | 2 |
| | 4 | 406,25 | 118,75 | 3 |
| | 5 | 525 | 118,75 | 4 |
| | 6 | 643,75 | 118,75 | 5 |
| | 7 | 762,5 | 118,75 | 6 |
| | 8 | 881,25 | 118,75 | 7 |

Given Table 3. 5 and Table 3. 6, we are able to determine the allowed and disallowed bands for the cases of 2, 4 and 8 subbands.

i. M=2

Let us summarize these results in Table 3. 7.

**Table 3. 7 - Recap table of allowed bandwidths for Fs, given k and M=2**

| | K | | | | |
|---|---|---|---|---|---|
| | 2 | | 1 | | 0 |
| subband n° | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin |
| 1 | | | ~~525~~ | ~~100~~ | 1050 |
| 2 | ~~666.67~~ | ~~525~~ | 1000 | 1050 | 2000 |


**Fig.3. 13 - Allowed (colored) and disallowed (white) ranges for M=2**

From Fig.3. 13, we notice that a unique sampling rate for both subbands implies that $Fs \geq 2GHz$, which corresponds to Shannon's theorem.

ii. M=4

The same calculations are made with the case of 4 subbands and summarized in Table 3. 8:

**Table 3. 8 - Recap table of allowed bandwidths for Fs, given k and M=4**

| | K | | | | | | |
|---|---|---|---|---|---|---|---|
| | 3 | | 2 | | 1 | | 0 |
| subband n° | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin |
| 1 | | | | | ~~287.5~~ | ~~100~~ | 575 |
| 2 | | | ~~350~~ | ~~287.5~~ | 525 | 575 | 1050 |
| 3 | ~~381.5~~ | ~~350~~ | 508.3 | 525 | 762.5 | 1050 | 1525 |
| 4 | 500 | 508.3 | 666.7 | 762.5 | 1000 | 1525 | 2000 |

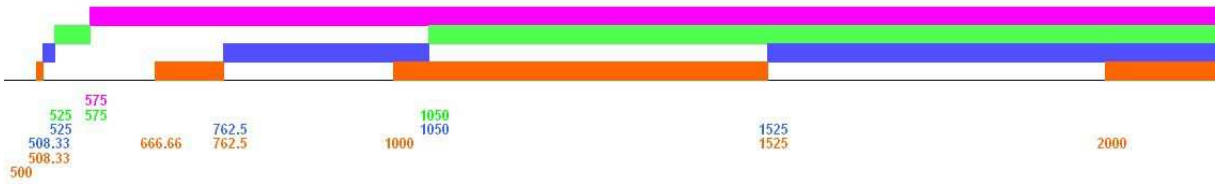


**Fig.3. 14 - Allowed (colored) and disallowed (white) ranges for M=4**

We draw the same conclusion as for the case of M=2, i.e. that a unique sampling rate is possible only if it is greater than 2GHz.

iii. M=8

The same calculations are made with the case of 8 subbands and summarized in Table 3. 9:

**Table 3. 9 - Recap table of allowed bandwidths for Fs, given k and M=8**

| | k | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 |
| subband n° | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin | Fsmax | Fsmin |
| 1 | | | | | | | | | | | | | | | 337.5 |
| 2 | | | | | | | | | | | | | 287.5 | 337.5 | 575 |
| 3 | | | | | | | | | | | 270.8 | 287.5 | 406.3 | 575 | 812.5 |
| 4 | | | | | | | | | 262.5 | 270.8 | 350 | 406.3 | 525 | 812.5 | 1050 |
| 5 | | | | | | | 257.5 | 262.5 | 321.9 | 350 | 429.2 | 525 | 643.8 | 1050 | 1288 |
| 6 | | | | | 254.2 | 257.5 | 305 | 321.9 | 381.3 | 429.2 | 508.3 | 643.8 | 762.5 | 1288 | 1525 |
| 7 | | | 251.8 | 254.2 | 293.8 | 305 | 352.5 | 381.3 | 440.6 | 508.3 | 587.5 | 762.5 | 881.3 | 1525 | 1763 |
| 8 | 250 | 251.8 | 285.7 | 293.8 | 333.3 | 352.5 | 400 | 440.6 | 500 | 587.5 | 666.7 | 881.3 | 1000 | 1763 | 2000 |

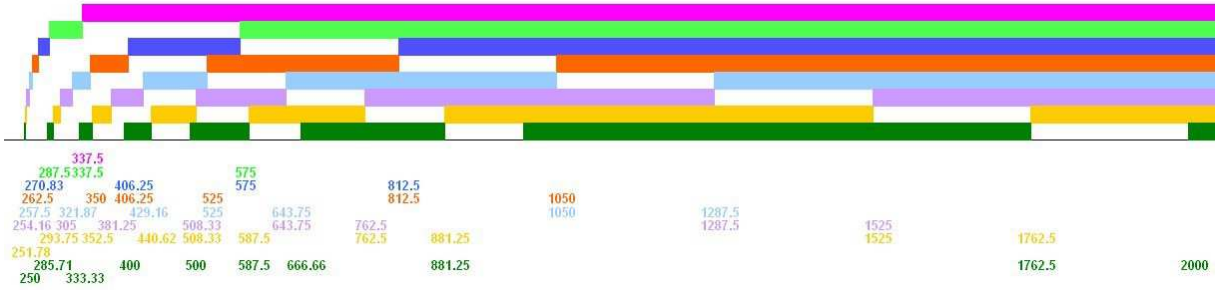


**Fig.3. 15 - Allowed (colored) and disallowed (white) ranges for M=8**

We draw the same conclusions as for the case of M=4, i.e. that a unique sampling rate is possible only if it is greater than 2GHz.
Yet, if we tolerate two different sampling rates, there are several possibilities. For example, we could choose a sampling rate between 1050MHz and 1287.5MHz for subbands 1, 2, 3, 4, 6, 7 and 8. For subband 5, we could have Fs greater than 1287.5MHz. We must be aware of the fact that the sampling rate should not be chosen at the edges of the allowed bands, because it would severly increase much the complexity of the filters.

### 3.1.3 Analytic signals

We have seen in Part 2 that with analytic signals, it is possible to have a unique sampling rate that should respect (2.26):

$$Fs \geq B$$

The choice of $Fs$ is independent on $Fmax$ and thus, this sampling rate is suitable for all subbands and could be unique.
We will first present Passive Polyphase Filters (PPF) that are a commonly used analog implementation of the Hilbert filters.

### *3.1.3.1 Presentation of components*

#### 3.1.3.1.1 Passive Polyphase Filters (PPF)

A polyphase filter generates quadrature signals from a differential input signal. As this "complex" analog signal processing allows to discriminate between positive and negative frequencies, it provides the ability to attenuate signals of positive or negative frequencies. This means that there is no aliasing with respect to Fs/2, so we can reduce $Fs$ such that it respects $Fs \geq B$, where $B$ is the signal bandwidth.

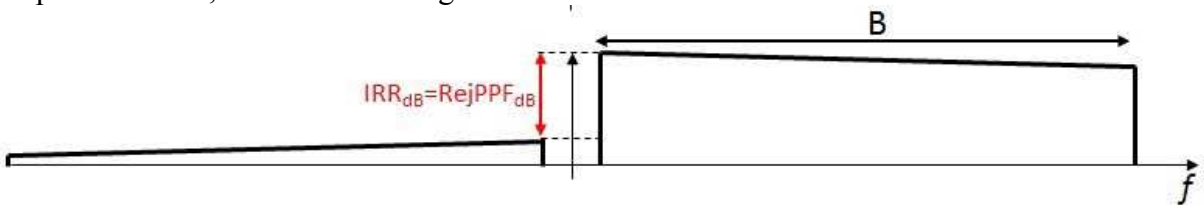


**Fig.3. 16 - Attenuation of negative frequencies on the bandwidth B**

To avoid aliasing, we should attenuate the alias subband. The needed attenuation has been quantified in 3.1.1.2.2 of this part and is evaluated to be at least -53dB. We specify the Image Rejection Ratio (IRR) with an added margin, so that we target IRR=60dB.
Given that $A_{bal}$ and $\Delta\theta$ define the amplitude ratio of I and Q outputs and phase deviation from an ideal 90° between I and Q branches, respectively, we need (see APPENDIX C):

$$A_{bal} = 0.017dB$$

and

$$\Delta\theta = 0.1°$$

So the PPF requires gain and phase errors of 0.01dB and 0.1° respectively (IRR=60dB) over the bandwidth B.

#### 3.1.3.1.2 Analog-to-Digital Converters (ADC)

In case of subband splitting, analog filters (BPF) are added in the architecture to decompose the input spectrum. Thus, to guarantee a full-scale signal at the input of the ADC, an AGC is added, before each ADC, more precisely, after the filters.
The limitation for choosing a low Fs will be the requirements on the filters which should reject aliasing due to Fs by 60dB.
In case of complex signals, an analog-to-digital converter is necessary for each branch I and Q. Nevertheless, the calculation of SNR is the same for analytical signals as for real signals (see APPENDIX D)
We can calculate SNR per branch using (3.6):

$$SNR_k = SNR_{Nyquist} + RejPow + 10\log\left(\frac{Fclk}{Fs}\right)$$

### *3.1.3.2 Comparison of architectures*

To evaluate the influence of analytic signals on the ADC specifications, we take as reference an architecture with a single ADC, shown on Fig.3. 17:

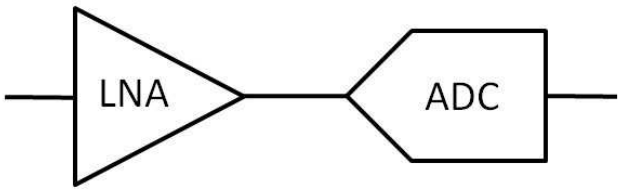


**Fig.3. 17 - Reference architecture**

So, we add a PPF and thus, double the number of ADCs, as depicted on Fig.3. 18:

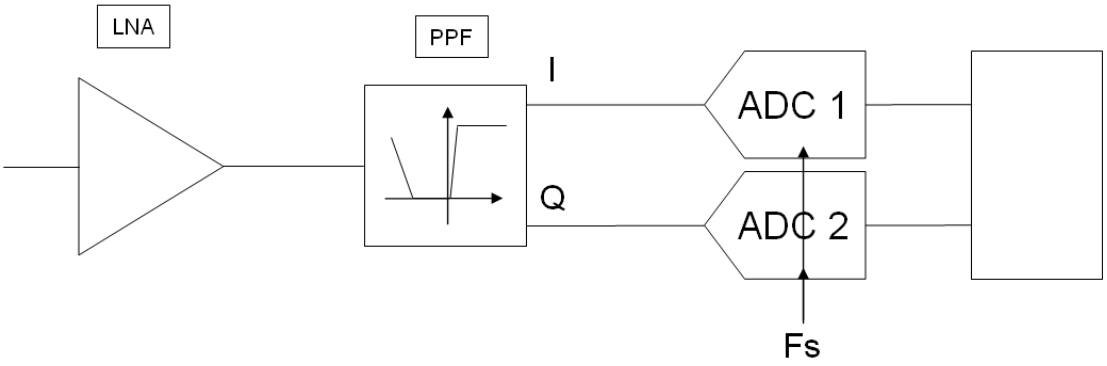


**Fig.3. 18 - Architecture with a wideband PPF, without subband splitting**

The main advantage here is the reduction of the sampling rate. However, the PPF has to attenuate the negative frequencies by at least 60dB, on the whole band, i.e. from 50MHz to 1GHz which is quite challenging.
In this case, $Fs$ is chosen equal to the bandwidth, i.e. 950MHz and thus, SNR is:

$$SNR_k = 55 + 10log\left(\frac{2.6 \times 10^9}{950 \times 10^6}\right) \approx 59.4dB$$

For now, the noise added by the PPF is not taken into account.

**Table 3. 10 - Comparison of real and analytic signals**

| architecture | signal | nb ADCs | Fs (Hz) | SNR (dB) | PPF | |
|---|---|---|---|---|---|---|
| | | | | | BW | $RejPPF_{dB}$ |
| reference | real | 1 | 2,6G | 55 | | |
| PPF+ADCs | analytic | 2 | 950M | 59,4 | whole | 60 |

Now, we add a mixer and study the advantage of such an architecture.

### 3.1.4 Mixing

The motivation for adding a down-conversion stage is to relax the bandwidth of the ADC (Sample-And-Hold). The idea is close to zero-IF/ Near-zero-IF RF architecture: the signal is down-converted to a center intermediate frequency (IF) which is close to DC. We will see that the constraints on IRR could be achieved by the PPF and the mixer together.

### *3.1.4.1 Presentation of components*

Two cases should be considered: Double-Balanced Mixer (DBM) and Quadrature Mixer (QM).

#### 3.1.4.1.1 DBM

Fig.3. 19 shows a Double-Balanced Mixer where RF, LO and IF are real signals. In our case, the RF signals are the output of the polyphase filter, so we will need a DBM for each branch I and Q. If we consider that the polyphase filter rejects the negative frequencies by 60dB, there is no image issue.

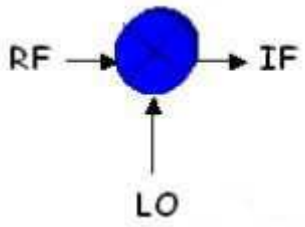


**Fig.3. 19 - Double-balanced mixer (DBM)**

#### 3.1.4.1.2 QM

Fig.3. 20 depicts a Quadrature Mixer where LO and IF are quadrature signals. A polyphase filter could be added after the QM to filter the unwanted signals.

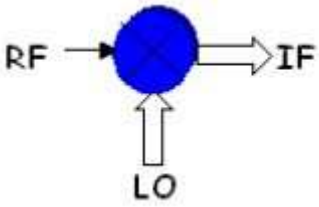


**Fig.3. 20 - Quadrature mixer (QM)**

Added behind the PPF, it becomes a Double Quadrature Mixer (DQM).
We define $RejLO_{dB}$ as the rejection of the negative frequency of the real LO. If the LO was perfectly complex, then $RejLO_{dB}$ would be $-\infty$.

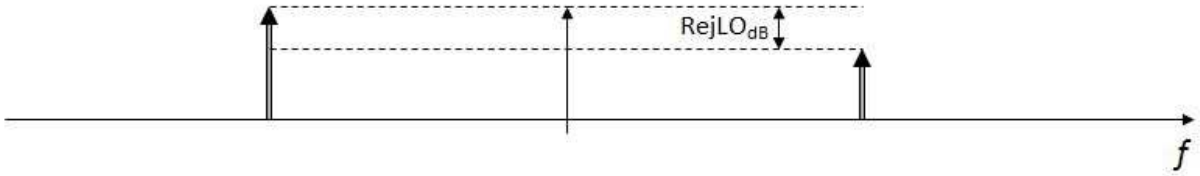


**Fig.3. 21 - Definition of RejLO for complex LO**

The requirement on Image Rejection is still 60dB.

$$IRR \approx RejLO_{dB} + RejPPF_{dB} \tag{3.24}$$

So, the constraints are shared between the PPF and the QM: 30dB each seems to be a good trade-off, as depicted in Fig.3. 22.

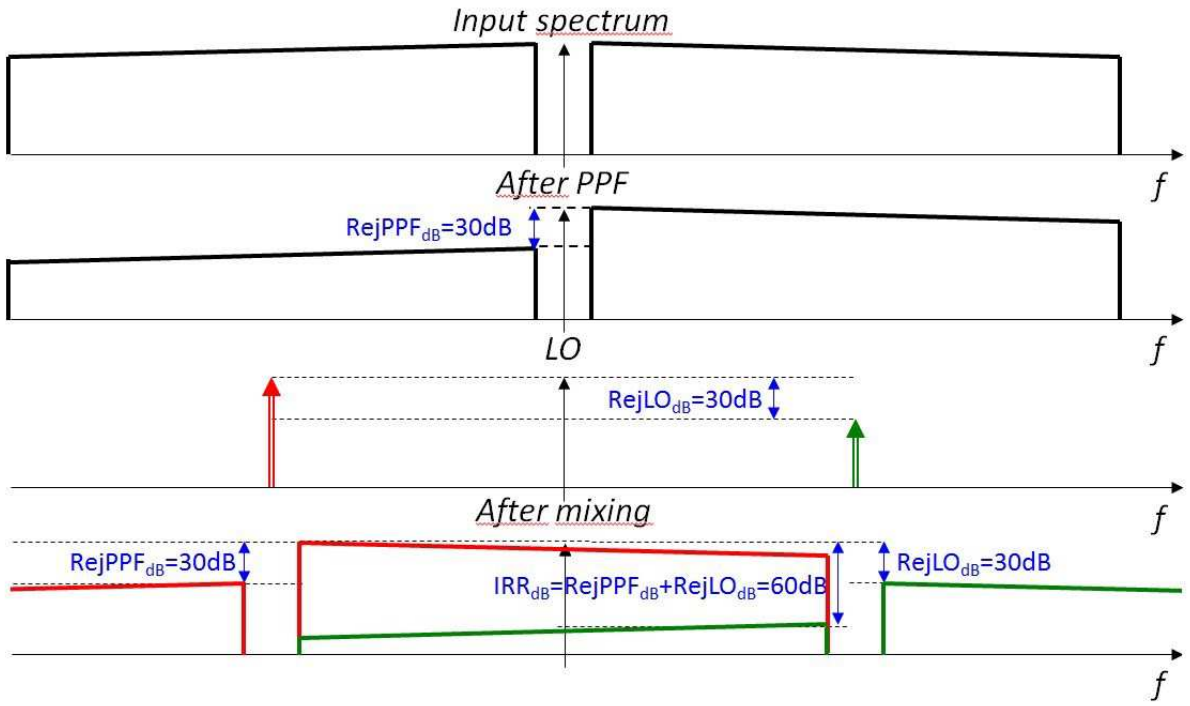


**Fig.3. 22 - Evolution of spectrum after PPF and DQM**

According to APPENDIX C, we know that the PPF requires gain and phase errors of 0.55dB and 3.62° respectively (IRR=30dB) over $-f_L \rightarrow -f_H$.
From now on, the study will be done with DQM to reduce the constraints on the IRR of the PPF and make it feasible.

Now, we may consider two cases of architecture:

- Homodyne architecture or zero-IF architecture

The LO is chosen such that the (sub)band is centered around 0. In case of several subbands, this implies that there will be one LO for each subband, i.e. M LOs. This is not optimal as clock generation is difficult.

- Heterodyne architecture

The LO is chosen such that the (sub)band is downconverted around a lower frequency called Intermediate Frequency (IF). This LO could be unique, even in case of several subbands. Thus, the best choice for the LO frequency is the middle of the whole band:

$$LO = \left(\frac{Fmax + Fmin}{2}\right) \tag{3.25}$$

In the following architectures, the downconverter is a QM with IRR=30dB, and the LO is unique and equal to 525MHz.

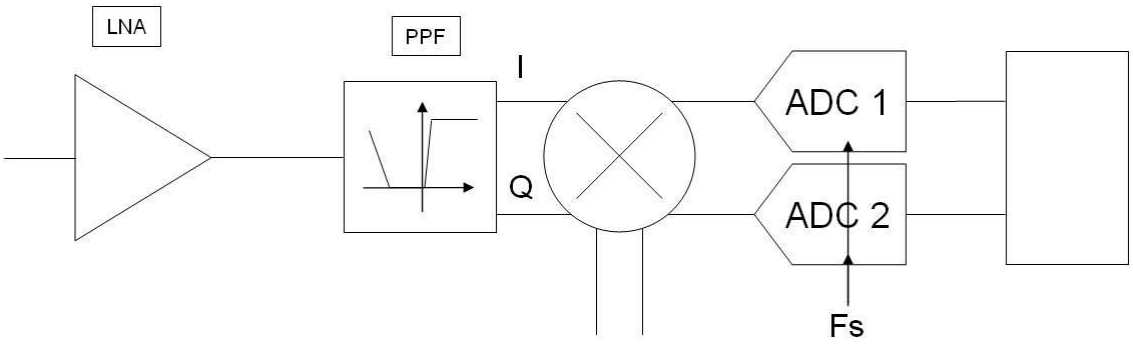


**Fig.3. 23 - Architecture with PPF and mixer**

So, after downconversion, the wanted band has still a bandwidth of 950MHz, but now, from -475M → 475MHz, and thus the maximum frequency at the ADC input is $\frac{Fmax}{2}$, as shown on Table 3. 11. This has no impact on the sampling rate and on the SNR as we intentionally do not take into account the noise of the mixer up to now.

**Table 3. 11 - Comparison between reference ADC and analytic signals with mixer**

| architecture | signal | nb ADCs | Fs (Hz) | SNR (dB) | PPF | | mixer | max $f_{in}$ ADC |
|---|---|---|---|---|---|---|---|---|
| | | | | | BW | $RejPPF_{dB}$ | $RejLO_{dB}$ | |
| reference | real | 1 | 2,6G | 55 | | | | Fmax |
| PPF+ADCs | analytic | 2 | 950M | 59,4 | whole | 60 | | Fmax |
| PPF+mixers+ADCs | analytic | 2 | 950M | 59,4 | whole | 30 | 30 | Fmax/2 |

Subband splitting could reduce the required SNR thanks to power rejection, and also relax the constraints on the PPF because the band to suppress will be narrower.

### 3.1.5 Subband splitting

Table 3. 11 shows that the combination of PPF and mixer is interesting for IRR and maximum input frequency of the ADCs. Yet, the PPF still have to reject the whole bandwidth. Thus, we propose to add analog filters such that they should reject only a subband. Moreover, the filters will also reject power and then, reduce the required SNR (see (3.6)). Unfortunately, the implementation of these filters has a cost in terms of surface and power consumption, since it implies that 2M branches, where M is the number of slices, and this will be studied in the following section.
So, the required SNR is:

$$SNR_k = 55 + 10\log\left(\frac{2.6\times10^9}{950\times10^6}\right) - 10log(M) \approx 59.4 - 10\log(M)$$

As for the requirements on SNR, it depends on the number of subbands, as depicted on Fig.3. 24.

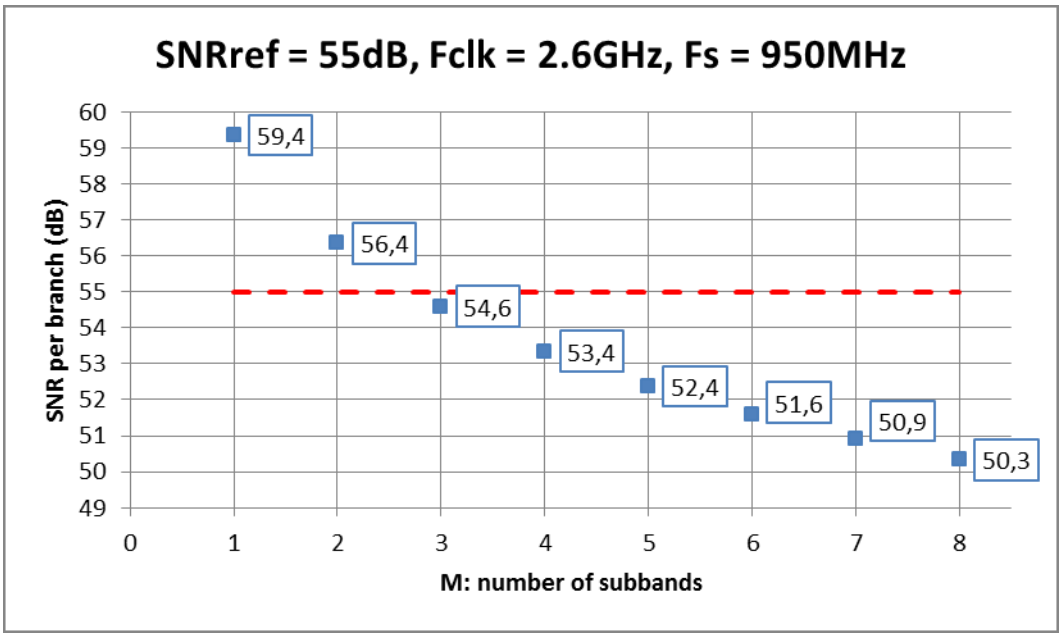


**Fig.3. 24 - SNR per branch versus the number of subbands**

We still do not take into account the noise added by the filters in this study.
These considerations are recapitulated in Table 3. 12.

**Table 3. 12 - Comparison between all architectures**

| architecture | signal | nb ADCs | Fs (Hz) | SNR (dB) | PPF | | mixer | max $f_{in}$ ADC |
|---|---|---|---|---|---|---|---|---|
| | | | | | BW | $RejPPF_{dB}$ | $RejLO_{dB}$ | |
| reference | real | 1 | 2,6G | 55 | | | | Fmax |
| PPF+ADCs | analytic | 2 | 950M | 59,4 | whole | 60 | | Fmax |
| PPF+mixers+ADCs | analytic | 2 | 950M | 59,4 | whole | 30 | 30 | Fmax/2 |
| PPF+mixers+ADCs + subband splitting | analytic | 2M | 950M | < 56,4 | subband | 30 | 30 | Fmax/2 |

The values of the required SNR could be even lower if we increase the sampling rate.

### 3.1.6 Proposed solution

We choose the subband splitting architecture (3.1.5) for several reasons.
We know that clock generation is a major issue. This is the reason why we are concerned about the choice of the frequencies. To have a unique sampling rate, we have added a Passive Polyphase Filter. Then, the signals are analytic and Shannon's theorem is $Fs \geq B$, instead of $Fs \geq 2Fmax$. A Quadrature Mixer has also been added to reduce the maximum input frequency of the ADC on the one hand, and to relax the constraints on the PPF about the IRR. Indeed, the requirement on IRR is shared between the PPF and the mixer. With the issue of clock generation in mind, we choose a unique LO frequency that is equal to 525MHz, the middle of the whole band. Then, we choose the unique sampling rate equal to 1.05GHz, that is twice the frequency of the LO. Furthermore, in this case, the aliasing fall out of the wanted band, so the analog filters could have a low-complexity. Their role is just to reject power, not aliasing and thus we choose simple 3$^{rd}$-order filters. We place these filters before the PPF to relax the constraints on the PPFs. Indeed, they have to reject image on a bandwidth that is smaller than the whole band. Finally, we choose to split the input spectrum into no more than

2 subbands, to avoid the implementation of bandpass filters which have much more components.
Finally, we have to add a lowpass filter per branch as anti-aliasing filters. A similar study as before shows that 4th-order Elliptic filters are necessary.

A study of group delay of the 3rd-order lowpass and highpass Elliptic filters has been done and shows that the maximum group-delay variation for a 6MHz-channel is 80ps and 100ps for the LPF and the HPF respectively, where group delay is, as usual:

$$\tau = -\frac{d\varphi}{dt}. \tag{3.26}$$

It is acceptable as the state-of-the-art is several tens of ns.

We also want IQ mismatches less than 60dB. This should be reachable thanks to digital correction. It is not linked to IRR of PPF and mixer. So we must have a gain error less than 0.01dB and a phase error $\Delta\varphi$ less than 0.1°.

Timing errors between the sampling instants of I&Q ADCs should also be studied. Calling $\Delta t_{clk}$ the difference of sampling instants, we have:

$$\Delta t_{clk} = \frac{\Delta\varphi}{2\pi . F_{carrier}}, \tag{3.27}$$

where $F_{carrier}$ is the frequency of the carrier. Therefore, a timing error between I&Q ADC is equivalent to an IQ phase mismatch. After downconversion, maximum frequency is 475MHz. So the minimum difference tolerated is:

$$\Delta t_{clk} = \frac{0.1}{2\pi \times 475.10^6} = 33.5ps$$

As far as the noise is concerned, the SNR of the ADCs is degraded by 0.36dB.
Fig.3. 25 depicts the proposed architecture.

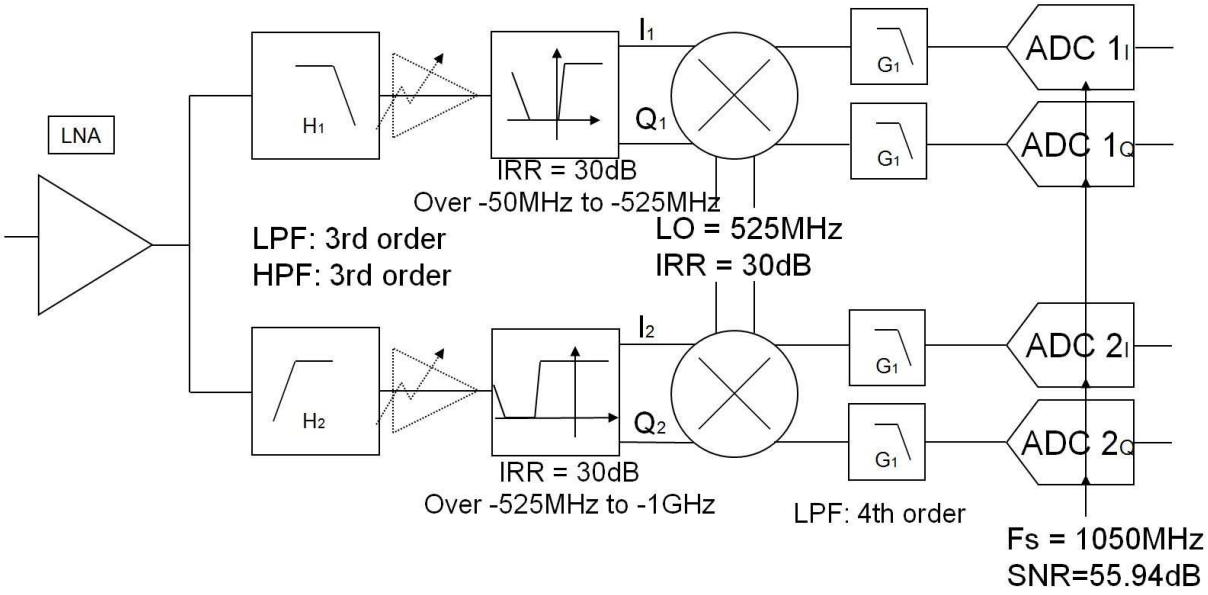


**Fig.3. 25 - Proposed architecture**

## 3.2 Cost function and comparison

For decision purposes, as well as the selection of the best working directions, we need an objective measure of the performances of the different solutions. With this in mind, we introduce a simple, but general cost function. Since the two key parameters are surface and power consumption, we simply choose to define the cost function as the function that associates the two indicators {Surface, Power} to any set of parameters describing the solution.
Next, we estimate the power and surface, thus cost, of the different architectures and then we compare the results with the cost of a single wideband ADC.
As the different architectures involve several ADCs with different specifications, we first review the different Figures of Merit (FoM) of ADCs, choose a reference ADC and see how we can extrapolate power and surface for another ADC with different sampling rate and SNR. The results are combined with state-of-the-art power and surface of the other components of our architecture. Finally, we will be able to compare our proposed architecture to the reference single wideband ADC.

### 3.2.1 Figure of Merit (FoM) of ADCs

In the literature, we find two main definitions of Figure of Merit for ADCs. On the one hand, the FoM links the ENOB, the effective resolution bandwidth (ERBW) and power dissipation P (e.g. [59], [60], [61]):

$$FoM = \frac{P}{2 \times 2^{ENOB} \times ERBW} \tag{3.28}$$

In our case, we assume that the ERBW is always 1GHz, and then, we will consider the sampling rate $Fs$ instead (e.g. [62], [63], [64]):

$$FoM = \frac{P}{2^{ENOB} \times Fs} \tag{3.29}$$

Table 3. 13 shows some examples of FoM for ADCs with performances relatively close to our specifications:

**Table 3. 13 - Examples of FoM**

| | Fs (GHz) | ENOB (bits) | S (mm²) | P (W) | FoM (pJ/conv.step) | Techno (nm) | Type |
|---|---|---|---|---|---|---|---|
| [65] | 2 | 5 | 1.02 | 0.145 | 2.27 | 180 | Flash |
| [66] | 1.1 | 6.5 | 0.37 | 0.092 | 0.92 | 90 | TI Pipeline |
| [67] | 1.35 | 8 | 1.6 | 0.175 | 0.51 | 130 | TI SAR |

### 3.2.2 Reference ADC

To compare our architecture to the architecture that converts directly the input spectrum (after the LNA which is out of the scope), we choose a reference ADC. We have selected [28], which is a Time-Interleaved ADC that has the following characteristics:

**Table 3. 14 - Characteristics of [28]**

| | |
|---|---|
| Pref (W) | 0.48 |
| SNDRref (dB) | 48.5 |
| Fclk (GHz) | 2.6 |
| Sref (mm²) | 5.1 |

Given the SNDR, we can easily calculate the Effective Number Of Bits (ENOB):

$$ENOB = \frac{(SNDR - 1.76)}{6.02} \tag{3.30}$$

So, the ENOB of the reference ADC is around 7.76 bits.
From (3.28), we have $FoM \approx \mathbf{0.85}$pJ/conversion-step.
To properly compare our architecture to an architecture with this ADC, we recalculate the SNR of the four ADCs using (3.6):

$$SNR_k = SNR_{Nyquist} + RejPow + 10\log\left(\frac{Fclk}{Fs}\right)$$

With $SNR_{Nyquist} = SNDR_{ref} = 48.5dB$, $Fs = 1.05GHz$, $Fclk = 2.6GHz$ and $RejPow = -3dB$, we have $SNR_k \approx 49.44dB$. And we deduce that $ENOB \approx 7.92dB$.

### 3.2.3 Power and surface estimation of ADCs

#### *3.2.3.1 Power consumption estimation*

In order to obtain a first estimate of the power consumption, we assume using ADCs with a known, constant, figure of merit FoM. For instance, if the ADCs are in the same family as the reference ADC, we have FoM=0.85pJ/conversion-step. Then, from the $SNR_{Nyquist}$, we deduce the ENOB, and with a given sampling frequency, we are able to estimate the power consumption of each ADC as:

$$P \approx FoM \times 2^{ENOB} \times Fs. \tag{3.31}$$

Applying (3.29) to our case, with FoM=0.85pJ/conversion-step, Fs=1.05GHz and ENOB=7.92 (from SNR=49.44dB), we get P=0.22W. As we have 4 ADCs, we get that the global power consumption is 0.88W.

#### *3.2.3.2 Surface estimation*

The reference ADC is a Time-Interleaved ADC. The number of interleaved elementary ADCs depends on the sampling frequency $Fclk$ of the ADC. The surface $Sref$ of the whole ADC is therefore nearly proportional to the number of unit ADCs. Thus, if we reduce the sampling rate $Fs$, the number of unit ADCs will be reduced proportionally, and so the surface. Indeed, we have:

$$\frac{Fclk}{Fs} = \frac{Sref}{S}. \tag{3.32}$$

Consequently, we will be able to estimate the surface of our ADC, assuming that it is the same technology.

In our case, Fs=1.05GHz, thus the surface of one ADC is S=2.06mm². As we have 4 ADCs, we consider that the global surface is 8.24mm².

Now, we have to look at the power and surface of the components incorporated so as to reduce the constraints on the ADC.

### 3.2.4 Power and surface of the whole architecture

#### *3.2.4.1 Power estimation*

We do not take the subband filters' and the polyphase filters' power consumption into account since they are passive. The power consumption of the AGCs and the mixers are estimated from the state-of-the-art.

**Table 3. 15 - Estimation of power consumption for AGCs, QMs and ADCs**

| AGCs | QM | ADCs |
|---|---|---|
| 119mW | 190mW | 880mW |

Thus, the global reception chain has a power consumption of 1.189W.

*Power saving*

As there is no recombination at the outputs of the analog-to-digital filters, we can imagine to switch-off unused subbands, in order to save power consumption.
We call $n$ the number of channels and $M$ the number of subbands.
The probability of having one channel in one subband is $\frac{1}{M}$. If we focus on an only subband, the probability to get $m$ channels is given by the binomial law:

$$p(m) = \sum_{m} \binom{n}{m} p^m q^{n-m} \tag{3.33}$$

Where $p = \frac{1}{M}$, $q = 1 - \frac{1}{M}$ and $\binom{n}{m}$ is the Newton coefficient.
What is interesting in our case is the probability for a subband to be empty:

$$p(0) = \binom{n}{0} q^n = \left(1 - \frac{1}{M}\right)^n \tag{3.34}$$

The non-occupation mean is $\left(1 - \frac{1}{M}\right)^n$.
For $M$ subbands, the mean of empty subbands is:

$$\bar{M} = M\left(1 - \frac{1}{M}\right)^n = \frac{(M-1)^n}{M^{n-1}} \tag{3.35}$$

So, we observe the results for 2, 4 and 8 subbands and we consider up to 16 channels.

- M=2

Fig.3. 26 shows the mean of empty subbands for a total of 2 subbands. This case is not very interesting.

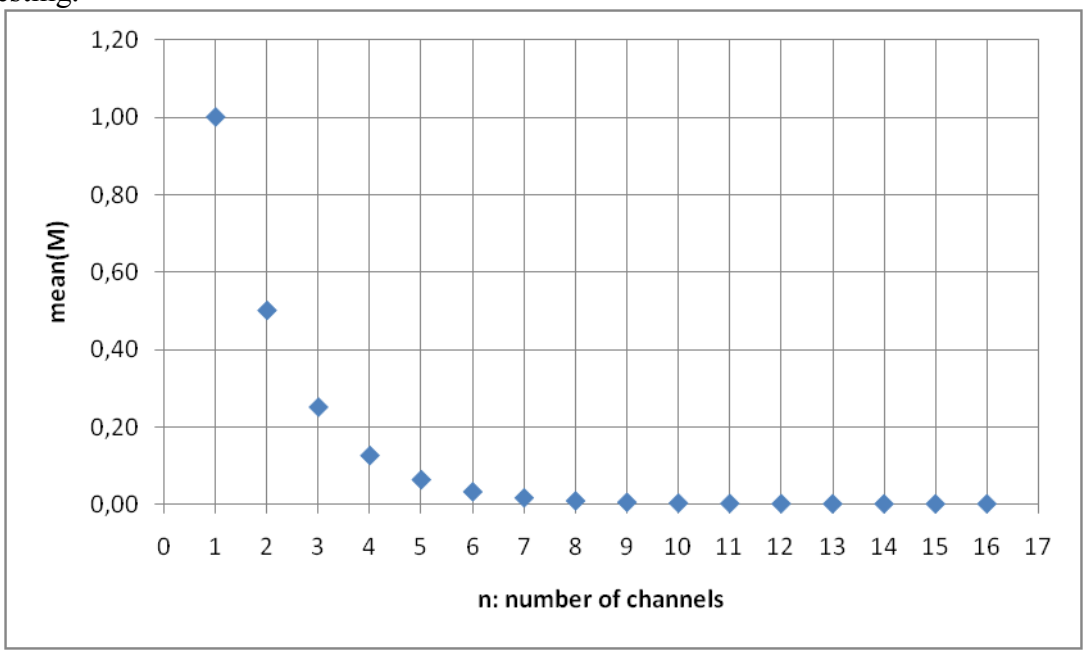


**Fig.3. 26 - Mean of empty subbands for M=2**

- M=4

Fig.3. 27 shows the mean of empty subbands for a total of 4 subbands.

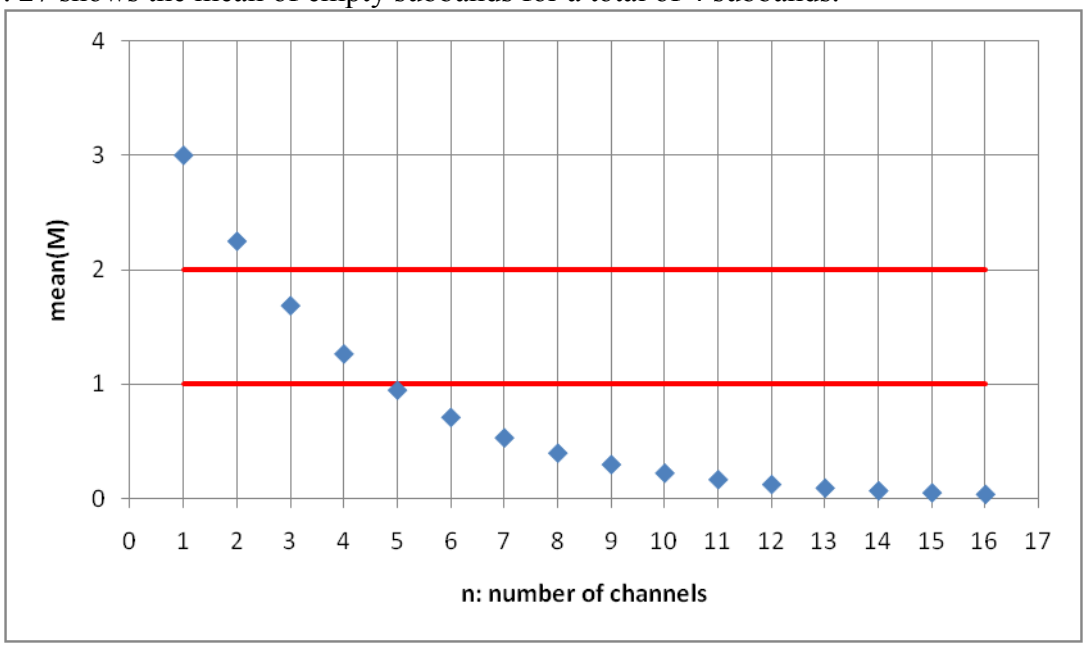


**Fig.3. 27 - Mean of empty subbands for M=4**

For example, if there are 5 channels to receive and 4 subbands, we could statistically switch-off one subband out of 4.
Indeed, if the number of channels is less than 5, we could switch-off one subband out of 4 and if the number of channels is less than 3, we could switch-off 2 subbands.

- M=8

Fig.3. 28 shows the mean of empty subbands for a total of 8 subbands.

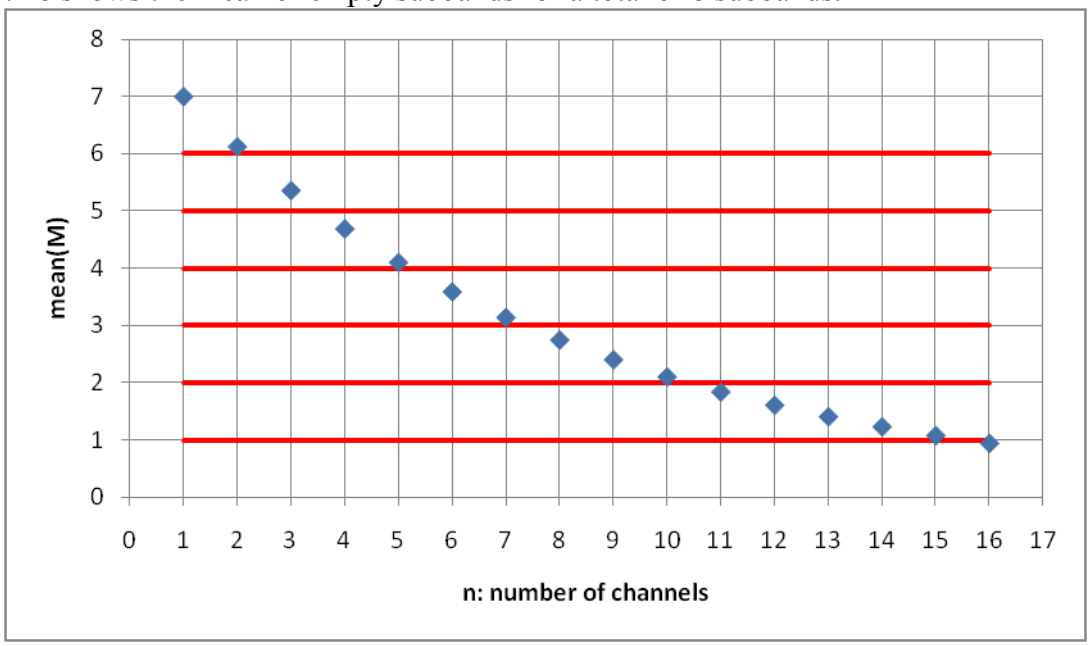


**Fig.3. 28 - Mean of empty subbands for M=8**

For example, if there are 5 channels to receive and 8 subbands, we could statistically switch-off 4 subbands out of 8.
In the case of 8 subbands, if we have less than 16 channels to receive, then we could statistically switch-off at least 1 subband out of 8.

Switching-off unused subbands could be a good solution for saving power. Yet, it is possible only for more than 2 subbands. And, as we saw before, we would have to implement bandpass filters instead of lowpass and highpass filters, which could be expensive in terms of surface, thus we should carefully study these cases.

### *3.2.4.2 Surface estimation*

To save surface and cost and because of know-how of NXP Semiconductors, the Front-End components would be in BiCMOS. The surface of the AGCs, mixers and PPFs are estimated from the state-of-the-art.
The filters split the input spectrum into two subbands. The first one is a lowpass and the second one a highpass. They are 3$^{rd}$-order Elliptic filters and passive. As we know their order and cutoff frequencies, we can find the components'values and estimate their surface (APPENDIX B).

**Table 3. 16 - Estimation of surface of the blocks**

| Filters | AGCs | PPF | QM | Filters | ADCs |
|---|---|---|---|---|---|
| 0.35mm² | 0.16mm² | 0.16mm² | 0.55mm² | 0.68mm² | 8.24mm² |

Thus, the global reception chain has a surface of 10.44mm²

### 3.2.5 Comparison

We compare the results of the architecture with the only high-performance ADC and the proposed architecture.

**Table 3. 17 - Comparison of the architectures**

| | Surface (mm²) | Power (mW) |
|---|---|---|
| [28] | 5.1 | 480 |
| our | 10.44 | 1189 |

Fig.3. 29 presents the comparison as a graph of power consumption versus the surface, for each architecture.

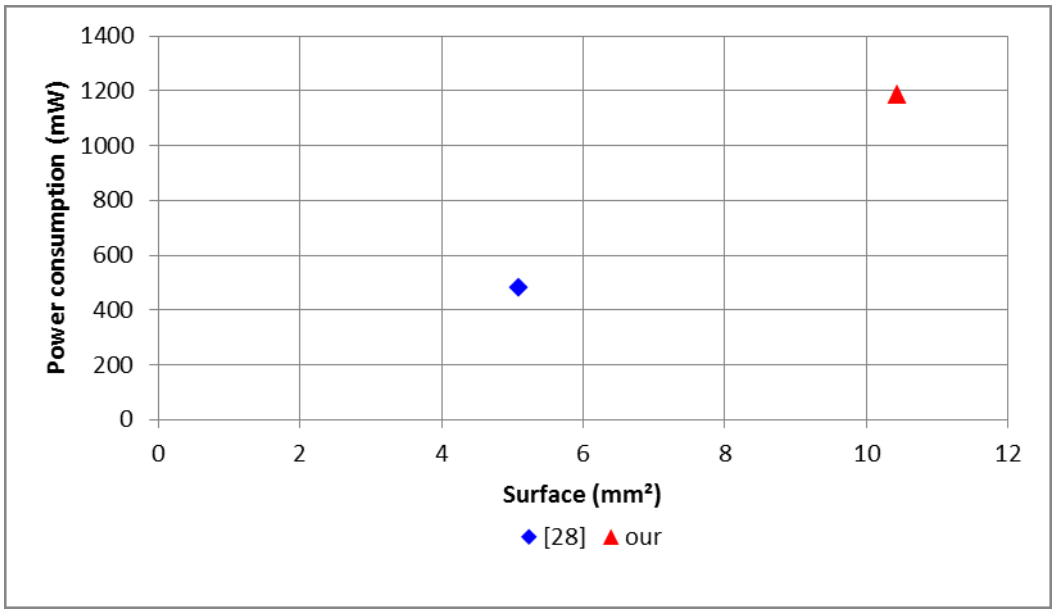


**Fig.3. 29 - Power consumption versus Surface**

The proposed architecture is not really competitive in terms of surface and power consumption because of the addition of several components and the multiplication of ADCs due to analytic signals. Nevertheless, this architecture has the major advantage that all the components are feasible, even the ADCs, and it is possible to switch-off subbands to save power.

So the proposed architecture could be good solution at the present time but it is not competitive in terms of power consumption and surface. Alternatives will be found in the following where we study Hybrid Filter Banks in Part 4.

# 4 HFB

As shown in Part 2, Hybrid Filter Banks is a parallel architecture with an analysis bank with analog filters, a bank of ADCs, upsamplers and a synthesis bank with digital filters. The outputs of each branch are summed together and we have the digital output of this HFB-based ADC that is equivalent to the analog input. The main advantage of this architecture is that aliasing is tolerated in each subband, because it is attenuated, ideally suppressed, by construction. Thus, the sampling rate of the subband ADCs can be the global sampling rate divided by the number of subbands. Theoretical studies on these filters have been made, e.g. in [56], for $M$ number of subbands.
Yet, we have selected a two-channel HFB architecture in order to minimize implementation cost of the analog filters. Indeed, bandpass filters are more expensive than lowpass and highpass filters in terms of surface because of the number of components they need. This architecture and the targets are presented in the following section. Then, we present our new optimization algorithm of the synthesis filters. We confirm next that this architecture is very sensitive to analog errors, so we propose a way to precisely identify the analog filters, but this method is also limited by measurement errors. Finally, we implement this architecture (to my knowledge) to prove the concept of aliasing attenuation and we check that the theoretical issues are valid.

## 4.1 2-channel HFB

Fig.4. 1 shows the architecture of a 2-channel HFB, where $H_0$ is a lowpass filter and $H_1$ a highpass filter.

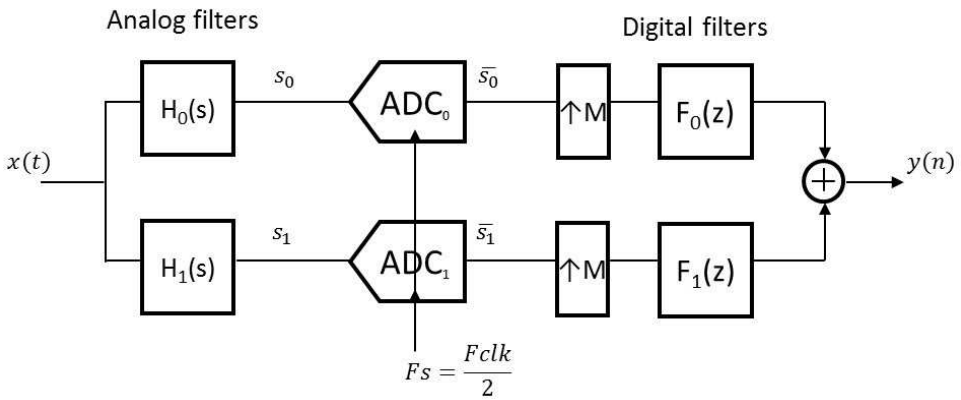


**Fig.4. 1- 2-channel HFB**

The following equations stand for this particular case, as studied in [38].
Let $X(j\omega)$ and $Y\left(e^{j\omega Tclk}\right)$ be the Fourier transforms of the input $x(t)$ and the output $y(n)$ of the system. Then, we have:

$$Y\left(e^{j\omega Tclk}\right) = G_{TF}(j\omega).X(j\omega) + G_{AF}(j\omega).X\left(j\omega - j\frac{\pi}{Tclk}\right) \quad (4.1)$$

with
$$G_{TF}(j\omega) = H_0(j\omega).F_0\left(e^{j\omega Tclk}\right) + H_1(j\omega).F_1\left(e^{j\omega Tclk}\right) \quad (4.2)$$

and
$$G_{AF}(j\omega) = H_0\left(j\omega - j\frac{\pi}{Tclk}\right).F_0(e^{j\omega Tclk}) + H_1\left(j\omega - j\frac{\pi}{Tclk}\right).F_1(e^{j\omega Tclk}) \quad (4.3)$$

In these relations, $G_{TF}$, as given by (4.2), is the distortion (or transfer) function while $G_{AL}$ in (4.3) is the aliasing function. The overall goal of the design of the HFB is to approach a perfect reconstruction, $PR$, i.e. $G_{TF}$ should be a pure delay and $G_{AF}$ should be null. These conditions can be satisfied with a digital filter bank but can only be approached with Hybrid Filter Banks. Thus, we have specified a maximum distortion of the transfer function (4.2) and a maximum aliasing rejection (4.3), so that the digitized output is considered sufficiently accurate for being further processed. In the present work the following targets have been set:

$$max(|G_{TF}|) < 0.5dB \quad (4.4)$$

$$max(|G_{AF}|) < -70dB \quad (4.5)$$

The target of the maximum of aliasing rejection is the aliasing rejection specified in Part 3 (-60dB) with an additional margin.

We propose the following representation of each block output from the input spectrum to the output to explain the principle of the whole architecture. For simplicity, the input spectrum is flat and located in the first Nyquist band, from DC to $\frac{Fclk}{2}$, where $Fclk$ is the global sampling rate, and the analog filters, $H_0$ and $H_1$, are represented as brick-wall filters on Fig.4. 2 and Fig.4. 3 respectively. Their cutoff frequencies are $\frac{Fclk}{4}$.

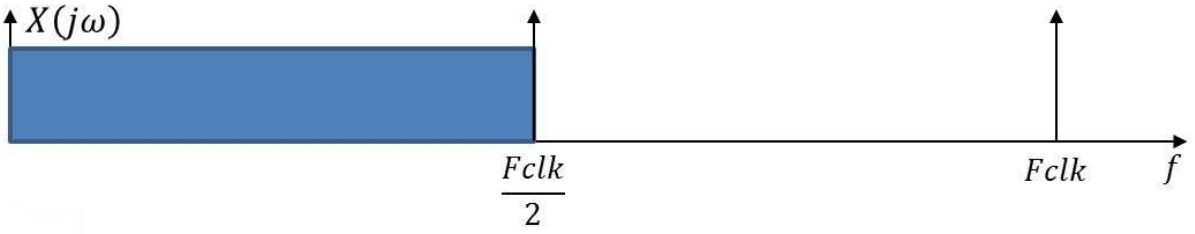


**Fig.4. 2- Input spectrum**

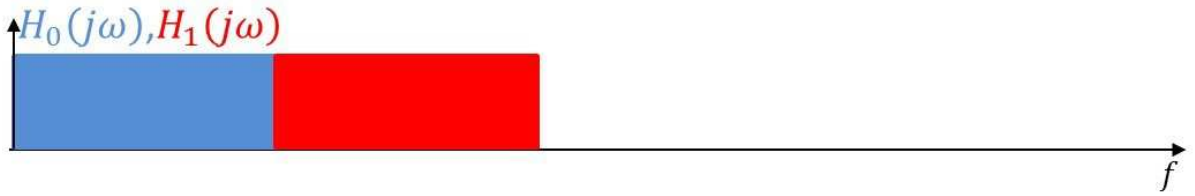


**Fig.4. 3- Analog filters**

The outputs of the analog filters can be represented by brick-wall filters as well, because the input spectrum is flat.

The ADCs sample the output signals of the analog filters at the frequency $Fs = \frac{Fclk}{2}$.

On Fig.4. 4, the replicas are stripped.

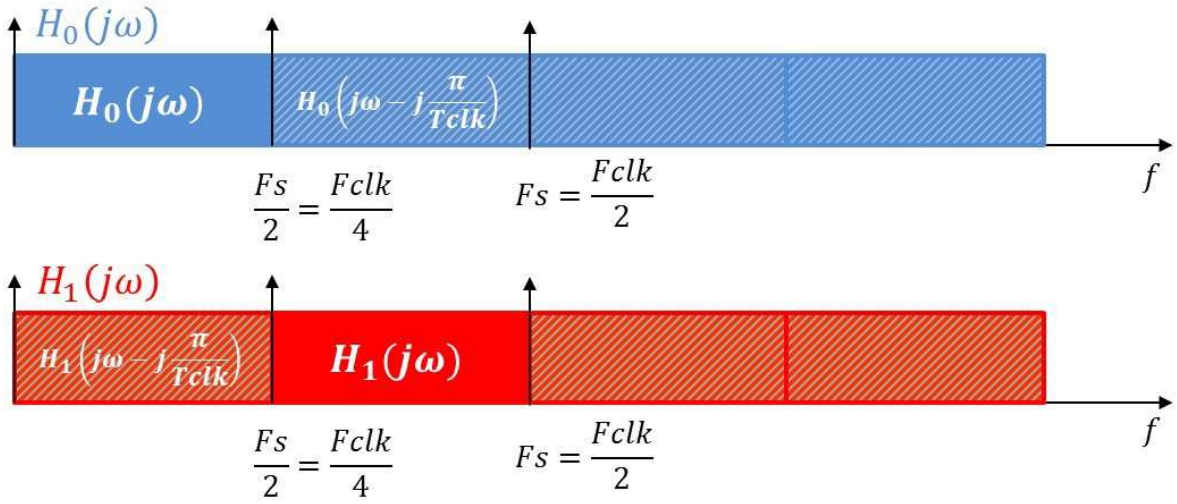


**Fig.4. 4- After sampling**

Then, upsampling is performed, as shown on Fig.4. 5.

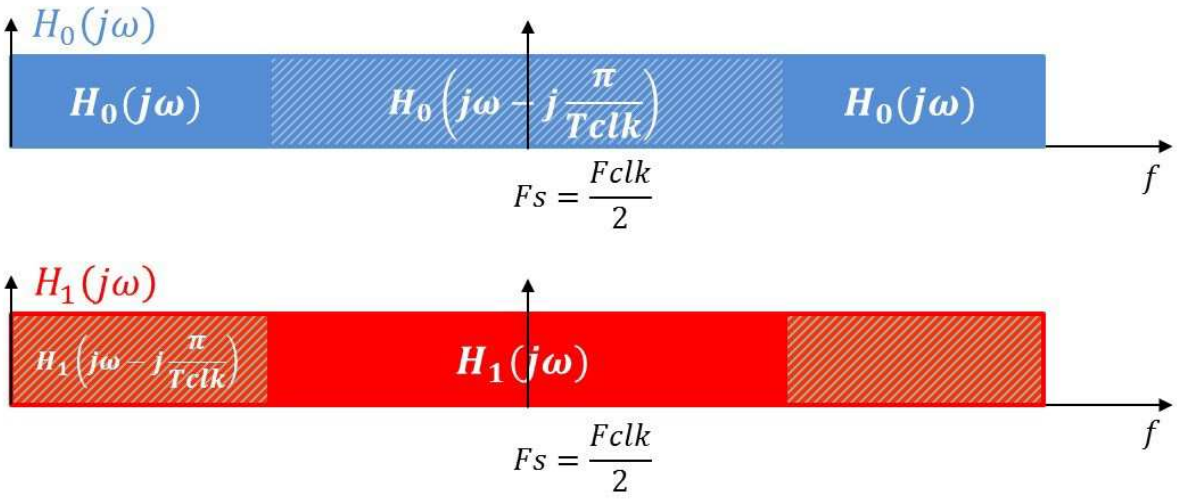


**Fig.4. 5- After upsampling**

To fulfill the QPR conditions, the digital filters, $F_0$ and $F_1$, should be a lowpass and a highpass filter respectively, as depicted on Fig.4. 6. We consider brick-wall filters in this case as well.

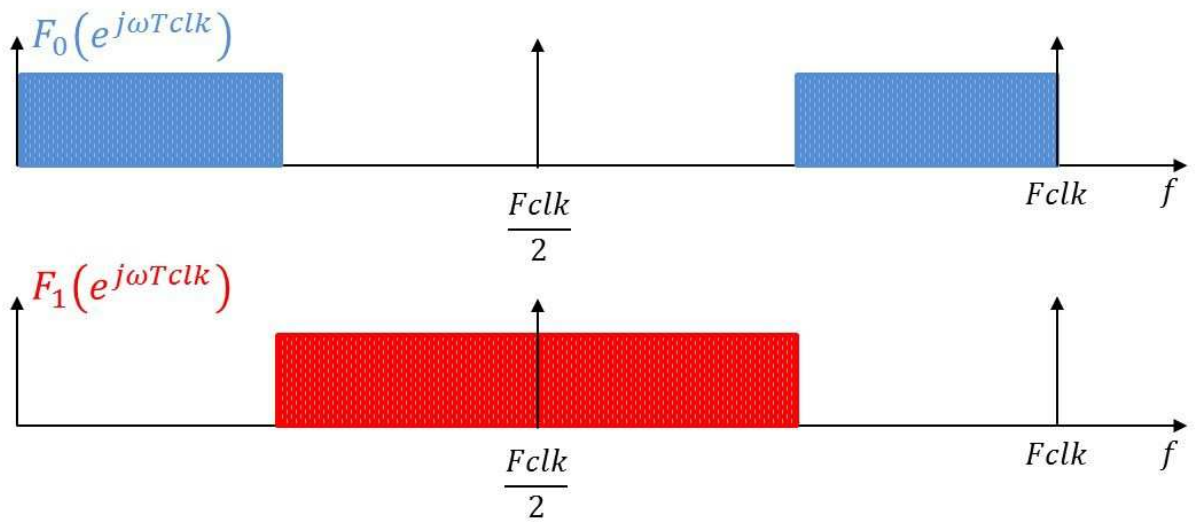


**Fig.4. 6 - Digital filters**

As shown on equation (4.2), the transfer function of the whole architecture, $G_{TF}$, is the sum of the transfer function of each channel, as depicted on Fig.4. 7. We expect $G_{TF}$ to be a constant and check this property on Fig.4. 8.

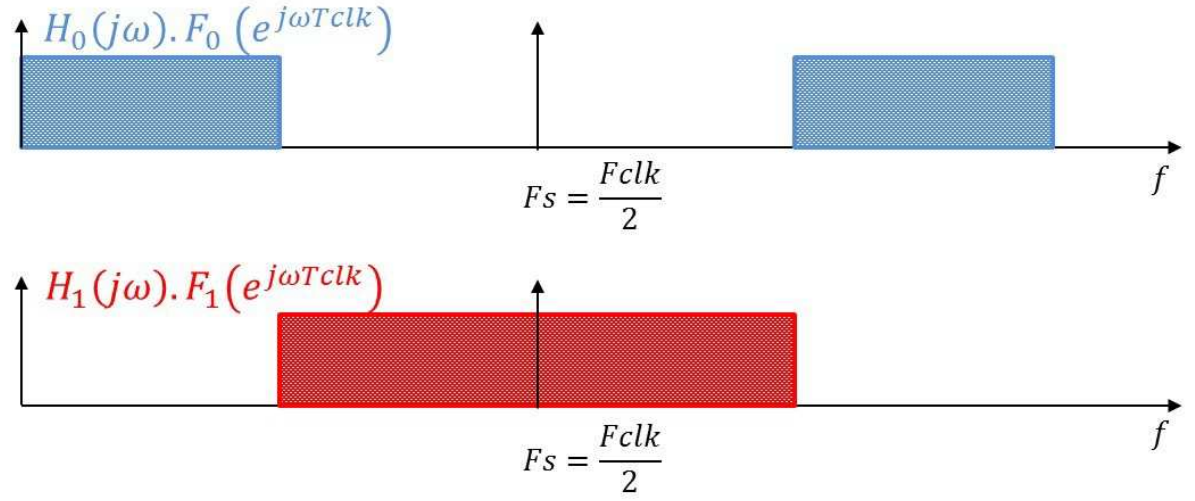


**Fig.4. 7 - Transfer function of each channel**

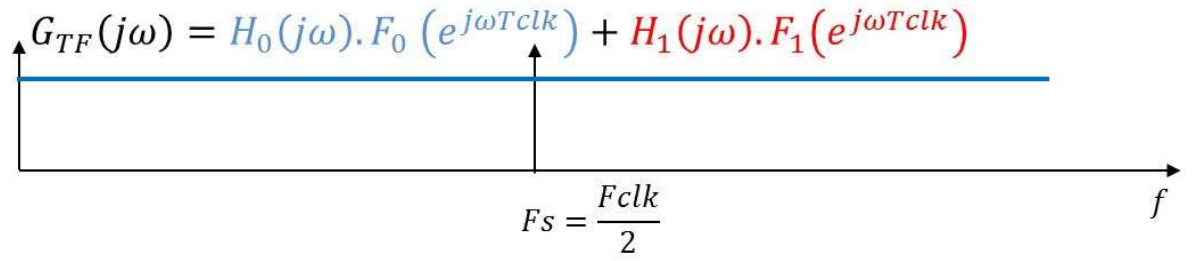


**Fig.4. 8 - Transfer function**

On the contrary, the tolerated local aliasing has to be ideally suppressed, at least much attenuated. Fig.4. 9 and Fig.4. 10 show that the global aliasing function, $G_{AF}$, is null, so are the aliasing functions for each channel.

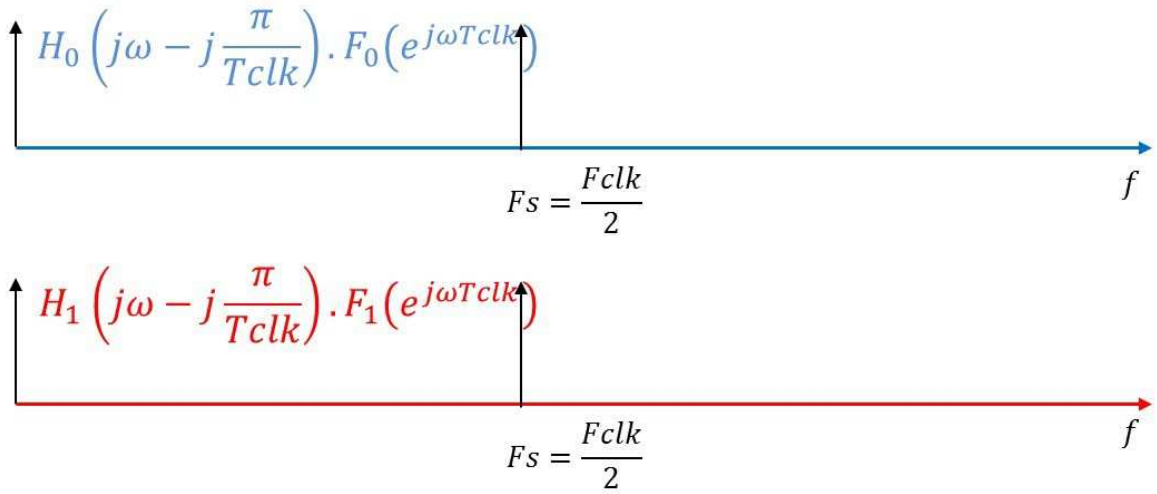


**Fig.4. 9 - Aliasing function for each channel**

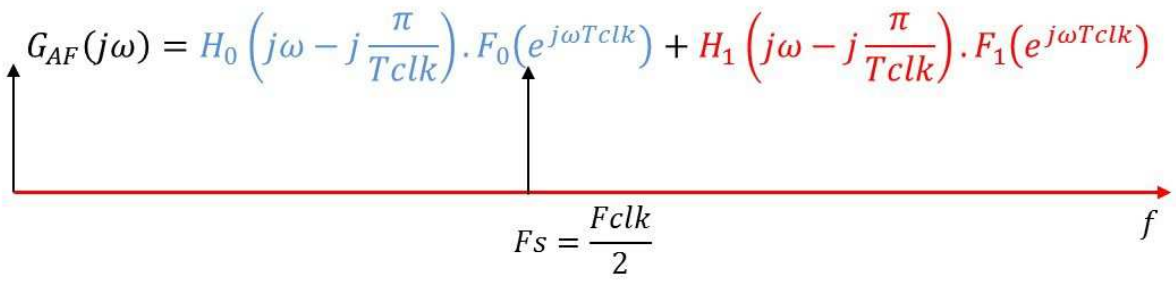


**Fig.4. 10 - Aliasing function**

Given that $G_{TF}$ is a constant and $G_{AF}$ is null, (4.1) becomes:

$$Y\left(e^{j\omega Tclk}\right) = constant \times X(j\omega) \qquad (4.6)$$

Thus, the digital output is the equivalent of the analog input and we have an HFB-based ADC.

So as to improve the performances, we introduce a guard band on each part of the band of interest, as shown in [68]. In this case, $G_{TF}$ and $G_{AF}$ are defined on the band of interest.
There are many ways to implement an HFB-based ADC. These are discussed below, with highlights on our particular choices.

The performance of HFB architecture relies on the design of the filter banks. Several solutions have been proposed to construct an HFB-based ADC. As PR is reachable with digital filter banks, a possible approach consists in using a Z-to-S transform to design the continuous-time analog filters [69]. However, this method results in high-order filter bank [70]. Specifically, the order of each analog filter equals the order of the prototype multiplied by the degree of the transform. A second approach consists in adjusting the poles and zeros of the analog filters so as to minimize the reconstruction errors. Another solution is to first optimize the analog filters and then, with the analog filters fixed, design the digital synthesis filters [71]. In [72], it is proposed to use power complementary filters for a two-channel HFB-based ADC, which are characterized by special relations between the numerators and denominators of the transfer functions of the analog filters. The previous approaches suffer either from the difficulty to design the required analog filters at 1GHz, or from the too high FIR number of taps.

With implementation cost in mind, we have decided to use standard and fixed analog filters with low-complexity. The complexity associated to the research of the QPR is thus reported on the optimization of the digital synthesis filters. In this part, we can better afford high-order synthesis filters to ensure QPR. However, we still use IIR structures for the synthesis filters so as to lower the filter order, compared to FIR filters. Stability issues of IIR filters have been taken into account in the optimization described in the following part.

## 4.2 Optimization algorithm

The aim of the optimization is to adjust the synthesis filters, $F_0$ and $F_1$, so as to approach QPR, as specified by a maximum distortion, and a maximum of aliasing rejection. Thus we are looking for a way to obtain a transfer function $G_{TF}$ close to 1 and to minimize the aliasing function $G_{AF}$. These two objectives are integrated into the single criterion:

$$J(F_0, F_1) = (|G_{TF}(j\omega)| - 1)^2 + \beta |G_{AF}(j\omega)|^2 \quad (4.7)$$

where $\beta$ is a parameter that tunes the relative weight of the two terms. The most stringent requirement being aliasing rejection as illustrated in Table.4. 2, the largest weight is given to this term. In the case of guard band, the criterion is only applied on the band of interest.
It has yet been reported [73] that the mixed criterion above suffers of local minima, which turns the filter synthesis into a difficult, but key, task.
In order to find possible (optimum) synthesis, we have developed a heuristic approach that rests on the application of two minimizations strategies: a direct simplex search method that minimizes the average energy of the criterion with fast convergence, complemented by a minimax procedure whose particular goal is to lower the local maxima of the criterion especially on the edges of the band [73]. The algorithm also includes a perturbation strategy to avoid local minima. The overall algorithm is depicted in Fig.4. 11 and described below.
The algorithm focuses on the specification of maximum of aliasing rejection. It ends when the target is reached. It optimizes the coefficients of the numerators and denominators of the IIR digital filters.

*Optimization functions* — Specifically, the algorithm is implemented under Matlab, and uses the functions *fminsearch* and *fminimax*. *fminsearch* is a direct search method which is based on the Nelder-Mead method. The corresponding algorithm will find the minimum of a function of $N$ variables. The function *fminimax* minimizes the worst-case (largest) value of a set of multivariable functions. This is generally referred to as the minimax problem. Both functions start at an initial estimate and may only give local solutions.

*Initialization* — Initial conditions for the synthesis filters are selected as follows. To fasten the process of optimization, we choose the synthesis filters optimized for a particular case of digital filter bank. Actually, we identify and use the discrete-time analog filters that correspond to the actual analog $H_0$ and $H_1$, the continuous-time filters. As we consider IIR filters, we have to stabilize the solutions given by the functions.

*Perturbation strategy* — As the functions may only give local solutions, a potential issue is to stall in a local minimum, before having reached the target. We first have to detect a possible local minimum. If two successive results of aliasing rejections have approximately the same value, we propose two ways to resolve it. On the one hand, we add a small deviation that

should be carefully chosen, to get out of the local minimum. On the other hand, we increase the order of the IIR filters, and we compare the two solutions.
The algorithm is stopped when the targeted performance is reached. We could go further but prefer keeping the solution which provides an IIR with the smallest order.

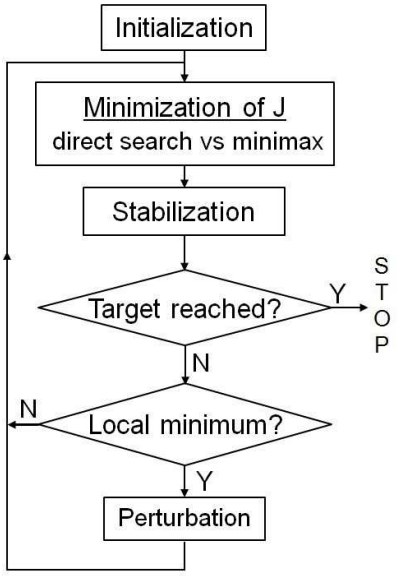


**Fig.4. 11 - Optimization algorithm**

All our tests show that the procedure reaches the targeted performances and gives very interesting results in the case of perfectly known analog filters.
The following table gives an example of performances predicted by simulation in the case of two analysis filters chosen as analog 3rd-order Butterworth filters. As shown in Table.4. 1, the IIR filters created are only 4th-order filters.

**Table.4. 1 - Performances with theoretical analog filters**

| $Max(G_{TF})[dB]$ | $Max(G_{AF})[dB]$ | Filter order |
|---|---|---|
| 0.03 | -72.22 | 4th |

However, as we know, these analysis filters are subject to realization and analog errors and thus deviate from the theoretical filters. It is thus important to examine the influences of such mismatches on the performances.

## 4.3 Sensitivity

Once the synthesis filters have been optimized for ideal analog filters, we introduce errors on the analog filters and examine the performances. We recall here the ideal transfer functions of a Butterworth 3rd-order LPF (4.8) and HPF (4.9):

$$H_{LPF}(s) = \frac{\gamma}{s^3 + \alpha s^2 + \beta s + \gamma} \tag{4.8}$$

$$H_{HPF}(s) = \frac{s^3}{s^3 + \alpha s^2 + \beta s + \gamma} \tag{4.9}$$

Then, we change the coefficients of the ideal transfer functions, such that we get:

$$H_{LPF\_modif}(s) = \frac{\gamma}{\delta' s^3 + \alpha' s^2 + \beta' s + \gamma} \quad (4.10)$$

$$H_{HPF\_modif}(s) = \frac{s^3}{s^3 + \alpha'' s^2 + \beta'' s + \gamma''} \quad (4.11)$$

where $\delta' = 1 + \varepsilon_{\delta'}$, $\alpha' = \alpha(1 + \varepsilon_{\alpha'})$, $\beta' = \beta(1 + \varepsilon_{\beta'})$, $\alpha'' = \alpha(1 + \varepsilon_{\alpha''})$, $\beta'' = \beta(1 + \varepsilon_{\beta''})$ and $\gamma'' = \gamma(1 + \varepsilon_{\gamma''})$. We define the error that we want to apply to these coefficients, $coeff\_error$, and we calculate the random error with the $rand$ function in Matlab, such that $\varepsilon_i = coeff\_error * rand(1)$. These random errors are added to the ideal coefficients of the transfer functions, except for $\gamma$ in $H_{LPF}(s)$ and for the coefficient of $s^3$ in $H_{HPF}(s)$ in order to keep the correct behavior at low and high frequencies respectively.

Table.4. 2 shows the impact of these errors on the performances, without changing the synthesis filters. We choose the example from Table.4. 1 as reference.

**Table.4. 2 - Performances with actual analog filters**

| Analog errors (%) | Performances | |
|---|---|---|
| | $Max(G_{TF})[dB]$ | $Max(G_{AF})[dB]$ |
| 10 | 0.99 | -15.86 |
| 1 | 0.09 | -40.39 |
| 0.1 | 0.03 | -56.79 |
| 0.01 | 0.03 | -71.63 |

We conclude from this table that this architecture is very sensitive to realization and analog errors. This problem has already been reported in [74].
As the actual analog filters could be different from the theoretical filters and since we do not know exactly their transfer functions, the synthesis filters that correspond to the theoretical case are not adapted and the performances are degraded. If we could precisely measure or calibrate the analog filters, it would be easy to optimize the synthesis filters.

## 4.4 Identification

### 4.4.1 Method

The ideal solution would be to be able to measure the actual analog filters with infinite precision and then to calculate the synthesis filters. However this is not practical because it is difficult to have good precision at high frequencies.
No measure could be done in the analog domain but it is still possible in the digital domain. If we dispose of a known test input signal *x(t)* with Fourier transform *X(f)*, then we can have access to the outputs of the ADCs, noted $\bar{s}_0$ and $\bar{s}_1$, given that we bypass the digital filters, cf. Fig.4. 1. These measures correspond to the outputs of the analog filters, $s_0$ and $s_1$, with local aliasing, because of undersampling. We thus have the following relationship:

$$\bar{S}_k(f) = S_k(f) + S_k^*(Fs - f) \quad (4.12)$$

where *Fs* is the sampling rate of each ADC, and

$$S_k(f) = X(f) \times H_k(f) \quad (4.13)$$

for k=0 or 1.
Assuming that we know the input signal and that the measurements have infinite precision, we could then identify the analog filters very well. For this, we use an optimization that

operates on the coefficients $a_k$ and $b_k$ the numerator and denominator of both identified analog filters. We start from the theoretical filters and the aim of the optimization is that the aliased outputs of the identified analog filters match the measured ones:

$$\inf_{a_k, b_k} \left| \bar{S}_k(f) - \left( X(f) \times H_k(f) + X^*(Fs - f) \times H_k^*(Fs - f) \right) \right|^2 \qquad (4.14)$$

This is implemented, again, using the *fminsearch* function.
In practice, we may not dispose of a pilot signal, but rather we might know that the input signal has the characteristics of a white noise (i.e. decorrelation and flat spectrum). In such a case, the identification criterion can be written with respect to the power spectrum and becomes

$$\inf_{a_k, b_k} \left| |\bar{S}_k(f)|^2 - (|H_k(f)|^2 + |H_k(Fs - f)|^2) \right|^2 \qquad (4.15)$$

Using this approach and 128 frequency measurements, the criterion is as low as $10^{-29}$, which indicates that we obtain a perfect identification. Then, from these identified filters, we optimize the synthesis filters and obtain excellent performances, since the estimated filters are close enough to the real analog filters, even if there are analog errors.
Unfortunately, the measurements are not perfect but corrupted by some measurement errors. Indeed, these errors include both modeling errors (e.g. the assumption of a flat spectrum) and errors related to the limited integration time. Therefore, the identification is operated from imperfect measurements. Since the synthesis filters are optimized from these identified analog filters, they will not be well-adapted to the actual analog filters. Simulations results show that the performances are affected and very dependent on the precision.

### 4.4.2 Results

Table.4. 3 gives the performances of the architecture when the analog filters are imperfectly known: errors are introduced on the values of the filters coefficients, and the identification procedure is used so as to estimate the actual filters. In this first case, the measurements of the spectrum are supposed free of errors. For different levels of errors, the identification procedure yields excellent results and performances follow.

**Table.4. 3 - Performances with actual analog filters**

| Analog errors (%) | Performances | | |
|---|---|---|---|
| | Identification precision | $Max(G_{TF})[dB]$ | $Max(G_{AF})[dB]$ |
| 0 | 2.65E-29 | 0.03 | -72.22 |
| 0.01 | 2.64E-29 | 0.03 | -72.07 |
| 0.1 | 2.61E-29 | 0.04 | -70.29 |
| 1 | 2.90E-29 | 0.04 | -71.45 |
| 10 | 3.27E-29 | 0.04 | -70.70 |

Next we examine the impact of measurement errors on the spectra computed at the output of ADCs and the performances that follow. We see that the performances are severely degraded, due to the imperfect identification. Acceptable performances of the whole design require measurements with more than 60dB of SNR.

**Table.4. 4 - Performances with measurement errors**

| SNR (dB) | Performances | | |
|---|---|---|---|
| | Identification precision | $Max(G_{TF})[dB]$ | $Max(G_{AF})[dB]$ |
| ∞ | 2.65E-29 | 0.03 | -72.22 |
| 80 | 5.32E-06 | 0.04 | -69.10 |
| 60 | 6.45E-04 | 0.04 | -54.70 |
| 40 | 0.05 | 0.06 | -39.93 |
| 20 | 5.64 | 0.46 | -17.43 |

## 4.5 Realization

These results clearly highlight that this architecture is very sensitive to realization and analog errors. This is a known limitation which has already been reported in [74].
However, few practical HFB realizations have been reported in the literature. The next section details the measurements operated on a 2-channel HFB.
The goal is to design a device with prescribed performances and then measure the actual performances of the realization.

**Fig.4. 12 - Overview of the testbench**

### 4.5.1 Description of the boards

To prove the concept of HFB-based ADC, we need two ADCs working at the same sampling rate with similar resolution. We have a Board HSMC from Altera, with two 150Msps 14-bit ADCs (AD9254), as depicted on Fig.4. 13.

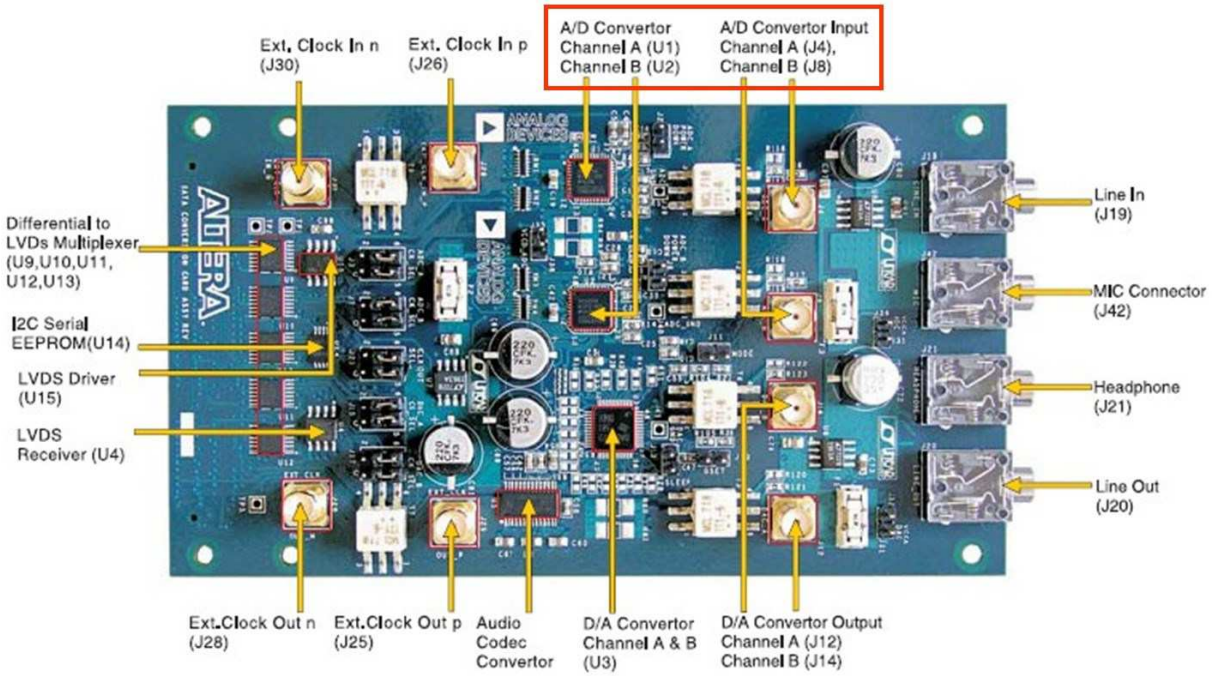


**Fig.4. 13 - Board HSMC**

For the digital part, a stratix III from Altera with an FPGA is connected to the board HSMC as follows:


**Fig.4. 14 - Board HMSC with stratix III**

Then, the two passive analog filters (3$^{rd}$-order Butterworth) are hand-made:

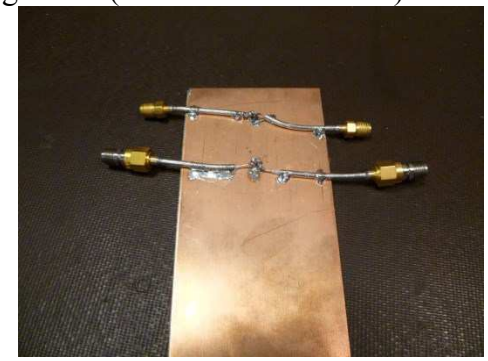

**Fig.4. 15 - LPF and HPF analog filters**

Using these boards, we should be able to design an HFB-based ADC working at 300Msps with 14 bits of resolution. Yet, in order to obtain a good reconstruction, we need to determine as accurately as possible the transfer functions of the analog filters. They were measured through the ADCs in order to take into account every possible parasitics due to the acquisition card. This has an impact on the design of the analog filters and on the input spectrum. This is explained in the following section, which focuses on the design of analog filters.

### 4.5.2 Analog filters

Measurements of analog filters use both ADCs: on one path, the input signal is digitized, while on the 2nd path the output of one filter is digitized. This operation is repeated with the opposite configuration. In order to avoid aliasing, analog filters outputs are digitized at the maximum sampling rate of 150Msps and the input spectrum spreads up to 75MHz at most.
Thus, the filters are designed such that their cutoff frequencies are around 37.5MHz.

The circuits on Fig.4. 16 and Fig.4. 17 are implemented, which lead to a cutoff frequency of around 37MHz for the lowpass filter and around 33MHz for the highpass filter (see APPENDIX F).

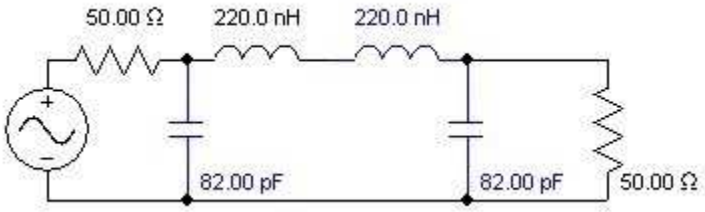


**Fig.4. 16 - LPF circuit**

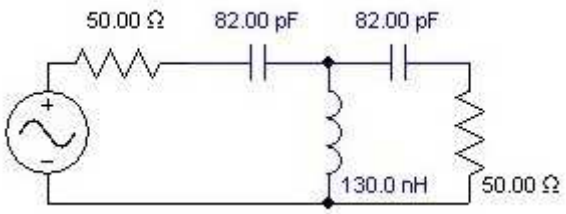


**Fig.4. 17 - HPF circuit**

Transfer functions of the filters have been measured from 5MHz to 75MHz. The results are reported on Fig.4. 18.

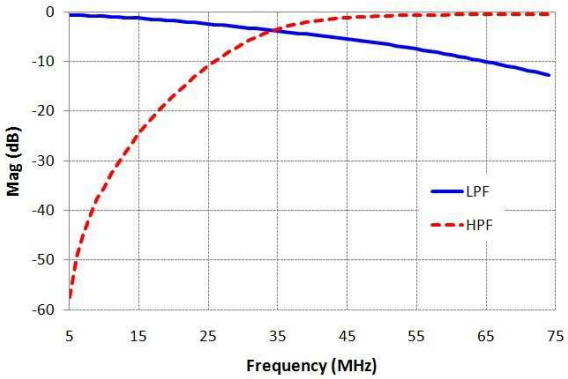


**Fig.4. 18 - Measurements of analog filters**

### 4.5.3 Reconstruction

The input spectrum ranges from 30MHz to 40MHz. Thus, to get a satisfactory reconstruction on this bandwidth, we need the aliasing which falls in it to be attenuated by more than 70dB and the distortion between the digitized and analog input to be less than 0.5dB. The algorithm described in section III.B is applied. It performs an optimization of the coefficients of the digital synthesis filters associated to the measured transfer functions of the analog filters. After optimization, we get two stable $4^{th}$-order IIR filters, which is a moderate order, and whose transfer functions are shown Fig.4. 19.

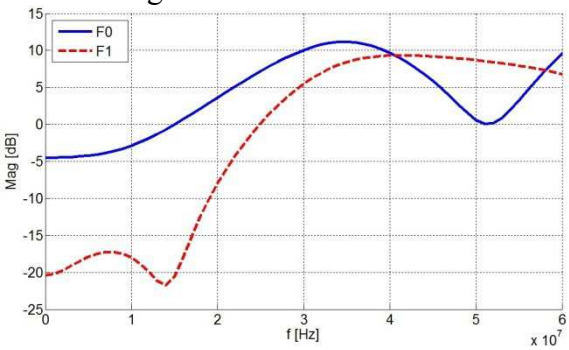


**Fig.4. 19 - $4^{th}$-order IIR filters obtained after optimization**

The following table gives the performances predicted after the optimization step, over the whole bandwidth:

**Table.4. 5 - Performances with measured analog filters**

| $Max(G_{TF})[dB]$ | $Max(G_{AF})[dB]$ | IIR order |
|---|---|---|
| 0.06 | -72.83 | 4 |

### 4.5.4 Results

To illustrate with concrete figures the previous description of the measurements, we fed the analog filters with a sinus at 36MHz. Sampling at 75MHz, the aliasing occurs at 39MHz. As shown in Fig.4. 20, this aliasing is attenuated by 75.2dB.

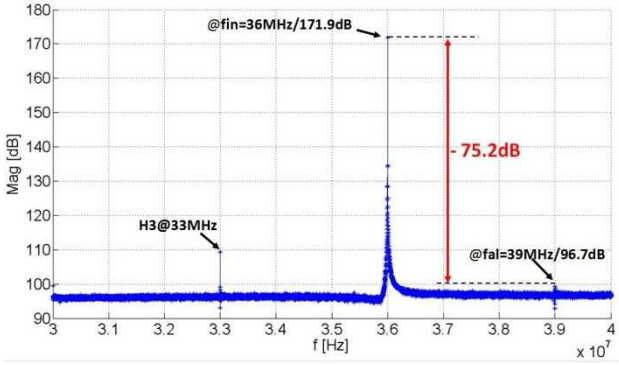


**Fig.4. 20 - Module of FFT (dB) after reconstruction**

The measurements have been done for several frequencies and the results are synthesized on Fig.4. 21, which compares the values predicted by simulation to the actual results on the device.

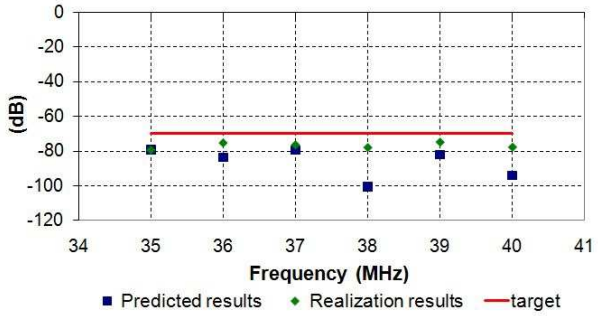


**Fig.4. 21 - Synthesis of aliasing rejection results**

The results are very interesting. However, if we repeat the measurements with the same configuration, we notice that the performances are degraded to values between -45dB and -60dB. Hence, we observe that the target of -70dB is not fully reached; but still approached. The differences between the measured and predicted performances are due to measurements imprecision of the analog filters, their drift in temperature and the high sensitivity of the architecture to mismatches.

We shall also mention that the level of performances is also dependent on the order of the analog analysis filters: the higher their order, the more aliasing rejection is obtained. There is also a trade-off between performances and complexity to tune at this point.

# 5 Conclusion

This PHD work thesis was a partnership between the BL TVFE of NXP Semiconductors in Caen and ESIEE Paris. Its goal was to provide a solution to multi-channel reception for cable network.
Indeed, multi-stream reception is a key point for future products in cable modem, terrestrial and satellite TV. NXP is already a leader in the domain of Silicon Tuners that are a tuner function implemented directly on the main board, thanks to fully integrated solutions. A tuner function is needed to select the desired channel among a large range of frequency for the demodulation. Multi-channel reception implies simultaneous reception of several channels located anywhere on the whole band or partial RF band. The simultaneous reception supposes either the use of as many tuners as wanted channels or the digitization of the whole band. The spectrum of interest spreads from 50MHz to 1GHz, and one might want to simultaneously receive up to 16 channels of 6MHz. Of course, using for instance 16 tuners Integrated Circuits for receiving 16 channels would be severely over-killing in terms of cost and power. Therefore it was of particular importance to investigate solutions for the complete digitization of the 1GHz input spectrum. Broadband digitization is a foreseen direction in RF sampling architecture: the whole RF band is sampled very early in the signal path. This reduces RF hardware, allows most of the processing to be done in digital domain, and thus facilitates reconfigurability by software (Software Radio). However, this puts tough requirements on the Analog-to-Digital Converter (ADC): the wide signal bandwidth requires a high sampling rate (>2Gsps) according to Shannon's theorem, while the lack of RF selectivity and the non-uniform input power spectral density (PSD) leads to high dynamic range requirement (>10bits). To evaluate the required performances of the ADC, we defined a test case where the input spectrum was considered flat over the whole bandwidth, and the wanted channel was 256QAM. From these assumptions and according to the standards, we concluded that a minimum SNR of 55dB was necessary to be able to demodulate the wanted channels.
Once these specifications determined, the literature has been assessed to find one ADC that reaches the target. Yet, the current Analog-to-Digital Converters architectures are not adapted to such an application. Flash ADCs, pipeline ADCs, Successive Approximation Register (SAR) ADCs and ΣΔ ADCs are either high speed or high resolution.
According to the literature, parallel structures for ADCs are a key for the design of high-speed, high-resolution data converters. Time-interleaving (TI), Hybrid Filter Banks (HFB) are potential architectures [1]. Another possible way to cope with this problem is to divide the issues by splitting the spectrum into subbands. This architecture is called RFFB and consists of a bank of analog filters and a bank of ADCs. We then defined power rejection that depends on the number of subbands and on the filters and aliasing rejection that is linked to the sampling rate and the filters. The relations between these rejections and the SNR have been demonstrated and a target has been set on aliasing rejection, for the information to be correctly demodulated. We have selected the Elliptic filters as the best analog filters in this case. Then, we noticed that there is a trade-off between the complexity of the filters and the reduction of the sampling rate. Moreover, when searching for a sampling rate lower than the Nyquist frequency, we found that at least two different sampling frequencies were necessary for this architecture, whatever the number of subbands. As having a unique sampling rate is a major advantage for clock generation, we used complex sampling, i.e. that we had a unique sampling frequency with less constraints, at the cost of a Passive Polyphase Filter per channel and the number of ADC had to be doubled. To decrease the maximum input frequency, a downconversion is performed with a mixer and a unique LO frequency. In the proposed

architecture, the LO frequency is half the unique sampling rate of the ADCs. This latter is chosen such that aliasing falls out of the interesting bandwidth and thus 3rd-order analog filters are complex enough.
Furthermore, as the wanted channels can be anywhere in the whole band, it is statistically possible that a subband be empty and as the subbands are independent, we can switch it off to save power.
So we finally proposed a promising architecture with the major advantage that all the components were feasible, even the ADCs, and it is possible to switch-off subbands to save power.
A general cost function was introduced to compare this solution to a wideband ADC close to our targets.
This cost function links surface and power consumption. To evaluate the surface and power consumption of our ADCs, we assumed that they were identical with the same FoM to calculate their power consumption and that they were time-interleaved to estimate their surface. For the other components of our solution, we took values from the state-of-the-art. Then the comparison showed that it could be a good solution at the present time but it is not competitive in terms of power consumption and surface. This work has been presented at EuMW [2].
An alternative was proposed in Part 4, where we study Hybrid Filter Banks. It was interesting to study this architecture with realization feasibility in mind. This is why we selected a 2-channel HFB with a 3rd-order Butterworth lowpass filter and a 3rd-order Butterworth highpass filter as low-cost analog filters, and thus we avoid implementing bandpass filters. Once the analysis bank was chosen, the digital filters had to be designed such that we reach our targets of distortion and aliasing rejection. We present an original procedure for the optimization of the synthesis filters, which combines direct simplex search, minimax methods and a perturbation strategy to avoid local minima. This method is efficient and gave good results as we found low-order IIR filters. We checked that this architecture is sensitive to analog mismatches by adding errors on the analog filters with fixed digital filters. We also addressed the calibration of the device, namely the identification of the actual analog filters, and highlighted the impact of the identification and of measurement errors on the overall performances. This work was presented at Newcas [3]. Finally, a physical realization proves the concept of aliasing rejection and confirms the parallel architecture sensitivity to analog mismatches (ECCTD [4]).

This realization is composed of three boards: one with the two 150Mbps ADCs, one with the FPGA and one with the two 3rd-order Butterworth analog filters. Many improvements could be done on this realization.
First, the upsamplers, the digital filters and the adder could be implemented on FPGA. This should not present any difficulties, except that we should be aware that the quantization of the coefficients of the digital filters could degrade the performances, unless the quantization is at least 28 bits.
FIR filters could be designed instead of IIR filters for a comparison of performances, sensitivity and complexity.
Another challenge would be to implement the optimization algorithm on FPGA, especially the Nelder-Mead method.
Then, for practical reasons, we have demonstrated the concept on a narrower band than the real bandwidth of the cable input spectrum and it would be interesting to check that this is easily adaptable to higher frequencies. As ADC, we could use [28] that has good performances and a sampling frequency of 1.35Gsps.

The analog filters could also be improved. They were good enough to prove the concept. We could also implement analog filters with higher complexity and see the impact on the performances.

It is worth mentioning that other studies are still on-going on HFBs, such as [78], [79] and [80], for example. [80] in particular proposes an analytical approach for determining the optimum synthesis filters. This solution seems very interesting, though the computational load seems very important and the practical results similar to ours. Since this communication is issued in 2013, well after the completion of the present work, we did not investigate this method.

To conclude, this subject of broadband digitization is really accurate and many solutions worth being investigated.

# APPENDIX A
# Margin vs IL

The standard SCTE40 gives the SNR per channel needed for the signal to be properly processed. It is Es/N0. Yet, we want to specify the SNR of the ADC. A margin has to be added to take into account the imperfections. We often define an Implementation Loss, $IL$. Let us see the relation between $IL$ and margin.
Let us consider a black box with a Signal-to-Noise Ratio $SNR_x$, that we have to calculate.

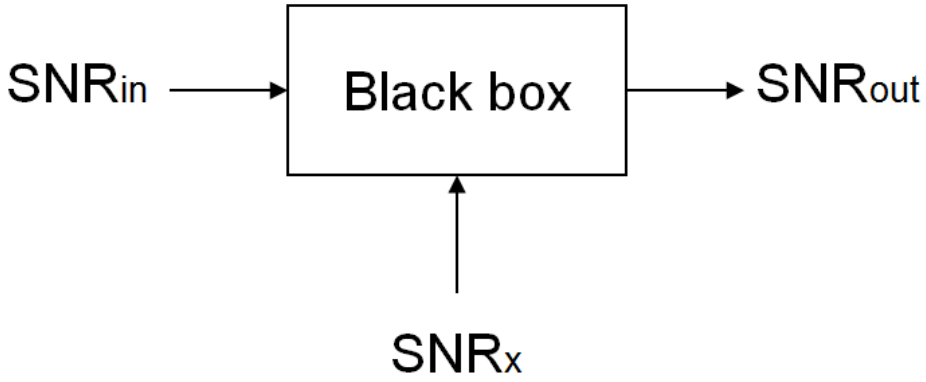


**Fig.A. 1 - Black box SNR**

Implementation Loss $IL$ links $SNR_{in}$ and $SNR_{out}$, as follows:

$$SNR_{in} = SNR_{out} + IL \quad \text{(A.1)}$$

Margin is defined as:

$$SNR_x = SNR_{out} + Margin \quad \text{(A.2)}$$

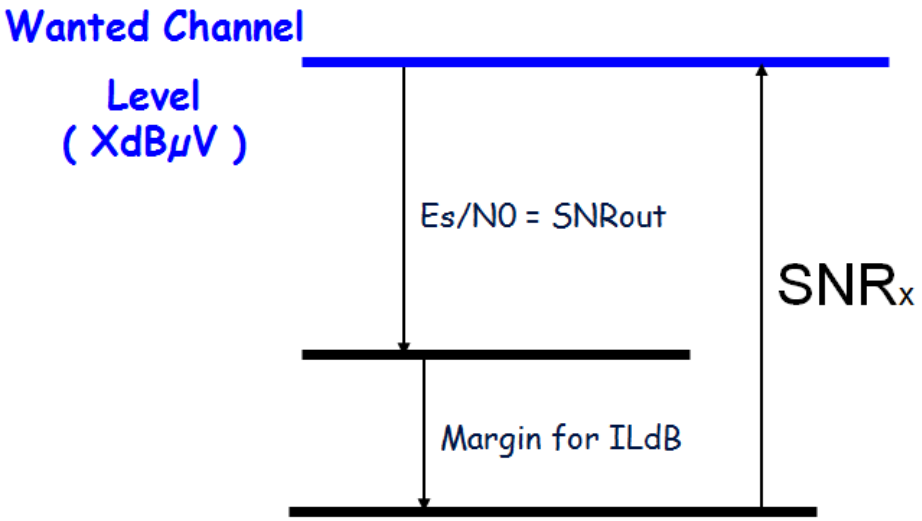


**Fig.A. 2 - Level diagram of $SNR_x$**

Relation between $SNR_{in}$, $SNR_x$ and $SNR_{out}$
By definition of Signal-to-Noise Ratio, we have, in linear:

$$snr_{in} = \frac{C_{in}}{N_{in}} \quad \text{(A.3)}$$

$$snr_{x} = \frac{C_{x}}{N_{x}} \quad \text{(A.4)}$$

$$snr_{out} = \frac{C_{out}}{N_{out}} \quad \text{(A.5)}$$

We assume that the signal is not degraded because the imperfections added are considered as uncorrelated noise and we assume that there is no gain nor attenuation. So, we have:

$$C_{in} = C_{x} = C_{out} = C \quad \text{(A.6)}$$

and

$$N_{out}{}^{2} = N_{in}{}^{2} + N_{x}{}^{2} \quad \text{(A.7)}$$

Dividing (A.7) by $C^2$, we get:

$$\frac{N_{out}{}^{2}}{C^2} = \frac{N_{in}{}^{2}}{C^2} + \frac{N_{x}{}^{2}}{C^2} \quad \text{(A.8)}$$

i.e.

$$\frac{1}{snr_{out}{}^{2}} = \frac{1}{snr_{in}{}^{2}} + \frac{1}{snr_{x}{}^{2}} \quad \text{(A.9)}$$

After a transformation from linear to dB scale and some calculations, we have:

$$SNR_{x} = SNR_{out} + IL - 10\log\left(10^{\frac{IL}{10}} - 1\right) \quad \text{(A.10)}$$

By comparison with (A.2), we conclude that:

$$Margin = IL - 10\log\left(10^{\frac{IL}{10}} - 1\right) \quad \text{(A.11)}$$

# APPENDIX B
# Computations of the components of an elliptic filter

As shown in the previous part, elliptic filters seem to be the better type of filter for our application.
The calculation of the components of an elliptic filter is important to do a cost function and to have an idea of the feasibility of the filter, and thus, the filter bank.
The calculation is possible up to the 7th order.

## *Elliptic lowpass filter*

Fig.B. 1 is the schematic of a 3rd-order lowpass filter (LPF):

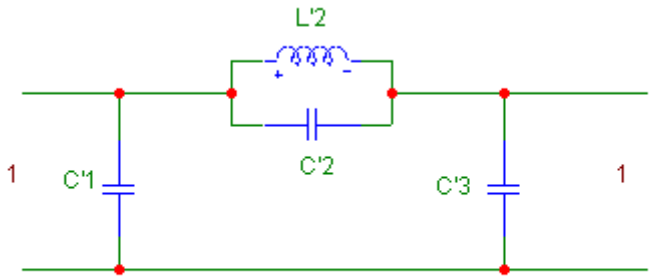


**Fig.B. 1 - 3rd-order Elliptic LPF**

Where $C_1'$, $C_2'$, $L_2'$ and $C_3'$ are normalized values.
We can find the values of the normalized components in a table of [75].
These ones depend on:

- The filter type: CC here for Elliptic
- The filter order: n
- $\rho$, which is linked to the ripple in the passband (see in table page 143, $A_{dB} = Rp$)
- $\theta$, which is linked to the attenuation in the stopband ($A_{min} = Rs$)

The, we note $\Omega_\infty$ and we find the normalized values.
To get the corresponding real values of the components, we have to determine $f_r$ and $R_r$.
Then we have:

$$C = C' \frac{1}{R_r \omega_r} \quad \text{(B.1)}$$

$$L = L' \frac{R_r}{\omega_r} \quad \text{(B.2)}$$

BPFs and HPFs are obtained from LPFs thanks to the following transformations.

## *Transformation of a LPF into a BPF*

A few steps are necessary. The first one is to replace all the capacitors of the LPF circuits by an inductor in parallel with a capacitor, and all the inductors of the LPF circuit by a capacitor and an inductor in series.

APPENDIX B: Computations of the components of an elliptic filter

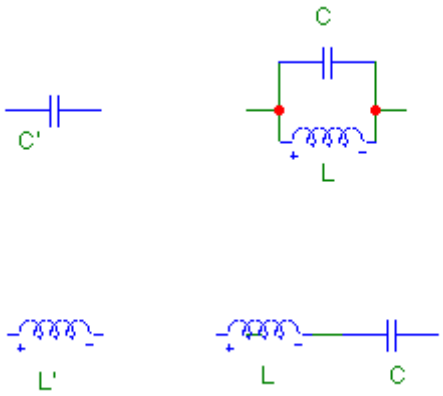


**Fig.B. 2 - LPF to BPF**

A special transformation has to be noticed, the following one:

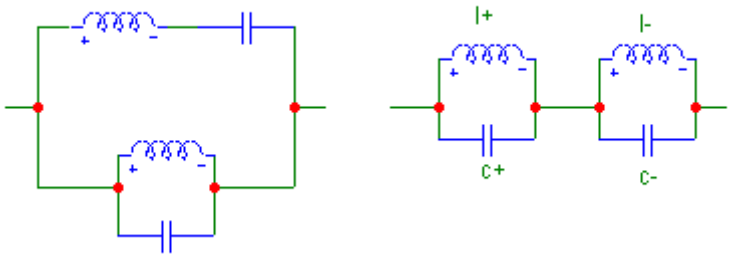


**Fig.B. 3 - Special transformation**

So that we obtain the following 3rd order Elliptic BPF:

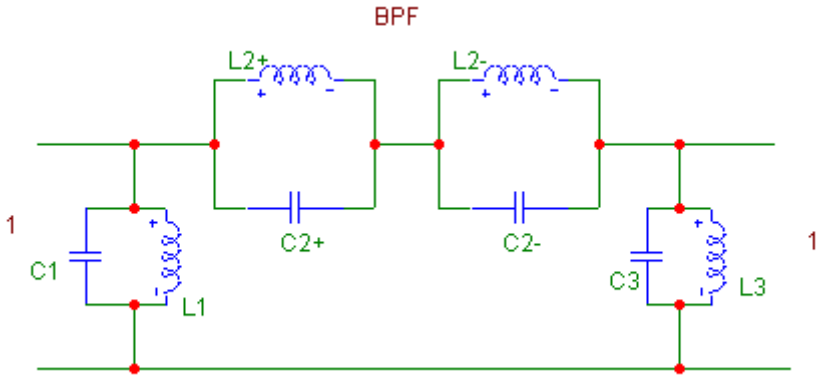


**Fig.B. 4 - 3rd-order Elliptic BPF**

A parameter $a$ should be defined to calculate real values as below:

$$a = \frac{f_0}{BW} \tag{B.3}$$

where $f_0$ is the central frequency and $BW$ the bandwidth of the bandpass filter. Then the components $C_1$, $L_1$, $C_3$ and $L_3$ can be computed easily:

$$C_{1,3} = aC'_{1,3}\frac{1}{R_r\omega_r} \tag{B.4}$$

$$L_{1,3} = \frac{1}{aC'_{1,3}}\frac{R_r}{\omega_r} \tag{B.5}$$

To calculate the four other components, more steps are necessary:

$$\Omega_{\pm} = \sqrt{1 + \left(\frac{\Omega_{\infty}}{2a}\right)^2} \pm \frac{\Omega_{\infty}}{2a} \tag{B.6}$$

$$c_{+} = \frac{1}{l_{-}} = ac'\left(1 + {\Omega_{-}}^2\right) \tag{B.7}$$

$$c_{-} = \frac{1}{l_{+}} = aC'\left(1 + {\Omega_{+}}^2\right) \tag{B.8}$$

Then,

$$C_{+} = c_{+}\frac{1}{R_r\omega_r} \tag{B.9}$$

$$C_{-} = c_{-}\frac{1}{R_r\omega_r} \tag{B.10}$$

$$L_{+} = l_{+}\frac{R_r}{\omega_r} \tag{B.11}$$

$$L_{-} = l_{-}\frac{R_r}{\omega_r} \tag{B.12}$$

### *Transformation of a LPF into a HPF*

The first step is to replace all the capacitors of the LPF circuits by an inductor and all the inductors of the LPF circuit by a capacitor.

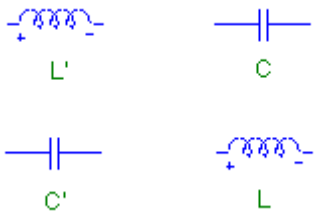


**Fig.B. 5 - LPF to HPF**

Then we obtain the following 3rd order Elliptic HPF:

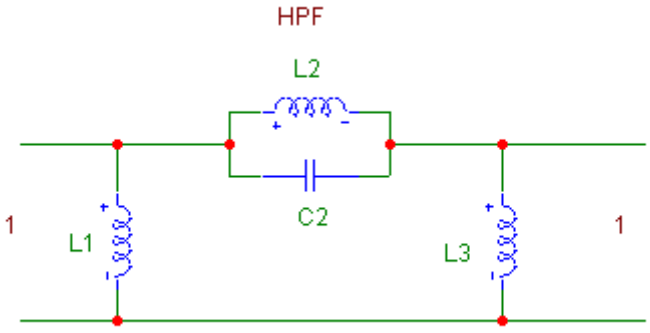


**Fig.B. 6 - 3rd-order Elliptic HPF**

Where

$$L_{1,2,3} = \frac{R_r}{C'_{1,2,3}\omega_r} \tag{B.13}$$

$$C_2 = \frac{1}{L'R_r\omega_r} \tag{B.14}$$

# APPENDIX C
# Relations between IRR and IQ mismatches

According to [76], we know that:

$$IRR = \frac{1 + 2A_{bal}cos(\Delta\theta) + {A_{bal}}^2}{1 - 2A_{bal}cos(\Delta\theta) + {A_{bal}}^2} \quad \text{(C.1)}$$

where $A_{bal}$ and $\Delta\theta$ define the amplitude ratio of I and Q outputs and phase deviation from an ideal 90° between I and Q branches, respectively.
From (C.1), we deduce:

$$IRR_{gain} = IRR_{\Delta\theta=0} = \left[\frac{1 + A_{bal}}{1 - A_{bal}}\right]^2 \quad \text{(C.2)}$$

And

$$IRR_{phase} = IRR_{Abal=1} = \cot^2\left(\frac{\Delta\theta}{2}\right) \quad \text{(C.3)}$$

- We will express $A_{bal}$ as a function of IRR, from (C.2):

$$IRR = \left[\frac{1 + A_{bal}}{1 - A_{bal}}\right]^2 \quad \text{(C.4)}$$

$$IRR = \left[\frac{1 + 2A_{bal} + {A_{bal}}^2}{1 - 2A_{bal} + {A_{bal}}^2}\right] \quad \text{(C.5)}$$

$$IRR\left(1 - 2A_{bal} + {A_{bal}}^2\right) = 1 + 2A_{bal} + {A_{bal}}^2 \quad \text{(C.6)}$$

$$(IRR - 1){A_{bal}}^2 - 2(IRR + 1)A_{bal} + (IRR - 1) = 0 \quad \text{(C.7)}$$

This is a 2nd-order equation.

$$\Delta = 4(IRR + 1)^2 - 4(IRR - 1) \quad \text{(C.8)}$$

$$\Delta = 4[IRR^2 + 2IRR + 1 - (IRR^2 - 2IRR + 1)] \quad \text{(C.9)}$$

$$\Delta = 4 \times 4IRR = 16IRR \quad \text{(C.10)}$$

$$A_{bal} = \frac{2(IRR + 1) + \sqrt{16IRR}}{2(IRR - 1)} \quad \text{(C.11)}$$

$$A_{bal} = \frac{IRR + 2\sqrt{IRR} + 1}{IRR - 1} \quad \text{(C.12)}$$

Numerical application:
We need $IRR_{dB} = 60dB$, so $IRR = 10^6$

$$A_{bal} = \frac{10^6 + 2\sqrt{10^6} + 1}{10^6 - 1} \approx 1.002$$

$$A_{bal\_dB} = 20\log(A_{bal}) \approx 0.017dB$$

- We will express $\Delta\theta$ as a function of IRR, from (C.3):

$$IRR = \cot^2\left(\frac{\Delta\theta}{2}\right) \quad \text{(C.13)}$$

$$IRR = \frac{1}{\tan^2\left(\frac{\Delta\theta}{2}\right)} \quad \text{(C.14)}$$

APPENDIX C: Relations between IRR and IQ mismatches

$$\tan^2\left(\frac{\Delta\theta}{2}\right) = \frac{1}{IRR} \quad \text{(C.15)}$$

$$\tan\left(\frac{\Delta\theta}{2}\right) = \frac{1}{\sqrt{IRR}} \quad \text{(C.16)}$$

$$\frac{\Delta\theta}{2} = \arctan\left(\frac{1}{\sqrt{IRR}}\right) \quad \text{(C.17)}$$

$$\Delta\theta = 2arctan\left(\frac{1}{\sqrt{IRR}}\right) \quad \text{(C.18)}$$

Numerical application:
We need $IRR_{dB} = 60dB$, so $IRR = 10^6$

$$\Delta\theta = 2arctan\left(\frac{1}{\sqrt{10^6}}\right) \approx 0.002$$

$$\Delta\theta = \Delta\theta \times \frac{180}{\pi} \approx 0.11°$$

In order to achieve an IRR of 60dB, gain and phase errors must be 0.01dB and 0.1° respectively [77].
These results correspond to the figure below, extracted from [77]:

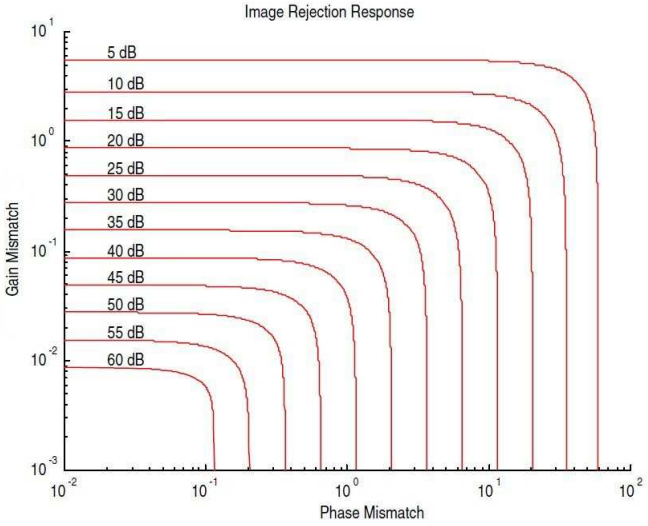


**Fig.C. 1 - IRR as a function of gain and phase errors**

# APPENDIX D
# Calculation of the SNR for a system with analytical signals

This appendix aims to compare SNRs at the output of a system with a real signal as input, and at the output of a system with analytical signals as input.

### *1st case: system with a real signal as input*

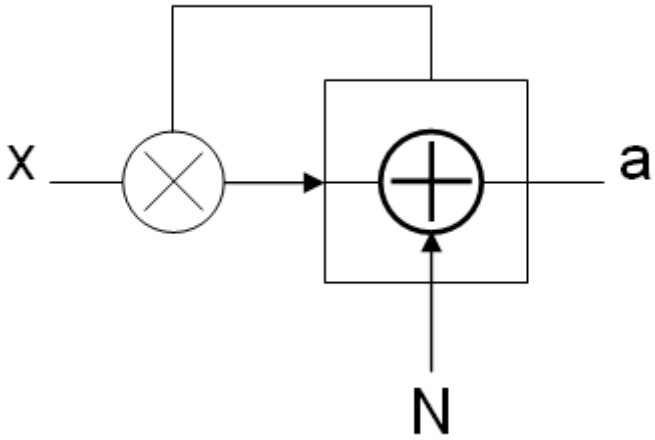


**Fig.D. 1 - Classical system with a real signal**

Suppose that the real input is a sinusoid, as follow:

$$x(t) = A\cos(\omega_0 t) \tag{D.1}$$

We consider an additive noise $N$ such that:

$$mean\big(n(t)\big) = 0 \tag{D.2}$$

And

$$std\big(n(t)\big) = N_{rms} \tag{D.3}$$

So the output is:

$$a(t) = x(t) + n(t) \tag{D.4}$$

$$a(t) = A\cos(\omega_0 t) + n(t) \tag{D.5}$$

$$SNR_a = \frac{A}{\sqrt{2} \times N_{rms}} \tag{D.6}$$

### *2nd case: system with analytical signals*

APPENDIX D: Calculation of the SNR for a system with analytical signals

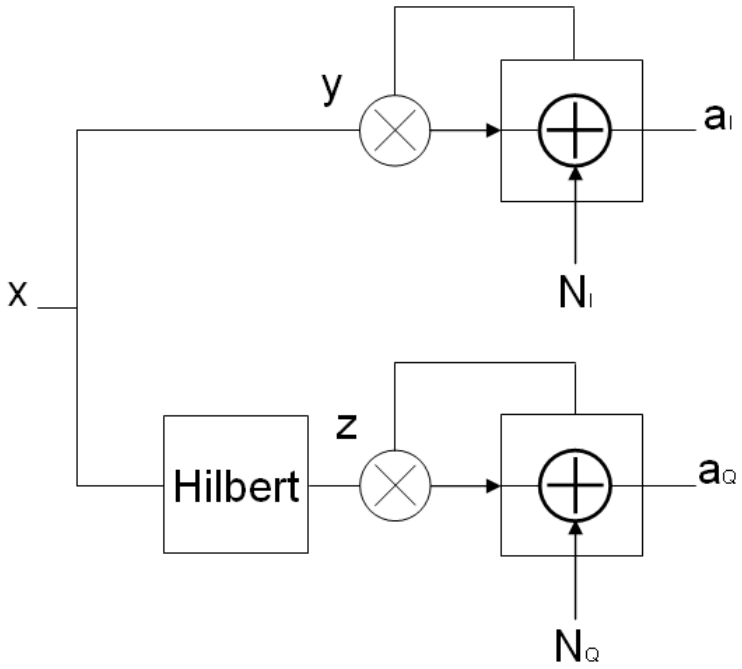


**Fig.D. 2 - System with analytic signals**

Given the same input signal:

$$x(t) = A\cos(\omega_0 t) \tag{D.7}$$

Thus, we have:

$$y(t) = A\cos(\omega_0 t) \tag{D.8}$$
$$z(t) = A\sin(\omega_0 t) \tag{D.9}$$

(quadrature thanks to Hilbert filter)

We notice that $y$ and $z$ are non-correlated (complex base (1,j) orthonormal)

$$a_I(t) = y(t) + N_I(t) \tag{D.10}$$
$$a_I(t) = x(t) + N_I(t) \tag{D.11}$$
$$a_I(t) = A\cos(\omega_0 t) + N_I(t) \tag{D.12}$$
$$a_Q(t) = z(t) + N_Q(t) \tag{D.13}$$
$$a_Q(t) = A\sin(\omega_0 t) + N_Q(t) \tag{D.14}$$

$N_I$ and $N_Q$ are uncorrelated but have the same std.

$$a_I(t) + ja_Q(t) = A\{\cos(\omega_0 t) + j\sin(\omega_0 t)\} + N_I(t) + N_Q(t) \tag{D.15}$$

$$SNR_{a_I+ja_Q} = \frac{std(A\{\cos(\omega_0 t) + j\sin(\omega_0 t)\})}{std\big(N_I(t) + N_Q(t)\big)} \tag{D.16}$$

## *Comparison*

$$\frac{SNR_{a_I+ja_Q}}{SNR_a} = \frac{\frac{std(sig_{cx})}{std(n_{cx})}}{\frac{std(sig_{Re})}{std(n_{Re})}} \tag{D.17}$$

APPENDIX D: Calculation of the SNR for a system with analytical signals

$$\frac{SNR_{a_I+ja_Q}}{SNR_a} = \frac{std(sig_{cx})}{std(sig_{Re})}\frac{std(n_{Re})}{std(n_{cx})} \quad \text{(D.18)}$$

To calculate this expression, we can first neglect noise in both systems ($N_{rms} = 10^{-10}$ for example).
Thanks to Matlab's program, we have:

$$\left.\frac{std\_cx}{std\_cos}\right|_{N\ll 1} = \sqrt{2} \quad \text{(D.19)}$$

Similarly, if we neglect the signal ($A = 10^{-40}$ for example), we have:

$$\left.\frac{std\_cx}{std\_cos}\right|_{A\ll 1} = \sqrt{2} \quad \text{(D.20)}$$

$$\frac{SNR_{a_I+ja_Q}}{SNR_a} = \left.\frac{std\_cx}{std\_cos}\right|_{N\ll 1} \times \left.\frac{std\_cos}{std\_cx}\right|_{A\ll 1} \quad \text{(D.21)}$$

$$\frac{SNR_{a_I+ja_Q}}{SNR_a} = \sqrt{2} \times \frac{1}{\sqrt{2}} = 1 \quad \text{(D.22)}$$

$$SNR_{a_I+ja_Q} = SNR_a \quad \text{(D.23)}$$

### *Conclusion*

For a given performance (noise floor), a system with an analytical signal has the same performance as a system with a real signal, because both analytical signals and noise are uncorrelated.

# APPENDIX E
# Trade-off between Fs and filter orders

There is a trade-off between the reduction of the sampling rate Fs and the complexity of the analog filters. The results have been obtained with Matlab for 2 and 4 subbands with equal bandwidth.
The minimum sampling rate is $Fs = B$. In this case, the aliasing is adjacent to the wanted signal and could only be attenuated with a square filter, which is not feasible. So, we progressively increase the sampling rate and look at the order of the filters, up to $7^{th}$-order filters only. For higher orders, the coefficients of the Elliptic filters are not available in [75].

- M=2

**Table E. 1 - Trade-off between Fs and filter orders for M=2**

| Subband n° | Elliptic filter / order | Fs (Hz) |
|---|---|---|
| 1<br>50MHz → 525MHz | LPF / 6 | > 760M |
| | LPF / 7 | > 626M |
| 2<br>525MHz → 1GHz | HPF / 3 | > 923M |
| | HPF / 4 | > 830M |
| | HPF / 5 | > 734M |
| | HPF / 6 | > 653M |
| | HPF / 7 | > 592M |

In the case of 2 subbands, the minimum sampling rate is $Fs = 475MHz$. Then, the minimum sampling rate such that a $7^{th}$-order Elliptic LPF reject the aliasing of at least 60dB is $Fs = 626MHz$. Similarly, $Fs = 592MHz$ is the minimum sampling frequency such that the aliasing is sufficiently rejected by a $7^{th}$-order Elliptic HPF. For this study, we increase the sampling rate up to $Fs = 950MHz$, which is the minimum sampling rate for the whole band (from 50MHz to 1GHz). We notice that the filters orders obviously decrease, since the aliasing fall much further away from the wanted subband. If we increase $Fs$ above 950MHz, alias fall out of the band and then, the constraints on the filter order are much relaxed, since the filters role is just to reject power, not aliasing.

- M=4

**Table E. 2 - Trade-off between Fs and filter orders for M=4**

| Subband n° | Elliptic filter / order | Fs (Hz) |
|---|---|---|
| 1<br>50MHz → 287.5MHz | LPF / 4 | > 855M |
| | LPF / 5 | > 524M |
| | LPF / 6 | > 388M |
| | LPF / 7 | > 322M |
| 2<br>287.5MHz → 525MHz | BPF / 4 | > 627M |
| | BPF / 5 | > 406M |
| | BPF / 6 | > 323M |
| | BPF / 7 | > 284M |
| 3<br>525MHz → 762.5MHz | BPF / 5 | > 388M |
| | BPF / 6 | > 314M |
| | BPF / 7 | > 280M |
| 4<br>762.5MHz → 1GHz | HPF / 3 | > 891M |
| | HPF / 4 | > 757M |
| | HPF / 5 | > 618M |
| | HPF / 6 | > 499M |
| | HPF / 7 | > 410M |

# APPENDIX F
# Theory of 3rd-order Butterworth filters

We calculate the transfer function of the 3rd-order Butterworth lowpass filter from the following schematic:

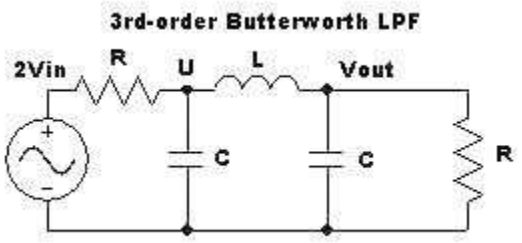


**Fig.F. 1 - 3rd-order Butterworth LPF**

On the one hand, we have:

$$U = \frac{2Vin}{1 + RCs + (1 + RCs)\dfrac{R}{Ls + RLCs^2 + R}} \tag{F.1}$$

And on the other hand, we have:

$$Vout = \frac{R}{R + Ls + RLCs^2}.U \tag{F.2}$$

Thus, from (F.1) and (F.2) we have the transfer function:

$$\frac{Vout}{Vin} = \frac{\dfrac{2}{RLC^2}}{s^3 + \dfrac{2}{RC}s^2 + \dfrac{L + 2R^2C}{R^2LC^2}s + \dfrac{2}{RLC^2}} \tag{F.3}$$

which is equivalent to:

$$H = \frac{\gamma}{s^3 + \alpha.s^2 + \beta.s + \gamma} \tag{F.4}$$

with $\alpha = \frac{2}{RC}$, $\beta = \frac{L+2R^2C}{R^2LC^2}$ and $\gamma = \frac{2}{RLC^2}$.

We know that the cutoff pulsation, $\omega_c$, satisfies the following condition:

$$|H(\omega_c)|^2 = \frac{1}{2} \tag{F.5}$$

Thus, we get equation (F.6):

$$\omega_c{}^6 + (\alpha^2 - 2\beta)\omega_c{}^4 + (\beta^2 - 2\alpha\gamma)\omega_c{}^2 - \gamma^2 = 0 \tag{F.6}$$

which is also:

$$ax^3 + bx^2 + cx + d = 0 \tag{F.7}$$

where $x = \omega_c{}^2$, $a = 1$, $b = \alpha^2 - 2\beta$, $c = \beta^2 - 2\alpha\gamma$, and $d = -\gamma^2$.
To find the solutions of equation (F.7), we use the Cardan's method. It shows that the discriminant Δ is:

$$\Delta = q^2 + 4\frac{p^3}{27} \tag{F.8}$$

where $p = \left(\frac{-b^2}{3a^2} + \frac{c}{a}\right)$, and $q = \frac{b}{27a}\left(\frac{2b^2}{a^2} - \frac{9c}{a}\right) + \frac{d}{a}$

In our case, the discriminant is positive and there are three solutions, with only one that is real:

$$x_1 = \sqrt[3]{\frac{-q + \sqrt{\Delta}}{2}} + \sqrt[3]{\frac{-q - \sqrt{\Delta}}{2}} - \frac{b}{3a} \quad \text{(F.9)}$$

So $x_1$ corresponds to ${\omega_c}^2$, i.e. the square of the cutoff pulsation, and we can easily find the cutoff frequency of this filter.

Using the same approach, we can deduce the cutoff frequency of the 3rd-order highpass filter. Fig.F. 2 recalls the schematic of the 3rd-order Butterworth highpass filter.

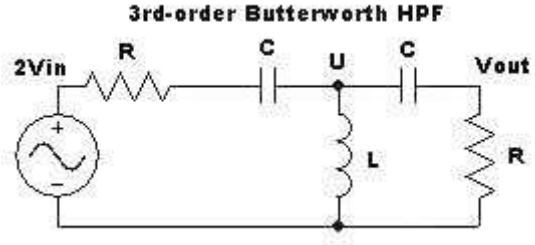


**Fig.F. 2 - 3rd-order Butterworth HPF**

We calculate that:

$$U = \frac{2Vin}{2 + \frac{R}{Ls} + \frac{1}{LCs^2}} \quad \text{(F.10)}$$

and

$$Vout = \frac{R}{R + \frac{1}{Cs}}.U \quad \text{(F.11)}$$

Thus, the transfer function of this filter is:

$$\frac{Vout}{Vin} = \frac{s^3}{s^3 + \frac{2L + R^2C}{2RLC}s^2 + \frac{1}{LC}s + \frac{1}{2RLC^2}} \quad \text{(F.12)}$$

which is equivalent to:

$$H = \frac{s^3}{s^3 + \alpha s^2 + \beta s + \gamma} \quad \text{(F.13)}$$

with $\alpha = \frac{2L+R^2C}{2RLC}$, $\beta = \frac{1}{LC}$ and $\gamma = \frac{1}{2RLC^2}$.

The cutoff pulsation, $\omega_c$, is the solution of equation (F.14):

$${\omega_c}^6 + (2\beta - \alpha^2){\omega_c}^4 + (2\alpha\gamma - \beta^2){\omega_c}^2 - \gamma^2 = 0 \quad \text{(F.14)}$$

which can be found using the Cardan'method.

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## *Abstract:*

This thesis is a partnership between the BL TVFE of NXP Semiconductors and ESIEE. Its goal is to provide a solution to multi-channel reception for cable network. This is linked to the problematic of broadband digitization. In the first part, the state-of-the art of ADCs, parallel architectures (TI and HFB) and sampling methods (bandpass sampling and complex sampling) is recalled. Then we study an architecture called RFFB with a bank of analog filters and a bank of ADCs. We try to reduce the constraints on ADCs, especially the sampling rate with the different sampling. We propose an interesting solution to broadband digitization and compare this solution to a challenging wideband ADC, using the cost function we introduce. This architecture has the major advantage that all the components are feasible, even the ADCs, and it is possible to switch-off subbands to save power. It could be a good solution at the present time but it is not competitive in terms of power consumption and surface. An alternative is proposed in Part 3, where we study Hybrid Filter Banks. It is interesting to study this architecture with realization feasibility in mind. This is why we select a 2-channel HFB with a lowpass filter and a highpass filter as analog filters. Then we propose an efficient optimization algorithm to find the best synthesis filters and reach our targets of distortion and aliasing rejection. An identification of analog filters is also suggested to cope with the issue of sensitivity to analog errors. Finally, a physical realization proves the concept of aliasing rejection and confirms the theoretical issues of this architecture.


*Keywords*: Analog-to-Digital Conversion, multi-channel reception, broadband digitization, Hybrid Filter Banks


## *Résumé:*

Cette thèse est le fruit d'un partenariat entre la BL TVFE de NXP Semiconductors et l'ESIEE dans le cadre d'une thèse CIFRE. Le but est d'apporter une solution qui permette la réception de plusieurs canaux pour le câble. Ce sujet est lié à la problématique de numérisation large bande. Dans la première partie, nous faisons un état-de-l'art sur les convertisseurs analogiques-numériques (CAN), sur les architectures parallèles (entrelacement temporel et bancs de filtres hybrides (BFH)), et sur les méthodes d'échantillonnage (passe-bande et complexe). Puis, nous étudions une architecture composée d'un banc de filtres analogiques et un banc de CANs. Nous cherchons à réduire surtout le taux d'échantillonnage. Nous comparons notre solution à un CAN large bande performant, avec notre fonction de coût. L'un des avantages de cette architecture est que tous les composants sont faisables, même les CANs, et qu'il est possible d'éteindre des sous-bandes pour diminuer la consommation. Cette solution est intéressante pour le moment mais n'est pas compétitive en termes de consommation et de surface. Nous proposons une alternative dans la partie 3, avec les BFH. Nous étudions cette architecture, en gardant à l'esprit la faisabilité de la solution. Nous avons choisi un BFH à deux voies, avec un filtre analogique passe-bas et un passe-haut. Puis, nous proposons un algorithme d'optimisation des filtres de synthèse pour atteindre nos objectifs de distorsion et de réjection de repliement. Une identification des filtres analogiques est aussi présentée. Finalement, une réalisation physique prouve le concept et valide les limitations théoriques de cette architecture.


*Mots-clés* : Conversion analogique-numérique, réception multi-canaux, numérisation large bande, bancs de filtres hybrides