International Journal of Electrical and Computer Engineering (IJECE)
Vol. 12, No. 2, April 2022, pp. 1223~1232
ISSN: 2088-8708, DOI: 10.11591/ijece.v12i2.pp1223-1232

Input-output linearization of DC-DC converter with discrete sliding mode fuzzy control strategy

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Article Info

Article history:

Received Apr 29, 2021
Revised Sep 17, 2021
Accepted Oct 10, 2021

Keywords:

Boost converter
DC-DC converter
Discrete sliding mode control
Fuzzy logic control
Sliding mode fuzzy control

ABSTRACT

The major thrust of the paper is on designing a fuzzy logic approach has been combined with a well-known robust technique discrete sliding mode control (DSMC) to develop a new strategy for discrete sliding mode fuzzy control (DSMFC) in direct current (DC-DC) converter. Proposed scheme requires human expertise in the design of the rule base and is inherently stable. It also overcomes the limitation of DSMC, which requires bounds of uncertainty to be known for development of a DSMC control law. The scheme is also applicable to higher order systems unlike model following fuzzy control, where formation of rule base becomes difficult with rise in number of error and error derivative inputs. In this paper the linearization of input-output performance is carried out by the DSMFC algorithm for boost converter. The DSMFC strategy minimizes the chattering problem faced by the DSMC. The simulated performance of a discrete sliding mode fuzzy controller is studied and the results are investigated.

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1. INTRODUCTION

In the latest trends the usage of power electronic converters are increasing and a survey says that by the end of next decade, more than 70% of electrical energy will be from power electronic equipment. Rapid development of microelectronics has a pronounced influence on the development of power electronics by constant improvement and making it economically reliable. Most commonly used applications are switched-mode power supply (SMPS), personal computers and communication equipment [1]–[4]. These converters are subjected to high load fluctuation because of increase in package density of on-board digital chips, which deteriorate the converter performance. Hence there is a necessity for an efficient controller which can work well during rapid load fluctuations [5], [6].

Power electronic converters are commonly used for easy implementation, high efficiency, improved power factor, compact size, and flexibility in control. Boost converters are frequently used because of their simple circuit design and their ease of implementation [7]–[10]. The fuzzy controller has been introduced to overcome the chattering phenomena faced by the power converter by means of discrete sliding mode control (DSMC) [11]–[14]. Further the ease of implementation of fuzzy systems has been exploited for hardware implementation of the controller.

An adaptive back-stepping discrete sliding mode control (SMC) strategy is implemented for the boost converter in [15] and it is implemented in real time to ensure the stability. Simulation and hardware implementation is done successfully and validates that the behavior of the proposed system is superior to conventional methods. An improved SMC technique is developed by combining a disturbance estimator with continuous SMC to overcome the voltage linearization problem of the boost converter [16]. The robustness of the algorithm is proved by simulation and practical results under voltage and load disturbance conditions. An indirect SMC method is implemented in [17] to regulate single-ended primary-inductor converters (SEPIC) voltage in which the sliding function is reframed by incorporating the current error. This technique is simple to use and reduces the cost of the controller. The behavior of the prototype is verified under output and input side fluctuation conditions in buck and boosts modes.

The nonlinear boost converter model is designed with a perturbed relay system is explained in [18]; this is implemented in industrial processes and the non-linear responses are analyzed. Theoretical model is validated by experimental results. A new approach to maintain steady load power in boost, Cuk and SEPIC converters is explained in [19]. A simple, cheap, and small prototype is set-up and the results are validated. A dynamic SMC technique with type-2 neural network is implemented in [20] for boost converter voltage regulation. A new dynamic sliding surface is defined with duty ratio and reference value. The implemented error tracking system is stable under inductor and capacitor variations; the results are compared and validated with experimental set-up. An adaptive SMC law is implemented for event-triggered communication systems [21] by incorporating a stochastic semi-Markov switching function. This law is implemented successfully in boost converter and verified with theoretical calculation.

Small-signal design of the boost converter is proposed in [22] for photovoltaic (PV) fed applications. This paper is projecting the stability problems due to the additional input capacitor which is required to couple the PV array with boost converter. This model is validated by experimental set-up under continuous and dis-continuous current modes. A DSMC is implemented for PV fed Cuk converter [23]; stability of the proposed controller is verified by adding disturbance in input and load. A type-2 fuzzy controller is proposed to overcome the stability problems due to negative impedance characteristics of DC-DC converters [24]. This is a non-integer intelligent controller and improves the stability of the converters connected to constant power loads. All these control techniques are robust but the chattering problem faced by the SMC is not addressed.

From the literature survey it is clear that a smooth gain change can be achieved by merging SMC with fuzzy which can overcome the chattering response of the system under uncertainties. This paper deals with the new development and performance analysis of boost DC-DC converters with control (DSMFC) with extended load and source regulation. The new control scheme is validated through computer simulation and by comparing with existing techniques. In the block diagram as shown in Figure 1 the power converter used is buck/boost converter and load used is a resistive load, controller is DSMFC. This paper develops the design and the mathematical modeling of DSMFC for boost converters.

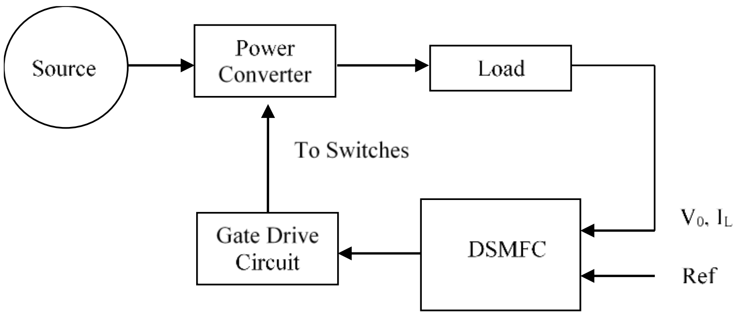

Figure 1. Block diagram representation of DSMFC

2. RESEARCH METHOD

2.1. Design of DSMC based boost converter

The circuit diagram of the boost converter is shown in Figure 2, where V_{in} is the supply voltage, L is the inductor connected in series with the supply voltage, a switch S1 is in shunt with the source and a capacitor C is connected across the load resistance R [9]. The discrete model of boost converter based SMC is represented by the (1) and (2), represents the discrete model when the switch is ON, (2) represents the discrete model when the switch is OFF [14].

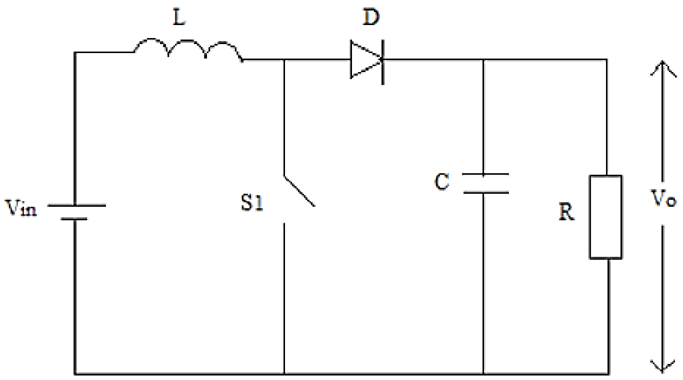

Figure 2. Circuit diagram of boost converter

$$x_1[K+1] = x_1[K] + \frac{T}{L}[V_{in} - (1-u)x_2] \quad (1)$$

$$x_2[K+1] = x_2[K] - \frac{T}{C}\left[\frac{x_2}{R} - (1-u)x_1\right] \quad (2)$$

Where $I_{ref}=\frac{V_{ref}i_L}{V_0}$

The sliding surface is given by the (3),

$$S[k] = e_p[k] + \mu_1 e_1[k] + \mu_2 e_2[k] \quad (3)$$

$$S[k] = x_1[k]x_2[k] - x_{1ref}x_{2ref} + \mu_1(x_1[k] - x_{1ref}) + \mu_2(x_2[k] - x_{2ref}) \quad (4)$$

where $e_1 = (x_1 - x_{1ref})$, $e_2 = (x_2 - x_{2ref})$ and $e_p = (x_1x_2 - x_{1ref}x_{2ref})$. Such that $\dot{e_1}[k] = \dot{x_1}[k]$ and $\dot{e_2}[k] = \dot{x_2}[k]$ where e_1 is the current error, e_2 is the voltage error, e_p is the power error, x_1 is the inductor current i_L, x_2 is the output voltage/capacitor voltage V_c and K is the positive integer.

The control law is given by the (5) where S is the sliding surface. The system has been converged when $S[k+1] < S[k]$, which can be obtained from Lyapunov stability criteria. That is when the future value is less than the present value then the system is converging.

$$u = \frac{1}{2}(1 - \mathrm{sgn}(S)) = \begin{cases} 0 \text{ if } S > 0 \\ 1 \text{ if } S < 0 \end{cases} \quad (5)$$

2.2. Mathematical modeling of discrete sliding mode fuzzy control for boost converter

The DSMFC based boost converter block diagram is shown in Figure 3, the controller uses the control signal $u[k]$ and change in control signal $u[k+1]$ as input to the controller. The foremost objective is to guarantee Lyapunov stability which used to satisfy the following condition $|S[k+1]| < |S[k]|$ [23]. Let the sliding surface be $S[k]$, the proposed DSMFC creates the derivative of the Lyapunov function as negative in sign. The rule-based table is established for this situation. They are: i) if $u[k]$ and $u\ [k+1]$ greater than zero then the duty cycle has to be increased; ii) else $u[k]$ and $u[k+1]$ less than zero then the duty cycle has to be decreased.

Thus, the control signal u[k] and its derivatives $u[k+1]$ are given as the input to the fuzzy controller, the output of the controller is the change in switching signal $\Delta\mu(k)$. The proposed DSMFC uses the sugeno fuzzy inference system (SFIS) from Simulink library. Fuzzification has been done by selecting gbell membership functions as fuzzy sets with the limit range [0 1] for the control signal u[k] and the change in control signal $u[k+1]$. The output signal is denoted by $\Delta\mu(k)$ where a set of rules are defined. The fuzzy set membership functions are symbolized by in1mf1, in1mf2, in1mf3, in1mf4, in1mf5, in1mf6, in1mf7 for input signals $u[k]$ and in2mf1, in2mf2, in2mf3, in2mf4, in2mf5, in2mf6, in2mf7 for u[k+1]. The change in Controller output signal $\Delta u[k]$ is specified in (6).

$$u[k] = \Delta u[k] + \Delta u[k-1] \quad (6)$$

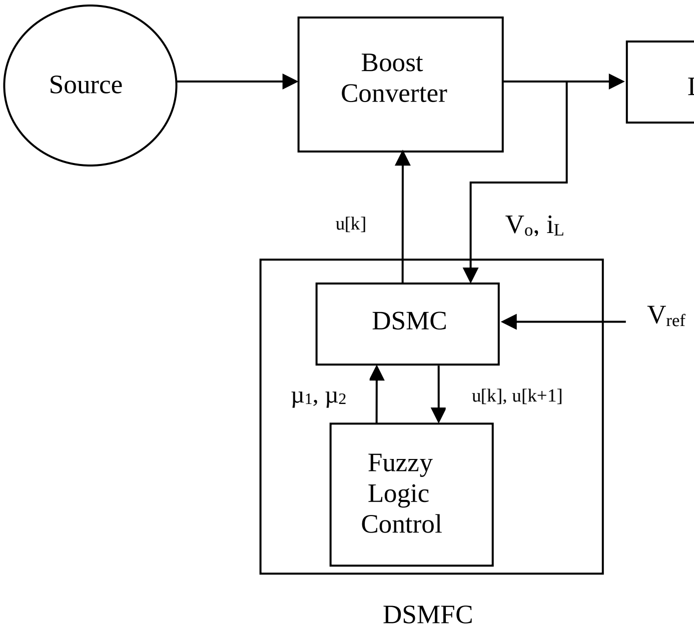

Figure 3. Block diagram of DSMFC for boost converter

3. RESULTS AND DISCUSSION

3.1. Used DSMFC boost converter

The DSMFC based boost converter is developed and simulated. metal oxide semiconductor field effect transistor (MOSFET) is recommended as a switch in this boost converter model because it has extraordinary speed of response [7], [8]. The switching of the MOSFET is controlled by DSMFC. The SFIS is composed of a fuzzification stage, a rule base table stage and a defuzzification stage. This can be achieved by means of rule editor function block in which input and output control parameters are well-defined with the assistance of membership functions. The rules are framed by choosing a suitable fuzzy set for each input variable such as $u[k]$ and $u[k+1]$ and also choosing the function $f(u)$ for the output variable. The gbell membership function has been used for both inputs in order to get smooth response for the corner values. The output parameter is specified by $\Delta\mu[k]$ and it has well-defined functions. The control surface can be viewed with the support of rule edit viewer function. The Figure 4 illustrates the simulated response of the control surface. This surface has been taken from the surface viewer of the rule edit function, which explains the controller output variation for different input combinations.

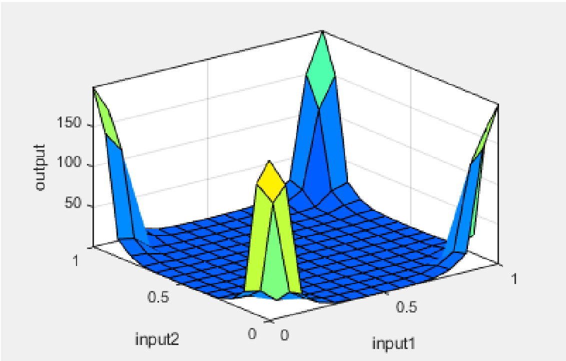

Figure 4. DSMFC control surface

The model of the DSMFC boost converter is simulated in the Simulink platform and the input voltage, inductor current, reference voltage and output voltage responses are illustrated in Figure 5. Initially input voltage is set as 5 V, during starting current response is started with a current spike of 12.5 A and settled quickly. The waveform is smooth until there is any sudden change. Reference voltage is set as 12 V; the output voltage is 12 V after a peak overshoot of 20.7852 V for the input of 5 V. A change in input voltage of 8 V is given at 0.5 sec; the output follows the reference with 12 V. When a change in reference voltage of 12 to 15 V is made at 0.7 sec; then the output response can be able to track the change. But there is a spike of 3 A at the time of 0.7 sec when there is a step change in reference voltage. This validates the robustness of the controller and the controller is able to track the reference even during sudden variations of the system parameters. From the analysis and simulated response of the boost converter it is clear that output voltage is more than or equal to the input excitation; and the simulation is conducted under discontinuous current mode.

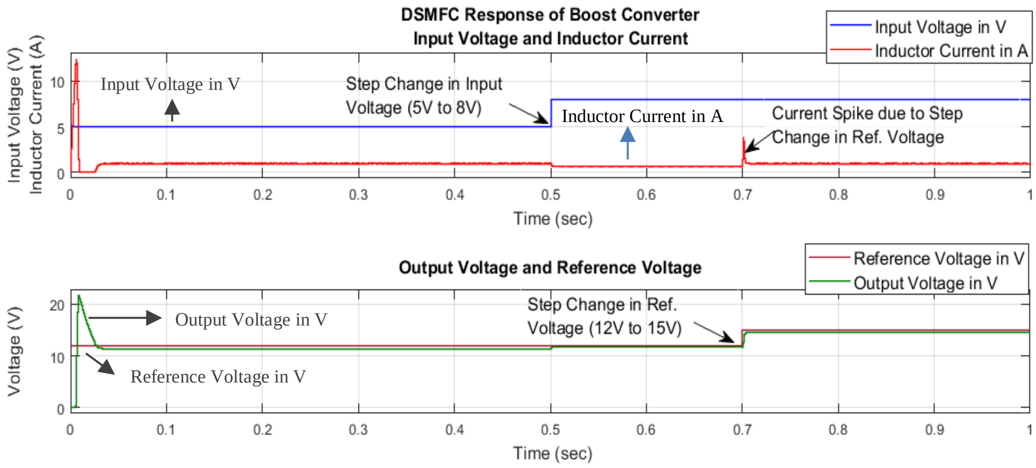

Figure 5. Simulated response of DSMFC boost converter for step-up change

The model of DSMFC is simulated with reduced input and reference voltage values. The simulated response of the boost converter has been plotted which is illustrated in Figure 6. Initially input voltage is set as 8 V, during starting current response is started with a current spike of 15.5 A and settled quickly. The waveform is smooth until it sees a change. Reference voltage is set as 15 V; the output voltage for the input of 8 V is 15 V after a peak overshoot of 29.5 V. A step-down in input voltage of 5 V is given at 0.5 sec; the output follows the reference with 14.5 V. A step-down in reference is introduced at 0.7 sec from 15 to 12 V; the output voltage can be able to track the reference of 12 V. This proved the robustness of the controller where the output is able to track the reference by sudden step-down variations of the system parameters.

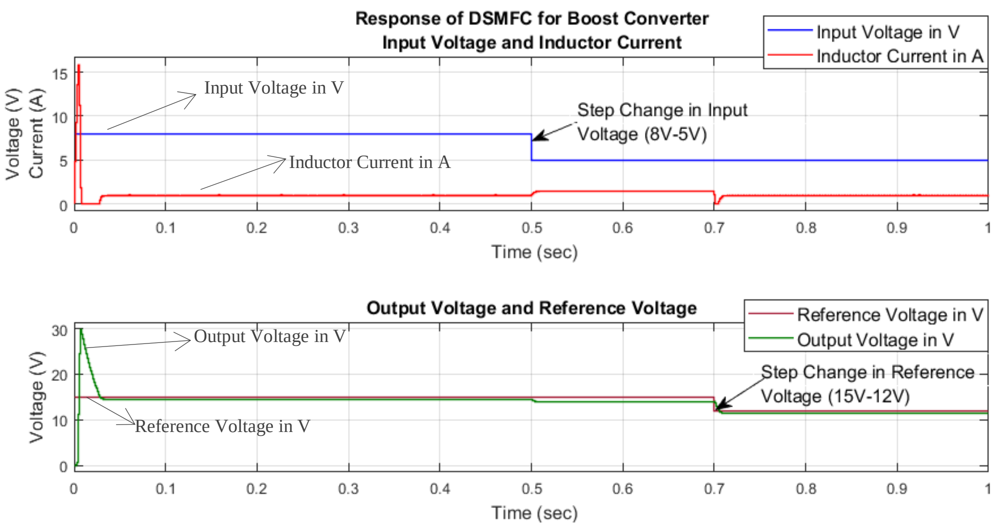

Figure 6. Simulated response of DSMFC boost converter for step-down change

The enlarged response of the DSMFC for the boost converter has been shown in Figure 7. It is observed that the chattering problem has been efficiently addressed along with reduced ripple current. Figure 8 illustrates the generated gate pulse of the simulated response of DSMFC for Boost converter along with input voltage with step change. Initially the input voltage has been set as 8 V; the corresponding gate pulse is shown in the second portion of the figure with pulse width of 10.9 µs. At a time of 0.5 sec; a step change in input voltage of 5 V is introduced. The gate pulse width got changed into 9.9 µs after the introduction of step change in input voltage.

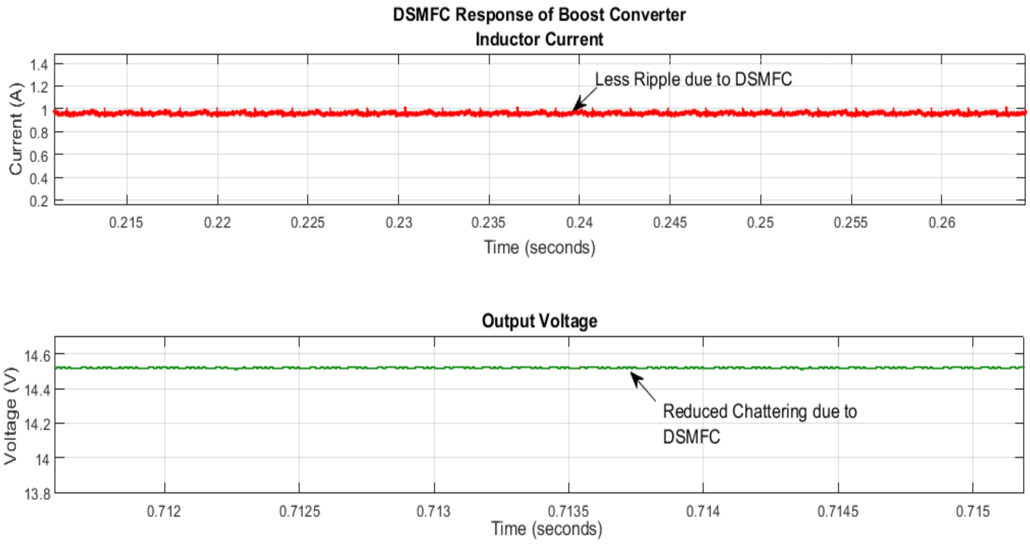

Figure 7. Enlarged response of DSMFC boost converter shows reduced chattering

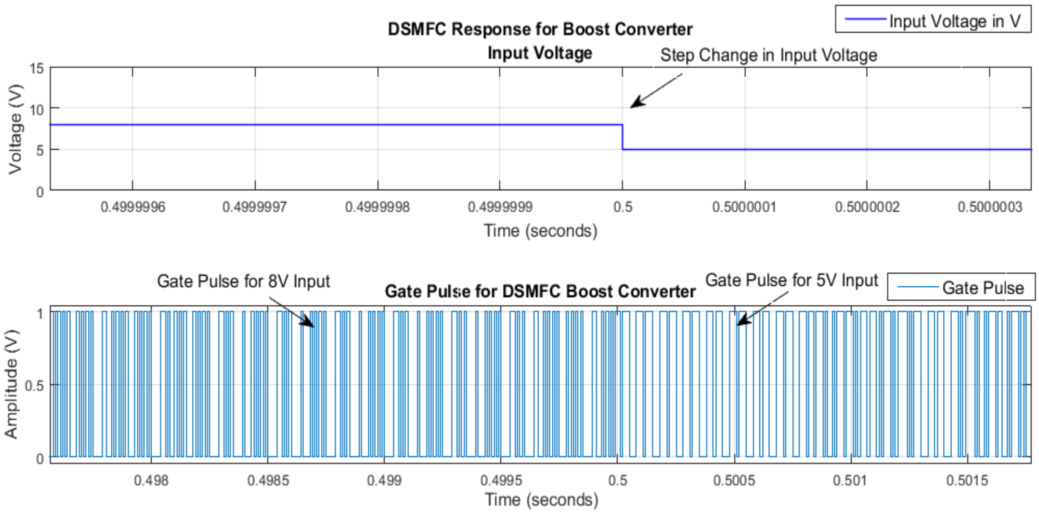

Figure 8. Gate pulse response of DSMFC for boost converter-input step change

Figure 9 illustrates the generated gate pulse of the simulated response of DSMFC for boost converter along with reference voltage with step changes. Initially the reference voltage is set as 15 V; the corresponding gate pulse is shown in the second portion of the figure with pulse width of 10.3 µs. At a time of 0.7 sec; a change in reference value of 12 V is made. The gate pulse width got changed into 5 µs after the incorporation of reference change. The reference voltages are selected according to the load voltage requirement.

The results from DSMC and DSMFC have been compared and it is observed that current has reduced ripple content with DSMFC. Figure 10 depicts the simulated results. Initially the input voltage is set as 15 V, the current of DSMC has a spike of 16 A but with DSMFC the spike is reduced to 12 A. When there is a step change in input voltage of 5 V at 0.5 sec there is a rise in current of 1.5 A in DSMC but the current is about 1 A in DSMFC, no spike introduced in both the controllers. When there is a step change in reference voltage of 12 V at 0.7 sec a low voltage spike of about 2 A is introduced in DFSMC but DSMC is not introducing any spike.

Figure 11 shows the enlarged response of the inductor currents of DSMC and DSMFC for boost converter. From the plot it is clear that the peak overshoot of inductor current for DSMFC is less than the DSMC; and also, the fluctuation of current is less due to change in input voltage for DSMFC. DSMFC for boost converter has been investigated; they find application in power converter circuits such as switched mode power converters, voltage regulators, battery operated vehicles and variable speed direct current (DC) drives because it offers smooth control under fluctuating loads. The simulated performance has been analyzed which is out of chattering. There is a boost in the output voltage for the given input voltage. When there is a step change in the input of the controller, it takes a short time to recover its performance which shows the robustness of the controller.

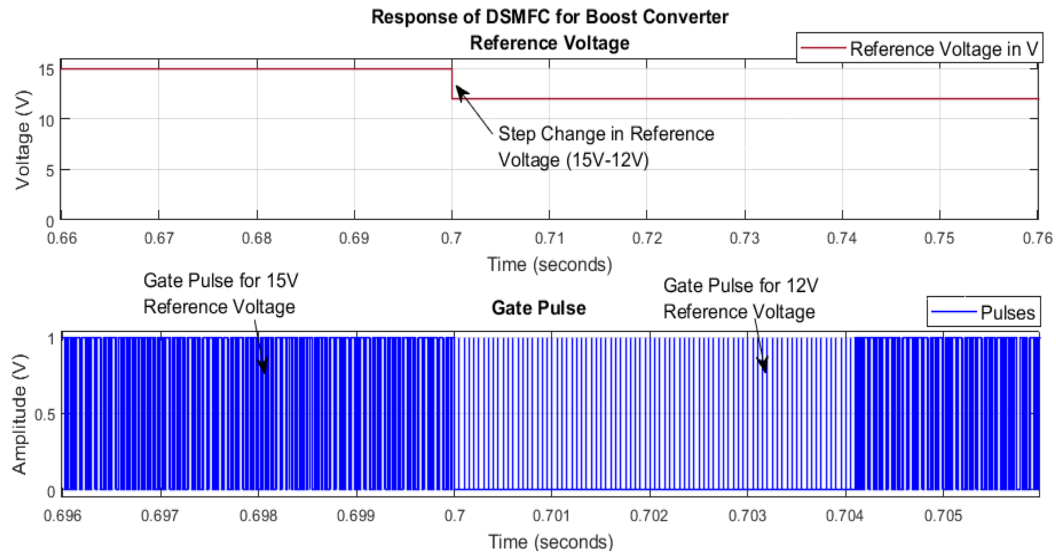

Figure 9. Gate pulse response of DSMFC for boost converter-reference step change

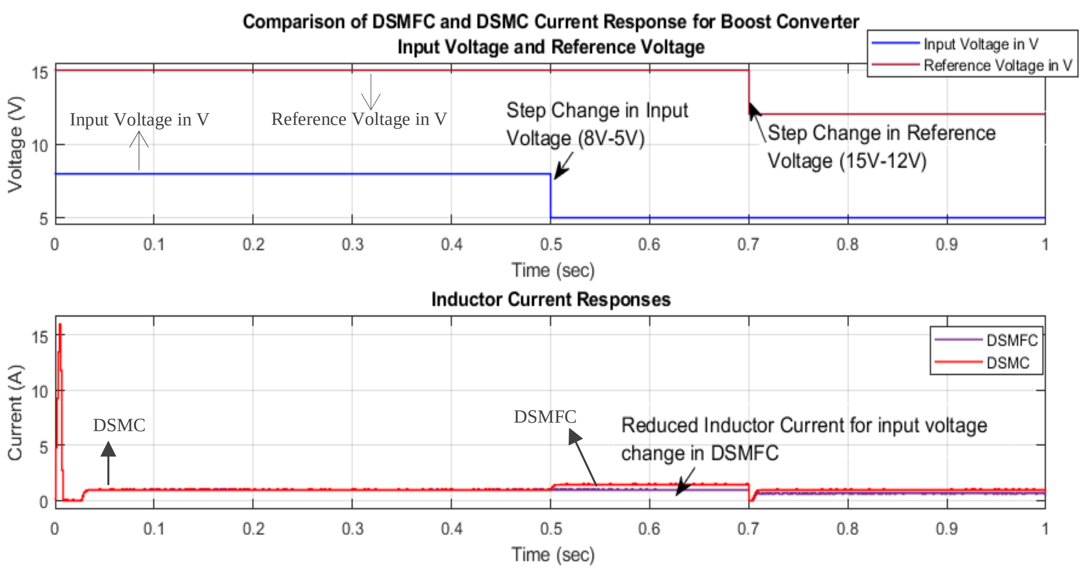

Figure 10. DSMC vs DSMFC comparative response for boost converter

3.2. Comparative analysis of DSMFC with DSMC for boost converter

Table 1 shows the results of a boost converter with DSMFC and DSMC techniques. Table 2 shows the improvements for the boost converter. In the voltage response of DSMFC, the rise time is 0.3 msec faster, the settling time is 3 msec faster, the peak time is 1.12 msec faster and percentage overshoot is 10% reduced as compared to DSMC. In the current response of DSMFC the rise time is 0.106 msec faster, the settling time is 2 msec faster, the peak time is 3.2 msec faster compared to DSMC. The SMC suppresses the oscillations in less than 10 sec [25], but the DSMC and DSMFC can reduce the oscillations in less than 20 msec of time.

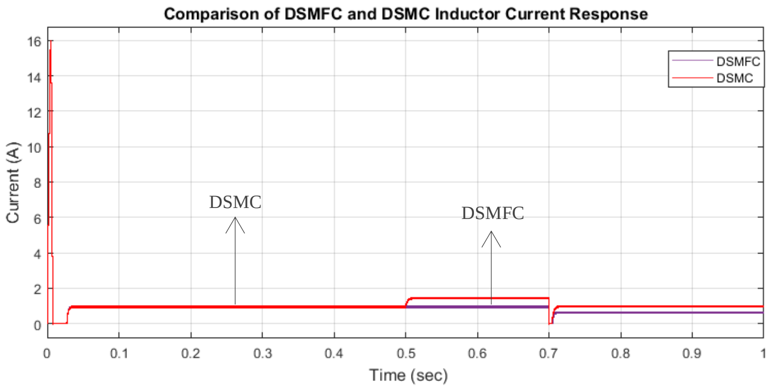

Figure 11. Comparison of DSMFC and DSMC inductor currents

Table 1. DSMFC-boost converter response (V_{in}=5 to 8 V, V_{ref}=12 to 15 V)

No.	Parameter	DSMFC		DSMC	
		Voltage response	Current response	Voltage response	Current response
1	Rise Time	0.9 msec	0.18 msec	1.2 msec	0.286 msec
2	Settling Time	17 msec	10 msec	20 msec	12 msec
3	Peak	20.7852 V	12.5 A	21.9852 V	12.503 A
4	Peak Time	8.0 msec	2.8 msec	9.12 msec	6.0 msec

Table 2. Improvement table for boost converter

No.	Response	Parameter	DSMFC	DSMC	Improvement	Percentage Improvement
1	Voltage Response	Rise Time	0.9 msec	1.2 msec	0.3 msec faster rise time	25%
		Settling Time	17 msec	20 msec	3 msec faster settling time	15%
		Peak Time	8.0 msec	9.12 msec	1.12 msec faster peak time	12.3%
		% overshoot	73.21%	83.21%	10%	10% reduced
2	Current Response	Rise Time	0.18 msec	0.286 msec	0.106 msec faster rise time	37%
		settling time	10 msec	12 msec	2 msec faster settling time	16.7%
		Peak Time	2.8 msec	6.0 msec	3.2 msec faster Peak Time	53.33%

4. CONCLUSION

In this paper control strategy based on DSMFC has been implemented for boost power converters which can be used for power converter applications such as switched mode power supplies. In both the cases such as change in reference and input; the output is able to track the reference, the chattering problem of DSMC strategy has been reduced by the incorporation of fuzzy logic. The robustness of the system has been investigated by introducing sudden change in input and reference voltages. The comparative analysis of this controller with DSMC has also been analyzed. It is observed that the DSMFC gives linearized output.

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BIOGRAPHIES OF AUTHORS

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