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An efficient design of 45-nm CMOS low-noise charge sensitive amplifier for wireless receivers

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ABSTRACT

Amplifiers are widely used in signal receiving circuits, such as antennas, medical imaging, wireless devices and many other applications. However, one of the most challenging problems when building an amplifier circuit is the noise, since it affects the quality of the intended received signal in most wireless applications. Therefore, a preamplifier is usually placed close to the main sensor to reduce the effects of interferences and to amplify the received signal without degrading the signal-to-noise ratio. Although different designs have been optimized and tested in the literature, all of them are using larger than 100 nm technologies which have led to a modest performance in terms of equivalent noise charge (ENC), gain, power consumption, and response time. In contrast, we consider in this paper a new amplifier design technology trend and move towards sub 100 nm to enhance its performance. In this work, we use a pre-well-known design of a preamplifier circuit and rebuild it using 45 nm CMOS technology, which is made for the first time in such circuits. Performance evaluation shows that our proposed scaling technology, compared with other scaling technology, extremely reduces ENC of the circuit by more than 95%. The noise spectral density and time resolution are also reduced by 25% and 95% respectively. In addition, power consumption is decreased due to the reduced channel length by 90%. As a result, all of those enhancements make our proposed circuit more suitable for medical and wireless devices.

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1. INTRODUCTION

Massive researches have been healed throughout decades in many wireless applications, medical imaging, and radiation detectors front-end circuits. As received signal has low amplitude and low Signal-to-noise ratio (SNR). It should be treated and manipulated by a circuit that takes the desired signal and wipes out or filters other noise signals, which is mainly done by a preamplifier. This preamplifier is an operational amplifier (OpAmp) used in amplifier integrator mode by using a feedback capacitance. The integrator mode of operation enables OpAmps to integrate weak charge pulses into voltage pulses. A preamplifier is used to enhance the SNR by converting the incoming charge into a usable voltage pulse signal in order to process it in later stages using the remaining components of the readout system. Because of that, this type of amplifier is called "charge amplifier" [1]-[4]. The integration mode amplifiers have very high input impedance, while the

output stage is a low-impedance buffer to drive a detected signal to the remaining components of the system. Figure 1 illustrates the basic charge sensitive amplifier (CSA) [1], [2], [5], [6].

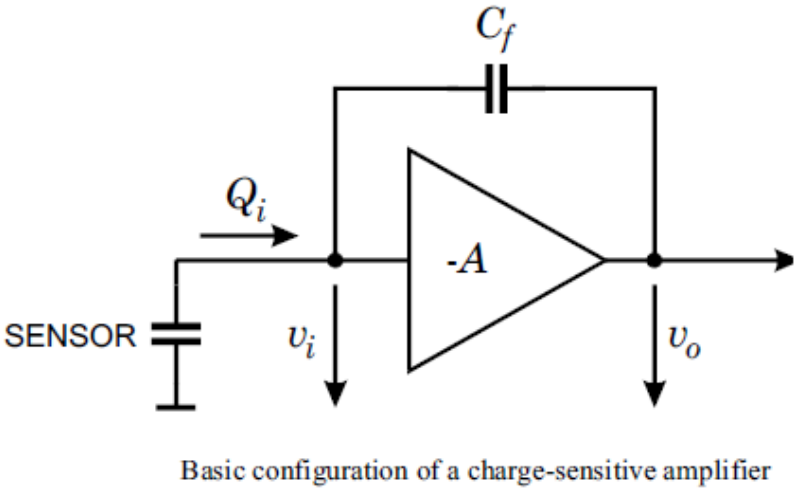

Figure 1. Basic charge sensitive amplifier

When looking at the transistor level, complementary metal–oxide–semiconductor (CMOS)-based technology is the dominant technology for CSA circuits and even for any other low-power amplifier application. Low noise field effect transistor (FET) comes as a first stage in the charge amplifiers [1]-[4]. The charge amplifier's open-loop gain is set sufficiently high so that the amplification is not affected by the detector capacitance. On the other hand, the input metal oxide semiconductor field effect transistor (MOSFET) of the preamplifier is designed and optimized to be the dominant noise source of the entire system. Many research papers made comparisons on the usage of junction field effect transistors (JFETs), bipolar junction transistors (BJTs), gallium arsenid metal semiconductor field effect transistor (GaAs MESFET), and CMOS [6] in terms of cost, SNR, and power consumption. In these comparisons, CMOS proved its advantages over other transistors. MOSFET has a high transconductance [7], [8] that generates smaller noise; this is useful for high-resolution images. Also, its low power consumption makes it better for high-dense detectors applications. As an example of the importance of low power consumption, a high-resolution positron emission tomography (PET) scanner system, manufactured by lutetium oxyorthosilicate (LSO) crystals coupled to avalanche photodiode (APD) arrays, uses up to 55K preamplifiers [6]. If we assume that a single CSA requires 1 mA current, then the PET scanner requires a total of 55 A. Thus, this example shows us that developing CSA is a very crucial issue regarding its power consumption [3], [4]. As a result, all state of art papers agree on CMOS and only CMOS to use in designing preamplifiers [9]-[13], but they still negotiate on which CMOS topology is more efficient.

Since the 90s of the last century, CMOS-based CSA circuits became technology dominant till now. From that time, all designers benefited from CMOS deep scaling down approach. Starting from 2 m CMOS [3], [4] down to 0.8 m CMOS in early 2000 [2], reaching now values of 45 nm nowadays. This trend - accompanying designs proved its advantages for high resolution and small scale applications [14], [15]. As CSA is used in high power consuming applications, it needs to reduce the power it dissipates. In our work, we have concentrated on overcoming ENC and power consumption issues. These two critical issues are the most important characteristics that a designer should take into consideration for Femto-coulomb signals receiving applications like PET scanners, wireless sensor networks, and IoT applications [16]-[18].

In this paper, an efficient design of a CMOS regulated cascode topology preamplifier is presented. In this proposal, a well-known topology is used in such circuits but with 45 nm scaling technology. Simulation results have shown that the performance of the proposed design has been improved significantly: a microwatt CSA with lower e-rms ENC, reduced power spectral density, reduced timing resolution, and faster response time compared with other scaling technologies. Those enhancements make our circuit ideal for wireless applications where ultra-low power weak signal receivers and higher resolution images are used.

The rest of the paper is organized as follows: Section 2 reviews recent work in cascode topologies CSA circuits used in PET applications. Our system design preliminaries are described in section 3. Section 4 discusses scaling techniques used in our proposed circuit. Section 5 introduces our modified telescopic cascode topology CSA. Section 6 shows the simulation results of our proposed design compared to other related works, and section 7 ends the paper with conclusions and future work.

2. RELATED WORK

Many conducted research through the last decades has led to many advances in the medical imaging field. All design trends head towards reducing channel length in FET to enhance image quality [19]-[22] and thus it is going toward more FET shrinking, this trend proves that it is very powerful and efficient in terms of reducing ENC ratio and improving image quality.

Schmitt *et al.* [6] have proposed a CSA circuit for the first time in 1987. They aimed to design a preamplifier suitable for avalanche photodiode-based scintillation detectors in the range of 5-20 MHz frequency. In this proposal, they used Discrete MOSFET technology and proved its outperforming characteristics over BJT, JFET, and GaAs MESFET in terms of cost, ENC, and power consumption. BJTs and JFETs were commonly used for detectors at that time. They have enhanced a preamplifier circuit with 300 mW power consumption for each channel. They implemented a dual-channel preamplifier resulting in a total of 600 mW power consumption. They designed a suitable circuit for large-scale high-density applications and this was a fair good result at that time but not comparable to what it is found recently.

Binkley *et al.* [4] have introduced a transimpedance preamplifier circuit using Complementary FET technology for the first time. They used 2 m CMOS and implemented it for APD applications. In their work, they proved that the ENC in the transimpedance preamplifier is much smaller than in CSA, where the measured ENC was 560 electrons-rms at peaking time = 68 n (in our work ENC equals 43). The presented circuit in [4] recorded a huge reduction in power dissipation compared to [6] with estimated power dissipation equaled 38 mW. The problem in such a transimpedence preamplifier is the high W/L ratio which in their design was 1200. This results in larger preamplifier circuit physical dimensions; thus this deficit increases the parasitic capacitances and maximizes the external interference since the preamplifier is not close enough to the detector.

Paulus *et al.* [3] presented a modified cascode CSA circuit and compared it with a previous simple design folded cascode circuit. The simple cascode circuits require a high W/L FET to reduce the Miller effect on it - especially at the input FET - which leads to a decrement in the input capacitance of the preamplifier. However, a large W/L ratio will lead to undesired chip area size as mentioned above. Also, cascode topology produces a low open loop gain. Therefore, they introduced their modified 2 m CMOS cascode design, which was 50 times greater in open loop gain than that of the simple cascode. They reduced the W/L ratio from 1200 in the simple cascode topology to 100, which will affect significantly the chip area. The only exception was the input FET which was PMOS with 7500 m /2 m shape factor to set the amplifier input capacitance to approximately 10 pF. In this work, the authors succeeded to reduce the ENC of the detector circuit but this led to an increment in power dissipation to 50 mW compared to 38 mW in [3]. This flaw affects Thick-film fabrication disallowing high density detector arrays to be implemented and reducing image resolution.

Binkley *et al.* [2] had returned to the regular simple cascode CSA topology but this time with 800 nm CMOS technology. The reduction of channel length to such value has significantly reduced power dissipation compared to [4]. In their work, they concentrated on power consumption at the expense of chip area which will affect in consequence high density detector arrays implementation and image resolution as mentioned earlier. Binkley *et al.* [2] also used large W/L CMOS values, ranging from 1200/0.8 m shape factor to 4800/0.8 m. They used the regulated cascode preamplifier architecture. It contains 1-pF feedback capacitance in parallel with l-MΩ feedback resistor (implemented by a MOSFET in the deep-ohmic region); this feedback was used to minimize the cascode input resistance while simultaneously maximizing the cascode output resistance which will increase dc loop gain. They replaced the input PMOS used in their previous work [4] with (NMOS. The change resulted in lower input white-noise voltage since n-type metal-oxide-semiconductor (NMOS) has higher transconductance. Their proposed circuit is optimal for wideband applications.

Pratte *et al.* [1] introduced CSA using 180 CMOS technology. They really introduced a circuit model that reduced power consumption to less than 10% compared to work in [2]. They proposed 2 circuit models. The power dissipated in the first design was 5 mW, and the second design was only 1 mW that led to an increase in the number of stacked detectors on a single chip. But in their design, they did not mention the value of W/L

ratio they had used in order to judge their design efficiency. The second issue is that the resulted ENC was very large; it recorded 1187 Electrons-rms at the peaking time compared to our 43 electrons-rms value. This reduces image quality, especially for high resolution imaging applications.

Ratti *et al.* [7] have introduced CSA circuit with 65 nm technology. They aimed to use this preamplifier in a circuit used as a time over threshold counter (TOT counter). In their research, they built a circuit based on folded cascode architecture with a regulated cascode load to boost impedance seen at the amplifier output. They used NMOS at the circuit input. A huge reduction in chip area was achieved. Many thanks to the reduction of MOSFET channel length. An equivalent noise charge of 120 e-rms. The power dissipation of the cascode CSA was 3.6 μW, which is slightly less than our 4 μW power dissipation and that is because they used the CSA in a 1.2 V power plane but we use 1.8 V. Using such a lower voltage value will be at the expense of the gain of the CSA.

To sum up, many research works have been introduced on CSA. We discussed the pros and cons of some recent works. Most of them made their designs with different topologies and had many differences, but all agreed on having CMOS channel length reduction. CMOS regime is the keyword of reducing power dissipation and reduction of ENC and this is what our paper depends on.

3. PRELIMINARIES

When designing a low noise charge amplifier, several design considerations should be taken into account: Thermal noise capacitive match, W/L ratio, and other parameters that we will state later in this paper [1], [3]. So, in this section, the models of ENC and Transconductance for a charge sensitive preamplifier are explained showing their controlling parameters.

3.1. Equivalent noise charge

The equivalent noise charge (ENC) is the traditional measurement term for describing the resolution of charge sensitive front-end electronics. The ENC corresponds to the charge that must be delivered to the front-end in order to have a unity signal-to-noise ratio [1], [4], [6] and it is measured in rms electrons. In (1) indicates the classical ENC model for a charge sensitive preamplifier [1]:

$$ENC^2 = (C_{det} + C_{gs})^2 \cdot \left(\frac{4KT\gamma}{g_m} + \frac{K_f}{C_{gs}} \right) \quad (1)$$

The first term i.e. $(C_{det} + C_{gs})$ is due to the input MOSFET thermal noise, and the second term $(4KT\gamma/g_m + K_f/C_{gs})$ is the input MOSFET $1/f$ noise. C_{det} is the detector capacitance and C_{gs} is the MOSFET gate to source capacitance, g_m is transconductance of source input MOSFET. K is the Boltzmann's constant, K_f is flicker noise coefficient of the MOSFET, T is temperature in kelvin, γ is the coefficient of thermal noise for the input MOSFET. And we should keep in mind that capacitance matching between C_{det} and C_{gs} is needed. Figure 2 shows parasitic capacitances in NMOS and its parasitic capacitances representation on MOS geometry side by side with detector capacitances. As we will show later in the proposed circuit, the input MOSFET is NMOS. NMOS has a higher transconductance when comparing with PMOS [8]. This will decrease ENC and reduce the noise of the received signal.

There are many variables that contribute to the ENC of a MOSFET that are technology-dependent and user-defined. A designer usually has only control of the W/L ratio of the transistor and therefore it is limited in the noise optimization process [22], [23]. The only parameters in (1) that the designer has control over is C_{gs} an optimum value for C_{gs} must exist since increasing or decreasing C_{gs} can mean large changes in the ENC. Later we will show Equations that define C_{gs} in terms of W and L in order to visualize how a change in W and L will affect each term [24], [25]. The noise of any MOSFET has 3 types: the white series noise, the white parallel noise, and the frequency noise. Figure 3 shows noise and capacitances models for CSA noise and capacitance are key parameters for CSA which gives an indication of how much this CSA is good when a certain technology is chosen, the only way to control the behavior of a component in the circuit is by changing the size of a component which we will do later.

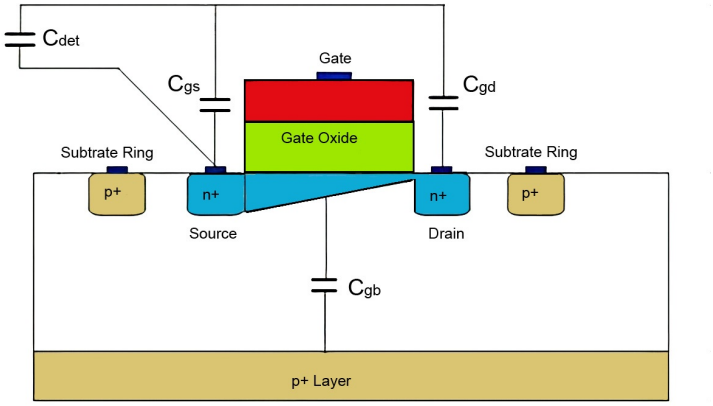

Figure 2. MOSFET overview with parasitic capacitances

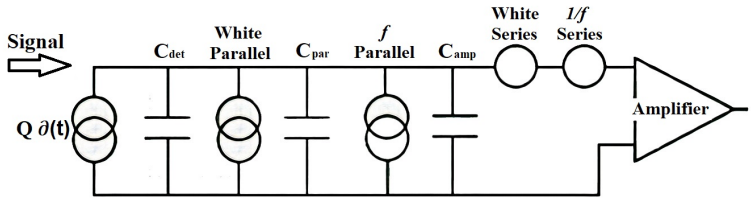

Figure 3. Noise and capacitance model for CSA

Now the general formula for ENC for any MOSFET is (2):

$$ENC = \sqrt{ENC_s^2 + ENC_p^2 + ENC_f^2} \tag{2}$$

where ENC_s is measurement for series noise and ENC_p is measurement for parallel noise and ENC_f is measurement for frequency noise [1]:

$$ENC_f^2 = C_{in}^2 \frac{K_{FN}}{C_{ox} W L} \pi A_f \tag{3}$$

$$ENC_p^2 = \frac{2KTA_p\tau_p}{R_{eq}} \tag{4}$$

$$ENC_s^2 = \frac{2KTA_sC_{in}^2}{\tau_p}\left(\frac{\gamma}{g_{mn}} + R_p\right) \tag{5}$$

where $A_{f,p,s}$ are the form factors of input the shaping function, C_{in} is total capacitance at the CSA input, T_P is the shaping function peaking time, K_{FN} is the NMOS flicker noise coefficient, R_P is the parasitic resistance in series with each transistor electrode, C_{ox} is the gate oxide capacitance per unit area, W is the width and L is the length of the input NMOS, and R_{EQ} is the equivalent resistance of the rest reading out system [1], [7].

3.2. Transconductance

One of the important parameters of a FET is the transconductance g_m. The formula for the g_m is:

$$g_m = \sqrt{2 \cdot \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} \cdot I_{DS}} \tag{6}$$

where I_{DS} is the drain to source current, and μ_{eff} is the charge-carrier effective mobility [20], [21].

For strong inversion mode:

$$C_{gs} = \frac{2}{3} C_{ox} \cdot WL \tag{7}$$

Now, solving the (7) for C_{ox} to find the relation between L and g_m produces the (8).

$$g_m = \sqrt{\frac{3\mu_N \cdot C_{gs} \cdot I_D}{L^2}} \tag{8}$$

If we look for the (8), we can figure out that transconductance is inversely proportional to the channel length. So reduction of technology means larger transconductance and conductance are achieved.

4. SCALING

The concept of scaling has evolved with the revolution of sub 100 nm technology. It is worth indicating that by scaling, we mean that the effective channel length is reduced by a scale of S. However, scaling can be challenging because when we reduce channel length by a scale S (for ¡ 100 nm technology) some parameters have to be changed to preserve currents and voltage relations in MOSFET, as described later. In addition, some nonlinearities will appear and should be taken into consideration [26].

In *constant-voltage scaling*, all dimension of the MOSFET are reduced by a factor of S [23], [24]. The power supply voltage will not be changed. The doping densities N_A and N_D must be increased by a factor of S^2 in order to preserve the charge-field, as listed in Table 1 [25]. When applying such scaling, the MOSFET parameters will be changed as seen in Table 2 [25].

Table 1. Constant voltage scaling

Quantity	Before scaling	After scaling
Dimensions	W, L, t_{ox}, x_j	Reduced by S
Voltages	V_{DD}, V_T	Remain unchanged
Doping densities	N_A, N_D	Increased by S^2

Table 2. MOSFET parameters before and after scaling

Quantity	Before scaling	After scaling
Channel width	W	$W' = W/S$
Channel length	L	$L' = L/S$
Gate oxide thickness	t_{ox}	$t'_{ox} = t_{ox}/S$
Junction depth	x_i	$x_j = x_i/S$
Oxide capacitance	C_{ox}	$C'_{ox} = S \cdot C_{ox}$
Drain current	I_D	$I'_D = S \cdot I_D$
Threshold voltage	V_{T0}	$V'_{T0} = V_{T0}$
Power supply voltage	V_{DD}	$V'_{DD} = V_{DD}$
Doping densities	N_A & N_D	$N'_A = S^2 \cdot N_A$ & $N'_D = S^2 \cdot N_D$

Now, we will use the scaling concept described and apply it on a 180 nm predesigned CSA [1], [10], [14], and replace all transistors with 45 nm transistors. Here, we are talking about scaling by S = 180/45 = 4. Thus, we will adjust the equations of the preamplifier by considering scaling effects. And we will prove that using 45 nm technology will enhance the gain, the response time, ENC, and the power consumption as well.

5. ANALYSIS

Figure 4 shows a circuit of the CSA that we will apply our analysis and modifications on [1], [3], [4]. This preamplifier is based on modified telescopic cascode topology. The advantage of this topology comes on low power dissipation, with mid-range voltage gain, and lower noise. The Input of the preamplifier is at Q1 which is typically an NMOS. NMOS provides higher transconductance over PMOS which results in minimizing ENC. Transistor Q2 is used as the main current source to produce the desired transconductance in the input transistor [1], [4]. Q7 is used as a feedback resistor as it works in the deep ohmic region. Q7 is in parallel with the feedback capacitor C_F which is necessary to let the CSA work in integration mode [4]. All MOSFETs have W/L = 100 for design symmetry. C_F and C_c both are set to 10 fF.

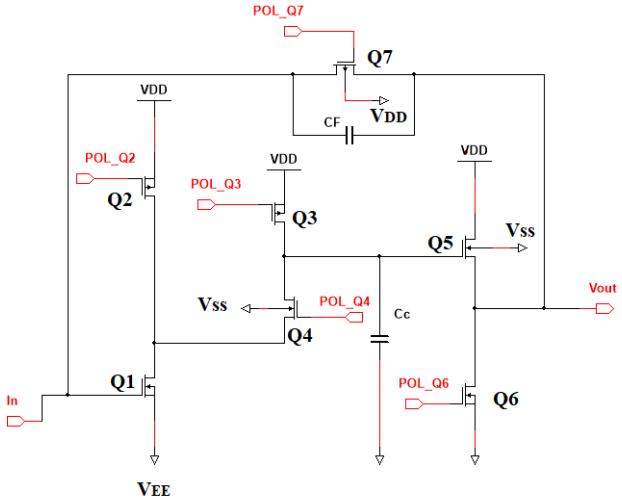

Figure 4. Main CSA circuit

Back to (6), we can note that g_m is controlled by oxide capacitance C_{ox}. Also, g_m is determined by the width of MOSFET and the channel length which in this case equals to 45 nm. Now by considering the scaling factor S, g_m will be scaled by S and this will be useful and leads to a more efficient design.

Now substituting $L = L/S$, $W = W/S$, $C_{ox} = S.C_{ox}$, $I_D = S \cdot I_D$ in in (1) and (8) yields to $C_{gs} = C_{gs}/S$

$$\begin{aligned} g'_m &= \sqrt{2 \cdot \mu_{eff} \cdot S \cdot C_{ox} \frac{W/S}{L/S} S \cdot I_{DS}} \\ g'_m &= \sqrt{2 \cdot \mu_{eff} \cdot S^2 \cdot C_{ox} \frac{W}{L} \cdot I_{DS}} \\ g'_m &= S\sqrt{2 \cdot \mu_{eff} \cdot C_{ox} \frac{W}{L} \cdot I_{DS}} \\ g'_m &= S \cdot g_m \end{aligned} \tag{9}$$

Also,

$$\begin{aligned} g'_m &= \sqrt{\frac{3\mu_N \left(C_{gs}/S\right) \cdot S \cdot I_D}{\left(L/S\right)^2}} \\ g'_m &= \sqrt{\frac{3S^2 \mu_N C_{gs} I_D}{L^2}} \end{aligned} \tag{10}$$

This leads also to (9). This proofs that current conductance (charges conductance) through the MOSFET channel length will be increased by factor S, consequently decrementing the signal distortion transmitted through MOSFET. Now substituting in (11):

$$\begin{aligned} ENC'^2 &= \left(\frac{C_{det} + C_{gs}}{S}\right)^2 \left(\frac{4KT\gamma}{Sg_m} + \frac{K_f}{C_{gs}/S}\right) \\ &= \frac{\left(C_{det} + C_{gs}\right)^2}{S^3} \cdot \frac{4KT\gamma}{g_m} + \frac{\left(C_{dt} + C_{gs}\right)^2}{S} \cdot \frac{K_f}{C_{gs}} \end{aligned} \tag{11}$$

Note that mathematically the new ENC^2 is reduced by S^3 for the first term and by S for the second term, which really makes a great enhancement on detection accuracy over 180-Nano detectors [1]. We will see in the next section the simulation results that will assure our enhancement shown in calculations.

6. SIMULATION RESULTS

Simulation of our proposed enhanced design was conducted by using PSpice circuit simulator and the results was extracted to Matlab to draw graphs. Simulation results showed that ENC and signal-to-noise ratios have been more stable and have minimum distortions.

6.1. Simulation parameters

In our simulation, we used W/L ratio equal to 100. The size of the input device was optimized for the derivative of a third-order semi-Gaussian shaping function [1], [2], [12], [15]. Bipolar CR^2–RC^2 shaper was used with a peaking time of 70 ns and 1.8-V power and ground plane. The following Table 3 presents CR-RC, CR^2–RC^2 and the derivative of a 3rd order semi-Gaussian shaping function for 70 ns peaking time [1].

Table 3. Shaping form factors

Form factors	CR-RC	CR^2-RC^2	Semi-Gaussian
A_f	1.18	1.55	1.61
A_S	1.85	2.27	2.15
A_P	1.85	1.45	2.10

Detector module has a capacitance of 50 fF and biased at 350 V with a Gain that is set to 55. Feedback capacitance C_F was set to 10 fF. An input signal is injected in the circuit on the form of a test pulse applied to a characterized 15 fF capacitor for the main circuit.

6.2. Voltage transfer characteristics (Gain)

Simulation results have shown that our proposed circuit has deduced a gain of 3.1 mV/fC, with a maximum output swing of 100 mV, as seen in Figure 5. An input signal approximately is injected in the circuit on the form of a test pulse applied to a characterized 15 fF capacitor for the main circuit. In obtaining this result, the input capacitance was set to 50 fF.

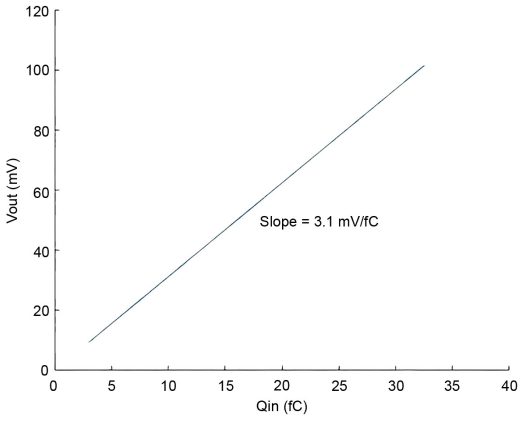

Figure 5. Gain of CSA circuit

6.3. ENC measurement

Figure 6 shows ENC for the peaking time range from 60 to 200 ns. ENC is measured as a function of different input capacitances. Simulation results have shown that ENC was reduced by more than 96% using 45 nm technology compared to 180 nm technology [1]. Figure 7 shows the ENC with $ENC_{S,P,1/f}$ for peaking time from 10 ns to 10 s at input capacitance = 20 fF. The resulting ENC showed minimum value of 43 electrons-rms at peaking time = 77 ns. This result shows a great enhancement over 180 nm technology that recorded 1117 electrons-rms at 100 ns [1].

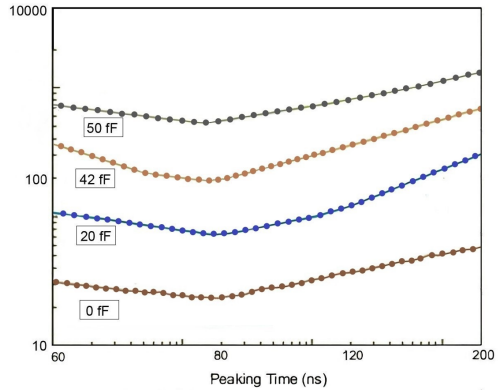

Figure 6. ENC vs peaking time for different input capacitances

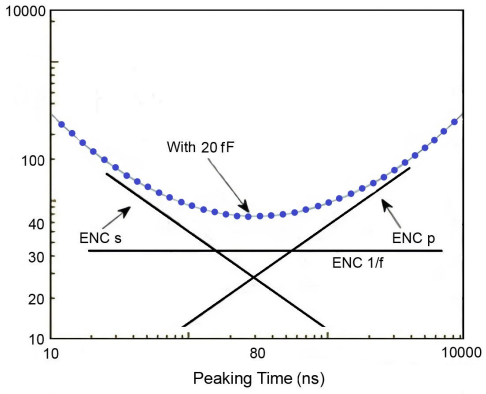

Figure 7. ENC vs peaking time

6.4. Power dissipation measurement

Figure 8 shows the power consumed by three different technologies for different measured ENC values. The figure clearly shows that when reducing the channel length, power dissipation is noticeably reduced by a good value.

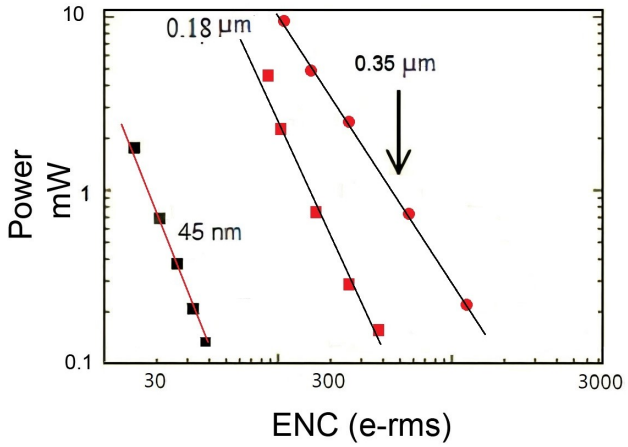

Figure 8. ENC VS power dissipation

6.5. Comparison with other previous works

Table 4 shows a comparison of our proposed scheme with other previous designs using main CSA different parameters. The common thing among them that all were developed for LSO/APD for PET systems. Also, all were implemented using CMOS technology except the first were developed using discrete MOSFET, not complementary. The comparison is represented in the shape of a historic timeline to show advances made with respect to time.

Table 4. Comparisons with different technologies

CSA Parameters	Schmitt *et al.* [6]	Binkley *et al.* [4]	Paulus *et al.* [3]	Binkley *et al.* [2]	Pratte *et al.* [1]	Ratti *et al.* [7]	Our work
Used echnology	Discrete MOSFET	2 μm CMOS	2 μm CMOS	800 nm CMOS	180 nm CMOS	65 nm CMOS	45 nm CMOS
e_n (nV/Hz$^{1/2}$)	0.9	1.6	1.1	0.65	0.57	N/A	0.41
Current (mA)	20	5	10	2	0.6	0.003	0.003
Time resolution (FWHM)	0.9 ns	9.2 ns	1.57 ns	1.15 ns	2.49 ns	N/A	82 ps
Rise time (using 0 pF) (ns)	5	22	7	6	9	17	5
Power (mW)	300	38	50	10	1	0.0036	0.004

- Technology used all CSA-based PET applications use CMOS as mentioned before and we notice that as time passes MOSFETS are minimizing their channel length. Our proposed circuit uses the 45 nm MOSFET, which is considered one of the minimal channel length currently used in such circuits.
- The noise spectral density is preserved between 0.41 and 1.6 in all of the above designs. It is known that the ENC is directly proportional to the spectral noise density e_n. In our work, this parameter is reduced by 25% compared to 180 nm technology [1]. This is due to higher transconductance in shorter channel MOSFETS.
- The feeding current is reduced with recent designs. Our 3 A circuit is very suitable for high dense applications.
- Time resolution full width at half maximum (FWHM) was reduced massively by more than 95% compared to [1] which is breaking through a constant fraction discriminator and a CR-RC Timing Filter Amplifier connected directly to CSA output to measure time resolution.
- Rise time is reduced by 45% compared to [1] which results in a faster responsive amplifier circuit.
- Power consumption is decreased due to the reduced channel length and that's why all most recent works are competing in shrinking CMOS used in CSA design. Our power reduction breakthrough will pave the road for higher dense – higher-resolution medical imaging applications.

7. CONCLUSION AND FUTURE WORK

This paper has introduced an efficient design of a low noise charge amplifier using 45 nm technology, which is made for the first time in such circuits. The proposed scaling technology with the amplifier design improves the efficiency in terms of limiting noise effect while maintaining amplification value. This will enhance the quality of received images in terms of resolution and accuracy in many PET and wireless applications. Simulation results proved that direction toward deep submicron CMOS circuit by shrinking transistors size is a powerful trend that leads to reduce noise, power consumption, ENC, noise spectral density, and time resolution. We have made our comparison mainly on 180 nm technology and the results show a great enhancement in ENC value by more than 95% and lowering power consumption by more than 95%. In addition, our comparisons consider other older technologies such as 350 nm, and 800 nm. Future work would concentrate on optimizing response time and frequency response. This would be a concrete step towards more interesting research lines. Moreover, our analysis on operating Q1 MOSFET assumed strong inversion operation mode, while it really works in a moderate-to-strong inversion region resulting in shifting the minimum ENC value at 70 ns peaking time to 77 ns. Future studies should take this into consideration in order to enhance results and their accuracy. In addition, researchers may test our proposed design's performance with Monte-Carlo simulation for the ENC variation for extra analysis.

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