2019

Sliding Mode Control Strategy for Three-Phase Three-Level T-Type Shunt Active Power Filters

Hasan Komurcugil

Sertac Bayhan

Samet Biricik

Sliding Mode Control Strategy for Three-Phase Three-Level T-Type Shunt Active Power Filters

Hasan Komurcugil[1], Sertac Bayhan[2] and Samet Biricik[3,4]

[1] Department of Computer Engineering, Eastern Mediterranean University, Famagusta, Via Mersin 10, Turkey
[2] Qatar Environment and Energy Research Institute, Doha, Qatar
[3] Department of Electrical and Electronic Engineering, European University of Lefke, Lefke, Via Mersin 10, Turkey
[4] School of Electrical and Electronic Engineering, Technological University Dublin, Dublin, Ireland

hasan.komurcugil@emu.edu.tr, sbayhan@hbku.edu.qa, sbiricik@eul.edu.tr

Abstract—In this paper, a sliding mode control (SMC) strategy is proposed for three-phase three-level T-type shunt active power filters (SAPF). The proposed control strategy has the ability to balance the capacitor voltages with respect to the neutral-point. The proposed SMC strategy is formulated in the natural frame which eliminates *abc/dq* transformation and two PI controllers compared to the design in the *dq* frame. In natural frame, only one PI controller is needed to generate the amplitude of grid current reference. The output of the PI controller is multiplied by the unity sinusoidal waveforms, obtained from the grid voltages, so as to obtain the grid current references. The filter current references are obtained by subtracting the measured load currents from grid current references. The performance of the proposed control method is investigated by simulation study during steady-state and transients caused by load change. It is shown that the grid currents are almost sinusoidal with small THD, grid currents and dc-link voltage track their references and capacitor voltages are balanced with respect to the neutral-point.

Keywords—Three-level T-type shunt active power filter, proportional-integral control (PI), sliding mode control.

I. INTRODUCTION

Due to the rapidly growing use of power-electronics devices in domestic, industrial and commercial equipment, the harmonic current distortion on the grid has increased considerably in recent years. It is well known that the distorted grid currents cause voltage drops on grid network impedances which may lead to unbalanced conditions. Distorted grid currents can also cause poor power factor, increase heating losses, and affect other loads connected at the point of common coupling (PCC). Therefore, in order to restrict the current harmonics injected into the grid and keep them below specified limits, standard regulation such as IEEE-519 is published [1].

Although conventional passive filters can be employed for compensating the undesired harmonics, they have many drawbacks such as resonance, fixed compensation ability, and large size. In contrast, shunt active power filters (SAPFs) are widely used for compensating the undesired current harmonics [2]. When a SAPF is connected to the PCC, it injects compensating currents having the same amplitude and opposite phase to those of the load current harmonics so as to obtain sinusoidal grid currents in phase with the grid voltages. In order to achieve this, the SAPF should be controlled by an appropriate control strategy which possesses several features such as fast dynamic response, good current tracking capability, robustness to parameter variations, low total harmonic distortion (THD) in the grid currents, and good dc bus voltage regulation. Generally, a control strategy consists of three parts, namely: i) generation of the reference compensating current; ii) current-control of the voltage-source PWM converter, and iii) control of the dc bus voltage. Generation of the reference compensating current plays an important role that affects the filtering performance since any inaccurate phase and magnitude of reference compensating currents result in degradation in the compensation process.

In the existing SAPF topologies, the standard two-level inverter is the most preferred inverter topology. However, the performance of two-level inverter is degraded at medium and high voltages. Nowadays, multilevel inverters are very popular in high-power and medium-voltage applications due to their attractive features such as high efficiency, less losses, low waveform distortion and good performance at low switching frequency. The increased number of levels in the inverter yields a staircase output voltage waveform which reduces the harmonic distortion. One of the popular multilevel inverter topologies is the neutral point clamped (NPC) topology [3]. Various control strategies have been proposed for SAPFs which employ the NPC topology [4]-[10]. These control approaches offer various advantages and disadvantages related to the control objectives mentioned above.

In [11], it is shown that the three-level T-type converter provides better efficiency than other multilevel converter topologies up to the medium switching frequency range. Also, the T-type converter topology has a small part count compared to three-level NPC topology in. Comparing NPC-type and T-type converters, one can see that both topologies employ four IGBTs in one leg. However, the NPC converters require additional two clamping diodes per converter leg for clamping the neutral point to positive or negative dc voltages. In T-type converters clamping is achieved by using an active bidirectional switching device connected between the midpoint of each leg and midpoint of series connected dc-link capacitors. Therefore, the T-type converters do not require clamping diodes at all. That's why T-type converters have less

conduction losses compared with NPC-type converters [12]. However, both NPC and T-type topologies suffer from capacitor voltage imbalance.

Recently, three-level T-type SAPFs are proposed to increase efficiency [13]-[16]. In [13], a phase separated control is introduced which eliminates the influence of DC-link voltage unbalance. In [14], a different capacitor voltage balancing strategy is proposed. The authors in [15] proposed to use fast Fourier transform (FFT), instantaneous reactive power method and synchronous reference frame techniques in generating the filter reference currents. In [16], the T-type inverter is connected to the point of common coupling (PCC) with the LCL filter. Since the T-type converter topology has emerged recently, there is no sufficient study investigating the performance of the T-type SAPF under various control methods such the SMC.

In this study, SMC of three-phase three-level T-type SAPF is proposed in the natural frame. The main advantages of SMC include fast dynamic response, high robustness against disturbances and variations in the system parameters, and implementation simplicity. The SMC with these features is recognized as one of the popular and powerful control tools in a wide range of applications such as uninterruptible power supplies (UPS) [17], DC-DC converters [18], grid-connected inverters [19], and PWM rectifiers [20]. The proposed SMC strategy can compensate the grid current harmonics, regulate the dc-link voltage and eliminate the imbalance existing in the capacitor voltages. Also, it offers implementation simplicity, robustness, and fast dynamic response.

II. T-TYPE SAPF AND ITS OPERATING STATES

Fig. 1 shows a three-phase three-level T-type SAPF. It consists of four switches per leg. It can be seen that the three-level T-type SAPF is an extended version of the standard two-level voltage source inverter with an additional active bidirectional switch which consists of two anti-series insulated gate bipolar transistors (IGBTs) connected between each phase leg and the capacitor's midpoint.
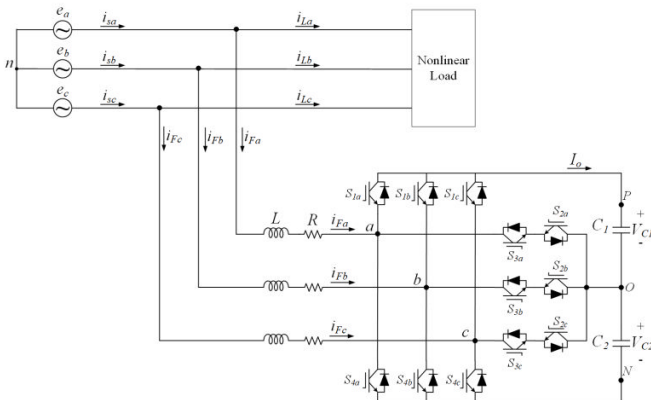

Fig. 1. Three-phase three-level T-type shunt active power filter.

Considering the combination of switching states, the SAPF can generate three different pole voltages v_{kO} ($k=a, b, c$).

These voltages occur when the midpoint of each leg is connected to positive (P), neutral (O) and negative (N) points. The operating states, switching states and generated pole voltages are shown in Table I. Clearly when the switches S_{k1} and S_{k2} are ON, and S_{k3} and S_{k4} are OFF, the SAPF operates in the P state generating $v_{kO} = (V_{C1} + V_{C2})/2 = V_{dc}/2$. When S_{k2} and S_{k3} are ON and S_{k1} and S_{k4} are OFF, the SAPF operates in the O state generating 0V. Finally, when S_{k1} and S_{k2} are OFF and S_{k3} and S_{k4} are ON, the SAPF operates in the N state and generates $v_{kO} = -V_{dc}/2$. Hence, it can be seen from the generated voltage levels that the T-type SAPF in Fig. 1 is able to generate a three-level voltage waveform. Similar to the traditional two-level SAPFs, the inductance L connected between the grid and midpoint of each phase achieves boost operation such that the dc-link voltage is always greater than the grid voltage.

TABLE I
OPERATING STATES, SWITCHING STATES AND POLE VOLTAGES

Operating State	S_{k1}	S_{k2}	S_{k3}	S_{k4}	v_{kO}
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

III. MATHEMATICAL MODELING OF T-TYPE SAPF

The differential equation of the SAPF can be written as

$$\mathbf{e} = L\frac{d\mathbf{i}}{dt} + R\mathbf{i} + \mathbf{v} \tag{1}$$

where R is the resistance of inductor L and

$$\mathbf{e} = \begin{bmatrix} e_a & e_b & e_c \end{bmatrix}^T, \ \mathbf{i} = \begin{bmatrix} i_{Fa} & i_{Fb} & i_{Fc} \end{bmatrix}^T, \ \mathbf{v} = \begin{bmatrix} v_{an} & v_{bn} & v_{cn} \end{bmatrix}^T \tag{2}$$

The grid voltages are defined as

$$e_a = E_m \cos(\omega t) \tag{3}$$

$$e_b = E_m \cos(\omega t - 2\pi/3) \tag{4}$$

$$e_c = E_m \cos(\omega t + 2\pi/3) \tag{5}$$

where E_m denotes the amplitude. The pole voltages are dependent on the switching states. It is worth noting that the dc-link capacitors are assumed to be identical ($C_1 = C_2$). In this case, the voltage across each capacitor is half of the dc-link voltage ($V_{C1} = V_{C2} = V_{dc}/2$). The control strategy of a SAPF has two objectives. The first objective is to achieve sinusoidal grid currents which are in phase with the corresponding grid voltages. The second objective is the regulation of the output voltage at the desired level. In order to achieve the first objective, an inner current loop is required which forces the grid currents to track their references.

IV. SLIDING MODE CONTROL OF T-TYPE SAPF

As mentioned in the previous section, one of the control objectives in a SAPF is to regulate dc-link voltage (V_{dc}) at the

Authorized licensed use limited to: Technological University Dublin. Downloaded on December 07,2021 at 10:01:46 UTC from IEEE Xplore. Restrictions apply.

desired level. It is well known that the PI controller exhibits good dynamic and steady-state performances for dc quantities. Hence, this control objective can be achieved by using a PI controller which generates the reference amplitude of the grid currents by processing the dc-link voltage error ($V_{dc}^* - V_{dc}$). In this case, the reference amplitude of the grid currents can be generated as

$$I_s^*(t) = K_p(V_{dc}^* - V_{dc}) + K_i \int (V_{dc}^* - V_{dc})dt \qquad (6)$$

where V_{dc}^* is the reference of V_{dc}, K_p and K_i are the proportional and integral gains, respectively. Equation (6) satisfies the dc-link voltage regulation provided that the line currents track their references.

In order to obtain the grid current references, the reference amplitude $I_s^*(t)$ should be multiplied with the sinusoidal waveform templates obtained from the grid voltages in (3)-(5) as follows

$$i_{sa}^* = I_s^*(t)\cos(\omega t) \qquad (7)$$

$$i_{sb}^* = I_s^*(t)\cos(\omega t - 2\pi/3) \qquad (8)$$

$$i_{sc}^* = I_s^*(t)\cos(\omega t + 2\pi/3) \qquad (9)$$

However, in order to control the SAPF currents, their references are needed. These references are obtained by subtracting the measured load currents from the reference grid currents in (7)-(9) as follows

$$i_{Fa}^* = i_{sa}^* - i_{La} + K_c(V_{C1} - V_{C2}) \qquad (10)$$

$$i_{Fb}^* = i_{sb}^* - i_{Lb} + K_c(V_{C1} - V_{C2}) \qquad (11)$$

$$i_{Fc}^* = i_{sc}^* - i_{Lc} + K_c(V_{C1} - V_{C2}) \qquad (12)$$

In (10)-(12), the term $K_c(V_{C1} - V_{C2})$ is needed to eliminate the imbalance which exists in the capacitor voltages. The gain K_c can be used to adjust the dynamics of the compensation, and it should satisfy $K_c > 0$ for a stable operation [21].

In this study, the SAPF current control is performed by using SMC. Now, let the sliding surface functions are defined as

$$\sigma_a = i_{Fa} - i_{Fa}^* \qquad (13)$$

$$\sigma_b = i_{Fb} - i_{Fb}^* \qquad (14)$$

$$\sigma_c = i_{Fc} - i_{Fc}^* \qquad (15)$$

The sliding mode occurs if the existence conditions are satisfied. Generally, existence conditions are derived from the sliding surface function (σ_k) and its derivative $\dot{\sigma}_k$ which should have opposite signs around the sliding line. The sliding mode is stable if the following condition holds

$$\sigma_k \dot{\sigma}_k < 0 \qquad (16)$$

Now, let us show that the condition in (16) can be satisfied for phase A. Substituting the derivative of (13) into (16) yields

$$\sigma_a \left(\frac{di_{Fa}}{dt} - \frac{di_{Fa}^*}{dt} \right) < 0 \qquad (17)$$

Assuming that $I_s^*(t)$, V_{C1} and V_{C2} are constant in the steady-state, the derivative of (10) is written as

$$\frac{di_{Fa}^*}{dt} = -\omega I_s^*(t)\sin(\omega t) \qquad (18)$$

Substituting (18) and the expression obtained from (1) into (16) gives

$$\frac{\sigma_a}{L}\left(\sqrt{(E_m^2 + (\omega L I_s^*(t))^2} \cos(\omega t + \theta) - v_{aO} \right) < 0 \qquad (19)$$

where phase shift is given by

$$\theta = \tan^{-1}\left(\frac{-\omega L I_s^*(t)}{E_m} \right) \qquad (20)$$

The inductor resistance (R) is neglected in the derivation of (19). Clearly, (19) can be modified as

$$\sigma_a \sqrt{(E_m^2 + (\omega L I_s^*(t))^2} \cos(\omega t + \theta) < \sigma_a v_{aO} \qquad (21)$$

Hence, if v_{aO} is large enough, (21) is always satisfied. Since the pole voltage v_{aO} contains V_{dc} as shown in Table I, then the stability can be dictated either by selecting large V_{dc} values or by selecting small E_m, and L values. The stability of the other phases can be obtained similarly.

V. SIMULATION RESULTS

The effectiveness and correct operation of the proposed control strategy has been verified by simulations using Matlab/Simulink. The block diagram of the proposed control method and the PWM generation scheme are shown in Fig. 2(a) and (b), respectively. The PWM signals are generated by comparing the sliding surface functions with the level shifted triangular carrier signals which are shown as "Car1" and "Car2" in Fig. 2(b). The system and control parameters used in the simulation studies are given in Table II.
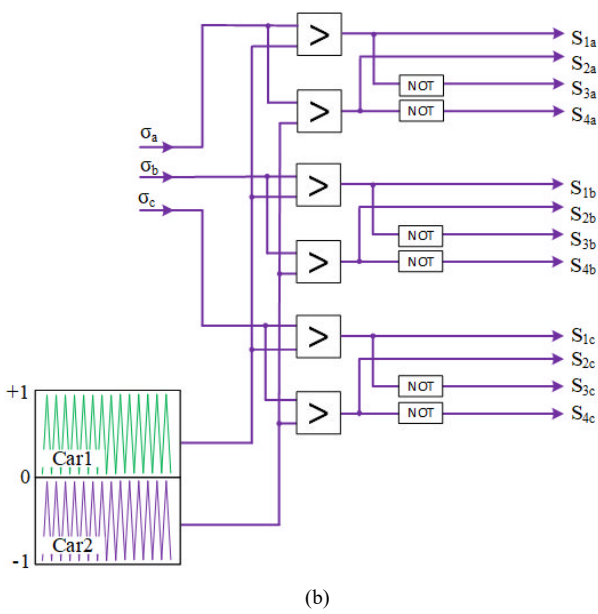

(a)

4940

(b)
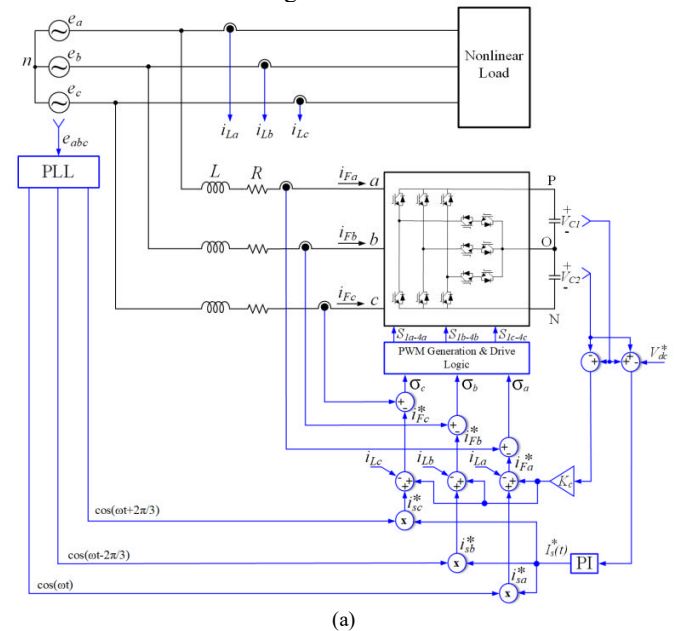
Fig. 2. Block diagram of the (a) proposed control method, (b) PWM generation scheme.

TABLE II
SYSTEM AND CONTROL PARAMETERS

Description and Symbol	Value
Grid voltage amplitude, E_m	$230\sqrt{2}$ V
Inductance, L	0.5mH
Inductor resistance, R	0.2Ω
DC capacitors, $C_1 = C_2$	2000μF
Load$_1$ (parallel RC)	R=20Ω, C=20μF
Load$_2$ (parallel RC)	R=40Ω, C=20μF
DC-link voltage reference, V_{dc}^*	800V
PI gains, K_p and K_i	1 , 100
Imbalance compensation gain, K_c	0.1
Switching frequency, f_{sw}	2.5kHz

Fig. 3 shows the steady-state responses of grid voltages (e_a, e_b, e_c), nonlinear load currents (i_{La}, i_{Lb}, i_{Lc}), filter currents (i_{Fa}, i_{Fb}, i_{Fc}), grid currents (i_{sa}, i_{sb}, i_{sc}), capacitor voltages (V_{C1}, V_{C2}), and dc-link voltage (V_{dc}) under a nonlinear load. It can be seen from Fig. 3(b) that the nonlinear load draws highly distorted currents whose total harmonic distortion is 14.5%. Based on the proposed control strategy, the SAPF produces the currents (see Fig. 3(c)) so that the grid currents (see Fig. 3(d)) become sinusoidal, as much as possible, with low THD and in phase with the grid voltages shown in Fig. 3(a). The THD of grid currents is computed to be 2.5%. The performance of the SAPF is clear when one considers the THD improvement from 14.5% to 2.5%. On the other hand, it can be observed that the capacitor voltages converge to the half of the dc-link voltage. Moreover, no imbalance exists in the capacitor voltages shown in Fig. 3(e). The dc-link voltage shown in Fig. 3(f) is regulated at

$V_{dc}^* = 800$V which shows that the proposed controller achieves its control objective successfully.
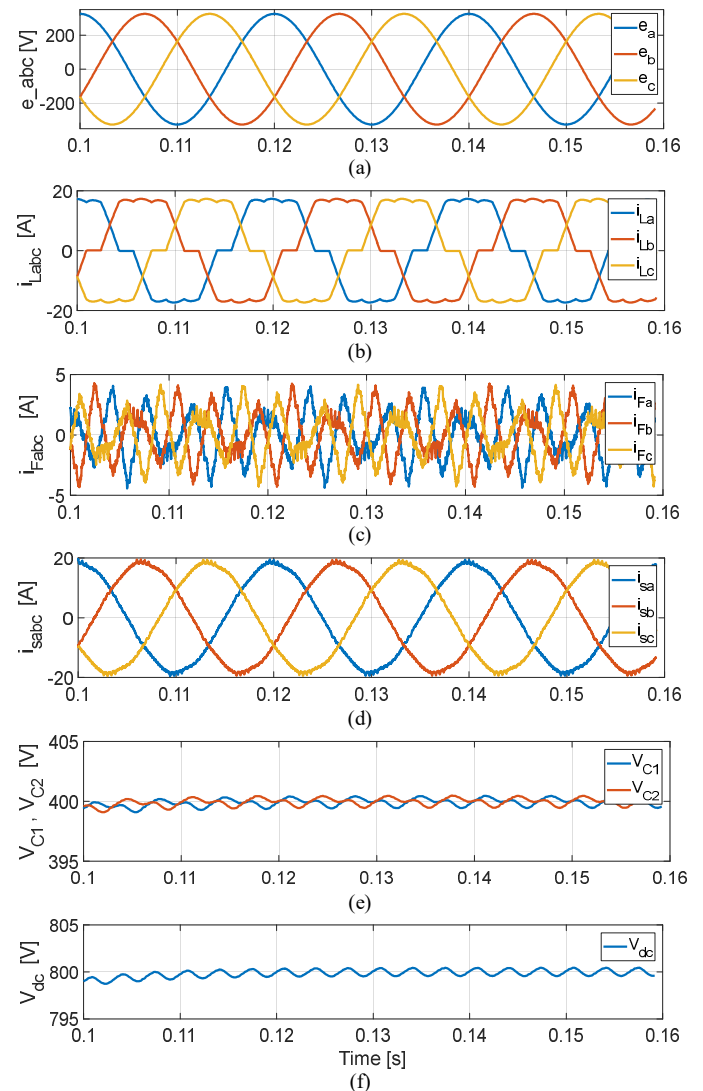

Fig. 3. Steady-state responses under nonlinear load: (a) Grid voltages, (b) Load currents, (c) Filter currents, (d) Grid currents, (e) Capacitor voltages, and (f) dc-link voltage.
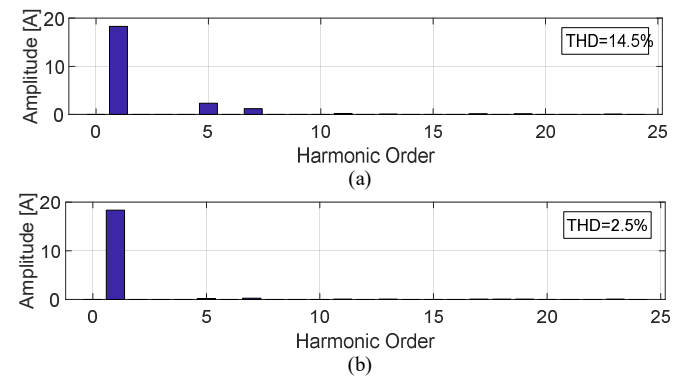

Fig. 4. Harmonic spectrums of load and grid currents of phase A in Fig. 3: (a) Load current, (b) Grid current.

4941

Fig. 4 shows the computed spectrums of load and grid currents for phase A which corresponds to the results in Fig. 3. The THDs of load and grid currents are 14.5% and 2.5%, respectively. This improvement in THD is due to the compensation of 5th and 7th harmonics existing in the load current.
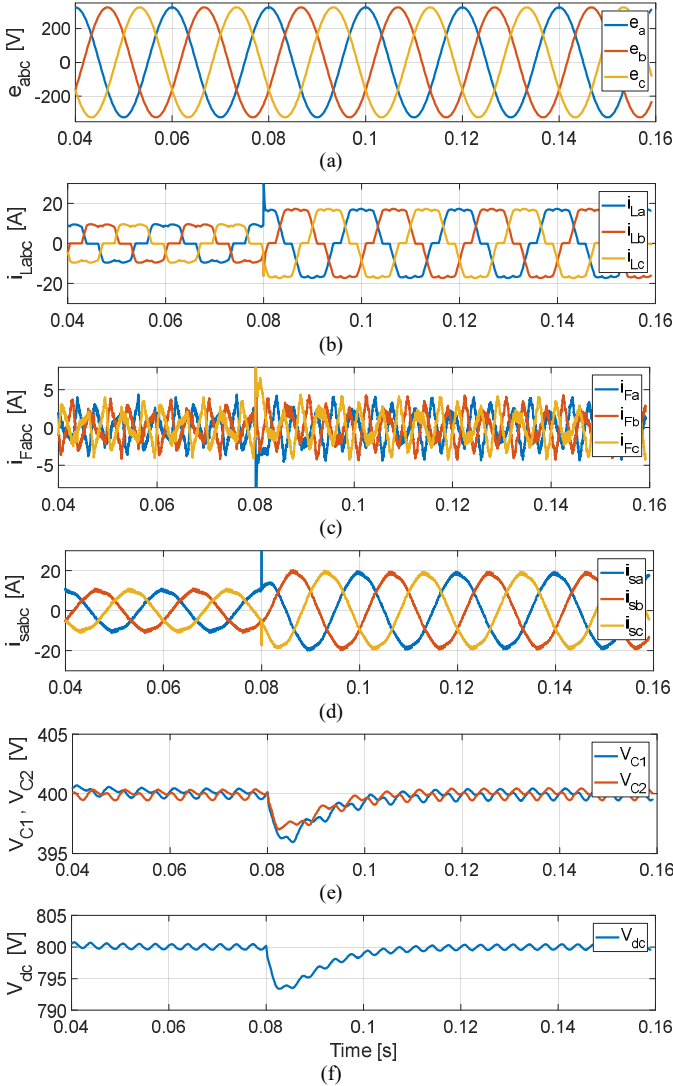

Fig. 5. Dynamic responses when load$_2$ is connected in parallel with load$_1$: (a) Grid voltages, (b) Load currents, (c) Filter currents, (d) Grid currents, (e) Capacitor voltages, and (f) dc-link voltage.

Fig. 5 shows the dynamic responses of grid voltages, load currents, filter currents, grid currents, capacitor voltages, and dc-link voltage when load$_2$ is suddenly connected in parallel with load$_1$. As shown in Fig. 5(c), the grid currents track their references with a reasonable response. Also, except for the short transition period, the capacitor and dc-link voltage voltages are regulated at $V_{dc}^*/2 = 400V$ and $V_{dc}^* = 800V$ as shown in Figs. 5(e) and 5(f), respectively. It is apparent that the capacitor and dc-link voltage have a slower response than the response of grid currents.
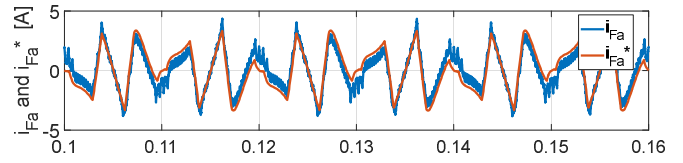

Fig. 6. Steady state responses of phase A filter current and its reference.

Fig. 6 shows the steady-state responses of phase A filter current (i_{Fa}) and its reference (i_{Fa}^*) which corresponds to Fig. 3. It is evident that the actual filter current tracks its reference with a negligibly small error compared to the current level.
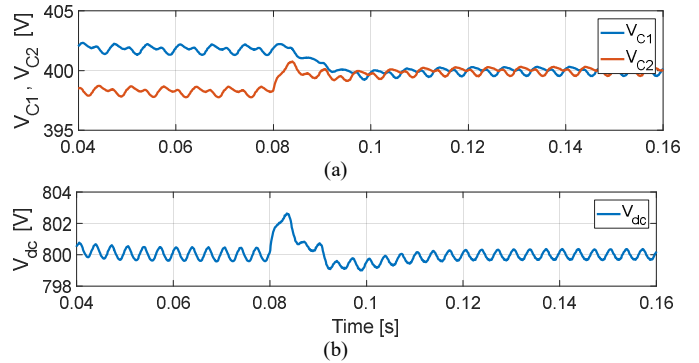

Fig. 7. Dynamic responses of capacitor and dc-link voltage without and with imbalance compensation control: (a) Capacitor voltages, (b) dc-link voltage.

Fig. 7 shows the dynamic responses of capacitor and output voltages obtained with and without imbalance compensation control. The results shown from t=0.04s to t=0.08s are obtained when the imbalance compensation control is disabled. It is obvious that there is an imbalance in the capacitor voltages. However, when the imbalance compensation control is enabled at t=0.08s, the capacitor voltages become balanced as shown in Fig. 7(a). The dc-link voltage, except for the short transition period, is regulated at 800V without and with the imbalance compensation control as shown in Fig. 7(b).

VI. CONCLUSION

A SMC strategy is proposed for three-phase three-level T-type SAPF. The proposed control strategy has the ability to balance the capacitor voltages with respect to the neutral point. The proposed SMC strategy is formulated in the natural frame. The consequence of formulating the controller design in the natural frame is that the *abc/dq* transformation and two PI controllers are eliminated. In the natural frame, only one PI controller is needed to generate the amplitude of grid current reference. The output of the PI controller is multiplied by the unity sinusoidal waveforms, obtained from the grid voltages, so as to obtain the grid current references. The filter current references are obtained by subtracting the measured load currents from grid current references. The performance of the

4942

proposed control method is investigated by simulation study during steady-state and transients caused by load change. It is shown that the grid currents are almost sinusoidal with small THD, grid currents and dc-link voltage track their references, and capacitor voltages are balanced with respect to the neutral point.

REFERENCES

[1]   *IEEE 519 Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Standard, 1993.

[2]   B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960–971, May 1999.

[3]   J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, Jul. 2010.

[4]   B. R. Lin, H. K. Chiang, and K. T. Yang, "Shunt active filter with three-phase four-wire NPC inverter," in Proc. 47th *IEEE International Midwest Symposium on Circuits and Systems*, 2004, pp. 281-284.

[5]   M. Asadi, H. Ebrahimirad, M. S. Mousavi and A. Jalilian, "Sliding mode control of DC-link capacitors voltages of a NPC 4-wire shunt active power filter with selective harmonic extraction method," in Proc. 7th *Power Electronics, Drive Systems & Technologies Conference*, 2016, pp. 273-276.

[6]   E. Pouresmaeil, D. M. Miracle, O. G. Bellmunt, and A. S. Andreu, "Instantaneous active and reactive current control technique of shunt active power filter based on the three-level NPC inverter," *European Trans. Electrical Power*, vol. 21, pp.2007-2022, 2011.

[7]   A. Munduate, E. Figueres, and G. Garcera, "Robust model-following control of a three-level neutral point clamped shunt active filter in the medium voltage range," *Electrical Power and Energy Systems*, vol. 31, pp. 577-588, 2009.

[8]   S. Saad and L. Zellouma, "Fuzzy logic controller for three-level shunt active filter compensating harmonics and reactive power," *Electrical Power Systems Research*, vol .79, pp. 1337-1341, 2009.

[9]   O. Vodyakho and T. Kim, "Shunt active filter based on three-level inverter for three-phase four-wire systems," *IET Power Electronics*, vol. 2, no. 3, pp. 216-226, 2009.

[10] O. Vodyakho and C. C. Mi, "Three-level inverter-based shunt active power filter in three-phase three-wire and four-wire systems," *IEEE Trans Power Electron.*, vol. 24, no. 5, pp. 1350-1363, May 2009.

[11] J. W. Kolar, "High efficiency drive system with 3-level T-type inverter," in Proc. EPE Appl., pp. 1–10, Aug. 2011.

[12] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Power Electron*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[13] Y. Han, M. M. Khan, G. Yao, L. D. Zhou, and C. Chen, "A novel harmonic-free power factor corrector based on T-type APF with adaptive linear neutral network (ADALINE) control," *Simulation Modelling Practice and Theory*, vol. 16, pp. 1215-1238, 2008.

[14] D. Chen, Q. Xu, Y. Hu, and G. Chen, "A DC-link voltage balancing strategy based on controllable neural current injected for T-type three-level active power filter," in Proc. 2nd *Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1-5.

[15] M. J. Chudasama, S. K. Chauhan, P. N. Tekwani and V. Patel, "Simulation as-well-as experimental investigations on T-type NPC topology based three-level shunt active power filter," in Proc. *International Conference on Technological Advancements in Power and Energy*, 2017, pp. 1-6.

[16] T. Adrikowski, D. Bula, and M. Pasko, "Three-phase active power filter with T-NPC type inverter," in Proc. *Progress in Applied Electrical Engineering*, 2018, pp. 1-5.

[17] H. Komurcugil, "Rotating-sliding-line-based sliding-mode control for single-phase UPS inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3719–3726, Oct. 2012.

[18] M. Salimi, J. Soltani, A. Zakipour and N. R. Abjadi, "Hyper-plane sliding mode control of the DC-DC buck/boost converter in continuous and discontinuous conduction modes of operation," *IET Power Electronics*, vol. 8, no. 8, pp. 1473-1482, 2015.

[19] H. Komurcugil, S. Ozdemir, I. Sefa, N. Altin, and O. Kukrer, "Sliding-mode control for single-phase grid-connected LCL-filtered VSI with double-band hysteresis scheme," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 864–873, Feb. 2016.

[20] Y. Yin, J. Liu, J. A. Sanchez, L. Wu, S. Vazquez, J. I. Leon, and L. G. Franquelo, "Observer-based adaptive sliding mode control of NPC converters: an RBF neutral network approach," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3831-3842, April 2019.

[21] S. Biricik and H. Komurcugil, "Three-level hysteresis current control strategy for three-phase four-switch shunt active filters," *IET Power Electronics*, vol. 9, no. 8, pp. 1732-1740, 2016.