2019

Three-Phase Two-Leg T-Type Converter based Active Power Filter

Samet Biricik

Hasan Komurcugil

Mohamed Trabelsi

Three-Phase Two-Leg T-Type Converter based Active Power Filter

Samet Biricik[1,2], Hasan Komurcugil[3], Mohamed Trabelsi[4,5]

[1] Department of Electrical and Electronics Eng., European University of Lefke, Lefke, Northern Cyprus TR-10 Mersin, Turkey
[2] School of Electrical and Electronic Engineering, Technological University Dublin, Dublin, Ireland
[3] Department of Computer Engineering, Eastern Mediterranean University, Famagusta, Northern Cyprus TR-10 Mersin, Turkey
[4] Department of Electronics and Communication Engineering, Kuwait College of Science and Technology, Kuwait
[5] Department of Electrical and Computer Engineering, Texas A&M University at Qatar, Qatar Foundation, Doha, Qatar

sbiricik@eul.edu.tr, hasan.komurcugil@emu.edu.tr, m.trabelsi@kcst.edu.kw

***Abstract*—In this work, a three-phase two-leg T-type active power filter topology is investigated when a three-level hysteresis band current modulation technique is applied. The three-phase two-leg T-type configuration which utilizes eight switching devices together split dc link capacitor banks is able to improve the reliability of the system as well as effectively reduces the power losses. The compensation of the current harmonics at each phase are achieved successfully with the control of phase-a and phase-b. Using this technique, the phase-c is directly connected to the midpoint of the split capacitors, which eliminates the necessity of additional control on the phase-c. The performance of the proposed topology and control method is demonstrated through the simulation results.**

Keywords—Reduced number of switches, T-Type NPC inverter, APF, Hysteresis current control.

I. INTRODUCTION

The continuous advances in the field of power electronics allow the development of new semiconductor devices that meet the trade-off between high switching frequency and power rating, while being available at reasonable prices. These switching devices offer an interesting techno-economic solution for a better quality of the delivered electrical power. However, this quality could be degraded by the nonlinearity characteristics of the switching devices. Frequency analysis of the voltage and current waveforms reveals the presence of harmonic components. Several solutions have been proposed to solve the problem of harmonic pollution in electrical distribution networks. Active power filter (APF) is considered as the most common solution for harmonics conditioning (elimination), due to their capabilities of filtering out both higher and lower order harmonics [1]. An active power filter is mainly an inverter whose role is the reproduction of harmonic components identical to those to be eliminated, but in opposition of phase [2].

It is well known that the number of semiconductor switches such as IGBTs or MOSFETs and associated driver circuits increase the cost and size of the power electronic interfaces. Due to this fact, the number of semiconductor switch reduction has been first proposed on the motor drive and electrical vehicle applications. Two-leg three-phase converter topologies are controlled as two-level inverters to obtain three phase voltages by controlling switches at the two legs. The main reason behind this idea is the cost and size of the topology. Therefore, the reduction of the number of drivers is the focus of several research works. Initially, the reduction of the switches and drivers was achieved on the single-phase and three-phase conventional inverters [3], [4]. Multi-level inverters offer advantages such as low electromagnetic interference level, low filter requirement, low losses, allowing ordinary semiconductor switches to be used in higher voltage level applications and to access higher power level. As a result, three-level inverters are often preferred for medium and high-power applications. Therefore, the use of multilevel inverters (MLI) is considered as a hot topic in the power electronics industry due to the above-mentioned advantages over conventional inverters [5]. Different MLI topologies such as Neutral Point Clamped [6], Flying capacitor [7], Packed U-Cell [8], and Cascaded H-Bridge inverters [9] have been reported in the literature for different applications. The T-type inverter, is a new multilevel inverter topology, has been applied for many applications such

978-1-7281-4878-6/19/$31.00 ©2019 IEEE

as induction machine drives [4] and grid-connected inverters [10].

To the best of authors knowledge, there is very limited studies on the use of three phases three-leg T-type for active power filter (APF) applications and no any reported paper related with two-leg T-type APF application. In [11], a method is proposed for the dc-link voltage balancing for the three-leg T-type APF. In [12], the most popular reference current extraction techniques such as fast Fourier transform, instantaneous reactive power technique and synchronous reference frame technique have been applied on the three-leg T-type APF converter to investigate their performances on the controller side.

In this paper, two-leg T-type three-phase APF topology is investigated, and three-level hysteresis band modulation strategy is employed. Moreover, dc-link voltage balancing method is adopted for balancing the voltage imbalance existing in the capacitor voltages [13].

II. CONTROL STRATEGY

A. *Determination of Filter Current Reference and Compensation of Imbalance in dc-link Capacitors*

The main aim of an APF is to compensate the undesired harmonics existing in the source current. The load current in any non-linear load group consists of fundamental and high frequency harmonic components given by:

$$i_L(t) = i_{L1}(t) + i_{Lh}(t) \tag{1}$$

where $i_L(t)$ is the load current, $i_{L1}(t)$ is the fundamental component at 50 Hz, and $i_{Lh}(t)$ is the high frequency harmonic component. Generally, the APF is run in the consumer power plant as a current source which connects directly to the distribution board. The main aim of the APF is to generate a compensating current, $i_c(t)$, which has the same magnitude with the drawn harmonic current components of the load but in opposite phase, i.e. $i_c(t) = -i_{Lh}(t)$. This action forces the source current to be sinusoidal as given by $i_s(t) = i_{L1}\sin(\omega t)$. A very large number of current harmonic distortion techniques have been developed and proposed in the literature [14]. In this study, self-tuning filter (STF) method is preferred to use for the detection of harmonic components. The STF algorithm has been found quite effective for the extraction of harmonics in the control of conventional two-level APF [15], [16].

In order to determine the reference for $i_{L1}(t)$, the measured load current $i_L(t)$ waveforms are converted into the two-phase system by using the following Clarke conversion:

$$\begin{bmatrix} i_{L\alpha}(t) \\ i_{L\beta}(t) \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La}(t) \\ i_{Lb}(t) \\ i_{Lc}(t) \end{bmatrix} \tag{2}$$

Then, the load current at the two phase coordinate system is processed through the STF. In [17], the transfer function of the STF is obtained by integration of the synchronous reference frame and it is defined as:

$$H(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = \frac{s + j\omega}{s^2 + \omega^2} \tag{3}$$

where

$$V_{xy}(t) = e^{j\omega t} \int U_{xy}(t) e^{-j\omega t} dt \tag{4}$$

In this study, the obtained two-phase load currents in (2) is processed as follows:

$$i^*_{L1\alpha}(s) = \frac{\gamma}{s}\left[i_{L\alpha}(s) - i^*_{L\alpha}(s)\right] - \frac{\omega}{s} i^*_{L\beta}(s) \tag{5}$$

$$i^*_{L1\beta}(s) = \frac{\gamma}{s}\left[i_{L\beta}(s) - i^*_{L\beta}(s)\right] + \frac{\omega}{s} i^*_{L\alpha}(s) \tag{6}$$

The obtained fundamental $(i^*_{L\alpha}\, i^*_{L\beta})$ reference load currents at two-phase coordinate system can be re-converted to the three-phase coordinate system as follows:

$$\begin{bmatrix} i^*_{L1a}(t) \\ i^*_{L1b}(t) \\ i^*_{L1c}(t) \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 0 & 1 \\ \sqrt{3}/2 & -1/2 \\ -\sqrt{3}/2 & -1/2 \end{bmatrix} \begin{bmatrix} i^*_{L1\alpha}(t) \\ i^*_{L1\beta}(t) \end{bmatrix} \tag{7}$$

It is important to mention that the obtained reference signals $(i^*_{L1a}, i^*_{L1b}, i^*_{L1c})$ cannot be used directly to drive the converter. Because there is need to determine converter active losses by using a proportional-integral (PI) algorithm. For this, the reference source current amplitude can be obtained by using a PI algorithm as:

$$I_s = k_p(v_c^* - [v_{c1} + v_{c2}]) + k_i \int (v_c^* - [v_{c1} + v_{c2}])dt \tag{8}$$

where $k_p$and k_i are the proportional and integral gains of the dc-link PI regulator, respectively. The summation of measured voltages on the split capacitors is equal to the inverter dc-link voltage. Therefore, the measured voltages on the capacitors are summed to obtain total dc-link voltage, i.e., $(v_c = v_{c1} + v_{c2})$. Then, the amplitude of each reference load currents $(i^*_{L1a}(t), i^*_{L1b}(t), i^*_{L1c}(t))$ can be calculated by using peak detector, and then divided by the determined reference signal for phase-a and phase-b as follows

$$i^{**}_{L1k}(t) = \frac{i^*_{L1k}(t)}{I_{L1k}}, \quad k = a, b \tag{9}$$

The parameters of phase-c can be ignored since there is no need to control phase-c in the studied topology. By this, $i_{L1a}^{**}(t)$ & $i_{L1b}^{**}(t)$ are determined as unity sine function which is varying between +1 and -1. Finally, the reference currents are calculated by multiplying (8) with (9) as follows

$$i_{ck}^{*} = I_s i_{L1k}^{**}(t), \quad k = a, b \tag{10}$$

As well known that PI regulator forces the summation of capacitor voltages (v_{c1} and v_{c2}) to follow pre-settled dc constant value during the harmonic current injection to the load bus. As mentioned in [13] that there exists an imbalance on the split capacitor's voltages which is one of the drawbacks of the multilevel inverter topology. The main reason behind this voltage difference is due to system's initial conditions. The second reason is due to the existence of small difference between the split capacitor values ($C_1 \approx C_2$) due to the practical reasons. As presented in [13], this imbalance voltage levels can be eliminated by adding the following voltage difference into the control equations:

$$(v_{ce} = v_{c1} - v_{c2}) \tag{11}$$

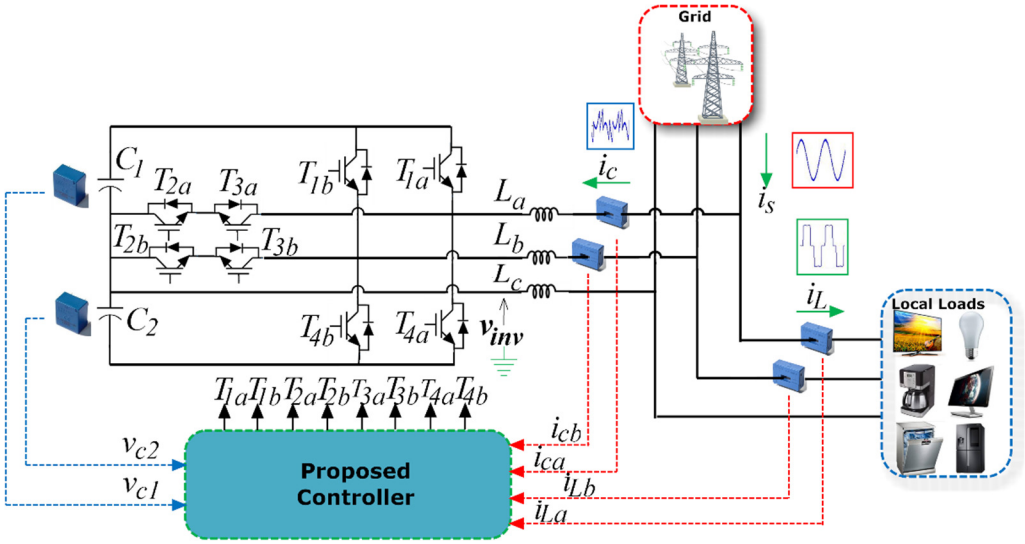

Fig. 1. Three-phase two-leg T-type active power filter.

For this, the obtained voltage difference between the capacitors first should multiplied with a gain (δ) and then summed with i_{ca}^{*} and i_{cb}^{*} as follows

$$\left.\begin{aligned} i_{ca}^{**} &= i_{ca}^{*} + \delta v_{ce} \\ i_{ca}^{**} &= i_{cb}^{*} + \delta v_{ce} \end{aligned}\right\} \tag{12}$$

where δ <0. Finally, the corresponding compensating filter current error is generated by subtracting the measured filter currents from the reference current in (12) as follows

$$\left.\begin{aligned} \Delta i_{ca} &= i_{ca}^{**} - i_{ca} \\ \Delta i_{cb} &= i_{cb}^{**} - i_{cb} \end{aligned}\right\} \tag{13}$$

The switching signals are generated by using the three-level hysteresis current control described in the next sub-section.

B. *Three-Level Hysteresis Current-Control*

As reported in the literature that conventional single-band or double-band hysteresis current control (HCC) methods cause high switching frequency with high switching losses.

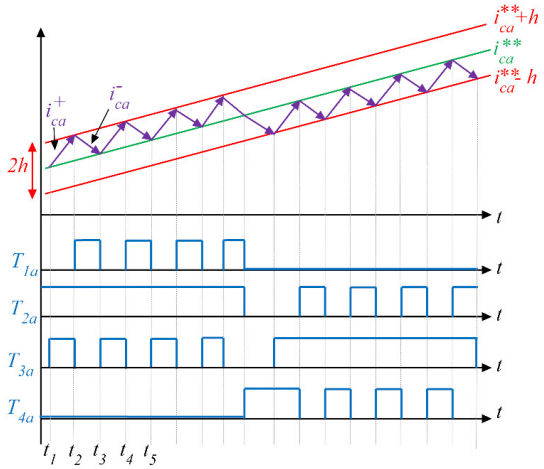

Fig. 2. Three-level Hysteresis current control and generation of PWM pulses for phase-a.

In order to solve this issue three-level hysteresis current control method is used in this study to drive the proposed T-type based APF converter.

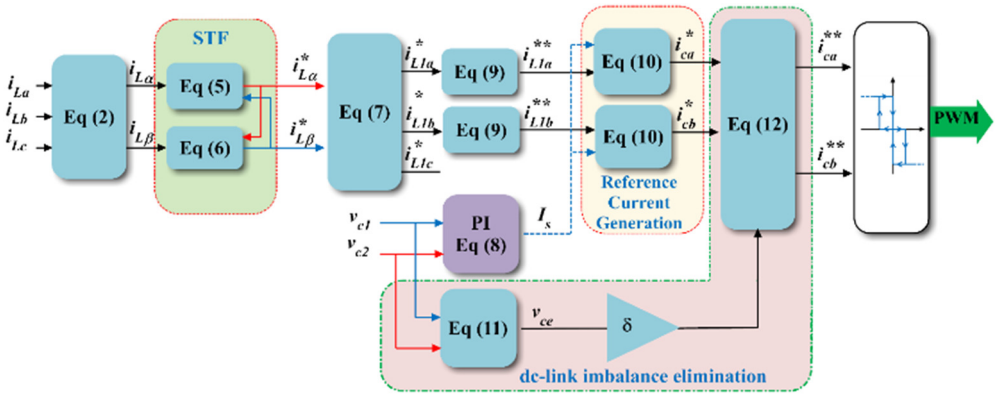

Fig. 3. Proposed control method.

Operational principle of three-level HCC is presented in Fig. 2 where h denotes the hysteresis band. The detailed analysis of three-level HCC can be found in [13] which is applied to half bridge three-phase APF. The proposed control method is presented in Fig. 3.

III. Simulation Results

The studied system is modelled and simulated in MATLAB/Simulink environment to verify the performance of the proposed techniques. In this model, three-phase phase-to-phase source voltage is assumed to be 90V. The full bridge rectifier supplied RC loads (Load 1 and Load 2) are used as nonlinear loads. The system and control parameters used in this study are given in the Table I. The total harmonic distortion (THD) of load current is computed to be 30.90 % with the first load and 28.28 % under full load condition (load 1 and load 2). The current feeding both loads is presented in Fig. 4. The generated and injected compensating filter current is presented in Fig. 5.

TABLE I
Parameters of the Simulated System

Symbol	Quantity	Value
v_{S} , f	Phase to Phase Volt. & Freq.	90 V, 50 Hz
L_c	Converter Filter Impedance	2mH
Z_L	Load Impedance	1 mΩ 0.5 mH
Load $_1$	Non-Linear Load Res. and Ind.	15 Ω, 20 µf
Load $_2$	Non-Linear Load Res. and Ind.	30 Ω, 20 µf
C_1 & C_2	APF dc Capacitors	5000 µf
v_c^*	dc- Link reference voltage	250 V
K_p & K_i	Proportional & Integral Gain	1.2 & 20
h / -h	Hysteresis band	0.1 / -0.1
γ	STF Gain	50
δ	dc-link imbalance gain	-0.15

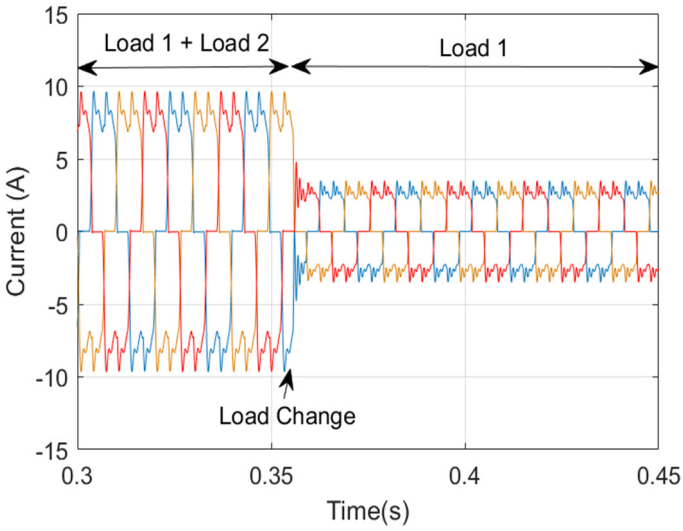

Fig. 4. Load current waveforms, i_L.

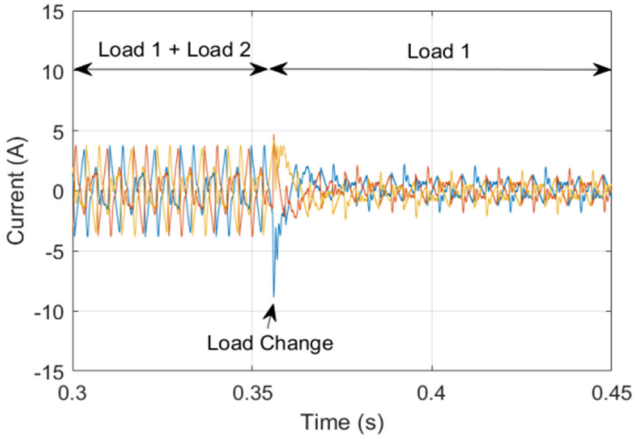

Fig. 5. Converter current waveforms, i_C.

Finally, the three-phase source current waveforms obtained under these loads are given in Fig. 6. The THD of the source currents are reduced from 28.90% to around 1.60 %. As discussed earlier, there is a need to determine the inverter losses and balance the split capacitor voltages.

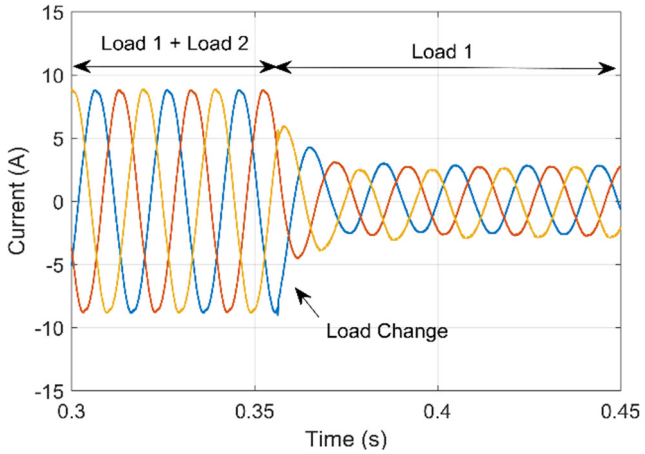

Fig. 6. Source current waveforms, i_s.

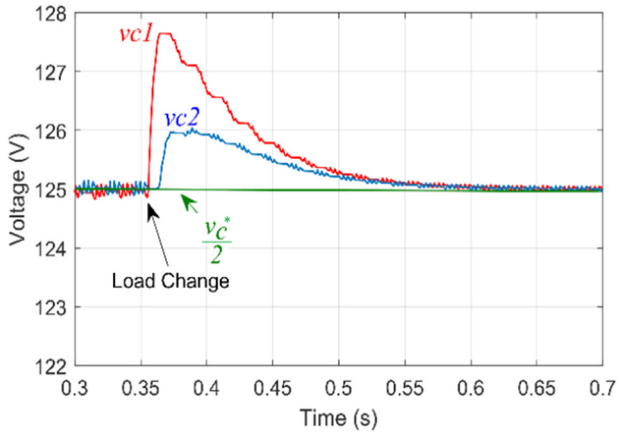

Fig. 7. Voltage profile across the upper and lower capacitors ($v_{c1}$and v_{c2}).

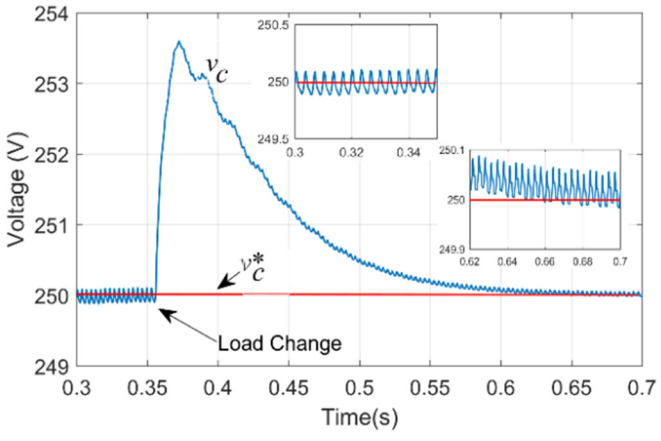

Fig. 8. voltage profile across the dc-link, v_c.

Therefore, the capacitor (C_1 and C_2) voltages at the dc-link are first measured and then processed by a PI algorithm. As can be seen in Figs.7 the voltage unbalance on the capacitors is eliminated successfully. More importantly, dc-link voltage is kept at the constant voltage v_c^*level which is 250 V as presented in Fig.8. The obtained multi-level phase to ground inverter steady-state output voltages are also presented in Fig. 9.

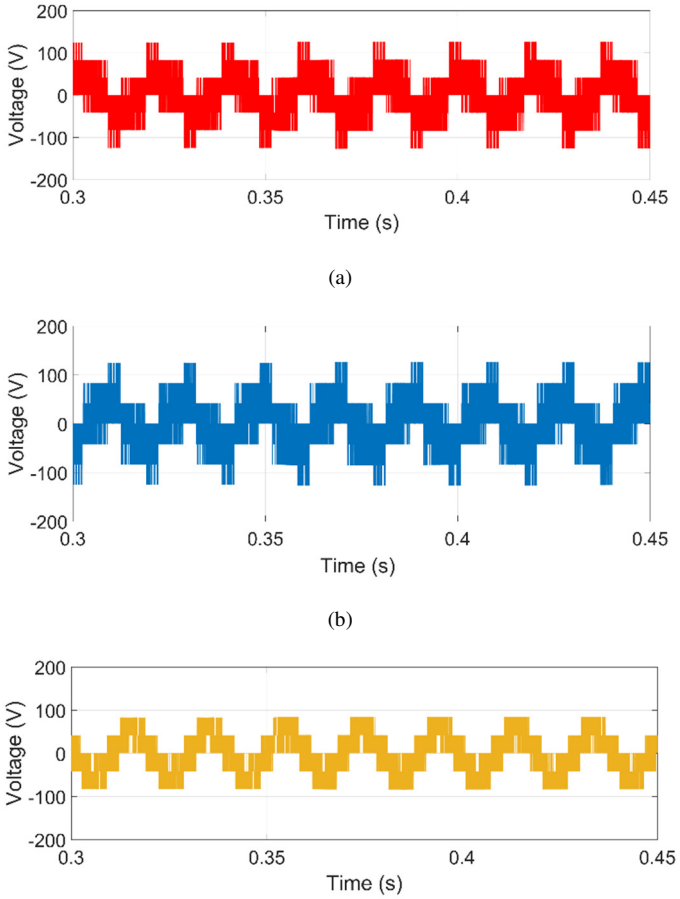

Fig. 9. Steady-state responses of inverter output phase to ground voltage waveforms v_{inv} at (a) phase-a (v_{inv-a}), (b) phase-b (v_{inv-b}), (c) phase-c (v_{inv-c}),.

IV. Conclusions

In this study, a two-leg three-phase T-type inverter topology is investigated for active power filter applications. A self-tuning filter technique is used to generate reference load current. Moreover, capacitor voltage balancing strategy is proposed. In order to reduce the switching frequency, three-level hysteresis band controller is proposed. The performance of the studied system is investigated by simulation study during steady-state and varying load conditions. The presented results show that the harmonic distortions are eliminated successfully with the proposed topology and control method.

REFERENCES

[1] He, Jinwei; Beihua Liang; Yun Wei Li; Chengshan Wang, "Simultaneous Microgrid Voltage and Current Harmonics Compensation Using Coordinated Control of Dual-Interfacing Converters". *IEEE Transactions on Power Electronics*. 32 (4): 2647–2660.

[2] V. Gali, N. Gupta and R. A. Gupta, "Mitigation of power quality problems using shunt active power filters: A comprehensive review," *2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Siem Reap, 2017, pp. 1100-1105.

[3] D. C. Lee, T. Y. Kim, G. M. Lee and J. K. Seok, "Low-cost single-phase to three-phase PWM AC/DC/AC converters without source voltage sensor," *IEEE International Conference on Industrial Technology, 2002,* pp. 792-797, Bangkok, Thailand.

[4] D. Lee and Y. Kim, "Control of single-phase-to-three-phase AC/DC/AC PWM converters for induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 797-804, April 2007.

[5] M. Vijeh, M. Rezanejad, E. Samadaei and K. Bertilsson, "A general review of multilevel inverters based on main submodules: structural point of view," *IEEE Trans. Power Electron.*, (Early access).

[6] S. Biricik, H. Komurcugil, T. Ngo and M. Basu, "Operation of three-level single-phase half-bridge NPC inverter-based shunt active power filter under non-ideal grid voltage condition with sliding mode controller," *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, Doha, 2018, pp. 1-6.

[7] M. Trabelsi, L. Ben-Brahim, A. Gastli and K. A. Ghazi, "An improved predictive control approach for Multilevel Inverters," 2013 IEEE International Symposium on Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), Munich, 2013, pp. 1-7.

[8] Shunlong Xiao, M. Metry, M. Trabelsi, R. S. Balog and H. Abu-Rub, "A Model Predictive Control technique for utility-scale grid connected battery systems using packed U cells multilevel inverter," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 5953-5958.

[9] L. Ben-Brahim, M. Trabelsi, T. Yokoyama and T. Ino, "Real Time Digital Feedback Control for VFD fed by Cascaded Multi-cell inverter," The 2010 International Power Electronics Conference - ECCE ASIA -, Sapporo, 2010, pp. 2493-2500.

[10] N. Altin, S. Ozdemir, H. Komurcugil, I. Sefa and S. Biricik, "Sliding-mode and proportional-resonant based control strategy for three-phase two-leg T-type grid-connected inverters with LCL Filter," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, pp. 4492-4497, Washington, DC, 2018.

[11] D. Chen, Q. Xu, Y. Hu and G. Chen, "A DC-link voltage balancing strategy based on controllable neutral current injected for T-type three-level active power filter," *IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Auckland, 2016.

[12] M. J. Chudasama, S. K. Chauhan, P. N. Tekwani and V. Patel, "Simulation as-well-as experimental investigations on T-type NPC topology based three-level shunt active power filter," *International Conference on Technological Advancements in Power and Energy*, Kollam, 2017.

[13] S. Biricik and H. Komurcugil, "Three-level hysteresis current control strategy for three-phase four-switch shunt active filters," *IET Power Electronics*, vol. 9, no. 8, pp. 1732-1740, 2016.

[14] T. C. Green and J. H. Marks, "Control techniques for active power filters," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 2, pp. 369-381, 4 March 2005.

[15] S. Biricik, O. C. Ozerdem, S. Redif, and M. S. Dincer, "New hybrid active power filter for harmonic current suppression and reactive power compensation," *International Journal of Electronics,* vol. 103, no. 8, pp. 1397-1414, 2016.

[16] S. Biricik, S. Redif, Ö. C. Özerdem, S. K. Khadem, and M. Basu, "Real-time control of shunt active power filter under distorted grid voltage and unbalanced load condition using self-tuning filter," *IET Power Electronics* , vol. 7, no. 7, pp. 1895-1905, 2014.

[17] M. Abdusalam, P. Poure, S. Karimi, and S.Saadate. "New digital reference current generation for shunt active power filter under distorted voltage conditions," *Electric Power Systems Research,* vol. 79, no. 5, pp. 759-765, 2009.