A New MMC Topology Which Decreases the Sub Module Voltage Fluctuations at Lower Switching Frequencies and Improves Converter Efficiency

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Abstract

Modular Multi-level inverters (MMCs) are becoming more common because of their suitability for applications in smart grids and multi-terminal HVDC transmission networks. The comparative study between the two classic topologies of MMC (AC side cascaded and DC side cascaded topologies) indicates some disadvantages which can affect their performance. The sub module voltage ripple and switching losses are one of the main issues and the reason for the appearance of the circulating current is sub module capacitor voltage ripple. Hence, the sub module capacitor needs to be large enough to constrain the voltage ripple when operating at lower switching frequencies. However, this is prohibitively uneconomical for the high voltage applications. There is always a trade off in MMC design between the switching frequency and sub module voltage ripple.

The converter reliability is the other important issue of using MMCs as they use a lot of components in their structure. A fault of one sub module can also cause the other components in the corresponding arm to fail and lead to total system collapse. When the quantity of broken sub modules is more than the redundant ones, the MMC would work with asymmetrical operation. In the worst case, this might result in system failure. Moreover, MMC needs higher number of voltage sensors which will increase the cost of converter and deteriorate the converter reliability.

In this research, a new topology for MMC has been proposed which can maintain the sub module voltage ripples in an acceptable range without the need for large capacitor values when operating at lower switching frequencies. The main contribution is the elimination of the sub module voltage fluctuations at lower switching frequencies which will lead to improved converter efficiency and maintaining the circulating current content in the acceptable range. Moreover, the proposed design doesn't need any sub module voltage sensors which will reduce the converter cost and complexity and will improve the converter reliability. It can also improve the converter reliability during the sub module capacitor failure. Considering open circuit status for the faulty sub module capacitor, the converter can continue the normal operation. The proposed topology provides robust and fast responses to sub module capacitor faults with minor additional costs and its reliability improvement is more significant as the number of sub modules increases. The simulation results demonstrate the effectiveness of the proposed topology in decreasing the converter total losses and reliability improvement.

Declaration

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This thesis was prepared according to the regulations for postgraduate study by research of the Technological University Dublin and has not been submitted in whole or in part for another award in any Institute.

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Abbreviations List

CSC	Current Source Converter
HVDC	High Voltage Direct Current
UHV	Ultra-High Voltage
VSC	Voltage Source Converter
IGBT	Insulated Gate Bipolar Transistor
GTO	Gate Turn-Off Thyristor
BJT	Bipolar Junction Transistor
IGCT	Integrate Gate-Commutated Thyristor
PWM	Pulse Width Modulation
MMC	Modular Multilevel Converter
SM	Sub Module
HB	Half Bridge
FB	Full Bridge
LCC	Line Commutated Converter
PD	Phase Disposition
NLC	Nearest Level Control
PSC	Phase Shifted Carrier
THD	Total Harmonic Distortion
SVM	Space Vector Modulation
3L-FC	Three-Level Flying Capacitor
FCMC	Flying Capacitor Multi Cell Converters
CSM	Composite Multilevel Sub Module
PMSG	Permanent Magnet Synchronous Generator

WECS	Wind Energy Conversion System
SCSM	Switched Capacitor Sub Module
DZ-SM	Double Zero Sub Module
MPC	Model Predictive Control
CCSC	Circulating Current Suppressing Control
PR	Proportional Resonant
PTG	Pole to Ground
LGF	Line to Ground
SCF	Short Circuit Fault
ACCB	AC Circuit Breaker
DCCB	DC Circuit Breaker
DMR	Dedicated Metallic Return
CDSM	Clamp Double Sub Module
QRB-MMC	Quasi Reverse Blocking Modular Multilevel
SPG	Single Phase to Ground
CLR	Current Limiting Reactors
FCL	Fault Current Limiter
TL-HMMC	Three Level Cell-Based Hybrid MMC
FDM	Fault Diagnosis Method
CA	Clustering Algorithm
SRF	Synchronous Rotating Reference Frame
ESR	Equivalent Series Resistance

List of Acronyms

V_{dc}	DC bus voltage
V_C	Sub Module Capacitor Voltage
L_{arm}	Arm Inductance
i_{SM}	Sub Module Current
v_{SM_out}	Sub Module Output Voltage
i_U	Upper Leg Current
i_L	Lower Leg Current
i_C	Circulating Current
i_S	Output Current
R_L	Load Resistance
L_L	Load Inductance
N_{on}	Number of Inserted Sub Modules
$K_{ripplemax}$	Maximum Sub Module Voltage Ripple
Δe_{pmax}	Maximum Sub Module Energy Variation
T_s	Switching Cycle of IGBT
E	Ripple Factor
S	Three Phase Apparent Power
W	Fundamental Frequency
M	Modulation Index
$cos\emptyset$	Power Factor
f_s	Switching Frequency
P_{cond}	Conduction Losses
V_f	Forward Voltage Drop
I_{av}	Average Current
I_{rms}	Root Mean Square Value of Current
P_{sw}	Switching Losses
X_L	Total Reactance of the Converter Transformer and the Phase Reactor
P_c	Active Power Exchanged Between the MMC and the AC System
Q_c	Reactive Power Exchanged Between the MMC and the AC System
PCC	Point of Common Coupling

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Chapter 1

Introduction

For the first half of twentieth century, AC power transmission was the preferable option due to the ability of power transformers to step up and step-down voltage levels to reduce the power losses. During the early 1950s, there was a renewed interest in the use of DC technology as it was a cost effective option for long distance overhead line transmission [1].Where transmission distances are very long (beyond 1000 km) the AC transmission capacity is limited due to stability considerations. A high voltage drop occurs across the AC transmission lines. However, the DC transmission line is free from inductance, and hence only a small resistive voltage drop occurs across the line. The other advantage of DC transmission line is that the phenomenon of skin effect is not present on the DC transmission line. Lower insulation requirement and absence of Corona effect are the other superiorities of DC transmission line. Fig. 1.1 depicts that the initial investment cost for the DC terminal is higher than the AC one. However, for long distances the total cost for the DC transmission will be lower than the AC transmission.
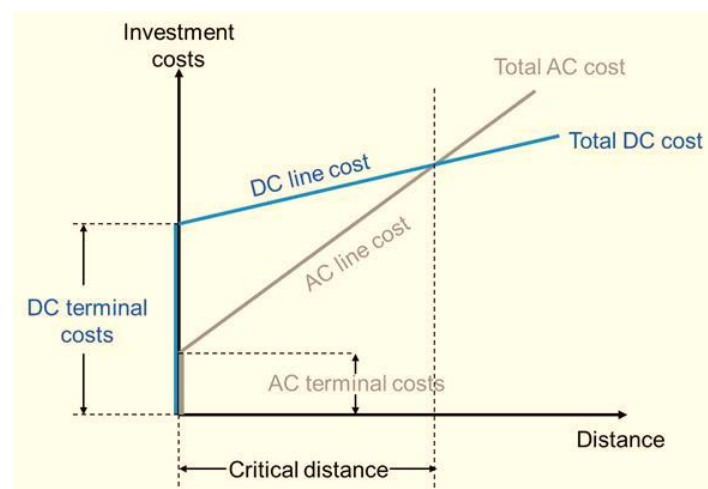
Fig. 1.1 Investment costs for DC and AC transmission lines

1.1 Power Converters

1.1.1 Current source converter (CSC)

As the name indicates, the current source converter (CSC) likes to see a stiff DC current source at the input (ideally with infinite Thevenin impedance). The current source can be achieved by connecting a large inductor (inductance) in series with a variable voltage source that is controlled by a current feedback loop. With a stiff DC current source, the AC output currents will not be affected by load conditions. Since power semiconductor devices in a CSC must withstand reverse voltage, symmetric voltage blocking devices such as thyristors are usually used [2].

CSCs have been the only HVDC transmission solution for many decades and they are still the first choice for bulk power transmission at the GW-level [3],[4]. A CSC is usually based on a 12-pulse bridge configuration as shown in Fig. 1.2 Three AC connectors are on the left-hand side and two DC terminals are on the right-hand side. Two of such 12-pulse bridges are usually connected in series to form the positive and negative terminals of the DC bus as shown in Fig. 1.3.
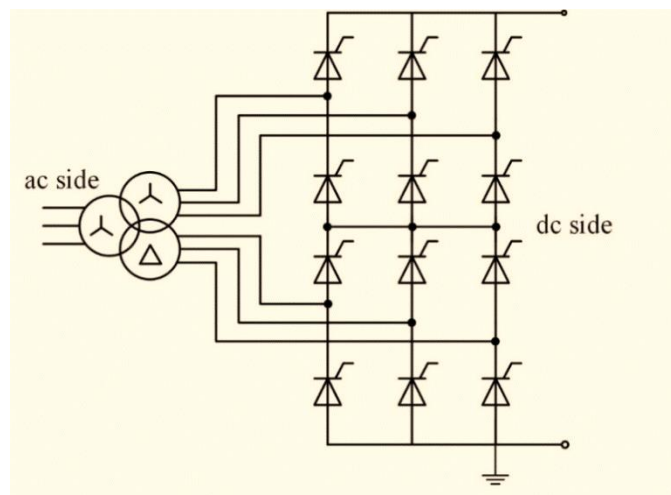
Fig. 1.2 A 12-pulse converter bridge [5]
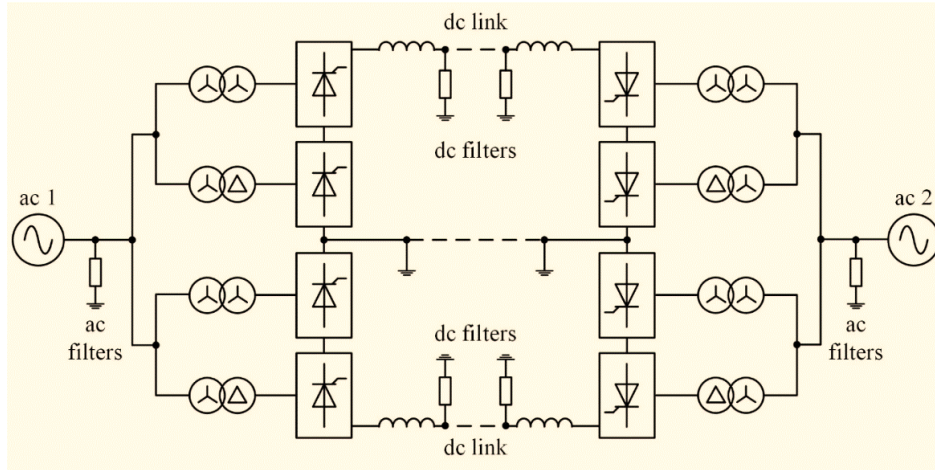
Fig. 1.3 A bipolar CSC-HVDC system with one 12-pulse bridge per pole [5]

The advantage of such a structure is that one pole can continue to transmit power in the case that the other one is out of service for whatever reason. Each system can operate on its own as an independent system with the earth return. Projects at a DC voltage of ±800 kV are also termed ultra-high voltage (UHV) DC systems and they usually consist of two such series connected 12-pulse bridges per pole.

The advantages of the CSC-HVDC system include a high overload capability, excellent robustness, reliability and low operational losses. The total loss of an AC transmission system with 6.4 GW capacity at 1,000 kV is around 7% per 1,000 km, while the line loss of a ±800 kV HVDC with the same capacity is only 3.5%. Even when the 0.7% converter losses per station are included, the total loss of a CSC-HVDC system is still much lower than the HVAC option [5].

Although the CSC-HVDC serves the transmission industry well, it has several drawbacks:

• First, the AC outputs contain significant low order harmonics, which will cause various power quality problems, leading to higher losses and the malfunction of sensitive loads [2]. Massive filters are necessary on both the AC side and DC side for smooth power outputs.

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- Second, due to the absence of the turn-off capability in the thyristor, the commutation of the switch is driven by the interconnected AC grid and the current is always lagging, i.e. keeps absorbing reactive power from the grid. As a result, massive reactive power compensation equipment is required on the AC side.

- Third, the direction of the power flow cannot be reversed by reversing the DC current due to the switch configuration. The change of power flow direction can only be achieved through a change in DC polarities. As a result, the relatively cheap and light polyethylene insulated DC cables are not suitable due to their poor fast polarity reversal capability. This is also one of the major obstacles to building a multi-terminal DC grid using CSC technology [6].

- Finally, the CSC-HVDC is sensitive to the strength of the inter-connected AC system. Particularly at the inverter side, slight disturbances in the AC system may lead to commutation failure in the converter. Consecutive commutation failures may lead to system breakdown.

1.1.2 Voltage source converter (VSC)

Voltage source converters (VSCs), as the name indicates, receive DC voltage at one side and convert it to AC voltage on the other. A VSC prefers a stiff DC voltage source at the input (ideally zero Thevenin impedance) which is usually achieved using large capacitors[2]. Ever since the first VSC project (±10 kV, Hellsjon experimental project) was built in1997, the voltage and power ratings of VSCs have steadily increased. Currently, VSC systems with ratings of up to ±320 kV, 1 GW are technically achievable. Fig. 1.4 shows the simplest VSC topology, i.e. the two-level AC/DC converter (with IGBT/diode modules). In VSCs, the power semiconductor switches always remain forward-biased due to the DC bus voltage, and therefore, not only IGBTs, but all other self-controlled forward or asymmetric blocking switches, such as GTOs, BJTs, power

MOSFETs, and IGCTs can be used. A diode is always connected across the device to achieve free reverse current flow and ensure the four-quadrant operation of the converter.
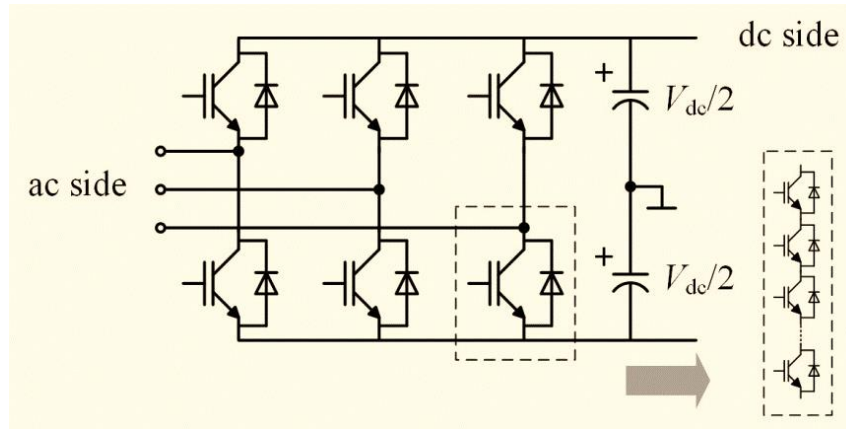
Fig. 1.4 Diagram of a two-level VSC

Since the blocking voltage of currently available IGBT modules is only up to 6.5 kV, in order to block the voltage up to a few hundred kV, large amounts of IGBT modules are directly connected in series as shown in the dashed box in Fig. 1.4. Typically, VSCs are controlled through pulse width modulation (PWM) techniques, among which the sinusoidal PWM (SPWM) is the simplest and thus is commonly adopted for industrial converters. When compared with the thyristor-based CSC-HVDC system, the IGBT-based VSC-HVDC system has the following benefits [7]:

- Both the amplitude and phase angle of AC output voltages can be controlled independently, offering independent and rapid control of the active and reactive power. The fast dynamic can help to enhance the transient stability of the interconnected AC grid.

- Owing to the self-commutation capability of the IGBT, VSCs can operate in all four quadrants of the *P-Q* operating plane without external reactive power compensation.

- Power reversal can be achieved through reversing the DC current instead of the DC voltage polarities, which is critical for a multi-terminal DC grid.

- Due to the high frequency of switching, the harmonics that need to be filtered are at high frequencies and thus the filtering demands are largely reduced.

On the other hand, two and three-level VSCs have their own disadvantages [8]:

- In order to achieve the high voltage rating, large amounts of IGBTs are connected in series, demanding very complex gating and protection schemes.

- The PWM process requires the simultaneous switching of series-connected devices at high frequencies (one to a few kHz), leading to significant power losses (typically 1.6% per station). This is one major reason why the CSC-HVDC is still preferable for bulk power transmissions.

The situation began to change with the advent of the modular multilevel converter (MMC), which was a milestone in VSC technology and in 2010 the first MMC project started commercial operations, i.e. the Trans Bay Cable in the United States rated at ± 200 kV, 400 MW.

Fig. 1.5 shows a typical configuration of a DC to three-phase AC MMC system. Valve in the converter arms is no longer a single IGBT/diode module but a controllable VSC itself, which is usually referred to as sub module (SM) or cell.

A SM can be a half-bridge (HB) converter as shown in the dashed line box (Fig. 1.5), a full-bridge (FB) converter, or it can appear in other forms. Direct series connection of power switches is no longer needed. Each SM can be switched as low as the AC line frequency leading to increased efficiency and reduced cooling demands. Typical losses for one MMC station can be less than 1.0%. The large number of steps in the synthesized AC voltage waveform provides low distortion and good EMC performance. Hence, harmonic filters become a thing of the past for both the AC side and DC side [6].
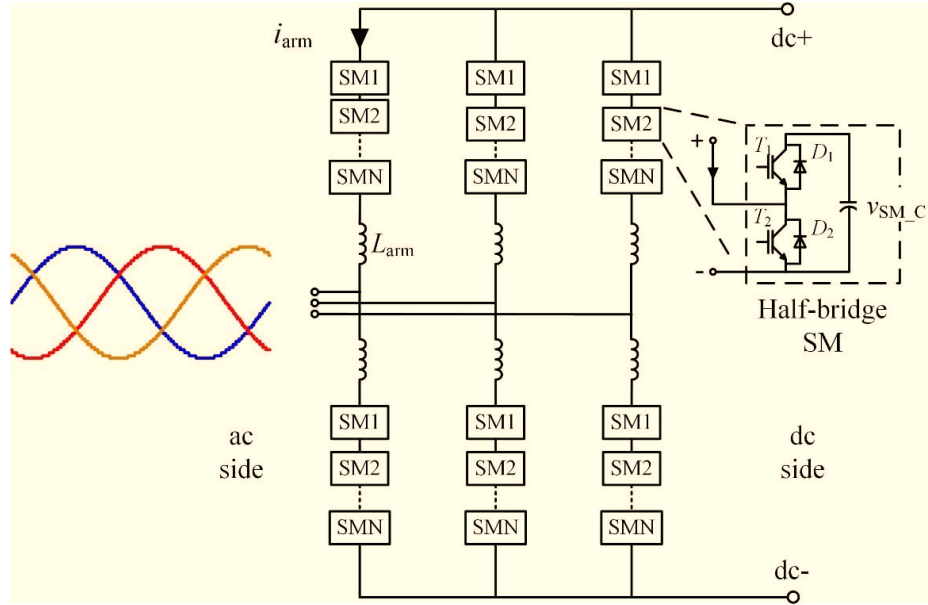
Fig. 1.5 Typical configuration of a DC to three-phase AC MMC system

1.2 High Voltage DC transmission

In recent times, High Voltage DC (HVDC) transmission is becoming more popular for the interconnection of remote renewable energy resources to the grid. Installation of HVDC transmission lines are increasing in China, Europe and North America. For long transmission distances, the lifetime cost for HVDC system is lower than HVAC system and this makes HVDC system the more appropriate option for long distance large-scale offshore wind energy transmission [9].

1.2.1 Line Commutated Converter (LCC) Based HVDC

The LCC HVDC system is a classic solution for the DC transmission system, in use since mid-20th century, which employs high power thyristors in converters. It is also called a Current Source Converter (CSC) as it acts as a current source to the grid. By regulating the firing angle (α), rectifier and inverter terminals control DC current and voltage respectively [10]. The LCC-HVDC transmission line can operate only in AC grids with established or live AC voltages as it requires these live AC voltages to commutate currents from outgoing to incoming arm. The direction of real power flow is

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from rectifier to inverter and both converters consume reactive power. The LCC station has large footprint as it uses large switched capacitor banks and AC side harmonic filters to supply its reactive power consumption, which varies with the magnitude of DC or real power transfer, particularly, at inverter terminal. The need for the fast-acting mechanical switches during the power reversal is one of the drawbacks of the LCC MTDC system. The other issue is the commutation failure at inverter terminal during asymmetric AC faults or generally during operation in weak AC grids [11]. The Sardinia-Corsica-Italy (SACOI) interconnection and the Hydro-Quebec-New England interconnection are examples of existing LCC MTDC systems. Currently, an increase in the rated power, nominal voltage and length of transmission distance is observed. The power capacity can exceed 5000 MW, at voltage of 800 kV and transmission distances via overhead line up to 3000 km. Work is underway on the use of 1100 kV voltage for the transmission of 10-12 GW power over the distance of 2000 km. The largest, so far, LCC HVDC systems have been built in China and India. An important application of LCC HVDC technology are subsea connections of non-synchronous areas. Many such connections have been implemented in Europe. The largest are the NorNed connection, between Norway and the Netherlands, with the following parameters: rated power 700 MW, cable length 580 km, voltage ±450 kV. Under construction is a connection between Norway and the UK with a length of 750 km and a rated power of 1400 MW.

1.2.2 Voltage Source Converter (VSC) Based HVDC

The application of voltage source converters in HVDC transmission system has been developing since 1997. VSC technology uses IGBTs with antiparallel diodes in the converter bridge to allow current flow in both directions and voltage blocking in forward and backward directions. The most beneficial advantage of VSC based HVDC over LCC based HVDC is independent control of active and reactive powers, which is achieved by

exploiting two available control degree of freedom. Moreover, because of less filtering and reactive power requirements, the footprint of a VSC is much smaller than an equivalent LCC station. The main disadvantage of VSC technology is the high switching losses due to the use of high frequency pulse width modulation (PWM) [12].

Table.1.1 Summary of some worldwide VSC-HVDC projects [13]

Name	Converter Station 1	Converter Station 2	Cable (km)	Voltage (kV)	Power (MW)	Year
Hellsjön-Grängesberg	Sweden – Hellsjoen	Sweden – Graengesberg	10, Overhead line	180	3	1997
Terranora interconnector (Direktlink)	Australia – Mullumbimby	Australia – Bungalora	59	80	180	2000
Cross Sound Cable	USA – New Haven, CT	USA – Shoreham, Long Island	40	150	330	2002
HVDC Troll	Norway – Kollsnes	Norway – Offshore platform	70	60	80	2004
Estlink	Estonia – Harku	Finland – Espoo	105	150	350	2006
NordE.ON 1	Germany – Diele	Germany – Borkum 2 platform	203	150	400	2009
Trans Bay	USA – East Bay –	USA – San Francisco,	88	200	400	2010
HVDC DolWin1	Germany – Dörpen	Germany – DolWin Alpha platform	165	320	800	2013
HVDC NordBalt	Sweden – Nybro	Lithuania – Klapeida	450	300	700	2015
DolWin3	Germany – Heede	Germany – DolWin	160	±320	900	2017
Caithness Moray HVDC	UK – Spittal	UK – Blackhillock	160	320	1200	2018
Nemo Link	Belgium – near Bruges	UK – Richborough Energy Park	140	400	1000	2019
IFA-2	France – Tourbe, Normandie	UK -Pilling, Hampshire	240	400	1000	2020

Currently, point-to-point systems up to 1200 MW with cross-linked polyethylene cables and 500 kV voltage are used. Table. 1.1 summarizes the installed VSC HVDC projects in the world. Research into the most appropriate converter bridge topology design is ongoing. One of the most advanced voltage source converters is the Modular Multi-Level Converter (MMC) and it is the converter technology that this research is based on.

Among the existing MMC topologies for the HVDC, an MMC structure consisted of Half-Bridge Sub Module (HBSM)s has characteristics such as reduced system cost and low operation loss. The main disadvantage of the Half-Bridge Sub Module MMC is its fault blocking capability during the DC fault condition. To cope this issue, Full-Bridge Sub Module (FBSM)s could be added to the MMC structure. However, balancing the sub module capacitor voltages where each arm of the MMC is consisted of mixed (HBSM)s and (FBSM)s, is very difficult. Chapter 2, investigates about different challenges for HVDC system considering modular multi-level converters and also design aspects for the MMC.

1.3 Research Motivation

Modular multilevel converters have become popular in recent years because of their high efficiency, low harmonic distortion without using output filters, low switching frequency and high modularity [14]. Several multilevel topologies have been proposed, including a hybrid multilevel converter with AC side cascaded H-bridge cells, an alternative arm modular multilevel converter and a DC side cascaded multilevel with half bridge or full bridge cells connected across the DC link [15, 16]. The presented MMC topologies have several disadvantages which affect their performance.

The circulating current which occurs mainly due to the sub module voltage fluctuations is one of the challenges of the DC side cascaded MMC topology. Several control methods are proposed in the literature to suppress and eliminate the circulating current and most of the proposed methods are complex and difficult to implement [17-19]. The sub module voltage fluctuation is the main reason for the appearance of the circulating currents. It should be noticed that choosing a higher switching frequency will lead to a less sub module voltage ripple as well as a smaller sub module capacitor size but it will increase the converter losses. So the ideal working point could be a lower switching frequency with an acceptable voltage ripple (less than 10%) for each sub module which will necessitate the large sub module capacitor to constrain the voltage ripple. However, the ideal point is prohibitively uneconomical for the high voltage applications because the ideal point can only be achieved with extremely large sub module capacitance.

Converter reliability is the other important challenge in modular multilevel converters, since they include many components. For this reason, the development of fault-tolerant converter topologies and strategies are relevant research topics nowadays. Multiple studies analyse the reliability and provide solutions to faults. However, these techniques imply a high increase in the converter cost and complexity [20, 21].

In this research, a new topology for the MMC has been proposed which can maintain the sub module voltage ripples in an acceptable range even with lower switching frequencies without the need for large sub module capacitors. Moreover, the proposed design has more reliability in case of sub module capacitor failure and can operate without sub module voltage sensors. The main contribution is providing the acceptable voltage regulation (less than 10%) for each sub module and minimum switching losses during switching period by adding additional switches to connect idle capacitors in

parallel with active sub modules. The other contribution is converter reliability improvement which is achievable by the elimination of using voltage sensors and fault tolerant operation.

1.4 Research Questions and Objectives

Based on the discussion of the previous sections, the research questions and aims are defined as follows:

- How to eliminate the sub module voltage fluctuations with smaller sub module capacitor values at low switching frequencies? This issue also will be addressed by proposing a new MMC topology.

- How the MMC can operate at lower switching frequencies? The proposed design implements idle capacitors in parallel with sub modules. Consequently, the sub module capacitor size will be increased without the need to large sub module capacitors and the MMC will operate at lower switching frequencies with acceptable sub module ripple.

- What will be the converter efficiency with the new proposed topology? The new design uses some extra switches during the switching period. So, the MMC loss analysis at the lower switching frequencies will be done to calculate the efficiency of the new design.

- What will be the content of circulating current after applying the new design? After applying the new design at the low switching frequency (100 Hz), the amount of circulating current will be comparable to the achieved value at higher switching frequency of 1000 Hz.

- How the reliability of converter can be improved applying the new design? Operation without using any sub module voltage sensors will reduce the converter cost and complexity and will improve the converter reliability. Moreover, the proposed

topology can be kept in operational condition and work with more reliability in the case of the sub module capacitor failure.

The proposed topology is validated in simulation by modelling in MATLAB/Simulink. The simulation speed is the main limitation for this research, specially when the higher number of switches are utilized in the MMC design.

1.5 Thesis Outline

The thesis is divided into 5 Chapters. The first Chapter is a brief introduction about the HVDC transmission with LCC and VSC technologies. Research motivation and questions are also presented at the end of this Chapter. Review of the modular multi-level converters and different challenges for HVDC system considering modular multi-level converters is presented in Chapter 2. Chapter 3 explains about the proposed new MMC topology and its operational principle. In Chapter 4, Operation of the new proposed design at HVDC system level, sub module capacitor failure condition and impact of applying the proposed design at reducing the number of sub module voltage sensors are investigated. The proposal for the future work and conclusions is presented in the final Chapter.

Chapter 2: Review of The Modular Multilevel Converters and Different Challenges for HVDC System Considering Modular Multilevel Converters

This chapter reviews about the operational principle and different modulation techniques of the MMC. Design considerations and challenges considering modular multilevel converters also are discussed in this chapter. The mathematical model of Half-Bridge MMC is investigated in section 2.2 and section 2.5 explains about the design considerations of MMCs. Submodule capacitor size and ripple, challenge of switch count, challenge of circulating currents, DC fault and protection and sub module faults are discussed in section 2.5, 2.7, 2.8, 2.9 and 2.10.

2.1 Basic Operation Principles of MMC

Fig. 2.1 shows the basic idea of a multilevel converter [22]. The AC output voltage V_{dc} is achieved by an appropriate number of series-connected pre-charged capacitors. The higher number of capacitors (sub modules) leads to smaller size of voltage steps and lower proportion of harmonics and high frequency noises.
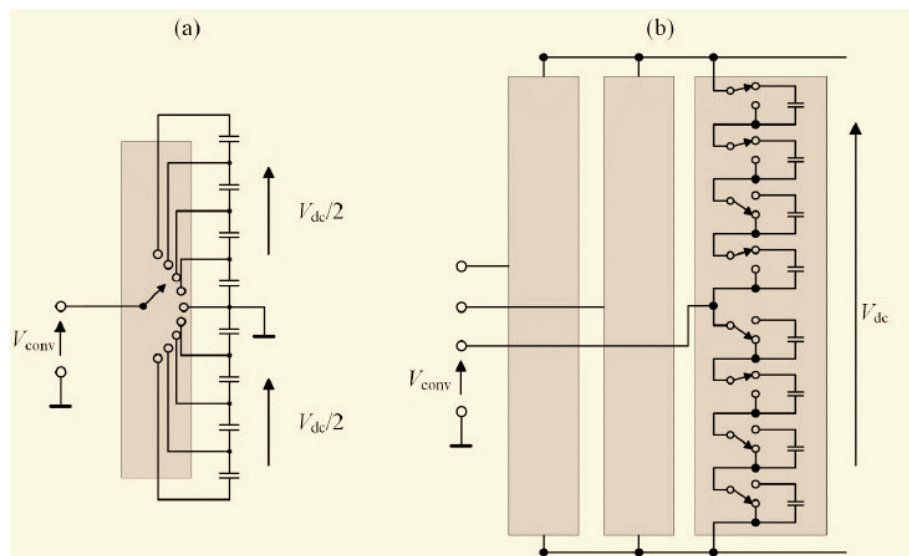
Fig. 2.1 (a) Basic representation of a multilevel converter; (b) the MMC's approach [22]

Fig. 2.1 (b) shows the MMC's approach to multilevel operation. There are three phase units corresponding to the three phases in the interconnected AC grid. Each phase unit has two converter arms, namely an upper arm and lower arm. Each converter arm consists of tens to a few hundred sub modules (SMs) connected in series. Each sub module itself is an independent VSC with usually a floating reservoir DC capacitor. Sub modules in each arm in total can withstand the entire converter DC bus voltage (V_{dc}). Each sub module can output either positive or zero voltage (sometimes negative with certain sub module topologies) to the arm circuit in order to synthesize the desired arm voltage. As shown in Fig. 2.2, through appropriate sub module switching strategies, the arm voltage is usually a sinusoidal waveform with a DC offset equal to half the DC bus voltage.
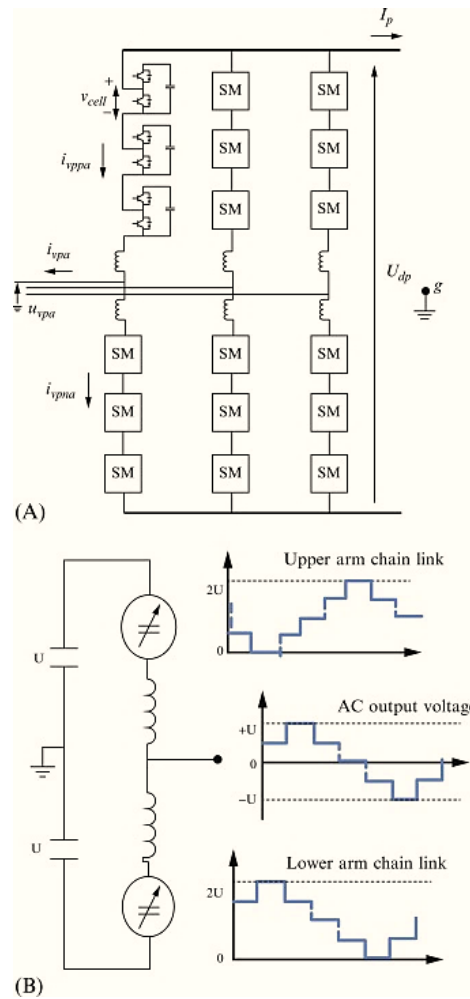
Fig. 2.2 Typical output waveforms of MMC [23]

2.1.1 Basic Operation Principles of Half-Bridge MMC

The basic operation principles of the Half-Bridge MMC are introduced in this section. The duty of each sub module is to output the desired voltage (usually positive or zero) when requested to synthesize the desired arm voltage. Among all the sub module topologies, the Half-Bridge sub module has been the most popular topology adopted for the MMC [24]. This is due to the presence of only two semiconductor switches in each sub module, leading to a lower number of devices, simpler circuit configuration, reduced control complexity, and higher system efficiency. Hereafter, the basic operation principles of the Half-Bridge sub module will be firstly introduced. Other sub module topologies will be discussed and compared at this Chapter.

Fig. 2.3 shows the circuit diagram of a Half-Bridge sub module, where T_1/D_1 represents the upper IGBT/diode module and T_2/D_2 stands for the lower IGBT/diode module. In normal operations, through switching the upper and lower power switches, the sub module capacitor C is either connected to the output port AB or bypassed, and the sub module output voltage v_{SM} will be equal to either the capacitor voltage v_C or 0. There are a total of six operating states for each Half-Bridge sub module as shown in Fig. 2.4 and Table. 2.1 depending on the switching states of T_1/D_1 and T_2/D_2 ('1' means ON and '0 means OFF) as well as the direction of the sub module current i_{SM}.
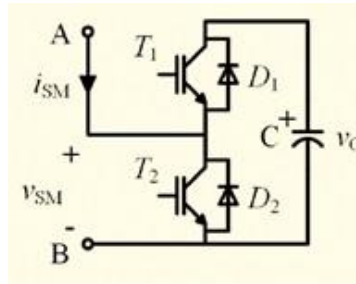
Fig. 2.3 Circuit diagram of a Half-Bridge sub module

- **"Sub Module blocked" – both switches are OFF**

In situations such as the system energizing, a fault, or dead bands between the upper and lower switches, both the upper and lower switches will be in an OFF-state. In such a case (State 1 or 2), the sub module output voltage can be either v_C or 0 depending on the direction of i_{SM}. For example, when the current flows into the sub module (from A to B), due to the blocked T_2, the current can only flow through D_1 and charge the capacitor, and v_{SM} out will be equal to v_C. When i_{SM} is negative, it will flow through D_2 and v_{SM} will be 0 (the ON-state voltage is neglected).

- **"Sub Module bypassed" – T1/D1 is OFF, T2/D2 is ON**

During normal operations, when the sub module is required to output '0' voltage (State 3 or 4), T_1/D_1 will be turned OFF and T_2/D_2 will be turned ON. The sub module capacitor will be always bypassed regardless of the direction of i_{SM}. Hence, States 3 and 4 are referred to as the sub module bypassed mode. More specifically, when i_{SM} flows into the sub module, since T_2 is turned ON, i_{SM} will flow through T_2 instead of the blocked D_1 by the forward-charged capacitor. When i_{SM} flows out of the sub module, the case will be the same as State 2 in that i_{SM} will flow through D_2 and v_{SM} will be 0.

- **"Sub Module switched-in" – T1/D1 is ON, T2/D2 is OFF**

When the sub module is required to output the sub module capacitor voltage v_C, T_1/D_1 will be turned ON and T_2/D_2 will be turned OFF. In such a case, the capacitor will always be switched into the arm circuit, being either charged or discharged depending on the direction of i_{SM}. Hence, States 5 and 6 are referred to as the sub module switched-in mode. More specifically, when i_{SM} flows into the sub module, since T_2 is OFF, the case is the same as State 1 in that i_{SM} will flow through D_1 and charge the capacitor. When i_{SM} flows out of the sub module, the capacitor will be discharged through T_1 and D_2 is blocked by the capacitor.

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Table. 2.1 Six operating states of a Half-Bridge sub module

State	Sub Module Status	Switching States $T_1\ T_2$	i_{SM}	v_{SM}	Conducting device	Capacitor state
1		0 0	in (A to B)	v_C	D_1	charging
2	Blocked	0 0	out (B to A)	0	D_2	bypassed
3		0 1	in (A to B)	0	T_2	bypassed
4	Bypassed	0 1	out (B to A)	0	D_2	bypassed
5		1 0	in (A to B)	v_C	D_1	charging
6	Switched-in	1 0	out (B to A)	v_C	T_1	discharging
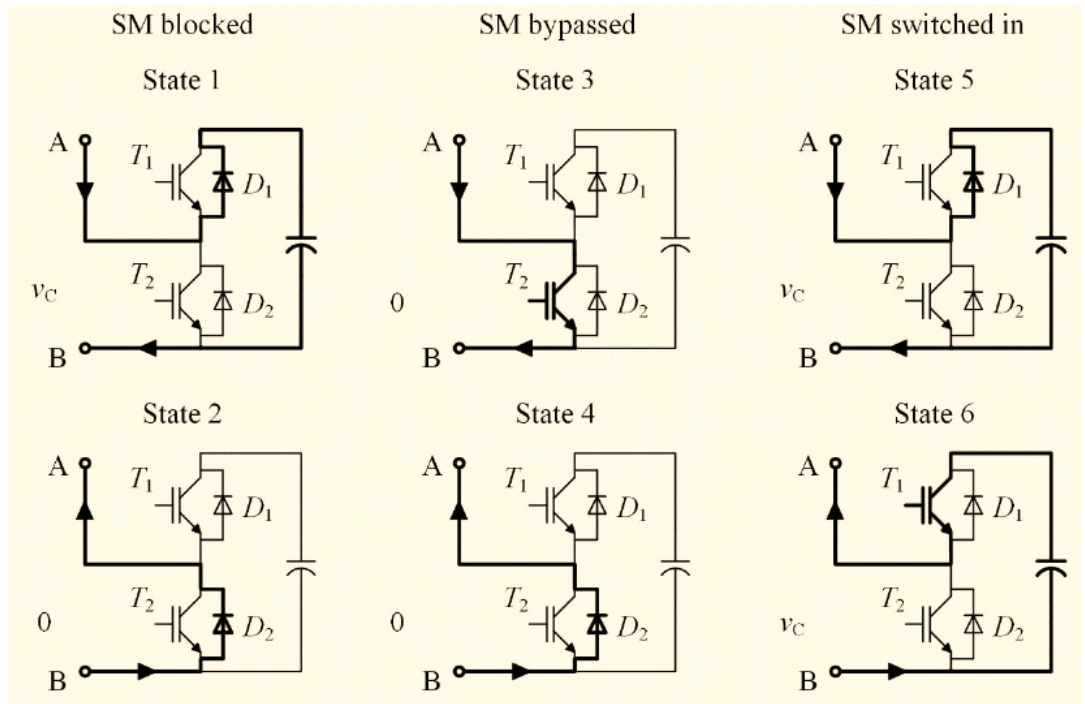
Fig. 2.4 Six operation states of a Half-Bridge sub module

2.1.2 Basic Operation Principles of Full-Bridge MMC

Fig. 2.5 shows the structure of a single Full-Bridge sub module, which includes 4 IGBTs (T_1, T_2, T_3, T_4), 4 anti-paralleled diodes (D_1, D_2, D_3, D_4), and a DC capacitor C_0.
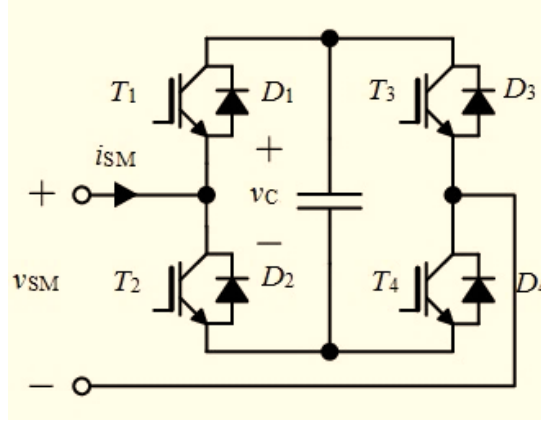
Fig. 2.5 Full-Bridge sub module structure

In normal operation, with T_1 and T_4 conducting, v_{SM} is equal to the capacitor voltage to v_C, and when T_2 and T_3 are on, v_{SM} is equal to -v_C, when T_1 and T_3, or T_2 and T_4 conduct, v_{SM} is equal to zero. Based on the above operation principle, the working states of Full-Bridge sub modules are classified into the following two modes:

- PLUS Mode: Full-Bridge sub module outputs v_C and 0 alternately.

- MINUS Mode: Full-Bridge sub module outputs -v_C and 0 alternately.

Supposing all the sub modules of Full-Bridge MMC work in PLUS mode, Full-Bridge MMC can work in the similar manner as Half-Bridge sub-module (HBSM), then their control methods and operation principles on steady states are nearly the same. However, Full-Bridge MMC needs about twice of the devices and losses compared with Half-Bridge MMC, which limits its industrial application to some extents. According to the characteristic that Full-Bridge sub module can work in MINUS mode, the peak value of the Full-Bridge MMC outputs phase voltage can be higher than its single pole DC voltage by modulation under the fixed DC voltage, thus the converter inputting current and its operational loss are reduced simultaneously [25].

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2.2 Mathematical Modelling of the Half-Bridge MMC

A schematic of a single-phase MMC with 10 SM feeding a RL load is shown in Fig. 2.6. The MMC is fed by a DC source with a constant DC voltage V_{dc}. There are two arms in the phase leg of the converter i.e., the upper arm which is denoted by subscript *"u"* and the lower arm which is denoted by subscript *"l"*. Each arm comprises of 5 series-connected identical Half-Bridge sub modules, and a series-connected inductor L. The resistor R represents the ohmic losses within the inductor L. the arm inductor suppresses high-frequency components in the arm currents, i.e., i_u and i_l . For this case, paralleling of the V_{dc} battery in shunt with the two $V_{dc}/2$ batteries doesn't have impact on the MMC operation but for the HVDC link it depends and the DC side circuit could be different.
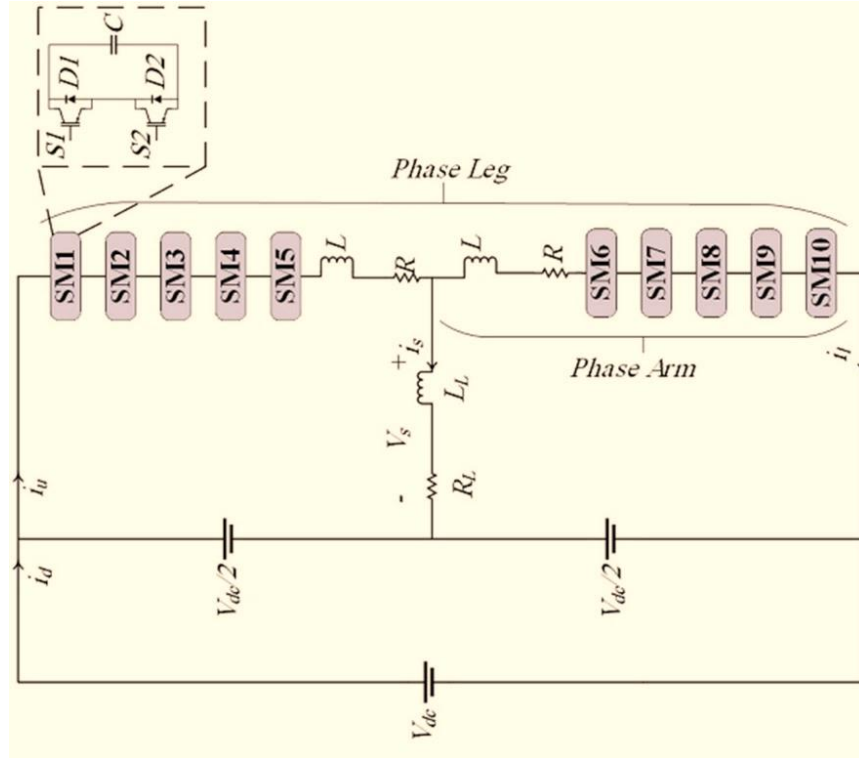
Fig. 2.6. Topology of a single-phase MMC with 10 sub modules [26]

In the MMC shown in Fig. 2.6, the upper and lower arm currents i.e., i_u and i_l are expressed as

$$i_u = \frac{i_s}{2} + i_c \quad \text{and} \quad i_l = -\frac{i_s}{2} + i_c \tag{2.1}$$

where i_s and i_c are the output and circulating currents, respectively. Therefore, the circulating current can be expressed by

$$i_c = \frac{i_u + i_l}{2} \tag{2.2}$$

Circulating current does not flow into the load but it increases the internal power losses and the amplitude of the capacitor voltage ripples. Hafeez et al [27], expressed the equations governing the dynamics of the upper and lower sum capacitor voltages as

$$\frac{C}{N}\frac{dv_{c,u}^{\Sigma}}{dt} = n_u(\frac{i_s}{2} + i_c) \tag{2.3}$$

$$\frac{C}{N}\frac{dv_{c,l}^{\Sigma}}{dt} = n_l(-\frac{i_s}{2} + i_c) \tag{2.4}$$

where C is the sub module capacitance, n_u and n_l are upper and lower arm insertion indices, $v_{c,u}^{\Sigma}$ and $v_{c,l}^{\Sigma}$ are the upper and lower arm sum capacitor voltages, respectively. The equations governing the dynamics of the output and circulating currents are expressed by (2.5) and (2.6), respectively.

$$(L_L + \frac{L}{2})\frac{di_s}{dt} = \frac{-n_u v_{c,u}^{\Sigma} + n_l v_{c,l}^{\Sigma}}{2} - (\frac{R}{2} + R_L)i_s \tag{2.5}$$

$$L\frac{di_c}{dt} = \frac{V_d}{2} - \frac{n_u v_{c,u}^{\Sigma} + n_l v_{c,l}^{\Sigma}}{2} - Ri_c \tag{2.6}$$

Where R_L and L_L are the load resistance and inductance, respectively. By using the equations (2.3)-(2.6), the mathematical model of the converter can be constructed as

$$\begin{pmatrix} \dfrac{di_s}{dt} \\[2mm] \dfrac{di_c}{dt} \\[2mm] \dfrac{dv_{c,u}^{\Sigma}}{dt} \\[2mm] \dfrac{dv_{c,l}^{\Sigma}}{dt} \end{pmatrix} = \begin{pmatrix} -\dfrac{R+2R_L}{L+2L_L} & 0 & -\dfrac{n_u}{L+2L_L} & \dfrac{n_l}{L+2L_L} \\[3mm] 0 & -\dfrac{R}{L} & -\dfrac{n_u}{2L} & -\dfrac{n_l}{2L} \\[3mm] \dfrac{N \times n_u}{2C} & \dfrac{N \times n_u}{C} & 0 & 0 \\[3mm] -\dfrac{N \times n_l}{2C} & \dfrac{N \times n_l}{C} & 0 & 0 \end{pmatrix} \begin{pmatrix} i_s \\[2mm] i_c \\[2mm] v_{c,u}^{\Sigma} \\[2mm] v_{c,l}^{\Sigma} \end{pmatrix} + \begin{pmatrix} 0 \\[2mm] \dfrac{V_d}{2L} \\[2mm] 0 \\[2mm] 0 \end{pmatrix} \qquad (2.7)$$

From the state space equations, it can clearly be seen that the variation of circulating current doesn't depend on the load current and has the DC offset value. The variation of the load current also is independent of the circulating current value.

2.3 Modulation Techniques of the MMC

The modulation techniques used for MMCs are considered extremely important since they are responsible for inserting and bypassing submodules, which means that they control the whole performance of the MMC. Many researchers have developed various types of switching algorithms for MMCs[28]; however, MMC modulation techniques can be divided into three main categories: reference signal-based, carrier-based, and nearest level modulation. The PWM methods fit neatly into these three categories listed. The following subsections illustrate the main idea behind each technique. Then, they show the selected technique to be used in the modelled MMC, explaining the reasons for this selection.

2.3.1 Direct Modulation

The simplest modulation scheme is the direct modulation, using an open-loop modulator based on a PWM approach [29]. The required arm voltages for each phase unit are used to derive two complementary sinusoidal reference waveforms as given by:

$$n_{arm\_pj} = N \frac{u^{*}_{arm\_pj}}{V_{dc}} \qquad (2.8)$$

$$n_{arm\_nj} = N \frac{u^*_{arm\_nj}}{V_{dc}} \tag{2.9}$$

where N is the number of sub modules in each arm. n_{arm_pj} and n_{arm_nj} are the reference waveforms, which are compared with the phase disposition (PD) carriers as shown in Fig. 2.7 to determine the number of sub modules to be inserted in the next control cycle. The direct modulation is very simple and robust. However, the resulting circulating currents are high, leading to an increased device rating and power losses [30].
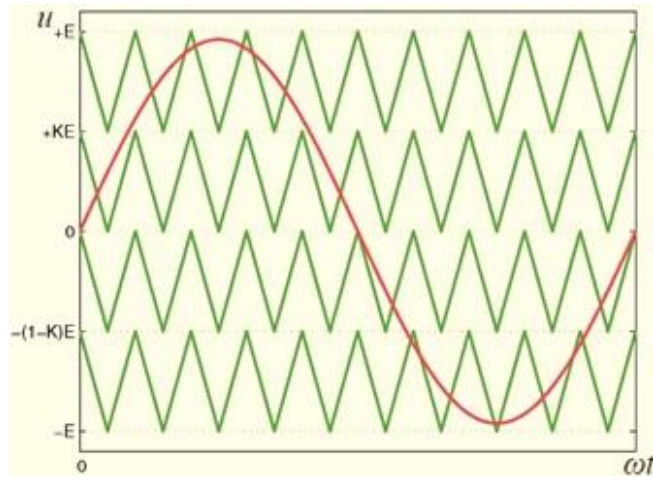
Fig. 2.7 Waveforms of phase disposition (PD) carriers

2.3.2 Nearest Level Control (NLC)

The nearest level control (NLC) can be categorized as direct modulation. It is emphasized here due to its effectiveness in the control of an MMC with a very large number of sub modules[31]. When compared with the direct modulation, PD carriers are no longer used. In the NLC scheme, the reference waveforms are directly sampled and the nearest integral value is taken as the number of inserted sub modules in the next control cycle. Due to the absence of PD carriers, the NLC is very fast especially with a very large number of sub modules. The main advantage of this method is its simplicity, as it can be implemented easily on industrial computers due to the small number of calculations. However, this switching algorithm suffers from a main drawback, which is

its relatively high harmonic content that makes it unsuitable for MMCs with a low or medium number of voltage levels [32]. Fig 2.8 shows the principle of NLM strategy.
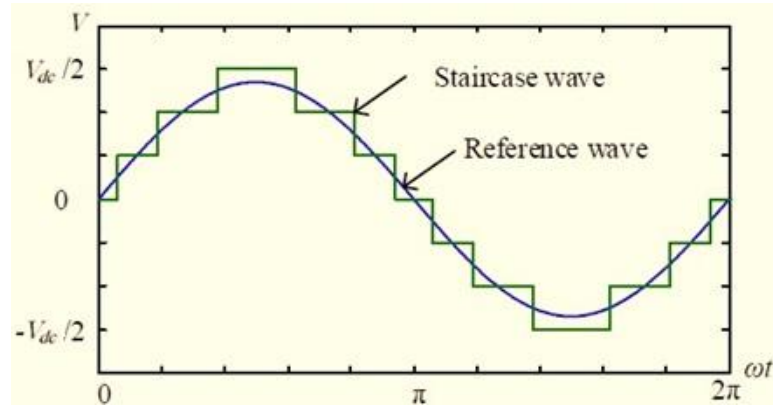
Fig. 2.8 Principle of NLM strategy [31]

2.3.3 Indirect Modulation

Indirect modulations can be further categorized into closed loop and open loop schemes. Indirect modulations can be further categorized into closed loop and open loop schemes. When compared with direct modulations, rather than using the nominal DC bus voltage to derive the reference waveform, the indirect approach uses the actual total capacitor voltage in each arm [33], which is either measured (closed loop) or estimated (open loop). The reference waveform is also compared with the PD carriers to decide on the number of sub modules to be inserted.

The indirect modulation allows sub modules to operate with their time average voltages being different from the natural equilibriums. Using this approach, the low AC output voltages can be achieved while maintaining the large number of voltage steps. Also, the controller allows the converter to operate with an imbalance in the energy strategies in different arms, when operating at low output frequencies or with a faulty sub module. When compared with the closed loop scheme, the main advantage of open loop indirect modulation is the substantial saving in communication resources since the capacitor voltage data does not have to be transmitted to the main controller. However,

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the major difficulty is the accurate estimation of parameters that are necessary to describe the system dynamics [34].

2.3.4 Phase-Shifted Carrier-Based PWM Technique (PSC-PWM)

One of the most attractive and widely used modulation schemes for MMCs is PSC-PWM. Lu et al [35] gives full details about the application of this method. To modulate the reference waveforms a carrier is used for each sub module. The phase shifts between these carriers determine harmonic characteristics of output voltage. So the phase shift between carriers of the sub modules of one arm should be 2π/N (N is the number of sub modules in each arm) incrementally to achieve best harmonic cancellation. The other phase shift in this method is the phase shift between sub-modules of upper and lower arms. By adjusting these phase shifts we will have two important modes of harmonic cancellation which are output voltage harmonics cancellation and circulating current harmonics cancellation. Based on the analysis that was done in [35] to get into the first mode (output voltage harmonic cancellation) the phase shift between carriers of upper and lower arms should be

$$\theta = \begin{cases} 0 & N \text{ is odd} \\ \dfrac{\pi}{N} & N \text{ is even} \end{cases}$$

(2.10)

And for second mode (circulating current harmonic cancellation)

$$\theta = \begin{cases} \dfrac{\pi}{N} & N \text{ is odd} \\ 0 & N \text{ is even} \end{cases}$$

(2.11)

For MMC with a great number of sub modules, the THD of the output voltage will be very low and no AC filters are needed. As a result, the harmonics of the circulating current become the main problem, which should be controlled at smaller magnitudes to reduce loss and the current stress [36].

2.3.5 Space Vector Modulation (SVM)

Space vector modulation (SVM) is commonly used in two-level VSCs. However, some researchers have proposed it for the switching of MMCs due to its attractive advantages [37]:

- Ability to be implemented digitally

- Reduction of the total harmonic distortion (THD) of output voltage and current waveforms

- Optimisation of switching sequences

Moreover, SVM for two-level VSC is extended to suit the N level MMC [38]. The possible switching states for an N level MMC is 2^{N-1}. It is obvious that the implementation process of the SVM technique is very complex due to the high number of switching states. This makes it not recommended for many MMC applications, especially those that have a high number of voltage levels. Table. 2.2 presents a comparison between the above-mentioned techniques from the point of view of complexity, output power quality and the natural balancing of capacitor voltages.

Table. 2.2 Comparison between different switching algorithms used for MMCs

Switching algorithm	Ease of implementation	Quality of output power	Natural balancing
Space vector modulation	Very complex	High	Good
Nearest level modulation	Simple	Low (particularly for low number of levels)	Bad
Phase shifted PWM	Moderate	Moderate	Acceptable

According to the table, the Phase-Shifted PWM method is selected to be used in the MMC model in this thesis due to the numerous advantages, such as the ease of implementation, the reduced losses due to the reduced switching frequency, and the stable performance during dynamic changes.

2.4 Sub Module Capacitor Voltage Balancing

Having series-connected submodules with unequal floating capacitor voltages cannot be accepted, as this condition will increase the differential current and thus, increasing the ripple content in the submodule capacitor voltages which means that the harmonics inside the DC-link voltage will be increased. Thus, capacitor voltages should follow a pre-defined reference signal. Moreover, these voltages should be balanced to lower the differential current and converter losses. Many strategies have been proposed in order to balance the voltages of the submodule capacitors by forcing the capacitor voltages to follow a desired value for the purpose of reducing ripples in these voltages, eliminating the AC components that are found in the differential current and enhancing the quality of the output power.

In normal operations, with certain modulation schemes such as the Phase-Shifted PWM, an additional sub module capacitor voltage balancing controller is required to balance and maintain the sub module capacitor voltage at a certain level. Various methods have been published to achieve this objective [39]. One common voltage balancing technique is based on a sorting algorithm [40].

Measurements of all sub module capacitor voltages as well as the arm current are needed for the sorting algorithm. In each control cycle, all sub module capacitor voltages will be recorded and sorted in ascending order. If the arm current is positive that charges the inserted sub module capacitors, the sub modules with the lowest capacitor voltages

will be switched in and charged. If the arm current is negative, the sub modules with the highest capacitor voltages will be switched in and discharged. With this approach, all sub module capacitor voltages in one arm will conform to each other.

The main drawback of the sorting algorithm is the resulting high switching frequency for each device. Even if the number of inserted sub modules in the two consecutive control cycles is the same, the sub modules may still be switched that the number of newly inserted sub modules equals the number of newly bypassed sub modules [41]. In order to solve this problem, Samajdar et al [17] proposed a modified sorting algorithm which reduces the switching frequency. In this method, the switching of the sub modules only occurs when the required number of inserted sub modules changes. Fig. 2.9 shows the operating principle of the reduced switching-frequency voltage balancing algorithm:

- If the newly required number of inserted sub modules (N_{on}) equals the number derived in the last control cycle (N_{on_old}), and ΔN_{on} is 0, then none of the sub modules will have their state changed.

- If extra sub modules need to be switched in during the next control cycle, and ΔN_{on} is positive, then no switching is required for those already inserted sub modules. The conventional sorting algorithm will only be applied to those currently bypassed sub modules.

- If some currently inserted sub modules need to be bypassed in the next control cycle, and ΔN_{on} is negative, no additional bypassed sub modules will be switched in. Only the currently inserted sub modules will be bypassed using the conventional sorting algorithm.

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$$\Delta N_{on} = N_{on} - N_{on\_old}$$

$\Delta N_{on} > 0$ $\Delta N_{on} < 0$

$\Delta N_{on} = 0$

Y $i_{arm} > 0$ N   Keep current gate signals   Y $i_{arm} > 0$ N

| Switch on $|\Delta N_{on}|$ SMs with the lowest voltages among ($N - N_{on\_old}$) off-state SMs | Switch on $|\Delta N_{on}|$ SMs with the highest voltages among ($N - N_{on\_old}$) off-state SMs | Switch off $|\Delta N_{on}|$ SMs with the highest voltages among N_{on_old} on-state SMs | Switch off $|\Delta N_{on}|$ SMs with the lowest voltages among N_{on_old} on-state SMs |
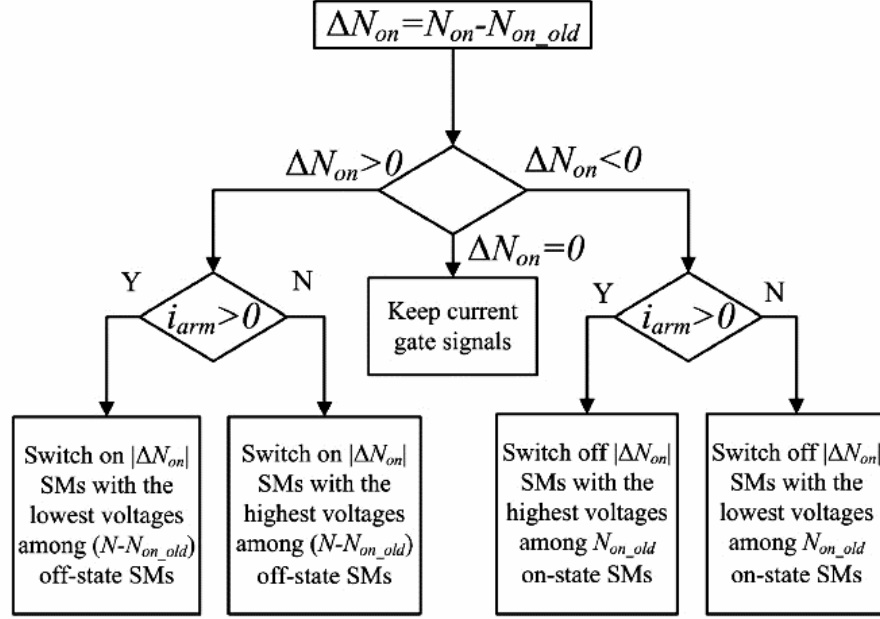
Fig. 2.9 Reduced switching-frequency voltage-balancing algorithm [42]

This method enhances the performance of the MMC since the converter losses are lowered due to the relatively low switching frequency. Moreover, there are no complex calculations or sophisticated PID control loops, which makes it simpler than other techniques. However, the ripples of capacitor voltages are increased due to the increased voltage bandwidth, which means that the differential current will be increased. Another drawback is that it still needs the measurement of each capacitor voltage.

All capacitor voltage balancing techniques have a common drawback, which is their need for capacitor voltage measurements. These measurements not only add many sensors but also require a high number of communication channels to transmit these signals. This has prompted the author to develop a new converter topology that does not depend on the measurement of submodule capacitor voltages and improves the converter reliability.

2.5 Design Considerations of MMCs

The following subsections show the design considerations of the MMC and the selection process of its parameters, particularly the procedure of selecting the sub module capacitor and arm inductor. It is important to mention that the sizing of these elements is very important for proper operation of the MMC.

2.5.1 Submodule Capacitance

The capacitance is calculated based on the energy variation inside the capacitor. Assume that the current passes through the capacitor is i_c and that the voltage across it is v_c. Then, the energy variation inside one capacitor during a period between t_1 and t_2 is:

$$\int_{t_1}^{t_2} v_c i_c dt = \frac{c(v_2^2 - v_1^2)}{2} \tag{2.12}$$

The capacitor voltage change is from v_1 and v_2. Since the MMC is formed from a series connection of sub modules, (2.12) can be applied for the whole arm instead of one sub module. The energy variation inside the upper arm (since both arms are identical) is [43]:

$$\Delta e_u = \int v_u i_u dt \tag{2.13}$$

Ignoring the power losses and the arm inductor voltages and assuming that output voltage v_o has a pure sinusoidal waveform, the voltage of the upper arm given in (2.14) can be rewritten as:

$$v_u = \frac{v_{dc}}{2} - v_o \tag{2.14}$$

The steady state representation of the output voltage and output current is given by:

$$v_o = \hat{V}_o \cos(\omega t) \tag{2.15}$$

$$i_o = \hat{I}_o \cos(\omega t - \varphi) \qquad (2.16)$$

Where $\hat{V}_o$ and $\hat{I}_o$ are the maximum values of the output voltage and output current, respectively. Since the power losses are ignored, the active output power can be expressed as:

$$P = \frac{\hat{V}_o \hat{I}_o \cos\varphi}{2} \qquad (2.17)$$

With the aid of (2.13) and (2.17), the energy variation of the arm as a function of the output active power can be expressed as:

$$\Delta e_u = \frac{v_{dc}}{\omega}(\frac{P}{\hat{V}_0 \cos\varphi})\sin(\omega t - \varphi) - \frac{P}{2\omega\cos\varphi}\sin(2\omega t - \varphi) - Pt \qquad (2.18)$$

Assuming that the allowable percentage of ripple is $k_{ripplemax}$, according to (2.18), the voltage will vary between v_c and $(1 + k_{ripple\,max})v_c$. The cell capacitance must be chosen such that the maximum value of the energy variation, $\Delta e_{p\,max}$, is smaller than this variation as per (2.19):

$$\Delta e_{p\,max} \leq \frac{NC_{sm}v_C^2((1 + k_{ripple\,max})^2 - 1)}{2} \qquad (2.19)$$

After rearranging (2.19), the value of the capacitor, C_{sm}, must satisfy the following:

$$C_{sm} \geq \frac{2\Delta e_{p\,max}}{Nv_c^2(1 + k_{ripple\,max})^2} \qquad (2.20)$$

2.5.2 Arm inductance

Arm inductors play a valuable role in the MMC, for limiting the differential and transient currents [44]. They also help in the correction of the total reactance of the system. Thus, the size of arm inductors should be carefully selected to limit DC fault currents to a value that is by far lower than the rating of the MMC IGBT switches [45]. To facilitate the estimation of differential current ripples, the maximum voltage across the arm is assumed

to be equal to the submodule capacitor voltage. Additionally, the average value for changing the switching states is assumed to be $\frac{T_s}{2N}$ where T_s is the switching cycle of the IGBT. In this case, the peak-to-peak ripples imposed in the differential current can be calculated according to:

$$\Delta_{idiff} = \frac{v_c T_s}{4NL_{arm}} \tag{2.21}$$

Each arm inductor is subjected to half of the peak-to-peak ripples. In this case, after rearranging (2.21), the arm inductor should be selected according to:

$$L_{arm} \geq \frac{v_c T_S}{8N \, \Delta i_{diff}} \tag{2.22}$$

2.6 Sub Module Capacitor Size and Ripple

The sub-module capacitor size makes a large contribution to the overall MMC weight and size and it is important to consider the ripple current of the capacitors in terms of lifetime of the capacitor when the capacitor with the large capacity such as an electrolytic capacitor is applied. Sub module capacitor design is the important issue and there is always trade-off between the sub module capacitor size and ripple. The sub module capacitor is typically selected to regulate the sub module voltage ripple below 10%. So, the sub module capacitance must be sized to ensure that the resulting voltage ripple is held to an acceptable level.

The sub module capacitor size is the main obstacle for the MMC to be used in some medium voltage applications. In the current designs of an MMC sub module (SM), the reservoir capacitor needs to absorb low-order harmonics and hence accounts for over 50% of the total size and 80% of weight. Merlin et al [43] proposes a mathematical model considering the energy deviation for the stacks of MMC. This paper also presents the

minimum sub capacitor design for MMC which meets maximum voltage deviation criterion under ideal conditions. The selection of sub module capacitor for MMC has been discussed in [46] which uses computational procedure and a set of curves to assist the capacitor selection. Important factors to choose the capacitor are maximum capacitor voltage, capacitor voltage ripple, sub module voltage capability and capacitor ripple current stress. Tang et al [47] introduces the new control strategy with a low-capacitance sub module operating at high capacitor voltage ripples. Zhao et al [48] proposes the capacitor dimensioning for full bridge sub module MMC considering zero sequence voltage injection. Reducing the cell capacitor size of full bridge sub module MMC is investigated in [49] which uses the zero sequence voltage injection method. According to the current literature, the methods for reducing capacitor ripples can be classified into two distinct categories. The first one consists of injecting specific harmonics within the circulating current [50-52]. These methods can attenuate ripples caused by converter output voltage and current (second order) effectively. Another strategy is to inject a high-frequency signal in circulating currents while injecting the same frequency harmonic to the converter output common mode voltage [53-56].

Yang et al [57] proposes a new asymmetric operation control strategy to address the issue of DC-link voltage influence on capacitor ripples. Reference [58] introduces a new MMC topology to reduce capacitor voltage fluctuations with fewer sub modules compared with the traditional MMC. Reduction of switching losses has been investigated in [59] which uses a new modulation technique. Yang et al [60] applies a decoupled current control with synchronous frequency damping for MMC in order to improve MMC dynamic performance. As a result, by using the proposed control and appropriate damping index, the low overshoot currents and fast step response time can be obtained. Application of the new sub module topology (flying capacitor sub modules) in order to

reduce the magnitude of circulating currents, voltage ripple, and footprint size as well as the efficiency improvement of MMC has been presented in [61].

In this research by increasing the capacitance of the sub module capacitors during the switching period, sub module voltage fluctuations and ripples will be eliminated. This is achieved by connecting idle capacitors in a parallel connection with conducting capacitors, hence the sub module capacitor size of MMC will be decreased. Consequently, the MMC will be able to work at lower switching frequencies without needing any large sub module capacitors. However, this target will be achieved with cost of some additional switches in the proposed design.

2.7 Challenge of Switch Count and Losses with Proposing New Sub-Module Topology

Reference [62] introduces a new three-level flying capacitor (3L-FC) sub module topology. Using this topology overcomes the zero/low-fundamental-frequency operation issues of conventional MMC without injecting common-mode voltage. However, the flying capacitor MMC suffers from high current stress due to the large amplitude of inner high-frequency current. Dekka et al [62] investigates the equivalent LC circuit in flying capacitor MMC, and proposes a control method to improve the performance of inner current control. Accordingly, the desired square wave is achieved for inner high-frequency current. Fig 2.10 shows the schematic of MMC with 3L-FC sub module.
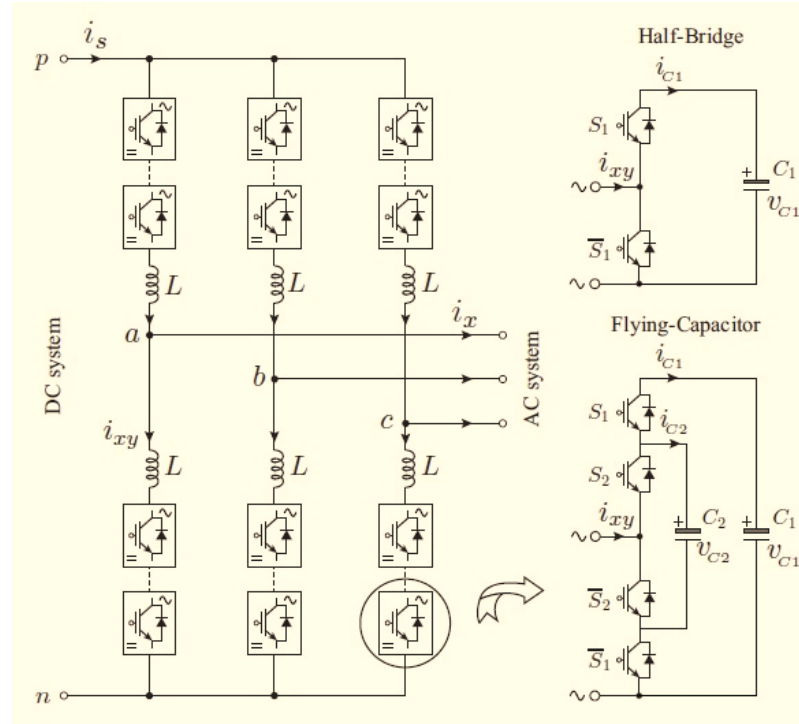
Fig. 2.10 MMC with 3L-FC submodule [62]

Paper [63] introduces a modified topology for flying capacitor multi cell converters (FCMCs). This topology has been shown in Fig. 2.11. Decreased number and voltage rating of the required DC voltage sources are the main advantages of the modified FCMC in comparison with the conventional topology.
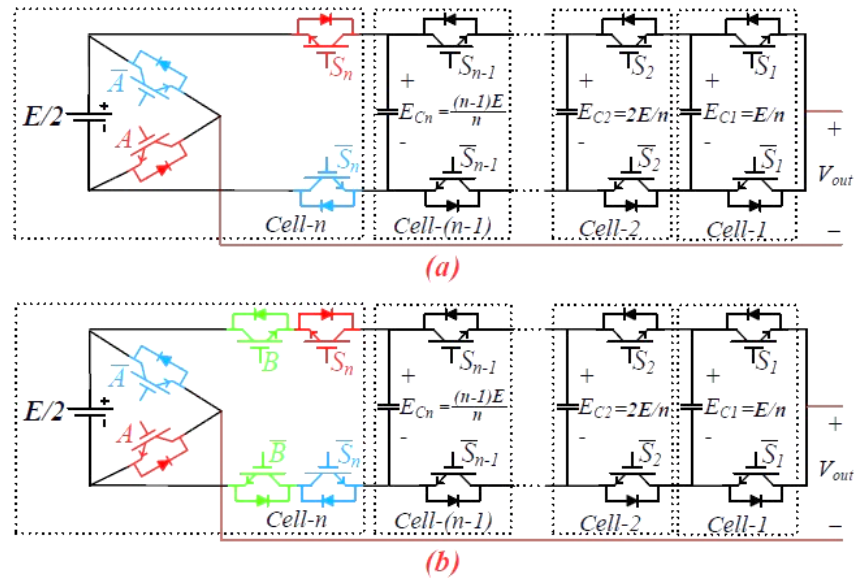
Fig. 2.11 Sub multilevel module of n-cell-n+1-level modified FCMC based on only one DC voltage source with maximum peak-to-peak voltage of E. (a) First design (b) Second design [63]

The control strategy for the modified FCMC is based on the PS-PWM technique; therefore, the natural balancing phenomenon of the flying-capacitor voltages which is one of the critical and crucial advantages of the FCMCs, is preserved in the sub multilevel module. Despite all the advantages of FCMCs, their main practical issue roots in a significant diversity in the voltage rating of flying capacitors whenever the high number of voltage levels is required. To suppress this issue, this paper proposes a cascade connection of the aforementioned sub multi-level modules to structure the modular multilevel converters (MMCs) to have more modular configuration.

Zhang et al [64] introduces a new type of self-blocking composite multilevel sub module topology (CSM) which has been shown in Fig. 2.12. The proposed topology's voltage output feature and its DC fault suppression characteristics in different blocking modes are also analysed in this paper.
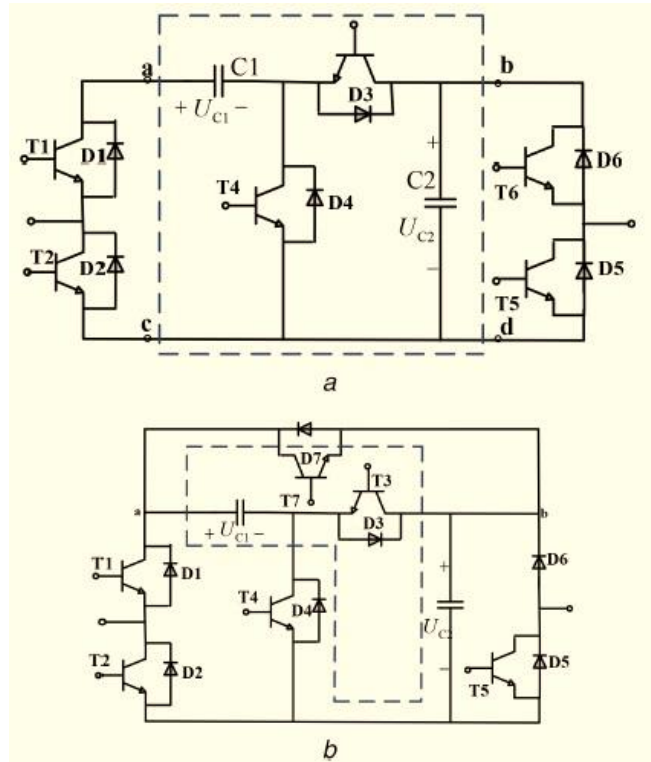
Fig. 2.12 Proposed self-blocking composite multilevel sub module topology (CSM topology) [64]

Adam et al [65] presents a new sub module topology with lower total semiconductor losses. Continuous operation of the MMC during sub module failures without the need for a mechanical bypass switch is the other advantage of this topology. The overview of different sub module topologies is shown in Fig. 2.13. This paper also investigates the use of the three-level neutral point clamped unipolar cell as a sub module.
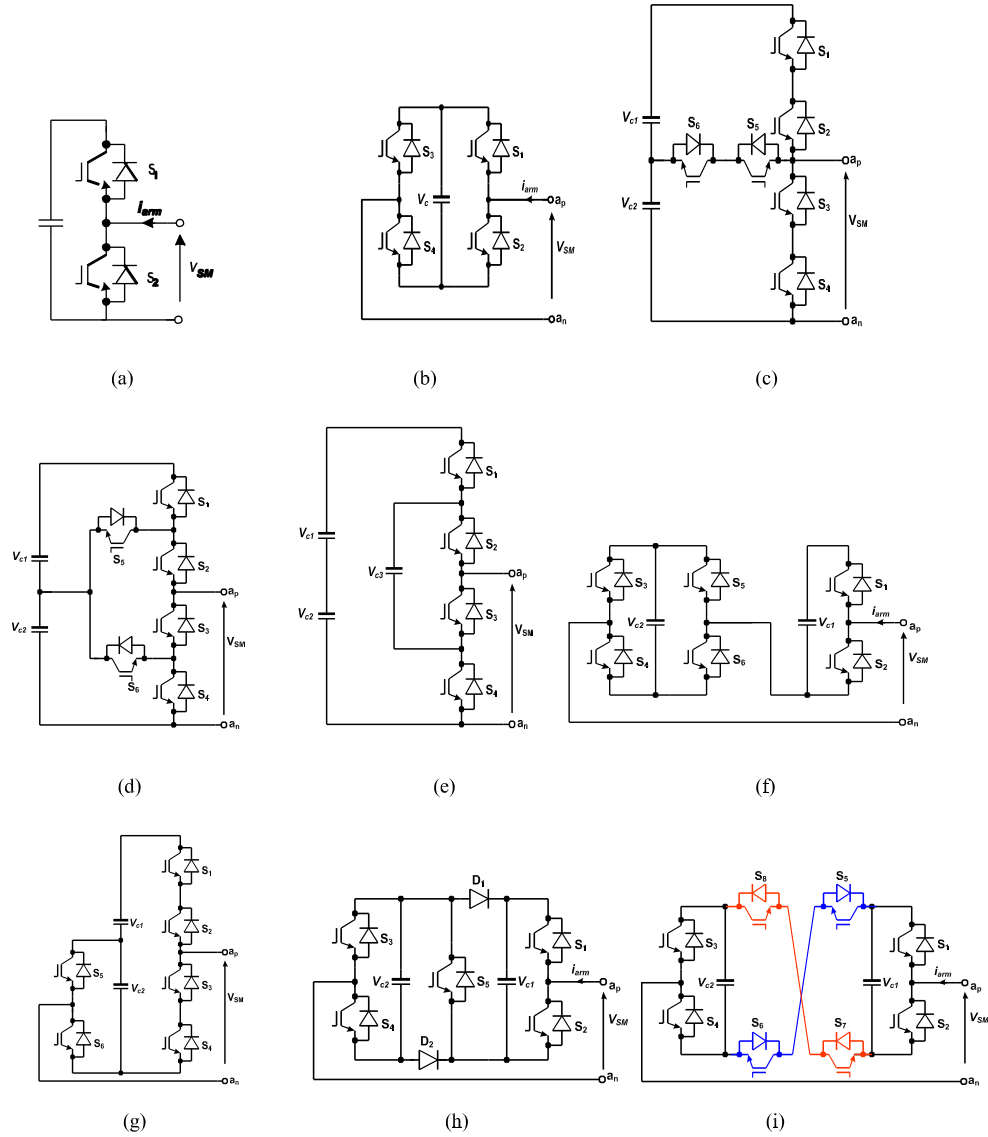
Fig. 2.13 Some of the known cell configurations for modular and hybrid multilevel converters. (a) Two-level half-bridge unipolar cell. (b) Three-level full-bridge symmetrical bipolar cell. (c) Three-level T-type unipolar cell. (d) Three-level neutral-point clamped unipolar cell. I Three-level flying capacitor unipolar cell. (f) Four-level asymmetric bipolar hybrid cell. (g) Four-level asymmetric bipolar cell. (h) Three-level asymmetric doubled clamped bipolar cell. (i) five-level symmetrical cross-connected bipolar cell [65]

Reference [66] presents a new hybrid modular multilevel converter for interfacing a full-scale, permanent magnet synchronous generator (PMSG)-based direct-drive variable-speed wind energy conversion system (WECS). The proposed hybrid converter, which is used on the grid side of the system, consists of a three-level modular multilevel converter (MMC) in series connection with three H-bridge modules. The generator-side converter is based on a conventional three-level neutral-point-clamped converter. The proposed hybrid converter, as opposed to the existing full-scale multilevel converter-based wind energy systems, provides structural modularity and a higher dc-bus voltage utilization.

The half-bridge sub-module (HBSM) does not have the capability to clear the DC fault current. Based on the analysis of DC fault current path, Wang et al [67] proposes a novel MMC sub-module topology with DC fault blocking capability. It uses a bidirectional switch and two diodes. This topology has been shown in Fig. 2.14.
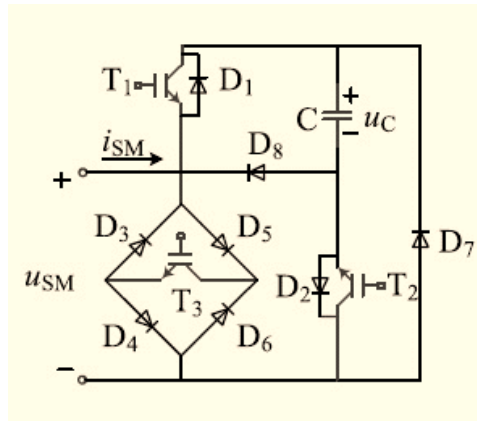
Fig. 2.14 The DCBSSM topology [67]

There is always trade-off between the switching frequency and sub module voltage ripple in MMC structures. Ilves et al [68] introduces the new sub module topology which has the capability to improve the balancing of the capacitor voltages at low switching frequencies. Qin et al [69] proposes two new sub module circuits as well as a hybrid design methodology to embed the DC-fault-handling capability in the MMC (Fig. 2.15).

Based on the hybrid design method, by replacing a number of half-bridge sub modules of the MMC system with those sub modules with the DC-fault-handling capability, the DC-fault-handling capability can be embedded without changing the control/modulation methods. In the proposed hybrid MMC configuration, any DC-side short-circuit fault is interrupted by blocking all of the switching devices of the sub modules within a fraction of a second. Based on the proposed design concept, the MMCs with variants of sub modules are investigated and compared in terms of their semiconductor device requirements and power losses.
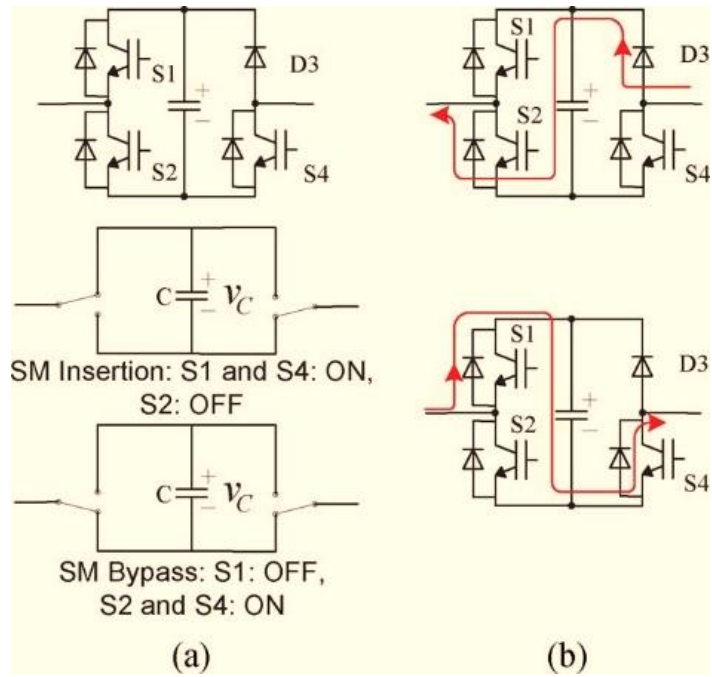
Fig. 2.15 Proposed unipolar voltage full-bridge SM circuit: (a) normal operation and (b) its current path when all switches are turned off [69]
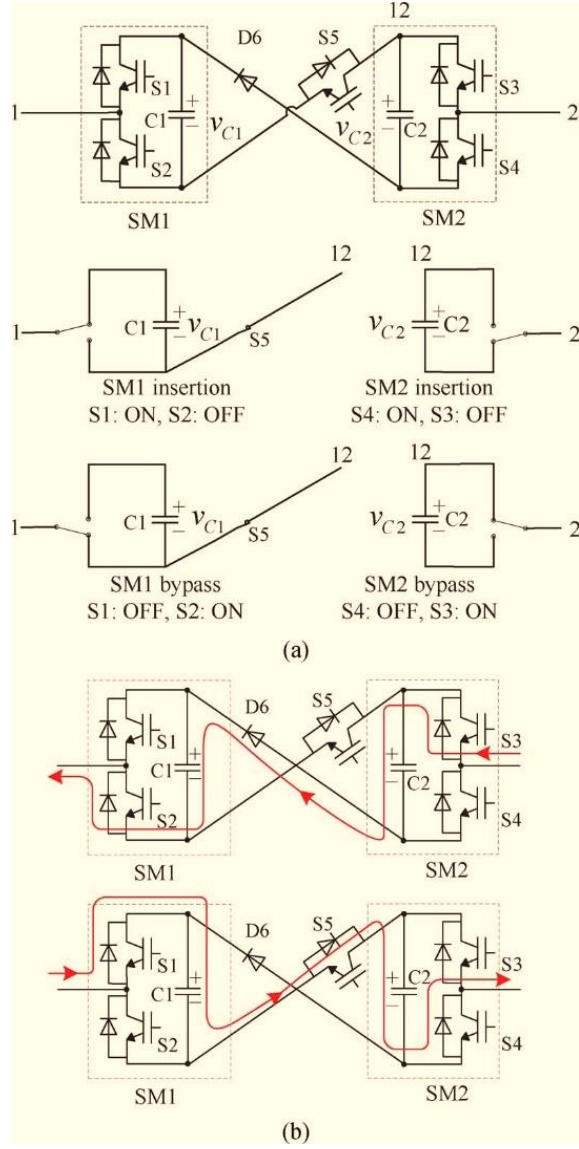
Fig. 2.16 Proposed three-level cross-connected SM circuit: (a) normal operation and (b) its current path

when all switches are turned off [69]

The semi-full-bridge sub modules topology is introduced in [70] which allows two

capacitors to be connected in parallel with both positive as well as negative polarity.
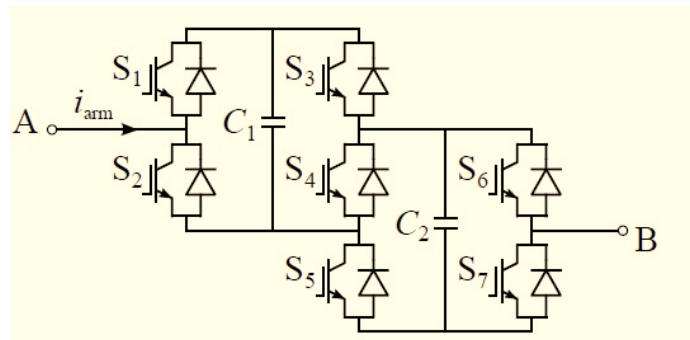
Fig. 2.17 Proposed semi-full-bridge-sub module [70]

The other new sub module topology has been presented in [71] which has DC-fault current blocking capability as well as a lower cost and power loss (Fig. 2.18).
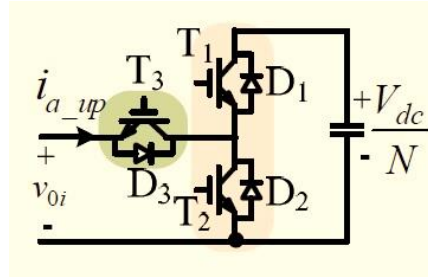
Fig. 2.18 New topology of sub module in the MMC [71]

Elserougi et al [72] proposes a new switched capacitor sub module (SCSM) for MMCs which has the DC fault blocking capability (Fig. 2.19). It has the advantage of less number of components and less complexity. However, considering these advantages, the proposed structure uses high number of components and has significant losses.
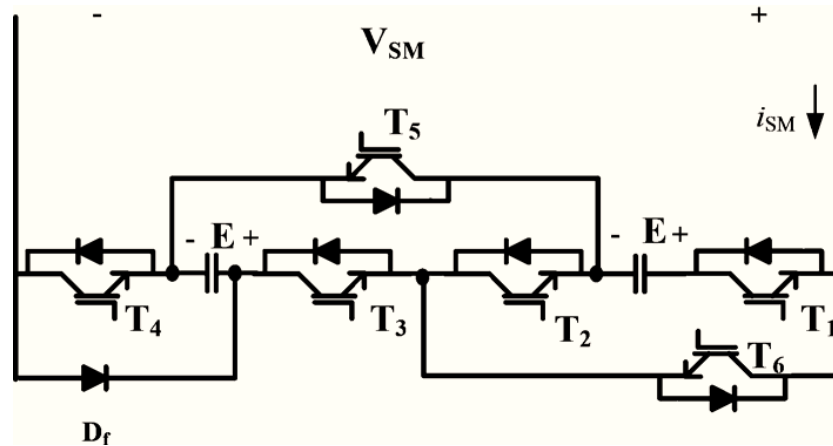
Fig. 2.19 Proposed switched capacitor sub module (SCSM) [72]

A modified modular multilevel inverter with sub module voltage suppression presented in [73]. In this paper, a power decoupling circuit is added to the conventional sub module topology, so that the fundamental frequency voltage fluctuation is eliminated at the sub module level. A circulating current-based closed-loop control system is then employed to eliminate the remaining second-order fluctuation.

Li et al [74] introduces an enhanced MMC topology with DC fault ride-through capability (Fig. 2.20). By employing the proposed diode clamp sub-module, the diode freewheeling effect can be eliminated, and the fault current can be extinguished. Then by de blocking additional IGBTs, MMC can rebuild the DC link voltage and can immediately and automatically resume normal power transmission for non-permanent faults. Employing the diode clamp sub-module structure, the required rated voltage of additional semiconductors is half that of conventional Semiconductors, resulting in low device cost.
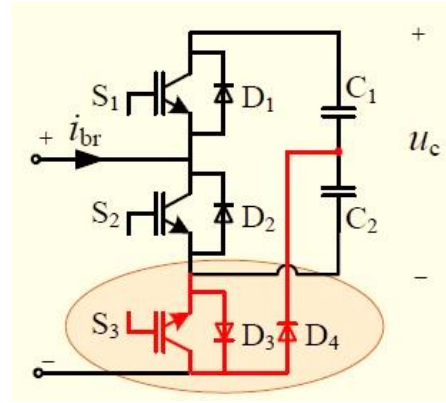
Fig. 2.20 Diode clamp sub module [74]

A novel double-zero sub module topology is investigated in [75]. This topology which is called (DC-DZ-SM) has less losses (Fig. 2.21).
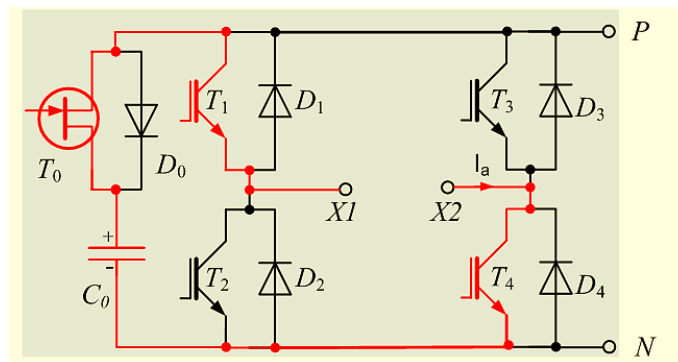
Fig. 2.21 Novel Double-Zero sub module [75]

Sallam et al [76] proposes the other new sub module topology with advantage of decreasing voltage ripples and improving the utilization of the capacitors.

From the different topologies that have been discussed it is clear that the number of MMC switches and losses are challenging issues in MMC design and research into the most appropriate sub module topology design is ongoing. Complexity of the sub module voltage control and the sub module capacitor size are the other challenges. The design topology proposed in this work has the advantage of operation at a lower switching frequency without the need for the large sub module capacitors. Operation at a low switching frequency will decrease the losses and improves the converter efficiency. Moreover, the control of the sub module voltage is not complicated.

2.8 Circulating Currents: The Challenge of Suppressing with Different Control Methods

The circulating currents occur mainly due to the fluctuations in the capacitor voltages in the Sub Modules (SMs) of the MMC. Imbalances between the upper and lower arm voltages give rise to a current comprising mainly low, even multiples harmonic components of the fundamental frequency. This current is termed the circulating current and it circulates within each phase of the converter, not affecting the output voltage and current. If the current is not properly controlled, it will increase the peak and RMS values of the phase arm currents, consequently increasing converter power losses and affecting lifetime and reliability of power switches and passive components. The phenomenon of circulating arm currents is investigated in [77]. As the current is sinusoidal in nature and comprising several, low order harmonics, this pose additional challenges of the selected control algorithms [78].

There are different control methods to suppress and eliminate circulating currents. Suppression of the second order harmonic in the circulating current is a critical issue and presence of the second harmonic will increase the losses and current-rating requirements of the converter. Jiang et al [79], investigates about the second-order harmonic injection

method to minimize circulating currents and converter losses. The conventional methods of eliminating second-order harmonic of the arm current are proposed in [80]. Marín-Hurtado et al [81] compares PIR and MPC (Model Predictive) based controllers for circulating current suppression in MMC. Li et al [82] investigates a control method which considers each component of circulating currents under the unbalanced voltage. There is the other control method to suppress circulating current under unbalanced grid conditions which uses proportional resonant controller strategy [83, 84]. In paper [85], a differential-based positive and negative sequence separation control method is proposed, which has limited delay and high precision after grid asymmetry occurring. A modified circulating current suppressing strategy including two controllers with a fixed-band sub module (SM) state transition principle is presented in [86]. Wang et al [87] introduces the on-line calculation method to inject reference voltages for circulating current elimination. In this method, there is no need for an extensive lookup table as well as the detection of the output current amplitude and phase. An even-harmonic repetitive control scheme that incorporates half-delayed control cycle to suppress the even-order harmonics in the differential current of an MMC has been introduced in [88]. Paper [77] applies a second harmonic capacitor voltage eliminating controller (SHCVEC) for capacitor voltage fluctuation suppression. Compared to the passive circulating current suppression method, the active control method doesn't bring additional hardware cost. But the main defect for the active circulating current suppression method is consumption of a certain amount of MMC voltage which means the maximum available output voltage as well as the power capacity of MMC has to be curtailed. In paper [89], by exploring the characteristic of sub module output voltage, it is discovered that, a second-order voltage component appears in both full-bridge sub modules and half-bridge sub modules with the opposite phase

angle when the modulation index is larger than 1. As a result, the second order circulating current is employed as a novel control freedom to balance the capacitor voltage [90].

The arm inductor is a key component in MMC design and for HVDC application, the MMC arm inductance is selected based on the circulating current suppression and DC fault current limiting requirements. Deng et al [91] develops the theoretical relationship between the arm inductance and switching frequency of the circulating current, which can be used to guide the arm inductance selection. Zhou et al [92] uses model predictive control to minimize circulating current. It works based on a normalized cost function to select the inverter switching patterns, which control the load current, while minimizing voltage fluctuation and circulating current. The weighting factors were selected based on minimizing the load-current total harmonic distortion (THD) and circulating current.

1) Methods Based on Energy Control

In paper [93], a method based on total energy control and energy balancing control between upper and lower arms is proposed. In this method, the voltages of SMs are needed to be measured consistently, which will be a problem if the number of SMs are increased.

2) Method Based on Double Line-frequency d-q Coordinate

In [94], a circulating current suppressing control (CCSC) method is proposed based on the theory that the circulating current is in the form of negative sequence with double line frequency, besides the DC component. Circulating current can be controlled directly by difference voltage. Thus two PI controllers can be used on d and q directions. The output of the controller V_{diff_ref} will be subtracted from both upper and lower arm voltage reference as shown in Fig. 2.22. Contrary to the existing circulating current controllers, the proposed approach does not rely on any mathematical approximate/inaccurate model

to design the controller. Instead, it takes an experimentally identified nonparametric model of the system to design the controller.
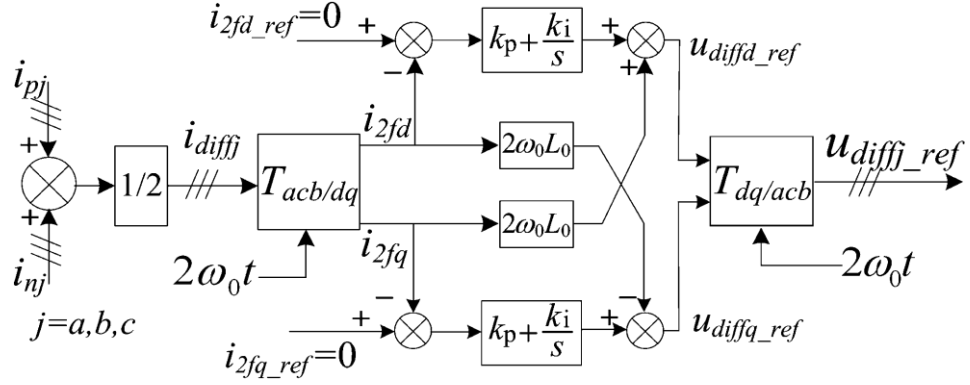
Fig. 2.22 Control diagram of the method based on double line-frequency d-q coordinate [94]

3) Method Based on Model Predictive Current Control

In [81], a method based on model predictive current controller is proposed. . Using the properly selected weighting factors, this method has shown an efficient and stable tracking of the reference current at steady-state and fast transient response. It is also capable of maintaining the capacitor voltages at their preselected and desired levels while minimizing the circulating current.

4) Methods Based on PR controller and Repetitive Controller

Rødal et al [95] investigates about using the PR controller in the circulating current suppressing. The PR controller is used because there are not only double line frequency components in the circulating current, but also even harmonics i.e. components with forth, sixth fundamental frequency. PR controller can achieve high gain at the resonant frequency, so that the components with known frequency can be regulated well. In this case, based on the pre-introduced control algorithms, several parallel connected PR controllers are used to eliminate the higher order harmonics in the circulating current.

The repetitive controller is used to eliminate the multiple harmonics in the circulating current. In [96], repetitive-plus-PI control scheme is proposed and the control diagram is shown in Fig. 2.23 (i_{zx} is circulating current). These linear controllers are based on the pole placement control design method. The major disadvantage for these controllers is that these solutions are not guaranteed to be optimal.
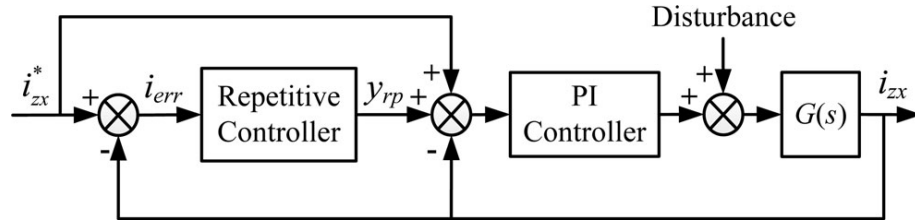
Fig. 2.23 Diagram of repetitive-plus-PI control [96]

In order to overcome the problems associated with MMC, particular attention was provided to the form and function of MMC with new design, control and harmonic mitigation schemes. In conclusion this section addresses the problem of circulating current reduction and attempts to make a detailed analysis with different control methods. The objective of this research is to propose and demonstrate the operation of a new topology for the MMC that utilizes the pulse-width modulation (PWM) switching states to use the idle capacitors during a low switching frequency period. The control acts directly on elimination of the sub module voltage ripple by increasing the sub module capacitor value and eliminates the need of big capacitors for the MMC. Consequently, the amount of the circulating current will be the same as the higher switching frequency condition with classic design (classic half-bridge sub module topology) and will not be increased because of a low switching frequency.

2.9 Challenge of DC fault and fault protection of DC grid based on hybrid MMC

Xiang et al [97] investigates about a new fault identification method based on wavelet transform. The response of an MMC-HVDC converter during grid faults also is discussed in [98]. Wang et al [99] proposes the use of hybrid DC CBs and a new RL-FCL branch that ensures the continuous operation of the healthy parts of MTDC systems under DC faults. Lin et al [100] proposes a PTG (pole to ground) fault ride through strategy for low impedance grounded radial multi-terminal HVDC systems. It is realised by the coordinated operation between half/full-bridge hybrid modular multilevel converters and mechanical DC switches. In [101] the system transient characteristics are investigated involving permanent line-to-ground faults (LGFs), permanent short-circuit faults (SCFs), temporary LGFs, and temporary SCFs with either AC circuit breakers (ACCBs) or DC circuit breakers (DCCBs) in service. Finally, the performances, including the fault clearance and recovery, comparison of DCCBs with two different breaking methods, and comparison of ACCBs and DCCBs, in the MMC-HVDC system are presented.

Li et al [102] investigates the development process of the fault and studies the analytical method of pole-to-pole DC fault in the MMC-MVDC system. Before the MMC is blocked, the discharging process is influenced by the AC system and the switching of the sub modules. The equivalent circuit model proposed in this paper can be used to solve the fault current at the AC side, DC side and in the bridge arms precisely. The equivalent circuit of the converter after blocking is an uncontrolled rectifier. The process could be divided into three stages including all diodes on stage, transitional stage and steady uncontrolled rectifier stage according to the state of diodes and transient characteristics of DC fault current. Kontos et al [103] studies the DC fault phenomena in a point-to-point multilevel modular converters. Lu et al [104] focuses on the discharge

problem on HBSMs' capacitor when hybrid MMC based HVDC systems riding through a long-term (e.g., several minutes or longer) pole-to-ground (PTG) fault condition. This paper also analyses the PTG fault characteristics. Moreover, a coordinate control of HBSMs' and FBSMs' output voltages is also proposed to achieve a quick and accurate HBSMs' capacitor voltage balancing. For bipolar schemes with a dedicated metallic return (DMR) conductor, discrimination of pole–ground faults and pole–DMR faults represents a challenging task due to their similar electrical characteristics. In paper [105], several approaches to detect DMR fault involvement are identified and analysed, comprising both non-invasive methods based on measurement data and invasive methods based on DC current control strategies of full-bridge VSC-MMC stations. The fault-tolerant control of MMC based on the carrier phase shift modulation has been proposed in [106].

Yu et al [107] proposes a novel bipolar modular multilevel converter (MMC) topology with DC fault ride-through capability. The proposed bipolar MMC topology is a hybrid of two types of arms: the half-bridge sub module (HBSM)-based arms (HBSM-arms) which are connected to the ground pole, and the unipolar-voltage full-bridge sub module (UFBSM)-based arms (UFBSM-arms) which are connected to the positive or negative pole. During a pole-to-ground or pole-to-pole DC fault, the hybrid-arm design offers the proposed UFBSM-based hybrid-arm bipolar MMC (UHA-BMMC) the capability to provide additional reactive power to support the AC grid while blocking the DC fault current. In [108] an enhanced control for HVDC system during asymmetrical DC voltage faults has been proposed. A new control variable is proposed on the arm voltages to distribute the power transmitted from the AC side between the upper and lower arms. By adopting the enhanced control, the overvoltage and the fault current can be eliminated when a PTG fault occurs.

Langwasser et al [109] introduces a fault current estimation method in MMC-based multi-terminal DC (MTDC) grids, which improves the current differential equation based methodologies including the dynamics of power and DC voltage controllers. The proposed method gives the possibility of analysing the fault current under different grid conditions (e.g., fault resistance and limiting inductor value). In view of the relationships among AC/DC voltages and currents in full-bridge-based MMC with the negative voltage state, Zeng et al [110] provides an analytical study to find a relation between capacitor voltage variation and the maximum modulation index. In paper [111], a hybrid MMC topology has been studied during the DC fault condition and restoration method is presented for a cost-effective DC fault protection solution for MMC-based MVDC systems. Serrano-Sillero et al [112] mainly discusses the impacts of three MMC-HVDC configurations on AC system stability under DC line faults. The first configuration is half bridge sub-module based MMC (H-MMC) HVDC configuration, which clears DC line faults by tripping the AC circuit breakers. The clamp double sub-module (CDSM) based MMC (C-MMC) HVDC configuration with DC line fault clearance ability constitutes the second configuration. A line-commutated converter (LCC) and MMC hybrid HVDC configuration with DC line fault clearance ability, named LCC-diode-MMC (LCC-D-MMC), is the third configuration. Ma et al [113] proposes a novel DC fault current-limiting scheme which uses a current-limiting resistance and dozens of serial controllable power electronics in parallel with the current-limiting resistance. The current-limiting resistance is designed to reduce the DC fault current and the requirement for the direct current circuit breaker (DCCB) capacity. Yang et al [114] proposes an improved quasi reverse blocking modular multilevel converter (QRB-MMC) with DC fault handling capability for HVDC applications. Different from the existing HBSM-MMC, QRBSMs and current limit modules (CLMs) are employed as the basic building blocks. Based on

analysis of the operation principles and the fault current blocking mechanisms, this paper verifies the feasibility and dynamic performance of QRB-MMC. Simulation results show that QRB-MMC is able to block the DC fault current effectively with the help of inverse voltage across the series-connected auxiliary snubber capacitors.

Paper [106] proposes an alternative sub module configuration of the MMC based on a carrier-phase-shift PWM scheme, which is easily implemented for switching the operation modes of the MMC from normal condition to fault-tolerant control. The arms of the proposed MMC are configured by typical half-bridge sub modules (HBSM) and suggested series-connected triple SMs (SCTSM) in interleaving series, where the SCTSM is composed of three HBSMs connected in series through an additional IGBT and a clamp diode. With the additional IGBTs and diodes, the SCTSMs can produce bipolar output voltages and the MMC can be restructured to operate as three-phase cascaded multilevel converter during pole-to-pole short circuits to control the converter currents. In addition, the cost and power loss of the proposed MMC are lower than those of the existing MMCs based on full-bridge SMs (FBSM), a hybrid of HBSMs and FBSMs, and clamp-double SMs. In paper [115], clearing of DC faults in a hybrid multi-terminal HVDC transmission system consisting of line commutated converters (LCCs) and voltage source converters (VSCs) is implemented and using the half-bridge modular multilevel converter (MMC) technology is investigated. The proposed DC fault recovery strategy demonstrates fast fault recovery performance.

Deng et al [116] presents a new control scheme that permits the H-bridge MMC to exchange active and reactive powers with the AC grid when operating in boost and buck modes (with the DC-link voltage varied over a wide range). This feature means the H-bridge MMC operated with the proposed control scheme is a suitable candidate for grid integration of large-scale solar farms, without the need of an intermediate DC/DC

converter, as normally used for maximum power point tracking. In addition, the presented control scheme enables the H-bridge MMC to ride-through DC faults without a converter blocking. Li et al [117] analyses the characteristics of valve-side single-phase-to-ground (SPG) faults in three configurations of MMC systems. Fault responses for symmetrical monopole MMCs are first studied. Upper arm over voltages and AC-side nonzero-crossing currents arising from SPG faults in asymmetrical and bipolar configurations are then investigated. Mei et al [118] proposes a collaborative optimal configuration method of current limiting reactors (CLRs) and fault current limiters (FCLs) in the modular multilevel converter (MMC)-based high voltage direct current (HVDC) grids. The calculation methods of DC line fault currents and bridge arm fault currents considering the collaboration of CLRs and FCLs have high accuracy.

Li et al [119] proposes a new topology that utilizes a combination of half-bridge and novel three-level cells where the three-level cells utilize a clamp circuit .Under DC side faults, this topology is capable of blocking fault current thereby avoiding over currents in the freewheel diodes.

In [120] the cascaded FB cells offer DC fault reverse blocking capability. The FBs also act as an AC circuit breaker to virtually eliminate inrush currents from the AC side when the converter is de-blocked during system restart following fault clearance. Controlled recharging of the DC cable capacitance is provided by the HB cells of the main power stage while the cascaded FB cells remain blocked. The main power stage of the proposed converter operates at relatively low switching frequency; hence, the switching losses are reduced. The cascaded FB cells are only used to compensate for the harmonics generated by the main power stage, drastically reducing the FB cell capacitance and dimension.

In conclusion, the main challenges related to DC fault protection in MTDC system are:

- To detect the DC fault fast and to protect the electronic components.

- To avoid communication delay in the protection process.

- To select and isolate the faulted transmission line fast.

- To develop high voltage direct current circuit breakers (DCCBs) since mature and economically viable DCCBs are not available yet.

- To restore the healthy part of an MTDC system quickly.

2.10 Sub-module Faults: Fault-Tolerant Approach for Modular Multilevel Converters under Sub-module Faults

Yang et al [121] elaborates a switch open-circuit fault diagnosis and a fault-tolerant operation scheme for MMCs with distributed control. The proposed fault diagnosis and fault-tolerant control method can significantly improve the reliability of the MMC while maintaining the modularity of its software implementation. The proposed fault diagnosis method has the following distinct features:

- It is implemented in sub modules and only requires arm current and locally measured voltage to diagnose the fault, which can maintain the modularity of the MMC

- It is suitable for MMCs with many sub modules and can be easily extended for applications with different number of sub modules

- It can identify faulty switching devices within a short period before severe malfunction of the MMC or a secondary fault occurs

- It can simultaneously locate multiple switching device faults

- No extra hardware circuit or sensor is required

In paper [122], an IGBT open-circuit fault ride-through strategy, including fault detection, localization, redundancy, and recovery, is proposed for MMC with NLM

(Nearest Level Modulation). The detection method is proposed based on an additional inductor winding, which is used to measure the voltage across arm inductors. When a fault occurs, the voltage become much higher during some time, and the fault pulses will be generated by a simple hardware circuit. Thus, computation cost is very small. Wang et al [123] presents a survey on the existing fault diagnosis methods (FDMs) of the switch devices for the rapidly developing modular multilevel converters (MMCs). Three categories, namely mechanism-based, signal processing-based and artificial intelligence-based FDMs, are evaluated and summarised depending on the operating principles. Paper [124] investigates about the impact of open-circuit switch failures on the operation of the MMC. Based on the analysis under sub module failure conditions, two sub module failure detection and location methods are proposed, that is, a clustering algorithm (CA)-based method and a calculated capacitance (CC)-based method. In the proposed CA-based method, a pattern-recognition-based fault diagnosis approach, which employs the clustering algorithm to detect and locate the faulty sub modules with open-switch failures through identifying the pattern of 2-D trajectories of the sub module characteristic variables, is developed. The proposed CC-based method is based on the calculation and comparison of a physical component parameter, that is, the nominal sub module capacitance, and is capable of failure detection, location, and classification within one stage. Deng et al [125] proposes a protection scheme for the MMC under diode open-circuit faults. The impact of diode open-circuit failures of the sub modules on the operation of the MMC is analysed to reveal that the diode open-circuit fault would cause the high voltage in the faulty sub module, which would destroy the MMC and disrupt the operation of the MMC. A protection scheme based on the varistor is proposed for the MMC under diode open-circuit faults, which can effectively limit the voltage, detect the fault, and protect the MMC.

In paper [126], a strategy for detecting, localizing and correcting sub module and sensor faults in MMCs has been presented. The use of a few external sensors provides fault detection capability and voltage sensor redundancy. Moreover, the use of additional sub modules allows the faulty ones to be substituted easily. The detection technique is based on measuring the voltage provided by a set of sub modules and comparing it with a calculated reference value. The localization method is based on forcing the deactivation of the suspicious sub modules until the fault disappears. This method provides robust and fast responses to both sub module and sensor faults with minor additional costs. The experimental results demonstrate the effectiveness of the proposed technique in detecting and correcting all considered faults in less than 5 ms, which is much faster than other methods that can be found in the literature.

Ghazanfari et al [127] presents a resilient framework for fault-tolerant operation in modular multilevel converters (MMCs) to facilitate normal operation under internal and external fault conditions. This framework is realized by designing and implementing a supervisory algorithm and a post fault restoration scheme. The supervisory algorithm includes monitoring and decision-making units to detect and identify faults by analysing the circulating current and sub module capacitor voltages in a very short time. The post fault restoration scheme is proposed to immediately replace the faulty sub module with the redundant healthy one.

In paper [128], a novel fault-tolerant modulation and control strategy is proposed for MMC in medium voltage applications. Compared with previous works, the proposed strategy provides optimum performances under healthy conditions and minimum performance degradation after sub module failures. During healthy conditions, the redundant sub modules are fully utilized to decrease sub module capacitor voltage for higher reliability and to reduce switching frequency for higher efficiency. While during

fault tolerant operation, by appropriate modification of the modulation and controllers, no extra healthy sub modules need to be bypassed and the output voltage harmonics of MMC remain unchanged without causing voltage mismatches. The fault-tolerant control of MMC has been discussed in paper [129] based on the carrier phase shift modulation. All the sub modules, including the hot reserved sub modules, work in the operating mode and the standby mode in turns. A rotating sliding choice box is adopted to select the operating sub modules and the corresponding phase-shift angles, which enables the equal burden of each sub module. Once the faults are detected and localized, the reserved sub modules can simultaneously replace the bypassed failed sub modules, which guarantees the fault-tolerant operation with a nearly seamless transition and very short recovery time. Furthermore, the line cycle is set as the rotating period in the control strategy, without increasing much switching loss. The mismatch pulses are greatly reduced as well.

Abdelsalam et al [130] develops a modulation based fault-tolerant (FT) strategy for restoring the operation of three-phase modular multilevel converters (MMCs) with faulty switches. This FT strategy is based on a proposed modified space vector modulation (SVM) technique that generates balanced line-to-line (line) voltages even in the case of a fault occurrence. Deng et al [131] proposes a fault-tolerant approach for the MMC under sub module (SM) faults. The characteristic of the MMC with arms containing different number of healthy sub modules under faults is analysed. Based on the characteristic, the proposed approach can effectively keep the MMC operation as normal under sub module faults. It can effectively improve the MMC performance under sub module faults but without the knowledge of the number of faulty sub modules in the arm, without extra demand on communication systems, which potentially increases the reliability. To enhance reliability and avoid unscheduled maintenance, it is desired that

an MMC can remain operational without having to shut down despite some of its sub modules are failed.

In paper [132], complete fault diagnosis and tolerant control solution, including the fault detection, fault tolerance, fault localization, and fault reconfiguration, have been proposed to ride through the insulated gate bipolar transistor open-circuit failures. The fault detection method detects the fault by means of state observers and the knowledge of fault behaviours of MMC, without using any additional sensors. Then, the MMC is controlled in a newly proposed tolerant mode until the specific faulty sub module is located by the fault localization method; thus, no overcurrent problems will happen during this time interval. After that, the located faulty sub module will be bypassed while the remaining sub modules are reconfigured to provide continuous operation. Throughout the fault periods, it allows the MMC to operate smoothly without obvious waveform distortion and power interruption. In paper [133] proportion and failure analysis of full-bridge sub-modules in a hybrid MMC is analysed. Paper [134] investigates about fault detection and localization methods through the Kalman filter. The fault localization is based on the failure characteristics of the sub module in the MMC. The proposed method can be implemented with less computational intensity and complexity, even in case that multiple sub module faults occur in a short time interval.

In paper [135], an improved post-fault strategy is introduced for modular multilevel converters, which utilizes the remaining healthy capacity of the converter more efficiently and increases the line voltage amplitude under these circumstances. The main contribution of the proposed method is maximizing the line voltage amplitude using the optimum DC component and the best neutral point position.

The modular multilevel converter is always designed with the redundant sub modules to continue the operation during the faults. Typically, the sub modules are designed with

a bypass switch connected across the AC output terminals. During the fault condition, the bypass switch is used to disconnect the faulty sub module and insert one of the redundant sub modules in the arm. Thus, the effect of faults on the MMC operation can be significantly minimized. However, detecting of faults and inserting redundant sub modules without inrush current is a great challenge.

2.11 Summary of Literature Review

Based on the literature review, MMC loss and efficiency is one of critical issues in any HVDC system. In extremely high-power converter 0.1% more or less in the losses is a very valuable commercial argument for the manufacturers. So, working in lower switching frequencies could be a solution to achieve lower losses and higher efficiency. However, choosing the switching frequency very low will impose higher ripple over the capacitor and will increase the THD of output current [102]. In this research, the new MMC topology is proposed to address this issue which will help the MMC to work even in lower switching frequencies by adding some extra switches and using some idle sub module capacitors during the switching period. Simulation results confirm that the new design can stabilize the sub module capacitor voltage in lower switching frequencies and improve the converter efficiency. Reliability is the other drawback of MMC which has been discussed in literature review. The proposed design can improve the converter reliability during the sub module capacitor failure. Considering open circuit status for the faulty sub module capacitor, the converter can continue the normal operation. Moreover, the proposed design can set the sub module capacitor voltages without using any sub module voltage sensors for each arm which will reduce the cost of the converter and will improve its reliability, since the number of devices that can fail is lower. Chapter 3, investigates about the proposed new MMC design and its operational principle. In

chapter 4, operation of the new topology at HDVC system level and converter reliability

aspects are discussed.

Chapter 3: Proposed New MMC Topology and Its Operational Principle

This chapter highlights the methodologies employed in addressing the research objectives. By proposing a new topology for MMC all research objectives will be addressed.

The proposed topology decreases the sub module capacitor voltage ripples at lower switching frequencies without the need for large sub module capacitors. It uses the additional switches and the capacitors that are idle during the switching period. Simulation results confirm the effectiveness of the proposed topology with reduced sub module voltage fluctuation at lower switching frequencies. Loss and efficiency calculations confirms that the converter efficiency is improved during operation at lower switching frequencies.

3.1 Research Methodology and Design

As discussed before, this research proposes a new topology for a high-voltage direct-current (HVDC) modular multilevel converter (MMC). The comparative study between the two classic topologies of MMC (AC side cascaded and DC side cascaded topologies) indicates some disadvantages which can affect their performance and the MMC power losses and reliability are one of them. In HVDC applications, the switching frequency should be kept low to reduce the converter switching power losses. However, choosing the switching frequency very low will impose higher voltage ripples on the sub module capacitors. So, a large sub module capacitor is needed to eliminate sub module voltage ripple which is prohibitively uneconomical for the high voltage applications.

The proposed topology has the advantage of reducing the sub module voltage ripples at lower switching frequencies without the need for large sub module capacitors. The

new design only uses additional switches and the capacitors that are idle during the switching period. Idle capacitors of sub modules are connected in parallel with active capacitors to increase the total capacitance. Moreover, the new design has more reliability in the case of sub module capacitor failure which keeps the converter in continues operation condition.

The other advantage is eliminating using of sub module voltage sensors which will increase the converter reliability. The converter cost and complexity also will be decreased because of using the proposed design.

This chapter introduces the new MMC topology to address the issues related to MMC operation at lower switching frequencies, MMC sub module voltage fluctuations and its high circulating current value at lower switching frequencies and MMC power losses.

Fig. 3.1 shows the new proposed MMC topology. Six additional switches (S_9, S_{10}, S_{11}, S_{20}, S_{21}, S_{22}) are added to common topology of the MMC (Half-bridge DC side cascaded topology) to use idle capacitors during the switching period. Table 3.1 indicates switching states for the upper leg of new proposed topology.

Depending on the states of main switches, additional switches will operate in such a way that idle capacitors be parallel with active capacitors in some states. Switching logic for the lower arm is similar to upper arm.

Voltage stress on the added switches is shown in Table. 3.2 which is $V_{dc}/4$ for each switch.

Table. 3.1 Switching states for the upper leg

$S_1S_2\,S_3S_4\,S_5S_6\,S_7S_8$	C_1	C_2	C_3	C_4	State Number
1 0 1 0 1 0 1 0	active	active	active	active	1
1 0 0 1 0 1 0 1	active	Idle	Idle	Idle	2
1 0 1 0 0 1 0 1	active	active	Idle	Idle	3
1 0 1 0 1 0 0 1	active	active	active	Idle	4
1 0 0 1 0 1 1 0	active	Idle	Idle	active	5
1 0 1 0 0 1 1 0	active	active	Idle	active	6
1 0 0 1 1 0 1 0	active	Idle	active	active	7
1 0 0 1 1 0 0 1	active	Idle	active	Idle	8
0 1 1 0 0 1 0 1	Idle	active	Idle	Idle	9
0 1 1 0 1 0 0 1	Idle	active	active	Idle	10
0 1 1 0 1 0 1 0	Idle	active	active	active	11
0 1 0 1 1 0 0 1	Idle	Idle	active	Idle	12
0 1 0 1 1 0 1 0	Idle	Idle	active	active	13
0 1 0 1 0 1 1 0	Idle	Idle	Idle	active	14
0 1 1 0 0 1 1 0	Idle	active	Idle	active	15
0 1 0 1 0 1 0 1	Idle	Idle	Idle	Idle	16

Table. 3.2 Voltage stresses on the added switches

Voltage Stress	Added Switch
Vdc/4	S_9
Vdc/4	S_{10}
Vdc/4	S_{11}
Vdc/4	S_{20}
Vdc/4	S_{21}
Vdc/4	S_{22}

Fig. 3.1 illustrates the schematics of the proposed new topology. Six switches (S_9, S_{10}, S_{11}, S_{20}, S_{21}, S_{22}) are added to the classic topology of MMC.

In states 1, 11, 13, 14 and 16 is not possible to connect the idle capacitors in parallel with the capacitors that are in the path. States 4, 10 and 12 could be considered as a similar state because C_4 is going to be parallel with C_3 in all of these states. In states 6 and 15, C_3 is parallel with C_2 during the switching period. States 3 and 9 also can be considered as similar states because C_4, C_3 and C_2 are parallel at the same time. In state 2, C_4, C_3, C_2 and C_1 have parallel connection. State 5, represents parallel connection of C_3, C_2 and C_1. In state 7, there is only one parallel connection between C_2 and C_1. In state 8, C_2 is parallel with C_1 and C_4 is parallel with C_3.
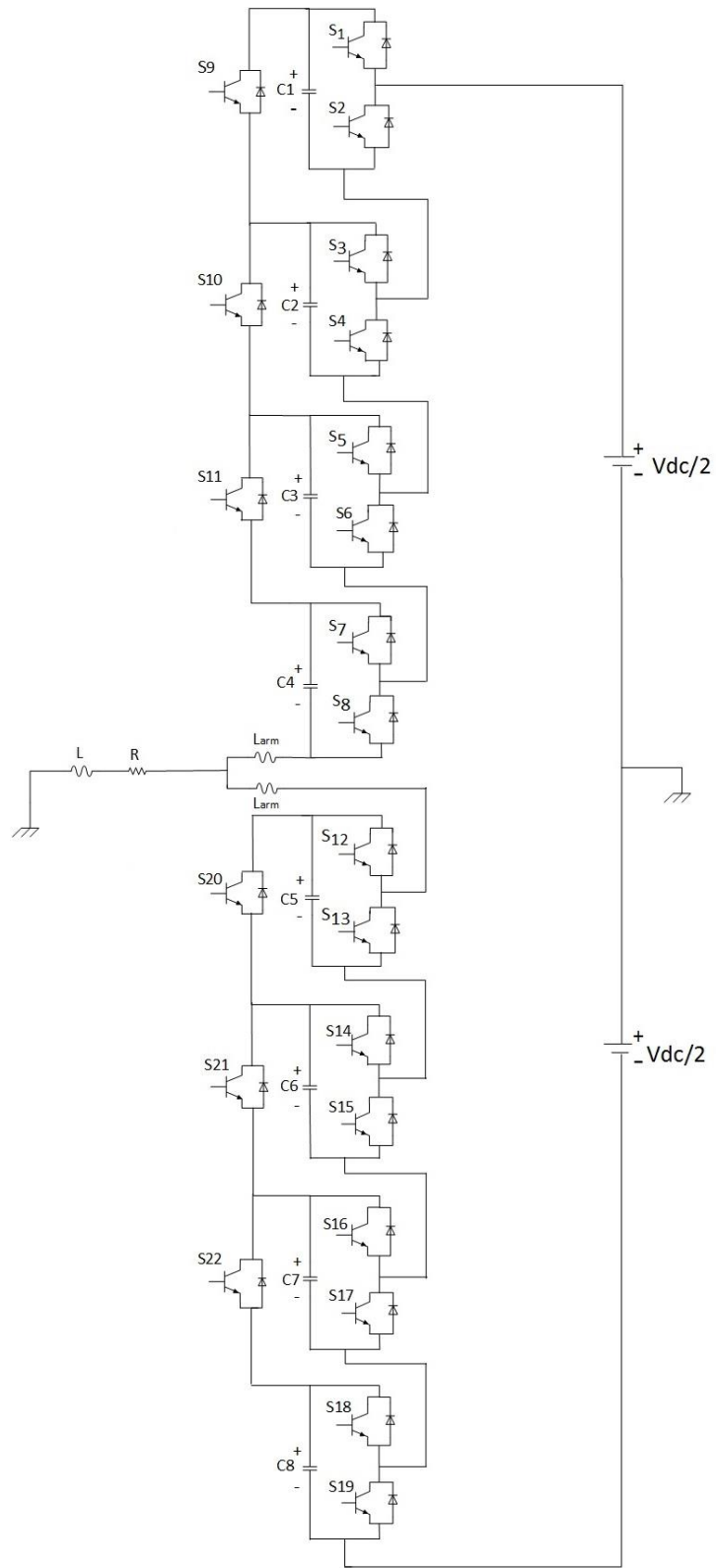
Fig. 3.1 New proposed topology (single phase)

If S_5: ON & S_8: ON Then S_{11}: ON (States 4, 10, 12)
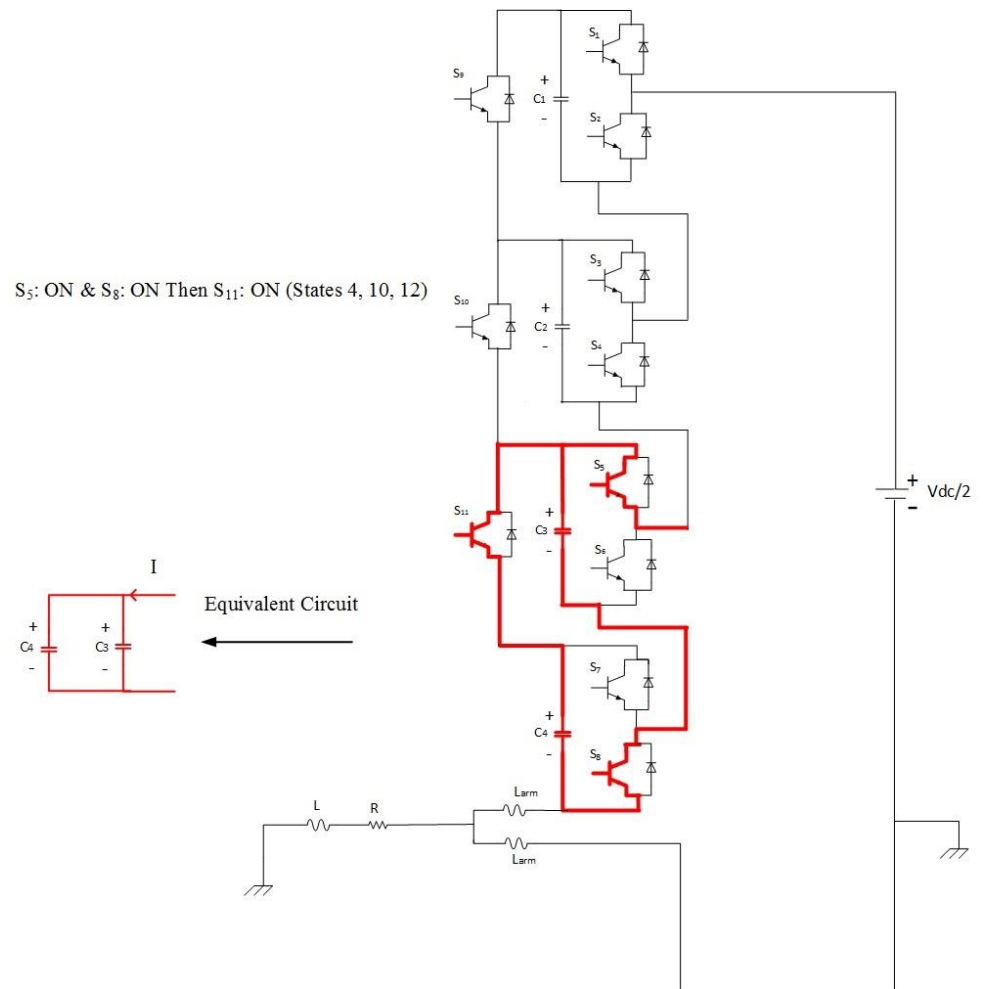
Fig. 3.2 States 4, 10 and 12

In these states, C_4 is parallel with C_5.

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If S_3: ON & S_6: ON Then S_{10}: ON (States 6 and 15)
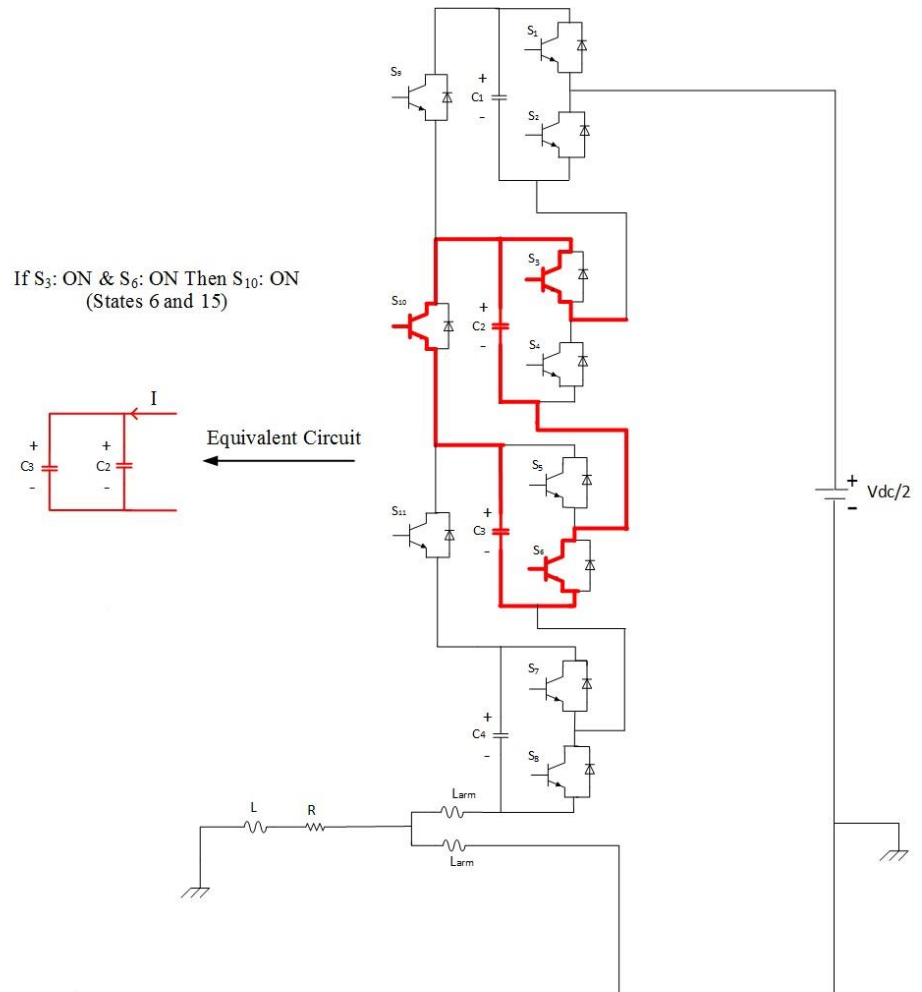
Fig. 3.3 States 6 and 15

In these states, C_3 is parallel with C_2.

If S_3: ON & S_6: ON & S_8: ON Then S_{10}&S_{11}: ON (States 3 and 9)
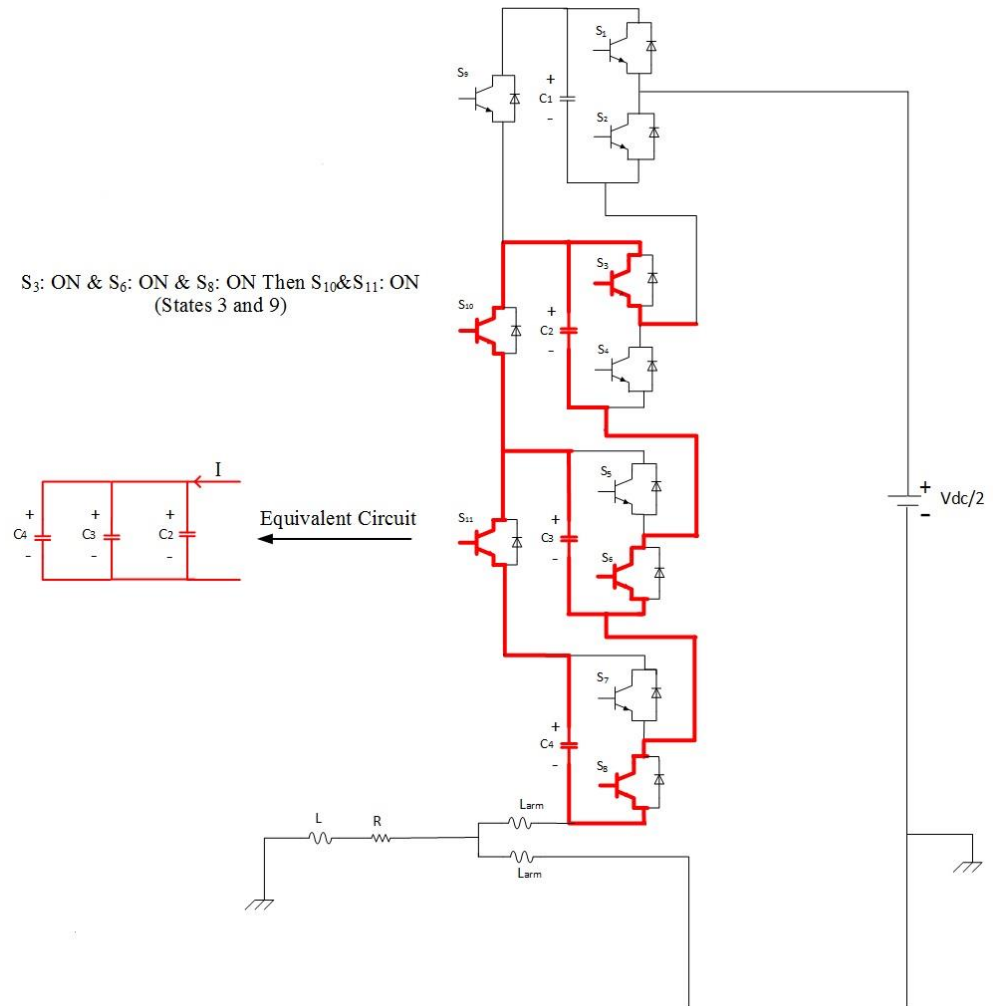
Fig. 3.4 States 3 and 9

In these states C_4, C_3 and C_2 are parallel.

If S_1: ON & S_4: ON & S_6: ON & S_8: ON Then S_9&S_{10}&S_{11}: ON (State 2)
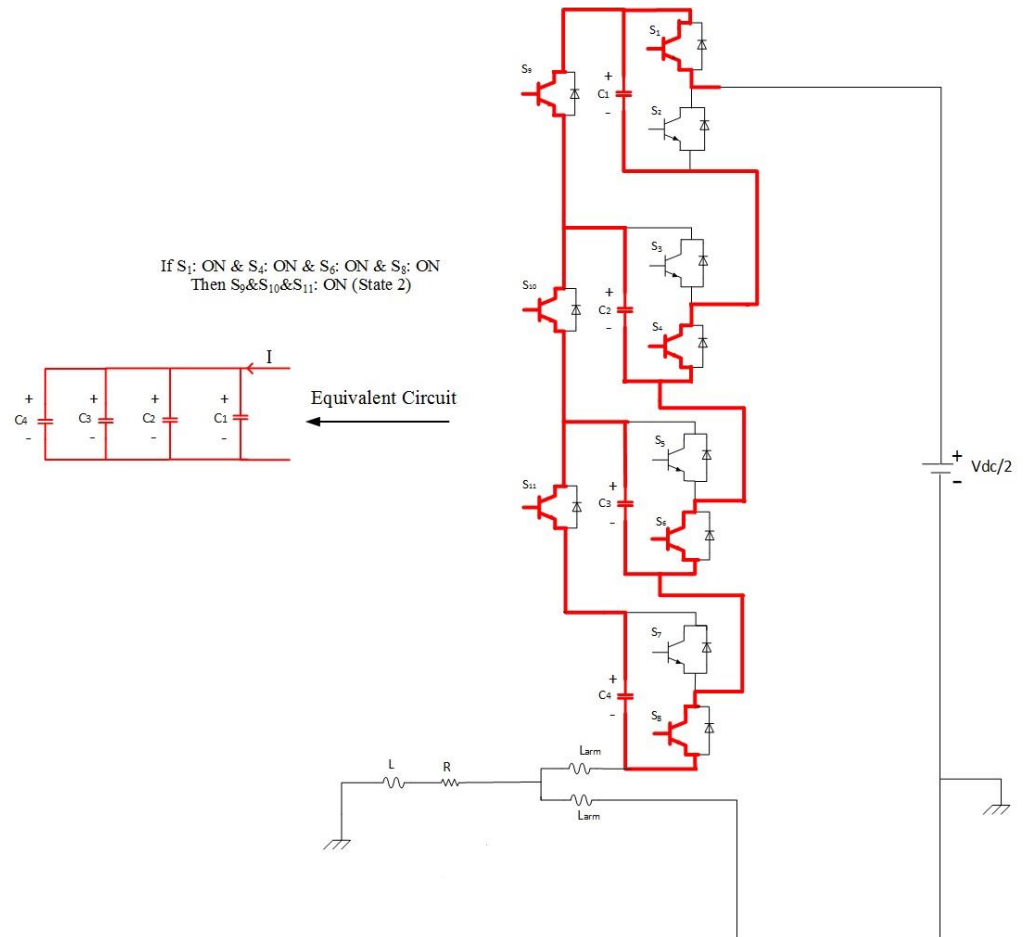
Fig. 3.5 State 2

In these states C_4, C_3, C_2 and C_1 are parallel.

If S_1: ON & S_4: ON & S_6: ON & S_7: ON Then S_9&S_{10}: ON (State 5)
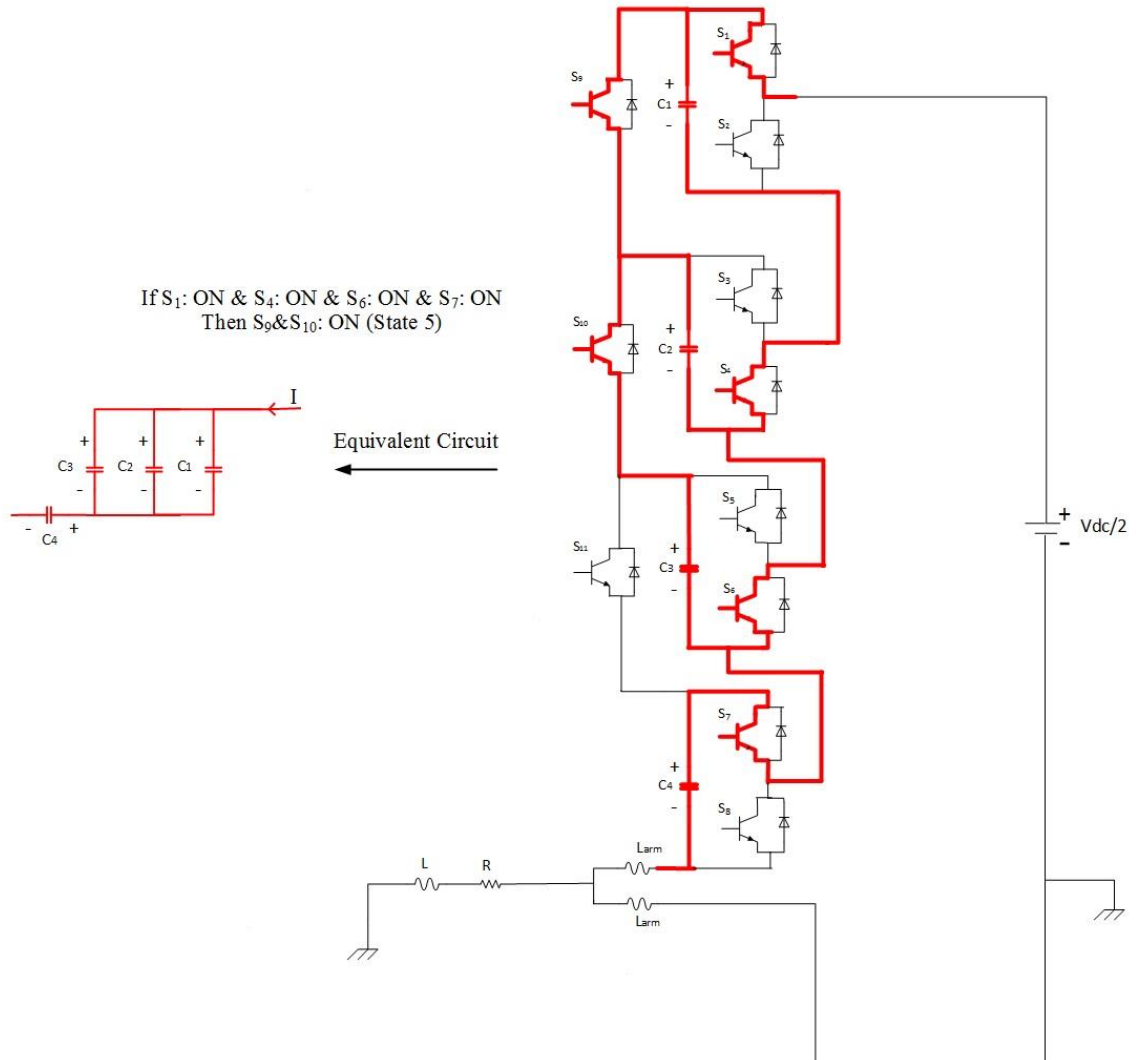
Fig. 3.6 State 5

This state represents parallel connection of C_3, C_2 and C_1

If S_1: ON & S_4: ON & S_5: ON & S_7: ON Then S_9: ON (State 7)
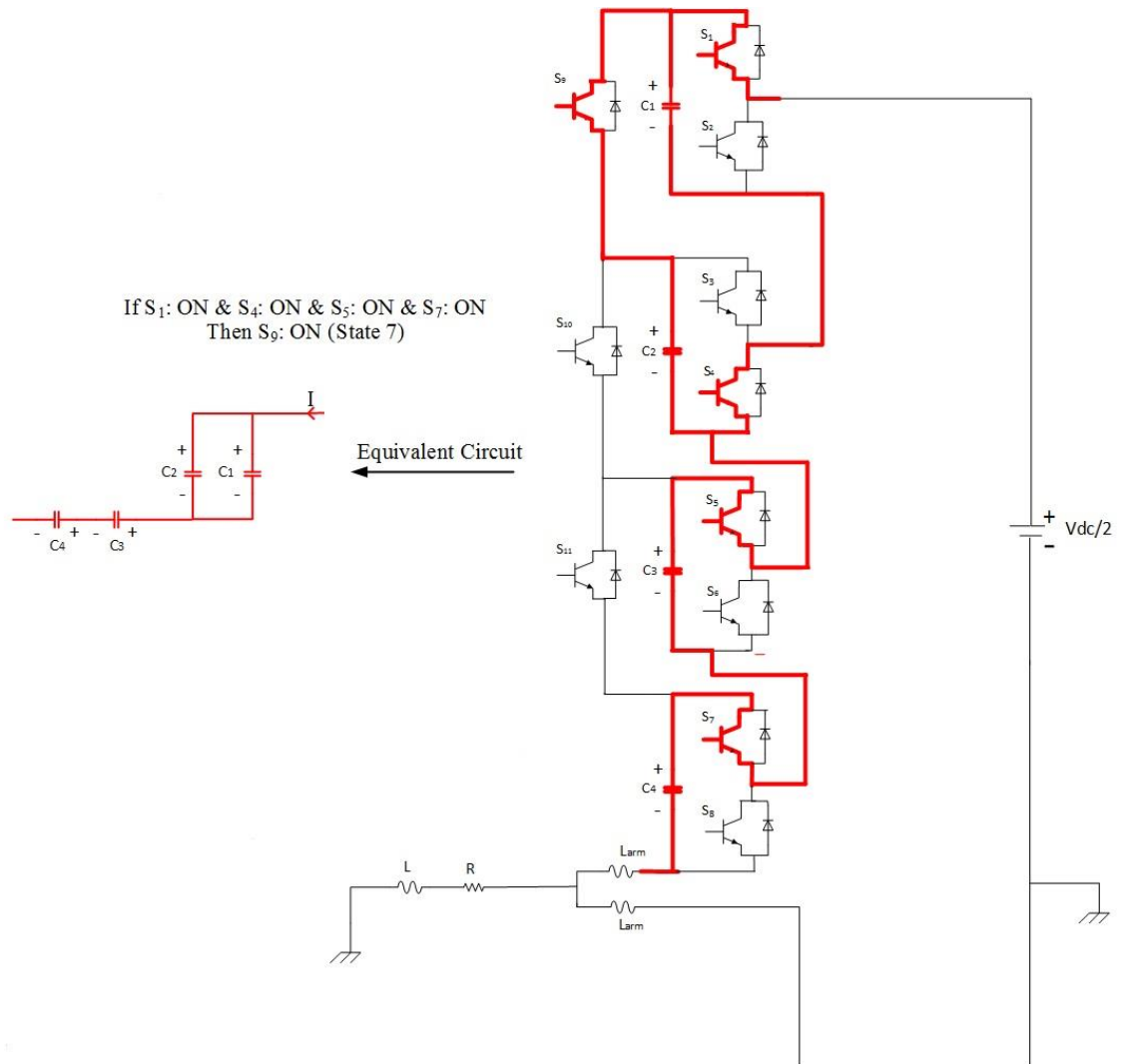
Fig. 3.7 State 7

In this state, there is only one parallel connection between C_2 and C_1.

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If S_1: ON & S_4: ON & S_5: ON & S_8: ON Then S_9&S_{11}: ON (State 8)

If S_1: ON & S_4: ON & S_5: ON & S_8: ON
Then S_9&S_{11}: ON (State 8)

Equivalent Circuit
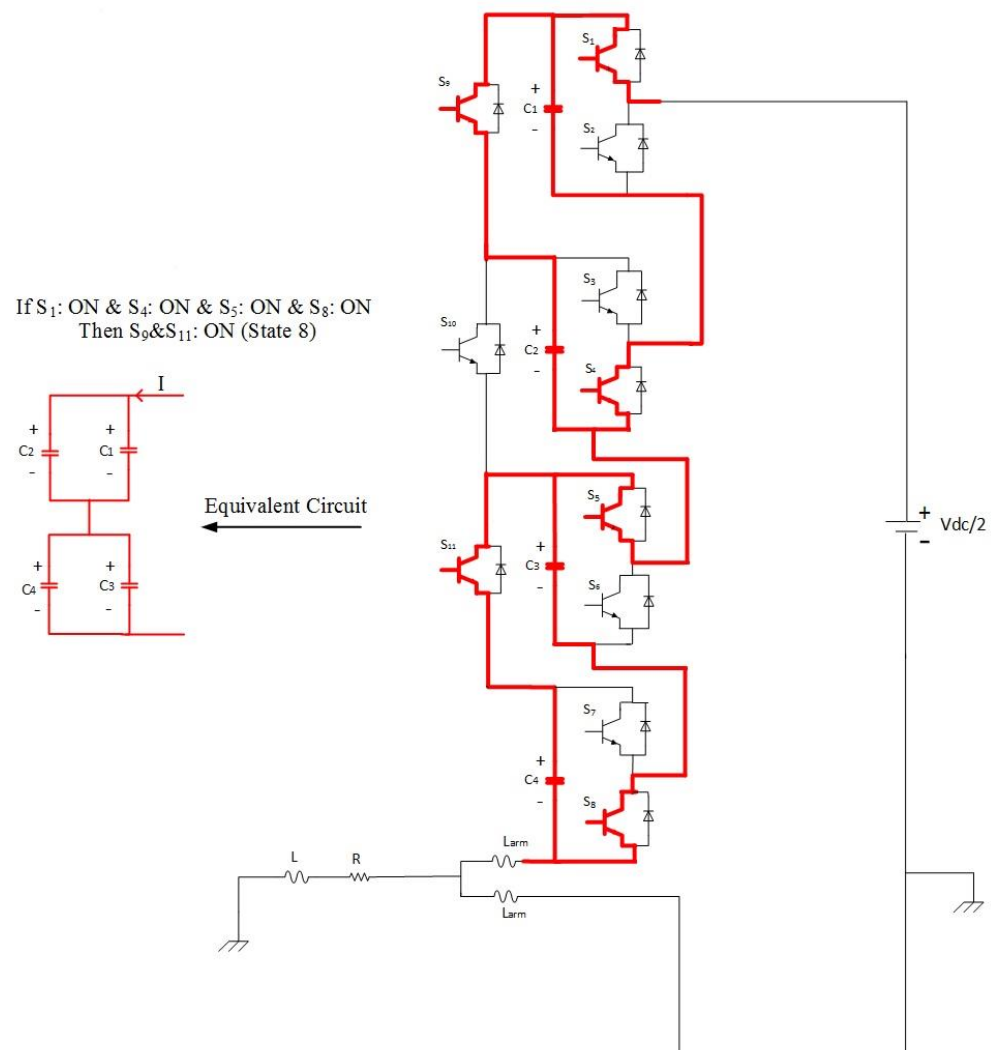
Fig. 3.8 State 8

In state 8, C_2 is parallel with C_1 and C_4 is parallel with C_3.

The lower arm follows the similar switching strategy as the upper arm.

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3.2 Sub Module Capacitance Selection Principle

Optimizing the selection of sub module capacitance is a critical issue in MMC design. When the sub module is in inserted mode, arm current flows through the sub module capacitor causing the capacitor voltage fluctuations. The sub module capacitance is designed to suppress the voltage fluctuation to meet the required specifications.

3.2.1 Definition of Sub Module Voltage Ripple Factor

In [136], the analytical relationship between sub-module capacitance and its voltage fluctuation is developed, on which the sub-module capacitance can be selected to meet the voltage fluctuation specifications. However, this relationship is derived based on the assumption that all sub module capacitor voltages are well balanced. To achieve well balanced sub module capacitor voltage, relatively high switching frequency is needed. Ripple suppression methods under unbalanced conditions is presented in [137]. Shekhar et al [45] has explained that the voltage-balancing control is under the cost of higher switching frequency to reduce the unbalanced voltage. For HVDC applications, MMC needs to operate at relatively low switching frequency conditions, in which case sub module capacitor voltage-unbalance issue cannot be neglected. As the unbalanced voltage increases the sub module capacitor voltage fluctuation, the sub module capacitance selection criterion based on the relationship between the sub module capacitance and voltage fluctuation derived in [49].

Hu et al [49] presents the analysis of capacitor voltage ripple for conventional MMC and ripple factor ε under varying operating conditions can be derived as:

$$\varepsilon = \frac{S}{3CV_C V_{dc}\omega m}\left[1-\left(\frac{m\cos\phi}{2}\right)^2\right]^{1.5} \tag{3.1}$$

It is considered that the converter is operating in steady state and all the arms are balanced. S is three phase apparent power, C is each sub module capacitance, V_C is the mean value of capacitor voltage, V_{dc} is the DC link voltage, ω is the fundamental frequency, m is modulation index and $\cos\phi$ is the power factor. From (3.1) it can be seen that under fixed DC voltage and constant power transmission condition, ε is closely related to m and ϕ. It should be noticed that the maximum acceptable ripple factor (ε) is 10% for each sub module voltage. In proposed design, the value of C is increased by the paralleling of idle capacitors which decreases the ripple factor (ε).

3.3 Simulation Results at Different Switching Frequencies

The proposed topology with 8 sub modules across all both arms for the single phase MMC has been simulated in Matlab/Simulink. The number of sub modules across all both arms is given as 8. It is the summation of the total sub modules in each arm which is 4 sub modules for the upper arm and 4 sub modules for the lower arm so totally 8 sub modules across all both arms. Matlab Simulation is the most preferable and best way to bring out the idealistic reality into a model-based design environment. The model described in this section illustrates modelling of a 5-level multilevel inverter considering the new design. The objective of the simulation is to demonstrate the use of proposed topology at low switching frequencies. The coupled inductors are employed as the arm inductors and R-L loads are used in the simulation. The carrier phase-shifted sinusoidal pulse width modulation (CPS-PWM) technology generates pulses for a PWM-controlled modular multilevel converter. Operations at four different switching frequencies at unity power factor condition are simulated. Table. 3.3 depicts the simulation parameters of the system which are taken from reference [128] as a benchmark.

Table. 3.3 Simulation Parameters in unity power factor condition [128]

Parameter	Value	Parameter	Value
Number of SMs across both arms	8	Carrier frequency	1000 Hz
			400 Hz
			100 Hz
			50 Hz
Number of Half-Bridge SMs across both arms	8	DC bus voltage	4 kV
SM capacitor voltage	1 kV	SM capacitance	3300 µF
		Output power	600 kW
Arm inductor	4 mH	Load resistance	10 Ω
		Load inductance	6 mH

Simulation results confirm the effectiveness of the proposed design. Capacitor ripples and circulating current values are significantly decreased after applying the new design at t=5 Sec during the operation at low switching frequencies (50 Hz and 100 Hz). Moreover, Output voltage, output current, upper arm and lower arm currents, harmonic analysis of sub module capacitor voltage and the output voltage harmonic investigation are shown in this section. It should be remarked that working at lower switching frequencies is an important target as it decreases the total switching power loss and improves the efficiency. Applying the new design will reduce the size of the required sub module capacitor at low switching frequencies to have acceptable voltage ripple (less than 10%). There is always a trade off in MMC design between the switching frequency and sub module voltage ripple. Choosing the working point in lower switching frequencies will impose higher ripples on sub modules [138]. Fig. 3.9 shows the engineering trade-off in designing the MMC system.
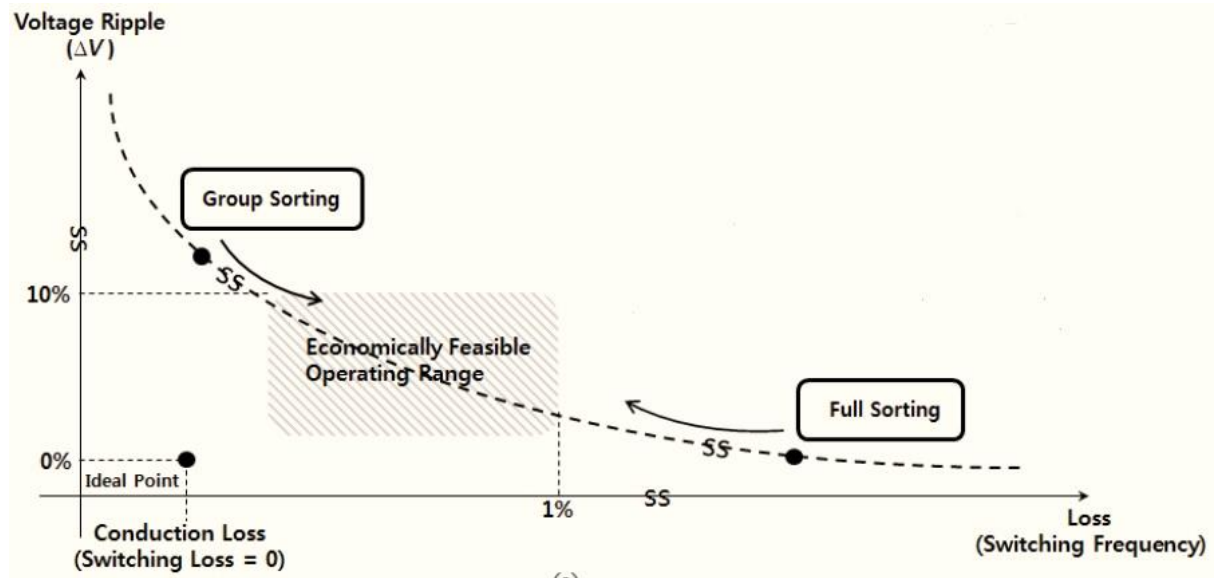
Fig. 3.9 Engineering Trade-off in Designing MMC System [138]

By applying the new design for MMC, the working point can be kept in the lower switching frequencies with acceptable sub module voltage ripple. For the lower switching frequencies (50 Hz and 100 Hz) simulation results show the acceptable sub module voltage ripple. Loss and efficiency analysis at 100 Hz switching frequency and 1000 Hz switching frequency depicts the same conduction losses range for both switching frequencies using the proposed design. However, because of decreasing the switching frequency, the efficiency will be improved. In Chapter 4, the nominal values of existing East-West inter-connector will be considered for the proposed design. This Interconnector has been used because is one of the important HVDC links in Ireland. So, using this benchmark will be helpful to do any further developments on converter topologies in the future.

3.3.1 Simulation Results at 1000 Hz Switching Frequency

It should be noted that for the first 5 sec of the simulation a classic half bridge DC side cascaded topology operation is simulated and at t=5 Sec the simulation of the proposed new topology commences. Sub module capacitor voltage, circulating current,

arm currents, output current and output voltage are shown as results for each switching frequency. Moreover, the output voltage and sub module voltage are analysed from harmonics point of view. From simulation results, the new design doesn't have any significant impact on sub module voltage ripple or on the circulating current value.
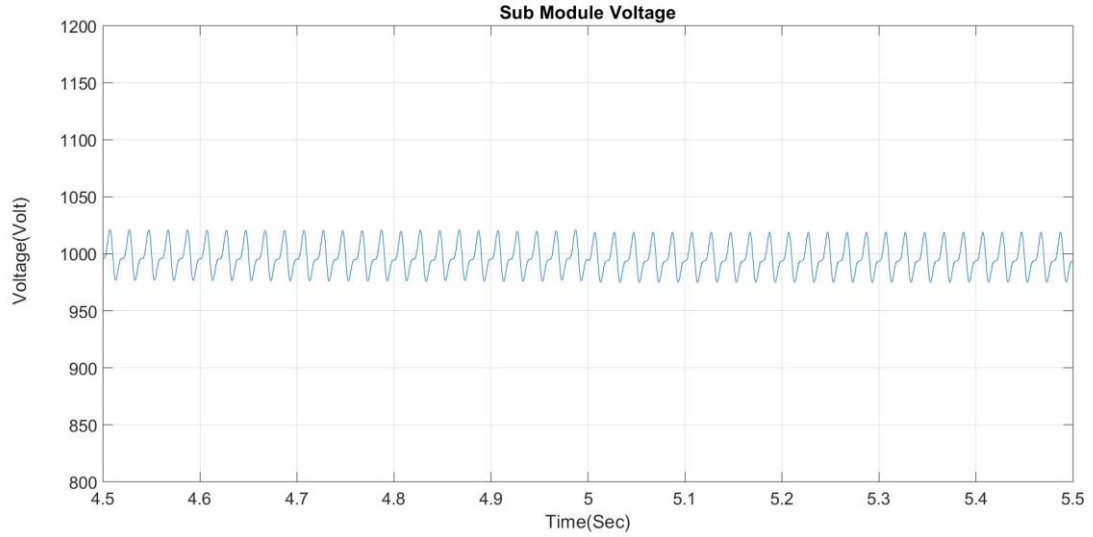
Fig. 3.10 Sub module voltage before and after applying the proposed design at t= 5 Sec and 1000 Hz switching frequency

Sub module voltage doesn't have any significant variation before and after applying the new topology at 1000 Hz switching frequency. So, Peak to peak value for the sub module voltage is identical before and after t=5 Sec.

Fig. 3.11 Circulating current before and after applying the proposed design at t= 5 Sec and 1000 Hz switching frequency

Variation of circulating current has been shown in Fig. 3.11 which depicts the amount of circulating current has been decreased 5% after applying the new topology. Fig. 3.12

and Fig. 3.13 illustrate variation of upper arm and lower arm currents which remain unchanged after t=5 Sec.

Fig. 3.12 Upper arm current before and after applying the proposed design at t= 5 Sec and 1000 Hz switching frequency

Fig. 3.13 Lower arm current before and after applying the proposed design at t= 5 Sec and 1000 Hz switching frequency

Fig. 3.14 depicts that the output current doesn't have any significant change after applying the new design at 1000 Hz switching frequency.

Fig. 3.14 Output current before and after applying the proposed design at t=5 Sec and 1000 Hz

switching frequency

Fig. 3.15 Output voltage before and after applying the proposed design at t=5 Sec and 1000 Hz

switching frequency

According to Fig. 3.15, peak to peak output voltage value is 4kV which remains unchanged after applying the new design at t=5 Sec and 1000 Hz switching frequency.

3.3.1.1 Harmonic Analysis of Sub Module Voltage, Output Voltage

and Circulating Current at 1000 Hz switching frequency

In order to identify the basic harmonic components of sub-module (SM) capacitor voltage the harmonic analysis has been done. The analysis implies that ripples with fundamental frequency and double line-frequency are basic components in the capacitor voltage ripple. The output voltage harmonic analysis shows the THD of output voltage will not change after applying new design at t=5 Sec and odd harmonics are dominant. Fig. 3.16 and Fig. 3.17 indicate the harmonic analysis of the sub module voltage and output voltage.

(a)   *(b)*

Fig. 3.16 Harmonic analysis of sub module voltage at 1000 Hz switching frequency (a) before applying the new design (b) after applying the new design

Fig. 3.16 depicts that harmonic components for the sub module voltage will not change after applying the new design and the THD value will be identical for both cases.

Fig. 3.17 Harmonic analysis of output voltage at 1000 Hz switching frequency (a) before applying the

new design (b) after applying the new design

Dominant harmonic values for the output voltage are 3rd, 5th, 7th and 9th which remain unchanged after applying the new design at 1000 Hz switching frequency.

Fig. 3.18 depicts the harmonic content of circulating current before and after applying the new design which contains second and other even-order harmonics as dominant harmonic components.

(a)   (b)

Fig. 3.18 Harmonic analysis of circulating current at 1000 Hz switching frequency (a) before applying

the new design (b) after applying the new design

The amount of THD is decreased 1.3% after t=5 Sec.

3.3.2 Simulation Results at 400 Hz Switching Frequency

Fig. 3.19 depicts the sub module voltage before and after applying the new design at t=5 Sec considering converter switching frequency of 400 Hz. The voltage fluctuations are in an acceptable range which is less than 10% variation. Peak to peak voltage ripple is similar before and after t=5 Sec. However, applying the new design will set the average ripple voltage to 1kV without any error and is exactly expected submodule voltage.

Fig. 3.19 Sub module voltage before and after applying the proposed design at t= 5 Sec and 400 Hz switching frequency

Fig. 3.20 shows the circulating current before and after applying the new design. The content of circulating current decreased 4% after applying the new design at t=5 Sec.
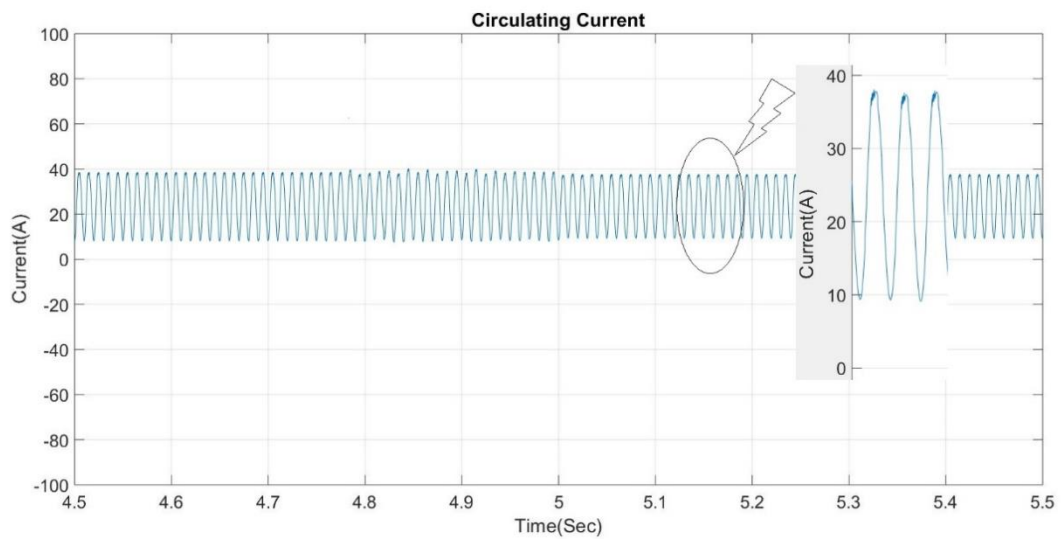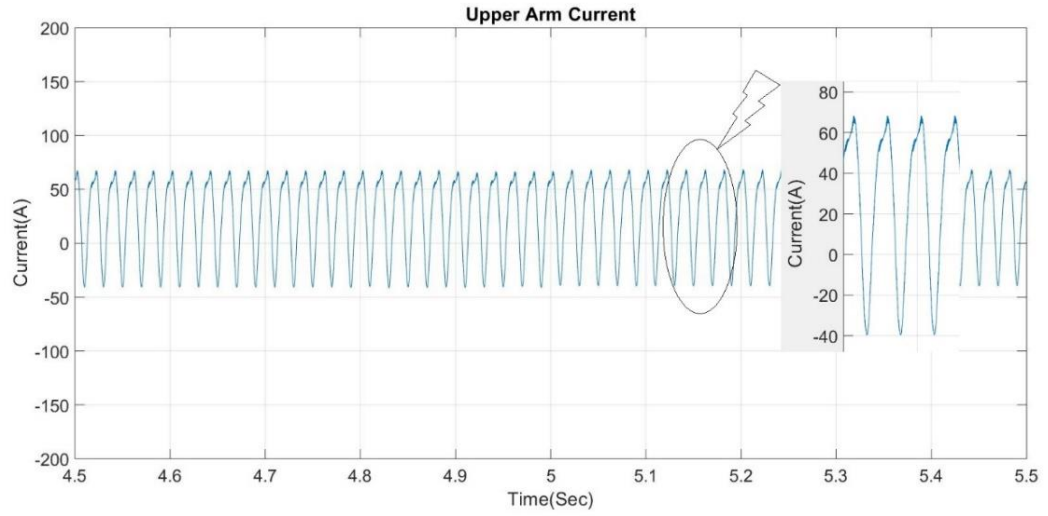

Fig. 3.20 Circulating current before and after applying the proposed design at t= 5 Sec and 400 Hz switching frequency

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Fig. 3.21 Upper arm current before and after applying the proposed design at t=5 Sec and 400 Hz

switching frequency

During the operation of the MMC, the arm current flows though the sub module capacitors, which charge and discharge the capacitors. Fig. 3.21 and Fig. 3.22 show the upper arm and lower arm currents before and after t=5 Sec. There is no significant change on arm currents after applying the proposed design.

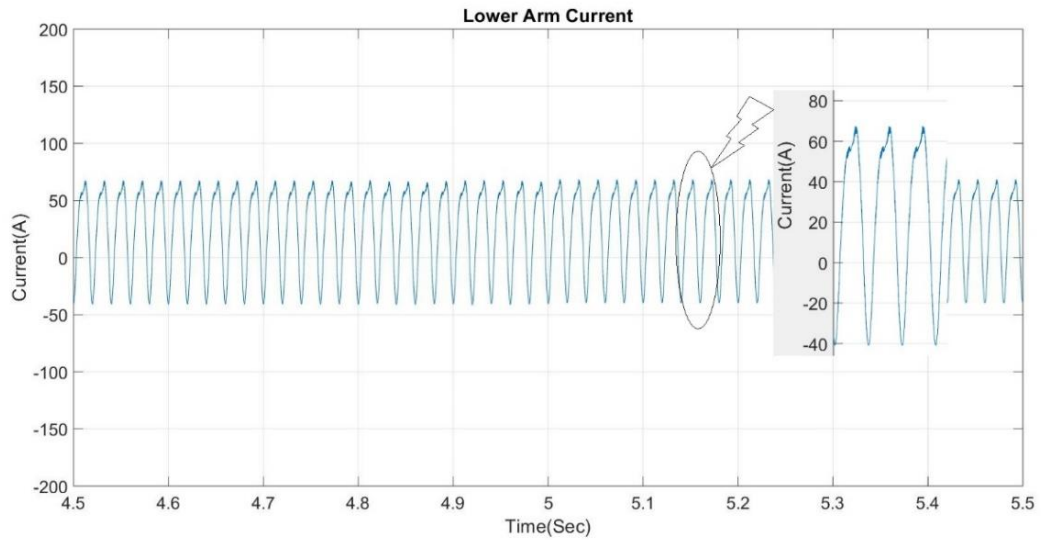*Fig. 3.22 Lower arm current before and after applying the proposed design at t=5 Sec and 400 Hz*

switching frequency

Fig. 3.23 and Fig. 3.24 depict the output current and output voltage at 400 Hz switching frequency. There is no significant change on the output voltage and current before and after applying the new design at t=5 Sec and 400 Hz switching frequency.
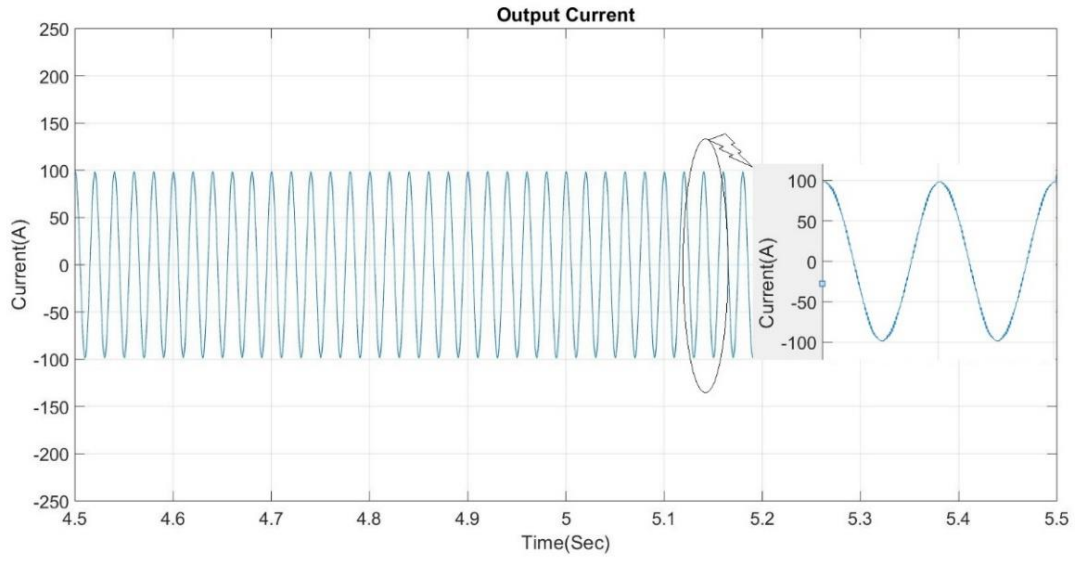

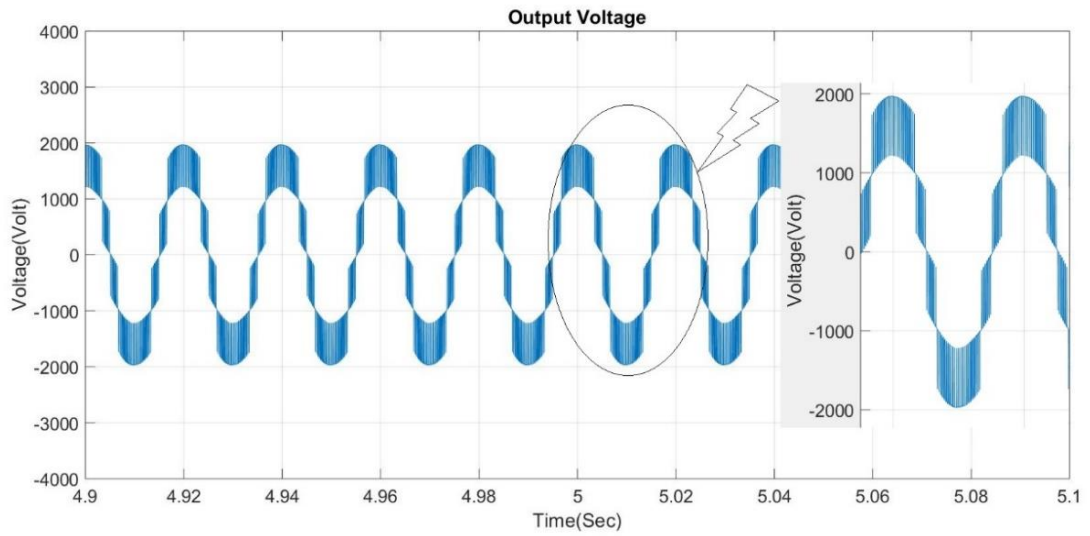*Fig. 3.23 Output current before and after applying the proposed design at t= 5 Sec and 400 Hz switching frequency*

Fig. 3.24 Output voltage before and after applying the proposed design at t= 5 Sec and 400 Hz switching frequency

3.3.2.1 Harmonic Analysis of Sub Module Voltage, Output Voltage

and Circulating Current at 400 Hz switching frequency

Fig. 3.25 and Fig. 3.26 indicate the harmonic analysis of the sub module voltage and output voltage at 400 Hz switching frequency. The dominant harmonic order of sub module voltage is second harmonic which remains unchanged after applying the new design at 400 Hz switching frequency. Sub module voltage THD has been increased 1% after applying the new design.
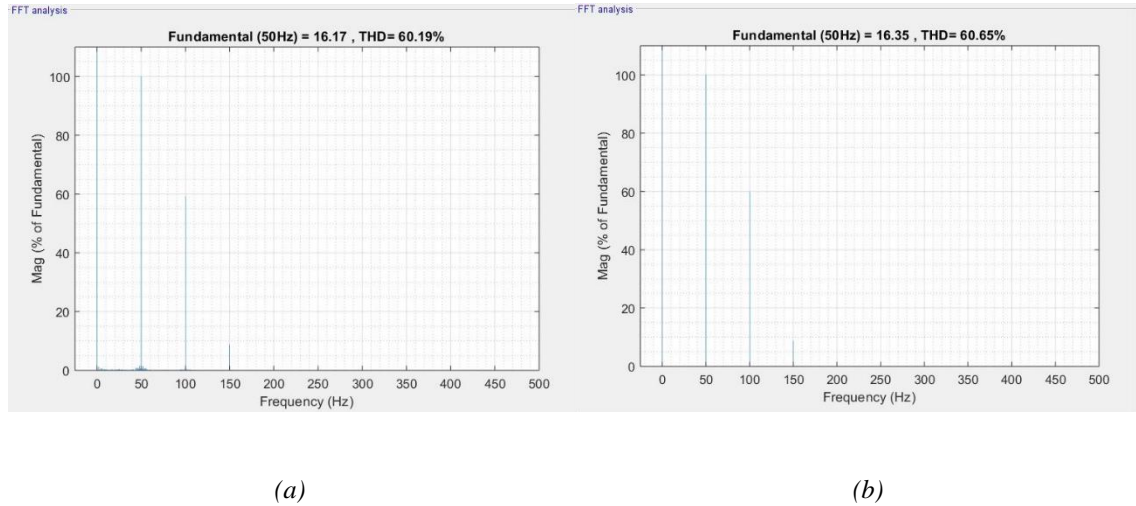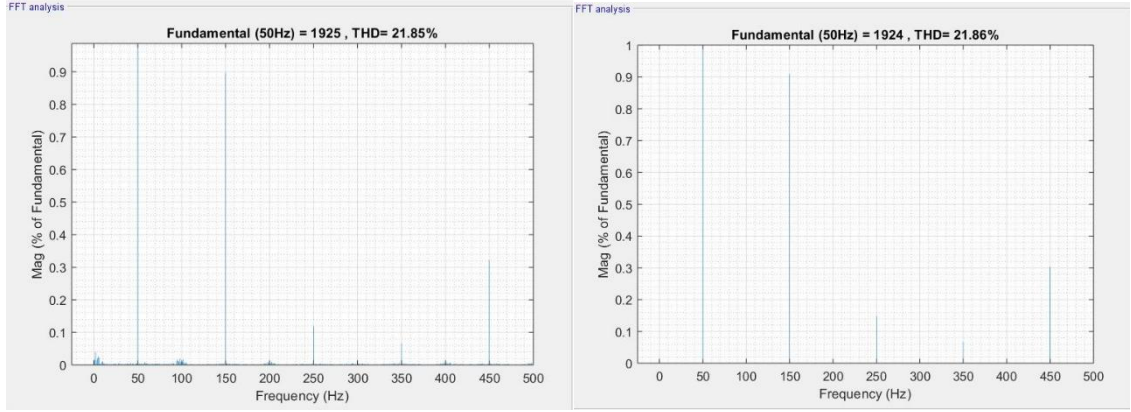

| | |
| (a) | (b) |

Fig. 3.25 Harmonic analysis of sub module voltage at 400 Hz switching frequency (a) before applying the new design (b) after applying the new design

The dominant harmonic order of output voltage is third harmonic.
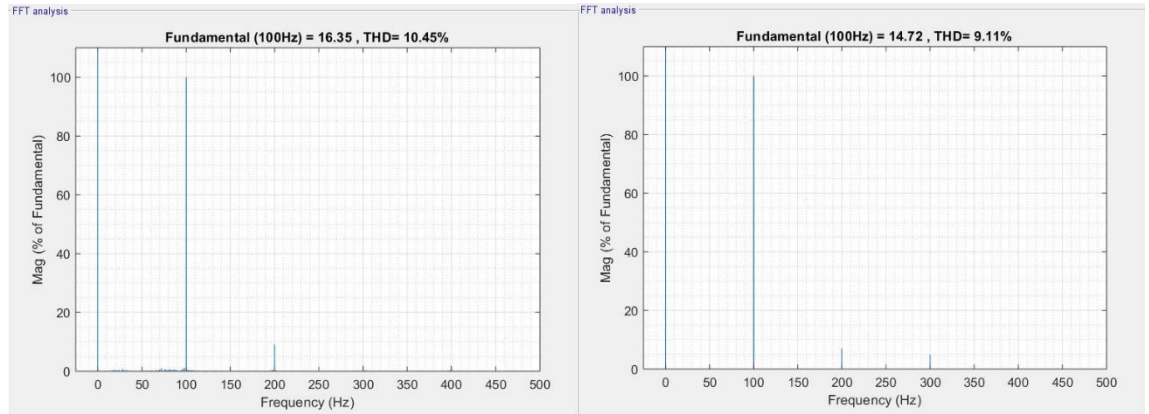

| | |
| (a) | (b) |

Fig. 3.26 Harmonic analysis of output voltage at 400 Hz switching frequency (a) before applying the new design (b) after applying the new design

From Fig. 3.26 it can be seen the new design doesn't have any significant impact on harmonic content of output voltage and THD value.

Fig. 3.27 illustrates the harmonic content of circulating current before and after applying the new design which contains second and other even-order harmonics as dominant harmonic orders.

(a)   *(b)*

Fig. 3.27 Harmonic analysis of circulating current at 400 Hz switching frequency (a) before applying the new design (b) after applying the new design

The amount of second harmonic is decreased after applying the proposed design. On the other side, THD has been increased from 8.76% to 10.97%.

3.3.3 Simulation Results at 100 Hz Switching Frequency

With decreasing the switching frequency to 100 Hz and applying the new design, the sub module voltage ripple will be the same as 1000 Hz switching frequency condition. Fig. 3.28 shows the sub module voltage variation before and after applying the new design at t=5 Sec and 100 Hz switching frequency. The amount of sub module voltage ripple is decreased 50% after t=5 Sec when the new design comes to the circuit and is the same as 1000 Hz switching frequency condition.
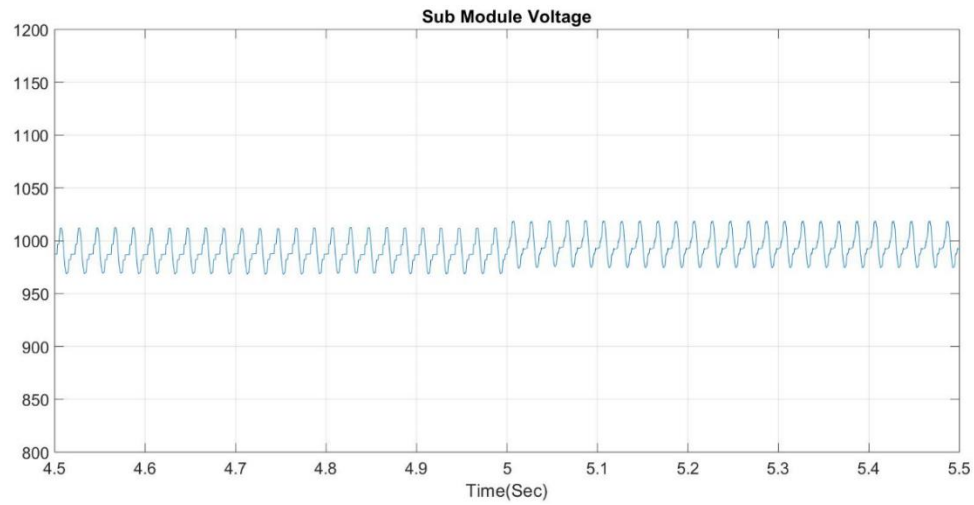
Fig. 3.28 Sub module voltage before and after applying the proposed design at t= 5 Sec and 100 Hz

switching frequency

Lowering the switching frequency will allow the idle capacitors have more time to be parallel with active capacitors during switching states which will lead to decreasing sub module voltage fluctuations and circulating current. This impact can clearly be seen at 100 Hz and 50 Hz switching frequencies.

Fig. 3.29 shows the circulating current variation before and after applying the new design. The content of circulating current decreased 80% after applying the new design at t=5 Sec.

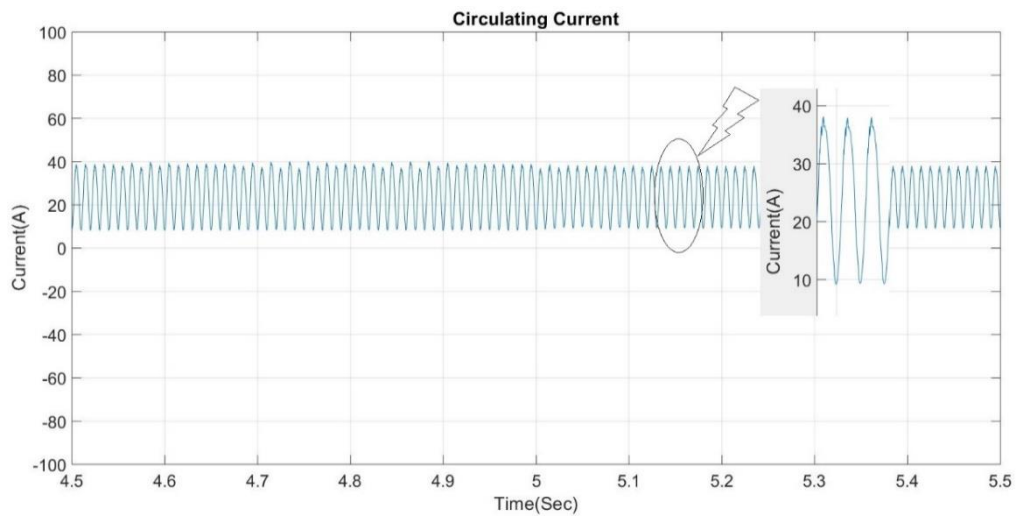*Fig. 3.29 Circulating current before and after applying the proposed design at t= 5 Sec and 100 Hz*
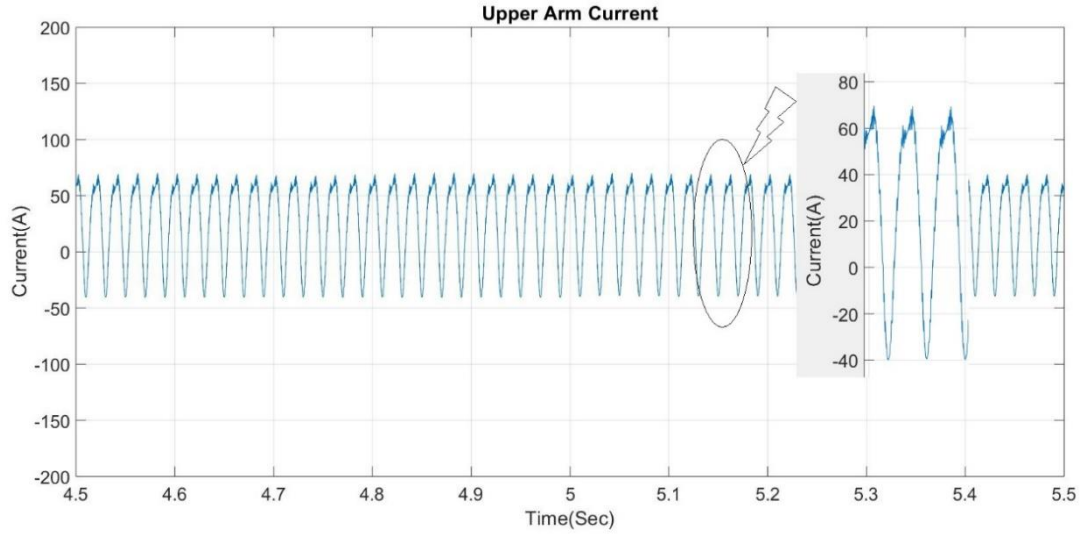
switching frequency

The amount of circulating current will be the same as 1000 Hz switching frequency after t=5 Sec when the new design comes to the circuit. Before t=5 Sec, the circulating current has quite large amplitude and after coming the new design the amplitude of circulating current will be limited.

Fig. 3.30 and Fig. 3.31 illustrate the upper arm and lower arm currents before and after t=5 Sec. The content of arm currents is limited after applying the proposed design.
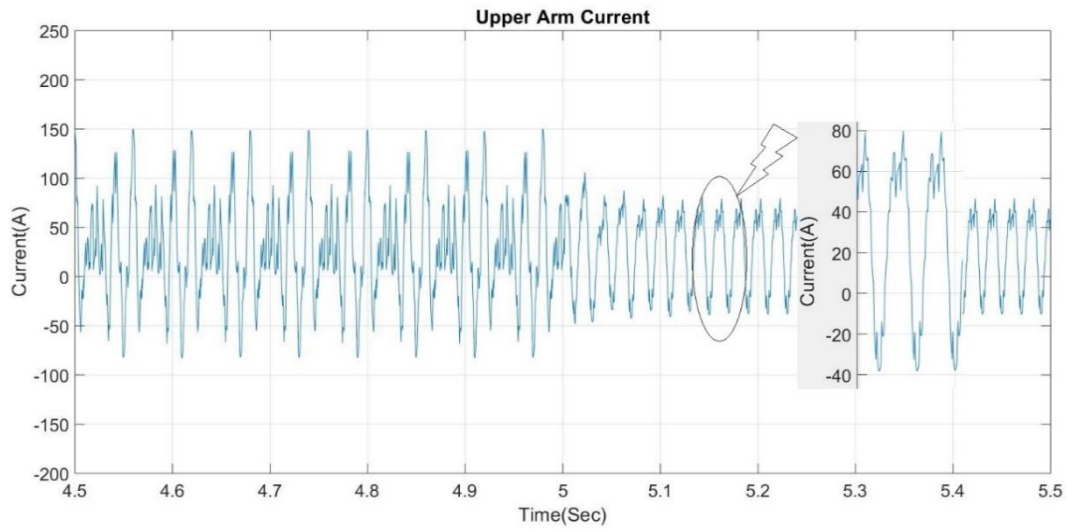
Fig. 3.30 Upper arm current before and after applying the proposed design at t=5 Sec and 100 Hz
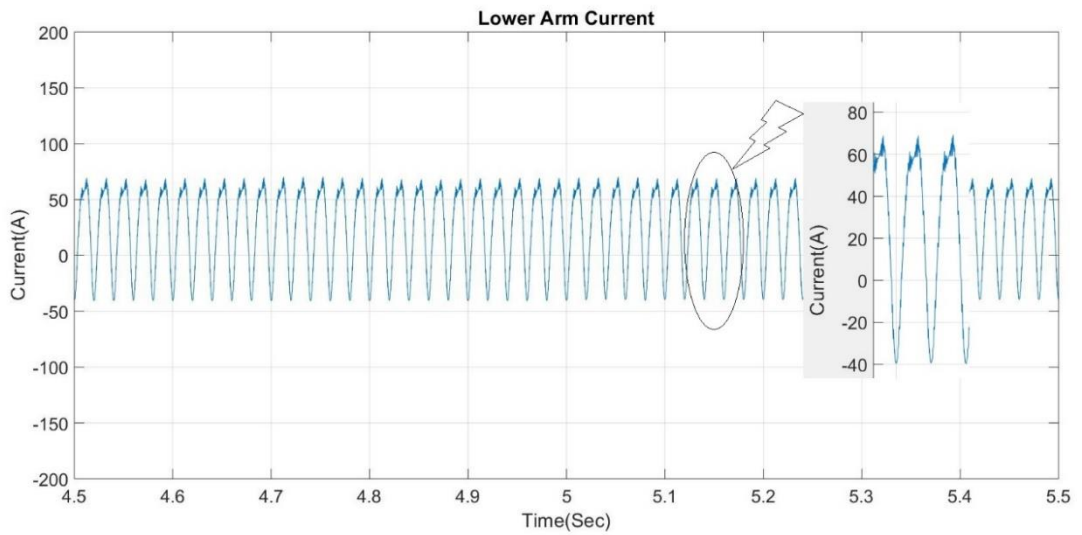
switching frequency
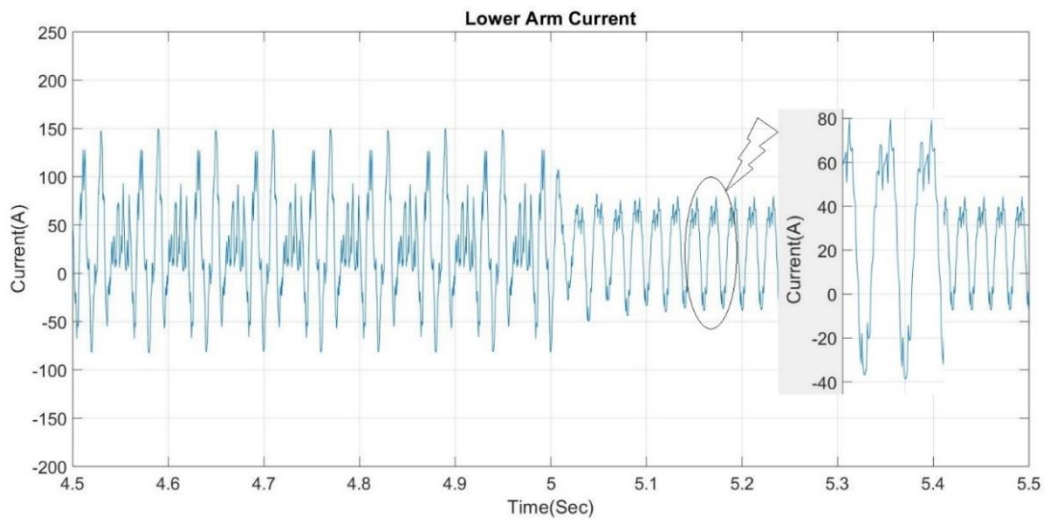
Fig. 3.31 Lower arm current before and after applying the proposed design at t=5 Sec and 100 Hz

switching frequency

Fig. 3.32 and Fig. 3.33 depict the output current and output voltage at 100 Hz switching frequency. When the new design comes to the circuit at t=5 Sec, output current and voltage waveforms will be more stable.
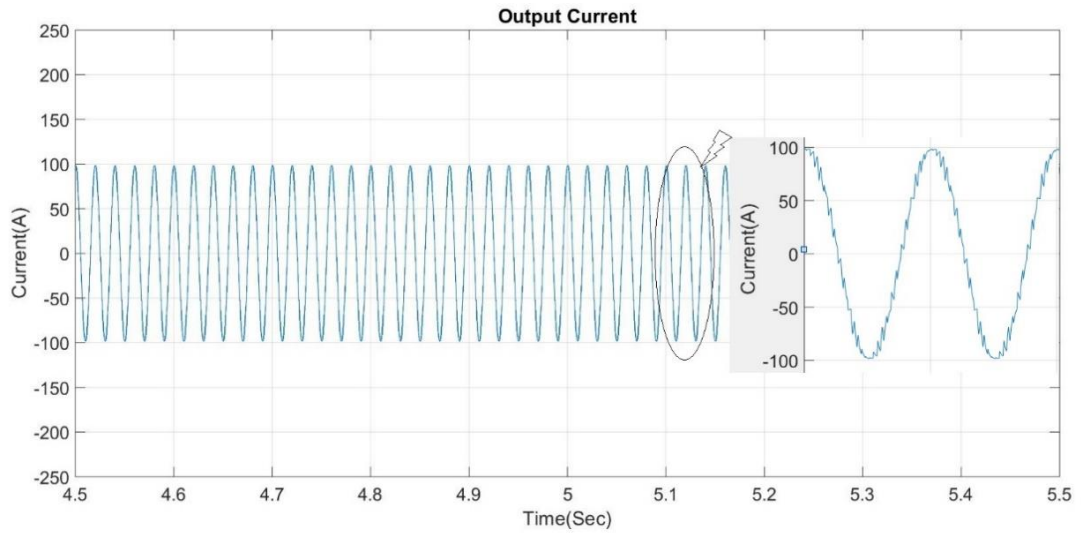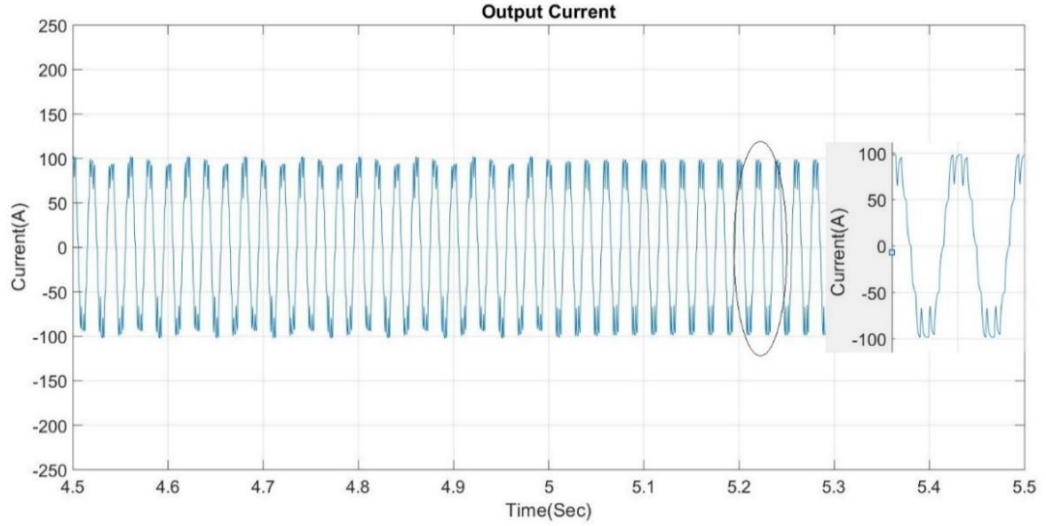

Fig. 3.32 Output current before and after applying the proposed design at t=5 Sec and 100 Hz switching frequency
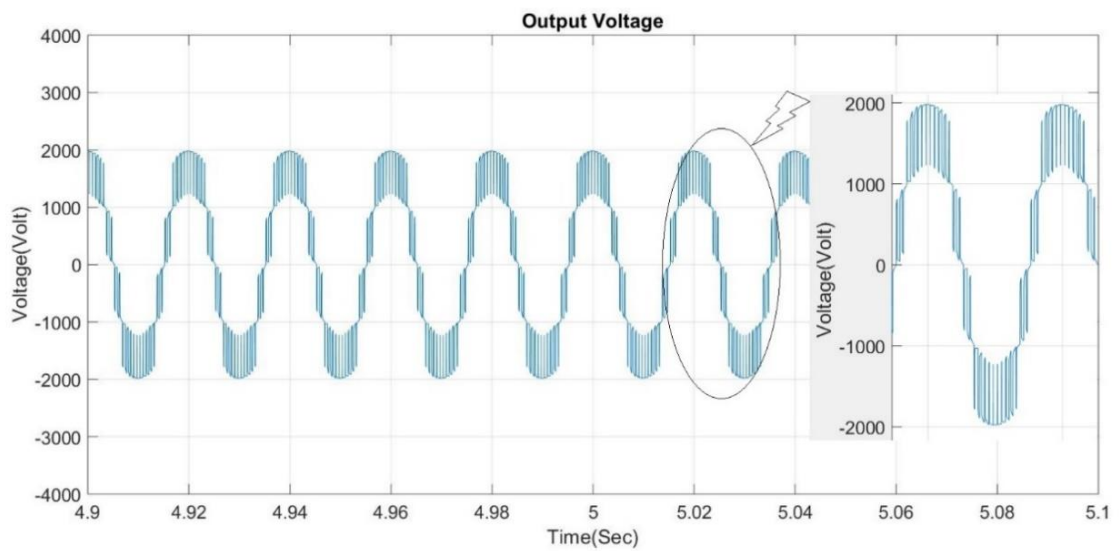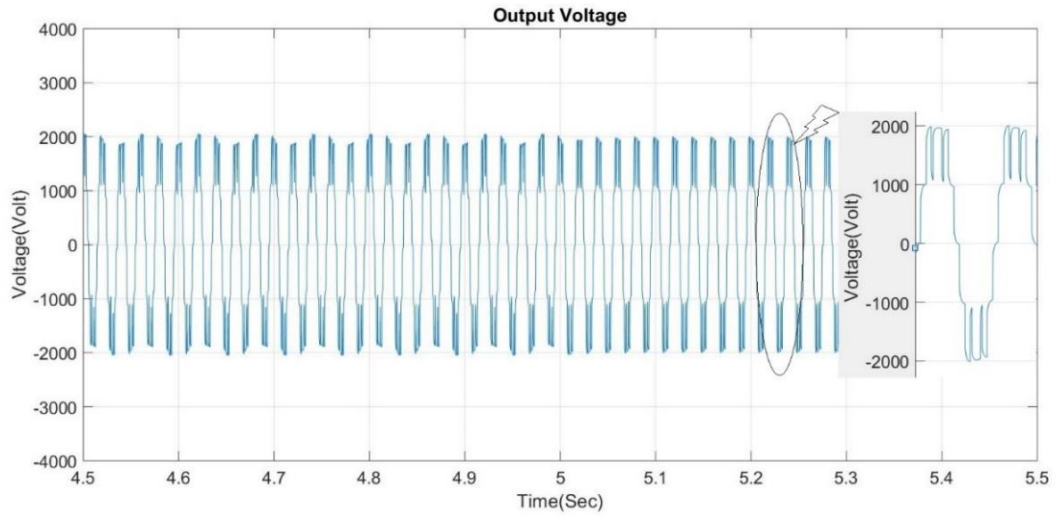

Fig. 3.33 Output voltage before and after applying the proposed design at t=5 Sec and 100 Hz switching frequency

3.3.3.1 Harmonic Analysis of Sub Module Voltage, Output Voltage and Circulating Current at 100 Hz switching frequency

Fig. 3.34 and Fig. 3.35 indicate the harmonic analysis of the sub module voltage and output voltage at 100 Hz switching frequency.

         (b)
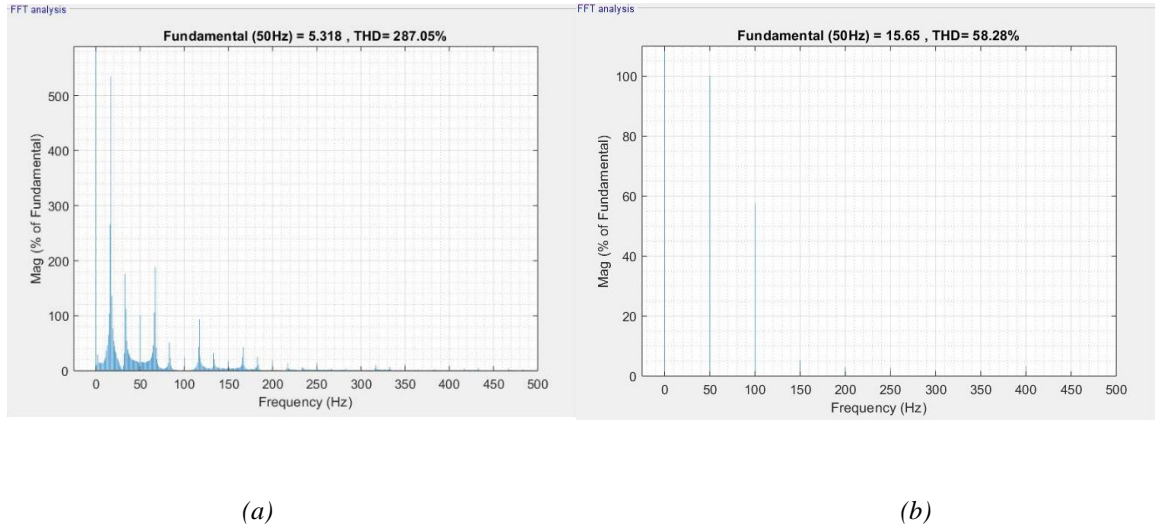
Fig. 3.34 Harmonic analysis of sub module voltage at 100 Hz switching frequency (a) before applying the new design (b) after applying the new design

Before applying the new design, the THD of sub module voltage is high because of existing sub harmonics and other harmonic orders. However, when the new design comes to the circuit THD will be improved from 287.05% to 58.28% significantly and all sub harmonics will be eliminated.
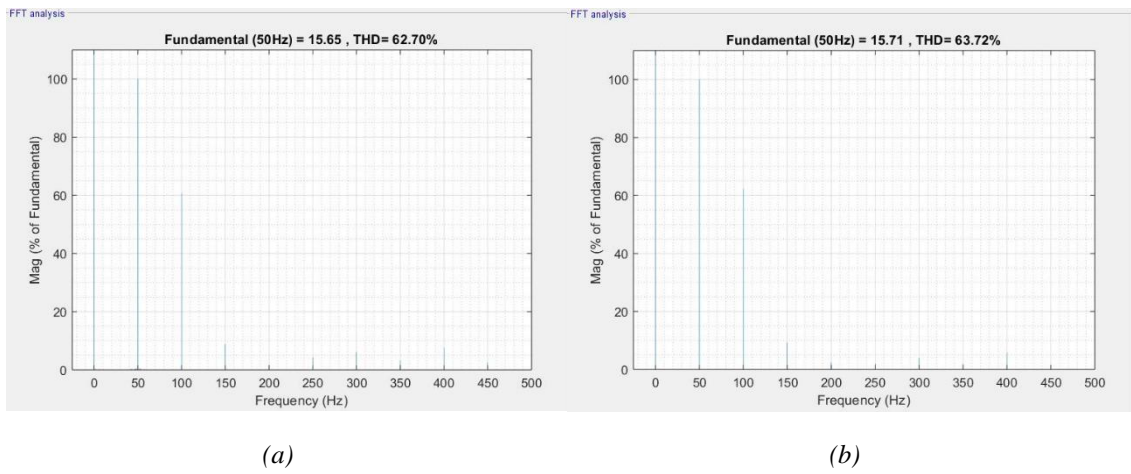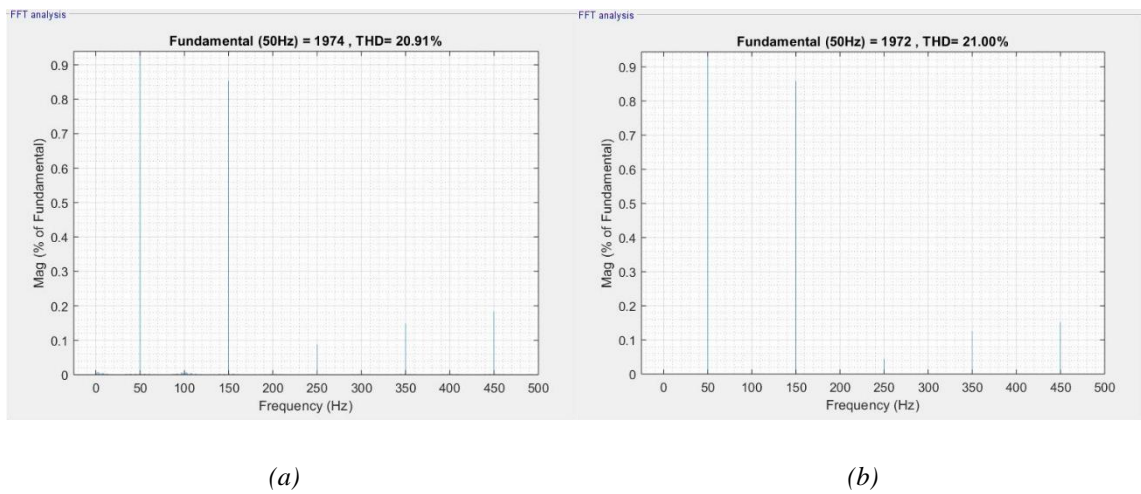

(a)   *(b)*

Fig. 3.35 Harmonic analysis of output voltage at 100 Hz switching frequency (a) before applying the new design (b) after applying the new design

Fig. 3.35 shows the harmonic contents of output voltage which has coefficients of 3rd harmonics and all extra unwanted harmonic contents will be eliminated applying the new topology.

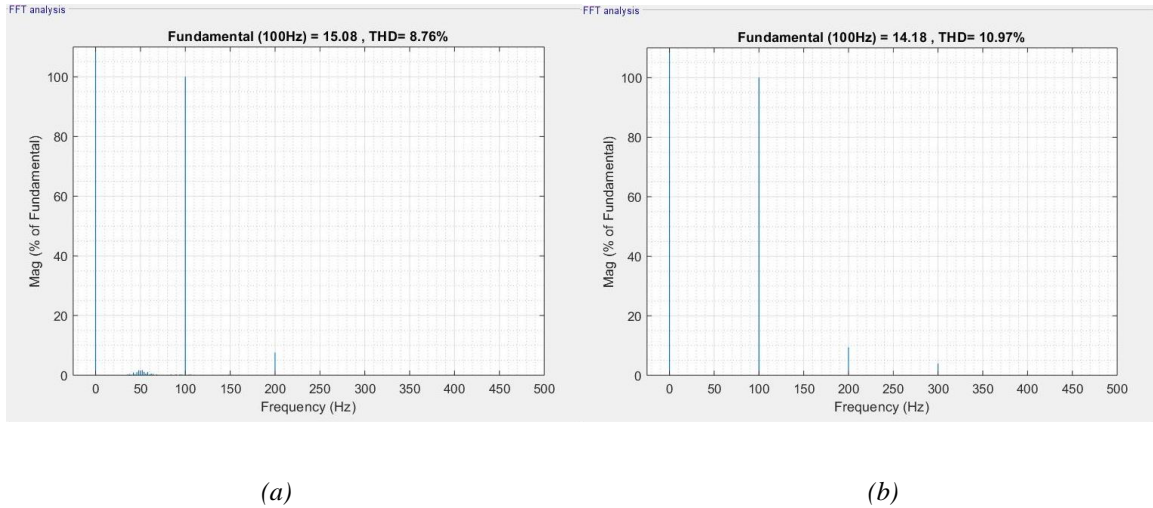*(a)*   *(b)*
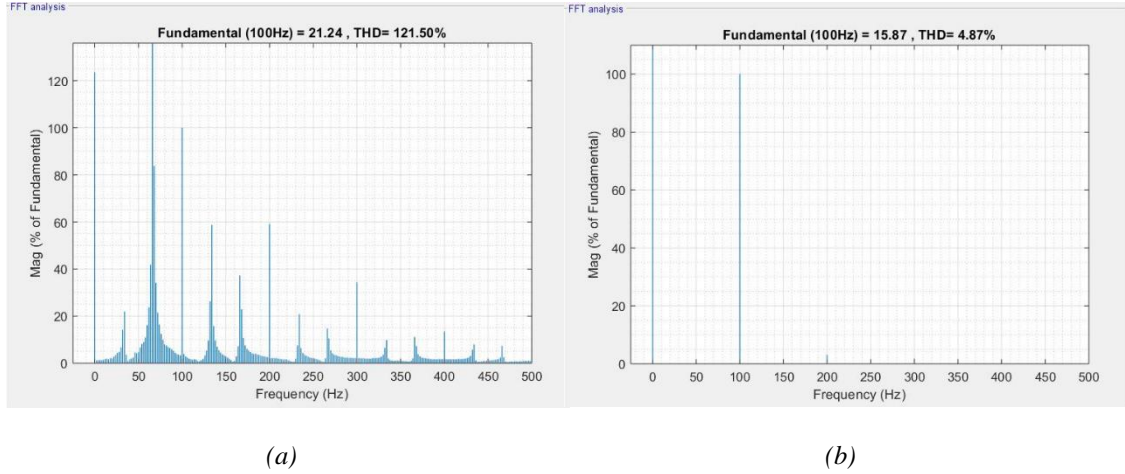
Fig. 3.36 Harmonic analysis of circulating current at 100 Hz switching frequency (a) before applying the new design (b) after applying the new design

Fig. 3.36 depicts the harmonic content of circulating current before and after applying the new topology. The circulating current has very high THD because some other extra harmonic contents exist and the second order harmonic is the dominant harmonic value. After applying the new topology THD will be improved from 121.5% to 4.87% and the content of second order harmonic will be decreased.

3.3.4 Simulation Results at 50 Hz Switching Frequency

Fig. 3.37 shows the sub module voltage variation at 50 Hz switching frequency. The proposed design decreases the sub module voltage ripples when comes to the circuit at t=5 Sec. The sub module voltage has very high fluctuation and is not adjusted to 1kV before applying the new design. This is because of very low switching frequency and sub module voltage controller is not able to set the voltage. However, the new design sets the sub module voltage and decreases sub module voltage fluctuations.
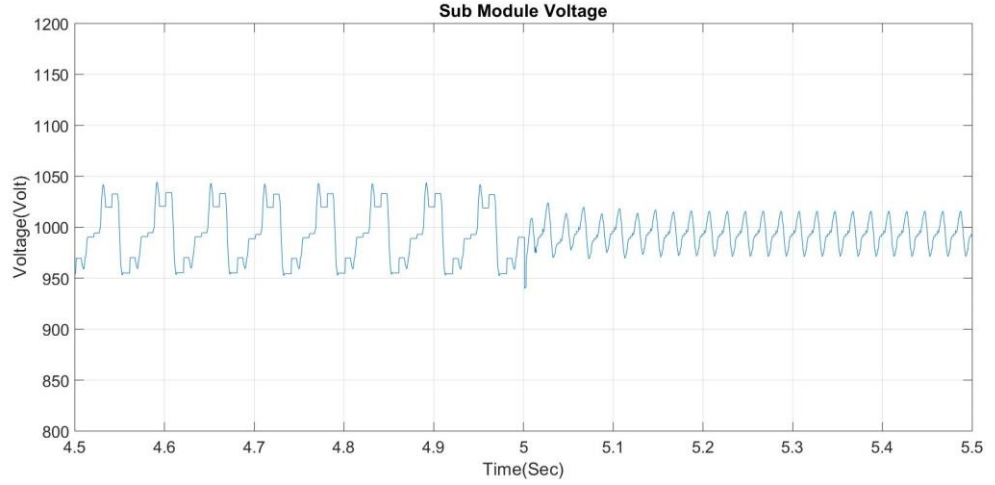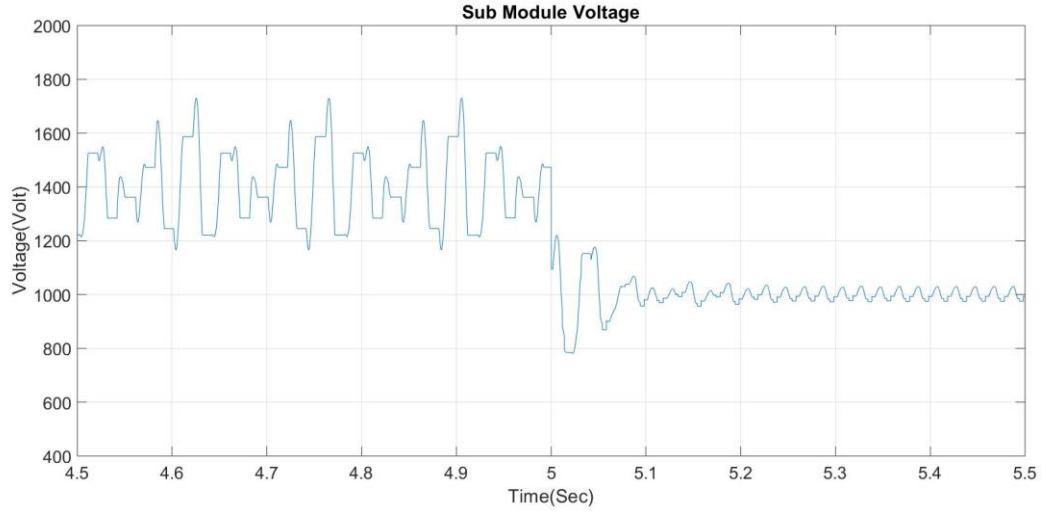
Fig. 3.37 Sub module voltage before and after applying the proposed design at t= 5 Sec and 50 Hz

switching frequency

The variation of circulating current has been shown in Fig. 3.38. It has very high fluctuations before t=5 Sec and its content will be decreased after applying the new design.
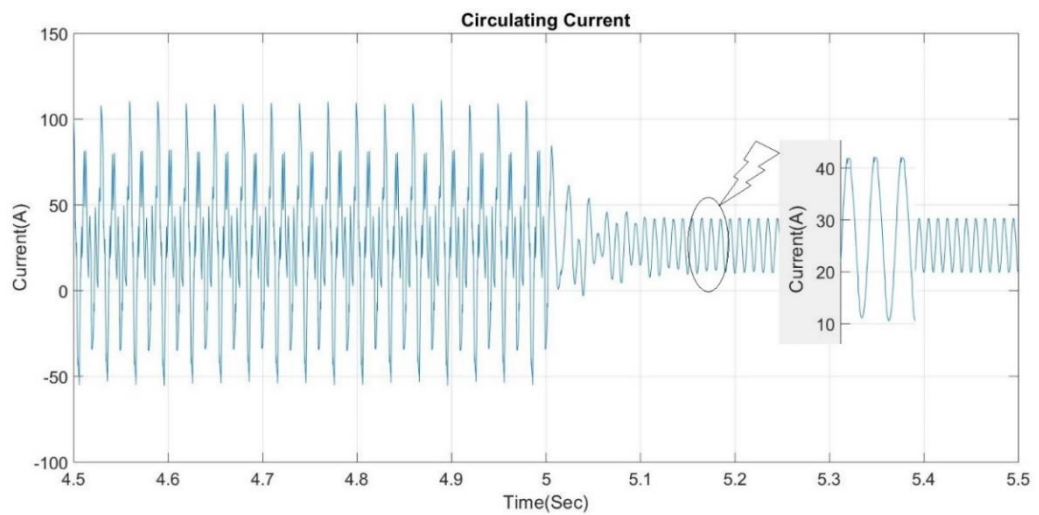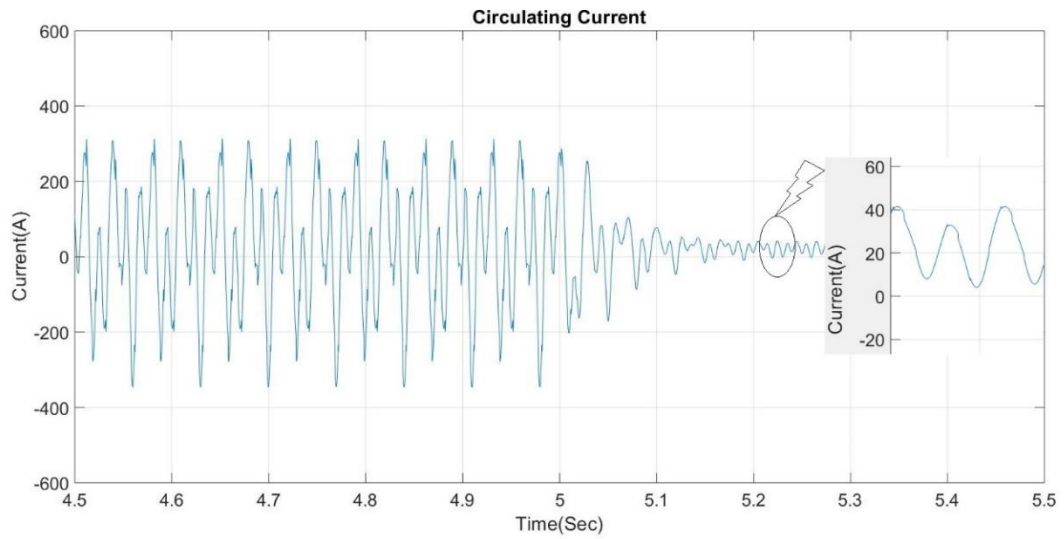

Fig. 3.38 Circulating current before and after applying the proposed design at t= 5 Sec and 50 Hz

switching frequency

Fig. 3.39 and Fig. 3.40 show the upper arm and lower arm currents before and after t=5 Sec. The content of arm currents are limited after applying the proposed design.
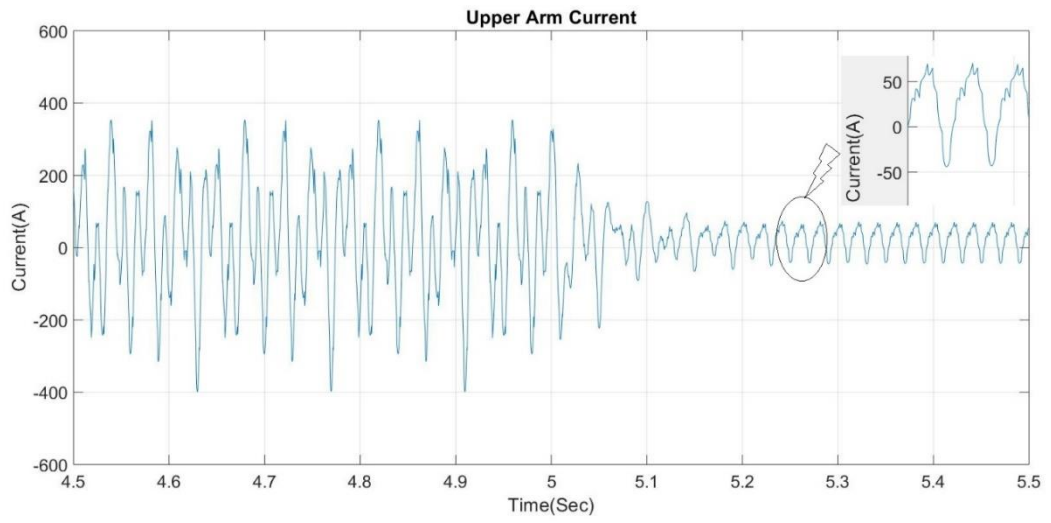
Fig. 3.39 Upper arm current before and after applying the proposed design at t=5 Sec and 50 Hz

switching frequency
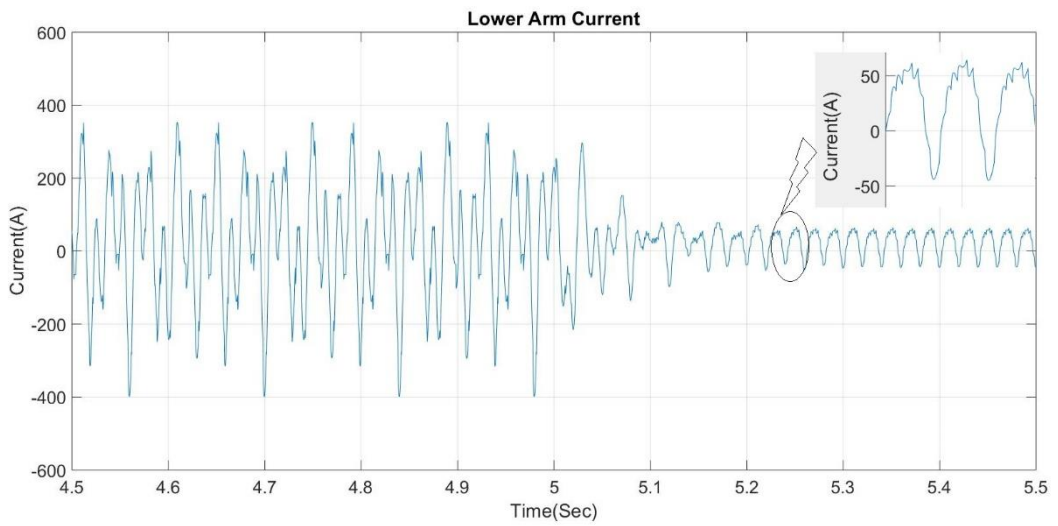
Fig. 3.40 Lower arm current before and after applying the proposed design at t=5 Sec and 50 Hz

switching frequency

Fig. 3.41 and Fig. 3.42 depict the output current and output voltage at 100 Hz switching frequency. Output current and voltage are more stable after applying the new design.
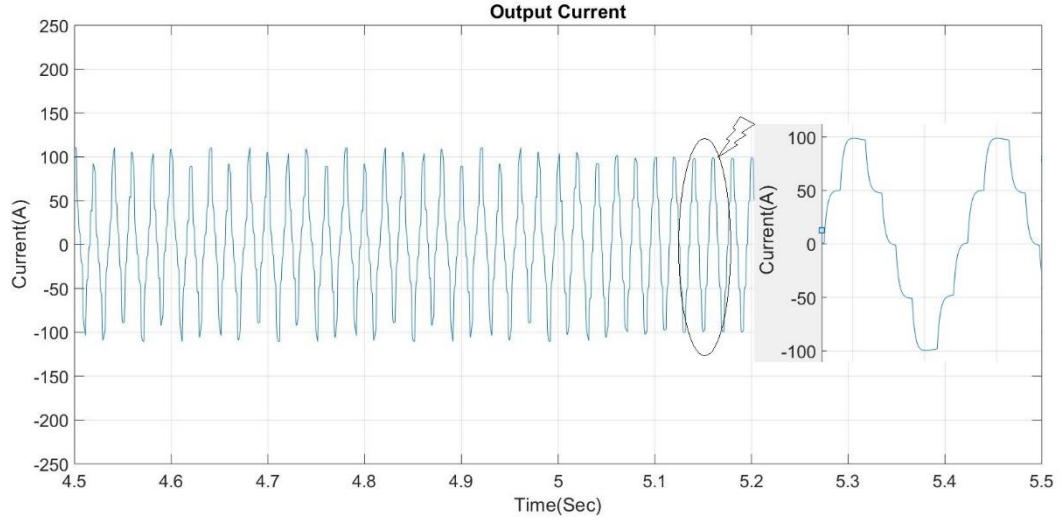
Fig. 3.41 Output current before and after applying the proposed design at t= 5 Sec and 50 Hz switching
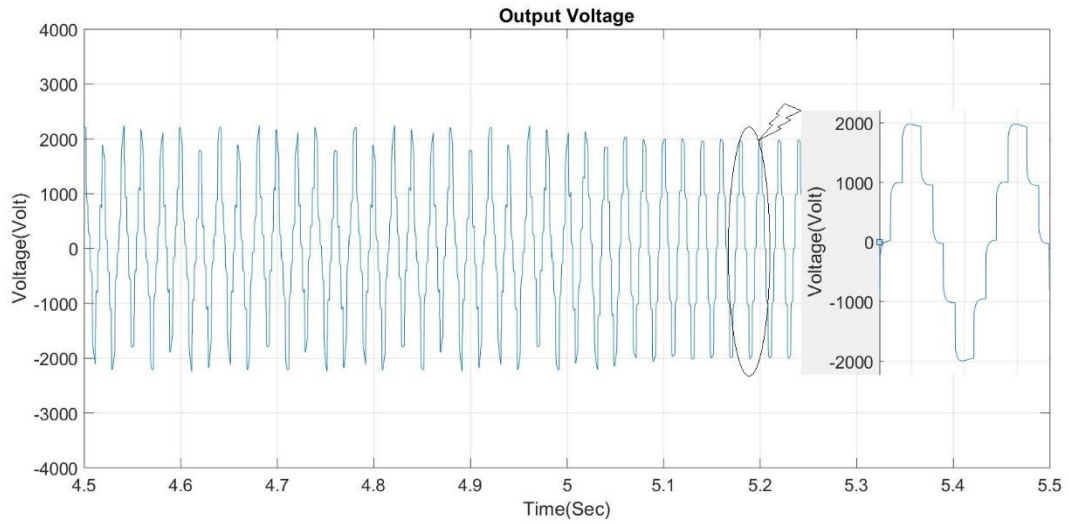
Fig. 3.42 Output voltage before and after applying the proposed design at t= 5 Sec and 50 Hz switching

3.3.4.1 Harmonic Analysis of Sub Module Voltage, Output Voltage and Circulating Current at 50 Hz switching frequency

Fig. 3.43 and Fig. 3.44 indicate the harmonic analysis of the sub module voltage and output voltage at 50 Hz switching frequency.

(a)   *(b)*
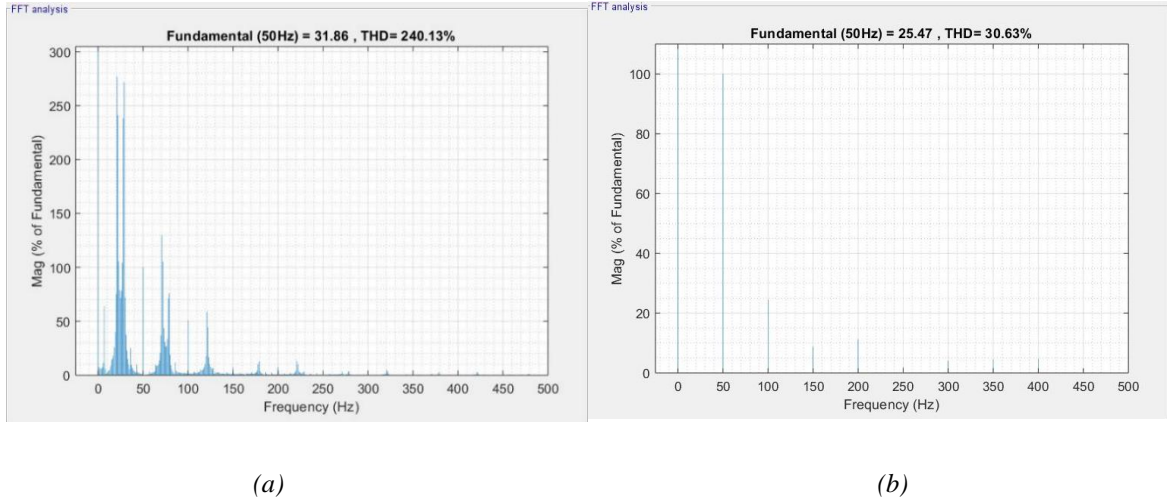
Fig. 3.43 Harmonic analysis of sub module voltage at 50 Hz switching frequency (a) before applying the new design (b) after applying the new design

The sub module voltage includes sub harmonics and high THD value. However, the new topology eliminates sub harmonic contents and improves the THD value from 240.13% to 25.47%. The main harmonic contents are fundamental, 2nd, 3rd and 4th.

(a)   *(b)*
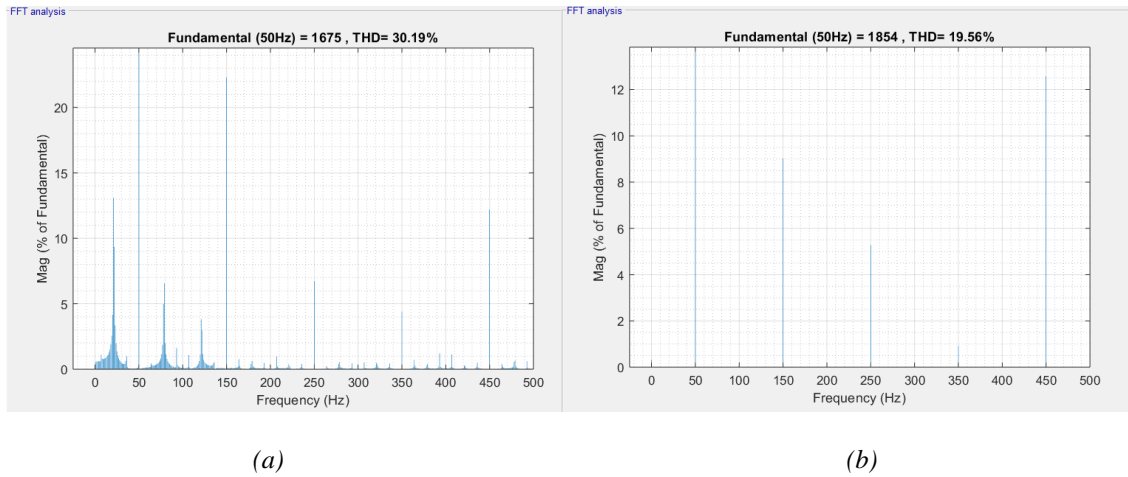
Fig. 3.44 Harmonic analysis of output voltage at 50 Hz switching frequency (a) before applying the new design (b) after applying the new design

Fig. 3.44 illustrates the harmonic contents of output voltage which has sub harmonics before t=5 Sec. After applying the new design all sub harmonics are eliminated and the

THD of output voltage is improved from 30.19% to 19.56%. Main harmonic orders are 3rd, 5th and 7th.
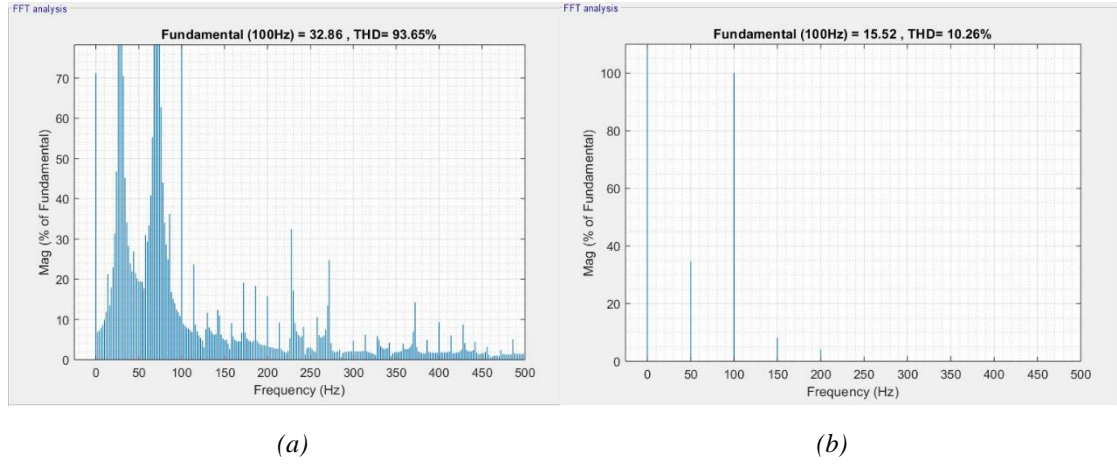
Fig. 3.45 Harmonic analysis of circulating current at 50 Hz switching frequency (a) before applying the new design (b) after applying the new design
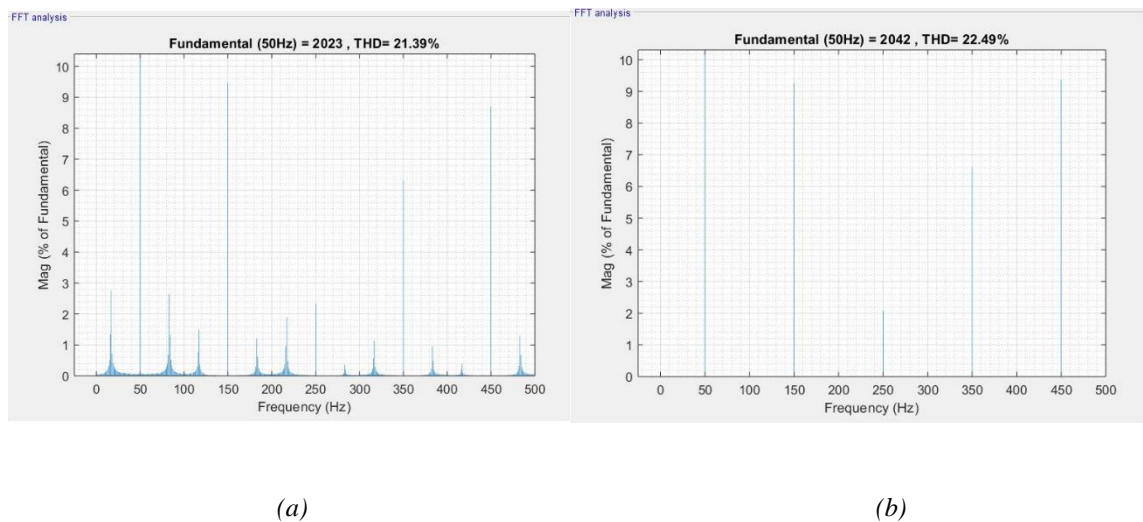
According to Fig. 3.45, the circulating current has very high THD because some other extra harmonic contents exist. However, after applying the new topology the THD will be improved from 93.65% to 10.26% and the content of second order harmonic will be decreased as a main harmonic order.

3.4 Loss and Efficiency Calculations

This section introduces a loss and efficiency calculation for the half bridge sub module DC side cascaded and the proposed topology. Then, loss and efficiency comparison between two topologies is presented. There are several methods of loss calculation for the MMC: e.g. calculation using adjustment of switching waveforms [139], calculation using the linear interpolation and semiconductor energy [140] and using real-time waveforms and temperature feedback [141]. The calculations of the losses in the switches are quite important for the design of a power converter. These electrical losses in the switches are translated to heat, that will increase the temperature of the switches. All this thermal energy must be extracted to the ambient to avoid excessive temperatures in the

switches that could damage or even destroy them. To do so, a proper heatsink must be added to the system.

There are four different types of loss for any kind of power electronics device which are: 1) Conduction losses, 2) Switching losses, 3) OFF-state losses and 4) Gate losses [142]. The Off-state and Gate losses are very small and normally neglected. Hence, in this thesis, only conduction and switching losses have been considered for the comparative analysis. Blaabjerg et al [143] presents the exact method for the inverter losses calculation. However, loss calculation for high power rated inverters are to be customised because of the number of series switches to withstand nominal voltage and parallel switches to withstand the rated current needs to be precisely considered. Computer simulation is one of the most powerful methods to calculate and evaluate the losses in a MMC converter. In this case the accuracy of loss calculations depends on how well the computer model is designed to reflect the real-world conditions.

The on-state voltage drop in the device produces the conduction losses. These losses are computed by averaging the conduction losses in each switching cycle as shown in equation (3.2) where f_s is the switching frequency and $\omega = 2\pi f_s$:

$$P_{cond} = \frac{1}{T} \int_0^T V_f\,(\omega t)\,i\,(\omega t)\,dt \tag{3.2}$$

Where, P_{cond} shows the conduction losses of the device, $V_f(\omega t)$ shows the forward voltage drop of the device and $i(\omega t)$ represents the current flowing through the device during the conduction period. T is the switching period. The forward voltage drop is calculated by using the following equation:

$$P_{cond} = V_f I_{av} + I_{rms}^2 r_f \tag{3.3}$$

I_{av} is the average current flowing through the device while I_{rms} is the root mean square value of the current flowing through the device for the conduction period of the switching

cycle [144]. These values of the current are calculated by using equation (3.4) and (3.5) respectively.

$$I_{av} = \frac{1}{T} \int_0^T i\,(\omega t)\,dt \tag{3.4}$$

$$I_{rms}^2 = \frac{1}{T} \int_0^T i^2(\omega t)\,dt \tag{3.5}$$

$$P_{sw} = \frac{f_s}{2\pi} \int_0^T k\,i\,(\omega t)\,dt \tag{3.6}$$

Where P_{sw} are the device switching losses, k is constant and is obtained from the switching energy graph of the device which is given in the data sheet. f_s is the switching frequency of the device. The switching frequency has a direct impact on the switching losses. For the loss calculation, the current and voltage waveforms of the switching devices must be known.

The present thesis analyses the power losses in both classic half bridge DC side cascaded and new design at four different switching frequencies and compares their overall efficiency using the computer simulation-based method.

3.4.1 Switch Selection

According to the simulation parameters (Table. 3.3), the DC link voltage is 4 kV and with considering 8 sub modules across both arms, the sub module voltage is 1 kV. The characteristics of the converter switches are obtained from the datasheets of the (ABB 1.7 kV, 800 A) switch which will be uploaded to the loss calculation program. A safety coefficient of 1.15 has been applied to the IGBT voltage ratings to ensure it can withstand the DC link voltage. Sajedi et al [145] provides additional details about the loss and efficiency calculations.

3.4.2 Heat Sink

All the calculated losses must be dissipated to avoid excessively high temperatures that can damage the IGBTs. The packages of the switches are sealed enclosures and do not extract heat easily. For this reason, they need a heatsink to evacuate the generated thermal power. The thermal models are similar to electrical ones. The temperature can be considered as the voltage, the power losses as the current and all the material between the switch and the ambient have a resistance. The thermal model of the IGBT is shown in Fig. 3.46.
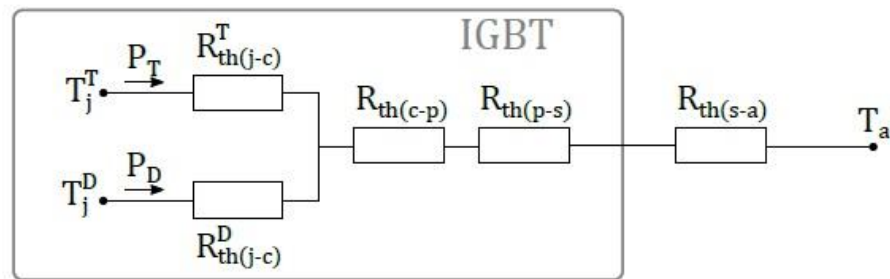
Fig. 3.46 Thermal model of IGBT

The losses of the IGBT P_T and diode P_D can be calculated and the maximum temperature in the junction T_j can be fixed to a desired value. This value must be low enough to avoid damaging the switches; the ambient temperature T_a is set to a reasonable value. All the thermal resistances of the different elements (diode, IGBT, case and electrical isolator) are known except the heatsink's one. So, a maximum resistance for the heatsink must be calculated to ensure that the temperature of the junction does not exceed the imposed limit. Afterwards, a heatsink available in the market with a lower thermal resistance must be selected. Where:

T_j is the temperature of the junction of the transistor or diode

T_a is the ambient temperature

P is the losses of the transistor or diode

$R_{th(j-c)}$ is the thermal resistance from the junction to the case of the transistor or diode

$R_{th(c-p)}$ is the thermal resistance from the case to the electrical isolator

$R_{th(p-s)}$ is the thermal resistance from the electrical isolator to the heatsink

$R_{th(s-a)}$ is the thermal resistance from the heatsink to the ambient

In the loss and efficiency calculations using the simulation program, all thermal details of a switch will be uploaded to the program according to the switch datasheet.

3.4.3 Damping Resistors

The proposed topology has some additional switches and the damping resistors (small value resistors) which should be added in series with additional switches. The damping resistors are included in the circuit to limit inrush currents during the switching process. Without considering damping resistors, a huge inrush current will flow through additional switches which can increase the switching losses and conduction losses. Considering (ABB 1.7 kV, 800 A) switch which has the voltage stress of (V_{DC} /4) the amount of damping resistor is:

$$R_{damp} = \frac{1000}{800} = 1.25\Omega$$

Damping resistors are essential part to eliminate inrush currents and protect the switches. However, existence of damping resistors for a long period in the circuit will have a big contribution in system losses and will decrease the efficiency [146]. Therefore, they can be considered during the start-up period for a short time and then be eliminated from the circuit.

Du et al [147] introduces a soft-start resistor and a bypass switch at the DC bus to limit the inrush current in the start-up process. Fig. 3.47 shows the circuit diagram of the proposed topology including damping resistors. In the efficiency and total loss calculations, the damping resistor losses are also considered.
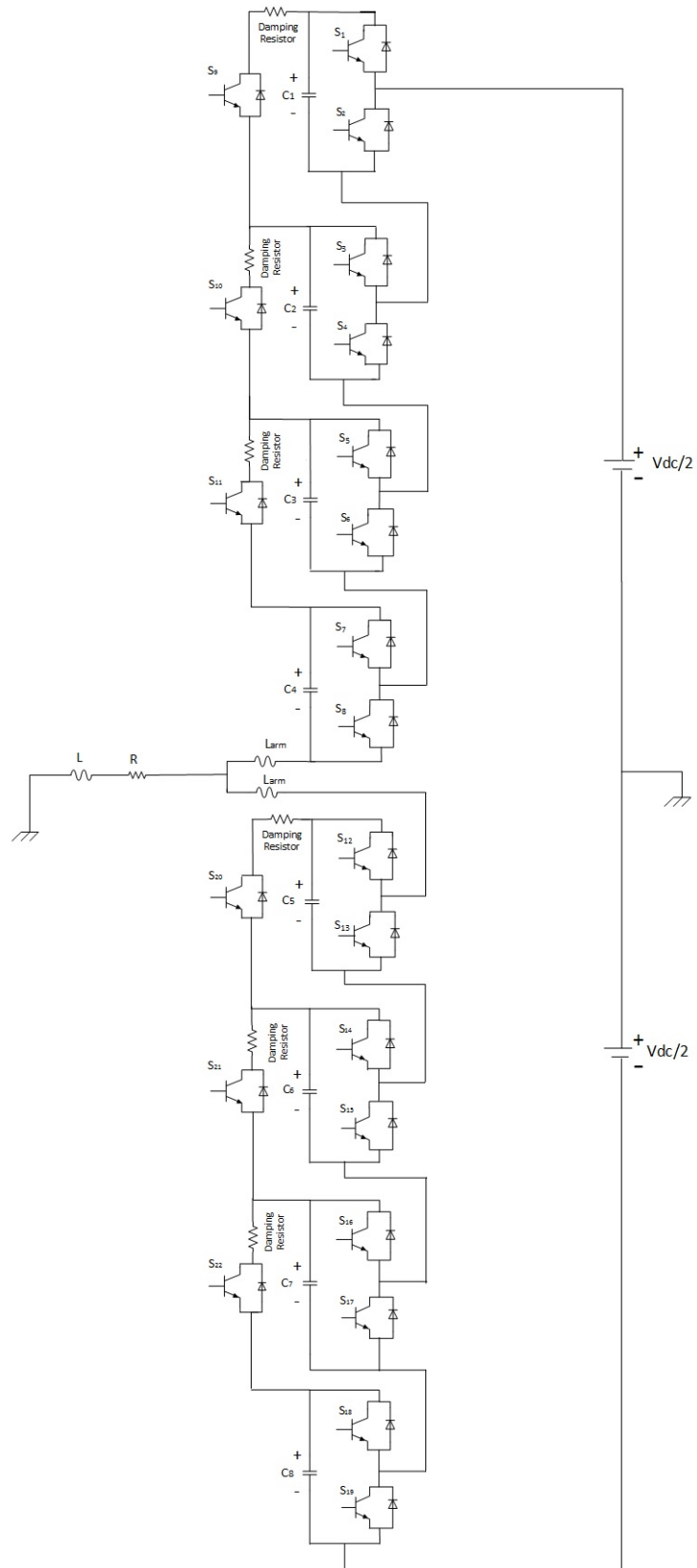
Fig. 3.47 Circuit diagram of the proposed topology including damping resistors

3.4.4 Loss and Efficiency Analysis of the Classic Half Bridge MMC Versus the Proposed New Topology

Fig. 3.48 shows the variation of the switching losses at four different switching frequencies (1000 Hz, 400 Hz, 100 Hz, 50 Hz) for the classic half-bridge MMC topology and the proposed topology. The increase of switching frequency will have significant impact on the switching losses.
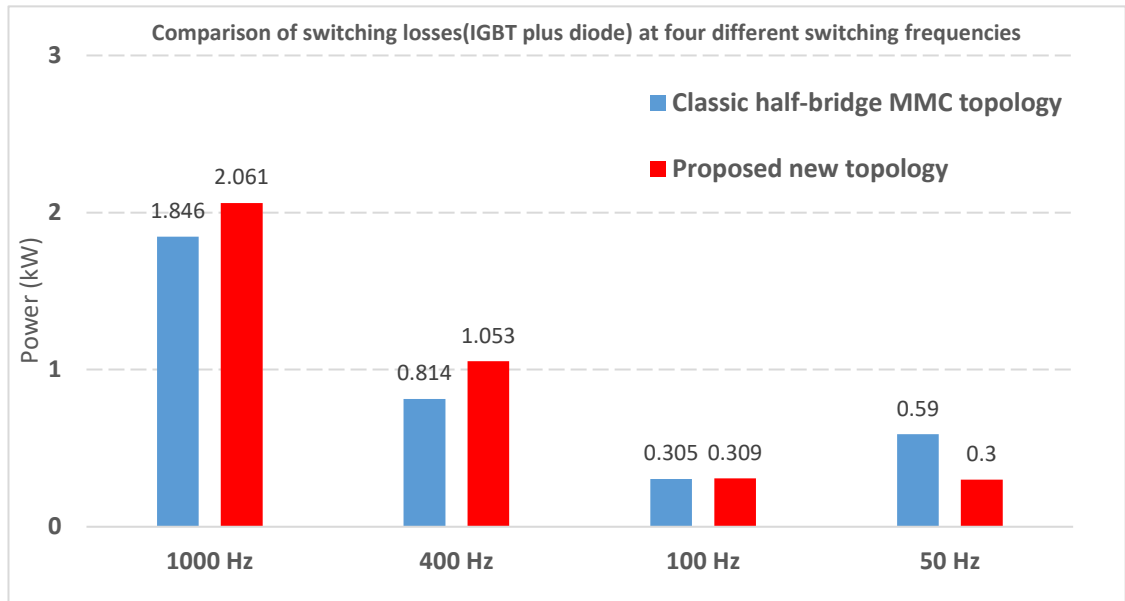
Fig. 3.48 Comparison of switching losses (IGBT plus diode) at four different switching frequencies considering classic half-bridge MMC topology and proposed new topology

The amount of switching losses at 1000 Hz and 400 Hz switching frequencies is higher for the proposed topology. This is because of the additional switches in the proposed topology. However, at lower switching frequencies the proposed design has lower switching losses.

Fig. 3.49 depicts the comparison of conduction losses at four different switching frequencies. At higher switching frequencies (1000 Hz and 400 Hz) the amount of conduction losses in the proposed topology is slightly more than classic half-bridge MMC because of existing additional switches. Decreasing the switching frequency will

lead to the higher values of conduction losses for the classic topology. However, the proposed design can eliminate the conduction losses to the range of higher switching frequency values (the amount of conduction losses at 100 Hz switching frequency is approximately identical with 1000 Hz switching frequency).
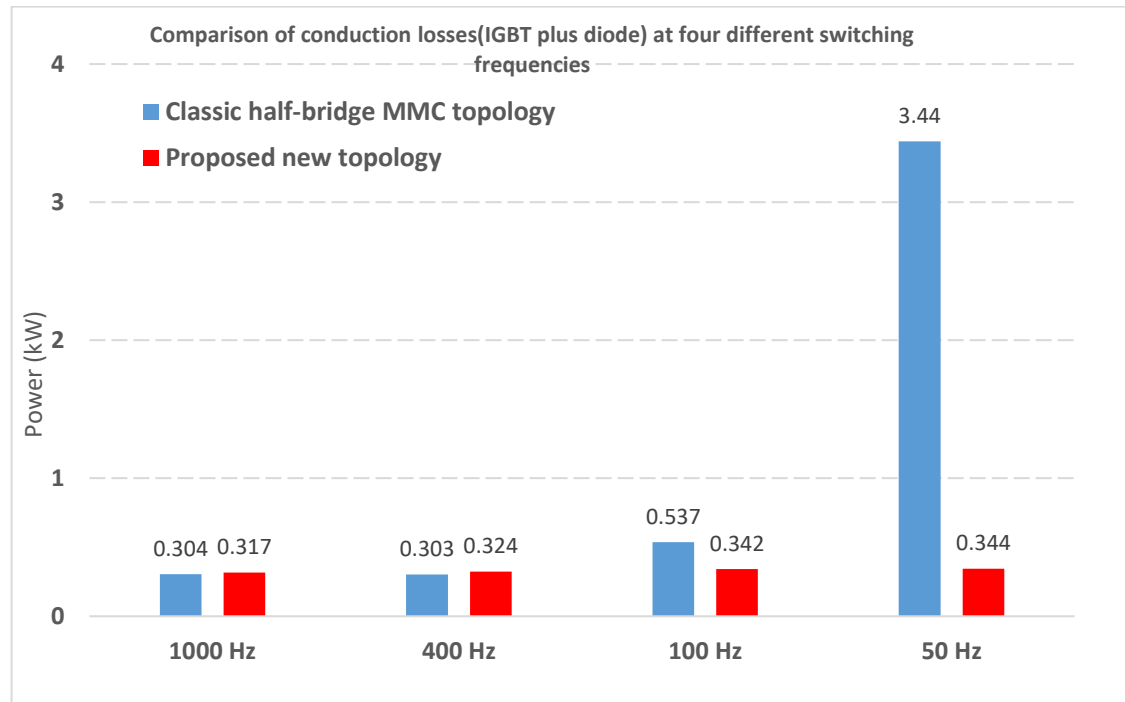
Fig. 3.49 Comparison of conduction losses (IGBT plus diode) at four different switching frequencies considering classic half-bridge MMC topology and proposed new topology

As mentioned before, damping resistors have contribution in total loss calculations and should be considered. For the higher switching frequencies, the amount of damping resistor losses is less than lower switching frequencies. Fig. 3.50 shows damping resistors losses which can be considered only in the new proposed design.
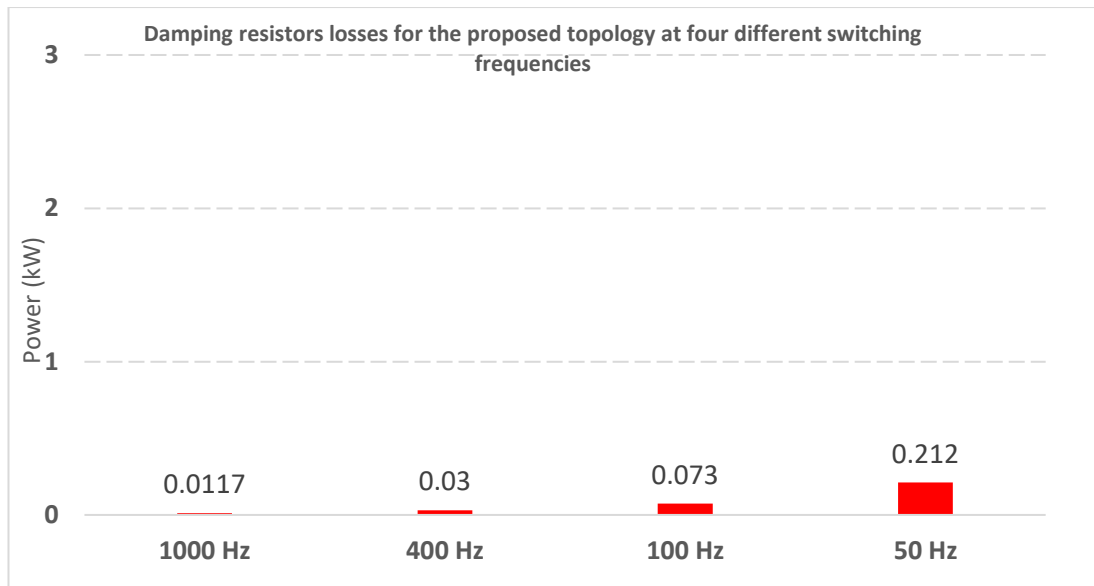
Fig. 3.50 Comparison of damping resistor losses at four different switching frequencies considering

proposed new topology

The total loss comparison is shown in Fig. 3.51. The switching losses are very high at 400 Hz and 1000 Hz switching frequencies. The total loss comparison between 100 Hz and 50 Hz shows that the 100 Hz switching frequency with the new design can be considered as an optimal switching frequency since it has lower switching losses as well as lower conduction losses and damping resistor losses.
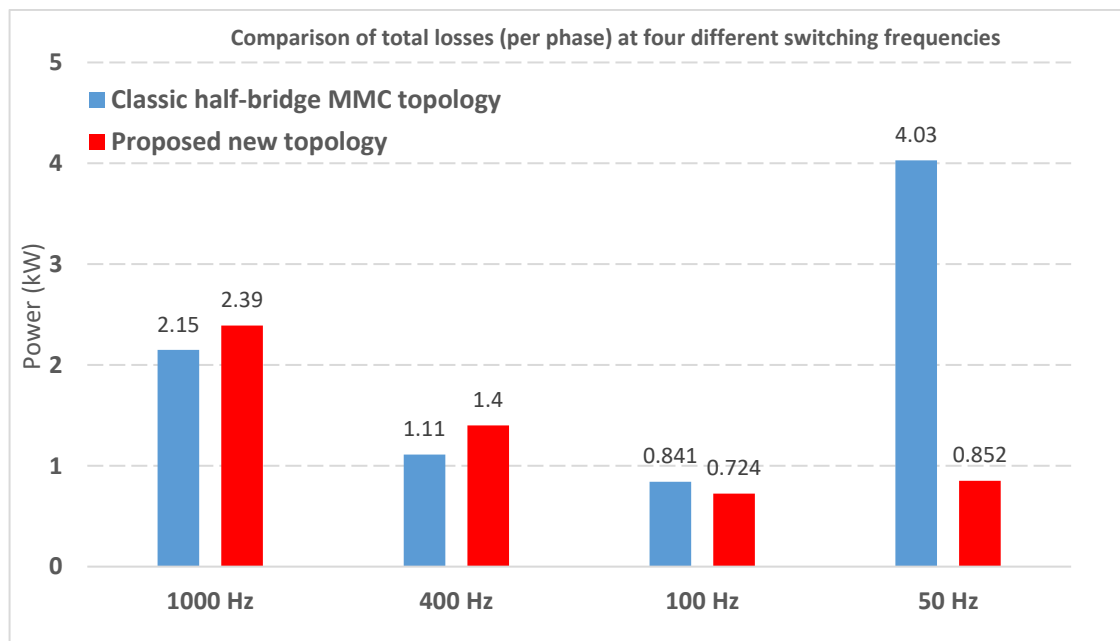
Fig. 3.51 Comparison of total losses (per phase) at four different switching frequencies considering

classic half-bridge MMC topology and proposed new topology

Fig. 3.51 show the comparison of total converter losses for each phase at four different switching frequencies.

Table. 3.4 shows the converter efficiency comparison between the classic half-bridge MMC and the proposed topology at four different switching frequencies. Applying the new proposed design at 100 Hz switching frequency gives the best efficiency. Moreover, 100 Hz switching frequency could be considered as an optimum frequency as it gives the highest efficiency for both topologies.

Table. 3.4 The converter efficiency at four different switching frequencies

Switching Frequency	1000 Hz	400 Hz	100 Hz	50 Hz
Efficiency of the classic half-bridge MMC topology	97.85%	98.88%	99.16%	95.20%
Efficiency of the proposed topology	97.61%	98.59%	99.31%	99.02%

3.5 Analysis of The New Topology Considering Hybrid MMC (Mixture of Half-bridge and Full Bridge Sub Modules)

In this section, circuit analysis and operation of the proposed design considering the hybrid topology is discussed.

3.5.1 MMC Hybrid Topology

Fig. 3.52 shows one leg of the hybrid MMC. It consists of upper and lower arms which are connected to the midpoint of the leg through buffer inductors. Each arm is constructed by cascade connection of full bridge and half bridge submodules [148].
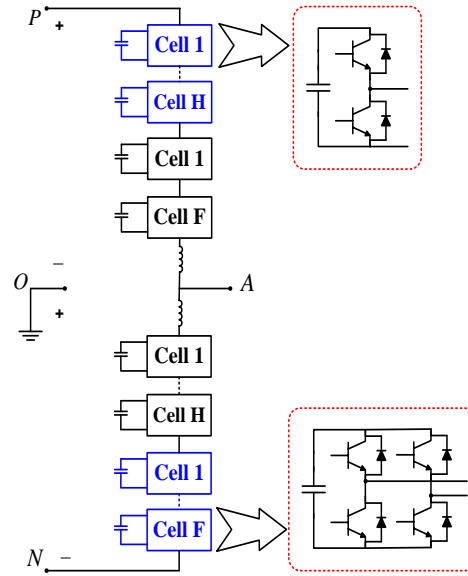
Fig. 3.52 One leg structure of hybrid MMC

Compared with the half-bridge MMC, the hybrid MMC has more control degrees of freedom. It is because the arm sub module clusters can generate negative voltages, which causes the modulation index greater than 1, named over-modulation. The hybrid MMC not only has DC fault blocking capability but also uses fewer semiconductor devices and has lower power loss than the full bridge MMC. However, in contrast to the conventional MMC in which all the sub modules are identical, sub modules in the Hybrid MMC function differently in the charging and discharging periods and therefore, their capacitor voltage ripple and balancing need to be carefully analysed. Paper [28] analyses the operating principles of a hybrid modular multilevel converter (MMC).

3.5.2 Proposed Topology Considering Hybrid MMC

Fig. 3.53 shows the circuit diagram of the proposed topology considering hybrid topology.
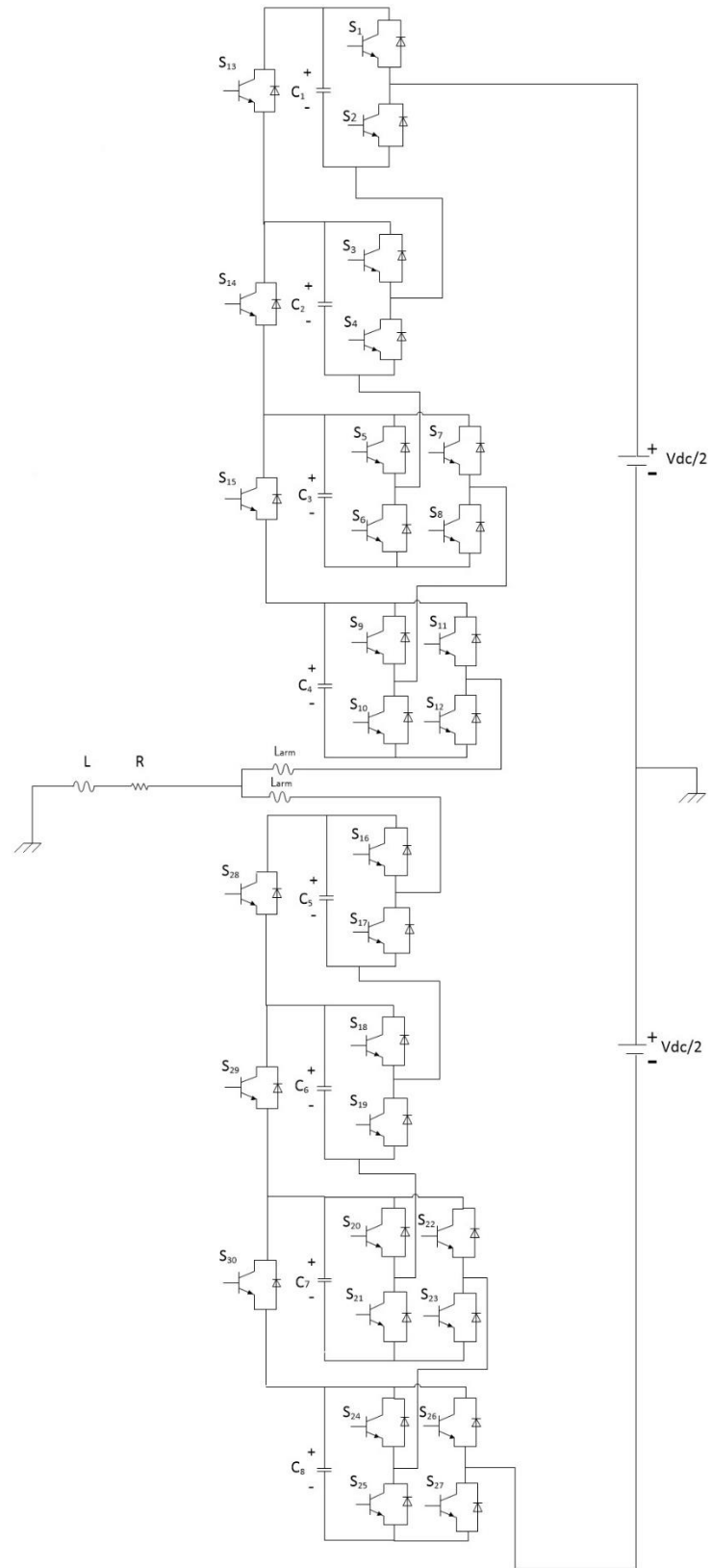
Fig. 3.53 the circuit diagram of the proposed topology considering hybrid topology

The operation principle is similar to half bridge topology. However, applying the new proposed design on hybrid structure is not practical. This is because of existing some impractical states during the switching process which prevent the paralleling of capacitors. Fig. 3.54, shows one of the states. In this state, S_3 is ON, S_6 and S_8 are ON then S_{14} should be ON to parallel C_2 and C_3.
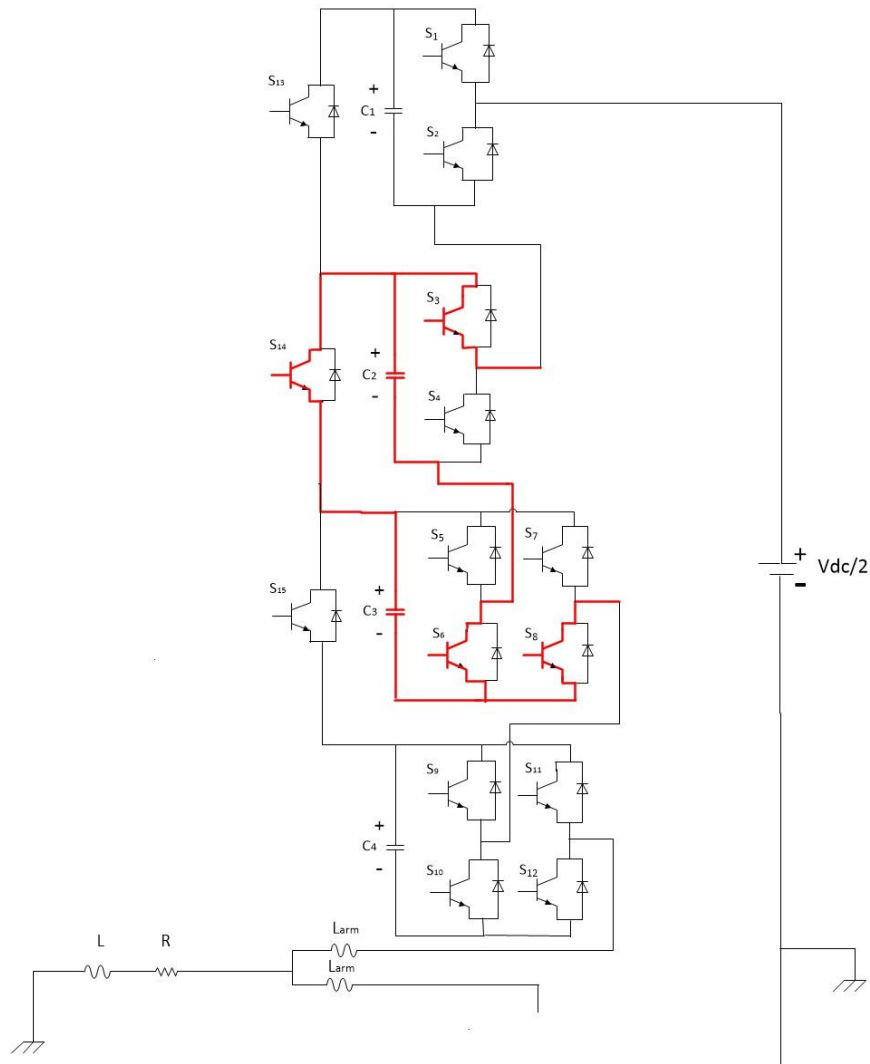
Fig. 3.54 one of the states

In the case that S_5 and S_8 are ON, there is no possibility to make S_{14} ON because the cell capacitor (C_2) will be short circuit. Similar states like this state could be considered as impractical switching states which prevent the paralleling of capacitors during the switching process. Fig. 3.55 shows one of the states which leads to the impractical state.
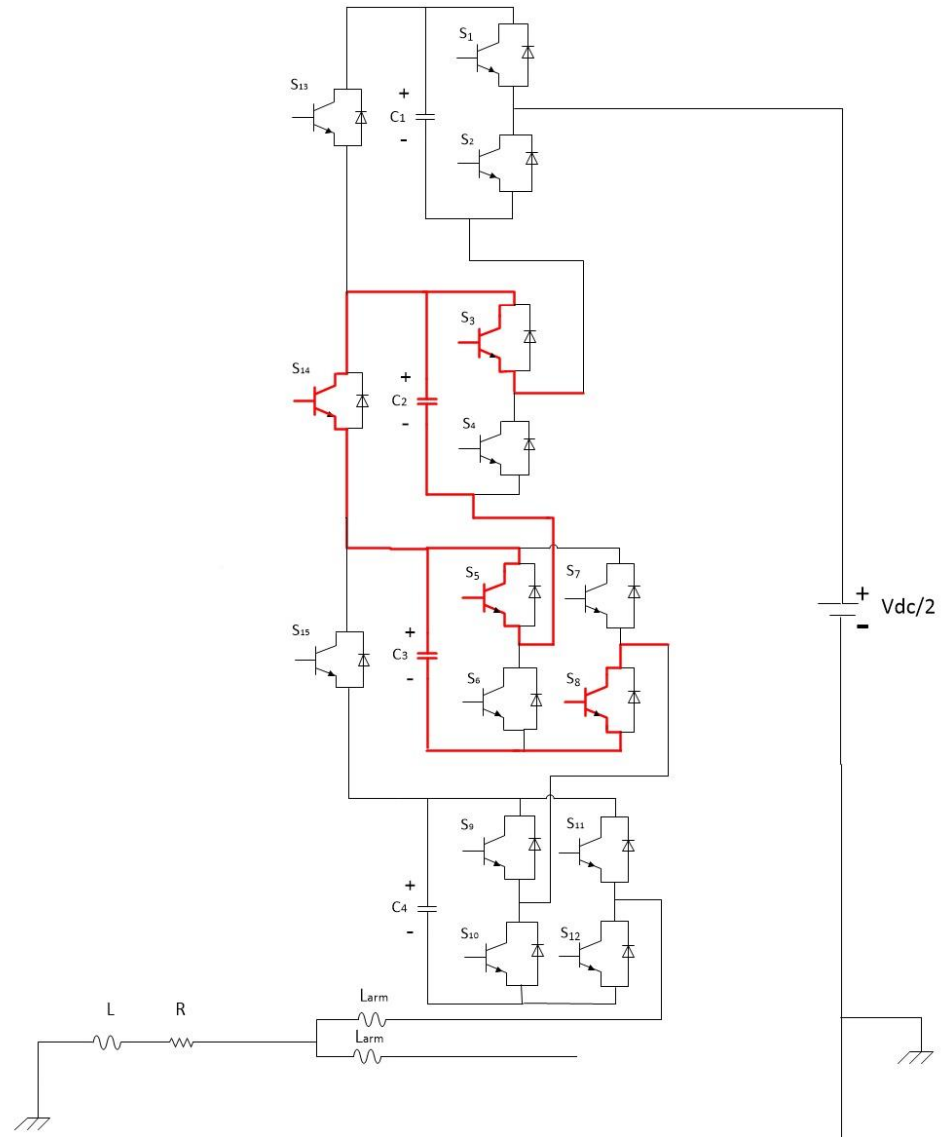
Fig. 3.55 One of the states (Impractical operation condition)

3.6 Chapter Summary

This chapter has presented a detailed review of the proposed multilevel topology, including its structure and operation principle. Furthermore, it presented the simulation of the new design at four different switching frequencies including loss and efficiency analysis. It can be concluded applying the new proposed design at 100 Hz switching frequency gives the highest efficiency. Finally, the proposed design has been tested on hybrid MMC topology which is not practical design because of flowing reverse currents through the diode of additional switches.

Chapter 4: Operation of the New Proposed Design at HVDC System Level and the Converter Reliability Improvement

As mentioned in Chapter 3, the sub module voltage ripple should be less than 10% for a stable operation of the MMC. If these voltages are left without control, the difference between them will lead to increasing the converter differential current, which means that the converter losses will be higher specially at lower switching frequency operation conditions. In addition, the differential current affects the quality of the output current because of the superimposed harmonics. Simulation results in Chapter 3 demonstrate that the new proposed topology eliminates the circulating current at lower switching frequencies and improves the converter efficiency. Section 4.1 presents operation of the new proposed design at HVDC system level considering the nominal values of East-West Inter-Connector and point to point HVDC connection. Moreover, the dynamic performance of the new design has been investigated using the closed loop control in section 4.4. Operation at four different switching frequencies as well as loss and efficiency analysis are discussed in section 4.3.

The sub module capacitor plays an essential role in the operation of the MMC; however, it may suffer from a lot of problems that can severely affect their operation. Sub module open-circuit fault is one of them. In section 4.5, the operation of proposed design at sub module capacitor failure condition is discussed which improves the converter reliability without any need to shut off the converter[149].

In real applications of the MMC, the number of sub modules per arm can reach to hundreds, requiring many voltage sensors with their associated acquisition and processing circuitry. This compromises reliability of the MMC, besides complicating its implementation and control. The proposed topology can address this issue by eliminating the number of voltage sensors needed to measure the sub module capacitor voltages in

the MMC, hence reducing the direct and indirect costs. Reliability improvement is the other advantage of reducing the number of voltage sensors which is explained in this Chapter.

4.1 Operation of the New Design at the HVDC System Level Considering the Nominal Values of East-West Inter-Connector (400 kV, 500MW)

The new design with 8 sub modules across both arms for the single phase MMC has been simulated in Matlab/Simulink. The carrier phase-shifted sinusoidal pulse width modulation (CPS-PWM) technology generates pulses for a PWM-controlled modular multilevel converter. Operations at four different switching frequencies at unity power factor condition are simulated. The simulation results are benchmarked against an existing operational HVDC system between Ireland and UK (East-West Interconnector) that can carry 500 MW power at 400 kV [150].

Table. 4.1 Simulation parameters in unity power factor condition

Parameter	Value	Parameter	Value
Number of SMs in each arm	8	Carrier frequency	1000 Hz
			400 Hz
			100 Hz
			50 Hz
Number of Half-Bridge in each arm	8	DC bus voltage	400 kV
SM capacitor voltage	100 kV	SM capacitance	5500 μF
Arm inductor	4 mH	Output power	$\frac{500}{3}$ MW

The simulation parameters are indicated in Table. 4.1.

4.1.1 Simulation Results of the Proposed Topology Considering the

Nominal Values of East-West Inter-Connector (400 kV, 500MW)

This section shows the simulation results of the proposed topology at four different switching frequencies (1000 Hz, 400 Hz, 100Hz, 50Hz). It should be noted that for the first 10 sec of the simulation a classic half bridge DC side cascaded topology operation is simulated and at t=10 Sec the simulation of the proposed new topology commences.

4.1.1.1 Simulation results at 1000 Hz switching frequency

Fig. 4.1 shows the sub module voltage after and before applying the new design. The new design doesn't have any significant impact on the amount of peak to peak sub module voltage ripple and can only set the average ripple voltage to 100 kV. The amount of the circulating current has been shown in Fig. 4.2. The new proposed topology only changes the offset value of circulating current and doesn't have any significant impact on the content of circulating current.
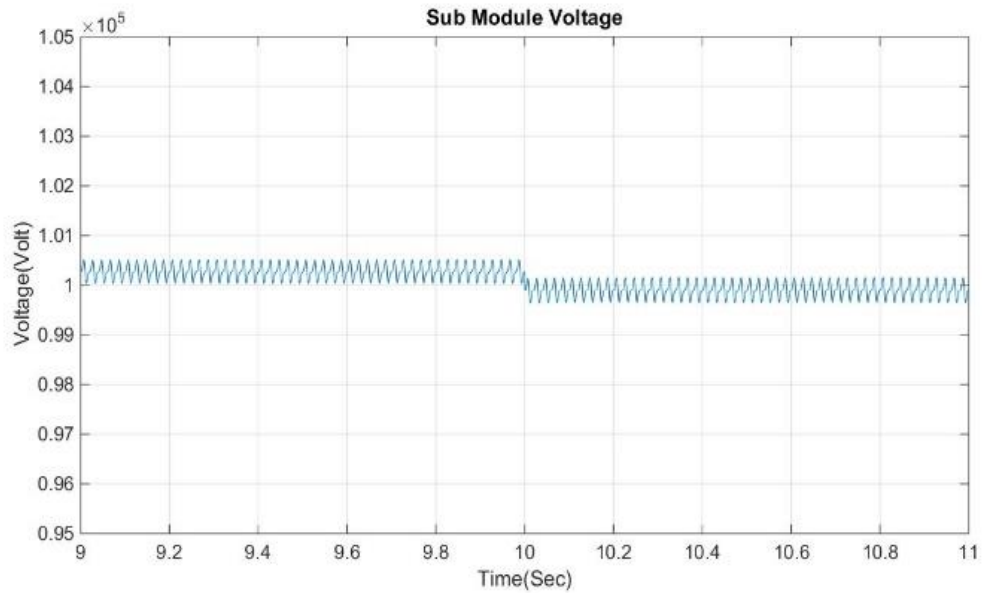
Fig. 4.1 Sub module voltage before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency
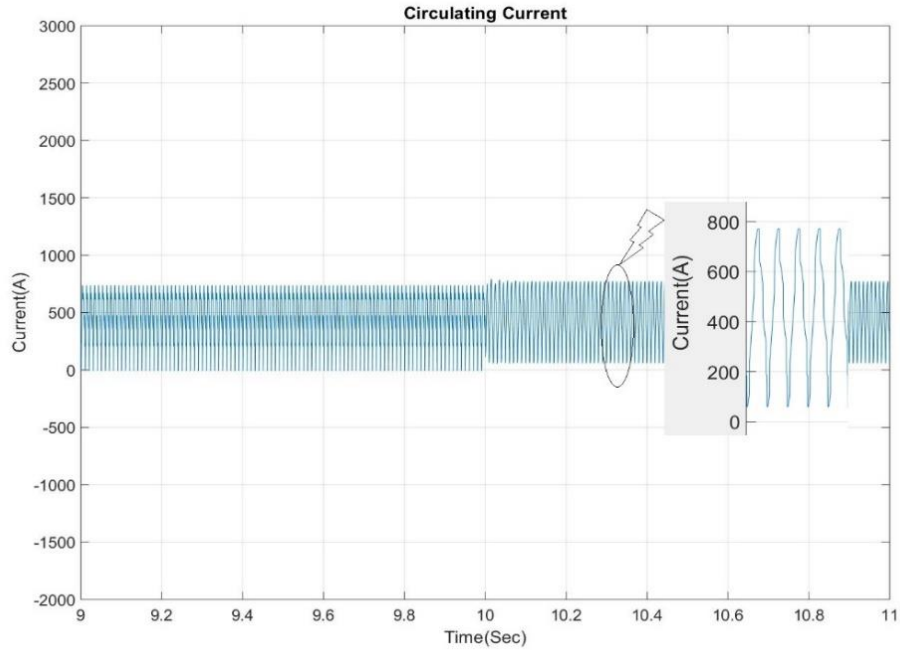
Fig. 4.2 Circulating current before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency

Fig. 4.3 and Fig. 4.4 show the upper arm and lower arm currents. Applying the new design can reduce the upper arm and lower arm currents 1%.
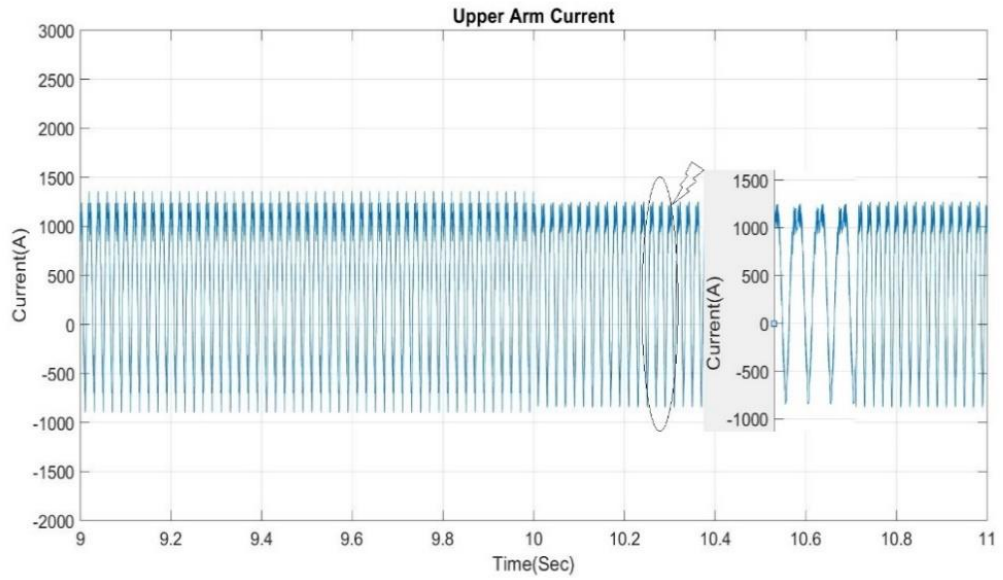
Fig. 4.3 Upper arm current before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency
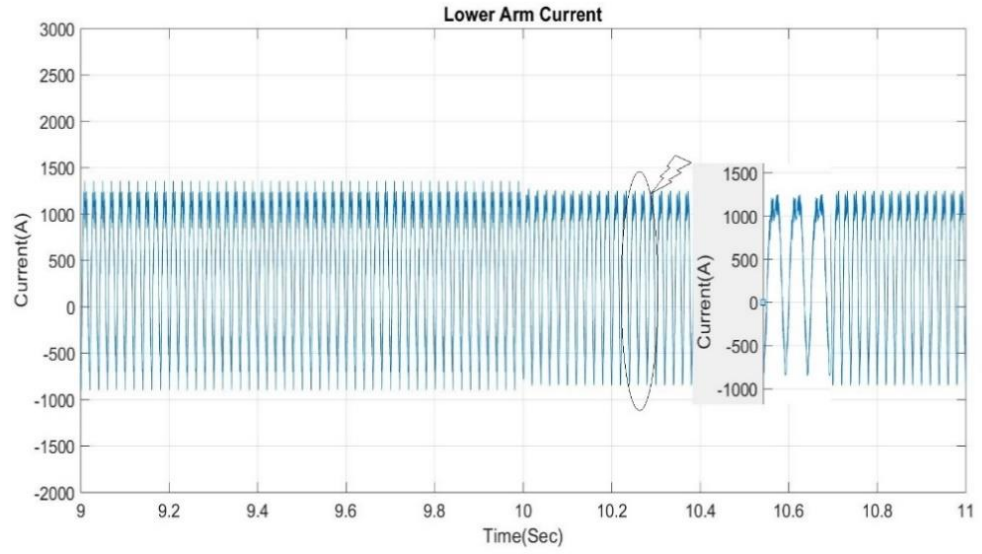
Fig. 4.4 Lower arm current before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency

Output current and output voltage are depicted in Fig. 4.5 and Fig. 4.6. When the new design comes to the circuit at t=10 Sec, output current and output voltage don't change.

Fig. 4.5 Output current before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency
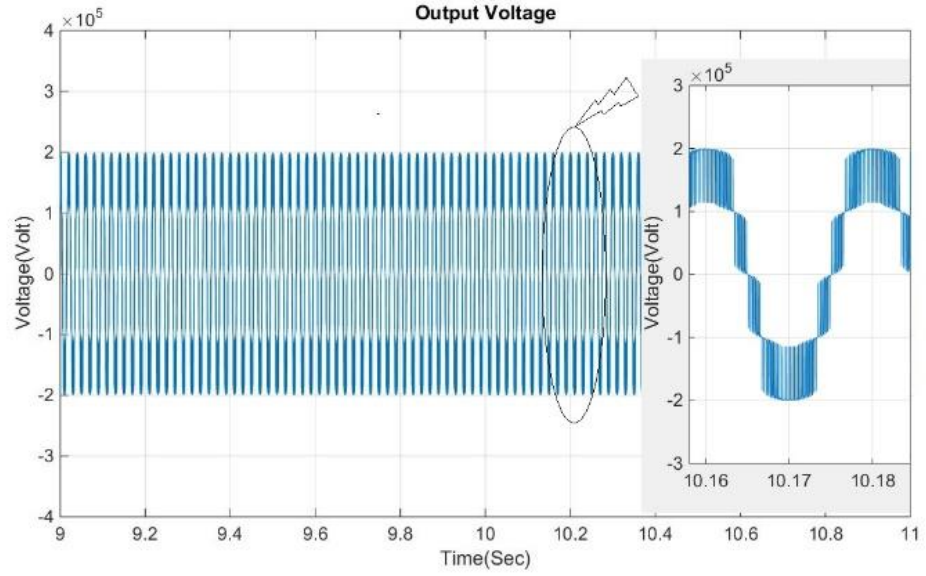
Fig. 4.6 Output voltage before and after applying the proposed design at t=10 Sec and 1000 Hz

switching frequency

4.1.1.2 Simulation results at 400 Hz switching frequency

Fig. 4.7 depicts the variation of sub module voltage before and after applying the new design at t=10 Sec. Sub module voltage fluctuations will be less after applying the new design. Moreover, the new design helps the control to set the sub module voltage to 100 kV.
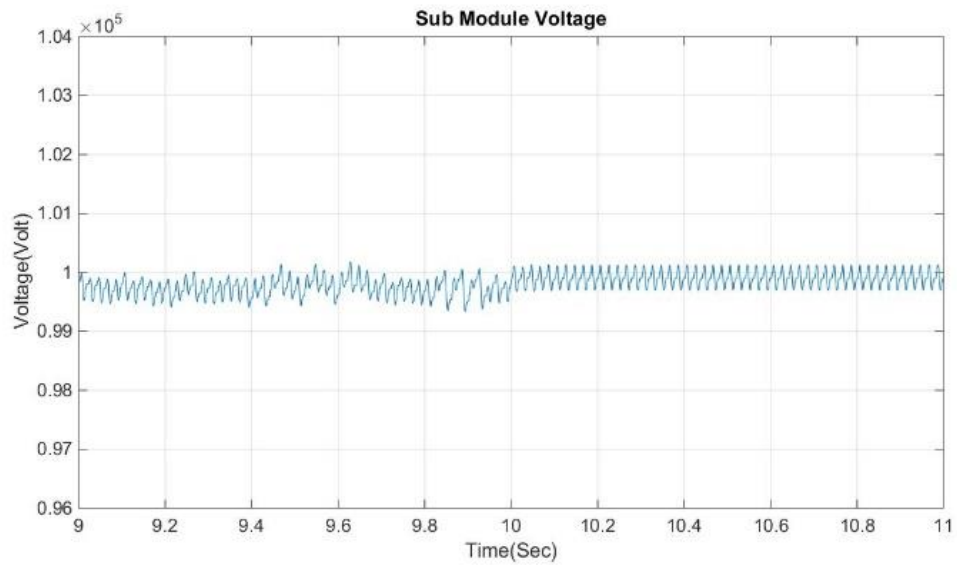
Fig. 4.7 Sub module voltage before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency

Variation of the circulating current, upper arm current and lower arm current are shown at Fig. 4.8, Fig. 4.9 and Fig. 4.10. Circulating current has lots of fluctuations at 400 Hz switching frequency and when the new design comes to the circuit, it can decrease all fluctuations and the content of circulating current by 30%.
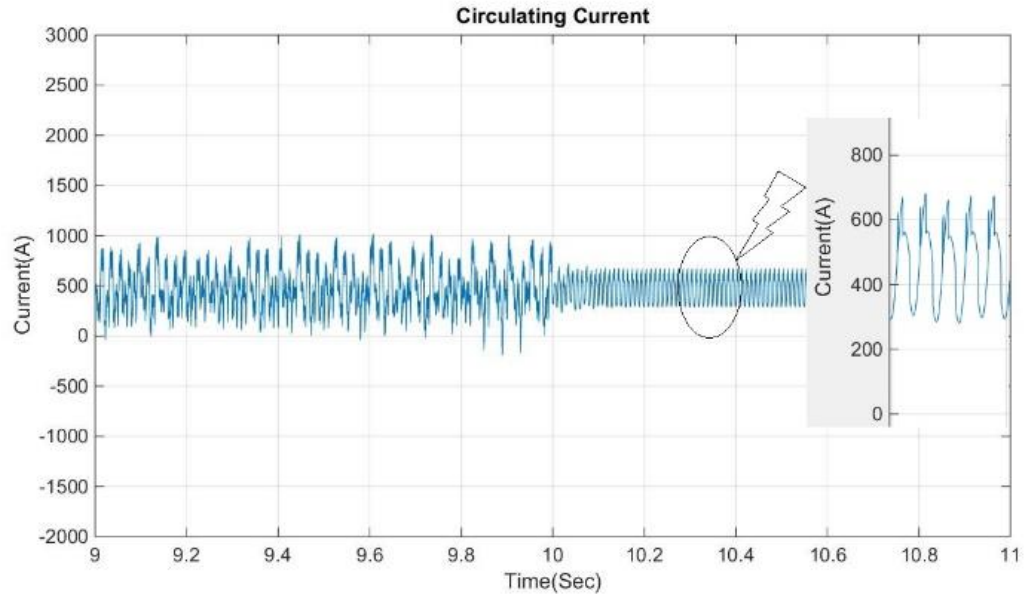
Fig. 4.8 Circulating current before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency
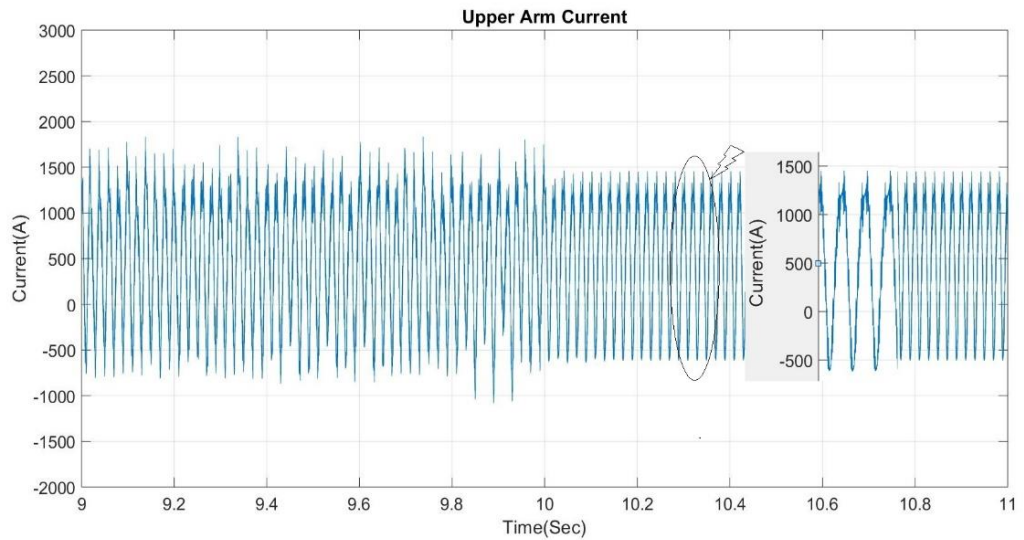
Fig. 4.9 Upper arm current before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency

Fig. 4.10 Lower arm current before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency

Upper arm and lower arm currents are also fluctuating at 400 Hz switching frequency and after t=10 Sec, the new proposed design eliminates fluctuations. Variation of the output current and the output voltage are shown in Fig. 4.11 and Fig. 4.12. The new proposed design doesn't have any significant impact on the output current and voltage at 400 Hz switching frequency.
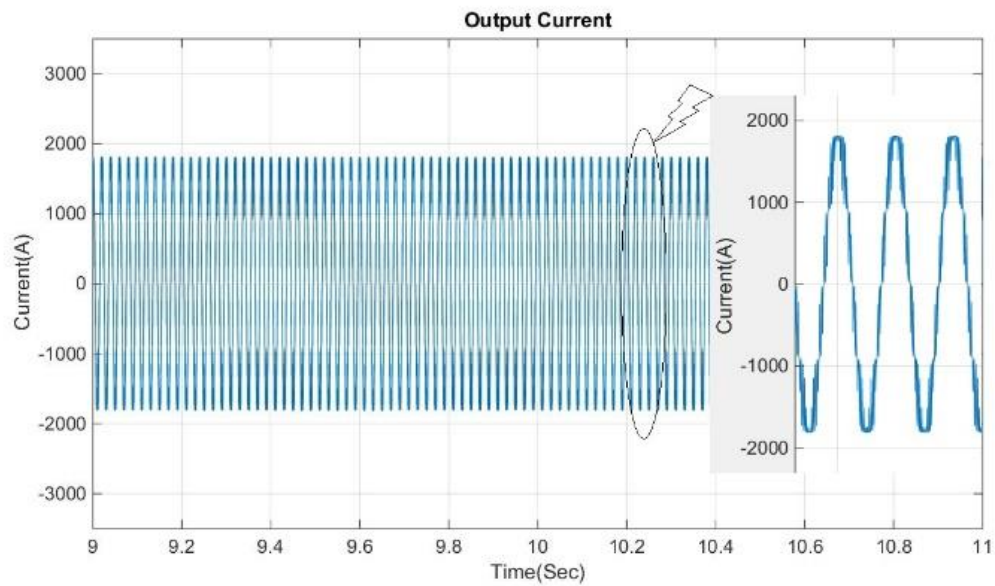
Fig. 4.11 Output current before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency
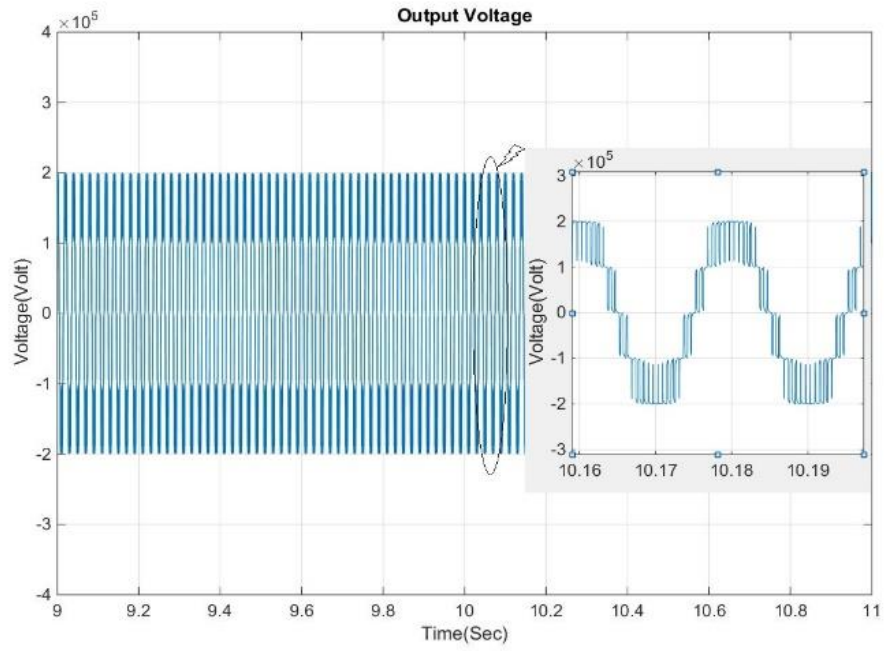
Fig. 4.12 Output voltage before and after applying the proposed design at t=10 Sec and 400 Hz

switching frequency

4.1.1.3 Simulation results at 100 Hz switching frequency

With decreasing the switching frequency to 100 Hz and applying the new design, the sub module voltage ripple will be suppressed.
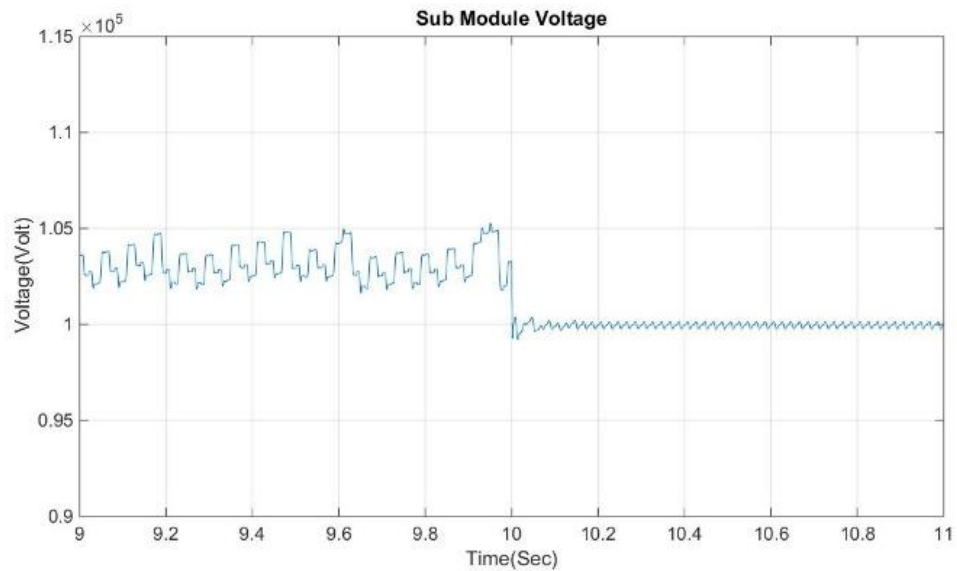
Fig. 4.13 Sub module voltage before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency

Fig. 4.13 shows the sub module voltage variation before and after applying the new design at t=10 Sec and 100 Hz switching frequency. The new proposed design can regulate the sub module voltage to 100 kV and eliminate sub module voltage fluctuations.

Circulating current and arm currents are shown in Fig. 4.14, Fig. 4.15 and Fig. 4.16. Circulating current has significant fluctuations at 100 Hz switching frequency and applying the new design eliminates all fluctuations and stabilizes the circulating current.
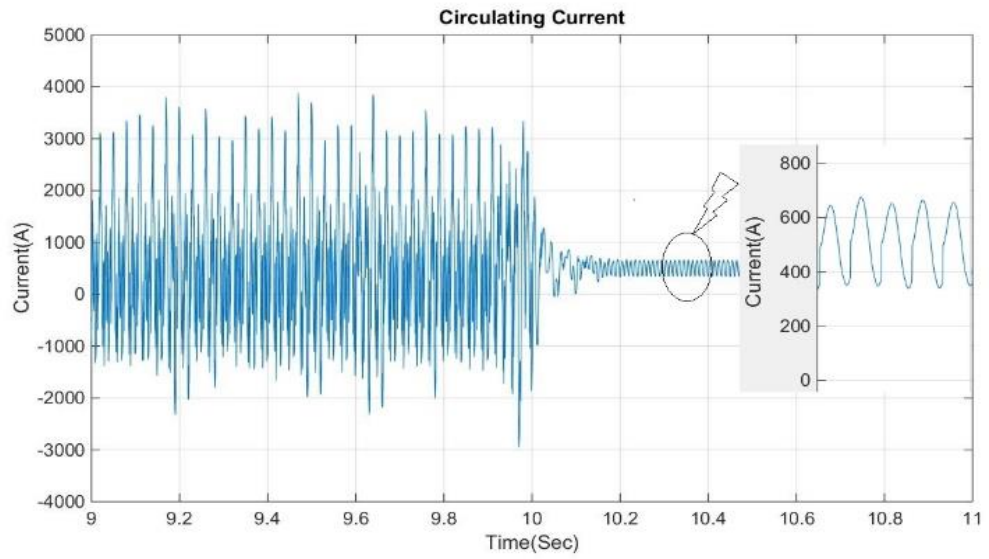
Fig. 4.14 Circulating current before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency
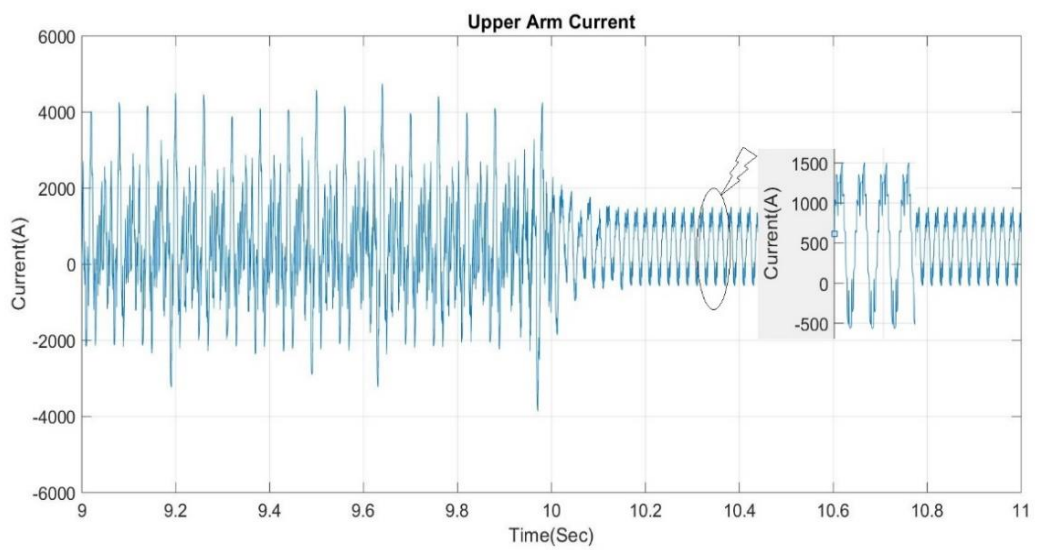
Fig. 4.15 Upper arm current before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency

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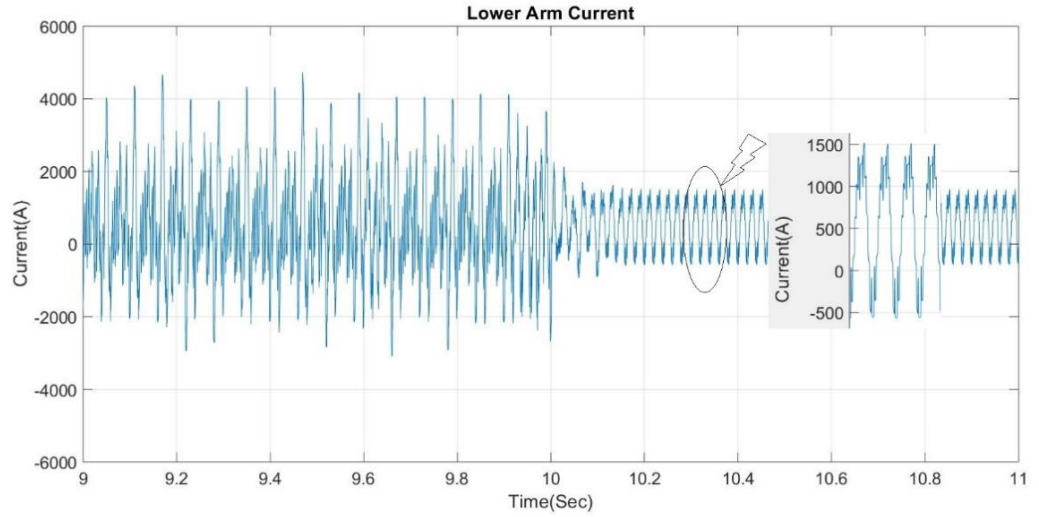
Fig. 4.16 Lower arm current before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency

Amount of fluctuations for the upper arm and lower arm currents are very high before applying the new design. However, after t=10 Sec when the new design comes to the circuit, the lower arm and upper currents will be more stable with less fluctuations.

The output current and output voltage are shown in Fig. 4.17 and Fig. 4.18. The new design can stabilize the output current and voltage.
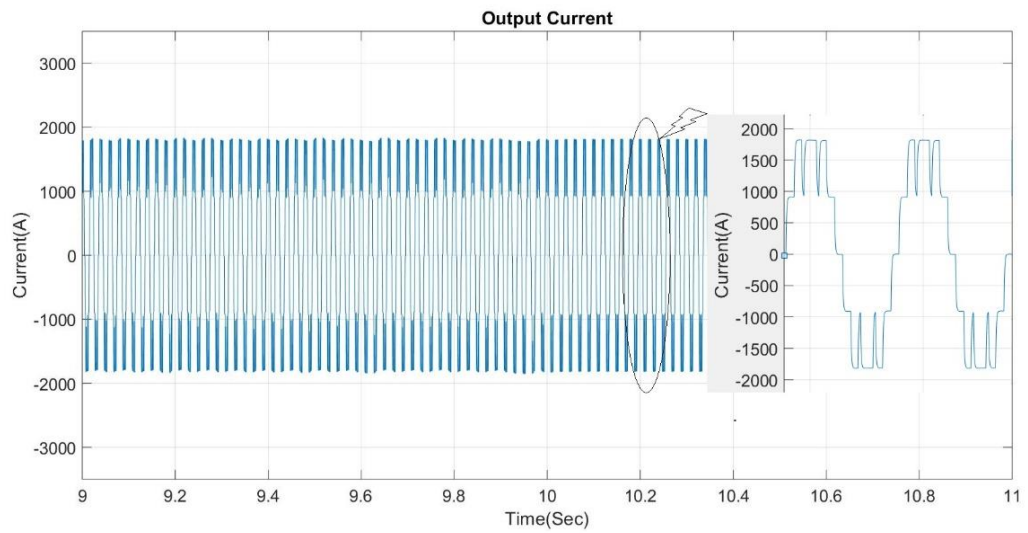
Fig. 4.17 Output current before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency
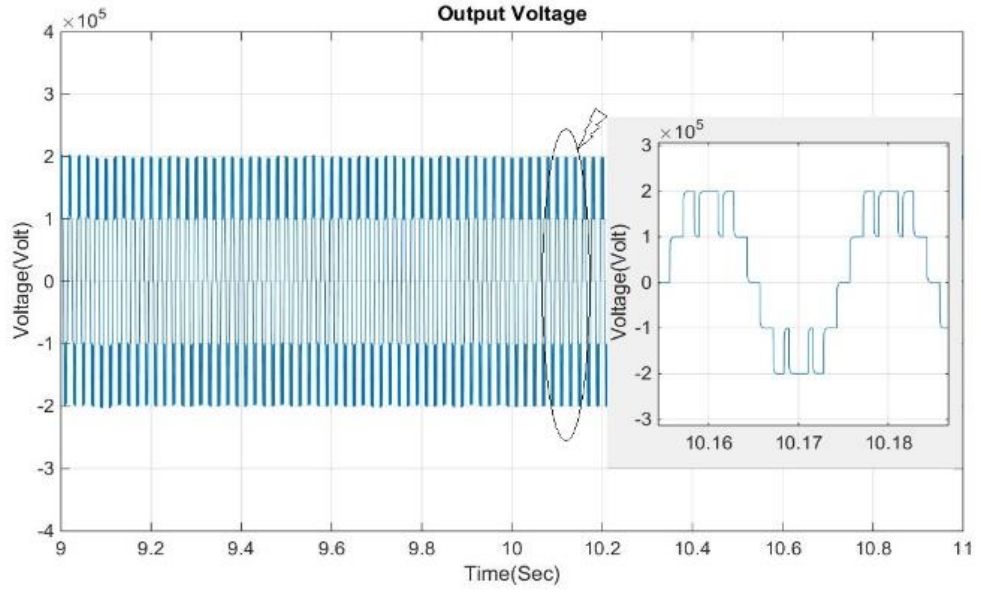
Fig. 4.18 Output voltage before and after applying the proposed design at t=10 Sec and 100 Hz

switching frequency

4.1.1.4 Simulation results at 50 Hz switching frequency

Decreasing the switching frequency to 50 Hz, will impose more ripples on the sub module voltage and will increase the circulating current content. After t=10 Sec, the new design comes to the circuit and the sub module voltage ripple and the circulating current will be eliminated.
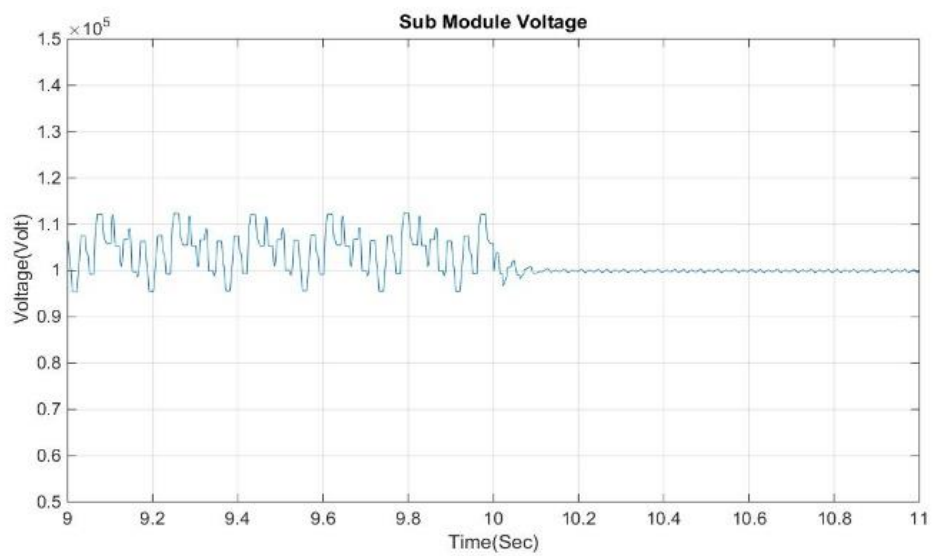
Fig. 4.19 Sub module voltage before and after applying the proposed design at t=10 Sec and 50 Hz

switching frequency
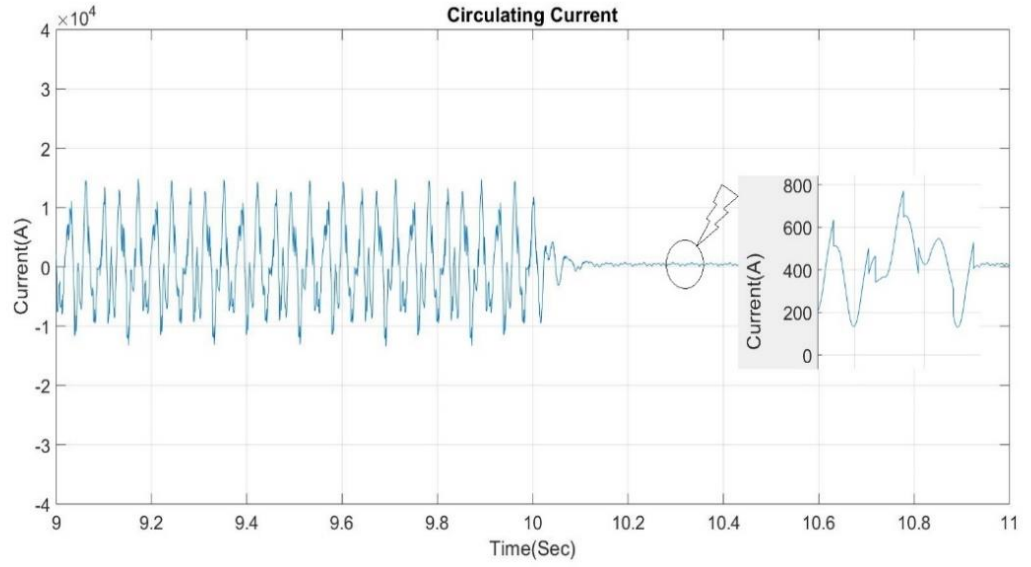
Fig. 4.20 Circulating current before and after applying the proposed design at t=10 Sec and 50 Hz

switching frequency

Fig. 4.19 and Fig. 4.20 show the variation of the sub module voltage and the circulating current at 50 Hz switching frequency. The proposed topology also sets the sub module voltage to 100 kV and keeps the variation of circulating current in the acceptable range which is less than 10%.

Arm currents are shown in Fig. 4.21 and Fig. 4.22 which are more stable with less fluctuations after applying the new design.
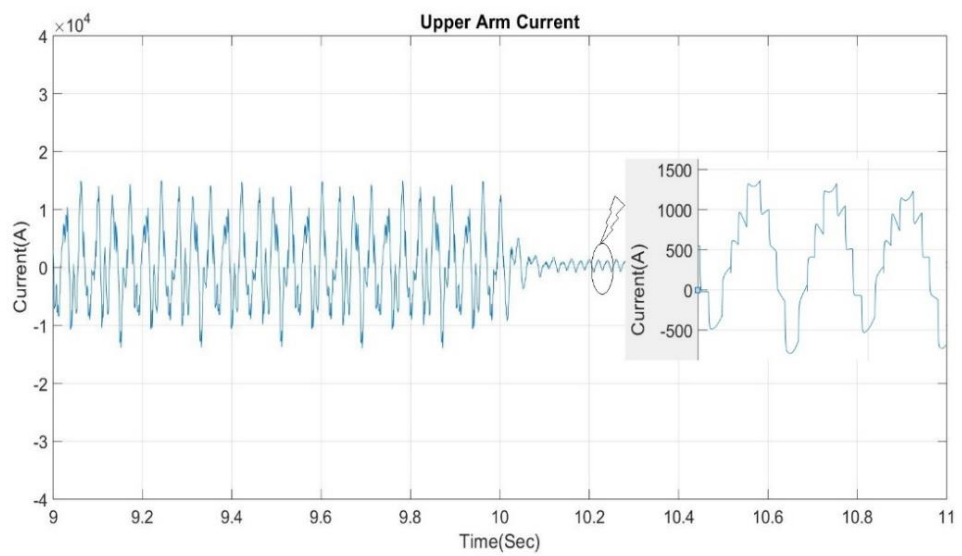
Fig. 4.21 Upper arm current before and after applying the proposed design at t=10 Sec and 50 Hz

switching frequency

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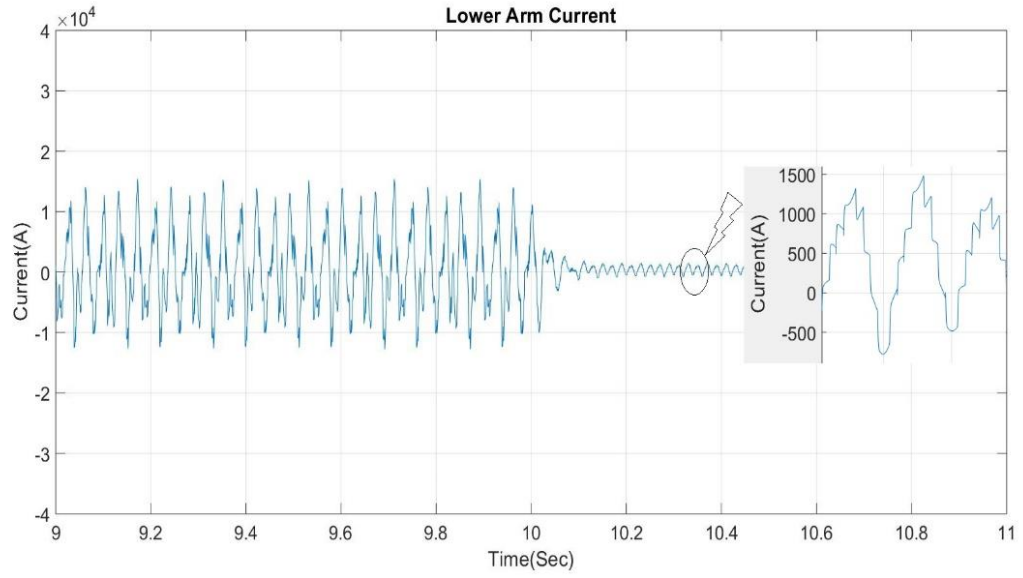
Fig. 4.22 Lower arm current before and after applying the proposed design at t=10 Sec and 50 Hz

switching frequency

Fig. 4.23 and Fig. 4.24 depict the output current and voltage at 50 Hz switching frequency which are more stable after t=10 Sec.
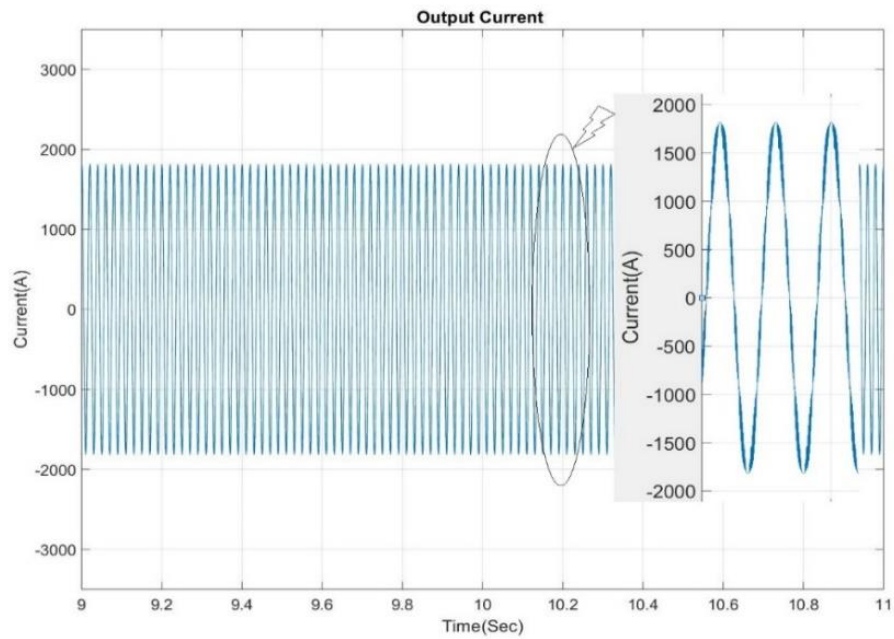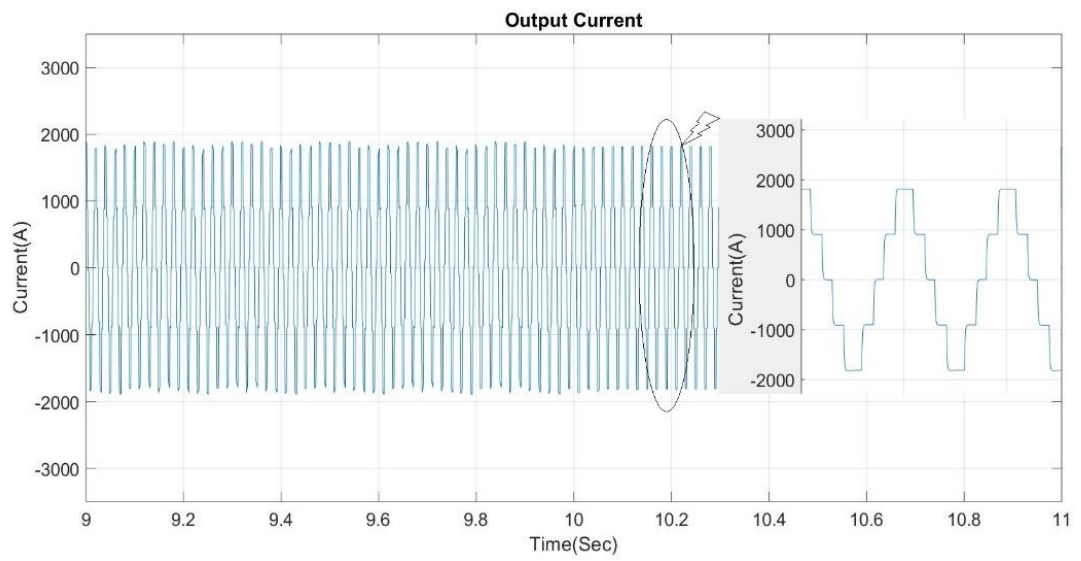

Fig. 4.23 Output current before and after applying the proposed design at t=10 Sec and 50 Hz switching
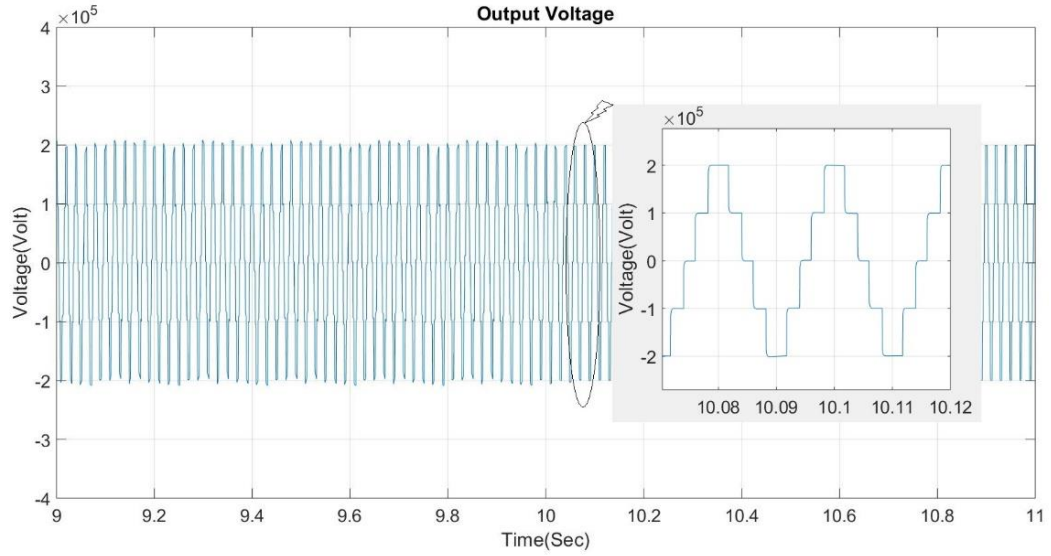
frequency

Fig. 4.24 Output voltage before and after applying the proposed design at t=10 Sec and 50 Hz switching
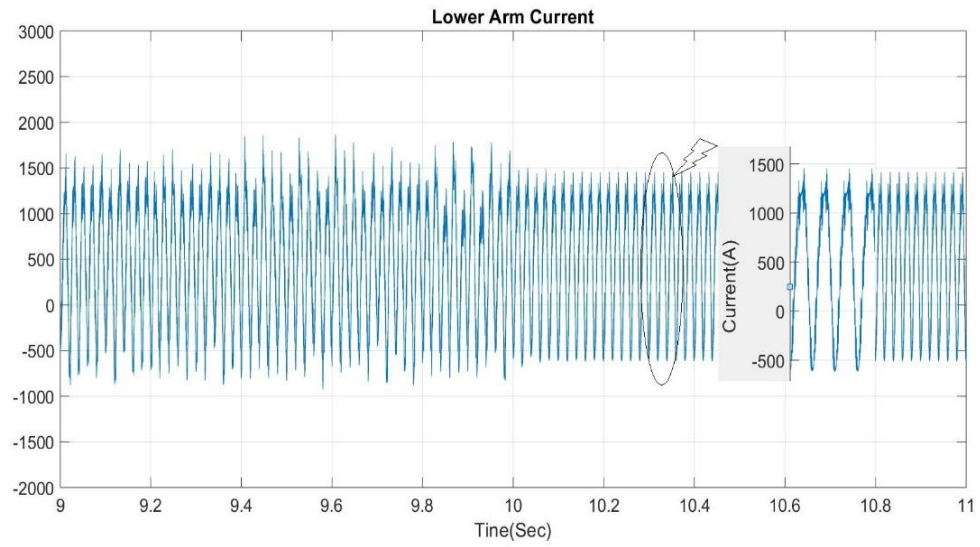
frequency

4.2 THD and Harmonic Analysis of the Output Current and Voltage at Four Different Switching Frequencies Considering the New Design

As discussed in Chapter 3, before applying the new design and considering the classic half-bridge topology the amount of THD and harmonic contents are high for the circulating current. However, when the new design comes to the circuit THD will be improved significantly and all sub harmonics will be cancelled. Working at lower switching frequencies will increase the amount of the voltage and current THD. In the other side, increasing the number of levels will eliminate the harmonic content of voltage and current to the acceptable level without any need to filter. In this thesis, because of using 8 sub modules across both arms, the amount of current and voltage THD are exceeding the standard values when the switching frequency goes lower. However, increasing the number of voltage levels will solve this issue without the need to any filter.

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Table. 4.2, shows the output voltage and current THD at 4 different switching frequencies for 5-level output voltage which can be improved by increasing the number of levels to 9-level output voltage.

Table. 4.2 Output voltage and current THD at four different switching frequencies for 5-level and 9-level output

Switching Frequency (Hz)	Output Current THD for 5-level	Output Current THD for 9-level	Output Voltage THD for 5-level	Output Voltage THD for 9-level
1000	7.74%	2.19%	24.37%	12.38%
400	15.46%	4.91%	25.17%	12.48%
100	24.35%	11.56%	27.03%	13.82%
50	20.34%	10.77%	22.18%	13.14%

4.3 Loss and Efficiency Analysis of the Classic Half Bridge MMC Versus the Proposed New Topology at the HVDC System Level

Details about the loss and efficiency calculations, switch selection, heat sink design and damping resistors selection are investigated in Chapter 3. Considering 8 sub modules across both arms and 400 kV as a DC link voltage, each sub module voltage will be 100 kV. The output voltage level depends on the phase shift value between carriers of the sub modules of each arm. As the harmonics of the circulating current have significant contribution in converter loss and efficiency, considering zero phase shift between carriers of each arm will eliminate the circulating current harmonics and will lead to 5-level voltage in the output. The characteristics of the converter switches are obtained from the datasheets of the 1.7 kV, 800 A, ABB switch. A safety coefficient of 1.15 has been applied to the device voltage ratings to ensure they can withstand the high DC link voltage for each converter. The number of parallel branches depends on the rated current of the system and the rated current of each switch. For example, for 100 kV, 68 ABB

1.7 kV switches should be series ($68*1.7 \cong 115$). The number of parallel branches depends on the rated current of the system and the rated current of each switch.

Fig. 4.25 shows the variation of the switching losses at four different switching frequencies (1000 Hz, 400 Hz, 100 Hz, 50 Hz) for the classic half-bridge MMC topology and the proposed topology.
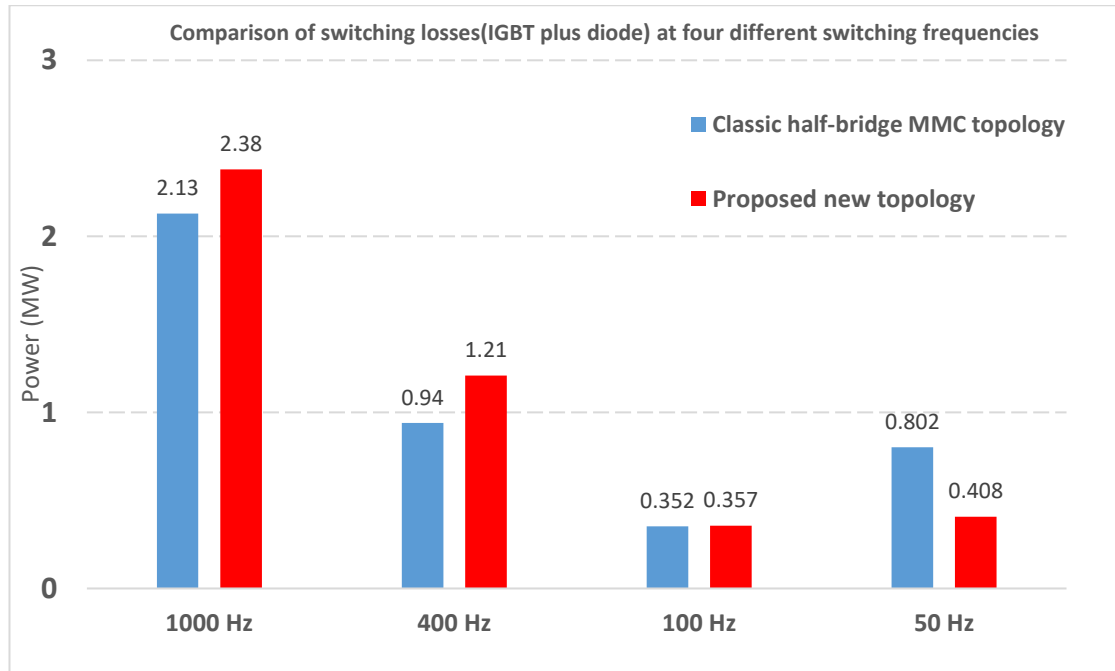
Fig. 4.25 Comparison of switching losses (IGBT plus diode) at four different switching frequencies considering classic half-bridge MMC topology and proposed new topology with East-West Inter-Connector values

Because of existing additional switches in the proposed topology, the amount of switching losses are higher than the classic half-bridge design at higher switching frequencies. At 50 Hz switching frequency, the amount of switching losses is lower than the classic topology. The reason is the instability of the classic design at very low switching frequency. Fig. 4.26 depicts the comparison of conduction losses at four different switching frequencies for the classic half topology and the proposed design considering East-West Inter-Connector values. Decreasing the switching frequency will increase the conduction losses. The proposed design can eliminate the conduction losses

to the range of higher switching frequency values (the amount of conduction losses at 100 Hz switching frequency is approximately identical with 1000 Hz switching frequency).
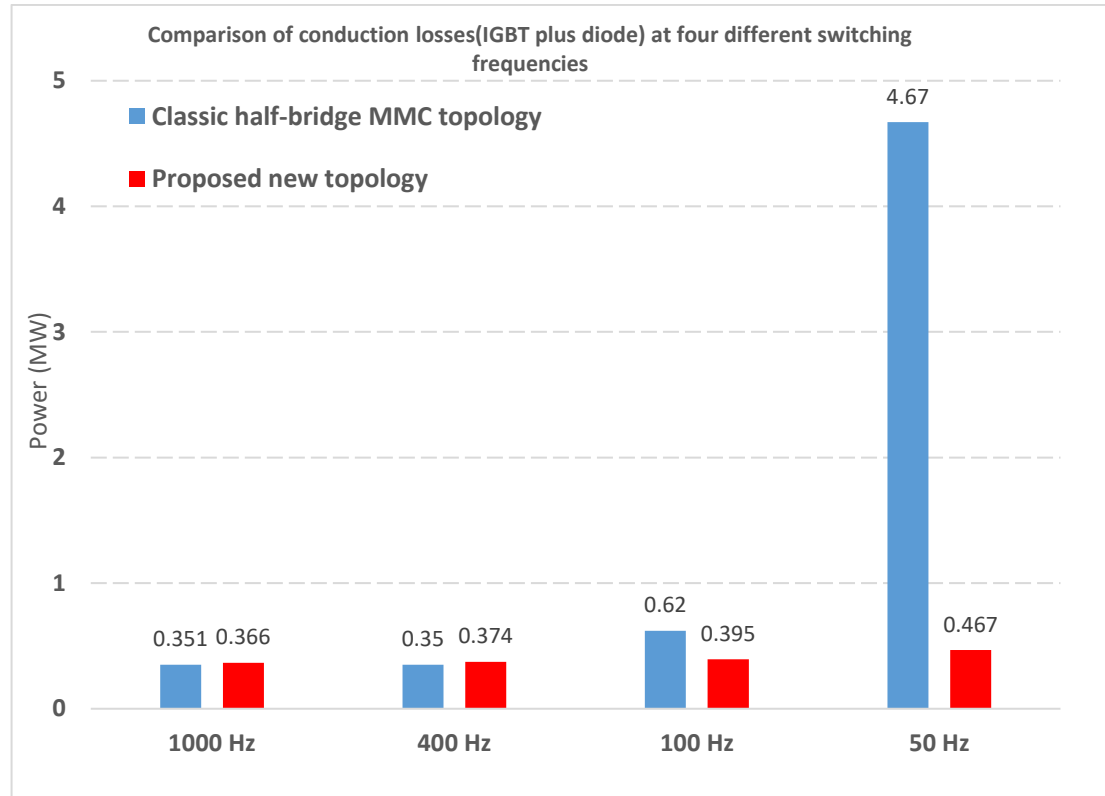
Fig. 4.26 Comparison of conduction losses (IGBT plus diode) at four different switching frequencies considering classic half-bridge MMC topology and proposed new topology with East-West Inter-Connector values

As explained in Chapter 3, the proposed topology has some additional switches and damping resistors (small value resistors) which are added in series with additional switches. Damping resistors are included in the circuit to limit the inrush currents during the switching period.
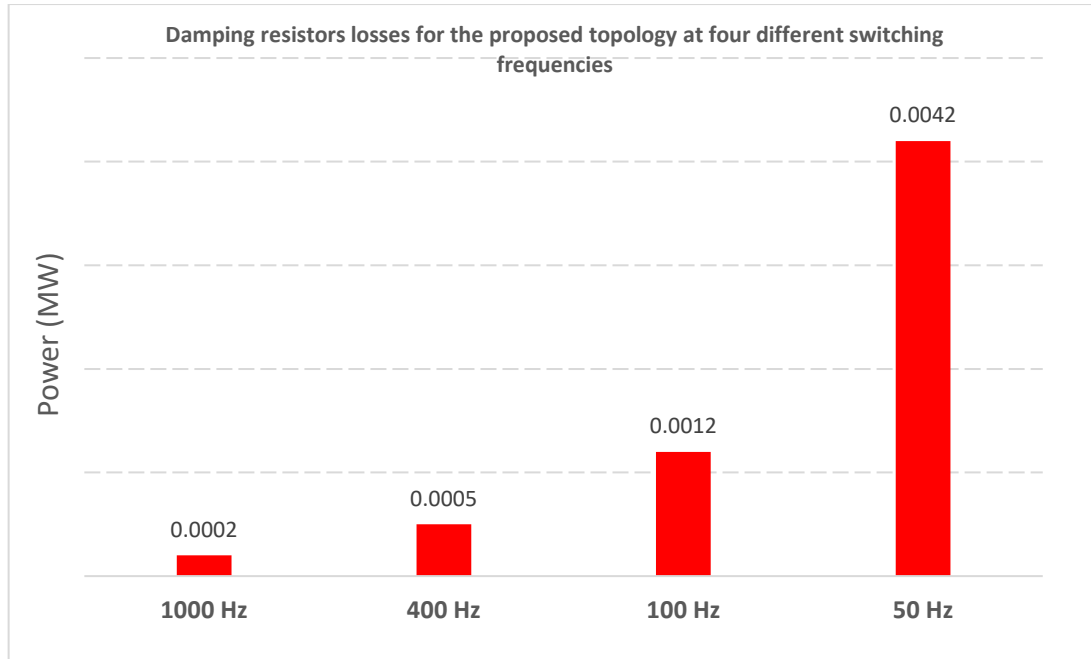
Fig. 4.27 Comparison of damping resistor losses at four different switching frequencies considering

proposed new topology and East-West Inter-Connector values

For the higher switching frequencies, the amount of damping resistor losses is less

than lower switching frequencies.
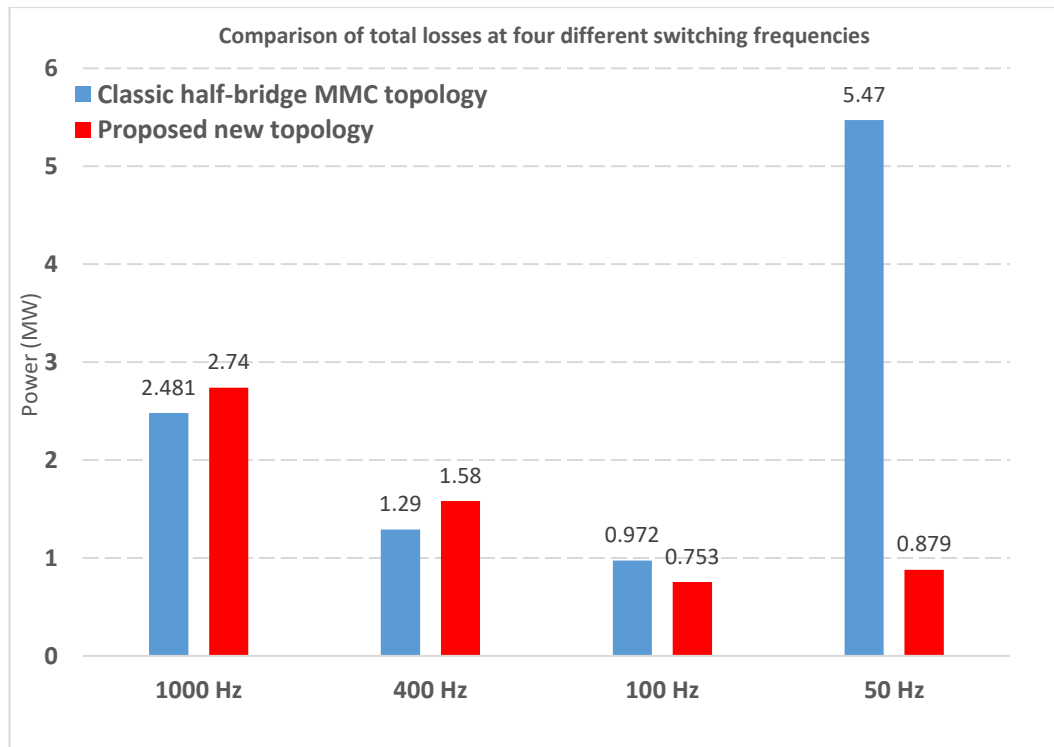
Fig. 4.28 Comparison of total losses (per phase) at four different switching frequencies considering

classic half-bridge MMC topology and proposed new topology with East-West Inter-Connector values

The total loss comparison is shown in Fig. 4.28. Switching losses are higher at higher switching frequencies. However, decreasing the switching frequency will increase the conduction losses and damping resistor losses. Fig. 4.28 shows the comparison of total converter losses for each phase at four different switching frequencies considering East-West Inter-Connector values.

The total loss comparison shows that the 100 Hz switching frequency considering the new proposed design can be considered as an optimal switching frequency since it has lower switching losses as well as lower conduction losses plus damping resistor losses.

Table. 4.3 shows the converter efficiency comparison between the classic half-bridge MMC and the proposed topology at four different switching frequencies. Operation of the proposed design at 100 Hz switching frequency gives the highest efficiency.

Table. 4.3 The converter efficiency at four different switching frequencies

Switching Frequency	1000 Hz	400 Hz	100 Hz	50 Hz
Efficiency of the classic half-bridge MMC topology	98.53%	99.23%	99.42%	96.82%
Efficiency of the proposed topology	98.38%	99.06 %	99.55%	99.47%

4.4 Closed Loop Control of the Proposed Design Considering the Nominal Values of East-West Inter-Connector (400 kV, 500MW) and Point to Point HVDC Connection

The fundamentals of MMC based HVDC system operation can be explained by considering each terminal as a voltage source connected to the AC transmission network via a three-phase reactor. In paper [151] a back-to-back MMC for medium voltage applications under faulted condition has been investigated. The two terminals are

interconnected by a DC link, as schematically shown in Fig. 4.29. X_L is the total reactance of the converter transformer and the phase reactor (if equipped) and V_{AC} and V_{Out} are rms voltages at the point of common coupling (PCC) and at the converter terminals respectively. The phase displacement angle of the converter output voltage with respect to the AC system voltage is δ and the voltage difference between the PCC and the VSC is ΔV. U_{dc} and I_{dc} are the DC link voltage and current. The active power and reactive power exchanged between the MMC and the AC system are P_c and Q_c.
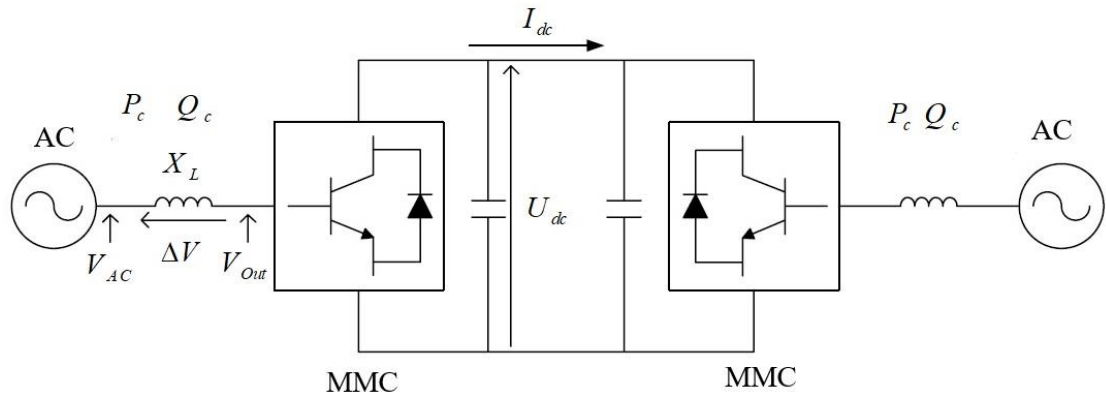
Fig. 4.29 MMC based HVDC transmission operation

The active power and reactive power can then be controlled by controlling the phase angle, δ and the modulation index, m respectively. The direction of active power flow decides the rectifier or inverter operation of converter and the capacitive and inductive modes of the converter are determined using the direction of reactive power absorption. Fig. 4.30 illustrates the ability of MMC to operate in all four quadrants of P-Q diagram. The active power is defined as positive if the converter injects power to the AC system and reactive power is positive if the converter injects reactive power to the AC system.
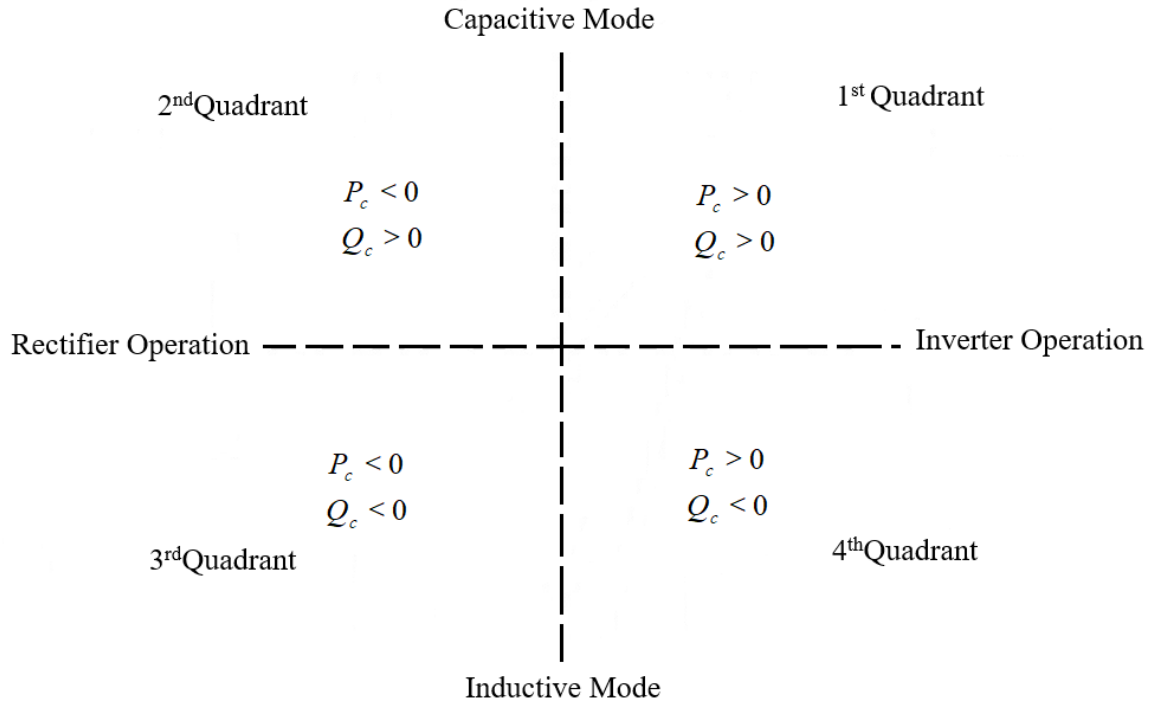
Fig. 4.30 Four-Quadrant Operation of MMC

Considering the new proposed topology as MMC converter and nominal values of East-West Inter-Connector (400 kV, 500MW) the point to point HVDC connection is created and dynamic of system regarding to active and reactive power change has been studied. Different control strategies of VSC-HVDC have been proposed [152]. It depends on the control target, in case of the rectifier station the control target is to regulate the DC link voltage of the DC transmission line during fast power variations and keep the input power factor near unity, while in case of the inverter station it controls active and reactive power. The system controller in each converter has two control loops, the outer loop generates the current references of the inner current control loop which uses the well-known vector control in synchronous rotating reference frame (SRF) as shown in Fig. 4.31. V_{gd} and V_{gq} are direct and quadrature values of the grid voltage. To achieve the Park transformation, a phase-locked loop (PLL) that detects the phase angle of grid

voltage is used. i_d and i_q are similarly the Park transformation for the grid current.
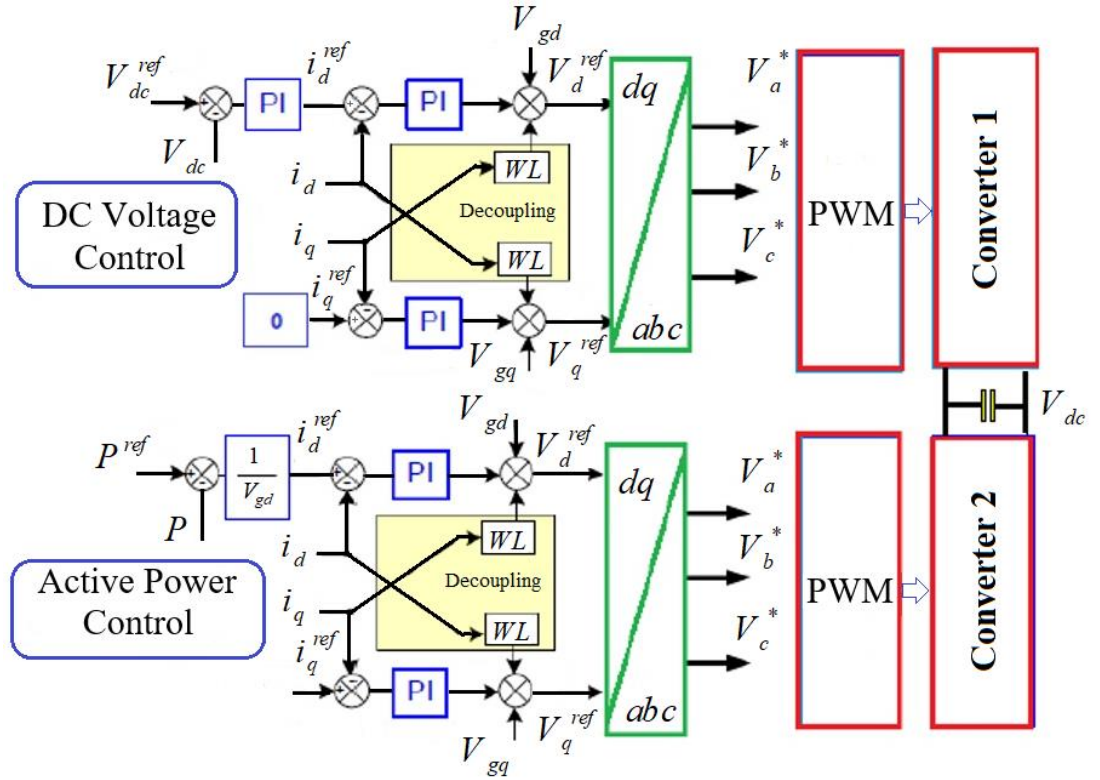
Fig. 4.31 Control schematic of MMC-HVDC

V_a^* is the reference voltage for the PWM generation. P is the instantaneous active

power and P^{ref} is the reference active power.

Table. 4.4 Simulation parameters considering East-West Inter-Connector nominal values

Parameter	Value	Parameter	Value
Number of SMs in each arm	12	Carrier frequency	550 Hz
Number of Half-Bridge in each arm	12	DC bus voltage	400 kV
SM capacitor voltage	66.66 kV	SM capacitance	9 mF
Arm inductor	3 mH	Output power	500 MW
Coupling inductor	10 mH	AC side peak voltage value	200 kV

In case of the rectifier operation, the DC voltage controller generates i_d^{ref} command and i_q^{ref} is set to zero to attain unity power factor. While in case of inverter operation, the active/reactive power controller generates the corresponding current commands. The simulation parameters for the proposed new design to create the point-to-point HVDC connection are according to Table. 4.4. In the simulation first quadrant has been considered as the working area.
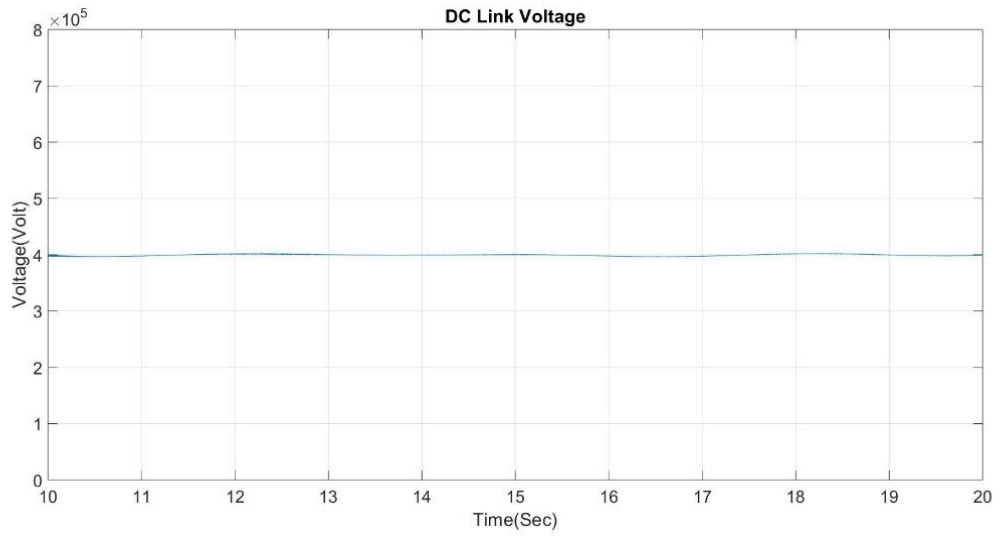
Fig. 4.32 DC link voltage

Fig. 4.32 shows the common DC link voltage between the rectifier and the inverter. Rectifier keeps the DC link voltage as a fixed value which is 400 kV and inverter responses the any dynamic variation on active power and reactive power. Fig. 4.33 depicts the dynamic change for active power which is changing from -500MW to +500MW with the slope of 500MW per second. The dynamic variation of reactive power is shown in Fig. 4.34 and is changing from -100MW to -200MW with the slope of -100MW per second. The difference between the actual value and the reference shows that the real signal follows the reference during any dynamic load change.
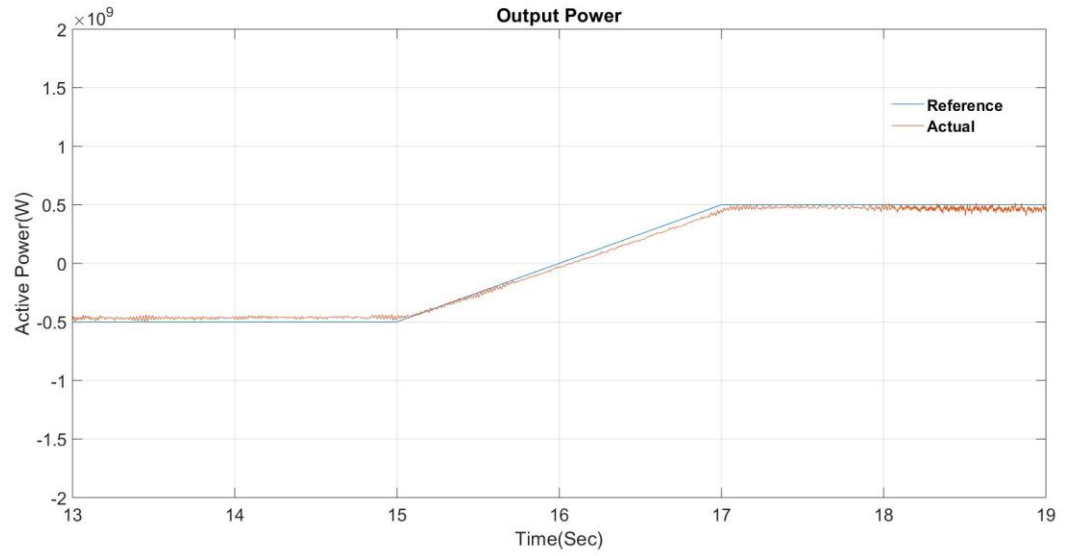
Fig. 4.33 Dynamic change for active power
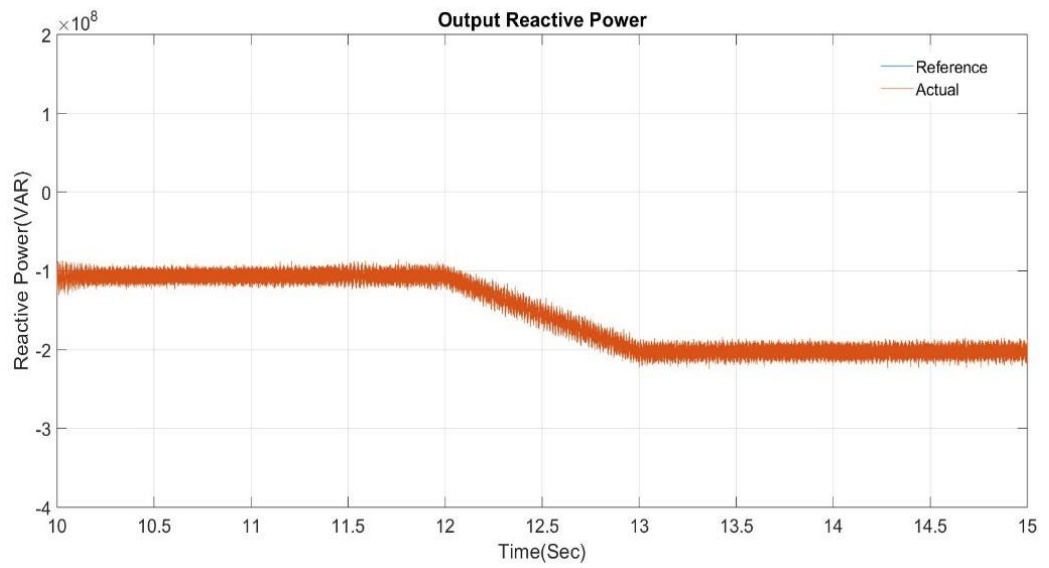
Fig. 4.34 Dynamic change for reactive power

Fig. 4.35 and Fig. 4.36 show the inverter output voltage and current. The output voltage has 13 voltage levels because of existing 12 sub modules in the arm and the output current is looking like to the sinusoidal waveform.
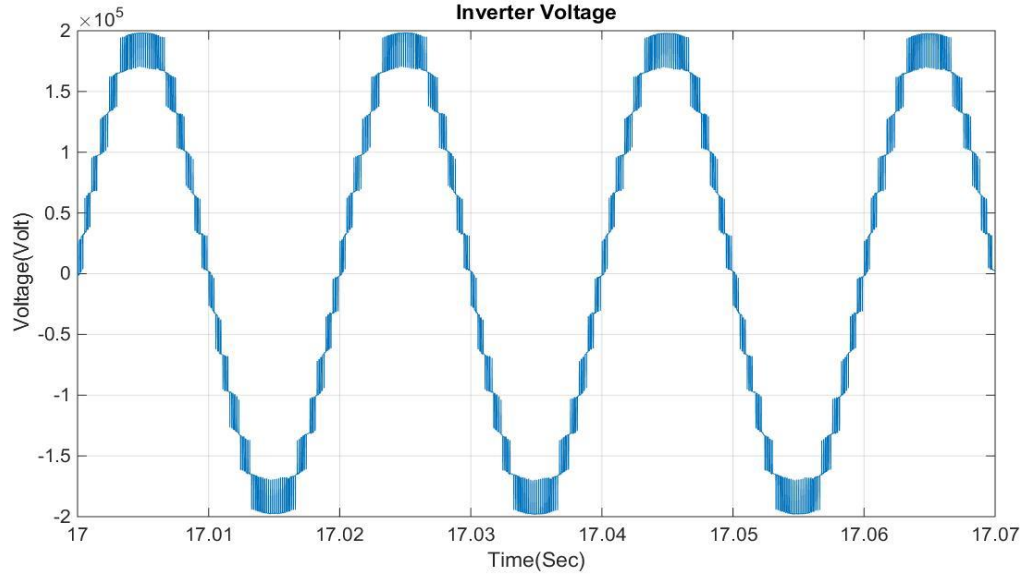
Fig. 4.35 The inverter output voltage
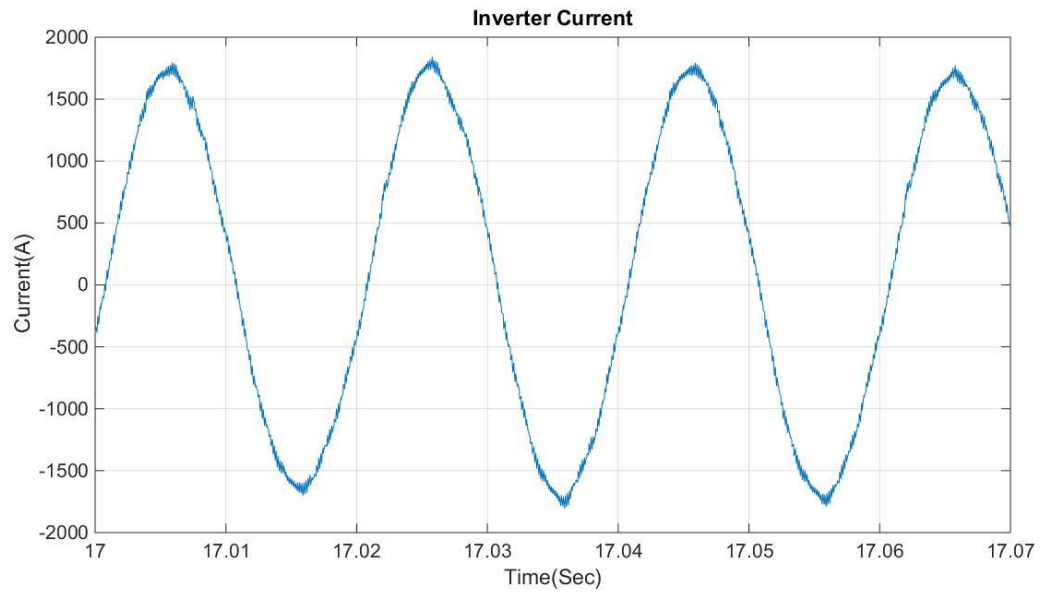
Fig. 4.36 The inverter output current

From the simulation results it can be concluded the proposed topology can work properly at HVDC system level considering the East-West Inter-Connector nominal values and has fast dynamic response to active power and reactive power variations on inverter side.

4.5 Converter Reliability Improvement Under Sub Module Capacitor Failure Condition

4.5.1 Faults in Sub Module Capacitors

As discussed in Chapter 2, there are different types of sub module faults that can strike MMCs and affect their operation. Since MMCs are used in important applications and are a big investment, it is extremely important to design fault tolerant topologies which can very quickly protect the whole system from sudden failures. The proposed topology has more reliability during the sub module capacitor failure and keeps the system in normal operation condition. The sub module capacitor plays an essential role in the operation of the MMC; however, it may suffer from a lot of problems that can severely affect their operation, such as sensitivity to temperature and frequency.

Table. 4.5 Faults in sub module capacitors

Fault Type	Failure Mechanism	Consequences
Open circuit	1) Leakage of electrolyte dielectric material 2) Loose connections of terminals	1) Increase in the capacitor voltage, current, and temperature 2) Mechanical vibration
Short circuit	Dielectric breakdown	Increase in the capacitor voltage, current, and temperature
Fault in capacitor structure	Change in the electrolytic capacitor structure and capacitance value	Increase in the capacitor voltage, current, and temperature

One of the most critical problems is the wear-out degradation failure. The main consequence of this failure is the increased equivalent series resistance (ESR). This ESR increase affects the rate of charge and discharge and then the whole operation of the

capacitor [153]. In addition to the wear-out failure, the submodule capacitor may be exposed to open circuit and short circuit failures, as shown in Table. 4.5.

The capacitor short circuit fault is the only fault type that needs the converter to be shut off, while, in all other fault types, it is not required to shut off the converter. The detection of capacitor faults is not considered in this thesis.

4.5.2 Operation of the Proposed Design Under Sub Module Capacitor Failure Condition

Modular Multilevel Converters (MMCs) are vulnerable to internal faults because of the large number of series connected sub modules. Additionally, it is highly recommended not to block the converter even if it is subjected to internal faults to secure the supply, to increase the reliability of the system and prevent unscheduled maintenance.

Table. 4.6 Possible sub module capacitor failure states (capacitor open circuit considering the upper arm)

C_1	C_2	C_3	C_4	State Number
S	S	S	S	1
S	S	S	F	2
S	S	F	F	3
S	F	F	F	4
F	F	F	F	5
F	S	S	S	6
S	F	S	S	7
S	S	F	S	8
F	S	S	F	9
S	F	F	S	10
F	S	F	S	11
S	F	S	F	12
F	F	S	S	13
F	F	F	S	14
F	F	S	F	15
F	S	F	F	16

S means safe capacitor and F means faulty one.

This thesis introduces a fault tolerant MMC topology which can operate in normal as well as sub module capacitor failure conditions. For the new design with 8 sub modules across both arms, possible states of the sub module capacitor failure (capacitor open circuit) considering the upper arm are mentioned in Table. 4.6. Operation with bypassing is the other alternative for the MMC continuous operation. However, in the case that the bypass switch is faulty, the proposed design can keep system in the operational mode, so the contribution is still valid.

During the capacitor open circuit fault, the output voltage will have some spikes during the faulty period. This is because of open circuit capacitors and losing some voltage levels. The pattern of spikes depends on the location of fault and takes 1 second in the simulation. Moreover, these spikes don't have any significant impact on the maximum allowable IGBT current. Considering the worst case with two faulty sub modules at the upper arm and two faulty sub modules at the lower arm, the output current will not exceed from the maximum allowable IGBT current because of the spikes. More details about this state and its operational logic will be explain later in this section. Fig. 4.37 shows the output current variation for this state. At t=9 Sec fault occurs and at t=10 Sec the new design comes to the circuit.
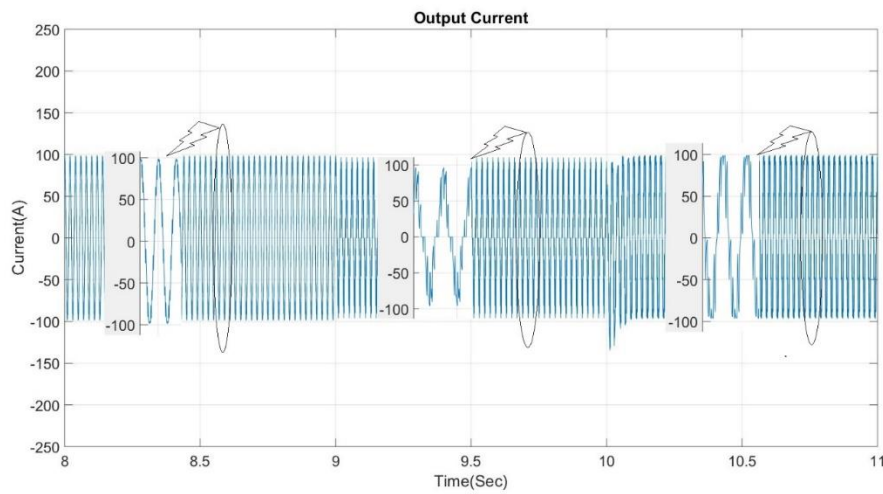
Fig. 4.37 Output current variation with two faulty sub modules at the upper arm and two faulty sub modules at the lower arm and considering the new design after t=10 Sec

There is only small transient after t=10 for few milliseconds. Similarly, the output current will not exceed from the maximum allowable IGBT current in the other faulty states considering the proposed topology.

When the capacitor open circuit fault happens at C_4 and two capacitors are faulty at the same time the proposed design is not able to operate as a fault tolerant converter. As an exception, the only state that converter supports two faults at the same time is state 11. States of the sub module capacitor failure (capacitor open circuit) for the lower arm is like to the upper arm. Similarly, for the lower arm if the capacitor open circuit fault happens at C_8 and two capacitors be faulty at the same time the converter will not have fault tolerant capability. Possible fault tolerant states are shown with their switching algorithm at the following section.

State 6:
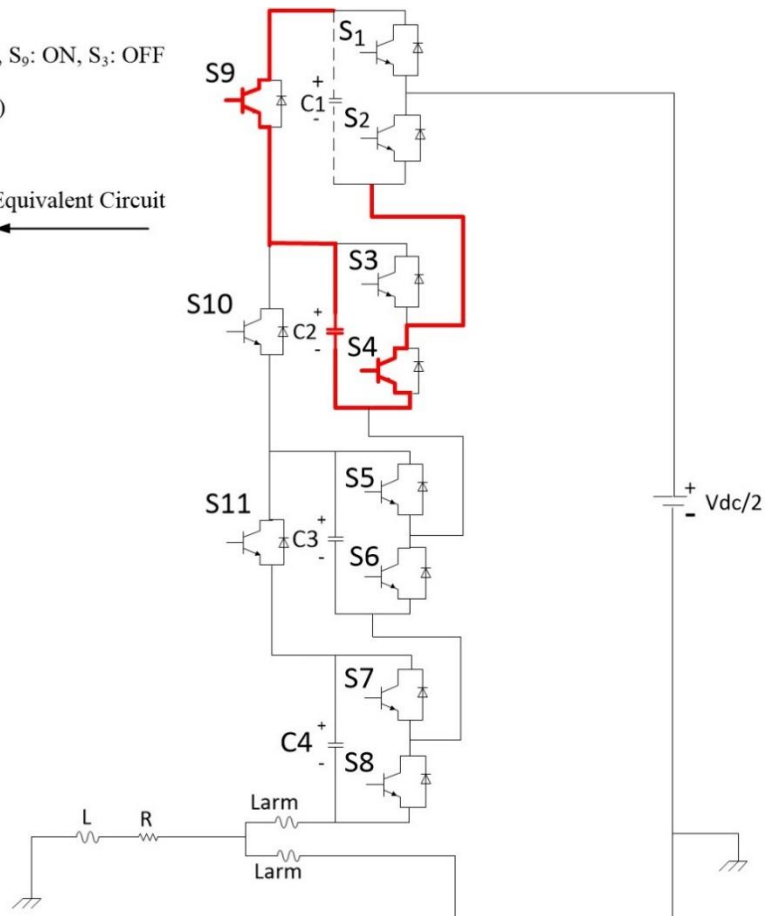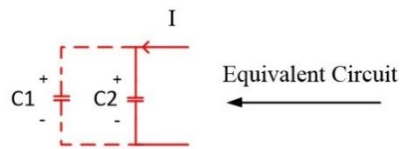
Fig. 4.38 Fault tolerant operation at state 6

In this case the faulty capacitor C_1 will be replaced by C_2.
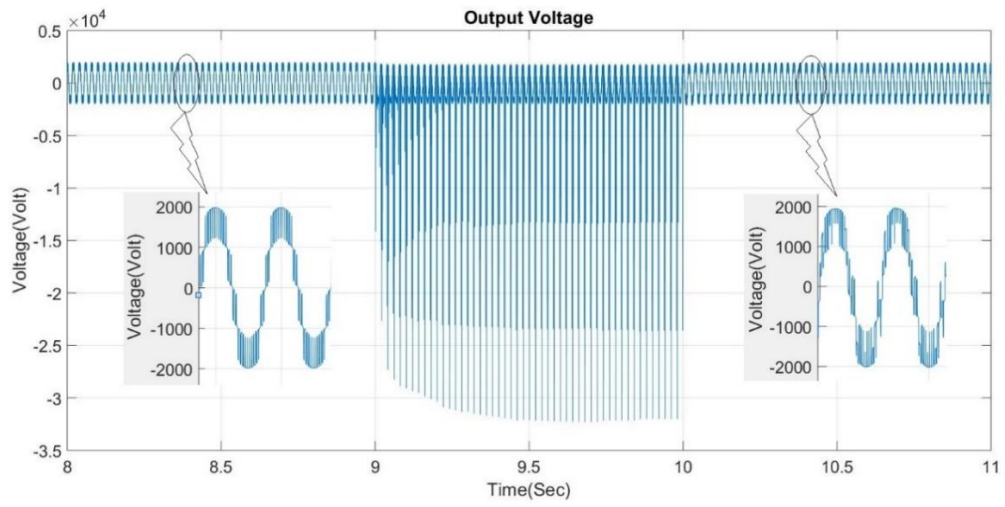
Fig. 4.39 Output voltage at state 6
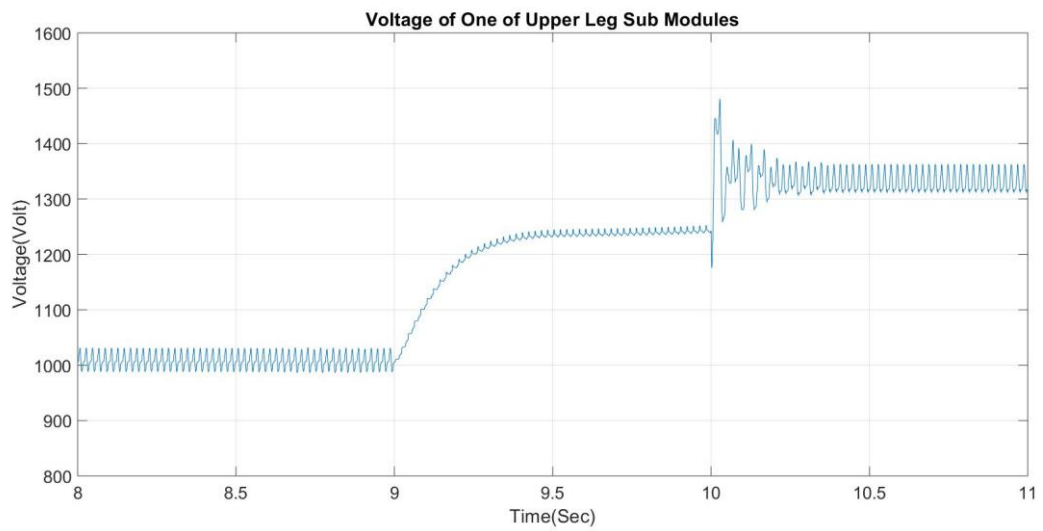
Fig. 4.40 Voltage of one of upper leg sub modules at state 6
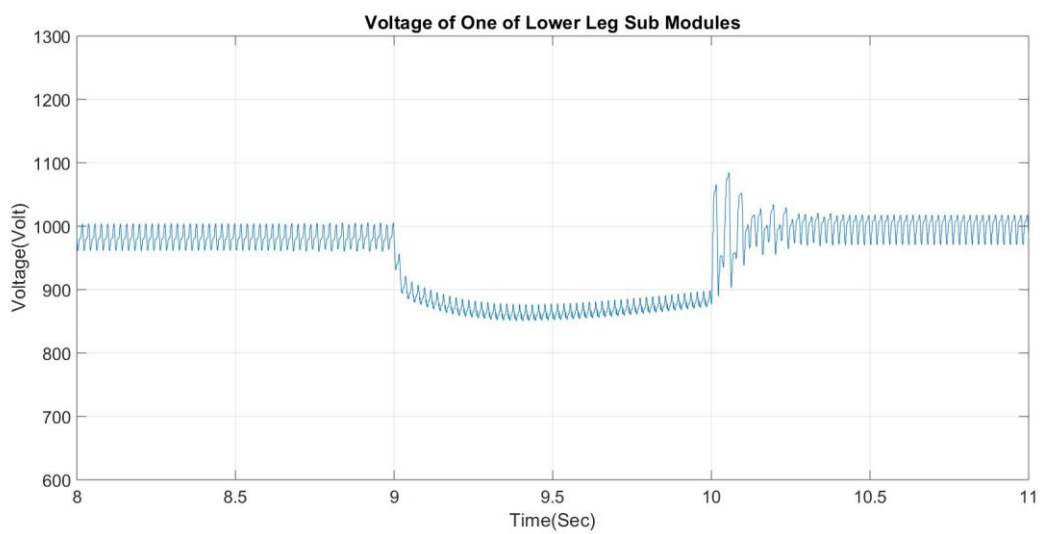
Fig. 4.41 Voltage of one of lower leg sub modules at state 6

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Considering simulation parameters from Table. 3.3 (4 kV DC system), when one of the sub module capacitors becomes open circuit at second 9, lots of spikes can be seen in the output voltage. At second 10 the new design comes to the circuit and produces the logic for switches to activate fault tolerant operation. Obviously one level voltage is lost (because one of the sub modules is gone) and this will lead to a little bit more THD at output voltage. However, the system can be kept in operational condition and work with more reliability. Considering that the capacitor open circuit fault happened at one of upper leg sub modules, the other three safe sub modules will be charged to 1333 volt. The lower leg sub modules will have the same voltage which is 1000 volt. The output voltage, voltage of one of upper leg sub modules and voltage of one of lower leg sub modules are shown in Fig. 4.39, Fig. 4.40 and Fig. 4.41.

States 7 and 8 are similar to state 6 as one of the sub module capacitors is faulty. Therefore, the output voltage and sub module voltage are like state 6.

State 7:
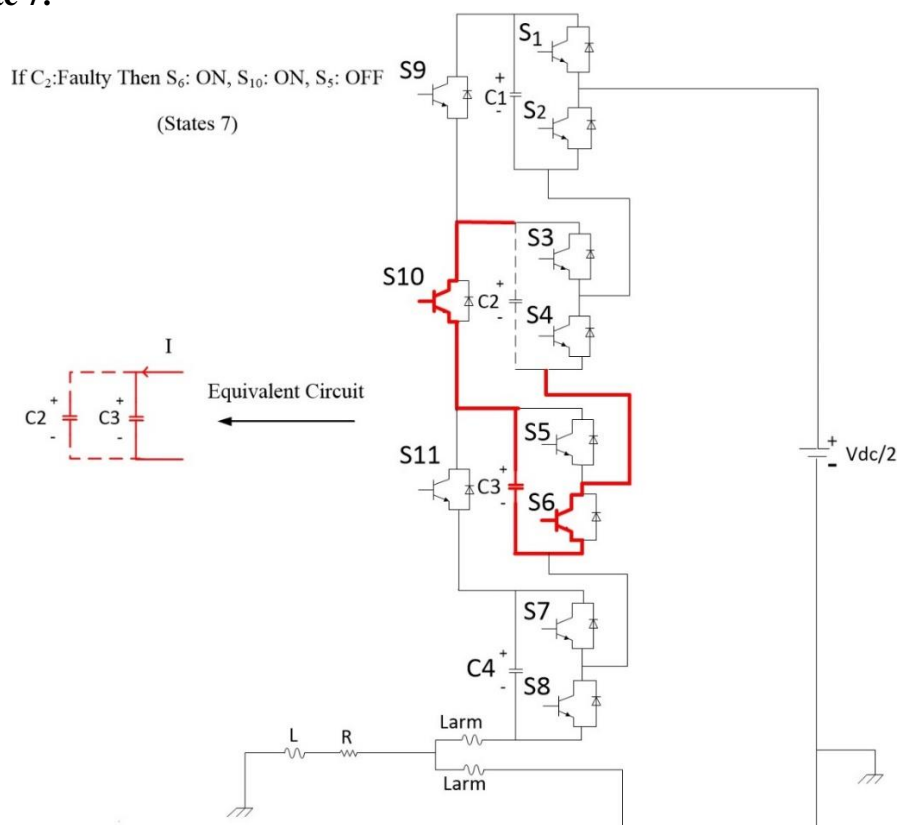
Fig. 4.42 Fault tolerant operation at state 7

State 8:

Fig. 4.43 Fault tolerant operation at state 8

State 11:

In state 11, C_1 and C_3 are faulty (open circuit) and they can be replaced by C_2 and C_4. As two sub modules are faulty at the same time, the output voltage will have more THD rather than one sub module faulty condition because of losing two voltage levels. Fig. 4.44 shows the fault tolerant operation of converter at state 11. Fig. 4.45, Fig. 4.46 and Fig. 4.47 depict the output voltage, voltage of one of upper leg sub modules and voltage of one of lower leg sub modules. In this case, the other two safe sub modules will be charged up to 2000 volt. At t=9 Sec capacitor faults occurs and at t=10 Sec the new design comes to the circuit. The lower leg sub modules will have the same voltage which is 1000 volt.

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If C₁:Faulty Then S₄: ON, S₉: ON, S₃: OFF

(States 11)

If C₃:Faulty Then S₈: ON, S₁₁: ON, S₇: OFF

(States 11)
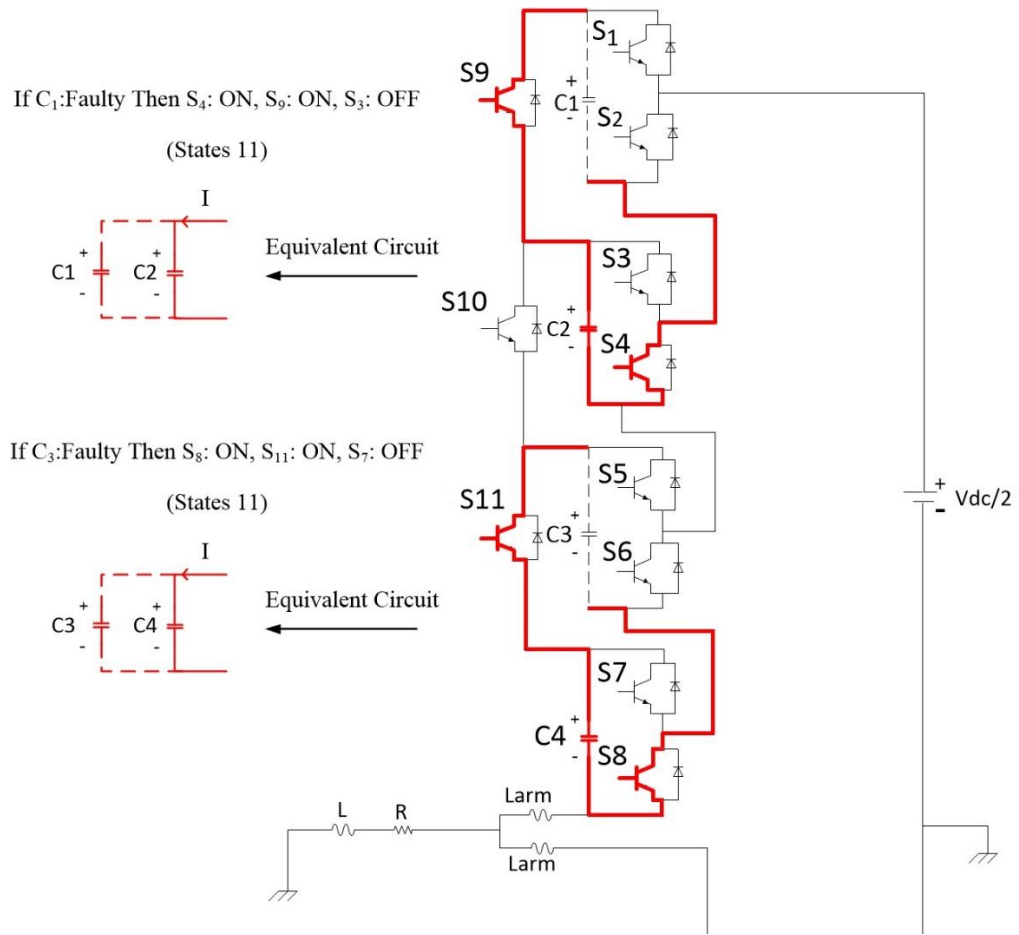
Fig. 4.44 Fault tolerant operation at state 11
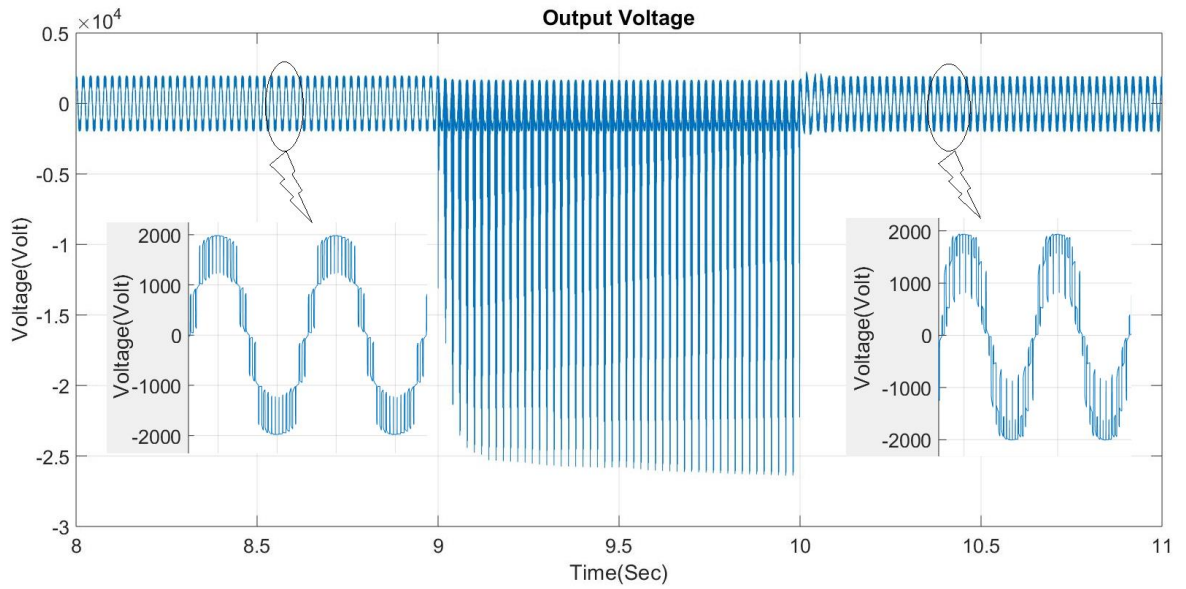
Fig. 4.45 Output voltage at state 11

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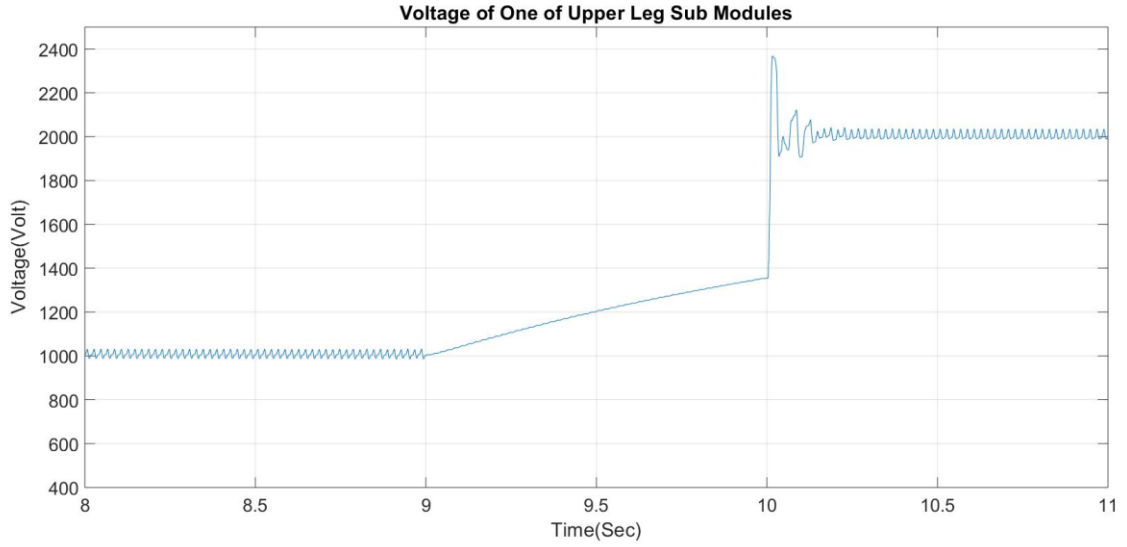
Fig. 4.46 Voltage of one of upper leg sub modules at state 11
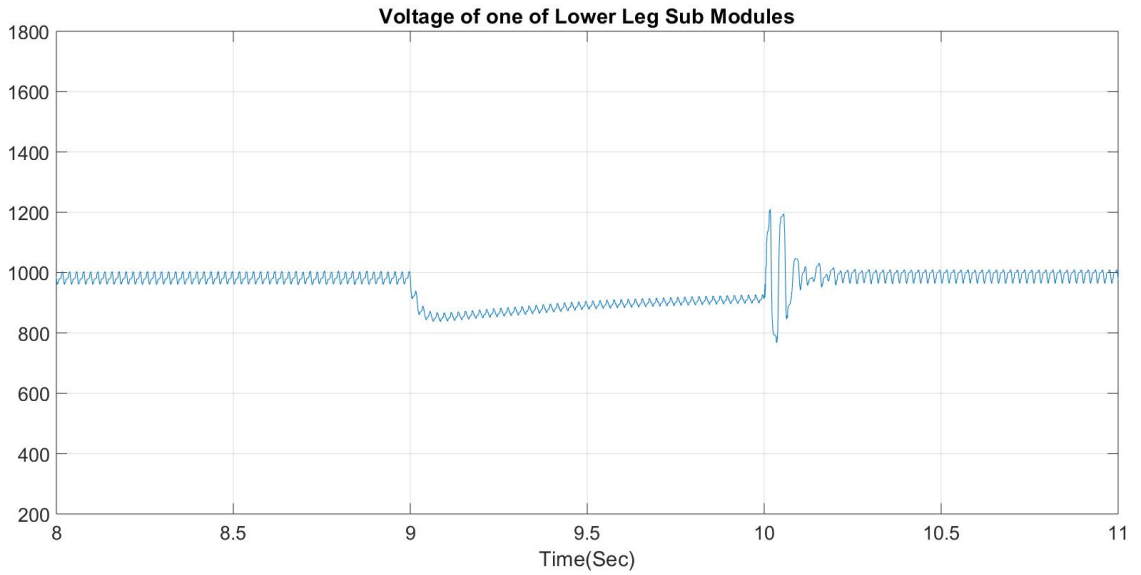
Fig. 4.47 Voltage of one of lower leg sub modules at state 11

Considering faulty sub modules for both arms simultaneously will lead to different results.

Two faulty sub modules at upper arm and one faulty sub module at lower arm:

Fig. 4.48, Fig. 4.49 and Fig. 4.50 show the results for two faulty sub modules at the upper arm and one faulty sub module at the lower arm. Fig. 4.48 shows the output voltage and because of losing 3 voltage levels, the output voltage will be more distorted even

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after applying the new design. Sub module voltage for the upper arm and the lower arm are presented in Fig. 4.49 and Fig. 4.50.
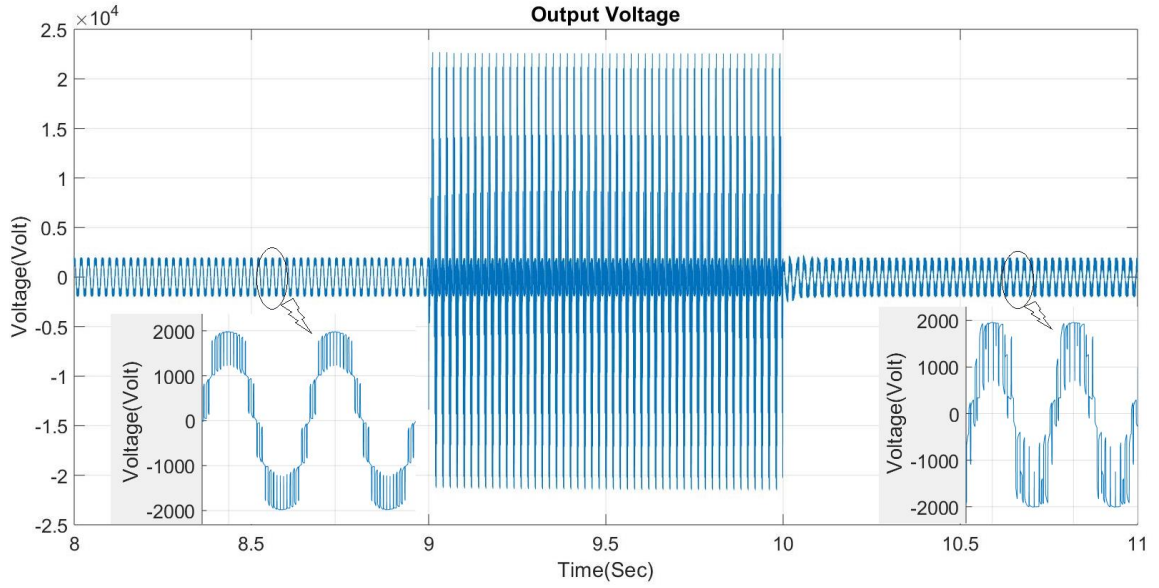
Fig. 4.48 Output voltage considering two faulty sub modules at the upper arm and one faulty sub module at the lower arm
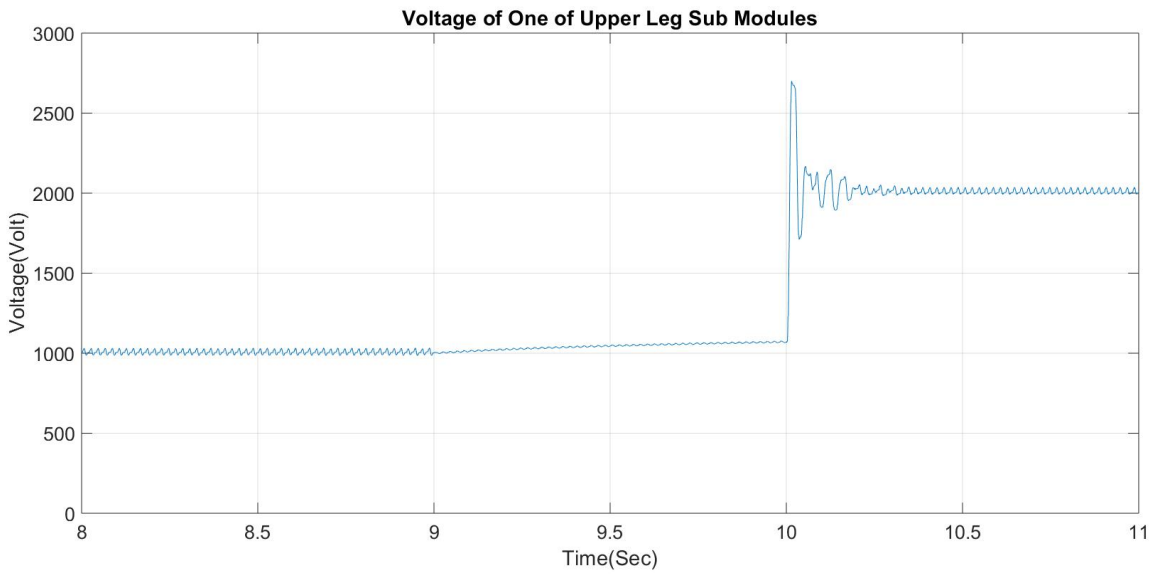
Fig. 4.49 Voltage of one of upper leg sub modules considering two faulty sub modules at the upper arm and one faulty sub module at the lower arm

Fig. 4.49 shows that after applying the new design at t=10 Sec, as there are only two safe sub modules at the upper arm each of them will be charged to 2000 volt. For the

lower leg as there is only one faulty sub module, the other three safe sub modules will share the 4000 volt equally and each sub module be 1333 volt.
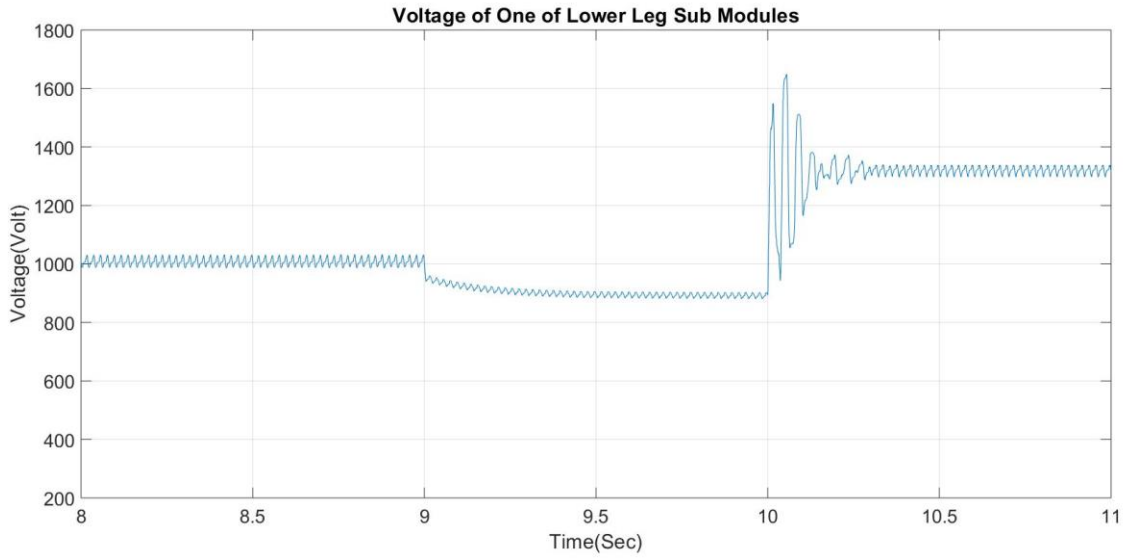
Fig. 4.50 Voltage of one of lower leg sub modules considering two faulty sub modules at the upper arm and one faulty sub module at the lower arm

Two faulty sub modules at upper arm and two faulty sub modules at lower arm:

Fig. 4.51 depicts the output voltage considering two faulty sub modules at the upper arm and two faulty sub modules at the lower arm which is more distorted because of losing 4 voltage levels.
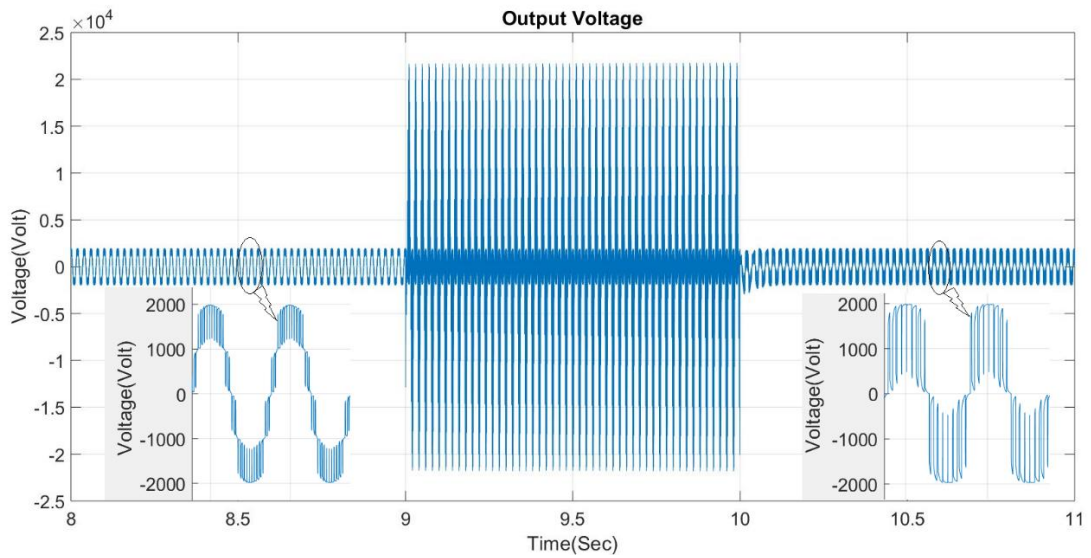
Fig. 4.51 Output voltage considering two faulty sub modules at the upper arm and two faulty sub modules at the lower arm

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The sub module voltage variations for the safe sub modules at the upper arm and the lower arm are shown in Fig. 4.52 and Fig. 4.53. Because of two faulty sub modules at the upper arm and two faulty sub modules at the lower arm, safe sub modules will be charged to 2000 volt.
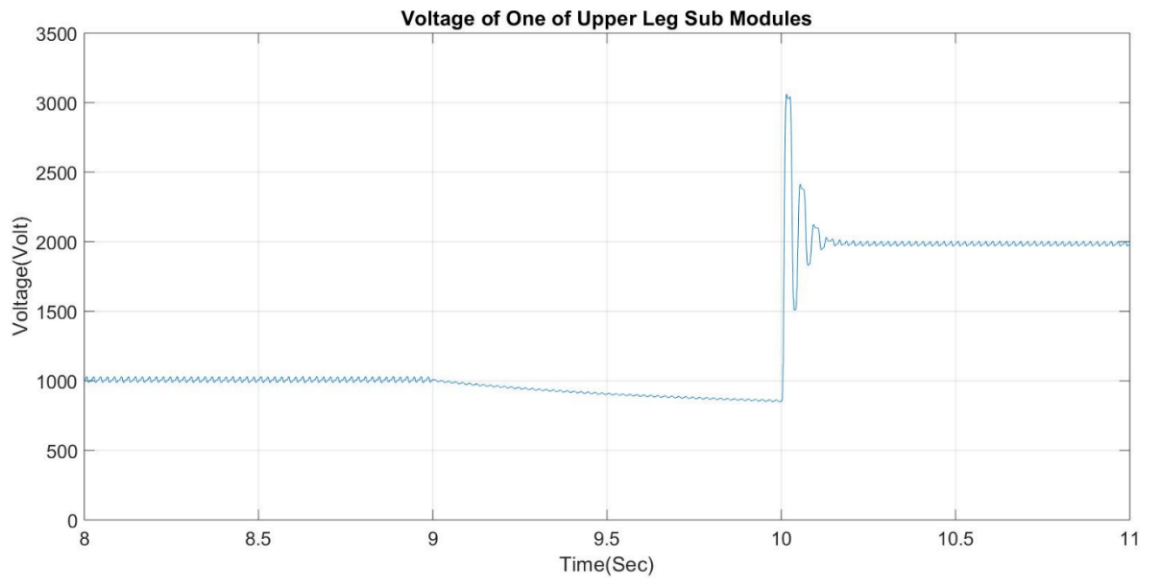
Fig. 4.52 Voltage of one of upper leg sub modules considering two faulty sub modules at the upper arm and two faulty sub modules at the lower arm
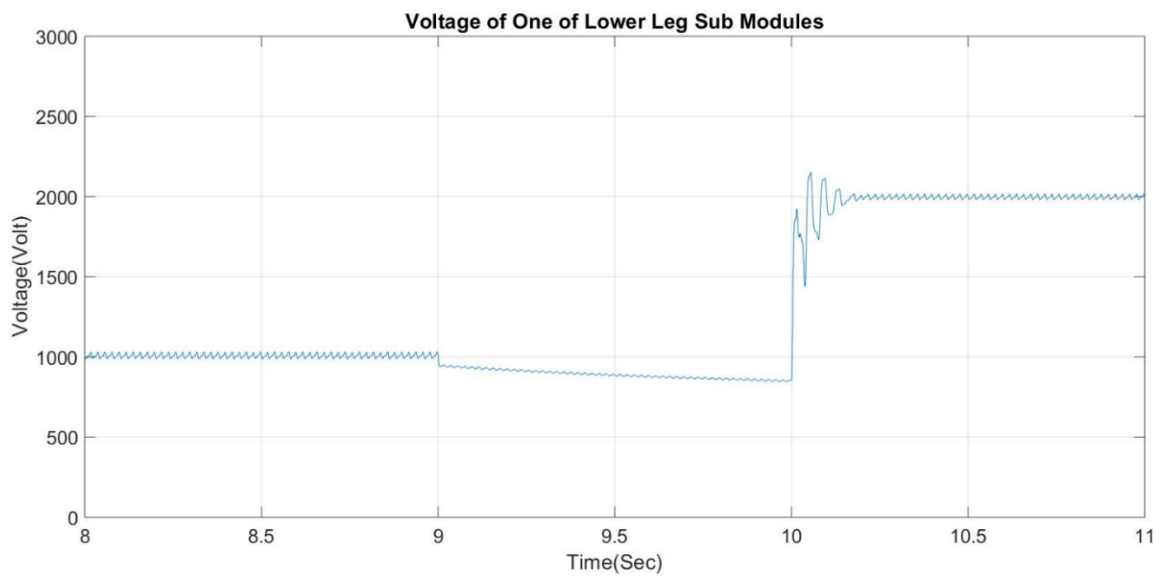
Fig. 4.53 Voltage of one of lower leg sub modules considering two faulty sub modules at the upper arm and two faulty sub modules at the lower arm

One faulty sub module at upper arm and one faulty sub module at lower arm:

The last scenario is one faulty sub module at the upper arm and one faulty sub module at the lower arm. Consequently, the output voltage has less distortion rather than the previous state. Fig. 4.54 illustrates the variation of output voltage. Fig. 4.55 and Fig. 4.56 represent the variation of sub module voltage for the upper arm and the lower arm.
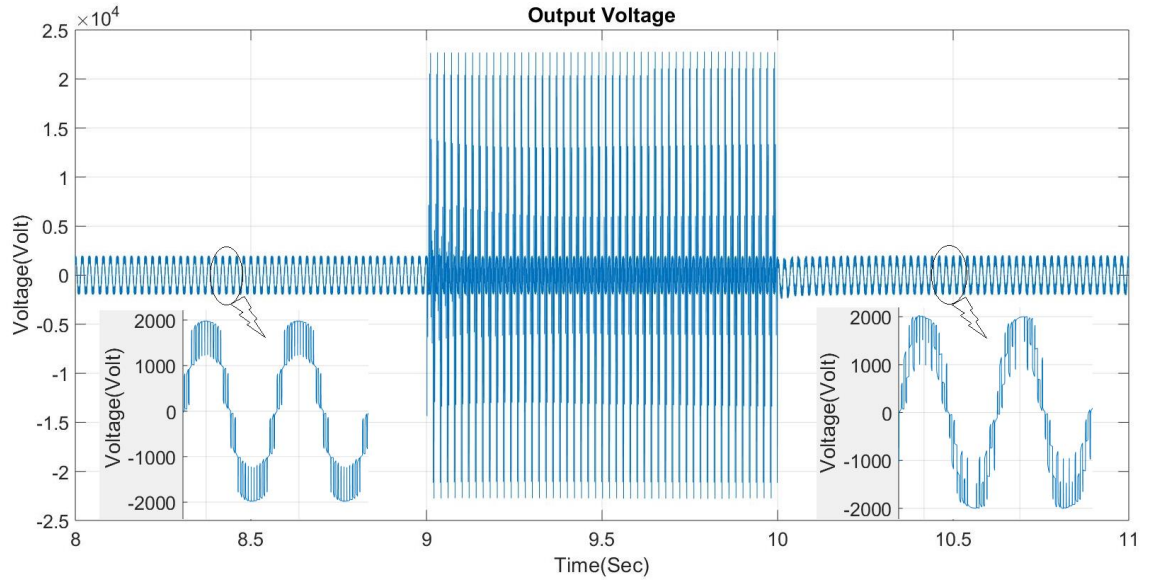
Fig. 4.54 Output voltage considering one faulty sub module at the upper arm and one faulty sub module at the lower arm
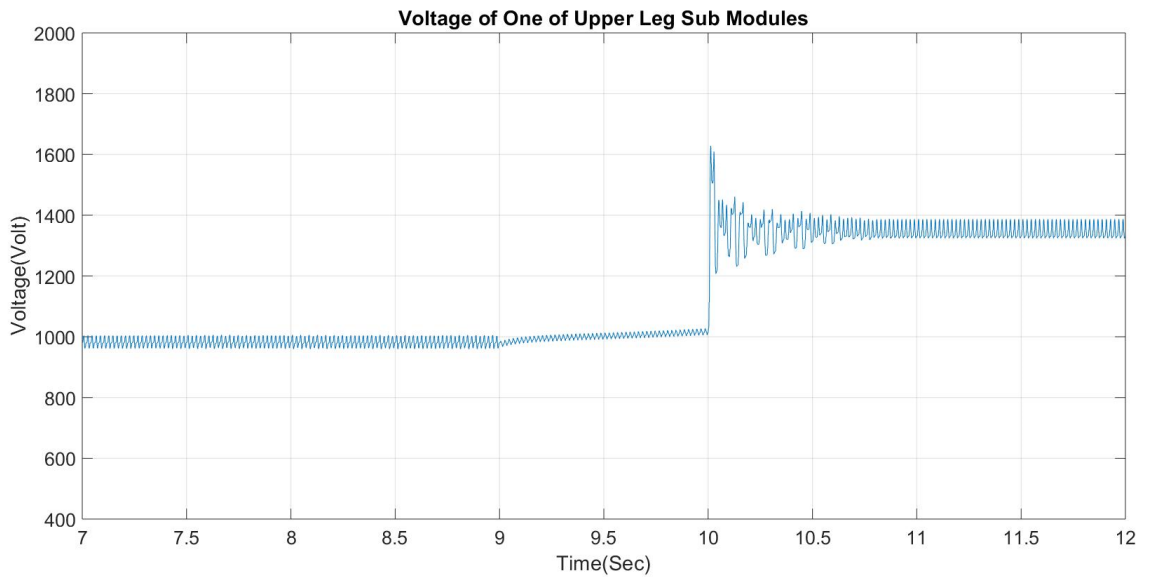
Fig. 4.55 Voltage of one of upper leg sub modules considering one faulty sub module at the upper arm and one faulty sub module at the lower arm

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Because of only one faulty sub module in each arm the other three safe sub modules will share the 4000 volts equally (Each sub module voltage will get 1333 volt).
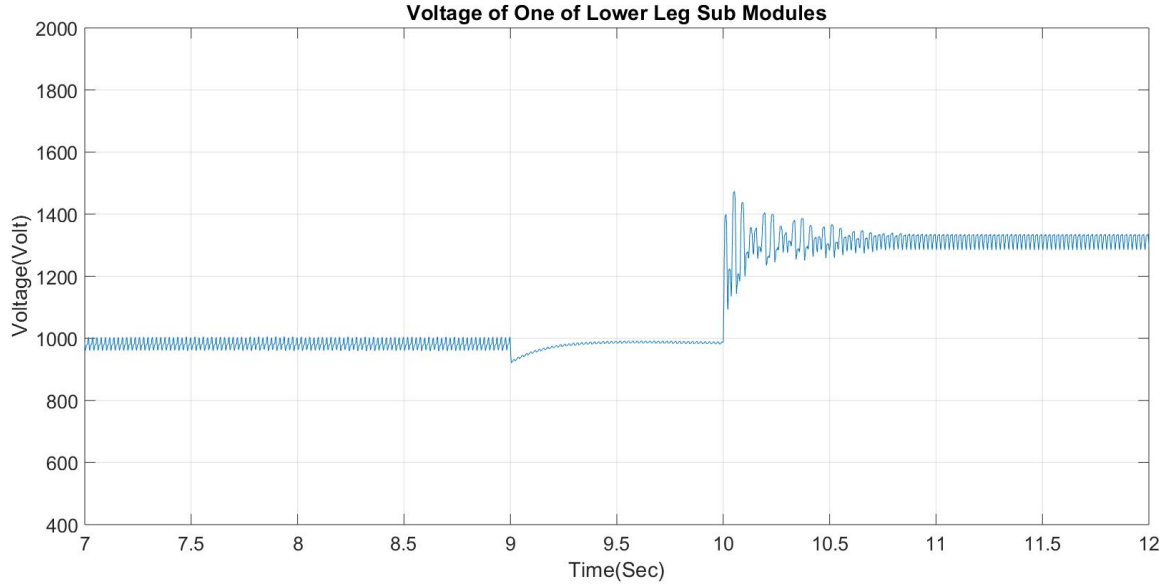
Fig. 4.56 Voltage of one of lower leg sub modules considering one faulty sub module at the upper arm

and one faulty sub module at the lower arm

4.6 Impact of Applying the Proposed Design at Reducing the Number of Sub Module Voltage Sensors

As discussed in previous chapters, to synthesize the voltage waveforms at the AC side of the MMC, multiple modulation techniques can be used. Most of them are based on defining the number of sub modules to be activated in each of the arms, and the particular sub modules are determined by a voltage balancing algorithm[154, 155]. Almost all these voltage balancing techniques operate in closed-loop and hence the values of the sub module capacitor voltages need to be known. In this thesis, a phase-disposition PWM (PD-PWM) technique with a voltage balancing algorithm based on measuring the capacitor voltages and the arm current direction is used. The capacitor voltages are usually obtained by direct measurement of all the sub module capacitors and the direction of arm currents are measured by current sensors at each arm. In real applications of the

MMC, the number of sub modules per arm (N) can reach into the hundreds. Therefore, many voltage sensors are required in order to provide signal measurements that need to be acquired and adapted. Aside from compromising its reliability, this complicates the implementation and control of the MMC.

To address this issue, the proposed design doesn't use any voltage sensors or current sensors required in the MMC. A low number of sensors per arm reduces the cost of the converter and improves its reliability, since the number of devices that can fail is lower. Simulation results of the proposed design without using any voltage sensors illustrates the operation of converter for the reliability improvement.

4.6.1 Simulation of the Proposed Design Without Using Voltage Sensors

For the first 10 sec of the simulation a classic half bridge DC side cascaded topology operation is simulated without using any voltage sensors and at t=10 Sec the simulation of the proposed new topology commences. Table. 4.7 depicts the simulation parameters of system without considering voltage sensors.

Table. 4.7 depicts the simulation parameters of system without using voltage sensors

Parameter	Value	Parameter	Value
Number of SMs in each arm	4	Carrier frequency	250 Hz
Number of Half-Bridge in each arm	4	DC bus voltage	4 kV
SM capacitor voltage	1 kV	SM capacitance	3.3 mF
Arm inductor	4 mH	Output power	100 kW

Fig. 4.57 and Fig. 4.58 illustrate the sub module voltage variation for one of upper arm sub modules and one of lower arm sub modules without using voltage sensors and considering the new design after t=10 Sec.
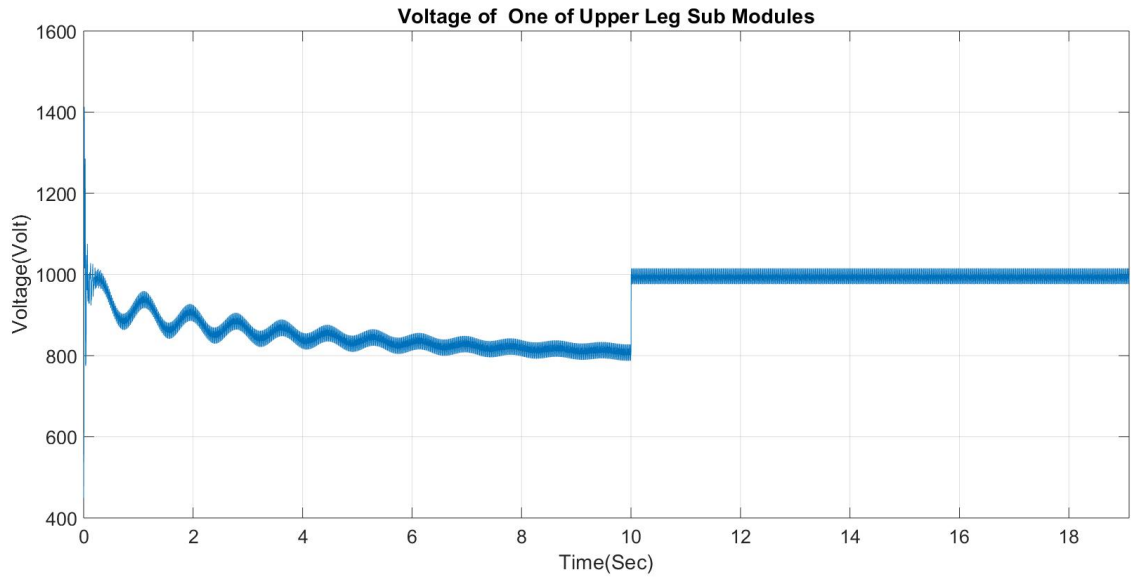
Fig. 4.57 The sub module voltage variation for one of upper arm sub modules without using voltage sensors and considering the new design after t=10 Sec
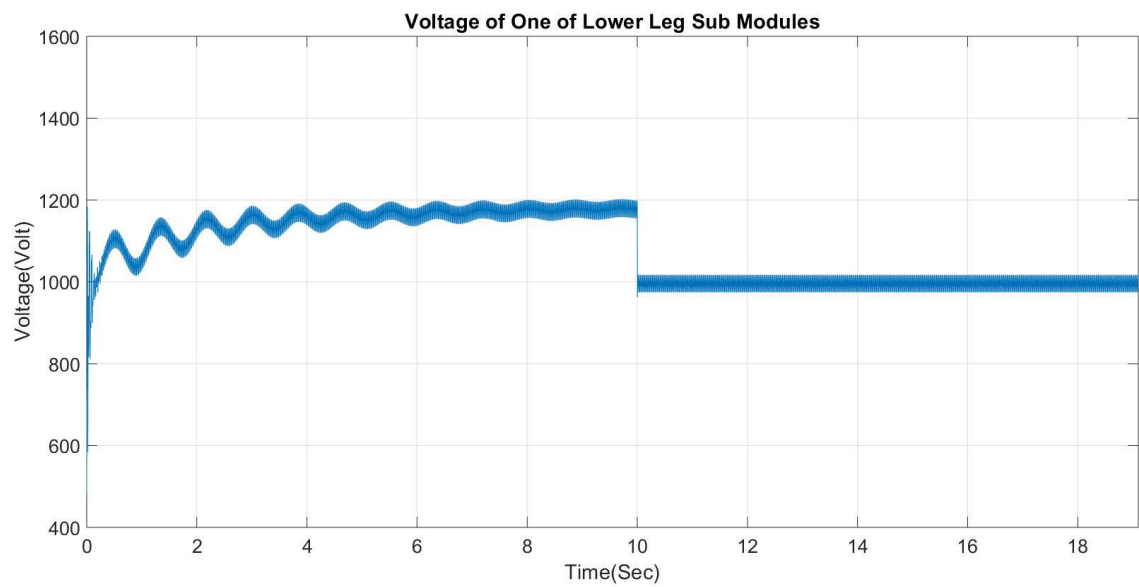
Fig. 4.58 The sub module voltage variation for one of lower arm sub modules without using voltage sensors and considering the new design after t=10 Sec

The new proposed topology can stabilize the converter operation without needing any voltage sensors. It comes to the circuit at t=10 Sec and adjusts all sub module capacitor voltages to 1 kV. The output voltage considering the new design without any voltage sensors is shown in Fig. 4.59.
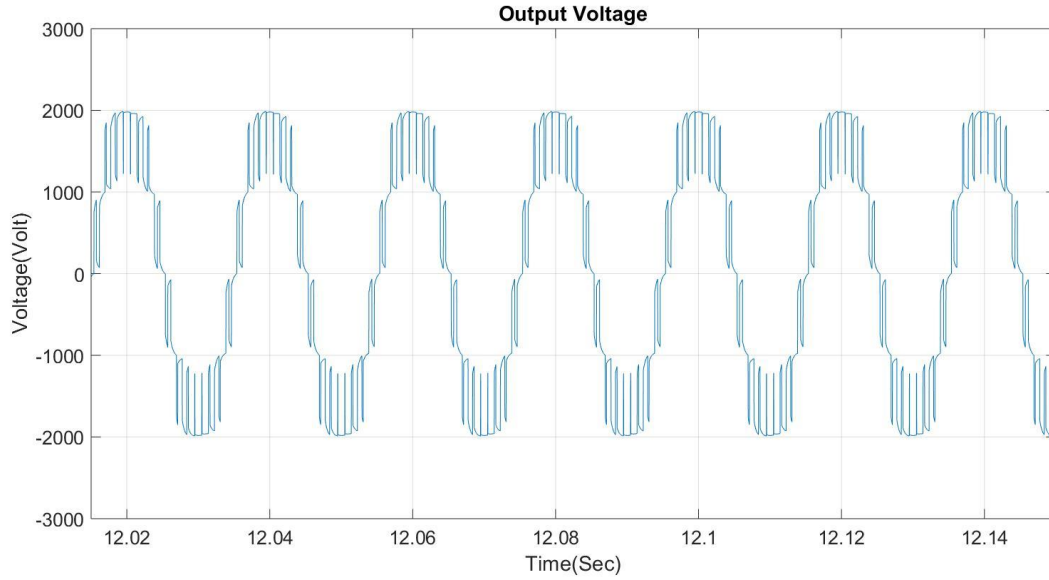
Fig. 4.59 The output voltage variation considering the new design without using voltage sensors

The circuit configuration of the modular multilevel converter (MMC) requires many current and voltage measurements as well as communications within the converter arms and between the arm controllers and the main control circuit. The proposed topology reduces circuit complexity and hardware requirements with their associated cost, while adding an additional level of reliability to the operation of the MMC. It can operate without any requirement to voltage sensors and adjust the sub module capacitor voltages. This substantial reduction in the number of voltage sensors improves the system reliability and decreases its cost and complexity. Proposing a new design always cannot improve all aspects at the same time but can improve the efficiency even with more switches.

4.7 Chapter Summary

This chapter proposes the application of proposed topology at HVDC system level considering the nominal values of East-West Inter-Connector. Loss and efficiency analysis also are investigated in section 4.3 and point to point HVDC connection is created to study operation of the system during the dynamic load change condition. Converter reliability is the other subject which is improved using the proposed design during some sub module capacitor failure conditions and investigated in section 4.4. Moreover, the proposed topology doesn't need any voltage or current sensors to regulate the sub module voltages. As a result, this improvement will reduce the total cost and the complexity of the converter. At the same time the converter reliability will get better. The last part of this chapter investigates about the operation of the proposed design without using any voltage or current sensors. Loss and efficiency calculations at HVDC system level confirms the converter efficiency improvement during operation at lower switching frequencies. Simulation results confirm the effectiveness of proposed design during sub module capacitor open circuit conditions. Moreover, the proposed topology can regulate the voltage of sub module capacitors without using any voltage and current sensors. As a result, it will reduce the total cost and the complexity of the converter. At the same time the converter reliability will get better. Simulation results validate the operation of proposed new topology without using voltage or current sensors.

Chapter 5: Conclusions and Future Work

5.1 Conclusions

This thesis proposes a new topology for modular multilevel converters (MMC's). The comparative study between different MMC topologies indicates some disadvantages which can affect their performance and MMC power losses is one of them specially in HVDC applications. To solve this issue, the switching frequency should be kept low to reduce the converter switching power losses. However, choosing the switching frequency very low will impose higher voltage ripples on the sub module capacitors which will lead to choose a large sub module capacitor to eliminate ripples and is uneconomical option. The proposed topology decreases the sub module capacitor voltage ripples at lower switching frequencies without the need for large sub module capacitors using additional switches and the capacitors that are idle during the switching period. Simulation results confirm the effectiveness of the proposed topology with reduced sub module voltage fluctuation at lower switching frequencies. Loss and efficiency calculations at HVDC system level considering the nominal values of East-West Inter-Connector confirms that the converter efficiency is improved during operation at lower switching frequencies. Moreover, the point to point HVDC connection considering the new design has been studied to show the operation of converter during dynamic load change.

The other important challenge of using modular multilevel converters is their reliability as they have lots of components specially when the number of sub modules is high. The proposed topology has capability to keep converter in normal operation condition during sub module open circuit fault condition. Using additional switches, the faulty capacitors will be replaced by safe capacitors. However, because of losing some voltage levels the output voltage will have more THD. Simulation results confirm the

effectiveness of proposed design during sub module capacitor open circuit conditions. Moreover, the proposed topology can regulate the voltage of sub module capacitors without using any voltage and current sensors. As a result, it will reduce the total cost and the complexity of the converter. At the same time the converter reliability will get better. Simulation results validate the operation of proposed new topology without using voltage or current sensors.

In all, this thesis provides the new MMC topology to address the issues related to MMC operation at lower switching frequencies, MMC sub module voltage fluctuations and its high circulating current value at lower switching frequencies, MMC power losses, MMC reliability and its total cost and the complexity because of using voltage and current sensors. The main drawback for the proposed topology is when the number voltage levels need to be higher. In this case, the simulation will be quite complicated and slow. Therefore, the average model will be needed to decrease the simulation time. The following major contributions are made in this thesis:

- Proposing the new topology for MMC which can work in lower switching frequencies condition. This aspect is verified in section 3.3.

- Elimination of the sub module voltage fluctuations at lower switching frequencies without any need to big sub module capacitor values as the proposed design uses the idle capacitors during the switching period. This aspect has been demonstrated in section 3.3.

- Mitigation of the circulating current content at lower switching frequency operation condition. This is achievable by applying the new design and the content of the circulating current will be at the same range of higher switching frequency condition. Simulation results in section 3.3, confirm the effectiveness of proposed topology at lower switching frequency condition.

- Decreasing the converter losses as well as its efficiency improvement by using the proposed design at a lower switching frequency. Loss analysis at section 4.3 in medium voltage level and HVDC system voltage level verifies efficiency improvement of the proposed topology rather than classic MMC topology.

- Converter reliability improvement by using the proposed new topology which keeps the converter at working condition during the sub module capacitor open circuit fault. Faulty capacitor is replaced by safe one. However, some voltage levels will be lost because of faulty sub modules. Simulation results in section 4.5, verify the efficiency of converter during the sub module capacitor open circuit condition.

- Decreasing the converter cost and complexity by elimination of using voltage and current sensors in the proposed design. This will lead to improvement of converter reliability as well. All sub module capacitor voltages will be regulated without any need to the PI controller as well as voltage sensors. Simulation results in section 4.6, confirm that the proposed topology can operate without voltage sensors and regulate the voltage of sub module capacitors.

5.2 Future Work

The following research points could be investigated in future:

- The proposed topology uses the Phase-Shift-PWM modulation technique. Other modulation techniques could be studied, in order to determine the most suitable switching algorithm for this design.

- Developing a solution to represent the MMC dynamic behaviour using an average model is challenging and complicated. The average MMC model can be further developed to the proposed design to simulate DC faults and other transients.

- The basic building block of the proposed MMC employed in the new design is a half-bridge-based sub module (HBSM). However, an HBSM-based MMC (HB-MMC) does not have a DC fault blocking capability. Using full-bridge-based sub modules could be a solution. However, as explained in Chapter 3 it is not practical to consider full bridge sub modules in the proposed design. In further research, proposing the new sub module topology which has the DC fault blocking capability and is compatible with the new design could be investigated.

- The proposed design can operate at low switching frequencies which can improve the converter efficiency. Several papers have referred to soft-switching techniques for MMCs, which can effectively decrease switching losses and thereby further improve efficiency. In further research, it would be worth investigating to compare the classic MMC converter efficiency by introducing soft-switching techniques with the proposed design at low switching frequency.

- Techno-Economic evaluation of the proposed new MMC topology and economic considerations.

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