RELIABILITY ANALYSIS OF SINGLE-PHASE PHOTOVOLTAIC INVERTERS WITH REACTIVE POWER SUPPORT

BY

CHARLES J. MURRAY

THESIS

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Adviser:

Associate Professor Patrick Lyle Chapman

ABSTRACT

Reactive power support is expected to be an emerging ancillary requirement for single-phase photovoltaic (PV) inverters. This work assesses related reliability issues and focuses on the second stage or inversion process in PV inverters. Three PV inverter topologies are analyzed and their reliability is determined on a component-by-component level. Limiting operating points are considered for each of these topologies. The capacitor in the dc link, the MOSFETs in the inverting bridge, and the output filter are the components affected. Studies show that varying power-factor operation with a constant real power output increases the energy storage requirement as well as the capacitance required in the dc link in order to produce the double-frequency power ripple. The overall current rating of the MOSFETs and output filter must also be sized to accommodate the current for the apparent power output. Modeling of the inverter verifies the conditions for each of the components under varying reactive power support commands. It is shown that the production of reactive power can significantly increase the capacitance requirement, but the limiting reliability issue comes from the increased output current rating of the MOSFETs.

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1. BACKGROUND

Electricity consumption in the United States has steadily grown for the past 50 years [1]. Energy security issues and detrimental environmental effects of fossil fuel electricity sources have led to an increased interest in renewable energy. Accordingly, wind power and photovoltaic (PV) markets have seen steady growth in the past five years [2]. Although there has been increased production of these technologies, renewable sources still account for a very small portion of energy generation [1]. Despite holding a small market share, it is very likely that the dependence on renewable sources will only increase in the future. There are several programs at both the state and federal levels that lay out specific targets or guidelines for renewable energy generation capacity or energy production. These targets range from 10% to 33% before a given year [3], and ensure a large investment in the development of renewable generation.

Renewable energy sources provide additional challenges to grid operators since the prime movers, solar radiation and wind, are intermittent. Although there are very technologically advanced forecasting tools for predicting wind and the amount of sun that shines, on a time scale of minutes or seconds, there are transient disturbances in the form of wind gusts or clouds and other forms of shading. The source intermittency is represented by a capacity factor which is the ratio of the power output of a system to its rated power over a period of time. Capacity factors for solar are on the order of 20% [4]. Due to small market share and low capacity factor, renewable energy sources are not held to the same interconnection requirements as fossil fuel based generation. On the other hand, since renewable generation tends to be more dependent on power electronics, there is an opportunity for these sources to provide additional support to the grid.

1.1 RENEWABLE ENERGY SYSTEMS INTERCONNECTION POLICY

There has been a major shift in the interconnection standards of renewable energy systems, but most of the new requirements have been applied to wind generation. Although there appears to be a similarity in the way wind power and PV interact with the grid, there are glaring differences. From a perspective of scale, in the United States wind generated more than 50 times the energy of solar power in 2008 [1]. The typical wind farm is on the order of 50-250 MW [5]. On the other hand, PV plants tend to be on the order of 1-100 kW although there are several larger projects planned for completion by 2014 [6]. As of 2008 the majority of new PV installations were in the residential sector [2]. The average size of these installations was 4.9 kW [2]. The implication of this is that the majority of PV installations in the United States are in single phase 240 V distribution systems. From the interconnection perspective, distribution and transmission networks have very different regulations. As solar energy sources reach high penetration, it is likely that many of the regulations for wind at the transmission level will be imposed upon solar at the distribution level.

High penetration for renewable generation sources is typically considered to be 30% of generation [4]. For the first major shift in policy regarding the interconnection of renewables, energy policy in Europe must be reviewed. There has been more development of renewable energy sources in Europe largely due to more expensive electricity prices and aggressive tax incentives from certain countries. The German utility E.ON started an interconnection code for wind turbines that required a maintained connection during a fault or low voltage condition [7]. Newer standards include wind turbines' ability to produce reactive power [7]. These standards are seeing rapid adoption in the United States, and there has been much speculation over which

of these ancillary services will be required for solar and wind in the context of distributed generation.

Distributed generation will be expected to support a long list of ancillary services. The main concerns include voltage regulation from reactive power support, power quality, harmonics, flicker, dc injection, unintentional islanding, protection design, equipment grounding, load and generation imbalance, generation interaction with controllable loads, and storage as well as storage control [8]-[10].

The basic concept of using reactive power to help support voltage comes from the fact that most distribution feeders—and more specifically, transmission lines—have higher inductance than resistance. By manipulating the reactive current of the energy source, the line voltage drop can be changed as needed to maintain ideal voltage for a specific location. This concept is typically employed at the transmission level by utility scale generation. PV inverters offer an opportunity to produce reactive power low in the system at the distribution level. This thesis will review some of the new hardware constraints that will be caused by reactive power support from photovoltaic inverters.

1.2 PHOTOVOLTAIC SYSTEM AND INVERTER CONFIGURATION

PV systems can be broken up into two categories: off-grid and grid-connected [2]. In an off-grid system, some energy storage device is typically employed. In this configuration there is no interaction between the PVs, the inverter, or the energy storage, and the grid. The energy storage and PV typically energize local loads. This is common in remote locations when the expense of running electrical service outweighs the costs of energy storage technology. Because there is no

interaction between the grid and the PV inverters, the off-grid system will not be considered in this thesis.

All utilities are required to provide net metering for their customers [11]. Grid-connected systems are more typical in the United States, and in 2008 87% of the new installed capacity of PV was grid connected [2]. Currently all of these buy-back plans are based upon the real power that is produced by a PV system owner. Electric meters at the residential scale do not typically measure reactive power as it is consumed or produced and currently there are no financial incentives for reactive power support.

1.3 System Scale and Micro-Inverters

A new development in photovoltaic markets has been the introduction of micro-inverters. In the past, inverters have catered to the power levels of the entire PV system level. These system scale inverters would be connected to a bank of PV panels with some in series and some in parallel. Connecting panels in series increases the voltage applied to the inverter, and parallel strings of panels increase the current. The standards for an SMA 5 kW inverter are shown in Table 1 [12]. The new development has been the micro-inverter or back-of-the-panel inverter. These smaller inverters would perform the dc-ac conversion at the panel level. Micro-inverters eliminate all dc wiring, and can increase a system's efficiency by performing maximum power point tracking (MPPT) at the panel level. Although the dc voltage input is significantly less, micro-inverter manufacturers are able to increase the reliability of the inverters. The specifications for an Enphase micro-inverter are also shown in Table 1 [13]. The following analysis will show that the input voltage, whether it be from a panel or system, has a large impact on the design constraints and reliability when producing reactive power from an inverter.

Table 1 Kilowatt scale and micro-inverter specifications

Inverter	MPPT Voltage (V)	Ac Output Power (W)	Peak Efficiency (%)	Warranty (Years)
Sunny Boy 5000	250-480	5000	96.8	10
Enphase M 190	22-40	190	95.5	15

1.4 INVERTER STANDARDS

All PV panels produce dc power. The conversion of this dc power to the US standard of ac power at a frequency of 60 Hz is accomplished using an inverter. There are many different types of inverters, and circuit topology, power rating, efficiency, and reliability vary between make and model. Overall behavior is governed by a few regulatory bodies. The three main standards that pertain to PV inverters are UL 1741 *The Standard for Safety of Inverters, Converters and Controllers for Use in Independent Power Systems*, IEEE 1547 *Standard for Interconnecting Distributed Resources with Electric Power Systems*, and for installation at the residential and commercial level the *National Electric Code (NEC)* [14]-[16].

The standards outlined in the first two of these documents cover operating limits such as grid voltage highs and lows as well as frequency limits and harmonic/dc injection. There are additional standards that cover anti-islanding protection and the total harmonic distortion that is considered tolerable. *Anti-islanding* means that when the grid voltage cuts out, either through a fault or intentional disconnection of service, the inverter can no longer inject current into the grid and must wait until a specified time of "ideal" voltage conditions before reconnecting. This is designed to protect utility workers. There is a chance that they may consider a line to be disconnected from its source, but in fact it is being fed by PV or other distributed generation.

Another issue of islanding is if, during an outage, the grid drifted out of phase with the energy source. Then when the line is energized without synchronism, there would be large current spikes. Some of the basic passive standards are described in Table 2.

Table 2 IEEE 1547.2-2008 standards [15]

Standard	Limit
Over Voltage (OV)	110% Rated
Under Voltage (UV)	88% Rated
Over Frequency (OF)	60.5 Hz
Under Frequency (UF)	59.3 Hz

These requirements are very rigid and will limit an inverter's ability to support ancillary services. For example, low voltage ride-through is a standard that for a specified voltage sag, a generator must remain connected to the grid. This standard was established because a loss of generation during voltage sag, or low frequency event, will tend to increase the impact of the event on the utility grid. During such low voltage events, the passive anti-islanding protection described in Table 2 will automatically disconnect the inverter from the grid.

Inverters providing reactive power compensation to the grid will need more advanced methods for determining islanding than these passive standards. The current standards require PV inverters to provide only real power to the grid. There are many researchers developing more active means of determining whether or not there is an island as opposed to the active standard shown above [17]. These new means of determining islanding are the first step to changing the standards for PV connection. Once more robust means of determining an island are available,

ancillary services that can support the grid during low voltage events can be more readily employed. These emerging ancillary requirements will now be evaluated for their impact on the inverter hardware.

2. DC-LINK CAPACITANCE REQUIREMENTS

In the IEEE 1547 standard, a distributed resource is expected to provide power at or very near a power factor of one [13]. The power factor (PF) is described in Equations (1) - (3) as the cosine of the difference between the phase angle on the voltage and the phase angle of the current of a system.

$$v(t) = V_m \cos(\omega t + \theta_v) \tag{1}$$

$$i(t) = I_m \cos(\omega t + \theta_i) \tag{2}$$

$$pf = \cos\left(\theta_v - \theta_i\right) \tag{3}$$

The grid voltage will be affected by the inverter output, but the inverter will be considered a current source. The details of this model will be explained in Chapter 4. This chapter will focus on the basic limitations of an inverter supplying reactive power in both single- and three-phase systems.

2.1 COMPLEX POWER

The notation of complex power is used to describe the phase relationship of voltage and current in terms of real and reactive power. Inductive loads will have currents that lag behind the voltage, and capacitive loads will have currents that lead the voltage. Power systems have a lagging power factor [18]. In order for real power to be consumed in a system, there must be some non-zero power-factor. As is shown above in Equation (3) the power factor can never be negative, and so it is necessary to specify whether the PF is leading or lagging. Equations (4) –

(6) below give the definitions of complex, real, and reactive power that will be used throughout the rest of this thesis.

$$S = P + jQ \tag{4}$$

$$P = VI\cos\left(\theta_v - \theta_i\right) \tag{5}$$

$$Q = VI\sin\left(\theta_v - \theta_i\right) \tag{6}$$

2.2 SINGLE-PHASE HARDWARE LIMITATION FOR REACTIVE POWER SUPPORT

A simple system configuration for a PV system is shown in Figure 1. This common configuration consists of a dc-dc converter that performs some maximum power point tracking (MPPT) and boosts the PV system voltage, and a dc link which provides filtering for the inverter stage or dc-ac conversion [19]-[22]. For single-phase inversion, there is a simple equivalency that must be true for the dc-ac conversion. Since both the current and voltage outputs are sinusoidal terms, a double frequency term and a dc power term are created. This is shown in Equations (7) and (8).

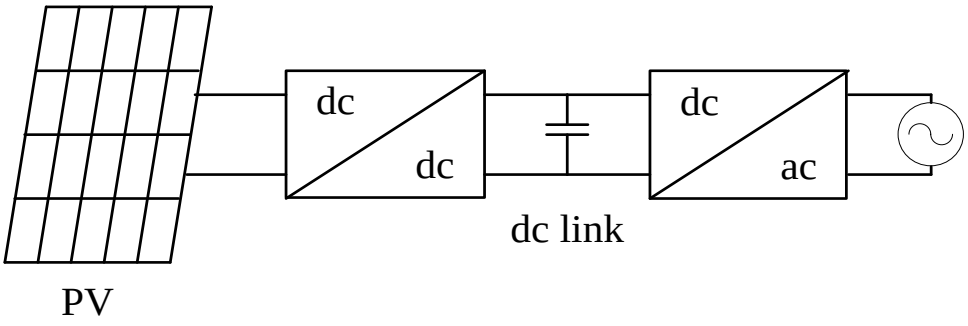

Figure 1 Topology A: basic single-phase PV system configuration

$$p(t) = v(t)i(t) = V_m I_m \cos(\omega t + \theta_v)\cos(\omega t + \theta_i) \tag{7}$$

$$p(t) = \frac{V_m I_m}{2}\left(\underbrace{\cos(\theta_v - \theta_i)}_{DC\ Term} + \underbrace{\cos(2\omega t + \theta_v + \theta_i)}_{Double\ Frequency\ Ripple} \right) \tag{8}$$

This second harmonic poses a significant dilemma for the inversion process. There must be energy storage to accommodate this double frequency term. There are several means of minimizing the necessary energy storage requirement. These solutions fall into the categories of active or passive filtering. Topology A tends to be a brute force method with a capacitor acting as a passive filter. Topology B, illustrated in Figure 2, uses an active filter design to drastically decrease the amount of capacitance needed. The details of this technique are specified in [23].

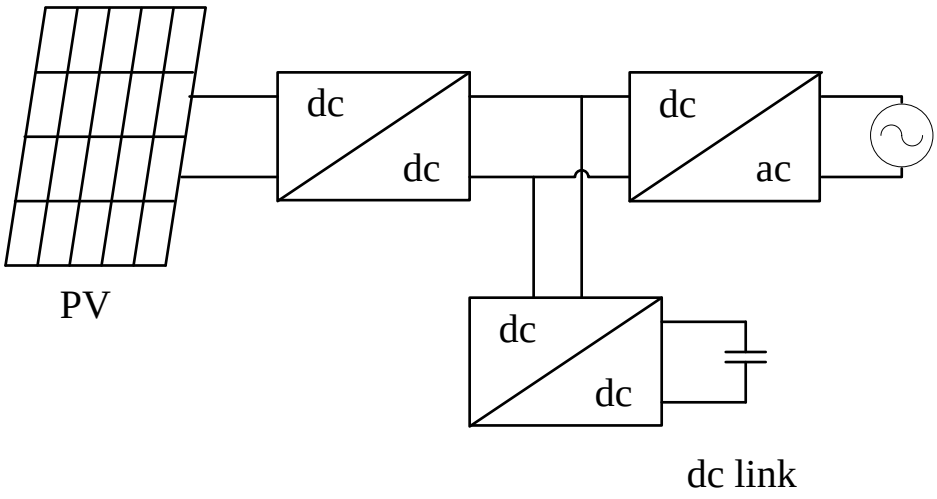

Figure 2 Topology B: single-phase PV inverter with active filter

Another unique topology, depicted in Figure 3, has the dc link connected directly to the dc terminals of the panel. In this topology there will be an oscillation around the maximum power point to supply the ripple. This decreases the efficiency of the total system since the operation point is moving continuously above and below the maximum power-producing point to supply ripple to the dc-ac conversion.

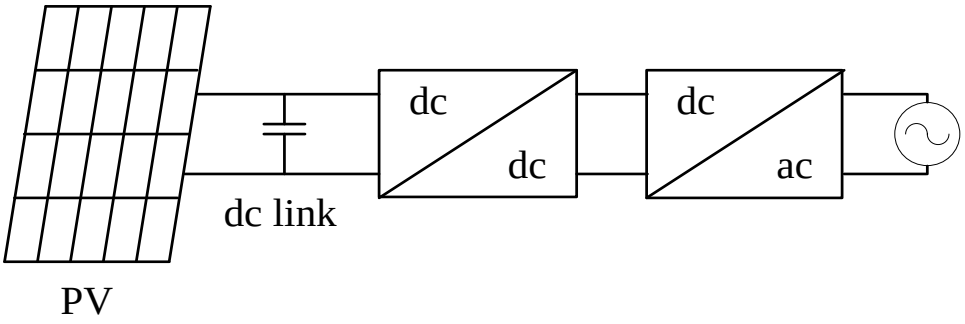

Figure 3 Topology C: single-phase inverter with panel side dc link

Topologies B and C are methods used to decrease the required capacitance. Shrinking the required capacitance reduces the energy storage cost. If the capacitance required can be decreased to the order of 10 μF, then film capacitors can be cost-effectively employed [23]. The replacement of electrolytic capacitors with film capacitors has been claimed to increase the expected operation life of the inverter by a factor of 100 [23].

2.3 Energy Storage Requirement for Topology A Inverter

The following analysis is for the single-phase inverter illustrated in Figure 1. Every inverter has a limitation on the output current and voltage that it can support. Since an inverter is connected to the grid, an ac source, the output limit will be considered an apparent power limit.

The first step is to define the amount of reactive power supplied. In many cases when reactive power support is supplied, the amount of reactive power is specified in VAr and not in a power factor. Given that PV is an intermittent source, and the effectiveness of reactive power support this low in the utility grid is dependent on the source to meet the total complex load at the output of the PV system, this analysis will be dependent on a coefficient γ to describe the portion of total apparent power used for reactive support. The relationship for this γ is shown in Equation (9) while the power-factor for this representation is derived in Equation (10).

$$S = \underbrace{(1-\gamma)^{1/2} S}_{P} + j\,\underbrace{\gamma^{1/2} S}_{Q} \tag{9}$$

$$pf(\gamma) = \frac{P}{S} = \frac{(1-\gamma)^{1/2} S}{S} = (1-\gamma)^{1/2} \tag{10}$$

Since the energy storage required is a function of the real and reactive power supplied as they affect the second harmonic, only the double frequency ripple term from Equation (8) is considered. The PV system is considered to be connected to an infinite bus and the voltage angle, θ_v, is set to zero. The definitions of real and reactive power shown in Equations (5) and (6) are combined with the ripple term of Equation (8) to give Equation (11) which governs the ripple.

$$p_{ripple}(t) = \frac{V_m I_m}{2} \cos(2\omega t + \theta_v + \theta_i) = P\cos(2\omega t + 2\theta_i) - Q\sin(2\omega t + 2\theta_i) \tag{11}$$

To get the energy storage required for the second harmonic, this p_{ripple} will be integrated over a period equal to one half of the double frequency sinusoid. For the time bounds it is important that the integral of this ripple is taken from one zero crossing to another. The appropriate integral is shown in Equation (12). In this way we ensure that the energy in Equation (13) is the maximum energy for a specified P and Q.

$$E = \int_{\frac{1}{2\omega}\left[\frac{\pi}{2}-\theta_i\right]}^{\frac{1}{2\omega}\left[\frac{3\pi}{2}-\theta_i\right]} \left[P\cos(2\omega t + 2\theta_i) - Q\sin(2\omega t + 2\theta_i)\right] dt \tag{12}$$

$$E = \frac{P}{2\omega}\left\{\sin\left(\frac{3\pi}{2} + \theta_i\right) - \sin\left(\frac{\pi}{2} + \theta_i\right)\right\} + \frac{Q}{2\omega}\left[\cos\left(\frac{3\pi}{2} + \theta_i\right) - \cos\left(\frac{\pi}{2} + \theta_i\right)\right] \tag{13}$$

As stated before, the limitations of the inverter are the current rating of the output. Figure 4 illustrates the relationship between the complex power output and the energy storage required for

an inverter. All values are per unit, and the horizontal line across the top signifies the constant output power. For this case the power factor is lagging. From this plot we can see that the energy storage is constant for a constant output apparent power. The power factor is directly proportional to the real power produced in this plot. This means that the real power production is decreasing with increased reactive power support in order to maintain current limits at the inverter output. As real power output is sacrificed for VAr production, Figure 4 gives some insight into the increased storage necessary for reactive power support.

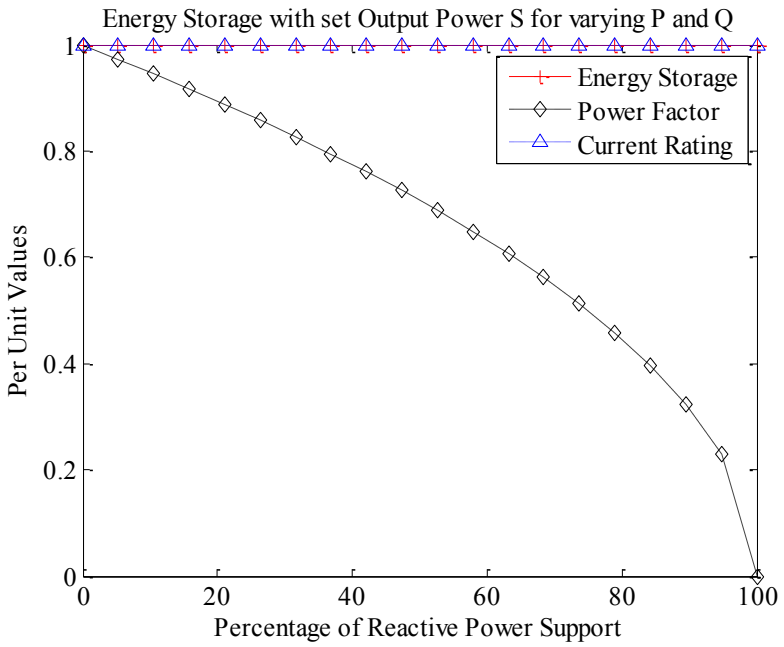

Figure 4 Energy storage for constant output apparent power

Reactive power support may not be that lucrative from the perspective of the system owner. On the residential scale, reactive power is typically not metered [24]. Although PV operates at rated power output only a small portion of the time, consistent with the power factor, this sacrifice of real power production is on the whole undesirable. Figure 5 shows the relationship between the

necessary increase in output current rating, energy storage needed, and the amount of reactive power support provided when rated real power output is constant and VAr support is increased. One more basic point to be made is that there is no difference in energy storage required when reactive power is considered with either leading or lagging power factor.

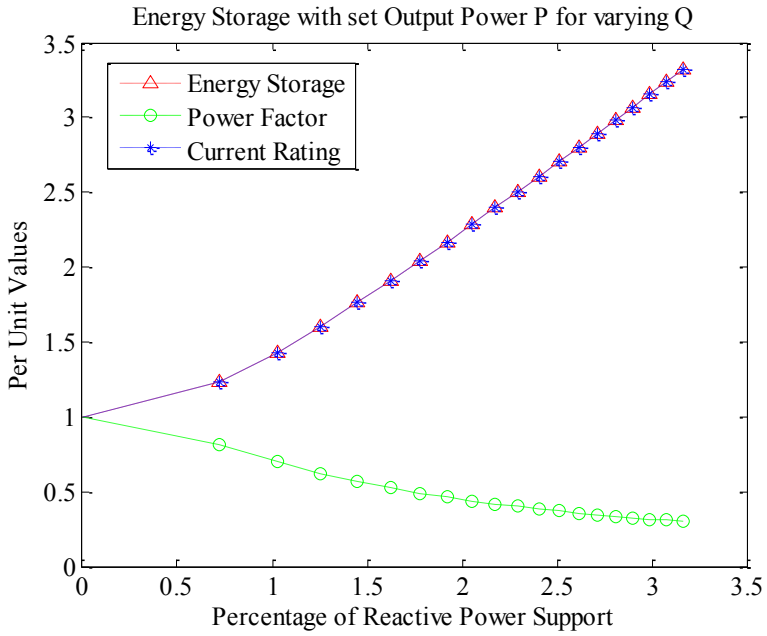

Figure 5 Energy storage for constant output real power lagging PF

These known energy storage requirements can be easily translated into a capacitance requirement. The capacitor energy is described by Equation (14). This can be equated to the energy storage requirements found in Equation (13). When this equivalency is made, the relationship in (16) for a unity power factor matches Equation (4) in [23]. $V_{1,ripple}$ corresponds to the allowed ripple at the dc source. This relationship shows that the ripple voltage and the amount of capacitance required are inversely related. This expression holds for inverters of Topology A.

$$E_{cap} = \frac{1}{2} C V^2 \tag{14}$$

$$C_A = \frac{|S_{rated}|}{2\omega \cdot V_{A,dc} V_{A,ripple}} \tag{15}$$

2.4 Energy Storage Requirement for Topology B Inverter

In the previous section the capacitance requirement to accommodate the second harmonic ripple in single phase systems was inversely related to the amount of ripple allowed. For systems that have Topology B, a common way to decrease the amount of capacitance required is to increase the ripple. Unfortunately, in this configuration the required voltage ripple from the capacitor to produce the double-frequency time-varying power term will also be applied to the panel. This causes the panel voltage to oscillate around the maximum power point, and any ripple that is seen by the capacitor will also be seen by the panel.

The required capacitance in this configuration is given by Equation (16), similar to the capacitance requirement of Topology A. Equation (17) can be generated to determine when Topology B yields less capacitance than Topology A. The limits to the amount of ripple that can be allowed at the panel require a better understanding of the general characteristics of a PV panel.

$$C_B = \frac{|S_{rated}|}{2\omega \cdot V_{panel} V_{B,ripple}} \tag{16}$$

$$\frac{V_{B,ripple}}{V_{A,ripple}} > \frac{V_{1,dc}}{V_{panel}} \tag{17}$$

Figure 6 is a generic I-V and P-V curve for a solar panel [25], [26]. The voltage at which the inverter draws current is governed by the MPP and the MPPT device [27]. This particular characteristic of PV panels is advantageous to reactive power support. In the event that there is an operating point at which the real power of the machine needs to decrease in order to achieve

the reactive power compensation desired and obey apparent output power constraints, the MPPT can simply float the voltage to decrease the real power input. However, for Topology B inverters, the increased voltage ripple means that the operating voltage will be constantly oscillating around the maximum power-producing voltage, the peak of the dotted blue trace in Figure 6. This oscillation to either side of the peak gives a mean power output that is less than the peak power output.

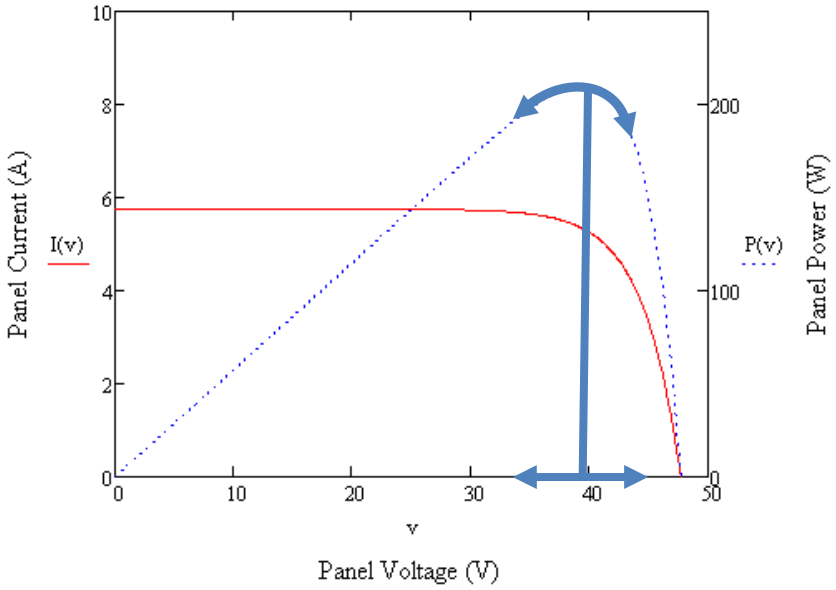

Figure 6 Photovoltaic panel I-V and P-V characteristics

Under standard test conditions (STC), the insolation on a panel is assumed to be 1000 W/m^2 and the module junction temperature 25 °C. Under these conditions the current as a function of voltage can be modeled using Equations (18) - (20) [28], which is a simplified model of the panel description derived in [29]. In these equations the MPP voltage and current are represented by V_M and I_M. The short-circuit current is I_{SC} and the open-circuit voltage is V_{oc}. The following analysis is performed for operation under STC.

$$\chi = \frac{(V_M / V_{OC}) - 1}{\ln\left[1 - (I_M / I_{SC})\right]} \tag{18}$$

$$\alpha = (1 - I_M / I_{SC}) e^{\left(\frac{-V_M}{\chi V_{OC}}\right)} \tag{19}$$

$$I(v) = I_{SC}\left[1 - \alpha\left(e^{\frac{V}{\chi V_{OC}}} - 1\right)\right] \tag{20}$$

Picking a PV module as an example [25], the effect of ripple on efficiency can be seen in Figure 7 as a function of allowed voltage ripple. The efficiency drops off very quickly after 20% voltage ripple. The inefficiency for ripple less than 20% may be acceptable in certain applications. It is clear that although ripple may be a solution to the size of the capacitance required for energy storage, the inefficiencies in this process must be taken into account.

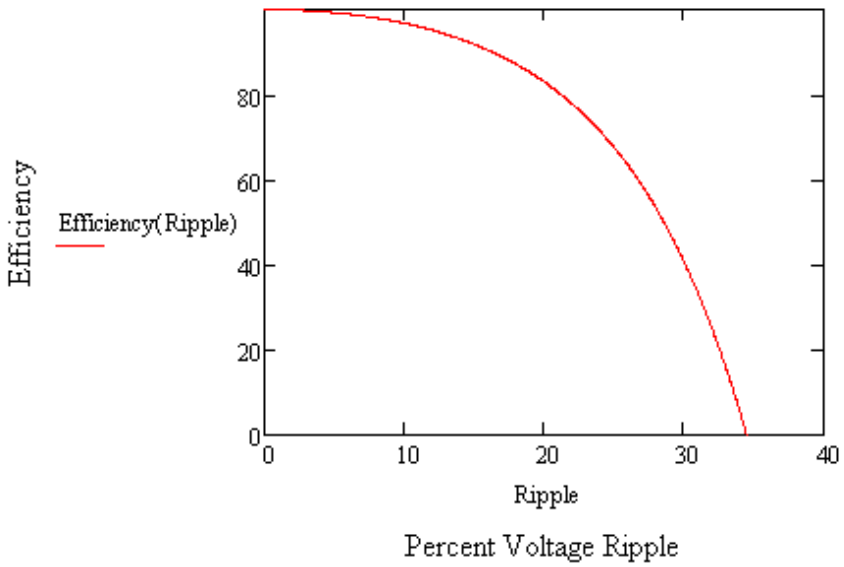

Figure 7 Power output and efficiency as a function of voltage ripple

2.5 ENERGY STORAGE REQUIREMENT FOR TOPOLOGY C INVERTER

Topology C offers an interesting benefit of an active filter. From [23] we see that the innovative idea from this topology is the switching converter in the dc link. The capacitor voltage imposed is described by Equation (21). Using the relationship between the capacitor's voltage and

current, the power is found to be a double frequency term in Equation (22).

$$v_c(t) = V_c \cos\left(\omega t + \frac{\theta_i}{2} - \frac{\pi}{4}\right) \tag{21}$$

$$p_c(t) = \frac{-V_c^2 C\omega}{2} \sin\left(2\omega t + \theta_i - \frac{\pi}{2}\right) \tag{22}$$

When Equation (22) is set equal to the ripple power found in Equation (9), the double frequency terms cancel each other and the total capacitance needed is found to be a function of the total output apparent power which includes the real and reactive power produced:

$$C_C = \frac{|S|}{\pi f V_c^2} \tag{23}$$

2.6 CAPACITANCE REQUIREMENT CASE STUDY

Now that the capacitance requirements for each of the three topologies have been derived, a simple case study will be performed for two separate PV panels. The first is a Sunpower 210 W panel [25] the second is an Evergreen 210 W panel [26]. The inverter is connected to a 240 V ac source, which correlates to a dc link voltage of approximately 340 V. In Table 3 the capacitance will be calculated for a power factor of unity, 0.75 leading, and 0.5 leading. For each configuration and each panel, power and voltage levels consistent with a micro-inverter are shown in the gray subdivision of the S_{rated}, V_{dc}, and C columns, and ratings associated with a kilowatt scale inverter are shown in the white subdivision. The system voltage for the kilowatt scale inverter was calculated from specifications in Table 1. For the Sunpower panel two strings of 10 panels in series give 400 V, and the 20 panel system provides 4,400 VA at unity power factor. For the Evergreen system 20 panels can be put in series without violating the inverter voltage input range [26]. This gives the system a voltage of 366 V. The results are shown in

Table 3 for the Sunpower panel and in Table 4 for the Evergreen panel.

Table 3 Capacitance requirements for SPR-210-BLK panel [25]

Topology	PF	S_{rated} (VA)		V_{dc} (V)		ΔV (%)	C (μF)	
(a)	1.0	210	4,400	340		±1	120	2,400
	0.75	280	5,900				160.5	3,225
	0.50	420	8,800				241	4,800
(b)	1.0	210	4,400	40	400	20	870	174
	0.75	280	5,900				1,125	232
	0.50	420	8,800				1,750	348
(c)	1.0	210	4,400	400		—	7.0	139
	0.75	280	5,900				9.3	186
	0.50	420	8,800				14	279

Table 4 Capacitance requirements for ES-A-210 panel [26]

Topology	PF	Srated (VA)		Vdc (V)		ΔV (%)	C (μF)	
(a)	1.0	210	4,400	340		±1	120	2,400
	0.75	280	5,900				160.5	3,225
	0.50	420	8,800				241	4,800
(b)	1.0	210	4,400	18.3	366	20	4,200	208
	0.75	280	5,900				5,550	277.5
	0.50	420	8,800				8,300	416
(c)	1.0	210	4,400	400		—	7.0	140
	0.75	280	5,900				9.3	186
	0.50	420	8,800				13.9	279

Table 3 and Table 4 illustrate the trade-offs in capacitor sizing between the three topologies. The two panels were chosen specifically since Sunpower manufactures a panel that has a high MPP voltage. This high voltage makes Topology B more viable on the micro-inverter scale. In the

case of the Evergreen panel, Topology B loses this advantage since there is a much lower V_M. This results in significantly higher required capacitance for the Topology B inverter in Table 4. Overall, the Topology C inverter is shown to require the least capacitance under any operating conditions with either panel. This decreased capacitance does come with the caveat of the additional components required for the dc-dc converter.

3. DC-LINK VOLTAGE CLIPPING

The previous chapter outlined three common PV inverter topologies. For the following analysis a more detailed inverter model is necessary. Figure 8 shows a circuit diagram of the Topology A inverter. The switches are assumed to be driven by some sort of pulse-width-modulated (PWM) signal to produce a sinusoidal output voltage at the inverter terminals. The inverter is connected to the grid through a small inductor, L_{OUT}. For a full-bridge single-phase PWM inverter, the amplitude of the output voltage is limited by the dc source voltage. Chapter 5 will discuss the dc voltage limitation for reliable inverter construction and operation.

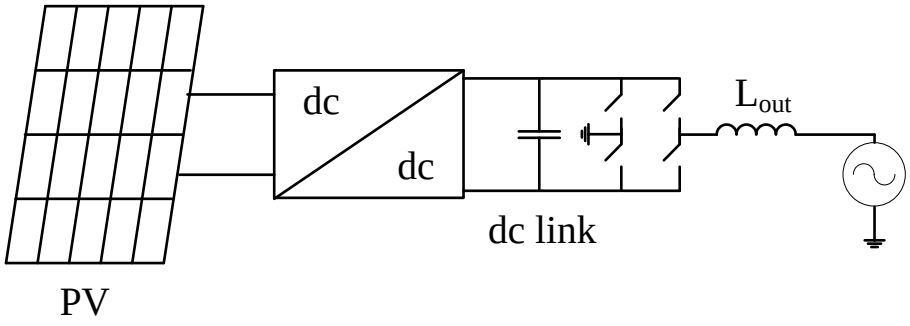

Figure 8 H-Bridge PV inverter with output filter

3.1 DC-LINK CLIPPING IN A PWM INVERTER

The dc-dc converter in Figure 8 can maintain a specific average voltage across the dc link using a boost converter and some basic feedback control. On the output side, there is a small inductor in series with the inverter as it connects to the grid. One condition was identified where, although the average voltage of the dc link was high enough to power a PWM inverter, the ripple voltage on the capacitor caused clipping between the output voltage and the dc-link voltage. This condition is illustrated in Figure 9.

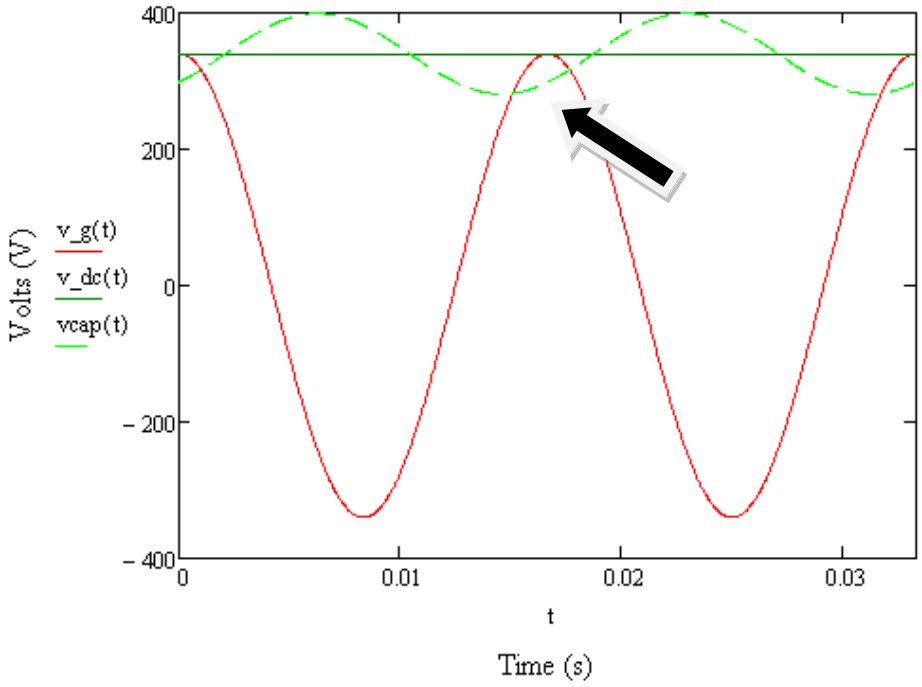

Figure 9 Capacitor voltage clipping output voltage

First, a representation of the capacitor voltage for this case must be derived. Using the voltage of the capacitor and the definition of the capacitor current as shown in Equation (24), the power output of the capacitor is found in Equation (25).

$$i_c = c\frac{dv_c}{dt} \tag{24}$$

$$p_c = v_c i_c = cv_c \frac{dv_c}{dt} \tag{25}$$

This capacitor power can now be equated to the double-frequency power ripple found in (11). Assuming that the capacitor voltage is some scaled sinusoid with a frequency equal to the grid frequency and some phase shift, the capacitor voltage can be found as a function of the operating apparent power. Equation (26) shows the capacitor voltage as a function of the apparent power, the operating frequency and the capacitance.

$$v_c(t) = \sqrt{\frac{2S}{2\pi fC}} \cos\left(\omega t + \frac{\theta_i}{2} - \frac{\pi}{4}\right) \tag{26}$$

The general expression for the voltage requirement is shown in Equation (27). The angle on the grid voltage will be taken as a reference equal to zero. The inductor voltage can be calculated as the current commanded by the inverter times the impedance of the inductor. This calculation is shown in expression (28). When representations of the time-varying terms of (27) are plugged in, the complete expression for the dc-link voltage constraint is provided in (29).

$$\langle V_{dc} \rangle + v_c(t) > v_{grid}(t) + v_{Lout}(t) \tag{27}$$

$$V_{Lout}(t) = i(t) \times jX_{Lout} = \frac{S_{out}}{|V_{grid}|} \cos(\omega t + \theta_i) \times j\omega L_{out} = \frac{S_{out}\omega L_{out}}{|V_{grid}|} \cos\left(\omega t + \theta_i + \pi/2\right) \tag{28}$$

$$\langle V_{dc} \rangle + \sqrt{\frac{2S}{2\pi fC}} \cos\left(\omega t + \frac{\theta_i}{2} - \frac{\pi}{4}\right) > \sqrt{2} V_{grid} \cos(\omega t) + \frac{S_{out}\omega L_{out}}{V_{grid}} \cos\left(\omega t + \theta_i + \pi/2\right) \tag{29}$$

Whenever this constraint is violated, there will be some clipping of the voltage output command. This will lead to an inability of the current controller to create the desired output waveform. The operation of this inverter is clearly dependent on the phase shift of the current command. From (29) the worst case scenario would be at a current phase shift of $-\pi/2$. This would put the inductor voltage in phase with the grid voltage, giving the largest magnitude to the right-hand term for clipping. This concept is illustrated in Figure 10.

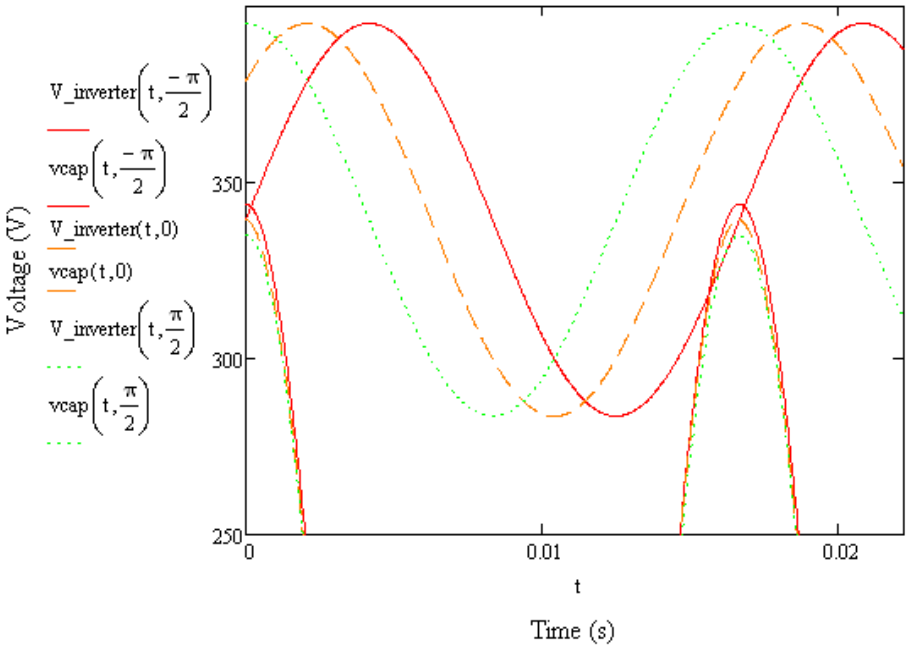

Figure 10 Dc-link clipping for various current phase shifts

The requirements for operation without clipping are fairly complex. The inverter designer has control over the size of the output filter and the dc-link capacitor, and the reference voltage for the dc link. The following is a brief exploration into each of these characteristics to see which of these parameters has the desired effect on performance.

3.2 Inductor Sizing to Avoid dc-Link Clipping

First the output inductor filter is considered. Figure 11 has three plots that show clipping conditions. Although the graphs show operating conditions for -200 to 200 VAr and 0 to 200 W, this inverter is designed to operate with a power factor as low as 0.7 and an apparent output power of over 280 VAs. The capacitance is calculated using Equation (15). The voltage ripple was assumed to be ±1% at an output voltage of 240 V rms. Using these parameters, the dc-link capacitance is found to be 936 μF. The blue portions on these graphs are output operating regions that produce clipping in the system.

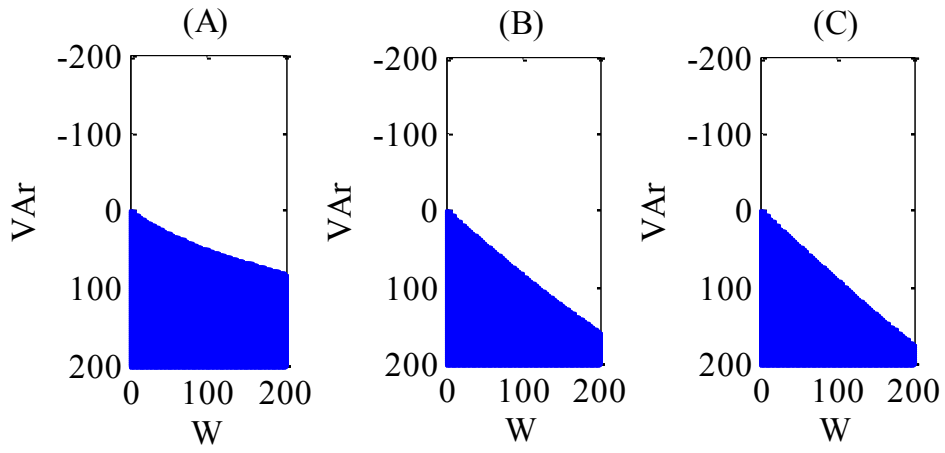

Figure 11 Clipping condition by operating point for (A) L_{out} = 0.1 H, (B) L_{out} = 0.01 H, (C) L_{out} = 0.001 H

Figure 11 proves that as the output filter inductance is decreased, the operating region increases. Inductors tend to be more costly than semiconductors and capacitors, so this is good news from a cost perspective. On the other hand, the output filter cannot be eliminated from the inverter completely as this will cause a large amount of distortion in the output current waveform. This tradeoff will be seen in the simulations of Chapter 4. It may be possible to increase the switching frequency such that a smaller inductor may be used to achieve the same amount of filtering. The last thing to keep in mind with respect to the output inductance comes from regulatory requirements for PV inverters. Many regulatory bodies require an output transformer, before the inverter output connects to the grid [13]. This small transformer provides isolation, and can act as a dc filter to make sure that there is never any dc current injection. This transformer must be rated for the full inverter current. Inherent to all transformers, this will add some inductance in series between the switches and the grid connection. From the plots it is clear that minimizing the inductance of this output transformer should be considered a significant design constraint.

3.3 CAPACITOR SIZING TO AVOID DC-LINK CLIPPING

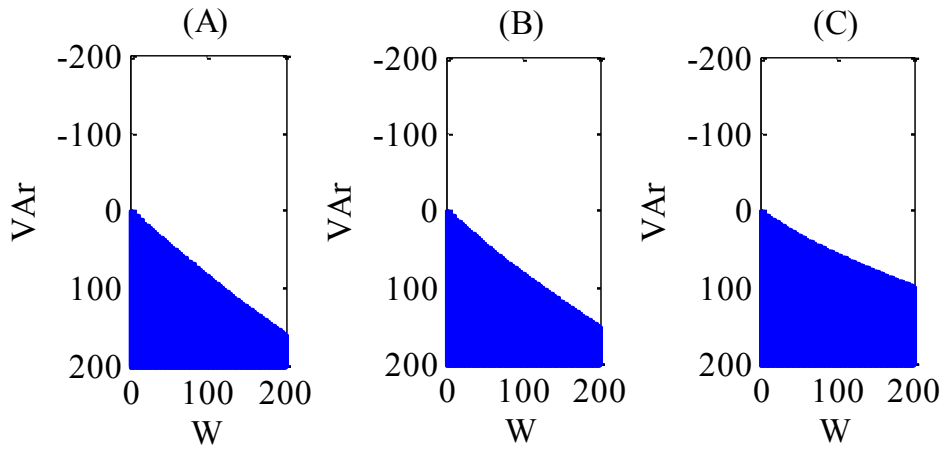

Figure 12 Clipping condition by operating point for (A) C = 1,000 µF (B) C = 5,000 µF (C) C = 100,000 µF

The next factor to be considered for the clipping constraint will be the capacitance in the dc link. From the expression in Equation 28 there is an interesting tradeoff. This capacitance is the only controllable design parameter that has a direct influence over the amplitude of the dc-link voltage ripple. It was also mentioned in the previous chapter that this capacitance is one of the major weaknesses in the expected inverter operating lifetime. Figure 12 shows the clipping conditions for the same range of operating points as Figure 11. The capacitances used for the plots in Figure 12 illustrate an interesting result. The capacitance in (A) is roughly the same as the required capacitance calculated for Figure 11. Figure 12 (B) has a capacitance value five times that of (A) and there is a slight decrease in the number of operating points that do not cause clipping. The last case of Figure 12 has an exaggerated value of capacitance, but it is meant to illustrate the trend when increasing the capacitance.

The capacitor ripple voltage amplitude is inversely proportional to the square root of the capacitance. In Figure 12 the capacitance has been increased to the extent that the waveform has flattened out, which causes more clipping than in case B. As can be seen in Figure 10, when the

current phase shift causes the inductor voltage to be in phase with the grid voltage, the peak amplitude of this combined voltage is now greater than the average dc system voltage. Since increasing the capacitance only affects the amplitude of the sinusoidal term, it is clear that very little good can be done with brute force capacitance.

3.4 Boosting the dc-Link Voltage to Avoid Clipping

The last method for reducing clipping in the inverter will be by boosting the dc link average voltage. From Equation (27) it is clear that this is the only dc term, and as such, it is the only term that could fix this issue with a sufficient boost in voltage from the dc-dc converter.

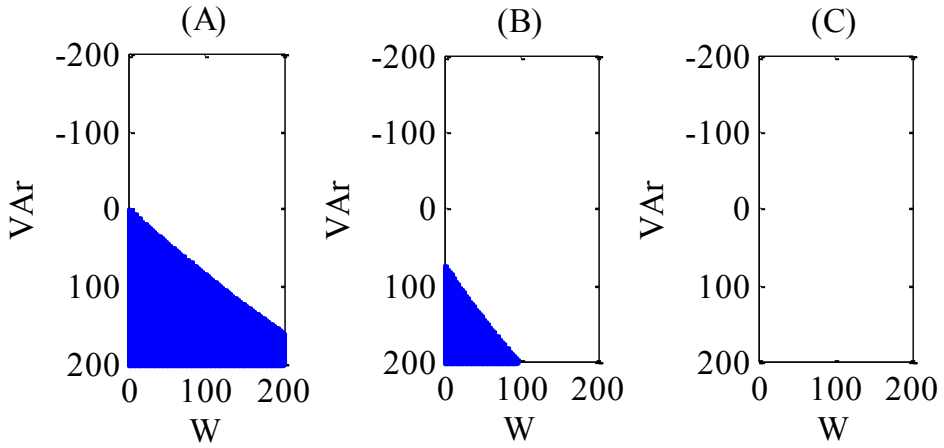

Figure 13 Clipping condition by operating point for (A)<V_{dc}> = 340 V, (B) <V_{dc}> = 355 V, (C) <V_{dc}> = 370 V

Figure 13 shows that a large enough boost from the dc-dc converter is able to eliminate all clipping in the dc link. The amount of voltage required is the real issue. There are two main concerns with this voltage increase in the dc link. The first is to make sure that all components exposed to this voltage do not require rerating. This issue will be considered in more depth in Chapter 5. The second issue is to make sure that this voltage increase does not require a topology change of the dc-dc converter.

So far the dc-dc converter has been considered a generic ideal input-output converter. In reality

this dc-dc stage is more likely a two-stage converter. The first stage will be connected directly to the panel, and will track the MPP voltage. The second will boost this voltage to the required dc link voltage. There will be some sort of control algorithm since the switching converter will have to take into account the dropping input voltage as well as the changing requirements in output voltage as a function of the amount of reactive power that is being supplied to the grid.

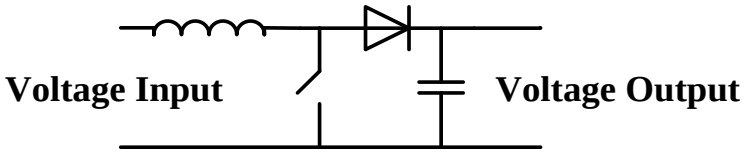

Figure 14 Boost converter

A boost converter is the topology that would most likely be used [19]. The configuration for an ideal boost converter is given in Figure 14. From this figure we can derive the relationship between the converter input and output voltages. Equation (30) describes the output voltage as a function of the input voltage and a duty cycle D. The duty cycle describes the portion of the switching period during which the switch is closed. A case study for the required duty cycle of a boost converter for both PV panels is shown in Table 5.

$$V_{out} = V_{in} \frac{1}{1-D} \tag{30}$$

Table 5 Second stage dc-dc converter boost requirements

Panel	**MPP Voltage**	**V_{in}/V_{out} w/o Reactive Support**	**Duty Cycle w/o Reactive Support**	**V_{in}/V_{out} w/o Reactive Support**	**Duty Cycle w/o Reactive Support**
ESA 210	18.3	9.3	0.8925	10.9	0.9083
SPR 210	40	4.25	0.7647	5	0.8

For an inverter supplying power to the grid, it was stated that in the residential split-phase system

of the United States, the grid voltage is 240 V rms. For a full bridge inverter this corresponds to a requirement of 340 V dc. For a micro-inverter topology, there is no doubt that some magnetics would be required in the dc-dc converter in order to achieve this required bus voltage. For a larger single-phase inverter, this might not be a problem. For larger multi-panel systems, the voltage input to the inverter may approach 450 V. In such a case there would be less need for magnetics in the dc-dc stage. However, the panel voltage dependence on temperature produces some variance that needs to be accounted for. To verify these results a model will now be developed in Simulink.

4. INVERTER MODEL AND SIMULATIONS

A model will be developed in Simulink to evaluate the performance of the design constraints developed so far and verify theoretical limits. This model will not take into account many component non-idealities, but will instead focus on the impact of reactive power support on the dc link as well as the grid output waveform. This will give insight into the voltage, current, and power requirements for these components.

4.1 PV MODEL

PV panels are typically modeled by a current source that is a function of incident solar radiation (insolation). In the models that follow a dc current source supplies the inverter. The dc supply is assumed to be a current source that follows a typical PV panel I-V curve. Figure 6 depicts the generic shape of a P-V, I-V. This curve is very important to inverter operation limits.

4.2 INVERTER MODEL

Inverter topology for these simulations is similar to the output stage in Figure 8. The Simulink model (Figure 15) has an H-bridge with an output inductor connected to an ideal ac voltage source representing the grid, as well as a capacitor to represent the dc link. The PV source is a controlled current source with a commanded dc current that can be defined as a function of insolation. In this simulation the current is given a constant 1 A dc command. The capacitor in the dc link is initialized with a voltage but manipulated by the inverter output. This will be explained in the Section 4.3 where the control for the gating signals G1 and G2 is discussed.

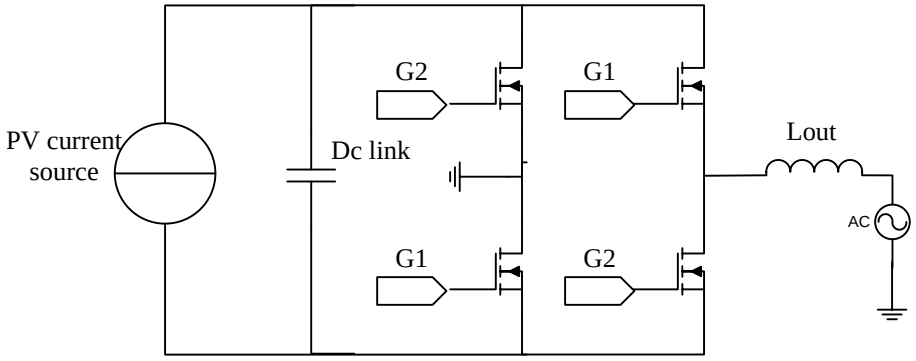

Figure 15 Inverter model in Simulink

4.3 SWITCHING CONTROL

Inverter switching control is performed using a hysteresis modulation method. This method, commonly applied to motor drives, generates switching commands for a dc-ac conversion. The hysteresis control compares the current sensed at the inverter output to a reference current waveform. The reference current is given an offset, δ, to define an upper and lower bound. The comparison of the actual current waveform to these bounds is what causes the switching action of gating signals G1 and G2. The comparisons performed are shown in Equation (31) where a 1 indicates a switch being closed. Figure 16 depicts this switching method's state diagram.

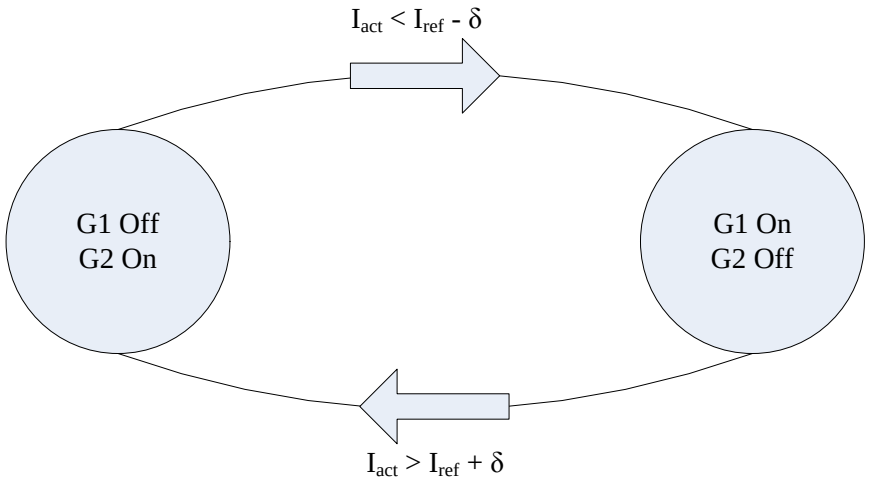

Figure 16 Hysteresis control state transition diagram

$$\begin{aligned} I_{act} < I_{ref} - \delta \quad & \begin{cases} G_1 = 1 \\ G_2 = 0 \end{cases} \\ I_{act} > I_{ref} + \delta \quad & \begin{cases} G_1 = 0 \\ G_2 = 1 \end{cases} \end{aligned} \tag{31}$$

Figure 17 illustrates a portion of the generated current waveform. It is intuitive that the waveform will bounce between the lower and upper limits. This is a common form of current control for an inverter [19], [30].

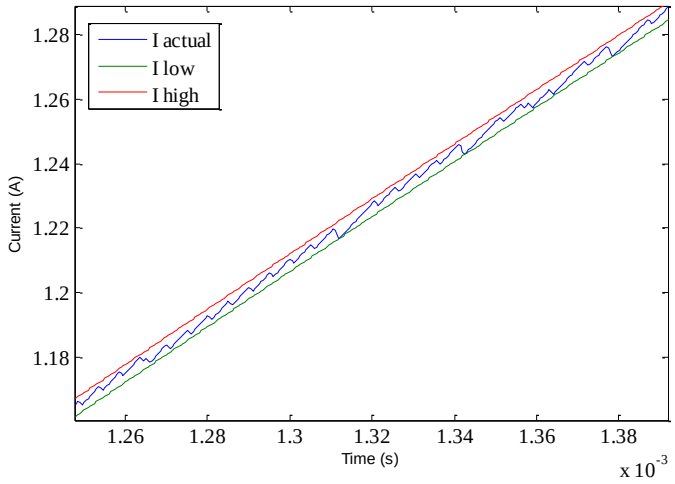

Figure 17 Hysteresis current control waveforms

A major weakness of hysteresis current control is the fact that there is no defined switching frequency [30]. This inverter will use MOSFETs which have acceptable performance above the 100 kHz range [31]. Alternatively the switching frequency can be affected by the upper and lower bound magnitude. If the boundaries are expanded, then the inverter will have to switch less often to meet the boundary conditions. An important side note with regard to switching frequency has to do with modeling this system. A Simulink model was created in the discrete time domain. For a fixed-step size solver, this discrete simulation places a constraint on the switching frequency. Thus, the solver used for the following simulations is a variable step trapezoidal solver.

The controller reference current is shown in Equation (33). This equation shows that the free variables for the reference will be the phase shift and the current magnitude. In experimental inverters a phase-locked loop, or zero detection scheme, would have to be employed [32]. This would ensure that the grid voltage phase was detected, and that the current phase was shifted appropriately. Synchronization between the voltage angle and current angle has been achieved by using the simulation time as a reference and starting the grid voltage with a zero phase shift.

$$i_{ref}(t) = I_m \cos(\omega t + \theta_i) \tag{32}$$

The only user-defined input that the inverter needs for this model is a value of reactive power, *Q*. When the grid voltage is taken as a reference equal to zero, Equation (33) defines θ_i.

$$\theta_i = \cos^{-1}\left(P/S\right) = \cos^{-1}\left(P/\sqrt{P^2+Q^2}\right) \tag{33}$$

Finding the required magnitude for the commanded current reference is significantly more difficult. In Section 4.1 the PV source was defined as a dc current source. In parallel with this current source is a capacitor representing the dc link. There are two scenarios to consider. In the first, the inverter passes no current to the grid. Here, the dc current source would feed into the capacitor. The relationship for a capacitor voltage to current has been defined in Equation (24). From this expression it is clear that for a constant positive dc current into the capacitor, the voltage would ramp to infinity, or at least until it destroyed the capacitor. On the other hand, if too much power is transferred from the dc side to the ac inverter terminals, eventually the dc-link voltage would sink below the requirement of Equation (27). At this point there would be significant clipping and the current output waveform would begin to inject harmonics into the grid. What follows is a method developed to command a current magnitude in such a way as to regulate the dc bus voltage to a reference value.

The control method subtracts the voltage on the capacitor from some reference voltage to calculate the error. This error is put through a proportional integral (PI) controller to produce a command for current magnitude. The current magnitude is then used to produce the hysteresis controller reference current. Figure 18 illustrates the basic PI controller.

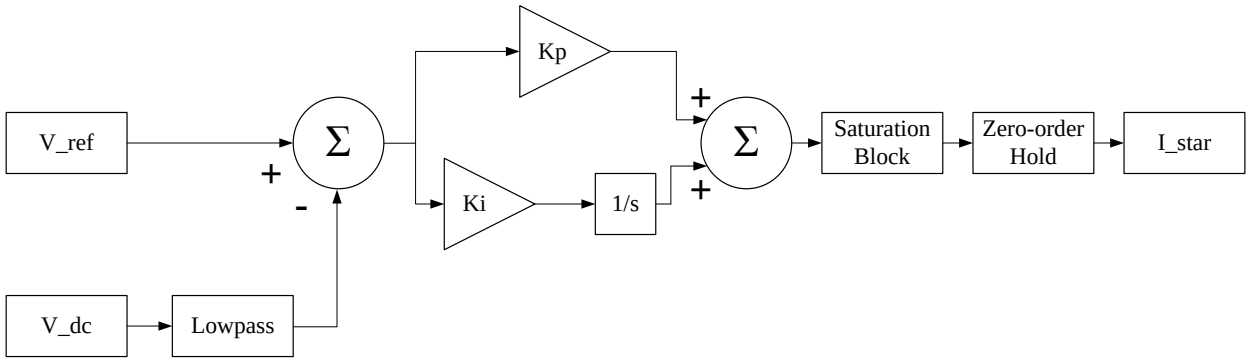

Figure 18 PI controller for dc-link voltage regulation

The double frequency ripple in the dc link is a recurring concept for single-phase inverters. To attenuate the ripple and speed up the controller, a low pass filter was placed on the measured dc voltage. When picking the cutoff frequency a balance must be kept between the amount of attenuation that the low pass filter is able to provide, and the speed at which the controller can operate. The cutoff frequency could be placed very low; 12 Hz was used in one case. Although this attenuated the ripple, it slowed the controller's ability to track the error. In the final simulation, the cutoff frequency was set to 60 Hz. Controller gains for this case were set to K_p = -0.1 for the proportional gain and K_I = -4 for the integral gain.

A saturation block, the second to last step before the output of I_star, ensures that there will be no current into the dc portion of the inverter if the reference voltage is above the dc-link voltage. In such a case the current command will go to zero and the capacitor will be charged with the dc current source representing the dc-dc converter output.

A zero-order hold is the last controller block. It ensures that no capacitor voltage ripple is passed to the current magnitude command. This is accomplished by holding the current command constant for one cycle. After 16.67 ms the magnitude is changed to the controller's new current command. In practice updating the current commanded would require some detection of the zero crossings [32]. Synchronization is accomplished by initializing the current in phase with the voltage.

This controller regulates the dc power from the panel to the grid. As was shown in Equation (8), the dc term corresponds to the real power produced. Some input from the reactive power requirements must be added to the reference current to produce the overall current command. The expression for the final reference current magnitude as a function of the controller current *I_star* and the reactive power commanded *Q*, is shown in Equation (34). This new reference current is for the apparent power output while *I_star* is for the real power. From these two currents the phase shift for the hysteresis control can be calculated in Equation (35).

$$\left|I_{ref}\right| = \frac{1}{\left|V_{grid}\right|}\sqrt{\left(\left|I_{star}\right|\left|V_{grid}\right|\right)^2 + \left|Q\right|^2} \tag{34}$$

$$\theta_i = \cos^{-1}\left(\frac{\left|I_{star}\right|\left|V_{grid}\right|}{\sqrt{\left(\left|I_{star}\right|\left|V_{grid}\right|\right)^2 + \left|Q\right|^2}}\right) \tag{35}$$

4.4 INVERTER PERFORMANCE

The first challenge for this inverter was tuning the PI controller so that the current magnitude commanded would come to steady state in a reasonable amount of time. Figure 19 shows the grid voltage, the output current, and the dc-link voltage. The controller operates as was described

in Section 4.3. This plot illustrates the oscillations in the output current magnitude, and the delayed relationship between the controller and the dc-link voltage.

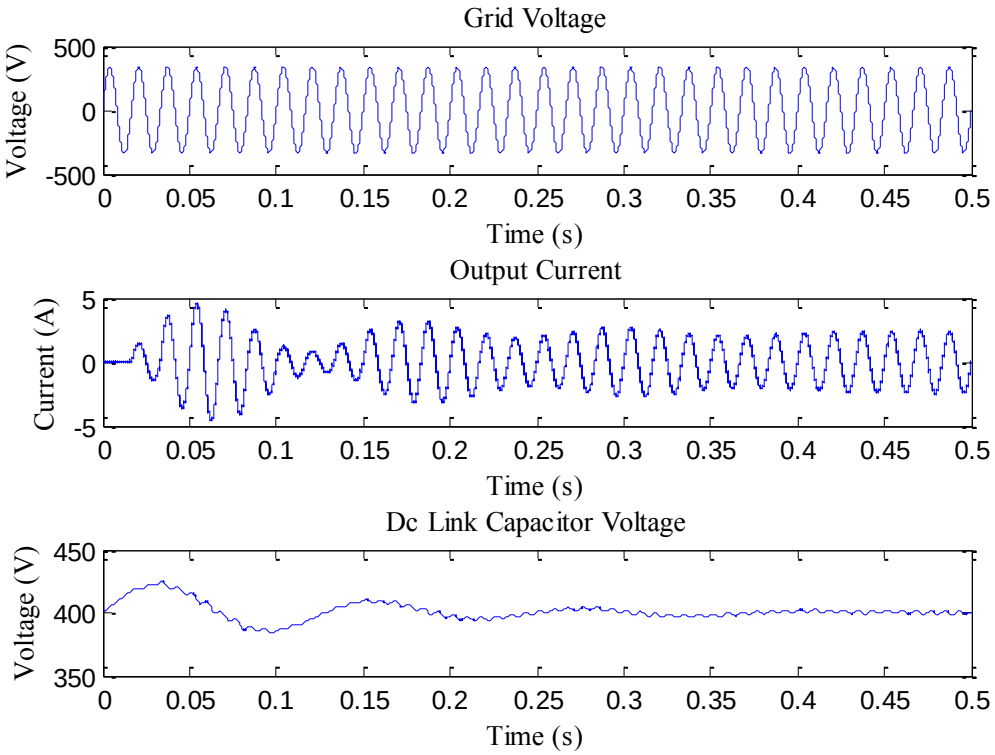

Figure 19 Current command control for single-phase inverter

The reference voltage for the dc link in this simulation was 400 V. This voltage allows oscillations in the controller without affecting the output waveform. As the dc-link voltage ramps up in the first 50 ms, the controller increases the current magnitude and power output to decrease capacitor voltage. The inverse relationship is evident in the next 100 ms. This controller comes to steady state, but is very slow due to the zero-order hold and low pass filter. The overall controller performance is successful. The dc-link voltage does not exceed ±30 V, which is an error of less than 7.5 %. Because the zero-order hold has been placed on the controller, there are no concerns of harmonics due to a varying current command. For the following simulations and

comparisons, all plots and data were taken at steady-state operation which can be seen in the last 50 to 100 ms of Figure 19.

The next issue to be addressed is the effect of a reactive power command on system operation. In prior sections, there has been discussion of the effects of reactive power production on the dc link and inverter operation. From Figure 20 there are no serious transients that need to be taken into account from a sudden reactive power command. This was expected since reactive power commands are not figured into the controller. Instead the additional magnitude and phase shift of reactive power support are performed algebraically after the controller as described in Equations (34) and (35). From the plot it appears that the magnitude of the dc-link voltage spikes considerably when the reactive power command is given; this is actually a shift in the dc-link voltage. It will be shown in the next plot that for VAr production the voltage ripple on the dc link will increase in magnitude. One last observation is the flatline of the dc-link voltage for the first 2.5 ms; this is due to an averaging tool that was used to clean up the voltage measurement so the non-ideal switching transients were not captured in the waveform.

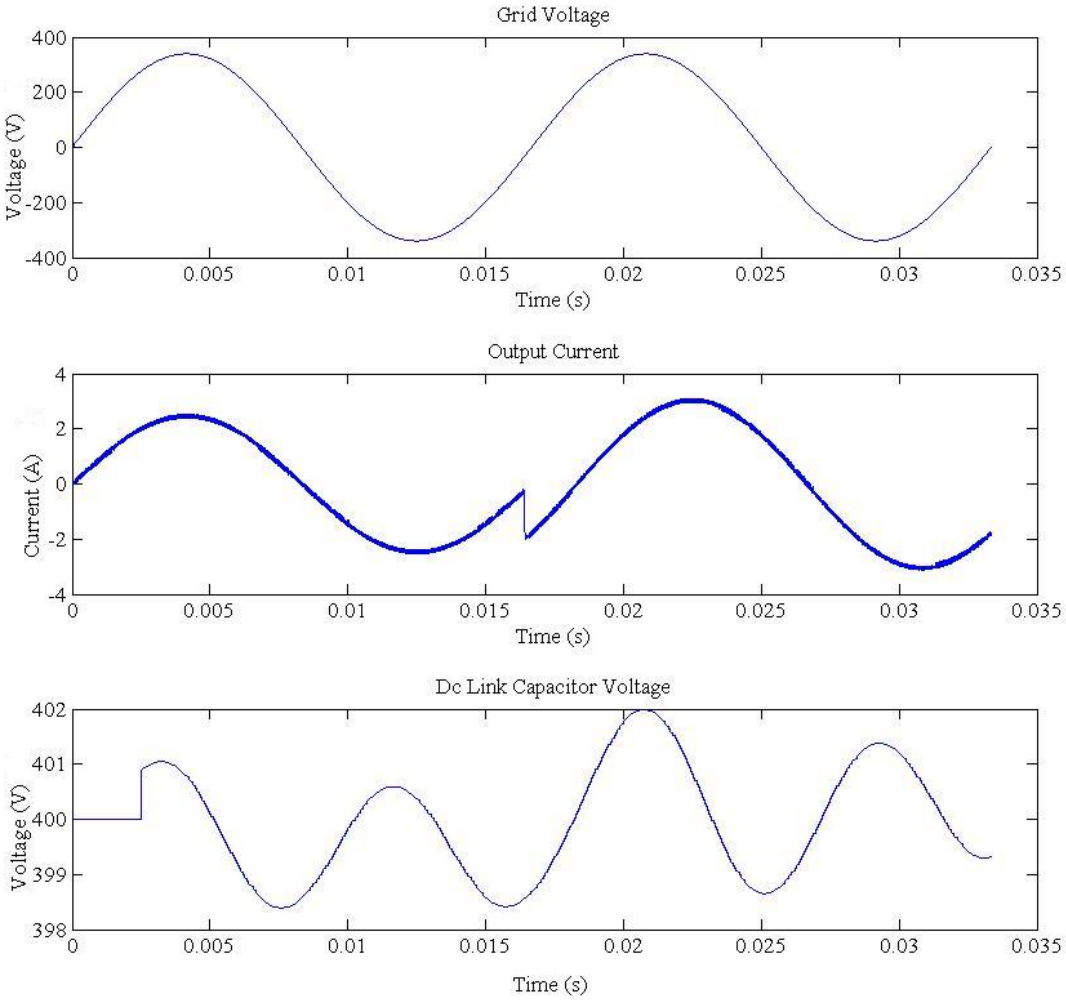

Figure 20 Reactive power support for single-phase inverter Q = 0 VAr to Q = 250 VAr

Figure 21 illustrates the effects of reactive power support on the dc-link. Reactive power commands are stepped from -400 VAr to 400 VAr in 200 VAr increments. The plot shows a trend of increasing the magnitude of the dc link voltage ripple. The relationship between the voltage ripple magnitude and the reactive power produced is subdued. The real power produced in this simulation was around 400 W, so the limits of reactive power production have not been

approached. Notwithstanding, a power factor of about 0.7 has been achieved without serious dc link complications.

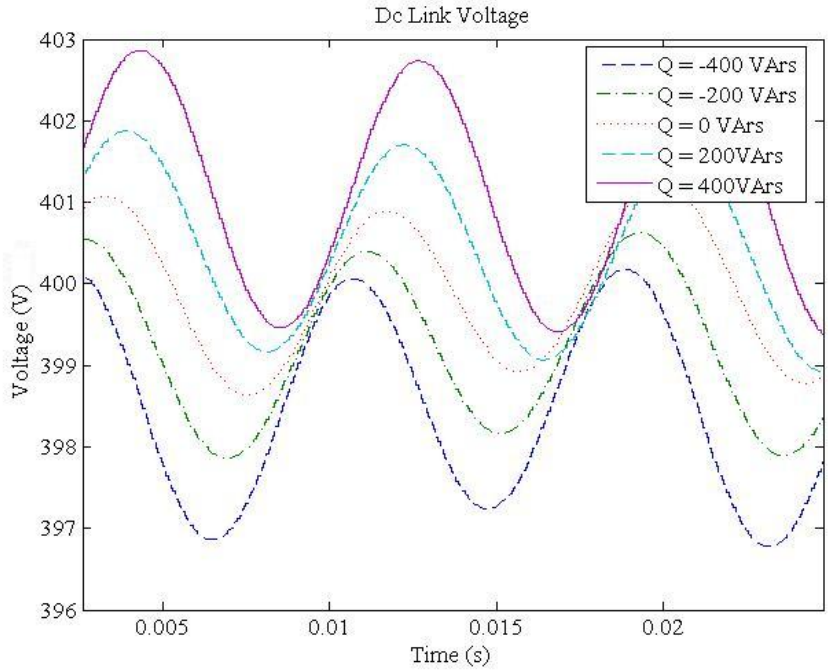

Figure 21 Dc-link voltage for reactive power support of -400, -200, 0, 200, 400 VAr

In the Chapter 3 voltage clipping was avoided by decreasing the output filter inductance. Figure 22 illustrates the effects of changing this inductance. The first plot has little inductance and shows the dilemma of using too small a filter to eliminate the switching transients in the output current waveform. When this inductance is increased tenfold, the waveform is cleaned up considerably, as shown in the middle plot. However, there is some limit to the amount of inductance that can be added to the output filter before clipping. The last plot shows the output current waveform when the filter has an inductance of 100 mH. This clearly causes some clipping in the system, and after the capacitor charge decreases there is a major non-ideality in

the output waveform at around 30 ms. The harmonics in this waveform violate the output waveform standards, so this inductance is not viable unless the dc input voltage is boosted.

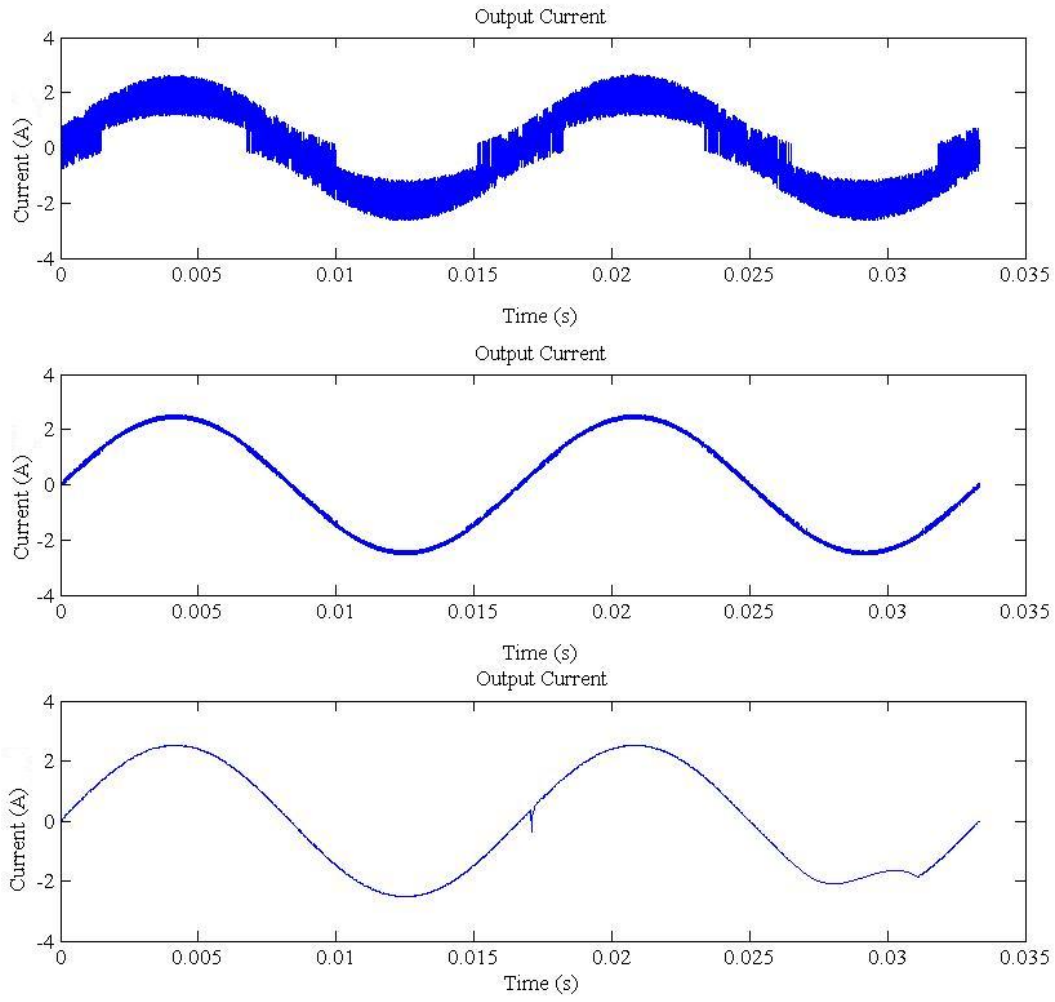

Figure 22 Current output waveform for inductor sizing of 1 mH, 10 mH, and 100 mH

The last simulation was to verify the relationship between capacitance and the double frequency ripple magnitude found in Chapter 2. In Figure 23 the dc-link voltage waveform is plotted for varying capacitance values. The relationship established in Chapter 2 holds, and the ac voltage magnitude decreases with increased capacitance. The clipping concerns of Chapter 3 have been eliminated in this case as the dc voltage of the dc link has been set to a sufficiently high

reference of 400 V. One of the benefits of the slow controller is that these oscillations will not cause a cycle-by-cycle oscillation in the current waveform output. This last simulation and the preceding ones verify that this inverter model behaves as expected and that the theoretical derivations are accurate. Next, a reliability study will be performed using these operating limits.

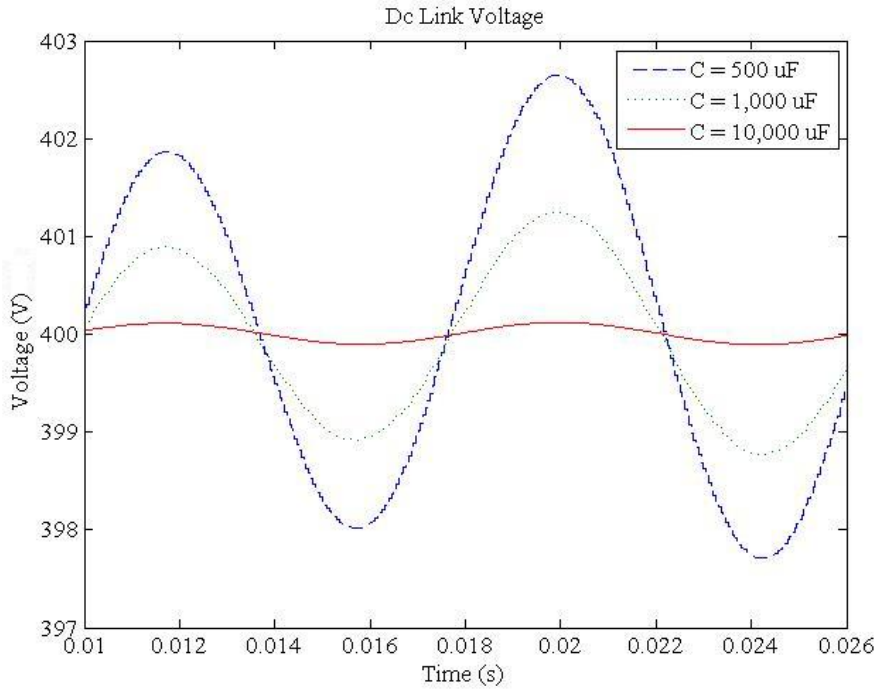

Figure 23 Dc-link voltage for capacitance values of 500 µF, 1,0000 µF, and 10,000 µF

5. COMPONENT RELIABILITY, COST AND PERFORMANCE

Throughout Chapters 2 and 3 the hardware constraints of supplying reactive power from a single phase inverter were determined. In Chapter 4 these constraints were tested using a Simulink model. Now these component constraints and operating conditions will be checked for reliability concerns and increased inverter cost. First, criteria will be developed for each component based on the military handbook *Reliability Prediction of Electronic Equipment* [33]. The cost of these components will also be explored in this section. The latter portion of this chapter will focus on case studies for various power levels and reactive power support capabilities.

5.1 MOSFETs

The predicted reliability of MOSFETs is calculated as a product of stress parameters with a base device failure rate. The expression in Equation (36) yields a number of failures per million hours of operation. The variables in this equation are λ_b the base failure rate for MOSFETs, π_A the application factor, π_Q the quality factor, π_E the environment factor, and π_T the thermal stress.

$$\lambda_p = \lambda_b \pi_A \pi_Q \pi_E \pi_T \tag{36}$$

Whether or not an inverter is supplying reactive power, the first three factors for the failure rate calculation will not change. The last stress factor, temperature, will have a large impact on the overall inverter reliability. This factor is a function of the device junction temperature as shown in Equation (37). The junction temperature is a function of the dissipated power. Equation (38) defines this relationship. The dissipated power is the resistive losses of R_{DS} and the current passed through the MOSFET. When this information is substituted into the original expression for the temperature stress factor, Equation (39) is created, where I is the current and R_{DS} is the 'on' resistance of the MOSFET. This current is dependent on the inverter apparent power rating.

With decreased power-factor operation, an increase in the total output current is expected. This will in turn increase the failure rate.

$$\pi_T = \exp\left(-2483\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right) \tag{37}$$

$$T_J = T_C + \theta_{JC} P \tag{38}$$

$$\pi_T = \exp\left(-2483\left(\frac{1}{T_C + \theta_{JC}(I^2 R_{DS}) + 273} - \frac{1}{298}\right)\right) \tag{39}$$

5.2 OUTPUT INDUCTOR

The output inductor acts as a filter, and was shown in Section 3.2 to affect the potential operating region. The higher the switching frequency that is used, the smaller the inductance required to effectively filter harmonics in the output current waveform. In reliability examples in [33], inductors are disregarded completely and are said to have a negligible contribution to the failure rate [34], [35]. Thus, in the case studies that follow, the inductor has been disregarded.

5.3 DC-LINK CAPACITOR

Two types of capacitors will be considered for the dc link. For large capacitance values on the order of hundreds or thousands of microfarads, electrolytic capacitors will have to be employed. These tend to be cheaper, and are common when large capacitance values are required. For this application, the electrolytic capacitors used will be aluminum. Equation (40) defines the capacitor reliability. This equation has similar stress parameters to the MOSFET failure rate equation. Aluminum electrolytic capacitors have a stress factor associated with their quality, π_Q, and the environment, π_E. The π_{CV} stress factor is a function of the amount of capacitance, as shown in Equation (41). The base failure rate λ_b takes into account the ambient temperature for

the device, the amount of ac and dc voltage applied, and the device voltage rating. Equation (42) gives the expression for the base failure rate with its dependence on the ambient temperature, T, the dc voltage applied, V_{DC}, the ac voltage applied, V_{AC}, and the device voltage rating, V_{Rated}.

$$\lambda_p = \lambda_b \pi_{CV} \pi_Q \pi_E \tag{40}$$

$$\pi_{CV} = .32C^{0.19} \tag{41}$$

$$\lambda_b = .0028\left[\left(\frac{V_{AC}+V_{DC}}{.55V_{Rated}}\right)^3 + 1\right]\exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right) \tag{42}$$

In Chapter 2, capacitance requirements for the double frequency ripple were calculated. These calculations were performed for a micro-inverter and a kilowatt scale inverter. From Table 3 and Table 4, the capacitance requirement of Topology C at the micro-inverter scale allows the use of film capacitors. Although these capacitors are significantly more expensive than electrolytic capacitors, [19] argues that the increase in reliability would be well worth the added cost. The difference in the failure equations is present in the base failure rate calculation. Equation (44) is the base failure rate for film capacitors. This equation shows a failure rate that is more dependent on the voltage applied, but has a coefficient that is more than a factor of five lower than the electrolytic capacitor failure rate. The stress factor for capacitance, π_{CV}, has also changed. Equation (44) shows this relationship.

$$\lambda_b = .0005\left[\left(\frac{V_{AC}+V_{DC}}{.4V_{Rated}}\right)^5 + 1\right]\exp\left(2.5\left(\frac{T+273}{358}\right)^{18}\right) \tag{43}$$

$$\pi_{CV} = 1.3C^{0.077} \tag{44}$$

5.4 RELIABILITY CASE STUDIES

Now that the reliability expressions have been outlined, they will first be applied to Table 3 capacitance requirements. The equations in the previous sections show a dependence on the capacitor rating with respect to the operating voltage, and the operating temperature with respect to the temperature rating. For the following case study all of the capacitor voltage ratings will be 125% of the operational voltage. The operating ambient temperature will be at 45 °C, with 85 °C temperature ratings. The capacitor characteristics are from Digikey, a well known supplier of electrical devices. All the components listed below are commercially available. The prices associated with each of these capacitors are listed in Tables 6 and 7. Price trends are fairly consistent for a specific applied voltage and capacitance value. Irregularities in price within a specific group may be due to the fact that not all of these components are produced in mass quantities. Appendix B has the exact product number for each of these components as is found on the Digikey web site.

Table 6 Capacitor failure rate case study

Topology	PF	Part Number (Appendix B)	Micro-inverter			Kilowatt Inverter		
			C (μF)	Cost ($)	λ_{CAP}	C (μF)	Cost ($)	λ_{CAP}
(a)	1.0	1 / 2	120	3.46	0.012	2,400	92.25	0.02
	0.75	3 / 4	160.5	4.20	0.014	3,225	110.58	0.024
	0.50	5 / 6	241	5.02	0.016	4,800	179.24	0.036
(b)	1.0	7 / 8	870	1.20	0.017	174	3.67	0.012
	0.75	9 / 10	1,125	1.52	0.018	232	5.02	0.016
	0.50	11 / 12	1,750	1.78	0.019	348	6.46	0.022
(c)	1.0	13 / 14	7.0	10.87	0.023	139	3.36	0.012
	0.75	15 / 16	9.3	13.80	0.024	186	3.94	0.013
	0.50	17 / 18	14	14.60	0.024	279	5.4	0.014

The results of this case study provide little insight into how to extend the inverter's expected life. This is in part because the analysis was performed for the same capacitor voltage. Had this study been performed with a standard capacitor voltage rating of 400 V there would be a decrease in the failure rate for the Topology B micro-inverter. This would be due to the new capacitor rating of 1000% operational voltage. In this particular case, the new capacitor rating would reduce the failure rate by a factor of 4.

From Table 6 it is clear that reactive power support from inverters does not have a large effect on the failure rate. As the capacitance values tend to at least double from unity power-factor operation to 0.5 power factor, the main impact of reactive power support can be seen in the cost. The Topology A capacitance cost is quite large for the kilowatt inverter. However, the micro-inverter for Topology A has relatively constant capacitance costs regardless of the power-factor.

Table 7 MOSFET failure rate case study

PF	Current Rating (% Operational Current)	Part Number (Appendix C)	Micro-inverter			Kilowatt Inverter		
			I_D / R_D	Cost ($)	λ_{MOSFET}	I_D / R_D	Cost ($)	λ_{MOSFET}
1.0	100	1 / 2	1.25/6.5	0.32	2.488	29.5/.120	8.95	46.524
	200	3 / 4	2.50/3.4	0.30	1.724	59.0/.055	19.8	14.544
0.75	100	5 / -	1.65/3.6	0.6	2.426	-	-	-
	200	6 / -	3.30/1.8	0.41	1.667	-	-	-
0.50	100	7 / -	2.50/3.4	0.30	4.922	-	-	-
	200	8 / -	5.00/1.0	0.63	1.858	-	-	-

So far it has been difficult to see the advantage of the Topology C micro-inverter. Even in the reliability case study in Table 6, there is no evidence that this more elaborate dc-link will decrease the failure rate. The real value in these capacitors is their incredibly high voltage

ratings. A 7 μF film capacitor rated at 1000 V is only $7. From Equation (43) we can see that the increased rating for film capacitors has a larger effect on the failure rate than for electrolytic capacitors [Equation (42)]. Electrolytic capacitor solutions also have a well defined voltage limit. Major manufacturers do not even offer electrolytic capacitors that are rated over 550 V. Voltage overrating is not novel, and since there are no conclusions to be drawn about the limiting effect of reactive power support on capacitor reliability, MOSFETs will now be analyzed.

Table 7 contains the failure rate study for the MOSFETs based on power factor. As all of the MOSFETs will be exposed to the same voltage, the difference will be the current that passes through them. This case study takes into account three different power factors and two current ratings for each, one at 100% of operating current, and a second at 200%. In practice MOSFETs can be paralleled to decrease the resistance through the device while performing with the same switching capability. Thus, only one case of the kilowatt inverter was considered, as the higher power MOSFETs required at non-unity power-factor operation would likely be replaced by several smaller MOSFETs in parallel. Again all of the MOSFETs considered in this table are readily available parts from the Digikey web site. Price jumps such as the difference in cost between MOSFET numbers 3, 5, and 7 are largely due to the fact that some of these MOSFET ratings are in between the characteristics of more common mass-produced MOSFETs. For a table with the detailed part number and description of each MOSFET as it appears in the Digikey catalog, see Appendix C. Table 7 gives some very interesting overall results. The first point is that the number of failures per million hours of operation is significantly higher for MOSFETs than capacitors. Comparison of the values in Table 6 and 7 show two orders of magnitude between these devices' predicted failure rates. From Equations (40)–(42), the MOSFET failure rate is a function of the output current magnitude, which is power factor dependent. This means

that MOSFET reliability is most directly affected by reactive power support, and that the MOSFET is the most likely device to fail.

Even though the MOSFET is the weak link in the inverter, the trends from overrating this device show promise in decreasing the failure rate. From unity to 0.5 power-factor operation, the current doubles, but by overrating the device, the number of failures remains constant. The same effect can be achieved for a MOSFET when two MOSFETs of the same rating are paralleled. In both cases the total power dissipated will be the same, and thus the reliability will be unchanged. There are limits to this effect. From Equation (40) there is still some component of the failure rate that is not dependent on the dissipated power. In the case of an ideal MOSFET with $R_D = 0$, the failure rate for the ambient conditions is on the order of one failure per million operating hours. The MOSFETs limit inverter reliability, but increased power dissipation due to reactive power support can be managed by decreasing the series resistance, either with an overrated device, or multiple paralleled MOSFETs.

6. CONCLUSIONS

Reactive power support from single-phase photovoltaic inverters is one of many emerging ancillary services provided by distributed generation [8]-[10]. Various design constraints have been outlined in previous chapters, including the impact of reactive power production on reliability. In the end there still needs to be some financial benefit for this additional operating feature.

The operating constraints for reactive power support were considered for three of many inverter topologies. It has been found that capacitor sizing to accommodate the double frequency ripple on the dc link has been a major concern. From reliability studies, the capacitors were shown to be of little interest. The real impact of the increased ripple as a function of reactive power support is in the capacitor cost. This cost can be mitigated by the unique topologies under consideration, but a general rule is to either limit the amount of capacitance required, as accomplished by both topologies B and C, or limit the voltage to which the capacitors were exposed, as was the case in the micro-inverter of Topology B. Otherwise it could be expected that the amount of capacitance would double to maintain the same ripple magnitude for operation at 0.5 power factor.

Determining the feasible amount of reactive power for production from an inverter will be dependent on the application. Single-phase inverters may use reactive power for intentional islanding, low voltage ride-through, or to support local area voltages. However, reactive power production must be taken into account in the power system operation. The increased cost of both the capacitors to maintain the same operational breadth, and the increase in MOSFETs to

maintain the reliability of the inverter, must be balanced with a financial benefit for reactive power support.

There have been studies to determine the beneficial effects of reactive power production in a distributed resource [36-37], as well as discussion of how this will eventually lead to increased value. Incentive programs have not yet been implemented in single-phase markets. Future work should involve a feasibility analysis of reactive power production showing the benefits to the grid and the distributed generation owner.

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APPENDIX A – EQUATION DERIVATIONS

Equations (7)-(8)

Ripple Derivation

$$v(t) = V_m \cos(\omega t + \theta_v)$$

$$i(t) = I_m \cos(\omega t + \theta_i)$$

$$p(t) = v(t)i(t) = V_m I_m \cos(\omega t + \theta_v)\cos(\omega t + \theta_i)$$

$$p(t) = \frac{V_m I_m}{2}\left(\underbrace{\cos(\theta_v - \theta_i)}_{DC\ Term} + \underbrace{\cos(2\omega t + \theta_v + \theta_i)}_{Double\ Frequency\ Ripple} \right)$$

Equations (9)-(10)

Coefficient γ

$$S^2 = P^2 + Q^2$$

$$S = \underbrace{(1-\gamma)^{1/2} S}_{P} + \underset{Q}{j\gamma^{1/2} S}$$

$$S^2 = \left((1-\gamma)^{1/2} S\right)^2 + \left(\gamma^{1/2} S\right)^2$$

$$S^2 = (1-\gamma) S^2 + \gamma S^2$$

$$S^2 = S^2 - \gamma S^2 + \gamma S^2$$

$$pf(\gamma) = \frac{P}{S} = \frac{(1-\gamma)^{1/2} S}{S} = (1-\gamma)^{1/2}$$

Equation (11)

$$\frac{V_m I_m}{2}\cos(2\omega t + \theta_v + \theta_i) = \frac{V_m I_m}{2}\left[\cos(2\omega t + 2\theta_i)\cos(\theta_v - \theta_i) - \sin(2\omega t + 2\theta_i)\sin(\theta_v - \theta_i)\right]$$

$$= \frac{V_m I_m}{2}\cos(2\omega t + 2\theta_i)\cos(\theta_v - \theta_i) - \frac{V_m I_m}{2}\sin(2\omega t + 2\theta_i)\sin(\theta_v - \theta_i)$$

$$= P\cos(2\omega t + 2\theta_i) - Q\sin(2\omega t + 2\theta_i)$$

Equations (12)-(13)

$$E = \int_{t_1}^{t_2} \left[P\cos(2\omega t + 2\theta_i) - Q\sin(2\omega t + 2\theta_i) \right] dt$$

$$= \int_{t_1}^{t_2} \left[P\cos(2\omega t + 2\theta_i) - Q\sin(2\omega t + 2\theta_i) \right] dt$$

$$= \frac{P}{2\omega}\sin(2\omega t + 2\theta_i) + \frac{Q}{2\omega}\cos(2\omega t + 2\theta_i)\Big|_{t_1}^{t_2}$$

$$= \frac{P}{2\omega}\left\{ \sin\left(\left[\frac{1}{2\omega}\left(\frac{3\pi}{2} - \theta_i \right) \right] 2\omega + 2\theta_i \right) - \sin\left(\left[\frac{1}{2\omega}\left(\frac{\pi}{2} - \theta_i \right) \right] 2\omega + 2\theta_i \right) \right\}$$

$$+ \frac{Q}{2\omega}\left[\cos\left(\left[\frac{1}{2\omega}\left(\frac{3\pi}{2} - \theta_i \right) \right] 2\omega + 2\theta_i \right) - \cos\left(\left[\frac{1}{2\omega}\left(\frac{3\pi}{2} - \theta_i \right) \right] 2\omega + 2\theta_i \right) \right]$$

$$= \frac{P}{2\omega}\left\{ \sin\left(\left(\frac{3\pi}{2} - \theta_i \right) + 2\theta_i \right) - \sin\left(\left(\frac{\pi}{2} - \theta_i \right) + 2\theta_i \right) \right\}$$

$$+ \frac{Q}{2\omega}\left[\cos\left(\left(\frac{3\pi}{2} - \theta_i \right) + 2\theta_i \right) - \cos\left(\left(\frac{\pi}{2} - \theta_i \right) + 2\theta_i \right) \right]$$

$$= \frac{P}{2\omega}\left\{ \sin\left(\frac{3\pi}{2} + \theta_i \right) - \sin\left(\frac{\pi}{2} + \theta_i \right) \right\} + \frac{Q}{2\omega}\left[\cos\left(\frac{3\pi}{2} + \theta_i \right) - \cos\left(\frac{\pi}{2} + \theta_i \right) \right]$$

Equations (15)-(16)

$$S_c(t) = v_c i_c = S\cos(2\omega t)$$
$$v_c(t) = V_{dc} + \tilde{v}$$
$$i_c(t) = \frac{S}{V_{dc}}\cos(2\omega t)$$
$$i_c(t) = C\frac{d\tilde{v}}{dt}$$
$$\tilde{v} = V_r \sin(2\omega t)$$
$$i_c(t) = 2\omega V_r C\cos(2\omega t)$$
$$C = \frac{S}{2\pi f V_{dc}\Delta V}$$
$$\Delta V = 2V_{ripple}$$
$$C = \frac{S}{2\omega V_{dc} V_{ripple}}$$

Equations (34)-(35)

$$S = I_{ref}\cdot V_{grid} = \sqrt{P^2 + Q^2}$$
$$= \sqrt{(I_{star}V_{grid})^2 + Q^2}$$
$$I_{ref} = \frac{\sqrt{(I_{star}V_{grid})^2 + Q^2}}{V_{grid}}$$
$$PF = \frac{P}{S} = \cos(\theta_v - \theta_i)$$
$$= \frac{I_{star}V_{grid}}{\sqrt{(I_{star}V_{grid})^2 + Q^2}} = \cos(0 - \theta_i)$$
$$\theta_i = -\cos^{-1}\left(\frac{I_{star}V_{grid}}{\sqrt{(I_{star}V_{grid})^2 + Q^2}}\right)$$

APPENDIX B – CAPACITOR COMPONENT DATA

Part Number	Digi-Key Part Number	Manufacturer Part Number	Description
1	P14022-ND	EET-HC2V121HA	CAP 120UF 350V ELECT TS-HC
2	CGS242T350V4L-ND	CGS242T350V4L	CAP 2400 UF 350V ELECT SCREW TERM
3	P11761-ND	EET-HC2G181CA	CAP 180UF 400V ELECT TS-HC
4	B43580A5338M000-ND	B43580A5338M000	CAP 3300UF 450V ELECT ST
5	P6150-ND	ECO-S2GP271CA	CAP 270UF 400V ELECT TSUP
6	CGH492T350W5L-ND	CGH492T350W5L	CAP 4900UF 350V ELECT ST
7	P11223-ND	EEU-FC1E102L	CAP 1000UF 25V ELECT FC RADIAL
8	P13861-ND	EET-UQ2G181HA	CAP 180UF 400V ELECT TS-UQ
9	493-1918-ND	UPW1H122MHD	CAP 1200UF 50V ELECT RAD
10	P6150-ND	ECO-S2GP271CA	CAP 270UF 400V ELECT TSUP
11	193-1628-ND	UHE1H182MHD6	CAP 1800UF 50V ELECT RAD
12	P13334-ND	EET-UQ2S391CA	CAP 390UF 420V ELECT TSUQ
13	338-1881-ND	SFA44S7.5K288B-F	CAP FILM OIL WOUND 7.5UF 440VAC
14	P13859-ND	EET-UQ2G151HA	CAP 150UF 400V ELECT TS-UQ
15	338-1879-ND	SFA44S10K375B-F	CAP FILM OIL 10UF 440VAC
16	493-2612-ND	LLS2W221MELC	CAP 220UF 450V ELECT LS SNAP
17	21FB4415-F-ND	21FB4415-F	CAP FILM OIL 15UF 440VAC
18	P11897-ND	EET-UQ2G331CA	CAP 330UF 400V ELECT TS-UQ

APPENDIX C – MOSFET COMPONENT DATA

Part Number	Digi-Key Part Number	Manufacturer Part Number	Description
1	FQPF2N40-ND	FQPF2N40	MOSFET N-CH 400V 1.34A TO-220F
2	497-3264-5-ND	STW26NM50	MOSFET N-CH 500V 30A TO-247
3	FQB3N40TM-ND	FQB3N40TM	MOSFET N-CH 400V 2.5A D2PAK
4	497-3268-5-ND	STY60NM60	MOSFET N-CH 600V 60A MAX247
5	IRFR310PBF-ND	IRFR310PBF	MOSFET N-CH 400V 1.7A DPAK
6	FQU5N50TU-ND	FQU5N50TU	MOSFET N-CH 500V 3.5A IPAK
7	FQB3N40TM-ND	FQB3N40TM	MOSFET N-CH 400V 2.5A D2PAK
8	497-6565-2-ND	STD7NK40ZT4	MOSFET N-CH 400V 5.4A DPAK