STABILITY AND BANDWIDTH INVESTIGATION OF ALTERNATIVE STRUCTURES FOR NANOPORE SENSORS

BY

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THESIS

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ABSTRACT

The genetic information carriers, DNA molecules can be thought of as the blueprints of living organisms. This crucial functionality of the DNA molecules may explain the drive and momentum for DNA sequencing research. The commonly used parallel sequencing methods require extensive sample preparation, long processing times and expensive chemical reagents. In order to realize the goal of $1000 genome sequencing, many alternative methods are proposed. One of the most promising technologies among these is nanopore sequencing. Nanopore sequencing involves the threading of a DNA molecule between two electrolytic reservoirs through a nanometer-sized pore on a synthetic or an organic platform by means of electrophoresis and/or magnetism. During the threading of DNA molecules, various electrical aspects of the bases are investigated. The minimal label-free sample preparation, possibility of parallelizability and high throughput are the factors that make this method a very promising solution for low-cost, robust and fast DNA sequencing. In the nanopore sequencing field, the synthetic platforms have the advantage of durability and mass production value due to the existing silicon device fabrication technologies. This thesis work focuses on the stability and bandwidth investigation of alternative structures for nanopore sensing. Membranes with various thicknesses of Al_2O_3, Si_3N_4 and SiO_2 stack configurations were fabricated. The fabricated membranes were analyzed and drilled through by focused e-beam sputtering in TEM. The membranes were tested in 0.1 M and 1 M KCl solutions for IV characteristics, noise level and AC response. The membranes with desirable noise and IV characteristics were further tested for DNA sensing purposes. The membranes featuring Al_2O_3 insulating layer configurations yielded low noise, high bandwidth and limited durability in KCl solutions. The low yield in DNA sensing in 1 M KCl solutions using these architectures forms the background and motivation for next generation structures for DNA sensing.

To Maria Berenice Carrasco for making everything more enjoyable.

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CHAPTER 1

INTRODUCTION

The genetic information carriers, DNA molecules can be thought of as the blueprints of living organisms. Grasping the language of these blueprints will ultimately unlock the paths to unprecedented developments in the fields of medicine and bioengineering. This crucial functionality of the DNA molecules and the many unknowns about its working mechanisms may explain the drive and momentum for DNA sequencing research [1, 2].

The human genome project was completed in 2003 by joint effort [3]. The sequenced DNA is available for research. The processing of the genetic code in the 1980s opened up new branches of science, like bioinformatics. The general belief is that with more advanced sequencing techniques, the sequencing of a human genome will be cheaper, faster and more robust. As the goal set by the Genome Project, the cost of sequencing the complete genome of a person is aimed to be reduced to $1000 [4]. This will allow a wider scale of genes to be sequenced. The amount of data gathered about the human genome is going to increase. That is ultimately going to allow the deduction of patterns in the genetic code that were not apparent before, paving the way for further developments in the biology related fields.

The commonly used parallel sequencing methods require extensive sample preparation, long processing times and expensive chemical reactions [5]. In order to realize the goal of $1000 genome sequencing, many alternative methods are proposed [6, 7]. One of the most promising technologies among these is nanopore sequencing. Nanopore sequencing involves the threading of a DNA molecule between two electrolytic reservoirs through a nanometer-sized pore on a synthetic or an organic platform by means of electrophoresis and/or magnetism. During the threading of DNA molecules through this confinement, various electrical aspects of the bases are investigated. The minimal, low-cost and label-free sample preparation, possibility of parallelizability and high throughput are the factors that make this method a very

promising solution for low-cost, robust and fast DNA sequencing.

In the nanopore sequencing field, the synthetic platforms have the advantage of durability and mass production value due to the existing silicon device fabrication technologies. This thesis research focuses on the stability and bandwidth investigation of alternative structures for nanopore sensing. Membranes with various thicknesses of Al_2O_3, Si_3N_4 and SiO_2 stack configurations were fabricated. The fabricated membranes were analyzed and drilled through by focused e-beam sputtering in TEM. The membranes were tested in 0.1 M to 1 M KCl solutions for IV characteristics, noise level and AC response. The membranes with desirable noise and IV characteristics were further tested for DNA sensing purposes. The membranes featuring Al_2O_3 insulating layer configurations yielded low noise, high bandwidth and limited durability in KCl solutions. The low yield in DNA sensing in KCl solutions using these architectures forms the background and motivation for next generation structures for DNA sensing.

CHAPTER 2

DNA SEQUENCING

2.1 Drive for DNA Research

Although the metabolism of living organism is an ancient subject of interest, the scientific study about the genetic information that governs the metabolism dates back to 1868 when the Swiss biochemist Friedrich Miescher identified the nucleic acids as the guiding substance in the development of cells and their functions [8]. At the beginning of the 1900s, Edmund Wilson hypothesized that the nucleic acid "is in a chemical sense the formative center of the cell" by the use of which the nucleus directs "the cell through the process of synthetic metabolism." In the later years, it was found that there were two fundamental types of nucleic acids, *ribose* and *deoxyribose* [9]. The developments in the biochemistry of nucleic acids around 1920 came to a dead end around the early 1940s. It was found that the nucleic acids consisted of four types of bases, but the observation that the number of each base could be found approximately in equal quantities in all of the examined nucleic acid polymer chains did not help to explain how the DNA functioned as a genetic information carrier.

DNA was unequivocally established to carry genetic information with the genetic experiments of Hershey and Chase in 1952 [10]. At the time, it was known that after a bacteriophage infected a bacterium, the bacterium began to produce replicas of the bacteriophage. The Hershey and Chase experiment showed that the bacteriophages hijacked the infrastructure of the bacteria by introducing their own genetic code, which they also established to be DNA.

With the advent of new microscopy techniques and crystallography, the structure of the DNA was resolved by James D. Watson, Francis Crick, Maurice Wilkins and Rosalind Franklin in the 1950s [11]. Further studies in biochemistry and genetics laid out DNA replication and repair mechanisms.

Based on these replication mechanisms, in 1974, Frederick Sanger and his co-workers developed a rapid sequencing method based on chain termination. Basically, the developed technology required template DNA in single-stranded form, primers, the fluorescently labeled deoxynucleotides, dATP, dGTP, dCTP, dTTP and chain termination nucleotides. These modified nucleotides (dideoxynucleotides) missed the 3' OH group which essentially caused the termination of the polymerization reaction. The sample DNA was divided into four tubes with regular nucleotides, polymerases and the primers. Each tube was assigned only one type of chain termination nucleotide. As the polymerase reaction progressed in a tube, the single-strand template was polymerized up to the point where the chain termination nucleotide was incorporated into the sequence. Eventually, the reaction would be terminated at each possible point in the sequence that had the assigned nucleotide. After the denaturation of the hybridized DNA chains, each tube had various length single strands ending with the labeled chain termination nucleotide. Then, the products of these four tubes were placed in four lanes and spread in polyacrylamide-urea gel using the gel electrophoresis technique according to their lengths. All the lanes were complementary to each other in terms of sequence length, which ultimately indicated the termination nucleotide at each sequence point. Currently, most of the commercially available automated sequencing systems are based on variants of this technology [12, 13].

2.2 Techniques in Use

At present, the Sanger method is still widely used. The main modification to the method is to use fluorescent labels for the chain termination nucleotides rather than the polymerization nucleotides. Each type of chain termination nucleotide has a different wavelength-activated fluorescent label. As a result, the reaction can take place in one tube, and the sample can be run in the same lane in the gel electrophoresis process [7].

2.3 Advantages of Nanopore Sensing

2.3.1 High Throughput

Another major advantage of nanopore sequencing schemes is its prospect for high throughput for sequencing. The high throughput is acquired by the minimal sample preparation, high-speed read-out and massive parallelizability. Compared to the commercially available technologies, the ideal sample preparation for the nanopore sequencing is minimal. This cuts down the sample preparation time significantly [14, 5].

In addition, since the DNA threaded through a nanopore, and the information on the molecule is read through electrical means, the rate of sequencing depends on the bandwidth of the system. The system consists of the sequenced sample and the means to sense it, in other words, the nanopore setup. The read sample has a durability that allows a certain amount of force to be applied according to the length of the DNA [15, 16]. That determines how fast the DNA can be threaded through a nanopore before it shears. On the other hand, the nanopore setup can be defined as a platform where two reservoirs, cis and trans, are spanned by a confinement that narrows the number of states that the DNA can translocate between to make the electrical attributes associated with the nucleotides become accessible. It also includes the means to take the measurement of this accessible information about the nucleotides.

Parallelizability means that this information gathering can be done in a parallel manner, rather than serially, by means of many pores with their own measurement setups. This part of the equation is also governed by the technologies that are used for forming the pores. For mass production, e-beam sputtering technologies that work in parallel may be required for the task [17, 18, 19].

2.3.2 Sample Preparation

One of the aspects that the nanopore sequencing schemes excel in is the low-cost sample preparation. As it is a label-free approach, it requires minimal sample preparation. It may be more intuitive to describe the main costs related with the Sanger method to illustrate how label-free DNA sequencing

is going to save costs.

As the sample DNA is polymerized with the fluorescently labeled termination nucleotides, the fidelity of the read-out is also a function of the purity and the quality of fluorescent label. The high purity of these labels and the quantity that is demanded make it a huge cost for the sequencing of a genome. Furthermore, as the method relies on the differentiation of different length DNA strands, they need to be amplified in great quantities. The DNA amplification is a very costly process as it entails biochemical reagents like primers, nucleotides and polymerases. Furthermore, during the gel electrophoresis step, in order to achieve single-base resolution, the DNA needs to be cleaved down to very short lengths. That also translates into very extensive gel electrophoresis to sequence a complete genome. Besides, the detection calls for sophisticated fluorescent microscopes [7].

Label-free nanopore DNA sequencing is going to minimize the cost of amplification, cleaving and the use of high-purity reagents. First of all, the DNA strands require lower number of cleavages for a read-out. Since it is going to be threaded through the pore, it only needs to be cut in specific lengths to accommodate the translocation. The length of the sample is a function of the DNA molecule's stress resistance and the probability of the end of the strand aligning with the pore or, in other words, capture rate. The maximum length of the ssDNA that can be translocated is about 25 kb. It has been reported that λ DNA molecules (48 kbp) can be threaded through nanopores [20, 21]. The capability to translocate such length molecules corresponds to several orders of magnitude less sample cleaving. The method does not require fluorescent labeling and extensive polymerase reactions. This decreases the cost related with high-purity chemical reagents, incubators and polymerases that facilitate the hybridization. It eliminates the gel electrophoresis step where the samples spread through the gel and are detected by a sophisticated fluorescent microscope.

2.4 DNA Sequencing Approaches using Nanopore Sensors

Even though it is demonstrated that single- and double-stranded DNA can be translocated and discriminated through synthetic and biological nanopore

sensors [22, 23], the single-nucleotide resolution is not yet achieved due to the limitations associated with geometry of the pores. The barrel length of the α-hemolysin biopores are 5 nm long, while the synthetic nanopores are commonly formed on 10 nm SiN membranes. Consequently, during the translocation of DNA, the modulation of ionic conductivity is caused by several nucleotides at once [24]. Even though the membrane thickness would be infinitely thin, the electric field through a nanopore sensor extends two times the diameter of the pore into the electrolyte solution. Considering that the ssDNA can translocate through a minimum pore diameter of 1.5 nm, the 3 nm effective electric field would ensure that the ionic modulation through the pore would be due to a minimum of eight nucleotides [25, 26, 27, 28]. Besides, the translocation rate through the nanopores can be decreased to one nucleotide/μs at 150 mV bias. Yet, the bandwidths of the current measurement systems are limited to hundreds of kilohertz at best. The ideal translocation rate would be equal or slower than one nucleotide/ms.

To overcome these limitations [5], different approaches are proposed. One such method is unzipping hybridized DNA while translocating through single-strand discriminating pores and detecing the by-products, like emitted photons or the force required for unzipping. Synthetic nanopore sensor methods include capacitor membranes and placement of tunneling probes through the pore. Using α-hemolysin pores with exonuclease attached barrels are also among the prominent approaches to achieve single-nucleotide resolution and specificity.

The detection of hybridized DNA strands is an intriguing idea due to the nanopore sensor capability to differentiate between single- and double-stranded DNA. The hybridized DNA can be translocated through a nanopore, and during the unzipping of the second strand, the photon that is emitted can be sensed. This method has the limitation of the common problems about the accuracy of site-specific hybridization [15]. Locating the hybridized probes to reconstruct the complete sequence is also prone to inaccuracies. Besides, although this approach can be extensively used and decreases the costs, it is not a label-free method [29, 30] (Figure 2.1).

Simulations of synthetic membranes with embedded capacitor electrodes show that they can theoretically achieve single-nucleotide resolution [31, 32, 33, 21] (Figure 2.2). These simulations are performed using a structure where the capacitor pads are 100 nm x 100 nm. Fabricated capacitor membranes

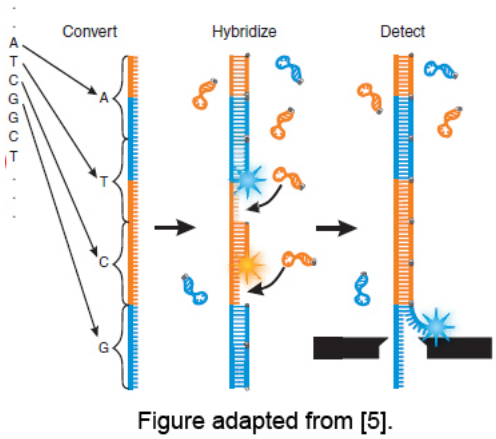

Figure 2.1: Hybridized DNA strands are threaded through a nanopore for nanopore sequencing.

to date use a MOS structure with 2 μm x 2 μm, 6 μm x 6 μm and 10 μm x 10 μm capacitor pads. These membranes have poor insulation between the capacitor plates and the electrolyte. They also have very high parasitic capacitive elements in the circuit that prevent nanopore sensing with single-nucleotide resolution. Furthermore, the use of highly doped silicon for the capacitor pads decreases the sensitivity of the sensor to the DNA strands.

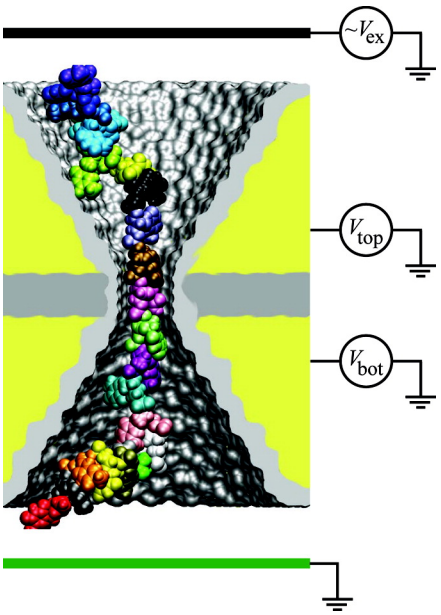

Figure 2.2: DNA sequencing using a capacitor membrane structure.

Experiments with STM probes show that transverse tunneling conduction through different nucleotides has different current signatures [34, 35].

This property is desired to be incorporated to a nanopore. So far, there has been no successful attempt at achieving such a structure (Figure 2.3). There are four main hurdles to be overcome [36]. First, the optimum temperature, pressure and electrolyte concentration for taking a tunneling current measurement in an electrolyte solution needs to be investigated. Second, the nanopore needs to ensure that the nucleotides pass through with highly reproducible orientation and position, because a small variation in the orientation of the molecule will significantly alter the measurement data [37]. Third, the translocation of the DNA needs to be slowed down to a rate that will allow enough sampling for single-nucleotide resolution. Fourth, the current characteristics between the bases need to be investigated to sense the differences between two bases. Another approach can be ensuring the rate of translocation very accurately to separate the signal reading between two bases based on the time intervals between bases. In order to attain this goal, use of carbon nanotubes and graphene layers is proposed. The nanotubes can be functionalized to bind nucleobases in desired specific orientations and control their rate of passage. On the other hand, graphene is also a good candidate for patterning electrodes for their single-layer topology which would be the closest alternative to infinitely thin electrodes. Another suggestion is to modify the first of the two metal electrodes with molecular groups that bind to the backbone of the DNA strand, while the second electrode is functionalized to complement the hydrogen bonds of one of the nucleotides [38]. Using this approach, the transverse tunneling current is greatly increased for only one type of base. Yet, this approach needs to address how to measure four different bases simultaneously.

Another prominent approach to nanopore sensors is to use biopores. It is shown that aminocyclodextrin-attached α-hemolysin pores produce distinct current signatures for different unlabeled dNTPs. The current signature was distinct enough to identify the different bases and the number of the bases that pass through. It has been proposed to attach an exonuclease to the opening of the α-hemolysin pores to ensure that the digested DNA molecule's bases sequentially pass through the pore [39, 40]. The major challenge about this proposal is to bind the exonuclease to the pore in a way that would not occlude the function of the exonuclease, while ensuring the digested base can only be released after passing through the pore.

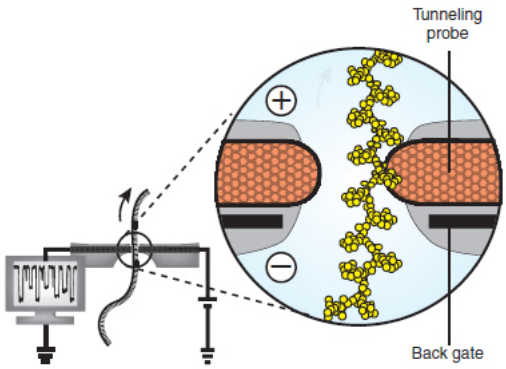

Figure 2.3: Transverse tunneling current through nucleic bases is used for identification.

2.5 Sensitivity and Long Read-Outs

Sensitivity of a nanopore can be explained as the capture rate for translocation through the nanopore for a given KCl concentration. The sensitivity of the pore is also a function of the length of the DNA polymer. As the polymer gets longer, the capture rate of a sample drastically decreases. These parameters conflict with each other on the path to achieving long DNA read-outs. Fortunately, recent developments in the field solve this conflict.

The capture rate depends on the probability that the end of the strand is aligned with the pore. This is governed mainly by two parameters: the length of DNA strand that needs to be translocated and the radius of the electric field that would pull the molecule inside the pore. The mainstream approach to capture the DNA in the pore is done through a stochastic process where the DNA molecules are homogenously distributed throughout the cis reservoir. The molecules with radius of gyration that coincides with the capture radius of the nanopore feel a force towards the pore. The translocation of the DNA is governed by the probability of the DNA molecule end finding a path to the pore and eventually being pulled through the membrane by the electrophoretic force. This process has a lower probability as the DNA strand gets longer and the KCl solution concentration increases. The longer strands have larger radius of gyration that decreases the probability that the end of the polymer is affected by the electric field that extends from the pore. An increase in electrolyte concentration decreases the Debye length and, thus, decreases the capture radius of the pore.

In order to solve the orientation problem, the Dekker group managed to attach DNA molecules to a bead with streptavidin bonds [41, 42]. An optical tweezer is used to control the location of the bead with the DNA molecule. The beads were aligned with the pore and a bias between the cis and trans reservoirs was applied to extend the attached DNA molecule. Thus, the translocated DNA molecule would have a controlled orientation rather than a stochastic one. Besides being low yield, this method required a highly customized and very sophisticated setup.

More recently, it is demonstrated that the DNA can be bound to magnetic beads by streptavidin-biotin bonds. Using a magnetic gradient, the DNA can be translocated through a nanopore in a controlled fashion whereby the electrophoretic force is pulling the DNA through the pore; the magnetic force on the bead provides the means to counter the pull [43]. This results in unprecedented control over the orientation and motion of the translocating DNA molecule. As it is called by the group, "magnetic tweezers" solve the problem associated with stochastic orientation of the DNA to the pore and bandwidth-related issues discussed previously. Furthermore, this method also opens the pathway to massive parallelization options with high levels of synchrony.

Another recent exciting development is the demonstration of the increased capture rate by the employment of different salt concentration in cis and trans reservoirs. The Meller group reported that the capture rate can be increased by 30 times compared to the experiments with symmetrical electrolyte concentrations in cis and trans reservoirs [44]. Because the conductivity is governed by the high salt concentration reservoir in a nanopore sensor fluidic system, decreasing the electrolyte concentration in the cis reservoir does not have any detrimental effects on the current level [45]. On the contrary, it marginally increases the bandwidth of the system by expanding the Debye length of the electrolyte solution in the cis reservoir. A greater Debye length provides a smaller double layer capacitance on the surface of the chip in the cis reservoir. In effect, the membrane capacitance is reduced while the electrolyte serial resistance is kept low. Most important of all, a greater Debye length increases the capture radius of the nanopore. This is also reflected by an order of magnitude increase in the capture rate of the pore in the presented experiments.

Consequently, in the light of the new developments, it would be reasonable

to assume that significant progress is being achieved in the solution of the problems due to orientation, capture rate and bandwidth with the mastery of these techniques.

2.6 Pore Formation Technology

The popularly used biopores, α-hemolysin pores, are demonstrated to be unexpectedly stable, despite the lipid platform they are embedded in. The lipid bilayer is shown to be modified to increase its integrity, using a combination of techniques involving agarose gel and smaller apertures [5]. The synthetic nanopores are formed on metal oxides, silicon nitride and silicon dioxide by ion beam sculpting [18], atomic layer deposition [46] and e-beam drilling [47] methods. Ultimately, the commercial nanopore systems are expected to be a combination of synthetic and biological nanopores [5]. As this thesis focuses on synthetic nanopores, the techniques to form pores on synthetic membranes will be discussed in greater detail.

Ion beam sculpting is a technique that employs a focused ion beam (FIB) tool to drill through an insulating free standing membrane. In Golovchenko's group, the free-standing 500 nm thick Si_3N_4 membrane is thinned down with a cavity from one side [18]. From the other side, the ion beam is scanned through the surface to etch with small increments (Figure 2.4). As the surface is uniformly etched, the tip of the cavity opens up and forms a nanopore. This procedure is automated by the detection of ion flow through the opened up hole. The cavity structure on the membrane is produced by wet etching, which is not an ideal technique as it requires extensive rinsing and it is hard to reproduce the etch profile. As this technique requires less initial investment compared to atomic layer deposition and e-beam drilling, it is a remarkable technique to research nanopore sensors.

Atomic layer deposition eliminates the need to form a cavity on the membrane to achieve a small pore on an insulating layer. Instead, a 100 nm diameter FIB drilled pore is placed in an ALD chamber [46]. Due to the atomic layer deposition's high uniformity, even on an anisotropic surface, the deposited material coats the surface with the same thickness (Figure 2.5). This attribute is utilized to shrink the size of the pore with the desired material with < 1 nm resolution. In Branton's group, Al_2O_3 is preferred due

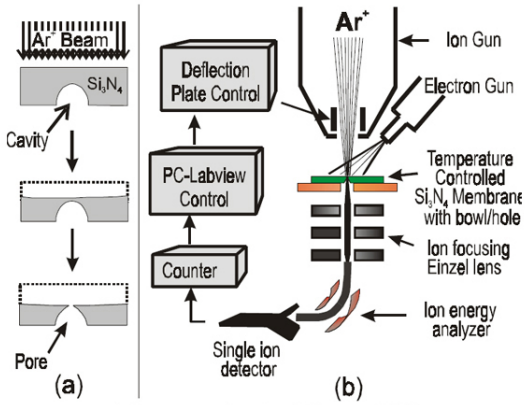

Figure adapted from [18].

Figure 2.4: Ion beam sculpting: *a*) 500 nm thick Si_3N_4 membrane with cavity. *b*) Automated drilling setup.

to its isoelectric point and other surface properties. This technique may be the solution for mass production of highly reproducible synthetic nanopores. Yet, with this technique the integration of electrodes into a pore is a big challenge to overcome.

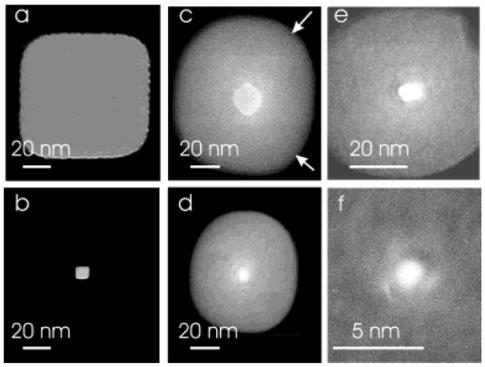

Figure adapted from [46].

Figure 2.5: TEM images of several FIB drilled pores (top row) after ALD procedure (bottom row).

E-beam drilling refers to a process that uses high energy electron beams to sputter the molecules on a thin free-standing membrane [47]. A transmission electron microscope (TEM) with a field emission gun is used to form pores on synthetic membranes with better than 1 nm resolution (Figure 2.6). The data presented in this thesis is also acquired with pores formed using this technique. During the sputtering process, the ability to control local heating

of the surface allows resizing of the formed pore by reflowing or expanding. The TEM is an instrument that can be highly automated and is capable of measuring the current flow through a sample. Although TEM is a very versatile and powerful tool, it is not engineered for forming pores on synthetic membranes. Therefore, the drilling of the pores is slow and requires the active attention of the operator.

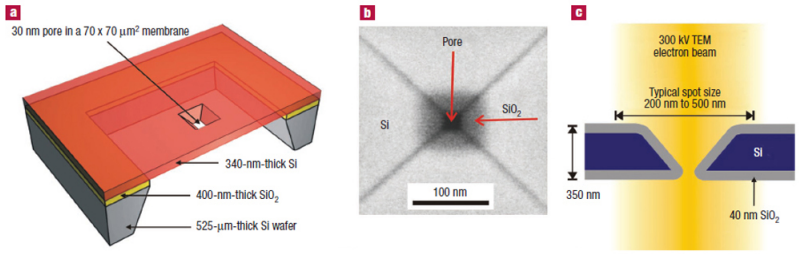

Figure adapted from [47].

Figure 2.6: Brief overview of e-beam drilling of a SiO_2 membrane.

As these methods are practiced in research environments, the formation of the pores requires a high level of manpower. The goal of massive parallelization makes it essential to form accurately reproducible nanopore arrays. This task demands commercial intervention and the advent of new instruments, such as field emission electron guns with multiple beams with automated drilling software.

CHAPTER 3

FABRICATION

3.1 Test Wafer 15

3.1.1 Motivation

The fabrication of test wafer 15 (TW15) aims to alleviate the low-yield problem in the previous runs, such as Test Wafer 10 (TW10), improve the bandwidth by using a relatively thicker passivation PECVD Si_3N_4 and supply new membranes for further DNA translocation and materials characterization experiments. The wafer yield turned out to be good, and the data taken with these membranes produced valuable results.

3.1.2 Fabrication

I fabricated this wafer in collaboration with Bala Murali Venkatesan (LIBNA Group member). A double-side polished wafer is deposited with ALD alumina which is followed by a silicon nitride passivation layer. The wafer front side is patterned with 7 mm by 7 mm dice with 30 μm features. The pattern is etched using reactive ion etching with CF_4 chemistry until the Al_2O_3 layer is exposed, which ultimately is going to form the free standing membrane. The back side is patterned in alignment with the front side. The features are etched in DRIE through the wafer to hit the Al_2O_3 layer. The fabrication of the membranes ends with stripping of the photoresist from the wafer.

Initially, the 300 μm thick, 10 Ω-cm, double-side polished <100> orientation silicon wafer is measured in the FSM tool and cleaned in piranha solution for 15 min. The cleaned wafer is carefully N_2 blow dried; in case a droplet stain due to incomplete drying results in pinholes in the ALD alumina layer. The wafer is placed inside the Cambridge Nanotech ALD system chamber

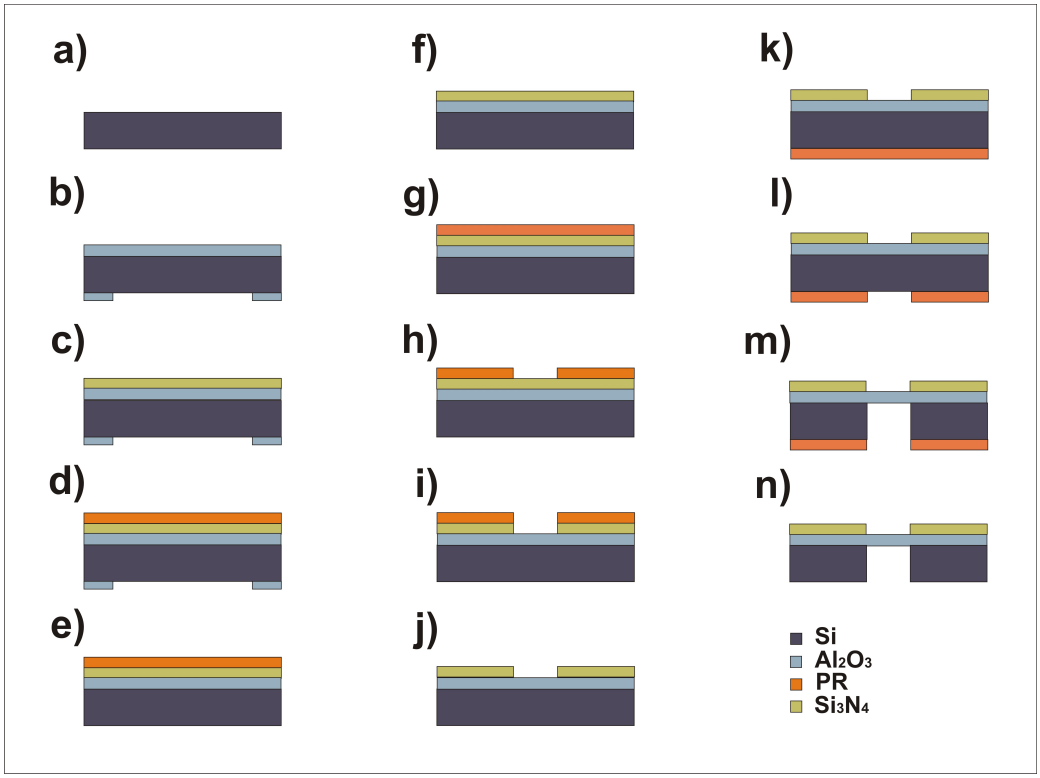

Figure 3.1: Process flow for TW15 fabrication.

at 250 ^{o}C and 256 mT. The reagents are pulsed in the ALD chamber for 700 cycles. The resultant alumina thickness is 723.369 Å(Table 3.1). The deposition bleeds to the backside of the wafer and covers up to half of the surface area (Figure 3.1.b).

Table 3.1: Ellipsometer measurements for ALD Al_2O_3 thickness.

Location #	thickness(Å)	Fit Error
1	722.824	2.983
2	728.905	2.995
3	717.403	2.995
4	722.169	2.984
5	725.546	2.979
Average	723.369	2.987

Following the ALD deposition, the wafer is deposited with silicon nitride using the STS PECVD system (Figure 3.1.c). The deposition is done with a mixed frequency recipe that produces low-stress films. The higher frequency

for the plasma excitation is 13.56 MHz while the lower frequency is 380 kHz. The process is done under 900 mT pressure with 40 sccm NH_3 and 40 sccm SiH_4 flow rate at 300 ^oC. The high-frequency cycle is 6 s long and the low-frequency cycle is 2 s long. In order to have an accurate measurement of silicon nitride thickness, a dummy silicon wafer is processed with the same recipe. The nitride thickness yielded 6692 Å (Table 3.2).

Table 3.2: Ellipsometer measurements for PECVD Si_3N_4 thickness.

Location #	thickness(Å)
1	6680.855
2	6706.804
3	6691.889
4	6684.738
5	6699.210
Average	6692.699

Based on previous data, the Al_2O_3 residue at the back side of the wafer increases the stress on the wafer and prevents the backside etch. Since both silicon nitride and the alumina are etched by buffered oxide etch (BOE), the front side needs to be protected during the back side residue removal. The front side is spun with AZ1518 at 3000 rpm for 30 s and baked for 10 min at 110 ^oC. The PR sputters at the back side are wiped with cleanroom wipes soaked in acetone and methanol (Figure 3.1.d). The wafer is dipped in 10:1 buffered oxide etch for 10 min in two 5 min steps. After the 5 min etch, the Al_2O_3 residue is visible on the back of the wafer. The rinse after 5 min removes the precipitate from the wafer. After the second etch, there is no residue left, and this can be confirmed by the hydrophobicity of the wafer (Figure 3.1.e). After the residue removal is completed, the front side protection PR is removed using acetone, methanol and DI (Figure 3.1.f).

After the removal of the ALD alumina residue layer, FSM measurement of the wafer is taken to check the stress induced by the deposited layers. The stress of these layers has utmost importance for the mechanical stability of the free standing membranes. The stress of the wafer is measured to be 29.83 MPa. This stress level is low enough to have mechanically stable membranes.

Before doing the front side lithography, the wafer is cleaned once more in piranha solution for 15 min. It is baked for 5 min at 125 ^oC for dehydration

and placed on the spinner chuck. The wafer is covered with HMDS and rested 30 s. When the time for the stabilization of HMDS is elapsed, it is spun at 3000 rpm for 30 s. Before spin-coating with AZ1518, the wafer is left to rest for 1 min. The AZ1518 is spread to cover at least 75% of the wafer, and spun at 3000 rpm for 30 s (Figure 3.1.g). The wafer is soft baked for 5 min at 110 ^{o}C and exposed to 426 nm wavelength UV at 7.4 mW/cm^2 for 80 s. The mask features 30 μm by 30 μm window on 7 mm by 7 mm dice. The wafer is developed in 1:1 AZ developer for 80 s (Figure 3.1.h).

The wafer is loaded to the Plasma Therm Freon RIE chamber and etched with CF_4 chemistry under 35 mT pressure at a flow rate of 60 sccm at 90 W for 17 min (Figure 3.1.i). After the etch, based on color evaluation of the film, it is confirmed that the Al_2O_3 layer is exposed. The photoresist layer is removed using acetone, methanol and DI (Figure 3.1.j).

Before the back side lithography, the wafer is placed on the hot plate for 5 min for a dehydration bake. HMDS is poured on the wafer, and, spun at 1000 rpm for 30 s. Then, the AZ9260 is poured to cover most of the wafer, and it is spun at 1000 rpm for 30 s. As the resist has very low viscosity, the spun PR is not smooth. The PR on the wafer is allowed to stabilize for 20 min prior to any further processing (Figure 3.1.k). When the wait time elapses, the wafer is soft baked for 6 min at 110 ^{o}C. Then, the wafer is aligned according to the dicing lines in a Quintel aligner and exposed at 426 nm wavelength at 7.5 mW/cm^2 for 200 s. The exposed wafer is developed in 3:1 AZ 400K developer for 8 min. Finally, the wafer is hard baked for 30 min at 110 ^{o}C (Figure 3.1.l).

The wafer is attached to an oxidized carrier wafer. The carrier wafer is spin-coated with AZ1518 at 3000 rpm for 30 s. The wafer is placed on the carrier wafer for 1 min at room temperature. Then, the bonded wafers are baked for 1 min at 110 ^{o}C on the hot plate.

The bonded wafers are loaded to into the Plasma Therm FREON RIE chamber and etched for 40 s under 35 mT pressure at a flow rate of 60 sccm at 90 W with CF_4 chemistry. This etch serves as a break-in etch for the native oxide. Right afterwards, the wafers are loaded to the STS ICP RIE chamber and etched for 2 h 40 min 12 s (Figure 3.1.m). The etch cycle is 12 s long and the plasma is excited at 13.56 MHz frequency with a 130 sccm SF_6 and 13 sccm O_2 flow rate under 36 mT pressure at 12 W. The passivation cycle is 8 s long with a C_4F_8 flow rate of 130 sccm under 18 mT pressure.

The wafers are separated in AZ Remover at 80 ^{o}C in 2 h (Figure 3.1.n).

3.2 High-Resistivity Wafers

3.2.1 Motivation

For improving the bandwidth of the system, the TW15 architecture is modified to have a thicker silicon nitride thickness, a high-resistivity wafer substrate and smaller opening through the passivation layer.

3.2.2 Fabrication

For this purpose, two wafers are fabricated, HR3 and HR5, which differ from each other only by the exposed alumina area through the passivation layer. The wafer fabrication procedure begins with the deposition of ALD alumina on a double-side polished wafer. The wafer is deposited with a 1.4 μm thick silicon nitride layer on the alumina layer to serve as a passivation layer. Then, the back side and the front side of the wafer are oxide sputtered to improve the PDMS/chip interface for sealing. The wafer stack is patterned on the front side and etched until the Al_2O_3 layer is reached. The back side is also patterned in alignment with the front side dicing lines and the membrane window. The wafer is placed in a deep silicon etch system to be etched until the Al_2O_3 layer is exposed to form a free standing membrane.

After a radius of curvature measurement, a double-side polished 300 μm thick, 10000 Ω-cm wafer is cleaned in piranha solution for 10 min. The wafer is placed in the ALD reactor to grow 700 cycles of alumina in two steps which will form the membrane on the complete structure. The ALD chamber temperature is 250 ^{o}C and the pressure is 250 mT (Figure 3.2.b). The pulsed reagents increase the pressure up to 1 Torr. This recipe yields an alumina thickness of 67.5 nm with a dark brownish red color (Table 3.3).

Right after the ALD process, the wafers are deposited PECVD silicon nitride for 1 h 30 min with a mixed frequency recipe (Figure 3.2.c). The mixed frequency recipes produce lower stress films compared to high frequency and low frequency recipes. The higher frequency for the plasma excitation is 13.56 MHz while the lower frequency is 380 kHz. The deposition takes place

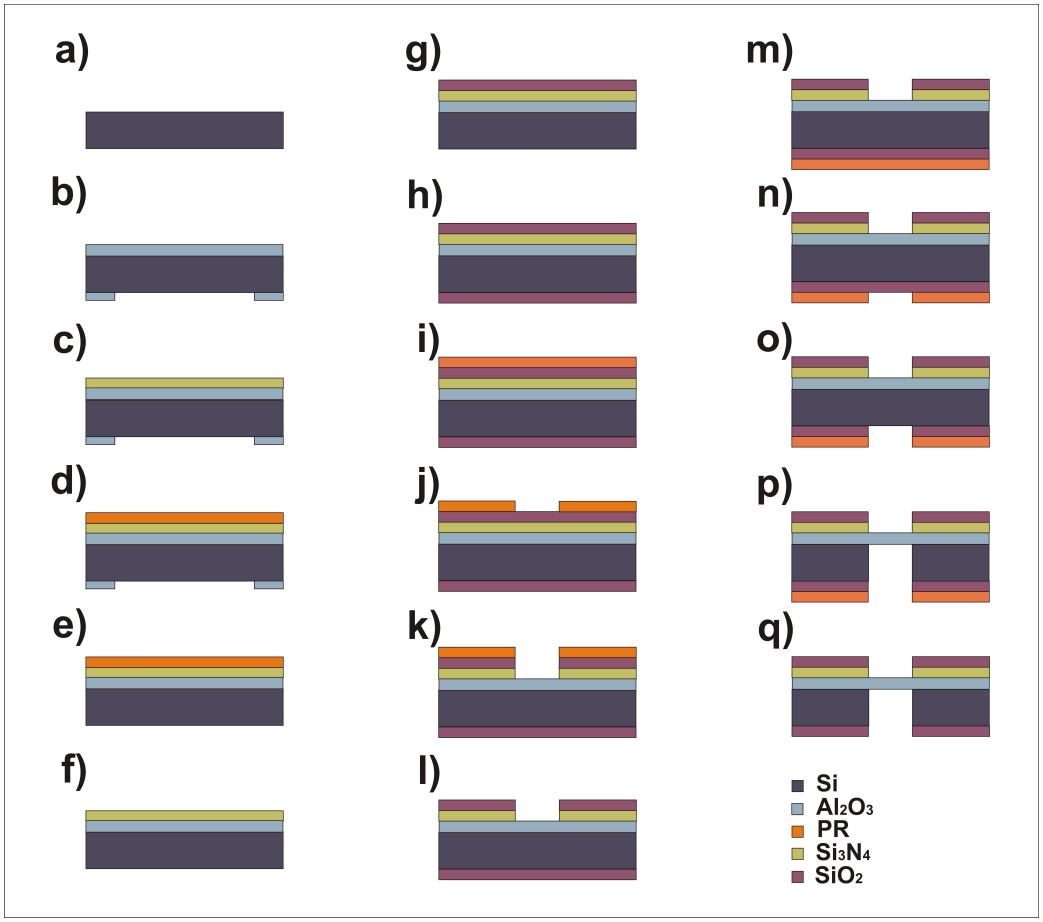

Figure 3.2: Process flow for high-resistivity wafer fabrication.

under 900 mT pressure with 40 sccm NH_3 and 40 sccm SiH_4 flow rate at 300 ^oC. The high frequency cycle is 6 s long and the low frequency cycle is 2 s long. At the end of this process, the wafers have a 13446Åsilicon nitride film which is confirmed by ellipsometer measurements on a dummy wafer that is processed with the identical recipe (Table 3.4).

After the ALD deposition, it is easily discernable that the Al_2O_3 is also deposited to a portion of the backside of the wafer. This layer has a potential of increasing the stress and also preventing the backside etch due to aluminas high resistance to reactive ion etching. Since both alumina and silicon nitride is etched by the buffered oxide etch, the front side of the wafer needs to be protected.

Therefore, AZ1518 photoresist is spun at 3000 rpm for 30 s on the frontside of the wafers after being coated with HMDS. The resist is baked for 10 min at 110 ^oC (Figure 3.2.d). During the spin process, sputters of PR is often

Table 3.3: Ellipsometer measurements for ALD Al_2O_3 thickness.

Location #	Thickness(Å)	Fit Error
1	672.621	0.292
2	674.167	0.287
3	671.689	0.290
4	678.625	0.286
5	680.180	0.286
Average	675.456	0.287

Table 3.4: Ellipsometer measurements for sputtered SiO_2 thickness.

Location #	Thickness(Å)	Fit Error	Refractive Index
1	13349.654	0.136	1.977
2	13447.361	0.240	1.986
3	13449.335	0.311	1.989
4	13498.114	0.320	1.998
5	13489.582	0.404	1.993
Average	13446.810	0.282	1.989

observed at the back of the wafer. These sputters are wiped with acetone and later methanol dipped cleanroom wipes. The use of wipes ensures that the front side PR is not affected by the backside clean up process. The wafers are rinsed in deionized water and dipped into the 10:1 buffered oxide etch for 10 min. When the wafers are rinsed, it is observed that no visible trace of the Al_2O_3 is left (Figure 3.2.e). Also, the wafer back sides become highly hydrophobic due to the stripping of the native oxide layer. Finally, the wafers are stripped from the photoresist by acetone, methanol and DI rinse (Figure 3.2.f).

Table 3.5: HR3 film stress measurements.

Scan #	Stress(MPa)	Radius(m)	Height(μm)	Film(Å)
1	0	180.24	6.94	0
2	43.01	17.81	70.20	14121

After the FSM measurement, the wafers are coated with sputtered oxide on the front side and the backside (Table 3.5). The silicon dioxide surface

provides a better surface for the PDMS gaskets that are used for sealing the chips to the cis and trans reservoirs. The front side is oxide sputtered for 3 h using a raised temperature recipe (Figure 3.2.g). The silicon dioxide target is sputtered with 300 W under 5 mT pressure with 20% O_2 and 80% Ar concentration at 150 ^{o}C. This recipe yields an oxide thickness of 925.4 Å on a dummy wafer when measured with a Rudolph ellipsometer (Table 3.6). The backsides of the wafers are sputtered using the recipe for 1 h (Figure 3.2.h). The wafer stack configuration is completed with this last step.

Table 3.6: Ellipsometer measurements for sputtered SiO_2 layer for etch characterization.

Location #	Thickness(Å)	Fit Error	Refractive Index
1	966.105	0.086	1.428
2	897.137	0.090	1.422
3	873.189	0.080	1.420
4	946.010	0.087	1.427
5	945.334	0.091	1.427
Average	925.555	0.087	1.425

The etch rate of the sputtered oxide in the Plasma Therm Freon RIE system is characterized with the CHF_3 recipe. The dummy wafer placed along with the HR3 and HR5 is spin coated with AZ1518 at 3000 rpm for 30 s after a HMDS spin. The wafer is exposed for 75 s using the 30 μm feature mask. Then, the pattern is developed for 70 s in 1:1 diluted AZ developer. The wafer is cleaved to two pieces for investigating the depth of different etch times. The first piece is etched for 3 min and the second piece is etched for 5 min. After the removal of the photoresist in acetone, methanol and deionized water, the features are investigated using the Alphastepper profilometer and SEM. Alphastepper measurements results are 202 Å/min etch rate for the 5 min sample and 196 Å/min etch rate for the 3 min sample (Table 3.7). The SEM images yields 173.3 Å/min for 3 min sample. The 5 min sample is etched at a rate of 182 Å/min (Figure 3.3 and 3.4).

The front sides of the wafers are patterned to etch through the SiO_2 and Si_3N_4 layers to hit the Al_2O_3 layer that would form the free standing membranes. Both HR3 and HR4 are spin coated with AZ1518 at 3000 rpm for 30 s after an HMDS spin (Figure 3.2.i). The spin coated wafers are prebaked at

Table 3.7: Alphastep profilometer etch depth measurement.

Trial #	3min Sample(Å)	5min Sample(Å)
1	580	1030
2	590	965
3	650	940
Average	607	978

110 ^{o}C for 5 min. The HR3 wafer is patterned with a 30 μm window mask while the HR4 is patterned with a 5 μm window mask. Both wafers are exposed for 75 s with 7.5 W/cm^2 426 nm wavelength UV light. The wafers are developed in 1:1 diluted AZ developer for 75 s. After 2 min hard bake at 125 ^{o}C, the HR3 and HR4 features are approximately 31 μm and 7.5 μm based on the optical microscope eye piece scale (Figure 3.2.j).

The wafers are placed in the Plasma Therm Freon RIE chamber to etch through the passivation layers using the CHF_3 recipe for 5min and CF_4 chemistry for 34 min under 35 mT pressure at a flow rate of 60 sccm at 90 W (Figure 3.2.k). The first 5 min etch goes through the SiO_2 layer. And the 34 minutes etch goes through the silicon nitride layer and hits the Al_2O_3 layer. The fact that the exposed area is really Al_2O_3 is also visually confirmed by the color of the membrane area (Figure 3.5).

The photoresist on the wafer front side is stripped using acetone, methanol and DI rinse (Figure 3.2.l). The process proceeds with a 3 min dehydration bake at 110 ^{o}C. The wafer is spun HMDS at 100 rpm for 30 s and covered with AZ9260. The PR is also spun at 1000 rpm for 30 s (Figure 3.2.m). Since the photoresist had high viscosity, it has to be left on the chuck for 20 min to allow the photoresist to reflow and become uniform. The wafer with the planarized resist is baked for 6 min at 110 ^{o}C and placed on the aligner. The dicing lines that form during the front side etch are used for backside alignment. For the backside alignment, the mask with 30 μm features is used as opposed to 5 μm features. Although it would be desirable to have a smaller exposure of the window area to the electrolyte solution from the backside of the wafer, it would be a daunting task to wet a 5 μm thick, 300 μm long channel. Furthermore, such a channel would constitute very high resistance which would ultimately decrease the bandwidth. The features are exposed for 155 s at 7.5 mW/cm^2 power. The exposed wafer is developed in

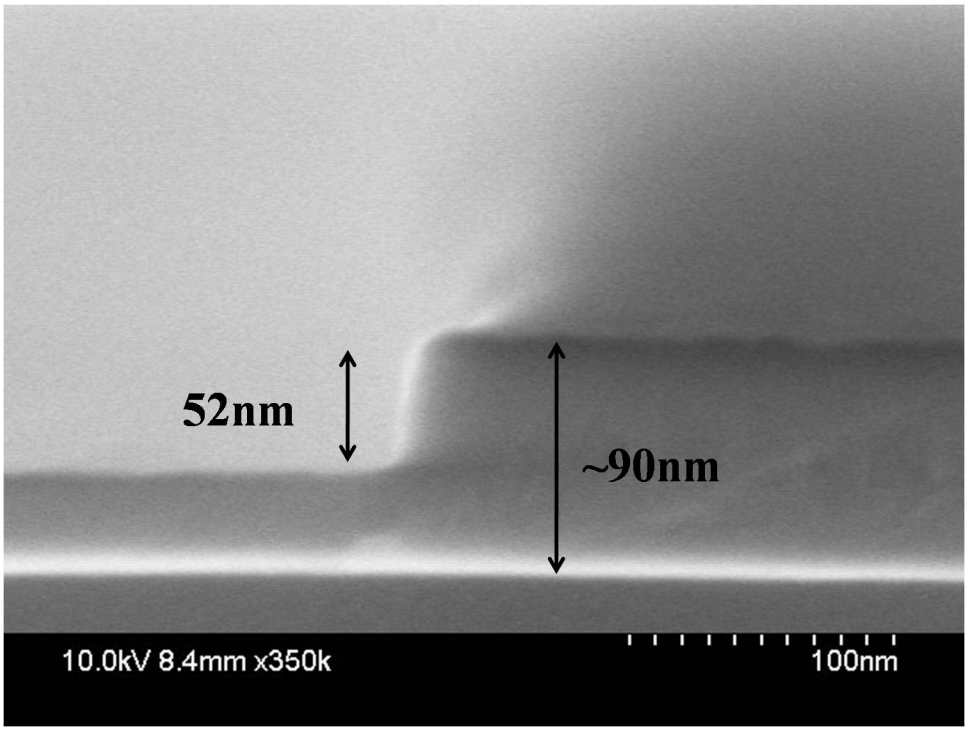

Figure 3.3: After 3 min etch, the SEM image shows that the total etch depth is 52 nm.

4:1 concentration AZ400k developer for 6 min 30 s. The backside lithography is completed with a 30 min 110 ^{o}C hard bake. The features after the hard bake look to be approximately 35 μm (Figure 3.2.n).

Prior to the deep etch, the wafer is O_2 plasma cleaned under 500 mT pressure with 300 W power for 3 min. This step is aimed to clean any residues left from the backside lithography step. The backside oxide is etched with the previously discussed CF_4 recipe for 10 min (Figure 3.2.o).

Since the wafer is going to be etched through the dicing lines and the window area, the integrity of the wafer will be remarkably weakened. Therefore, the wafer is bonded to a 4 in alumina wafer using cool glue, a metal-based, high-heat conductivity paste. After the chamber is cleaned with the commonly employed O_2 plasma cleaning procedure for 10 min, the wafer is loaded into the STS ICP RIE. The wafer is etched for 2 h and 35 min 30 s using a SF_6 Bosch process (Figure 3.2.p). The etch cycle is 12 s long and the plasma is excited at 13.56 MHz frequency with a 130 sccm SF_6 and 13 sccm O_2 flow rate under 36 mT pressure at 12 W. The passivation cycle is 8 s long with a C_4F_8 flow rate of 130 sccm under 18 mT pressure. The membranes are eas-

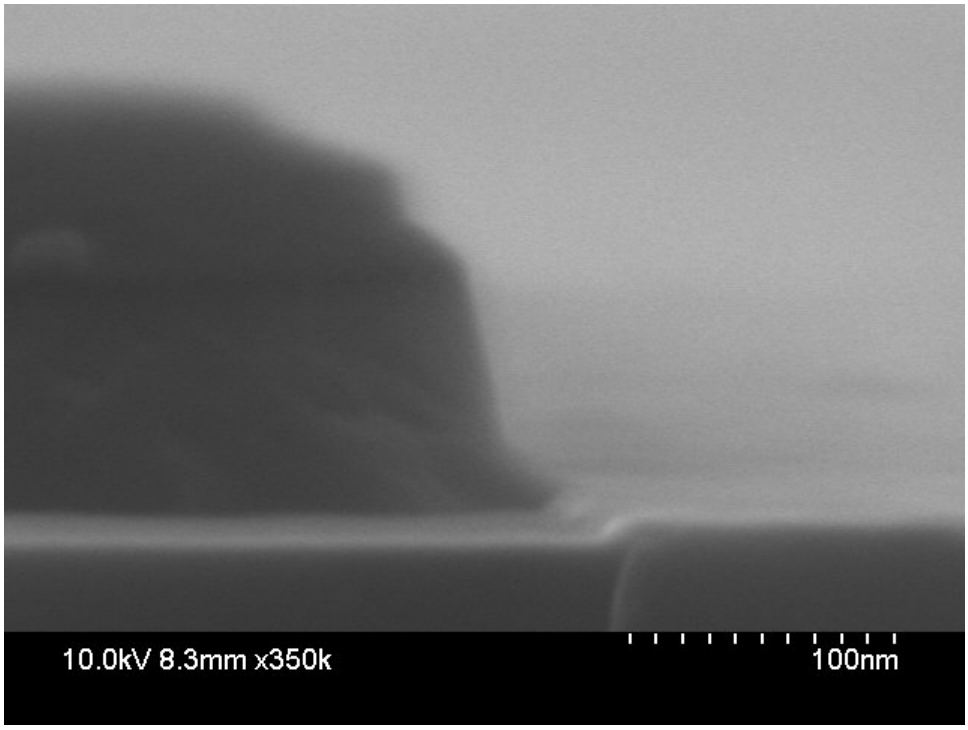

Figure 3.4: After 5 min etch, as can be seen in the SEM image, there is no silicon dioxide left.

ily discernable under normal lighting conditions with an optical microscope. When illuminated with UV light from the back of the wafer, the membranes allows transmission of light under an optical microscope.

The wafer is separated from the alumina wafer using acetone, methanol and DI rinse. The wafer was further cleaned with acetone, methanol and DI after separation from the carrier wafer (Figure 3.2.q).

3.3 Thin Membrane

3.3.1 Motivation

The insensitivity of conduction current to the DNA molecules through the nanopores formed on newly fabricated high resistivity wafers, HR2 and HR3, demands further knowledge about the base material Al_2O_3 as a membrane. Therefore, the investigation of the stability of Al_2O_3 ALD membranes as a function of thickness surfaces is a logical route to take.

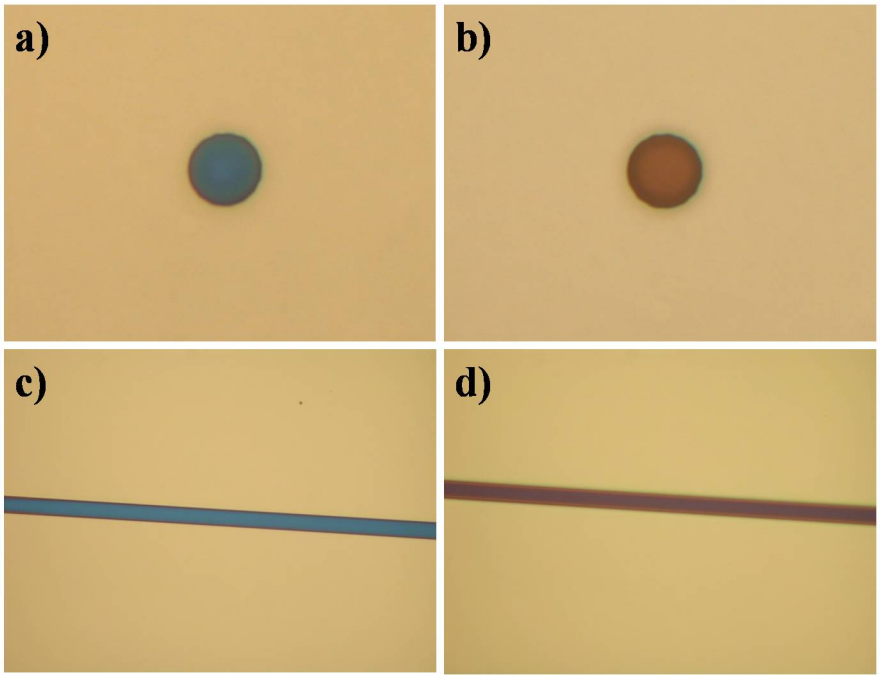

Figure 3.5: a) An incomplete etch where silicon nitride residue is visible over the alumina membrane. b) A complete etch over the membrane area with only alumina layer visible. c) An incomplete etch on a dicing line with silicon nitride residue. d) A complete etch over the dicing line.

3.3.2 Fabrication

During the investigation of the stability of Al_2O_3 ALD membranes as a function of thickness, five different wafers were fabricated. The membranes were formed with 300 μm thick, double-side, polished float-zone wafers. Initial cleaning steps consisted of a 1 min buffered oxide etch (10:1), followed by 10 min of 300 W O_2 clean. Cleaning steps were aimed at removing the native oxide layer and oxidizing the surface in a controlled fashion to prepare the wafer for ALD deposition.

The wafers are deposited with 40 cycles (HR13), 100 cycles (HR14), 200 cycles (HR10), 400 cycles (HR11) and 600 cycles (HR12), all of ALD Al_2O_3 at a wafer chamber temperature of 300 ^{o}C. The wafer with 100 cycles ALD Al_2O_3 is over-etched and the dice do not have an intact membrane. Immediately after the ALD deposition (Figure 3.6.b), the 40 cycles ALD Al_2O_3 deposited wafer (HR13) is deposited 16 s of Si_3N_4 PECVD with a mixed

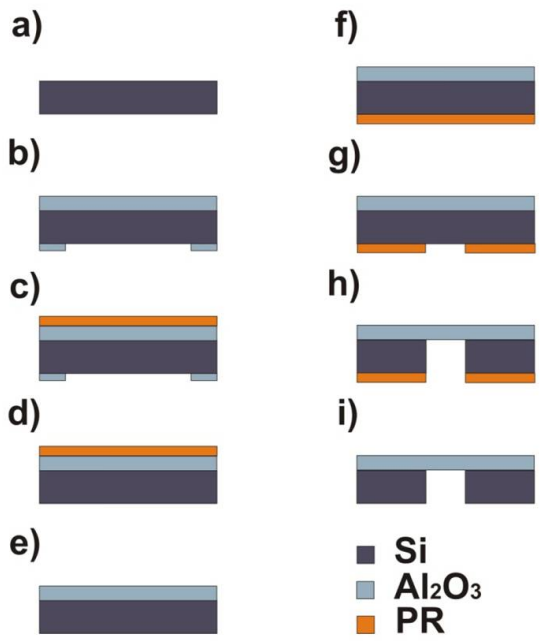

Figure 3.6: Process flow for thin membrane fabrication.

frequency process[1] which yields stress levels lower than 50 MPa. To measure the thickness of the deposited Si_3N_4 accurately with an ellipsometer, a dummy 500 μ thick, 10 Ω cm one-side polished silicon wafer is deposited with Si_3N_4 using the same recipe.

The ALD system deposition bleeds out to rims of the backside of the wafers, as can be seen in Figure 4.1.b (on page 31). Before removing the residue Al_2O_3, the front sides of the wafers are spin coated with AZ1518 positive resist to protect the deposited Al_2O_3 film as in the Figure 3.6.c. After the spin coating process, the wafers are dipped in BOE (10:1) for 10 min. This is a severe over-etch time to make sure aluminum oxide on the backside of the wafer is removed (Figure 3.6.d). This step is of crucial importance, since the Al_2O_3 is a very resistant etch stop for the upcoming RIE process.

The fabrication process is continued by the removal of the photoresist using acetone and methanol, as in the Figure 3.6.e. The backsides of the wafers are spin coated with reactive ion etching resistant AZ9260 positive photoresist

[1] Si_3N_4 deposition recipe:
Equipment: STS PECVD system
Pressure: 900 mT; Temperature: 300 ^oC; NH_3 flow: 40 sccm; SiH_4 flow: 40 sccm
High frequency: 13.56 MHz for 6 s, Low frequency: 380 kHz for 2 s.

(Figure 3.6.f). The PR (photoresist) layer is exposed to 7.5 mW/cm^2 for 500 s with a mask that defines the dicing lines and 30 μm windows as the Figure 3.6.g depicts. The PR film is developed using AZ400K developer to have approximately 35 μm features. The feature size is an estimate based on the optical microscope's measurement utility.

At this step, the wafer is etched with reactive ion etching that uses CF_4 chemistry to break through the newly formed native oxide, which is highly selective compared to silicon. Since the PR has very similar etch selectivity as the oxides and the silicon nitride, the CF_4 etch also cleans up the residues that may be left on the revealed feature areas. This step allows the RIE step with SF_6 chemistry to have more uniformity across the wafer.

After the development of the features, the wafers were fixed to a carrier alumina wafer with Cool-Grease (a high-thermal conductance paste by AI Technology). The wafer is then etched with deep reactive ion etching using SF_6 chemistry with a typical 2.5 μm/min etch rate[2]. Since the dicing lines are also defined along with the membrane features, the mechanical integrity of the membrane wafer is significantly weakened during the DRIE process. This is the primary reason a carrier wafer is required for support of the membrane wafers.

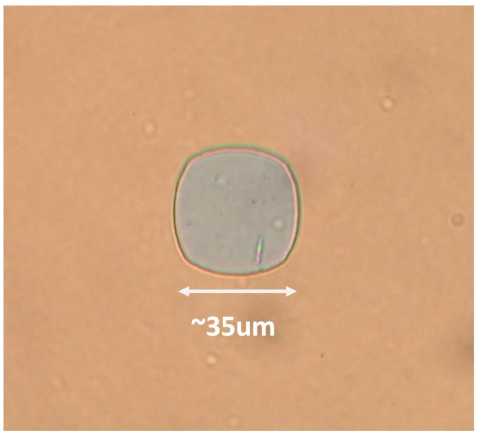

Figure 3.7: An optical microscope image of the HR12 membrane after the DRIE etch.

When the wafer is completely etched through up to the Al_2O_3 film, the

[2]Deep reactive ion etching recipe:
Equipment: STS ICP RIE
Etch step: Duration: 12 s; Frequency: 13.56 MHz; SF_6 flow: 130 sccm; O_2 flow: 13 sccm; Pressure: 36 mT; Power: 12 W
Passivation step: Duration: 8 s; Frequency: 13.56 MHz; C_4F_8 flow: 18 mT; Power: 0 W

features can be discerned by their higher transparency under an optical microscope, as can be seen in Figure 3.7. At this stage, Cool-Grease allows the wafer to be detached from the carrier wafer without the need to use acetone or any other solvent that could potentially harm the PR film. Ultimately that enables the designer to adjust the etch times during a run in cases where the wafer is not completely etched through. In such cases, the wafers were placed back into the DRIE chamber with increments of 1 minute etch times. The variation in the etch times can be due to the wafer thickness difference, the DRIE chamber's daily condition changes and residues that may be left on the features after the photolithography step.

The wafer with 100 cycles (HR14) failed during the DRIE step. There are no intact membranes on the wafer which can be visually discerned by the indication of color difference around the dices sides. After the deep etch process, the wafers are stripped of the PR layer using acetone and methanol, making them ready for testing.

CHAPTER 4

METHODS

4.1 Capacitance Measurements

The bandwidth of the measurement system is one of the fundamental factors that determine the resolution of the DNA sensing method. In a nutshell, the measurement setup should be able to sample at least two times faster than the translocation rate of a single base pair. In order for the measurement setup to have such sampling capability, the nanopore system should have high-enough bandwidth to accommodate high-frequency signals. Therefore, the evaluation of the bandwidth of the nanopore system is essential, as it gives an insight into the theoretical basepair resolution that can be achieved for DNA translocation experiments.

To evaluate the bandwidth, first, a lumped element circuit model is developed. Then the voltage drop across the investigated membrane is measured while sweeping an applied 50 mV AC signal from 2 Hz to 2 MHz. The measurement data is used to fit the model developed earlier in a SPICE simulation based circuit design program by Agilent, Advanced Design System. Fitting the model allows us to extract the values of the circuit components which in turn provides the necessary parameters to calculate the bandwidth of the nanopore system.

4.1.1 Lumped Element Circuit Model

The bandwidth evaluation requires a good grasp of the lumped circuit element model. When immersed in electrolyte solution to perform the DNA translocation experiments, the fabricated nanopore system allows two nodes of electrical excitation, namely the cis and trans reservoirs. An analysis of the topology of the electrical pathways reveals that developing an accurate

lumped element circuit model is an involved process. For demonstration purposes, the HR4 wafer chip topology lumped element circuit modeling will be discussed in detail.

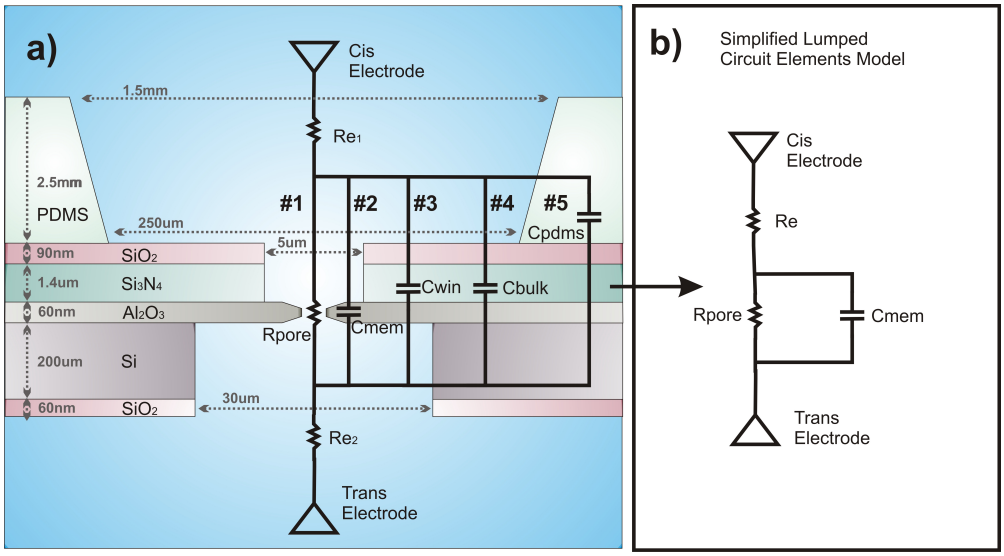

Figure 4.1: a) The topology and lumped element circuit model of HR4 wafer chips. b) Simplified lumped element circuit model.

In the Figure 4.1.a, a lumped circuit element model of the HR4 wafer chips is shown. The CIS reservoir Ag/AgCl electrode is depicted to face a serial resistance due to the electrolyte resistance. After this point, the lumped element model divides into five different current paths. Path #1 is the nanopore resistance or the membrane resistance when there is no pore. Path #2 describes the displacement current through the membrane. Current Path #3 stands for the area where the free standing membrane is covered by a passivation layer. The "Cwin" capacitor on this path is associated with the silicon nitride passivation layer which is also the dominant and the smallest capacitive element on this current path. As the parallel resistance of the silicon nitride layer is on the order of 10s of gigaohms, the displacement current path is dominant for the measurement frequencies of interest. Therefore, a parallel resistance is not depicted in Path #3 in Figure 4.1.a. Path #4 corresponds to the electrolyte-exposed surface area of the chip that is above the bulk silicon. As in Path #3, the dominant circuit element,"Cbulk" is associated with the passivation layer. In Path #5, the current path through the PDMS is modeled with a capacitor. All of these paths converge again and continue to the trans reservoir electrode through the electrolyte serial

resistance.

This model can be further simplified to the form in Figure 4.1.b which lumps the capacitive elements “Cmem”, “Cwin”, “Cbulk” and “Cpdms” into “Cmem”. This simplification can be justified by taking into account that the capacitance of Path #3, Path #4 and Path #5 are negligible compared to the membrane capacitance. It is also convenient for simulation and extraction of circuit parameters based on the measurement data.

4.1.2 AC Measurements

During the AC sweep measurements a Signal Recovery 7280 lock-in amplifier is used. A lock-in amplifier works on the basis of comparing the magnitude and phase of the excitation signal and output signal of a circuit. This is done by providing the lock-in amplifier a reference signal which is also usually the excitation signal for the measured circuit. The output of the circuit is also provided to the lock-in amplifier. The amplifier matches the reference signal's frequency with an internal oscillator and takes the difference between the output of the measured circuit. As the matching of the internal oscillator to the reference signal is of utmost importance for the accuracy of the measurement, the internal oscillator of the lock-in amplifiers is designed to be very high-fidelity. Consequently, the lock-in amplifier oscillator output can also be utilized as the reference signal that is used to excite the measured circuit.

The amplifier oscillator output is connected to the CIS reservoir and the input port A is connected to the trans reservoir Ag/AgCl electrodes. The input port A has an input impedance that can be described with a 100 MΩ resistance in parallel with a 25 pF capacitance. For electrode contacts approximately 3 feet long, BNC cables are used.

The amplifier is interfaced with Labview code through the GPIB port. The online provided driver script is modified to update the time constant and the frequency and write the measurement values to a text file.

Using the above setup, the nanopore system is applied an AC signal with 50 mV magnitude while sweeping the frequency from 2 Hz to 2 MHz in 256 logarithmically increasing steps.

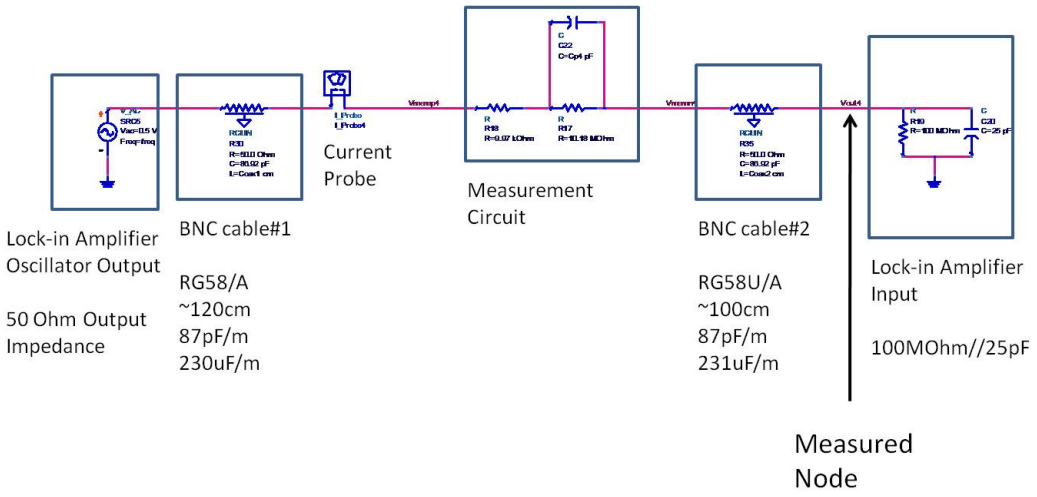

Figure 4.2: SPICE model of the measurement setup.

4.1.3 Advanced Design System and Calibration

As the measurement system is not a four-point probe setup, the impedance of used cables needs to be accurately accounted to extract the lumped element circuit parameters. Therefore, the model circuit needs to be calibrated according to the cables used and the input impedance of the lock-in amplifier. This is done by measuring components with known values using the same AC signal sweep from 2 Hz to 2 MHz (Table 4.1).

All the known components in the measurement setup are accounted in the SPICE model. As in Figure 4.2, the BNC cables are depicted with transmission lines with resistance, capacitance and inductance values. The oscillator output of the lock-in amplifier is an AC signal voltage source. The "A" input of the amplifier is represented by a 25 pF capacitor in parallel with a 100 MΩ resistor, as the manual for SR7280 states. The calibration involves pinning down the BNC cable parameters, so that they can be used in fitting the model to the data for circuits with unknown component values.

The data is imported to the Advanced Design System and the model is simulated with the same frequencies as the data provided. The simulation results are designed to be converged to the reference data by adjusting the parameter associated with the BNC cables using a gradient approximation algorithm. As can be seen in the sample fit in Figure 4.3, the data and the results are in very good accordance with each other.

Table 4.1: BNC cables calibration circuits.

Circuit #	Rs(Ω)	Rp(Ω)	Cp(pF)
1	10 k	10 M	50
2	10 k	10 M	20
3	10 k	10 M	5
4	10 k	10 M	1
5	10 M	-	-
6	1 G	-	-

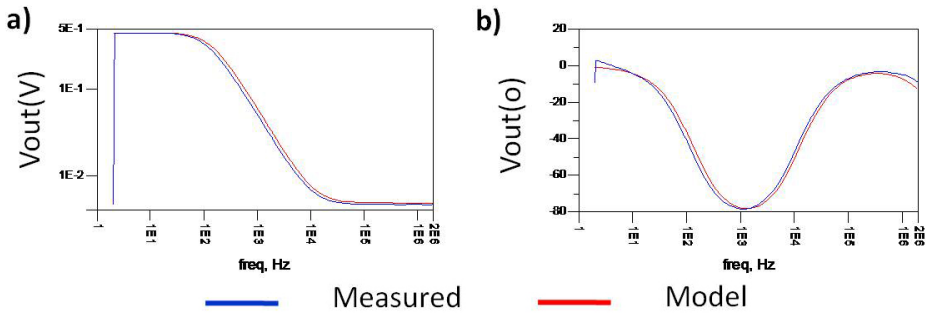

Figure 4.3: SPICE model calibration fits for circuit #2. a) Magnitude of the recorded signal at the input of the SR7280. b) Phase of the recorded signal at the input of the SR7280.

4.1.4 Modeling and Simulation

The Path #5, Path #4 and Path #3's capacitances are negligible compared to Path #2. Therefore, for bandwidth investigation purposes, the model can be reduced to a simple serial resistor and a parallel resistor to the membrane capacitance. The serial resistor stands for the electrolyte resistance while the parallel capacitance accounts for the displacement current around the exposed membrane area. On the other hand, the parallel resistance describes the pore resistance or, if there is no pore, the leakage current through the membrane. For fitting purposes, the values of these components are set to vary between 50% and 200% of the theoretical values.

The measurements are done at the input of the lock-in amplifier. Therefore, the measurement data reflects the voltage drop across the input of the lock-in amplifier with 100 MΩ resistance and 25 pF capacitance. It can be thought of as a voltage divider rule, where if a 50 mV signal is applied to the nanopore circuit and the input of the lock-in measures 25 mV, then the

impedance of the input of the lock-in and the impedance of the nanopore micro-fluidic system is similar in magnitude.

4.2 Membrane Assembly for Nanopore Experiments

The membranes are cleaned with piranha (3:1) solution for 3 min. In addition to its cleaning properties, piranha solution is commonly used for increasing the interaction of the DNA molecules with the pore [48, 49]. Although some of the tested membranes did not have pores, they were strained with the same conditions that a membrane with pores for DNA testing would have to withstand.

The cleaning process is followed by alignment of our house-made gaskets with the 250 μm opening to the membrane area of the chip. The 2 mm thick PDMS gaskets were designed with a sticky cellulose layer that provides excellent sealing for the membranes. When a membrane binds to a gasket, the membrane cannot be taken apart without the use of excessive mechanical stress. This feature of the gasket is both an advantage and a disadvantage in the sense that it makes it harder to examine the membranes after a failure. Under the application of such a high stress level, the membrane may not have an intact membrane. Therefore, what caused the membrane to lose its integrity after the disassembly of the setup (either the experiment or the disassembly itself) is unknown.

The membranes were put into a Teflon holder in creating two separate reservoirs: cis and trans. The assembly involves the distribution of a thin layer of vacuum grease on the gasket's surface that binds to the holder. When the vacuum grease adheres to the Teflon holder, it is easy to evaluate the seal by observing the interface between the gasket and the Teflon holder through the transparent gasket. When there is a breach in the seal, shiny air pockets form at the interface. These pockets can be remedied easily by the application of even force around the area of the breach, which in turn, causes the vacuum grease to fill those gaps and push the air pockets out of the interface.

Afterwards, the membrane's back and front is exposed to 100 W O_2 plasma for 42 s with 8 sccm O_2 flow. The O_2 plasma makes the surface of the membrane highly hydrophilic, promoting the wetting of the membrane area

from the back side and front side of the chip. Without the use of O_2 plasma, the 200 μm long and 35 μm x 35 μm footprint window from the back side of the chip would inevitably trap micro-bubbles which would occlude the contact of electrolyte with the membrane.

First, the membrane is wetted with methanol which has a lower surface tension than water to reduce the possibility of trapping air bubbles around the membrane region. Then, the membrane is submerged into the electrolyte in the holder and vacuumed in a dessicator chamber to extract the remaining bubbles. The electrolyte solution's configuration is 1 MKCl 10 mM Tris and pH 8.0.

CHAPTER 5

EXPERIMENTS

5.1 Preliminary Data with Test Wafer 10

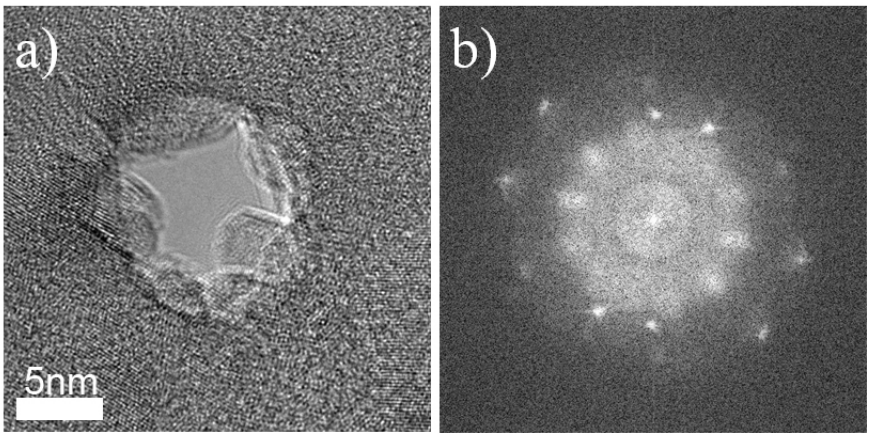

Figure 5.1: Pore on test wafer 10 membrane #22. a) The effective radius of the pore is 4.3 nm. b) The fast Fourier transform of the pore image shows the nanocrystalline nature of the alumina around the pore area.

Test wafer 10 (TW10) is a membrane wafer with 700 cycles of ALD alumina deposition and silicon nitride passivation layers. The passivation layer has a 30 μm window that exposes the alumina layer. The membrane stack is formed on a 10 Ω-cm 100 orientation 4 in wafer. From this wafer, Membrane #22 is drilled using e-beam sputtering in CBD mode at 1.6 nm spot size with alpha set to 9 (Figure 5.1.a) on JEOL 2010F FEG TEM. As can be seen in Figure 5.1.b, during the drilling process nanocrastalline structures form around the pore area on the alumina layer. These structures were further investigated by my colleague Bala Murali Venkatesan (LIBNA group member) and claimed to have improved mechanical stability.

After a PDMS gasket is adhered to the membrane and assembled to the structure, it is immersed in the 1 MKCl electrolyte solution. In Figure 5.2,

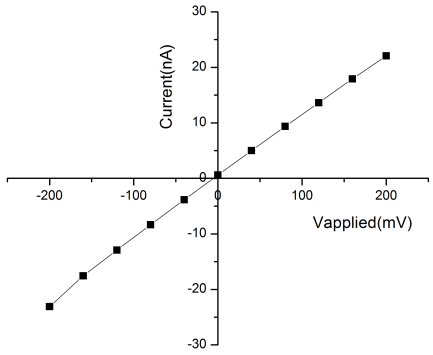

Figure 5.2: Test wafer 10 membrane #22 IV curve with 1 M KCl 10 mM Tris pH 8.0 electrolyte solution.

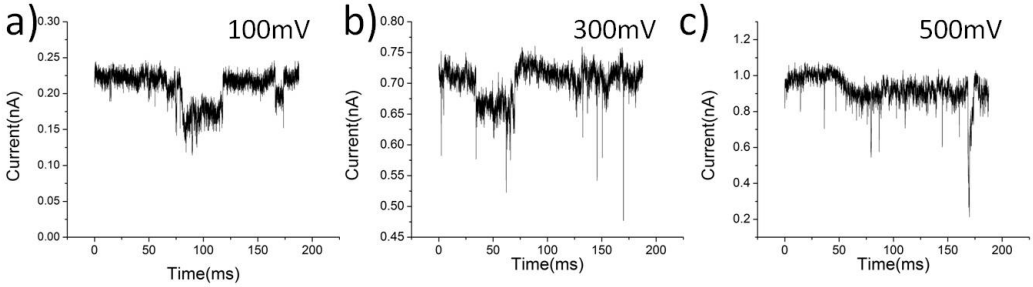

Figure 5.3: Test wafer 10 membrane #22 5 kbp dsDNA translocation experiments at a) 100 mV, b) 300 mV and c) 500 mV.

the IV curve of the immersed membrane is shown. The pore current is linear and does not show hysterisis, which confirms that the membrane is stable and ready for DNA translocation experiments. Then 5 kbp dsDNA is introduced into the cis reservoir. Using the Axopatch system, the current traces at 100 mV, 300 mV and 500 mV applied DC voltage are recorded at 200 kHz sampling rate with a 100 kHz lowpass filter imposed by the hardware itself (Figure 5.3). The current traces show modulations caused by DNA translocation through the nanopore.

The modulations show patterns in coherence with the electrical potential difference between cis and trans reservoirs. The events are analyzed using an automated algorithm (Appendix B). The scatter plots of events show that as the applied DC voltage increases the current blockage ratio increases along with a decrease in the translocation times (Figure 5.4). Based on the analy-

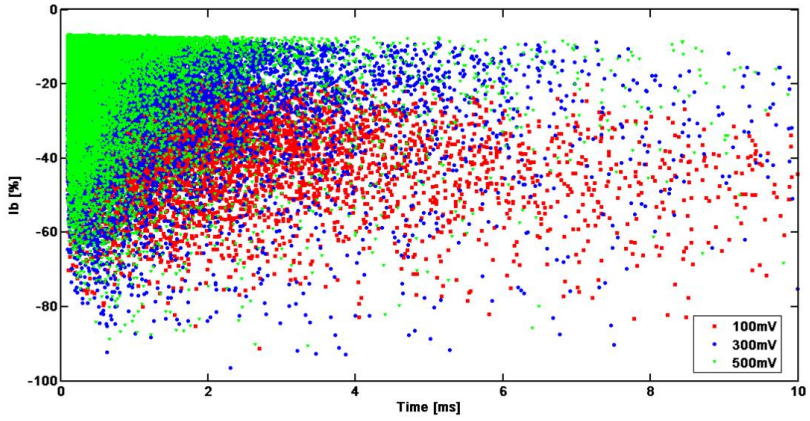

Figure 5.4: Test wafer 10 membrane #22. Scatter plot of the events in terms of current blockage ratio versus translocation time.

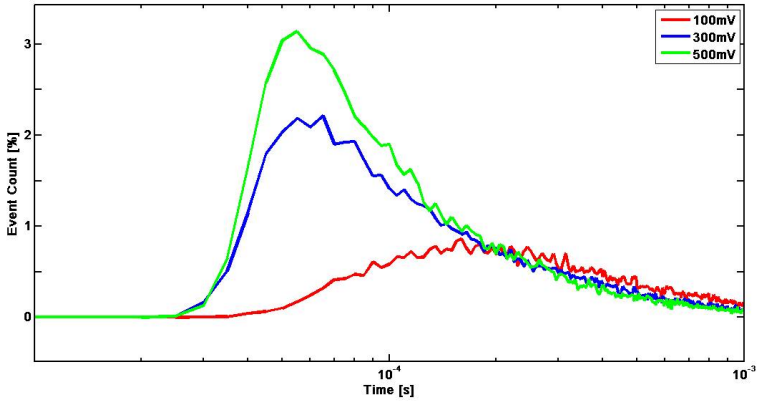

Figure 5.5: Test wafer 10 membrane #22. Normalized event translocation time histogram in terms of percentage.

sis data, the translocation rate at 100 mV can be estimated to be 25 bp/μs. Therefore, in order to resolve the charge associated with a single nucleotide, the measurement system bandwidth needs to be at least 50 MHz. When examining at the histogram of the 100 mV data in Figure 5.5, the translocation time may be surmised to produce a Gaussian distribution. Following this assumption, the higher voltage measurements would also show a greater rate of translocation expected value, with a sharper Gaussian distribution. Due to the limitations of the current amplifier, the Axopatch 200B system, the minimum sampling interval is 5 μs, which occludes further analysis of the distribution at higher voltages. The fits accomplished using a Gaussian distribution formula on the 300 mV and 500 mV data histogram curves are

not accurate enough to make reliable estimations at higher voltages than 100 mV.

5.2 High Resistivity Wafers

5.2.1 Noise and Capacitance Measurements

The new improved topology of high resistivity wafers improves upon the capacitance of the TW15 membranes. The thicker passivation layer, updated gasket design and float zone wafer handle increases the insulation thickness between the cis and trans reservoirs while keeping the thickness of the membrane itself the same. These modifications result in a lower noise and higher bandwidth, which would ideally allow shorter DNA strands to be resolved at a time.

The simplified SPICE model is used to extract the parameters from AC sweeps of the membrane system. When a comparison between the capacitance values is done as in Table 5.1 between LR1[3], TW15 and HR5, it becomes apparent that the new topology of high-resistivity wafers is superior to its predecessor versions (Figure 5.6).

The improvement in capacitance also improves the bandwidth. As can be seen in the bandwidth of simulations (Figure 5.7), the 3 dB point of HR5 wafer membranes are almost 1.5 times higher than TW15 and almost an order of magnitude better than the LR1 wafer membranes. This improvement in the bandwidth also manifests itself in the form of lower noise in Figure 5.8.

Table 5.1: Simulation results for circuit parameters of LR1, TW15 and HR5.

Wafer	Rs(kΩ)	Rp(GΩ)	Cp(pF)
LR1	0.79	99	3009
TW15	4.7	104.7	54.4
HR5	27.3	0.057	15.23

[3]Low resistivity wafer 1:
700 cycles of ALD Al_2O_3 on 4 in. 10Ω-cm wafer with no passivation layer.

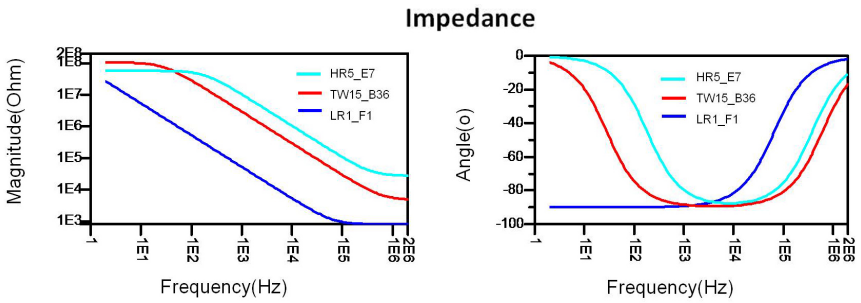

Figure 5.6: Impedance comparison of high resistivity wafer, test wafer 15 and low resistivity wafer.

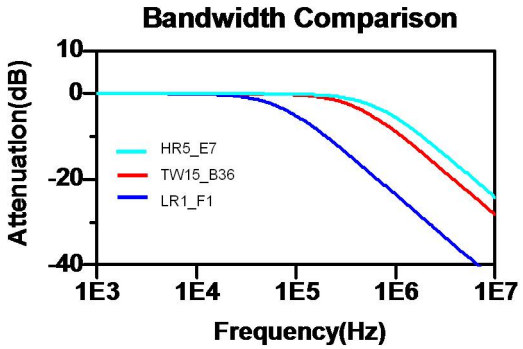

Figure 5.7: Bandwidth comparison of high resistivity wafer, test wafer 15 and low resistivity wafer.

5.2.2 DNA Translocation Experiments

DNA translocation experiments are done with DNA molecules that varied from 993 bp to 3.5 kbp. Relatively low number of membranes yield expected current levels for the used electrolyte concentration. Furthermore, the membranes that show modulation with DNA translocation have low blockage ratios and longer than expected events.

The low blockage ratio of the events can be hypothesized to be caused by the weakened alumina layer after e-beam sputtering. The pore area becomes significantly thinner than the rest of the membrane and more prone to electrolytic leakage. Therefore, the pore itself may not be the only DC conduction path between the cis and trans reservoirs.

On the other hand, the experiments with insensitivity to DNA translocation may be explained by the low capture radius of the pore area due to the

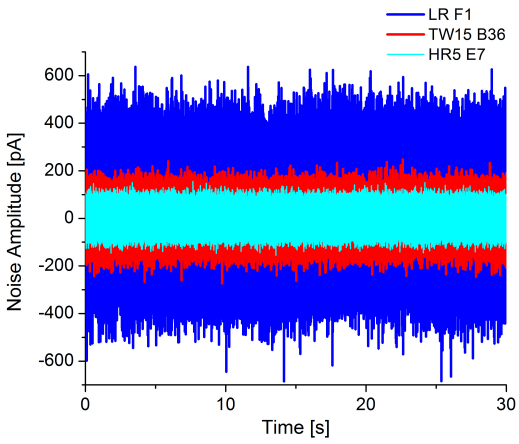

Figure 5.8: Noise comparison of high resistivity wafer, test wafer 15 and low resistivity wafer.

salt concentration. As the Meller group points out, a gradient of low salt concentration in the cis reservoir and high salt concentration in the trans reservoir can yield a higher yield of DNA interaction with the nanopore.

HR5 E21

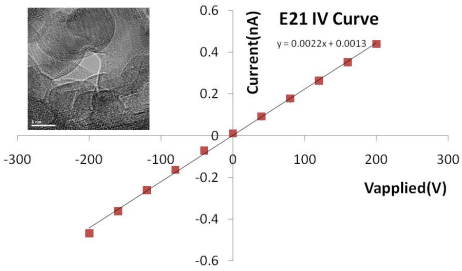

Figure 5.9: HR5 E21 IV curves and HRTEM pore picture.

The membrane is drilled a 4.4 nm effective diameter pore using a JEOL 2010F FEG TEM with the focused e-beam sputtering technique (Figure 5.9 inset). The membrane is immersed in to 0.1 MKCl 10 mM Tris pH 7.5 electrolyte solution and the IV curves of the membrane are taken (Figure 5.10). Following the stabilization of the current conduction, the cis reservoir is introduced with 3.5 kbp dsDNA which resulted a final 42 aM concentration in the cis reservoir. Current traces are recorded at 100 kHz hardware lowpass

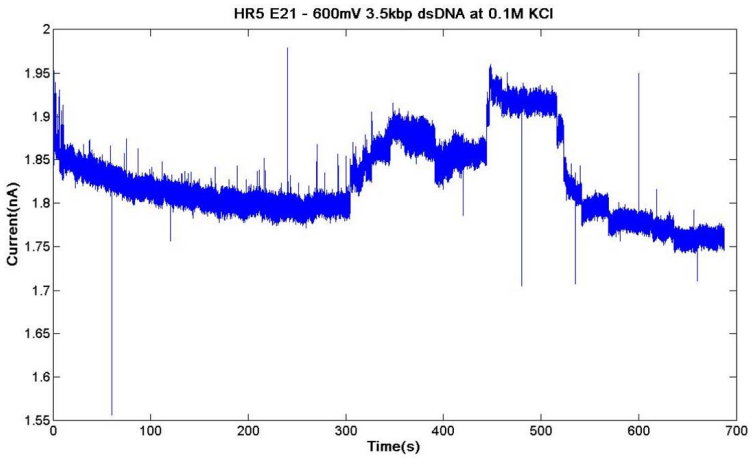

Figure 5.10: Sample current trace from the HR5 E21 membrane.

filtering with 200 kHz sampling rate for 10 min at various voltages.

As can be seen in the sample current trace, the current blockage ratio associated with DNA translocation is about a maximum of 10% and the current modulation is on the order of 10 s at a time. These results do not produce a pattern that allows further investigation.

HR5 E40

The membrane is drilled a 4.33 nm effective diameter pore using a JEOL 2010F FEG TEM with the focused e-beam sputtering technique (Figure 5.11 inset). The membrane is immersed in a 1 MKCl 10 mM Tris pH 8 electrolyte solution, and the IV curves of the membrane are taken (Figure 5.11). Following the stabilization of the current conduction, the cis reservoir is introduced with 993 bp dsDNA which resulted a final 10 mM concentration in the cis reservoir. Current traces are recorded at 100 kHz hardware lowpass filtering with 200 kHz sampling rate for 10 min at various voltages.

As can be seen in the sample current trace, the current blockage ratio associated with DNA translocation is about a maximum of 5% and the current modulation is on the order of 10 s at a time (Figure 5.12). These results do not produce a pattern that allows further investigation.

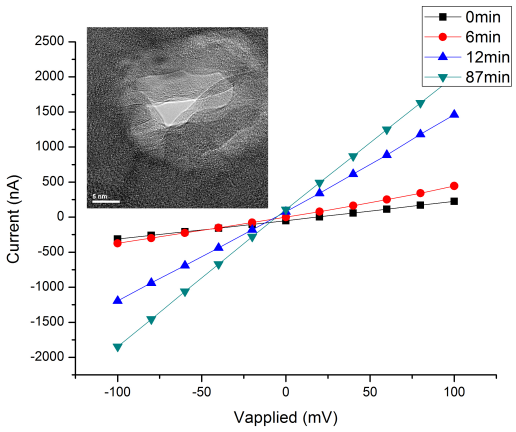

Figure 5.11: HR5 E40 IV curves at several time intervals and HRTEM pore picture.

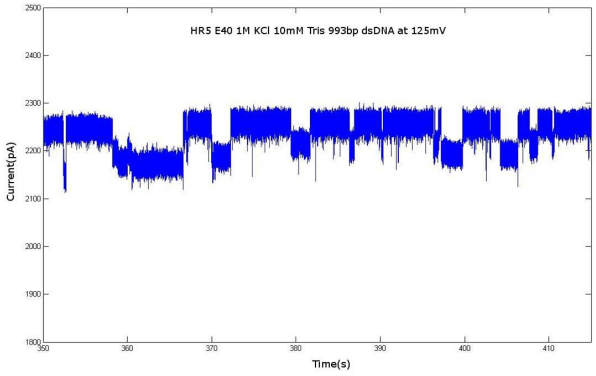

Figure 5.12: Sample current trace from HR5 E40 membrane.

5.3 Thin Membrane Wafers

5.3.1 Materials Analysis

The thickness and the material composition of the ALD films are investigated using electron energy loss spectroscopy (EELS). EELS is a technique that analyzes the energy loss of electrons that penetrate through a thin sample. Every material has a unique energy loss spectrum that provides the researcher with the information to deduce the material composition. During the measurements, the thicknesses of the samples are determined by calculating the ratio of electrons that penetrate through the membrane with zero energy loss (the area colored with red in Figure 5.13) to the total number

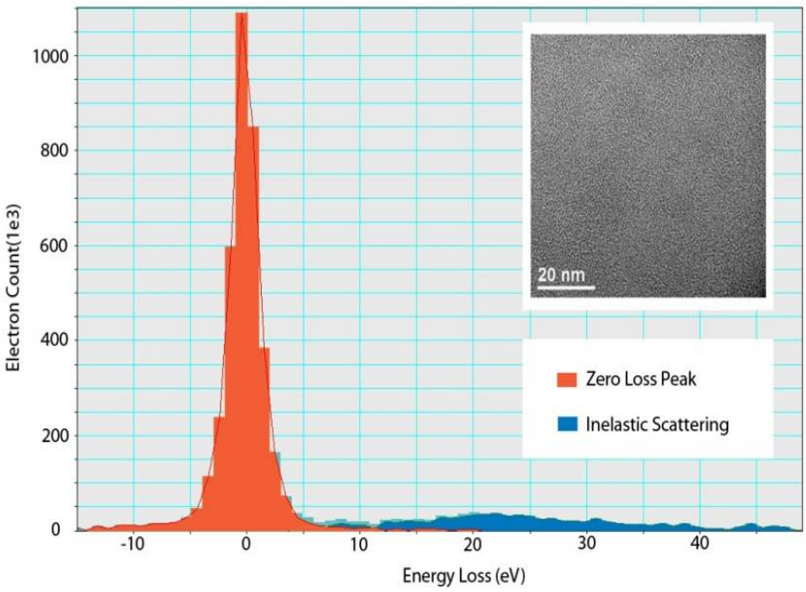

Figure 5.13: The area colored with red shows the electrons that do not lose energy while crossing through the membrane. The blue area shows the number of electrons that lose energy through inelastic scattering. Inset: A high resolution transmission electron microscope image of the area under analysis.

of electrons that are collected. This parameter corresponds to the thickness of the sample in units of inelastic mean-free path of electrons through the analyzed material. In this case, the inelastic mean free path of Al_2O_3 layer is 140 nm. In Table 5.2, the initial measurements are taken with an ellipsometer, while the final measurements are taken using the EELS technique. The thickness differences between initial and final thicknesses are due to the over-etch that occurs during the DRIE etch.

Table 5.2: Sample thickness measurements.

Wafer	ALD cycles(#)	Initial(nm)	Final(nm)
HR10	200	23.5 +/- 0.2	11.9 +/- 0.7
HR11	400	44.0 +/- 0.3	33.13 +/- 6.6
HR12	600	63.6 +/- 0.3	N/A
HR13	40 + 16 s Si_3N_4 PECVD	9.0 (5.7+3.4) +/- 0.3	8.2 +/- 0.6
HR14	100	N/A	N/A

5.3.2 IV Curves

The current through the blank membranes was measured at 0 V and 50 mV, using the Axopatch200B. In addition, continuous IV measurements were taken for the cases where the membrane resistance was above 100 MΩ at 1 M KCl electrolyte concentration (Figure 5.14). A pore below 2 nm in diameter would not readily allow the translocation of a double-stranded DNA molecule which is 2.3 nm in diameter, approximately. The 100 MΩ impedance is also the expected impedance of a 2 nm pore. Therefore, 100 MΩ impedance is an agreeable lower limit for considering the membrane for further investigation.

As can be summarized from the presented results in Table 5.3, the alumina membranes below 30 nm thickness had limited stability in 1 M KCl concentration. The instability of the membranes can be attributed to the weakness of alumina against KCl solution.

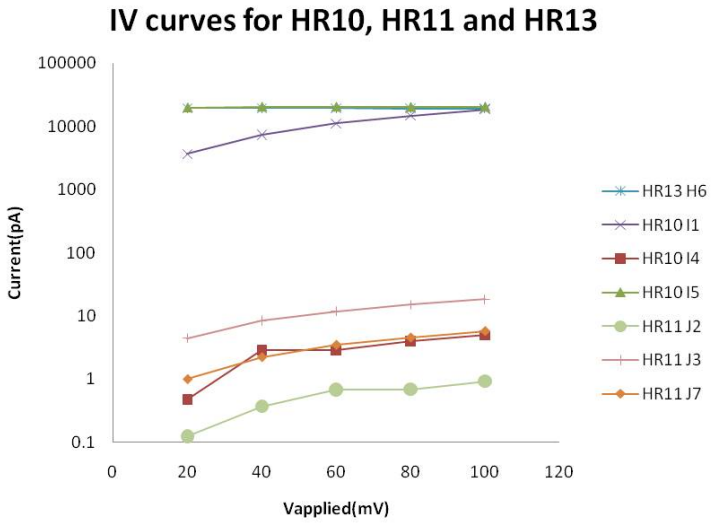

Figure 5.14: IV curves for three different thickness ALD alumina membranes.

Table 5.3: Stability of ALD alumina membranes as a function of thickness.

Wafer	Final Thickness(nm)	Trials(#)	Stable(#)	Failed(#)
HR13	8.2 +/- 0. 6	5	0	5
HR10	11.9 +/- 0.7	6	1	5
HR11	33.13 +/- 6.6	4	4	0

CHAPTER 6

CONCLUSION

The stability and bandwidth of structures for nanopore sensing is investigated in various stack configurations. Membranes with various thicknesses of Al_2O_3, Si_3N_44 and SiO_2 stack configurations are fabricated. The fabricated membrane material properties are analyzed and the membranes are drilled through by focused e-beam sputtering in TEM. The membranes are assembled between cis and trans reservoirs and immersed in 0.1 M and 1 MKCl solutions. The assembled membranes are tested for AC response, noise level and IV characteristics. The membranes with stable conduction are further tested with DNA translocation experiments. The membranes with improved insulation (HR5 wafers) yield low sensitivity to DNA translocation during the experiments. This may be explained by too high salt concentration that signficantly decreased the capture radius. The membranes that show modulation with DNA translocation have low blockage ratios which may be attributed to weakened membrane structure that becomes prone to electrolytic leakage. The knowledge gathered from this experience helps the design of new wafers with a ZrO_2 layer and electrodes that would enable tunneling current measurements in the updated versions.

The membranes were tested in 0.1 M and 1 M KCl solutions for IV characteristics, noise level and AC response. The membranes with desirable noise and IV characteristics were further tested for DNA sensing purposes. The membranes featuring Al_2O_3 insulating layer configurations yielded low noise, high bandwidth and limited durability in KCl solutions. The low yield in DNA sensing in 1M KCl solutions using these architectures form the background and motivation for next generation structures for DNA sensing.

APPENDIX A

ASYMMETRIC PATTERNING

A.1 Motivation

This project is done in collaboration with Prof. Hsia's group from the Mechanical Engineering Department at the University of Illinois. The purpose of the project is to form three dimensional structures that would utilize hydrophobicity to direct fluids in desired directions. In theory, when such a surface is tilted, it may be more favorable for a water droplet to move up the slope instead of downwards, as gravity dictates. Due to the topology, such a displacement may provide a lower energy level. In order to test this idea, the fabricated geometry is 10 μm by 10 μm pillars with 10 μm gaps among them with a depth of 40 μm.

A.2 Asymmetric Patterning Fabrication

The fabrication of the discussed geometry is formed by an initial oxide growth on the wafer. This is followed by patterning the oxide to provide the mask for the deep silicon etch to form the pillars. After pillars are formed, they are oxidized a second time to protect the sidewalls of the pillars. The procedure is followed by the removal of the oxide on the tips of pillars to expose the silicon for angled etch. The dice are attached to a tilted pyrex platform and etched a second time to shape the tips of the pillars. Finally, the dice are dipped in BOE to remove the surrounding oxide, revealing the pillars with tilted tips.

Based on the results of several tries with AZ1518 PR, it can be concluded that the hard mask is the better approach to form the pillars for two main reasons. The PR mask causes micrograss formations due to the masking of

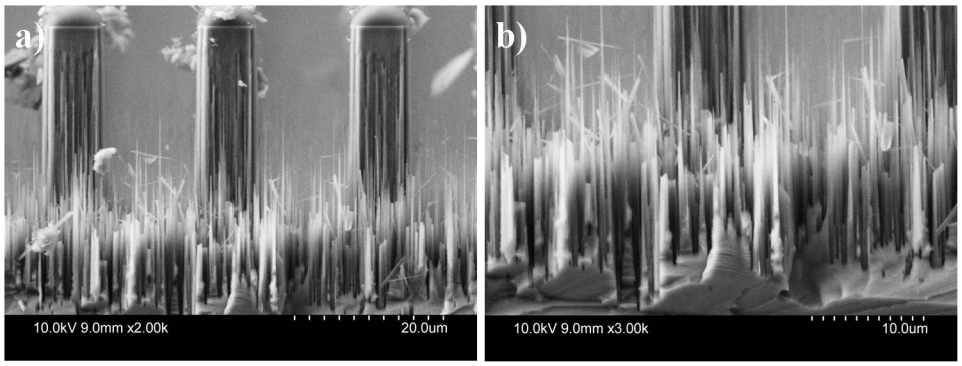

Figure A.1: a) SEM image of the pillars formed using AZ1518 PR. b) Close-up of the base of pillars; the PR mask causes micrograss formation.

sputtered particles during the inductively coupled plasma etch, as can be seen in the Figure A.1. In addition, after exposure to the RIE, the AZ1518 PR proves to be hard to remove from the wafer. Therefore, due to its integrity and desirable 100:1 selectivity against silicon in the STS ICP RIE system, thermal oxide turns out to be the choice that provides the best results.

A 500 μm thick, single-side polished 100 orientation 4 in. wafer with a 10 Ω-cm resistance wafer is piranha-cleaned for 10 min before processing. The wafer is placed in the furnace for 20 min in dry oxidation and 60 min wet oxidation at 1100 ^{o}C to form a 500 nm oxide layer (Table A.1).

Table A.1: Ellipsometer measurements for initial thermal SiO_2 layer.

Location #	Thickness (Å)	Fit Error	Refractive Index
1	4911.907	1.458	0.345
2	5002.128	1.464	0.295
3	4861.199	1.443	0.282
4	4901.478	1.459	0.335
5	5188.863	0.1462	0.306
Average	4973.115	1.194	0.312

The oxide layer is patterned to provide the mask for the deep silicon etch. After a HMDS spin, the wafer is spun AZ 1518 PR at 3000 rpm for 30 s. A 5 min 110 ^{o}C prebake is followed by a 75 s exposition using a mask, featuring 10 μm by 10 μm squares with 10 μm spacing in the x and y directions from each other (Figure A.2). The PR pattern is developed in 1:1 diluted AZ Developer for 65 s. The lithography is completed with a 3 min hardbake at

110 ^{o}C. The features are approximately 8 μm after the lithography.

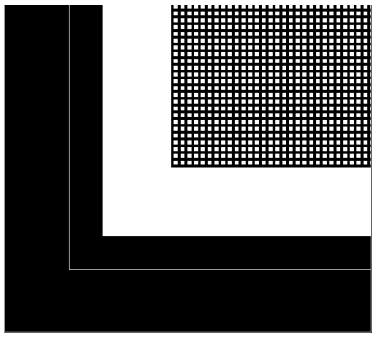

Figure A.2: The mask image for the left bottom corner of a die where 10μm by 10μm features can be seen.

The pattern is transferred to the oxide by etching the wafer in the Plasma Therm Freon RIE system. The wafer is etched for 30 min with CF_4 chemistry under 35 mT pressure at a flow rate of 60 sccm at 90 W. Based on the previous etch characterization, the etch rate is 21.3 nm/min on the thermal oxide. The measurements for the characterization are taken with the Alpha Stepper profilometer. The resist is stripped using acetone and methanol. The wafer is further cleaned in piranha solution for 10 min prior to the deep reactive etching. The transferred oxide feature is approximately 6.7 μm and the depth of the etch varies between 697.5 nm to 724.5 nm which is enough for revealing the silicon, as can be seen in the Figure A.3.

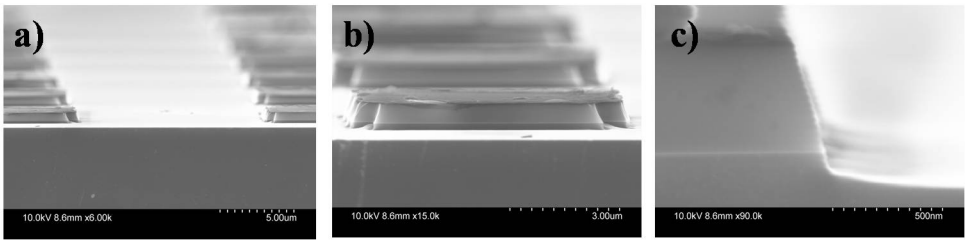

Figure A.3: a) The patterned silicon oxide serves as the mask for the DRIE step. b) The feature size is approximately 8 μm. c) The 500 μm oxide is etched through.

The STS ICP RIE advanced silicon etcher system chamber is cleaned with O_2 plasma for 10 min to prevent micrograss formation due to residues from previous processes. Afterwards, the wafer is etched for 12 min with a SF_6 Bosch process recipe. The etch cycle is 12 s long and the plasma is excited at 13.56 MHz fequency with a 130 sccm SF_6 and 13 sccm O_2 flow rate under

36 mT pressure at 12 W. The passivation cycle is 8 s long with a C_4F_8 flow rate of 130 sccm under 18 mT pressure. The anisotropic etch was followed by a 1 min isotropic etch to clean the possible micrograss formations. This process produces 28 μm tall pillars with no micrograss, as can be seen in the Figure A.4.

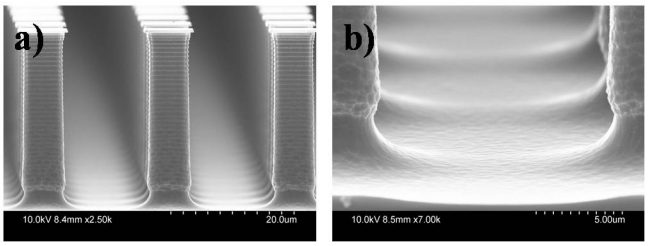

Figure A.4: a) The SEM images of pillars after the DRIE step to form the pillars. b) The base of the pillars does not have any micrograss formation.

The wafer is oxidized a second time to protect the sidewalls during the angled etch. The pillars are oxidized in the oxidation furnace at 1100 ^oC with 20 min dry and 20 min wet setting. The oxide thickness is 370 nm, which is confirmed with ellipsometer and SEM images (Figure A.5).

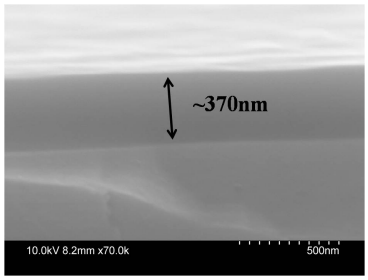

Figure A.5: 20 min dry thermal oxide thickness is 370 nm.

The oxide layer at the top of the pillars is removed to expose the silicon using a Plasmatherm Freon RIE with a CHF_3 chemistry under 35 mT pressure at a flow rate of 60 sccm at 90 W. CHF_3 has higher selectivity for silicon than oxide. As can be seen in Figure A.6, the etch reveals a 32 nm silicon layer underneath the oxide. According to the Alphastep profilometer characterization, the etch rate of CHF_3 is 14.5-15 nm/min of oxide. Based on these data, the oxide is etched for 28 min. The thickness of the revealed silicon is approximately 40 nm. At the skirts of the pillars, the color difference between the silicon and oxide also confirms that the revealed area on the top of the pillars is only silicon (Figure A.6). From the top-down perspective

picture, it is noticeable that the areas around the pillars are free of oxide. The revealed areas are the parts that are etched during the tilted etch.

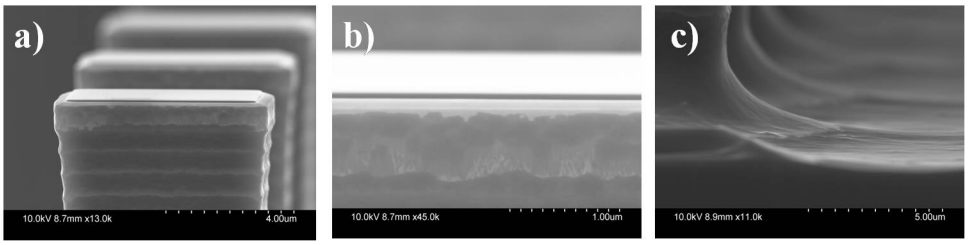

Figure A.6: a) The top of the pillar after the silicon is exposed. b) The revealed oxide is 32 nm thick. c) The base of pillars shows variation in color, confirming the removal of oxide also at the base of the pillars.

At this point in the process, the pillars are ready for the tilted etch. As the STS ICP RIE chamber can only take samples with a maximum height of 5 mm, the wafer is diced to 7 mm by 7 mm dice. The dice are glued to a 45^o angle pyrex ramp using Cool Grease by AI Technoloy (Figure A.7). The pyrex ramp is attached to a 4 in alumina carrier wafer and loaded to the STS ICP system.

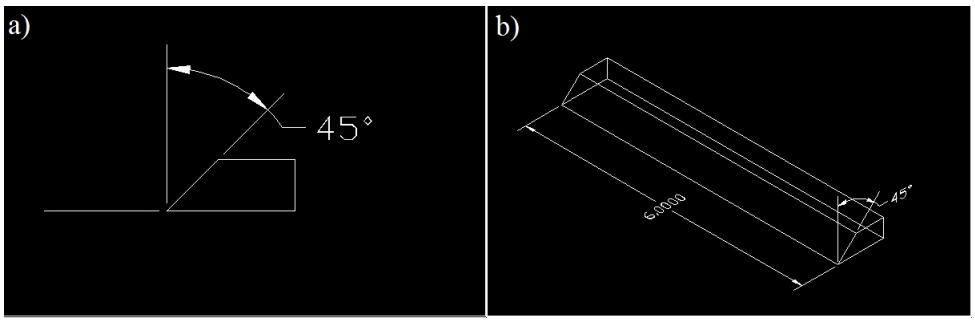

Figure A.7: The pyrex ramp used for attaching the membrane on using Cool-Grease.

The STS ICP RIE advanced silicon etcher system chamber is cleaned again with O_2 plasma for 10 min to prevent micrograss formation due to residues from previous processes. Afterwards, the wafer was etched for 8 min with another SF_6 Bosch process recipe. The etch cycle is 12 s long and the plasma is excited at 13.56 MHz frequency with 12 W power at a 130 sccm SF_6 and 13 sccm O_2 flow rate under 36 mT pressure. The passivation cycle is 8 s long with a C_4F_8 flow rate of 130 sccm under 18 mT pressure. Although this recipe etches with smaller steps and yields smoother surfaces, it is also

prone to produce excessive amounts of micrograss. The anisotropic etch was followed by a 15 s isotropic etch to clean the possible micrograss formations. After the tilted STS DRIE etch, the oxide around the pillars is hollowed while the silicon inside the oxide confinement is discernable in the SEM images.

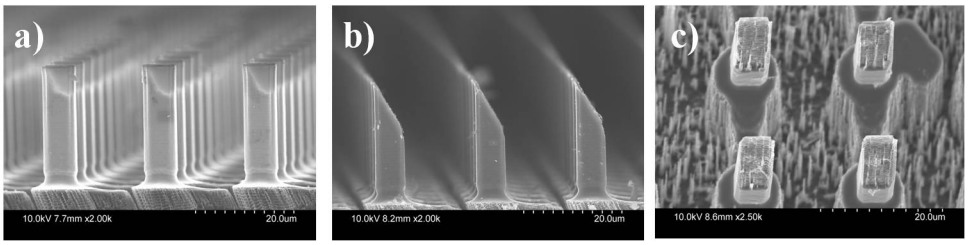

Figure A.8: The pyrex ramp used for attaching the membrane to using Cool-Grease.

The dice are dipped into 20 min of BOE to remove any oxide residues. As can be seen in the figure, due to the height difference of the chip during the tilted etch, the angles and the etch rate of the pillars gradually change throughout the chip from top to bottom. As the bases of the pillars are also freed from oxide before the tilted etch, the pillars get elevated on islands of silicon during the tilted etch. The base of the islands has micrograss due to the second STS DRIE recipe (Figure A.8).

A.3 Experiments

The chip is placed on a platform that would provide a 22^o angle. In the images below the slope is upwards from right to left. The tip angle of the pillars in these experiments is not known as they show variation from top to bottom of the chip.

When the droplets are dispensed, they evaporate too fast for extended observation of the motion. In the first trial, Figure A.9, the droplet is dropped onto a lower section of the chip where the tip angle of the pillars is steeper. The droplet seems to be evaporating upwards as expected. However, in the second trial, the droplets seem to evaporate at the spot where they are injected. In the second trial, Figure A.10, the droplet is also dispensed at a higher section of the chip where the tip angle of pillars is lower. In addition, the surface does not seem to be very hydrophobic. Due to extensive BOE etch, the pillars may only have a thin layer of native oxide.

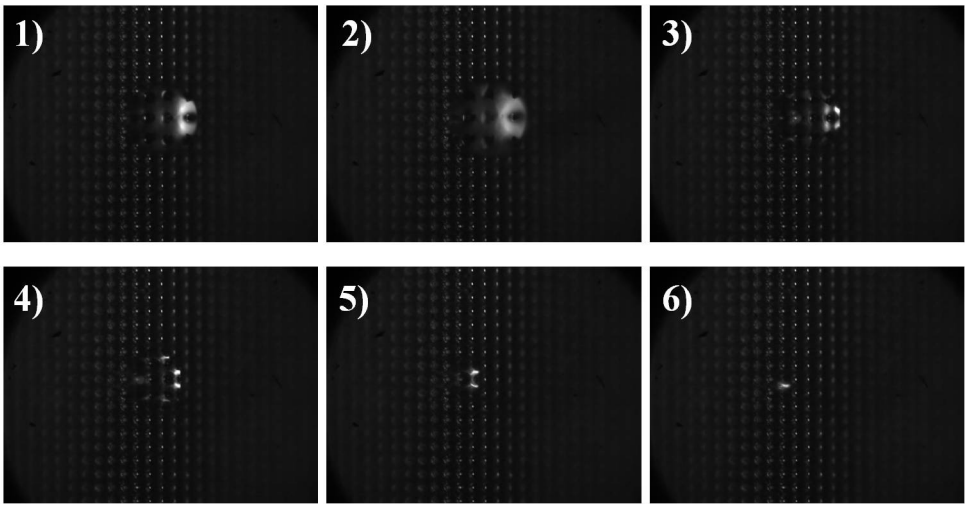

Figure A.9: Trial #1: The time progresses from frame 1 to 6.

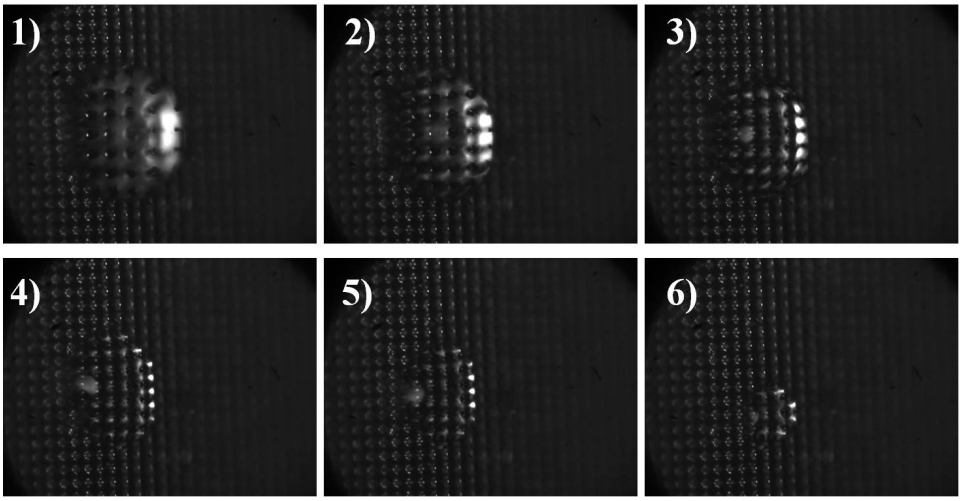

Figure A.10: Trial #2: The time progresses from frame 1 to 6.

This experiment can work better if the dispensed liquid is an oil droplet instead of a water droplet. The surface of the pillars may quickly become hydrophillic due to the native oxide. In such a case, a hydrophobic droplet that does not evaporate on a hydrophobic surface may perform better in terms of expected upwards displacement.

APPENDIX B

DATA ANALYSIS ALGORITHM

In order to give an insight about the inner workings of the computer analysis program, the calculation of the baseline of the current transient and the definition of an event in the algorithm will be briefly discussed. For computing the baseline, the algorithm takes the moving average[4] of the current transient data, which is similar to lowpass filtering of the data. As a result, the computed baseline follows the data unaffected by the modulations, as expected from the baseline (Figure B.1).

The current transient data feature events range in duration from milliseconds to seconds. In the seconds-long events range, the current blockages also have millisecond-long modulations where the current is lower than the open pore current value. These characteristics of the current transient data necessitated the program to handle the events in many regimes. For example, for 10 ms to 100 ms long event regimes, a different baseline is used than the one used for 100 ms to 1 s events. The baseline that the program utilizes for the shorter duration event regimes follows the data more closely than the ones that are used for longer duration event regimes.[5]

The definition of an event can be summarized as the continuous data points over a certain threshold current. While the algorithm is sweeping through the current data points, if it detects a point which is at a greater magnitude than the threshold value above the baseline, it marks the point. From the marked point, to record the beginning of event, the program threads backwards through the data points until the difference between the data and the

[4]Moving average can be considered as a convolution window that takes the average of the data points in the range. The calculated value is assigned to the midpoint in the convolution window. The programmer determines the size of the window.

[5]The baseline keeps up with the data more closely when the moving average convolution window size is decreased. This way the baseline is the average of a closer vicinity of data points, whereby ensuring greater adaptability to the change in the current level. For an event duration regime, the moving average window size is kept about three times the longest duration event that would like to be detected.

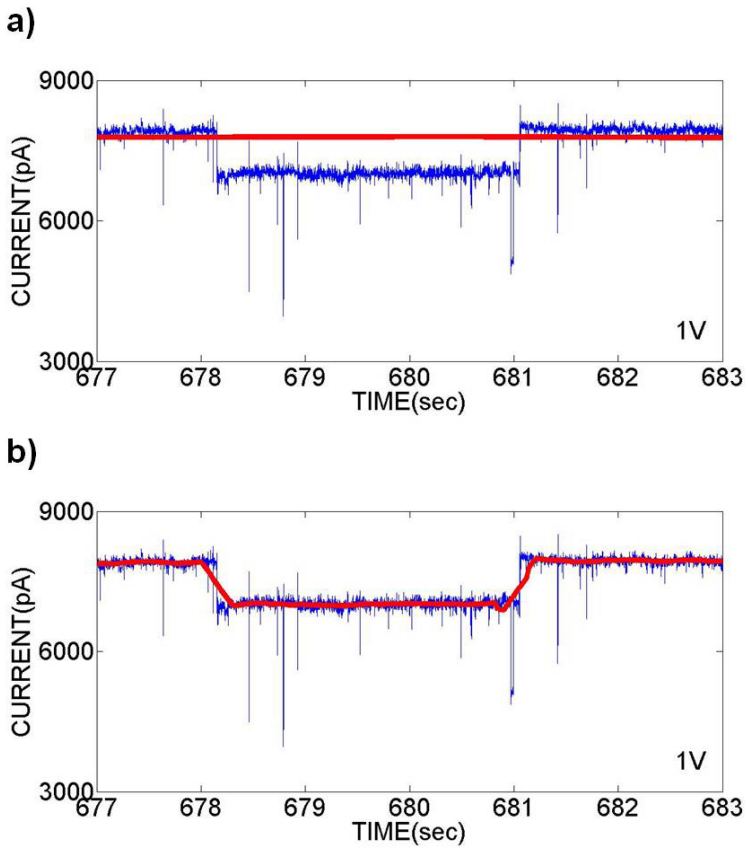

Figure B.1: The baseline in part a) is used for event durations ranging from 1 s to 5 s. All shorter and longer events than the duration regime that are of interest for that particular analysis sweep are discriminated. The baseline in part b) is used for event durations ranging from 10 m to 100 ms.

baseline drops to the 20% of the threshold value. Afterwards, the program threads forwards from the marked point until the data and the baseline distance again drops to 20% of the threshold value to record the end of the event.

The algorithm also records the duration, magnitude and the blockage ratio of the event. The event duration is acquired by subtracting the end point from the beginning point. Another parameter, the peak of the event, is found by making a search for the maximum of the data points framed by the beginning and the end of the event. The current blockage ratio is gathered by calculating the ratio of the baseline current value to the magnitude of the event (Figure B.2, Table B.1).

The threshold current for events for a certain voltage measurement is evaluated by taking the standard deviation of a span of data, i.e. 20 s long, that

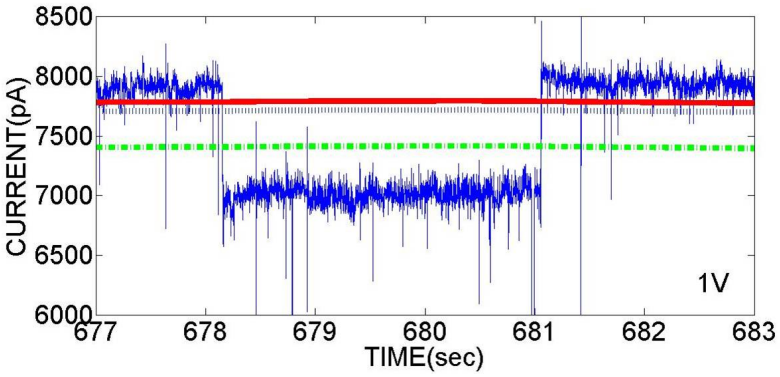

Figure B.2: The red solid line is the baseline. The green dashed line with dots is the current event threshold, and the black dashed line just below the threshold line is the 20% of the threshold level.

Table B.1: Sample algorithm output for Figure B.2.

#1	#2	#3	#4	#5	#6
678.1543	681.0553	2.9010	-3411.0398	7741.4415	-44.0621

#1: Beginning of the event
#2: End of the event
#3: Duration of the event
#4: Current blockage magnitude
#5: Baseline value
#6: Current blockage ratio.

does not show any events. Assuming that the noise of the data can be modeled by the Gaussian distribution, the valid events are going to be the data points that are outside of the range of at least 3 σ. When the threshold value is calculated by multiplying the standard deviation by 3 σ, it is observed that the authenticities of some events are still questionable . Therefore, the standard deviation of the data is multiplied by four to determine the threshold current.

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