LOCAL CONTROL OF MULTIPLE MODULE CONVERTERS WITH RATINGS-BASED LOAD SHARING

BY

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THESIS

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ABSTRACT

Multiple module dc-dc converters show promise in meeting the increasing demands on efficiency and performance of energy conversion systems. In order to increase reliability, maintainability, and expandability, a modular approach in converter design is often desired. This thesis proposes local control of multiple module converters as an alternative to using a central controller or master controller. A power ratings-based load sharing scheme that allows for uniform and non-uniform sharing is introduced. Focus is given to an input series, output parallel (ISOP) configuration and modules with a push-pull topology. Sensorless current mode (SCM) control is digitally implemented on separate controllers for each of the modules. The benefits of interleaving the switching signals of the distributed modules is presented. Simulation and experimental results demonstrate stable, ratings-based sharing in an ISOP converter with a high conversion ratio for both uniform and non-uniform load sharing cases.

To my family and friends, for their love and support

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CHAPTER 1

INTRODUCTION

Increasing demands on the efficiency and performance of energy conversion have led to new approaches in dc-dc converters. Voltage regulator modules need to deliver high current (around 100 A) at a low voltage (approximately 1 V) to computer processors. At these levels, the output impedance of a single converter can seriously degrade efficiency and make regulating output voltage difficult, if not impossible. Power distribution with higher intermediate bus voltages is common in telecommunication systems and data centers in order to increase overall system efficiency. This forces higher voltage step-down ratios for point-of-load (POL) converters. Other applications that have high voltages often require the use of IGBTs instead of MOSFETs when traditional energy conversion approaches are taken. This limits the switching frequency and increases the size of filter components.

Multiple module dc-dc converters (also referred to as multiphase converters or cellular converters) show considerable promise in addressing these challenges. First of all, the energy that must be delivered to the load can be divided among the modules in the converter. This not only allows the converters to share the stress caused by changes in the load but also enables the ratings of the devices in each module to be comparatively lower. Lower ratings can lead to smaller package size and better heat dissipation. There is also more freedom in component selection. Another benefit of having multiple modules is that converters with high input to output ratios can be realized in one stage instead of cascading converters in a number of stages. This can increase the overall efficiency and performance of the energy conversion system. Multiple modules can also provide redundancy with possible improvements in reliability, availability, and maintainability. By interleaving the switching of the modules, the output ripple can decrease considerably. This corresponds to a decrease in the size of the output filter necessary. Of course, multiple module converters have drawbacks

including more components and complexity.

An important issue with multiple module converters is load sharing. Conventionally, the load is shared uniformly among the modules of the converter. This simplifies the design since each module is designed to be identical and is controlled in the same way. Load sharing methods fall into the two main categories of droop control and active sharing. Due to the poor voltage regulation that droop control provides, active current sharing methods have been explored for modules with outputs in parallel. In order to increase reliability and modularity, a distributed approach is often desired when implementing load sharing control. Distributed control tends to introduce communication and increase complexity of the system. Hence, finding a simple, distributed control technique that does not require even load sharing is a motivating factor in this research project. Previous research into non-uniform current sharing has been based on supervisory control. Distributed switch interleaving methods are also explained.

One challenge of a multiple module converter is to be truly modular. The contribution of this research is the demonstration of independently controlled modules that can unevenly share the load. Previous research constrains the control parameters or the power ratings of the modules to be identical, thereby limiting the possible benefits of a modular approach. In this thesis, a modular converter is realized through local control of each module in the converter. The modules are designed to supply different amounts of power to the load. Specific attention is given to the input-series output-parallel (ISOP) configuration which is well suited for a high voltage conversion ratio in a step-down operation. A power rating resistor in each module is connected in a series stack to provide local information that drives ratings-based load sharing. Each module's digital controller utilizes the local information and a global output voltage reference and implements open-loop sensorless current mode (SCM) control. Simulation and experimental results demonstrate stable, ratings-based load sharing in an ISOP push-pull converter.

CHAPTER 2

MULTIPLE MODULE CONVERTERS

There are four primary ways in which multiple module dc-dc converters can be constructed. Most multiple module converters in use today employ an input-parallel output-parallel (IPOP) configuration. A converter that uses this configuration is commonly referred to as a multiphase converter. Input-series output-parallel (ISOP), input-parallel output-series (IPOS), and input-series output-series (ISOS) arrangements are also possible and are showing potential in a variety of applications. While other nested configurations are possible with multiple module converters, they are not common. The general configurations are shown in Fig. 2.1.

When the inputs or outputs of the modules are connected in parallel, each module has equal input or output voltage, respectively. The current from each module will then add in accordance with Kirchhoff's current law at the input or output nodes. Both of these properties are due to the simple fact that they share the same node. Similarly, when the inputs or outputs are connected in series, the average input or output current is the same, respectively. The voltages will add in accordance with Kirchhoff's voltage law. These seemingly simple properties of multiple module converters have significant impact on the ways in which they can be used and controlled.

An important distinction to make is that multiple module converters are not the same as multiple input or multiple output converters. Of course, multiple input/output converters and multiple module converters are not mutually exclusive concepts; a multiple module converter can have multiple inputs or outputs. While there are similarities or overlap in the operating principles, the scope of this research is limited to converters with a single input and a single output.

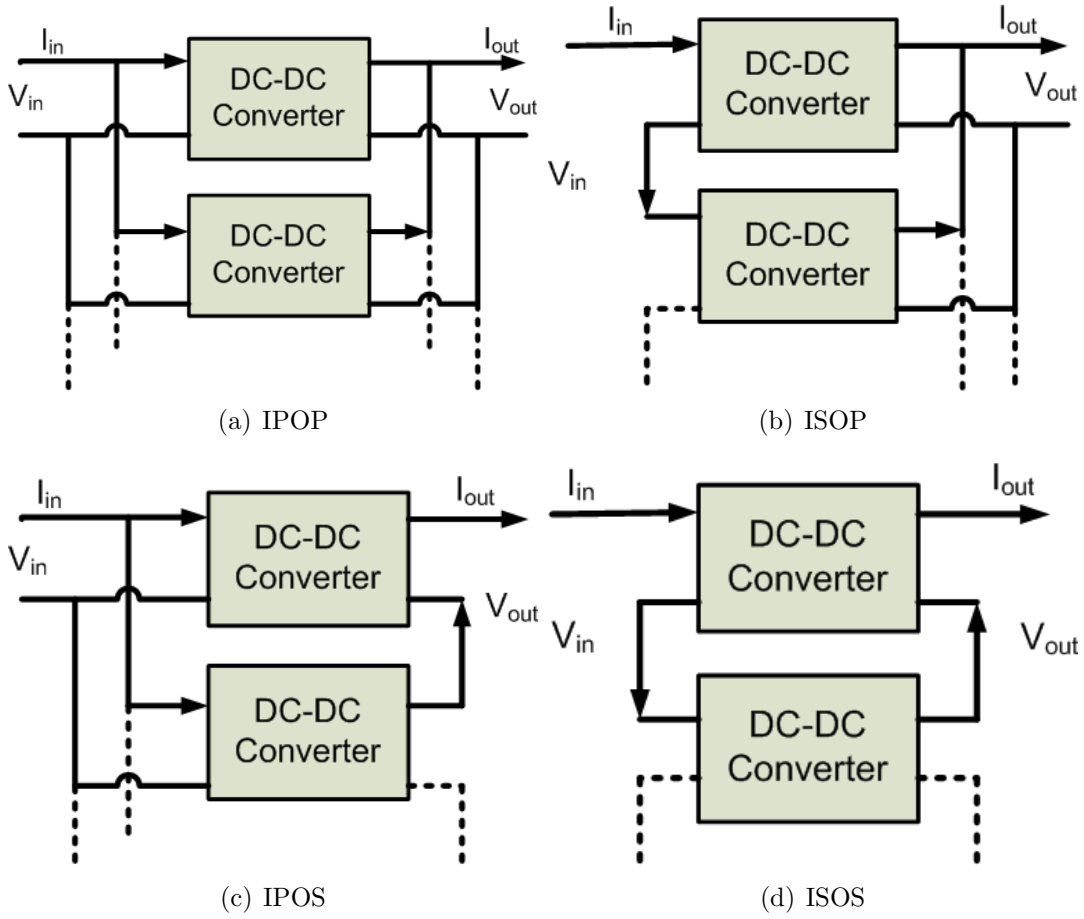


Figure 2.1: Possible structure of a multiple module converter: (a) input-parallel output-parallel (IPOP), (b) input-series output-parallel (ISOP), (c) input-parallel output-series (IPOS), and (d) input-series output-series (ISOS). When a parallel connection is made, the voltage of each module is the same and the currents add together in accordance with circuit laws. The converse is true when modules are connected in series.

2.1 Motivation

Multiple module converters have been extensively researched over the past few decades. Some of the motivation came from applications such as voltage regulator modules (VRM) which need to supply a tightly regulated output voltage to computer processors. While the output voltage is around 1 V in VRMs, the output current can be around 100 A at full load. Therefore, the output impedance of the converter needs to be very low since the impedance of the load can be on the order of 10 mΩ. If the output impedance of the converter is not low enough, the converter efficiency can substantially decrease and it may even be infeasible to reach the desired output voltage.

In order to meet the increases in the load current and slew rates, multiple buck converters working in parallel were introduced. This topology, commonly called a multiphase buck, is an example of an IPOP converter. With multiple buck converters operating in parallel, the aggregate output impedance of the converter decreases due to the parallel connection. Each phase of the converter is matched to support uniform power sharing. If correctly controlled, the phases can work together to respond to changes in the load and decrease output ripple.

In most energy conversion systems, voltage levels are converted in stages that are cascaded. For instance, in a computer data center, multiple conversion stages transform the relatively high input voltage down to the 1 V level of the central processing unit. Each conversion stage has a certain efficiency; the overall efficiency is the product of the efficiency of each stage. Even if each stage has decent efficiency, the overall efficiency can be relatively low. However, a multiple module converter may be especially suited for this operation. Instead of cascading multiple converters, an ISOP converter can step-down a relatively high voltage to a low voltage in one stage, thereby increasing the overall efficiency. The IPOS configuration is the dual of the ISOP configuration and can be advantageous when a high step-up ratio is needed. This concept is exemplified in Fig. 2.2 where a hypothetical converter steps down 48 V to 1 V.

Another motivating factor behind a modular structure is increased system reliability through redundancy. If a fault occurs in one of the modules in the converter, the whole converter need not fail and can continue to provide power to the load. Of course the total

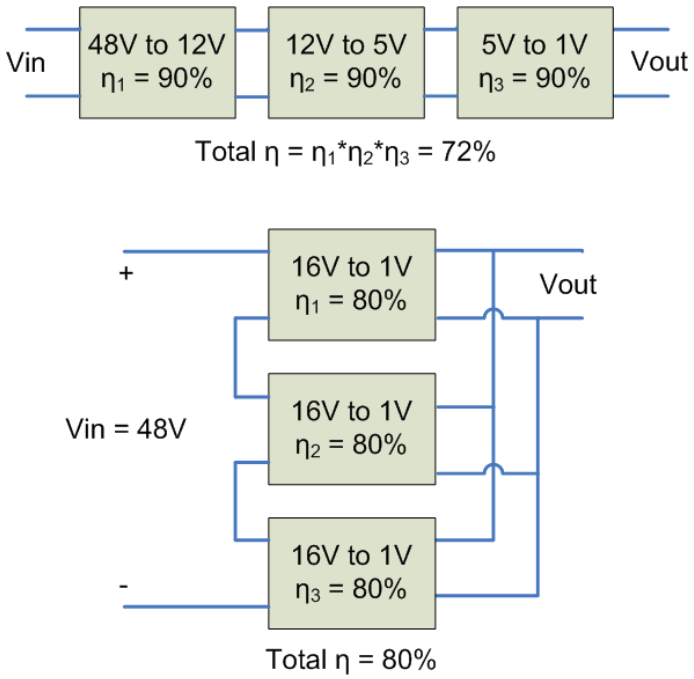


Figure 2.2: Comparison of system efficiency in a hypothetical system. The cascaded conversion system has a lower overall efficiency η than the single stage, multiple module system. This is in spite of the fact that each module of the multiple module converter might be less efficient than each stage of the cascaded converter.

power that can be delivered to the load will decrease, but at least the load will still receive some power. If, on the other hand, there was only one module in the converter and it experienced a fault, no power would be provided to the load. Often a converter with equal power modules is designed to have one more module than what is necessary to meet the full load requirement. This is referred to as $N + 1$ redundancy and allows complete fault coverage in the case of a single fault. An important caveat, as mentioned in [1], is that it is not always clear whether system reliability is improved by adding redundant modules.

In some applications expandability, maintainability, availability, and flexibility are driving factors of system design. In these systems a modular approach is beneficial. For instance, the load requirements in computer data centers may change considerably in just a few years, long before the intended life of the power electronics is reached. Instead of having to install a new converter, adding extra modules that account for the long term load changes can save money and time. It is helpful to have easily expandable converters when it is difficult to foresee the

long term load. Maintainability is especially important in mission critical applications like telecommunications [2]. Similarly, hot-swapping converters may be useful [3] when system availability is vital. Overall, multiple module converters provide a foundation for flexible converters that are not possible otherwise.

Multiple module converters even support more flexibility when designing converters. Since the voltage or current ratings of components in each module generally decrease as more modules are added to a converter, an extra degree of freedom in component design is introduced. For instance, in an ISOP converter the input voltage is divided among the modules, thereby allowing the switch ratings in each module to decrease. This makes it possible to use MOSFETs instead of IGBTs in high power systems like high-speed trains [4]. Multiple module converters by their nature are able to get around traditional device ratings constraints and provide the opportunity for more optimal component selection.

2.2 Load Sharing

One of the primary control objectives in a multiple module converter is load sharing. Load sharing is important for a number of reasons. If the modules are designed to share the load evenly, but in fact do not do so, one module will place more stress on its components than another module. This could decrease the life of the module, violate component ratings, or possibly cause a system failure. Even if the components can handle the extra stress, converter performance or efficiency could be affected.

In applications where the load is evenly shared among modules, each module is usually designed to be exactly the same and provides equal power to the load. Therefore, most load sharing techniques assume that each module is supplying the same amount of power. This means that uniform load current sharing or uniform load voltage sharing is the goal (depending on the configuration). Most research has focused on uniform load current sharing in IPOP converters. Since the voltage at the input and output will automatically be matched due to circuit laws, IPOP converters control the modules to evenly share the current at either the input or output.

There has been some research into non-uniform current sharing for parallel output con-

verters [5, 6]. Non-uniform sharing enables each module in a converter to be optimally designed to supply a different amount of power. This means different current levels are supplied by the modules in parallel output converters. The modules can be dynamically enabled or disabled so that the converter operates with high efficiency over a wide load range. For instance, when operating at light load, some of the modules designed for high power can be turned off. In a converter with uniform load sharing all the modules have the same region of high efficiency, but in a converter with non-uniform sharing the high efficiency region of the modules occurs at different load levels. This is useful in VRMs as is demonstrated in [5] with a three module IPOP converter that operates with higher efficiency over a wide load range as compared to conventional VRM designs.

While phase shedding techniques are commonly used in converters with uniform load sharing, non-uniform load sharing provides greater resolution and a smoother transition between operating points. This creates a more flat efficiency curve that ranges from light to heavy loads. In [6] this is accomplished with binary logarithmic power ratings such that the n^{th} module is rated for $2^{(n-1)}P_0$, where P_0 is the power rating of the lowest power module. A hysteretic logic block was also included to prevent chattering of module enabling/disabling when the load level of the converter is near the boundary of two modes of operation. The primary drawback so far is that research on non-uniform load sharing has relied on a central controller to select which modules are active at various load levels.

The two main categories that control methods fall into are droop control and active sharing [7]. Droop control is so named since each module responds to dips in the output of the converter. A feedback loop is created by comparing the output with an internal reference and using the difference of the signals to control the module's duty ratio. One benefit of droop control is that no extra connection or communication wire among the modules is necessary since each module can sense the output. This enables a modular design of power converters and improves fault-tolerance. However, there is often a trade-off that must be made between load regulation and load sharing accuracy [8, 9]. For instance, when the output voltage in an parallel output converter droops, the output current from each module increases based its output impedance. Modules with a low output impedance will provide more current (and therefore more power) than modules with a high output impedance. Varying the effective

output impedance of each module is a basis for load sharing in droop control. Due to the poor load sharing that droop control provides, active current sharing methods have been explored for modules with outputs in parallel.

A number of active current sharing methods have been developed which mitigate the effects of component parameter variation. Generally, each module implements some form of current mode control and is provided a current reference. Each module tracks this current reference such that all modules uniformly share the load current. In a converter with a central or supervisory controller it is relatively simple to command even load sharing. Sensorless current mode (SCM) control can be used to reduce sharing complexity [10]. However, there are cases in which sharing can be problematic. When modules are forced to share based on a given reference they may not be operating in their individual region of highest efficiency. If dynamic load sharing is enforced, transient response can also be limited.

Load sharing is more challenging when the modules are controlled in a distributed fashion. A number of methods have been developed as a result. In a master-slave approach, one module is the "master" and sets a current reference for the rest of the modules [11]. In a "democratic" scheme, a single-wire communication bus can provide information about the average output current of all modules [12]. In [13] frequency-based current sharing is implemented by filtering the output ripple to obtain output current information. The benefit of distributed load sharing is increased modularity and fault-tolerance. As is expected, distributed load sharing tends to increase part count and system complexity. A major drawback of these methods is that they only work if the load is evenly shared among the modules.

The control algorithm used in each module is usually the same but does not need to be. In [14], peak current mode control and sensorless current mode control were implemented on separate modules. This approach profited from the distinct current sharing and voltage regulation abilities of the two control algorithms. Not only can different control methods be used on each module, but the modules themselves can be designed differently. For instance, one module can be designed to quickly respond to load changes while other modules provide most of the power in steady state [15].

Load sharing does not require active control of every module. Some approaches have no

output regulation on some or all of the modules in a converter. In [16] a high frequency IPOP coverter was constructed with several unregulated modules and one module that regulated the output. A central controller would turn the unregulated modules on or off depending on the load. Another idea proposed in [16] was to use only unregulated modules but to modulate the active modules to meet load requirements. The main drawback of this approach is increased energy storage at the converter output. In [17] a converter designed for a VRM application was proposed with multiple unregulated modules and one regulating module. The unregulated modules were connected in parallel with the one regulating module connected in series at the input to form a quasi-ISOP converter. In many ways it is similar to what was proposed in [15].

2.3 Switch Interleaving

Interleaving the switching signals brings important advantages to multiple module converters. Switch interleaving increases the effective output ripple frequency for a given switching frequency. This happens when switch turn-on times of the modules are spread throughout the switching period. When the inductor current of one module is increasing, the inductor current of another module might be decreasing. This can effectively cancel out most of the ripple. In the ideal case with interleaved timing and the right duty ratios, output current ripple could be canceled completely. A simple example of switch interleaving is shown in Fig. 2.3.

In general, when a converter with n modules evenly shares the load and evenly distributes the switching, the output current ripple will decrease by a factor of $1/n$. This allows smaller output filter components to be used. Alternatively, the switching frequency could be reduced if the filter remained the same.

Switch interleaving has been implemented with both distributed and central control methods. It can be accomplished with relative ease in a central controller where the phase delay of the kth module is given by $(k-1)(360^\circ/n), k \in 1, ..., n$. This evenly distributes the switch turn-on times throughout the switching period. The major challenge comes when there is no central control. The mathematical foundation of distributed interleaved systems has been

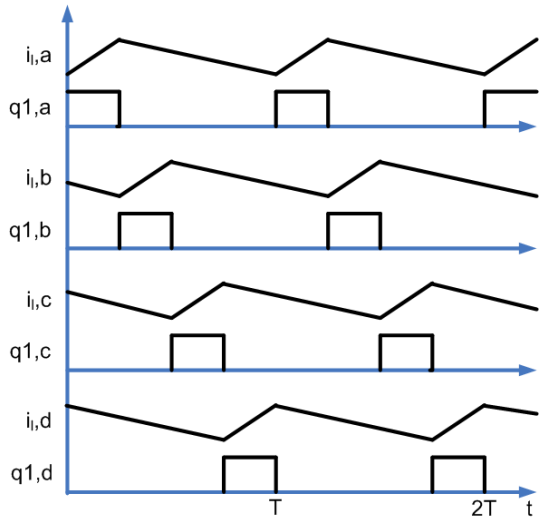


Figure 2.3: Interleaved switches in a converter with four modules having switching period T.

discussed in [18]. Each module has a local controller with an independently generated base clock. It has been shown that even if no action is taken to coordinate the switching among the modules, the stochastic reduction in ripple is on the order of $\sqrt{n}$, where n is the number of modules [19]. Upper bounds on the current ripple amplitude and conditions for zero ripple were explained in [20]. The methods for distributed switch interleaving published so far either require or are geared for even spacing of switch times (i.e. modules with equal ripple magnitude). This implies that switch interleaving with non-uniform ripple magnitude is not considered or optimized. Another common assumption is that all the modules are operating with an identical switching frequency.

A number of papers have examined how to interleave the switching signals in distributed converters [19, 21, 22]. When active interleaving measures are taken, the removal or addition of a module should not disrupt the interleaving scheme. One approach uses a separate control bus to actively interleave the switching signals in distributed converters [19]. Controllers for the distributed converter modules are connected to this *interleaving bus* and operate in a way that drives their base clock to be 180° out of phase with the aggregate clock. Another scheme uses a bus that sets a voltage signal V_{mod} such that the voltage controller phase delay between modules will be $360°/n$ [21]. This scheme requires even sharing of the load between

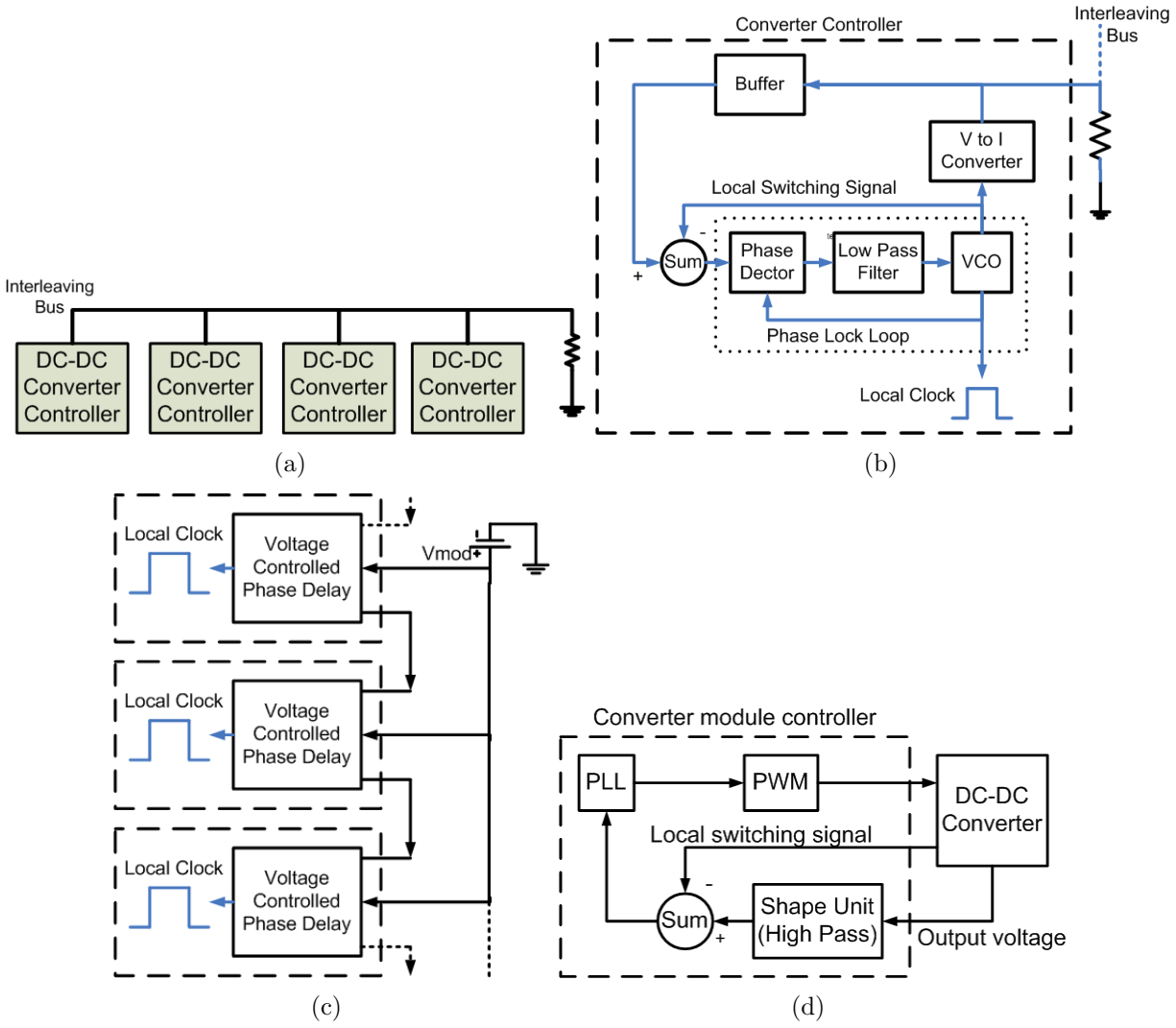


Figure 2.4: Diagrams of various interleaving schemes. In (a) the overall structure of the interleaving bus is shown. In (b) the local operations performed by each module in the interleaving bus scheme are shown. The voltage based phase delay scheme is displayed in (c). In (d) the output sampling and filtering scheme is shown.

the modules as well as a known number of phases in order to set V_{mod}. One scheme does not require a bus for interleaving [22]. It filters the collective output of the modules to detect the switching instances. The challenge is sensitivity to noise. Diagrams of these interleaving schemes are shown in Fig. 2.4.

2.4 Push-Pull Converter Topology

One important aspect of multiple module converters is the common node (or lack thereof). In IPOP converters, all of the converters share a common ground. This is not the case in ISOP, IPOS, and ISOS converters. The ground node of one module has a lower or higher voltage than another module connected in series. As a result, electrical isolation provided by a transformer or coupled inductor is generally necessary in each module. This enables the other port of the converter to be connected in parallel and share a common reference node with the other modules. A number of dc-dc converter topologies provide isolation including flyback, forward, full-bridge, half-bridge, and other forward type converters.

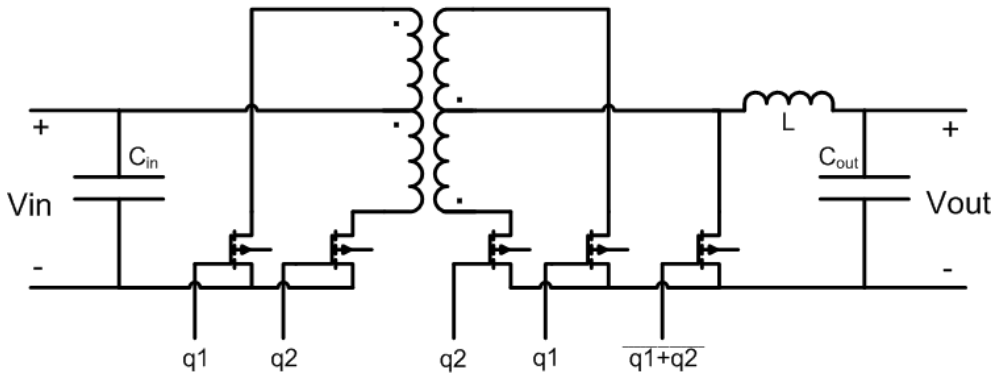


Figure 2.5: Circuit diagram of a push-pull converter.

A push-pull converter is a buck-derived forward typology that is suitable when isolation is needed. It is also useful in situations requiring a high voltage conversion ratio since the transformer can provide both isolation and voltage conversion based on its turns ratio. In an ISOP converter this topology works well since, as seen in Fig. 2.5, it is essentially a buck

converter at the output with a transformer on the input side. The transformer can be small given a high switching frequency.

In a push-pull converter, the switch signals $q1$ and $q2$ have equal duty ratios but will not overlap. There will be an interval when neither is on, depending on the duty ratio D of the switches. The ideal average relation of input voltage V_{in} and output voltage V_{out} is given by

$$V_{out} = \frac{2DV_{in}}{a} \tag{2.1}$$

where a is the turns ratio of the transformer. The basic operation of the converter is shown in Fig. 2.6. When either $q1$ or $q2$ is on, the inductor current increases since the input voltage is being applied to the switch side of the inductor through the transformer. When $q1$ and $q2$ are off, the inductor current decreases. Since the transformer is wound in a bifilar fashion and $q1$ and $q2$ have equal on times, the volt-second balance in the transformer should be stable.

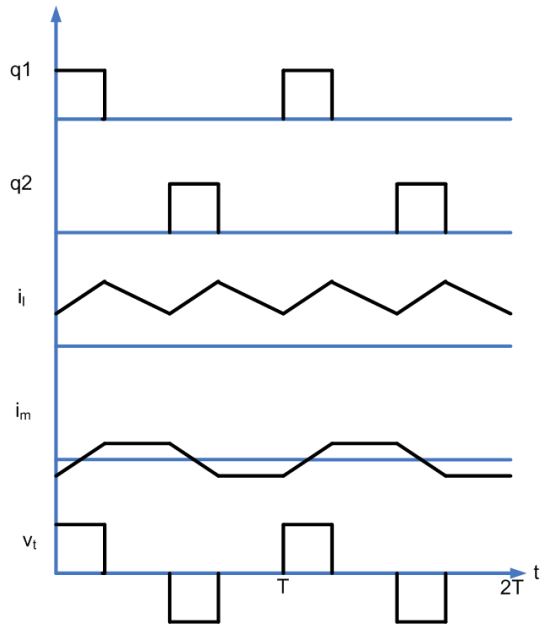


Figure 2.6: Operation of a push-pull converter.

CHAPTER 3

LOCAL CONTROL OF MULTIPLE MODULE CONVERTERS

A central or supervisory controller for a multiple module converter simplifies control functions such as switch interleaving, provides unambiguous global reference signals, and tends to keep parts count down by limiting local control hardware. However, centralized control yields single points of failure and requires intensive data exchange to manage control of modules. Distributed control lends itself to a modular design but often requires considerable coordination and communication among the modules in the converter [23, 24]. While communication among modules can be beneficial, drawbacks include increased complexity, decreased reliability, relatively slow response to disturbances, synchronization needs, establishment of protocols, error checking, operational interdependency, bandwidth limitations, and other issues. The work presented here seeks distributed controls that reduce or eliminate communication among modules without unnecessarily increasing each modules intelligence.

Local control takes the perspective of each module in the converter. Each module becomes an agent, operating within the system. Possible control frameworks for understanding such a system include multi-agent systems and cooperative distributed problem solving [25, 26]. These frameworks are used to describe the interactions in flocks of birds, traffic systems, and robot formations. The goal is convergence to a common point for mobile, autonomous agents as described for flocking algorithms in [25]. Local sensors (vision) were modeled to provide information for coordination without requiring global information or communication. In [26], more emphasis is placed on having intelligent agents that can cooperatively solve problems by means of various strategies. These multi-agent systems also were discussed in the context of distributed dc power systems in [27]. Droop control was implemented with dynamic load interruption on a locally controlled, distributed dc system. A noted drawback is that sometimes distributed systems require substantial intelligence or communication in order to

coordinate the system. The aim of local control is to capitalize on the local information of each module in order to increase the independence of each module in a manner that meets global system control objectives.

Many agent-based distributed controls require substantial intelligence for each element. There is often much more total system computation involved than would be present in a centralized control. In this research, the intent is to avoid complexity as much as possible, seeking out control methods that have an inherent tendency to meet global power conversion requirements with minimal local effort or data exchange. For example, in [28] the complexity of feedback control for a multi-module ISOP or IPOS converter is actually reduced by eliminating some of the control loops. The simplified structure leads to converters that are forced to share power by virtue of circuit laws rather than active control. The intent of the present work is to broaden results like this by developing control approaches that are deployed on a module-by-module basis but tend to take actions favorable to the global system.

An outline of a locally controlled module is shown in Fig. 3.1. The three primary sources of information are the input line, the output load, and any internal components of the converter module. Local control algorithms can utilize line or load measurements to actuate desired responses. For instance, filtered load information can be used to perform functions like switch interleaving [22] or load sharing [29]. Internal states such as inductor current or certain node voltages are also commonly used to control converter modules. Another option is to add internal components or circuitry that can be used in the control algorithm to either infer global information or replace it.

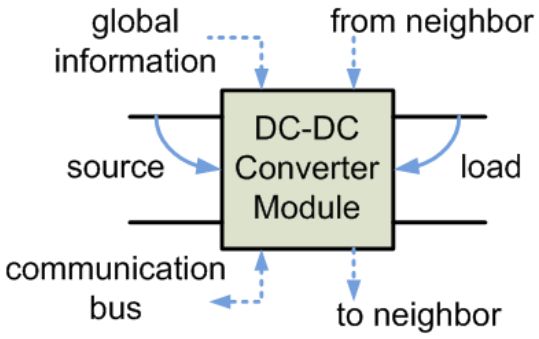


Figure 3.1: Sources of information for a locally controlled converter module.

While an emphasis is placed on locally available information, limited external information can also be used. For example, combined global reference signals may be helpful or necessary to ensure that the modules share a common control objective. Sharing of information among near neighbors can also be useful in operations like switch interleaving. A communication bus can be included for monitoring and configuring modules as desired. Local control does not prohibit external information but seeks to minimize it or at least limit dynamic dependence on it.

In a truly modular system, it should be possible to add or remove modules at will. The system should maintain stable operation and meet load requirements. Another goal is to enable dissimilar modules to work together with minimal information exchange yet still perform as needed. Such a system would be easily expandable and could be upgraded with new control algorithms to meet a change in load requirements. Applications of this modular energy system range from microgrid and alternative energy resource management to telecommunications and computer data centers.

In this work, an ISOP push-pull converter with local control is explored. The goal is to demonstrate how relatively simple modules can cooperatively and stably meet global control objectives. Communication between modules is limited to one bit used to interleave the switching of the modules. The following sections describe sensorless current mode control and how power ratings-based load sharing can be beneficial in locally controlled modules.

3.1 Sensorless Current Mode Control

The usefulness of sensorless current mode (SCM) control has been previously established [30]. It is an observer-based technique that reconstructs the inductor current by integrating the inductor voltage. This avoids noise issues and supports wide load dynamic range. While it can be applied to essentially all converter topologies, SCM has been shown to produce "super-matched" power sharing in an ISOP configuration since the input currents and the output voltages of the modules must match [31]. The stability of SCM control has also been established for the ISOP configuration [28].

The standard control law for SCM is given by

$$v_I(t) = G \int (V_{sw} - V^*_{ref})dt \tag{3.1}$$

where V^*_{ref} is either a fixed reference in open-loop control or the output of a voltage feedback loop, V_{sw} is the voltage at the switching node, and G is an integrator gain. The voltage V_{sw} for this converter is essentially qV_{in}, where q is the sum of the two input-side switching functions in the push-pull circuit. The controller output v_I is fed into a conventional, fixed-frequency pulse width modulator (PWM) to generate the switching signals. As is typical in current mode control, the carrier function includes a stabilizing ramp.

In an ISOP push-pull module, the voltage at each switching node is based on a fraction of the total input voltage. With n modules and even load sharing, for example, the module input voltage would be V_{in}/n. The control law for an ISOP push-pull converter with even load current sharing becomes

$$v_I(t) = G \int (q_k \frac{V_{in}}{na} - V^*_{ref})dt \tag{3.2}$$

for the kth module, $k \in 1, ..., n$. The value V^*_{ref} is still a global reference – either a fixed value for open-loop control or the output of a voltage feedback loop. Synchronization pulses can be sent to the modules to aid in interleaving the switching signals. A diagram describing SCM control in an ISOP converter with even load sharing is shown in Fig. 3.2.

SCM control in the ISOP converter enforces automatic, stable input voltage and output current sharing. This follows from the structure of SCM and the circuit dynamics. Furthermore, SCM control will not be disrupted by line disturbances since the control provides a line feedforward effect. While the discussion so far has focused on even sharing of the load, SCM is still stable when the input voltage to each module differs from V_{in}/n.

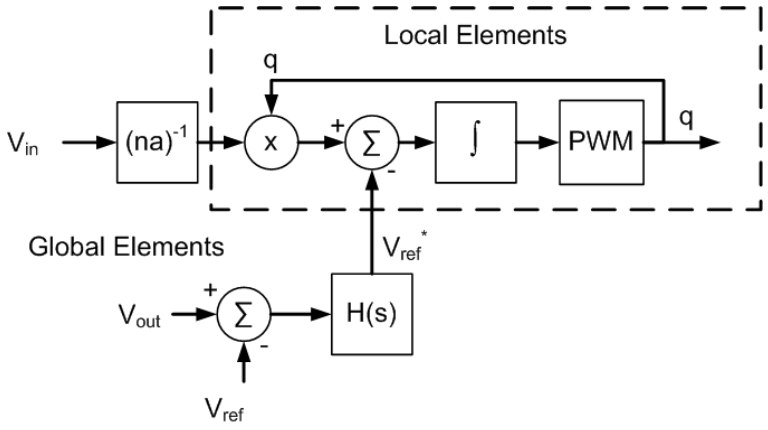


Figure 3.2: Diagram of SCM control for uniform sharing in an ISOP configuration.

3.2 Ratings-Based Load Sharing

Most multiple module converters are designed and controlled so that each module provides equal power to the load. In converters with a parallel output, even load sharing requires each module to provide the same average current to the load. It has been shown that in an ISOP configuration, input voltage sharing is equivalent to output current sharing [32]. Hence, another way of looking at load sharing in ISOP converters is input voltage sharing. In [28], the desire to have input voltage of V_{in}/n for each module had the effect of matching the duty ratios of the modules and resulted in uniform output current sharing.

Many applications could benefit from controlled uneven load sharing [5, 6]. Modules with various power ratings could be used to increase efficiency and dynamic response of the converter. For ISOP converters with SCM control, the input voltage of each module can be weighted by unequal amounts without compromising overall stability. This allows the input voltage to be set based on a signal proportional to the module's power rating. In turn, this enables ratings-based load sharing.

One possible method is to use a voltage divider stack, as shown in Fig. 3.3, to set module input voltages. To provide ratings-based sharing, each converter has a front-end "set" resistor proportional to its intended power rating. These resistors are stacked as a series divider, thus providing a local input voltage reference proportional to the respective power ratings. Instead of driving the input voltage of each module to be V_{in}/n, each module's input voltage

is driven towards the voltage across its "set" resistor. Therefore, the control law for the kth push-pull module with ratings-based sharing is

$$v_I(t) = G \int (q_k \frac{V_{stack,k}}{a} - V^*_{ref}) dt \tag{3.3}$$

where $V_{stack,k}$ is the voltage across the kth module's power rating resistor, V^*_{ref} is a global voltage reference, and G is determined by the modulation process.

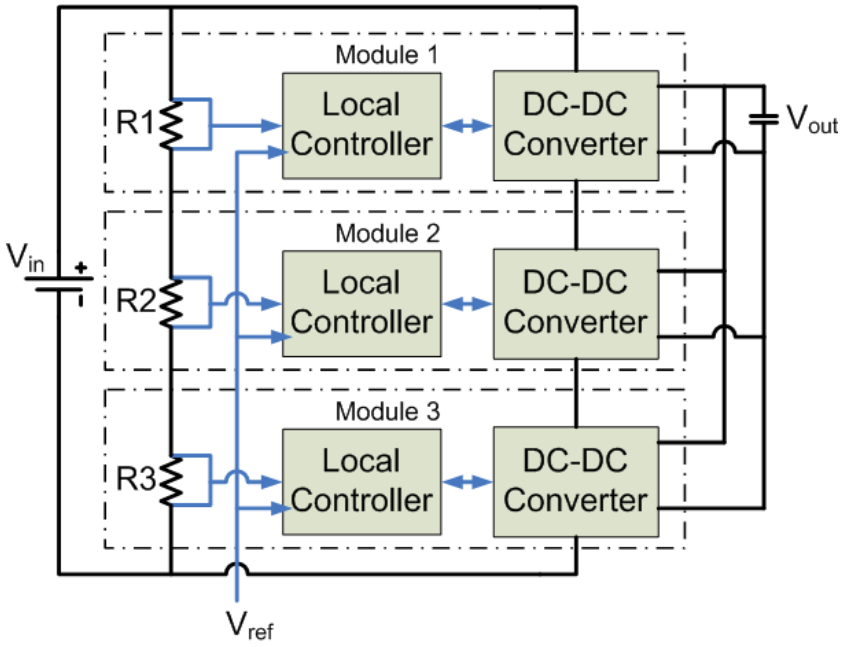


Figure 3.3: Power ratings-based load sharing with local control by way of a resistor stack. The voltage across each resistor serves as an input voltage reference for the corresponding module's controller.

An example application of ratings-based sharing is an ISOP circuit. The objective is to share power automatically in proportion to the individual module's ratings. The output voltage of each module is the same, while the input voltage of each module is subject to control. Since the input current of each module must match, the power provided by each module follows its input voltage. The SCM control will operate in a manner that sets each module's input voltage to the voltage of the respective rating resistor. Thus a module with a higher power rating will operate at a higher input voltage, and therefore provide higher power, in proportion to its relative set resistor. Low-power modules enforce low input voltage

and provide low power, and so on.

In Fig. 3.3, if the power rating of one module is double that of another, the resistor in the stack will have double the resistance and will double the input voltage reference for the corresponding module. The sum of the voltages is the total input voltage V_{in}. If another module needs to be removed or added, the voltage divider stack would adjust the reference voltages for the new configuration. Output current sharing follows the same ratio as input voltage sharing. Of course, if each module in the converter has set resistors with the same resistance (i.e. the same power rating), the voltage across the power rating resistors will be the same, thereby commanding even load sharing. Hence, ratings-based sharing works for both uniform and non-uniform load sharing.

A standardized system for resistor values could be established for automatic ratings-based sharing. Other weighting methods could be implemented as well. Dynamic weighting of the modules could be achieved by connecting capacitors in parallel with the resistors in the voltage divider. By varying the capacitance, sharing behavior during line disturbances would be established. Modules with higher parallel capacitance would react more slowly to the disturbance than modules with lower capacitance. A steady-state limit on module input voltage could also be enforced by connecting Zener diodes in parallel with the resistors.

One concern of ratings-based load sharing might be that it introduces another power path and a single point of failure in the system. If any of the set resistors fails, the converter will no longer operate properly. To overcome this problem, each module could include a switch that bypasses a failed rating resistor. This switch would be triggered in the event of a fault. Another perspective to consider is the overall reliability of rating resistors. It may be less likely for rating resistors to fail than a more complex converter that does not add another wire for load sharing. Further investigation on the system reliability of each approach would be necessary before conclusions about reliability can be made.

While the discussion so far has focused on the ISOP case, ratings-based load sharing can be applied to a variety of multiple module configurations. For instance, if the converter has a parallel input, ratings-based load sharing is still possible. One approach would be to find the dual of the voltage divider in a series input converter. The logical choice would be a current divider connected in series at the input of a parallel input converter. The "set" resistors in

the current divider should be weighted based on the power rating of each module. Hence, the current through each resistor would be weighted based on its respective module's power rating. By sensing this current, an input (or output) current reference would be established. Of course, very small resistors would need to be used; otherwise, there would be significant power loss. This strategy is shown in Fig. 3.4. Another approach would be to include a voltage divider or a current divider at the output of the converter to obtain the necessary reference signals.

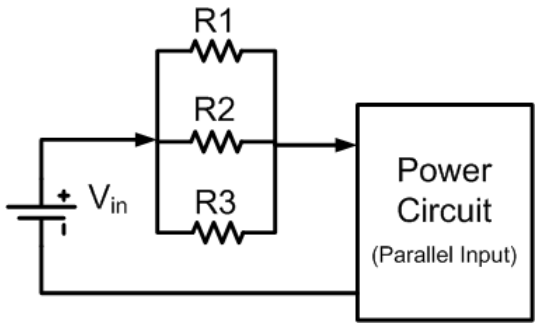


Figure 3.4: Power ratings-based load sharing for converters with a parallel input. The current through each resistor serves as a current reference for the corresponding module's controller.

3.3 Distributed Synchronization

The timing of events in a distributed system can have significant effects on the system's performance. For this reason, many distributed systems seek to synchronize the agents so that their actions occur at the appropriate time. To be clear, in this context synchronization does not mean that events occur at the same time but that they occur at the desired time. In the case of multiple module converters, synchronization is a form of coordination that is important due to its effect on switch turn-on timing. As explained previously, switch interleaving can substantially influence the output ripple of a converter.

The time dependent nature of switch interleaving poses an even greater challenge when the modules in a converter are locally controlled. Unlike in a single central controller, communication among distributed controllers appears to be necessary for synchronization.

If no communication among the modules is present, how can synchronization occur? The short answer is that there are numerous direct and indirect methods with varying degrees of communication that can address the timing problem. Since this project focuses on local control, communication was limited to a single bit with neighboring modules. No other communication among the modules was present although a global output voltage reference was provided to each module.

The switch interleaving approach using one bit of communication between modules takes the form of a repeating daisy chain. One module will send a signal that resets the digital PWM counter of the next module in the chain. This module will then delay the reset signal for a fraction of the switching period before passing the reset signal on to the following module. After this chain is completed and the final module has been reached, the reset signal will be sent to the first module to start the cycle over again. This simple method of distributed switch interleaving is shown in Fig. 3.5.

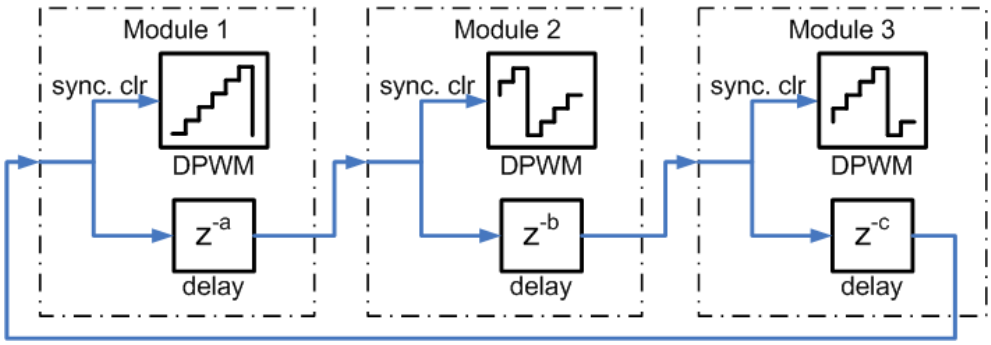


Figure 3.5: Distributed switch interleaving with a daisy chain approach. The delay introduced by each module need not be the same.

An immediate question that arises is how each module decides how long to delay the reset signal before passing it on to the next module. This fraction of the period by which each module is staggered is probably the most important parameter in a switch interleaving scheme since it has the greatest effect on the output ripple. When the modules are identically designed, as is often the case in multiple module converters, the desired delay will be an equal amount of time for each module. This means a T/n delay between the switching turn-on times, where T is the switching period and n is the number of modules.

If the modules are not identically designed, the delay time is a little more complex and a more fundamental examination is in order. In converters with parallel outputs, the output ripple is determined by the sum of the ripple of each module's inductor current (i.e. the ac components of the inductor current).

$$i_{ripple}(t) = i_1(t) + i_2(t) + \ldots + i_n(t) \tag{3.4}$$

This follows from Kirchhoff's current law where the sum of the output is equal to the sum of the input at a node. The dc components of the inductor currents do not have any effect on the output ripple and therefore do not need to be considered. The ripple of each inductor is primarily dictated by the voltage across it, V_L, and its inductance L since

$$\frac{di_L}{dt} = \frac{V_L}{L} \tag{3.5}$$

In steady state, the average inductor current will not change; therefore, all the change in the inductor current is ripple. Since the voltage V_L is approximately the same in each module of parallel output converters, the parameter that has the largest effect on the inductor ripple is its inductance. A module with low output inductance will have a larger ripple than a module with a higher output inductance. Hence, information about the output inductance of each module should guide the switch interleaving.

In modules with non-uniform load sharing, the output ripple of the module will often be proportional to the power rating. This is assuming that the inductor is selected based on a percentage ripple specification, as is generally the case. A module that provides a large amount of average current (and therefore power) can have a lower inductance and meet the ripple specification. For example, a 2% ripple on an average current of 20 A is larger than a 2% ripple on an average current of 2 A. The inductance needed by the higher power module is less than what is required by the lower power module.

In a multiple module converter with ratings-based load sharing, the power rating information can be used to infer information that can be useful for switch interleaving. Since the output inductance of a module is likely to be proportional to its power rating, the delay

that each module introduces in the interleaving scheme can be based on the voltage across the rating resistor. In the case of uniform load sharing (i.e. all the rating resistors have equal resistance), the desired delay of T/n for each module will result. For uneven load sharing, the delay that each module introduces will vary. More delay time will be alloted to the modules with larger ripple since their power rating resistor is larger. While this method does not ensure optimum switch interleaving, it does provide a base for improved switch interleaving for modules with non-uniform load sharing.

3.4 Digital Control

Local control of multiple module converters can be implemented in a number of ways. Digital control of power electronics has received significant interest in recent years. Nonlinear and adaptive control techniques can be implemented in a way that would be difficult or impossible with an analog approach [33, 34, 35, 36]. Additionally, there is considerable flexibility and ease in reprogramming a digital controller as opposed to an analog controller where the actual parts would have to be replaced to meet a changing control objective. Digital control also has a higher tolerance to signal noise and is relatively insensitive to component parameter variation. Another interesting aspect of digital control relates to the man-to-machine interface (MMI) [37]. Since many industrial and home electrical devices have an MMI which almost inherently comes with an embedded microprocessor, digital control can be implemented with the microprocessor already included. The shortened time to market of model-based design can cut overall cost and increase market share. Digital control is well suited for this design approach.

Of course there are a number of issues involved in digital control that must be considered as well. Some of them are challenges while others are just things to keep in mind when designing and implementing a digital controller and may have a negligible effect. These issues include signal conditioning, sampling, synchronization, quantization, finite precision arithmetic, limit cycle oscillations, and delays. Many of these issues are inherent to sampled data dynamic systems such as a digitally controlled power electronics. Methods of mitigating or eliminating these issues may be important in a variety of applications.

One major benefit of digital control is the ability of the controller to process data and implement control strategies in a fast, effective manner. In order for the controller to obtain the necessary information to perform the required functions, information from the analog converter is discretized so that it can be processed. This data acquisition path is where some of the challenges associated with digital control come into play.

First of all, the converter output needs to be sensed appropriately and converted from an analog signal to a digital signal. A Hall effect sensor, for instance, may be used to measure the output current. In order for the analog to digital converter (ADC) to work properly, the signal needs to be conditioned. The two main goals for signal conditioning are that (1) the sensor signal is amplified such that is uses the full scale range (FSR) of the ADC and (2) the signal is sampled so as to provide sufficient information yet avoid aliasing.

It is important to use the full scale range of the ADC so that quantization effects are minimized. Quantization is a critical issue when it comes to digital control. A given digital signal can be represented as a binary code that can only hold certain distinct values as opposed to a continuous range of values of an analog signal. The quantization step Q of an ADC can be expressed as follows where n is the number of bits of the binary code.

$$Q = \frac{FSR}{2^n} = LSB \tag{3.6}$$

The least significant bit (LSB) is often used in literature when discussing issues related to quantization. It can be seen that when quantization occurs, there is a loss in signal information of $\pm\frac{LSB}{2}$. This is often modeled as an additive noise known as the quantization noise. It is helpful to know that the maximum signal-to-noise ratio of the ADC as a function of the number of its bits is given by

$$\begin{aligned} SNR &= 10log_{10}\left(\frac{3}{2}2^{2n}\right) \\ &= 6.02n + 1.76(dB). \end{aligned} \tag{3.7}$$

This allows a designer to estimate the number of bits needed in the ADC if the desired

SNR is known. Keep in mind, however, that this does not take into account other sources of noise associated with the signal conditioning circuit or power converter but only considers the quantization noise. The actual SNR will be lower than what is estimated using the above equation.

Coming back to the second goal of signal conditioning, the signal must be sampled so as to avoid aliasing. This is a fairly fundamental concept in sampling. The Nyquist frequency f_C is the highest frequency that can be sampled without aliasing. The sampling frequency f_s must be at least twice the desired Nyquist frequency as shown below.

$$f_s \geq 2f_C \tag{3.8}$$

The time at which sampling occurs may also be important to consider. Often the sampling is synchronized with the switching in power converters. This means that the sampling frequency will be equal to the switching frequency. This is important to ensure that the sampled signal will accurately reconstruct the desired signal value (average output current, for example). The sampling need not occur exactly when the switching occurs; in fact, sampling in the middle of the switch-on period or in the middle of the switch-off period may produce the best results. Sometimes sampling rates that are much higher that the switching frequency may be used if more detailed information is necessary.

Once a signal has passed through the ADC stage, it will be processed by a digital signal processor (microcontroller, DSP, FPGA). Finite precision arithmetic is an inherent aspect of arithmetic and logic units. The results of their computations have limited precision which will pass on some error and possibly shift the system poles. While floating point arithmetic units can decrease the effects of finite precision arithmetic, fixed point arithmetic units are considerably cheaper and more widely used. Generally there is sufficient resolution in the fixed point arithmetic units that the effects of the finite precision arithmetic are not taken into account.

At the output of the digital controller, quantization also affects the converter. Probably the greatest challenge associated with the output of the digital to analog converter is the creation of a limit cycle oscillation (LCO). This occurs when the desired operating point lies between

to quantization states. As a result, the controller output will oscillate between a higher state and a lower state around the desired operating point. LCOs can cause unwanted instability and are a challenge uniquely presented by digital control loops. It is difficult to ensure that LCOs are eliminated, but there are some necessary conditions for their elimination [38].

Another significant challenge with digital control that deserves consideration is delay. The overall delay of the controller is a combination of delays produced at every step from ADC to switching signal generation. Some delays are more difficult to mitigate than others. Even if the delay introduced by a component (i.e. successive approximation ADC) can be reduced by using another component (i.e. flash ADC), accuracy can diminish or cost can increase. However, as electrical devices continue to improve in speed, these delays decrease. For example, a field programmable gate array (FPGA) can be used to swiftly compute switching control signals allowing for very fast response to transients in the system.

CHAPTER 4

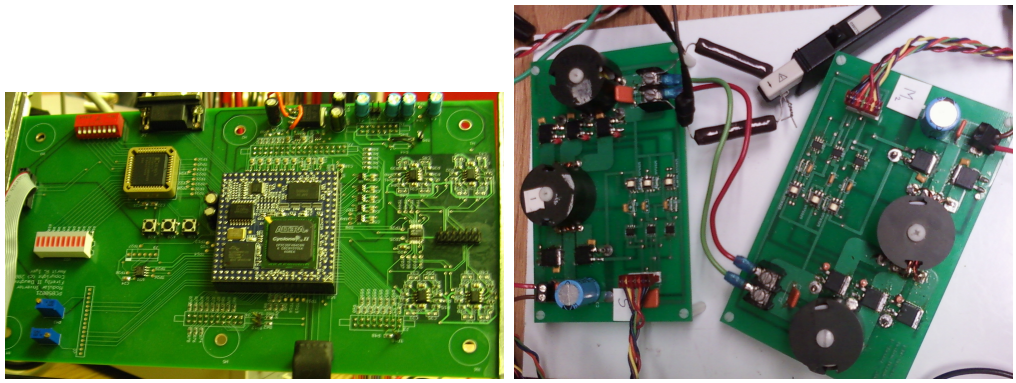
EXPERIMENTAL SETUP AND RESULTS

To verify the proposed local control with ratings-based load sharing scheme, an ISOP push-pull converter was tested in simulation and experiments. Simulation results focus on three push-pull modules since this setup furnishes the necessary level of detail without making the simulations cumbersome. For physical circuit implementation, six push-pull modules were built with three different power ratings, in pairs rated at 40 W, 20 W, and 10 W. To mimic the voltage requirements of a VRM in a computer server, the nominal conversion of 48 V to 1 V was selected. This will demonstrate the converter's ability to step the voltage down when there is a high voltage ratio. For the case of even load sharing, a lower input voltage of 30 V was selected.

The "set" resistor of each module is weighted according to the power rating of the module and provides an input voltage reference for the local SCM control. Relatively high values of resistance are used (on the order of 100 kΩ) so that power dissipation through them is kept low. Each module locally implements SCM control on a separate Altera Cyclone II FPGA. While the controls in this work do not require the computing capabilities of an FPGA, the FPGAs provide an easily configurable platform that lends itself to a research environment. Photographs of two push-pull modules and an FPGA control board used in this work are shown in Fig. 4.1.

4.1 Simulation Results

An ISOP push-pull converter was simulated with an ideal switch model. This is necessary to show the switch interleaving. If an averaged model was used in the simulations, the switching artifacts would not be visible. An example of the interleaved inductor current waveforms of



(a) FPGA control board (b) Push-pull modules

Figure 4.1: Hardware used to experimentally verify local control with ratings-based sharing.

three modules is shown in Fig. 4.2. To keep the simulations simple yet meaningful, three modules with a push-pull topology were simulated with open-loop SCM control.

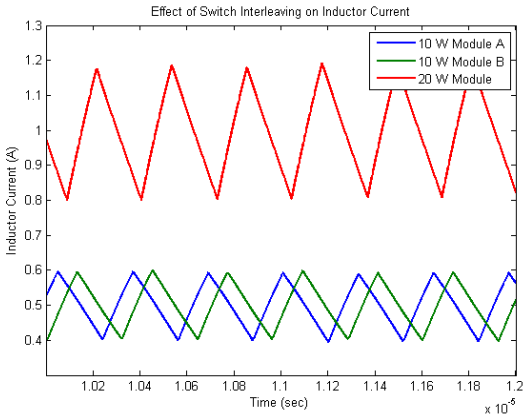


Figure 4.2: Inductor current waveforms of three modules with switch interleaving. The 20 W module has an average current of 1 A and the 10 W modules have an average current of 0.5 A.

The simulations were performed by combining Dymola and MATLAB Simulink software packages. The analog power components of the push-pull modules were modeled in Dymola with ideal switches and transformers. Dymola has an easy circuit layout interface backed by efficient circuit solvers. The Dymola model was placed within a MATLAB Simulink model using the Dymola block library. MATLAB Simulink was selected because it contains many

useful control libraries and analysis tools. The most useful library for this project is the Altera DSP Builder library. This library contained the components used in programming the FPGAs. A block diagram of the ISOP converter was created using these components. Thus, the simulations used the exact same controls as the actual FPGA would, and they contained many of the same digital control artifacts such as quantization and time delays. This similarity made transferring the controls from simulation to hardware quite smooth and easy. The base clock for the digital components in the simulations was 50 MHz. An 8 bit digital pulse width modulation (DPWM), a 30 bit integrator, and an 12 bit ADC were included. The circuit parameters of the simulated modules are listed in Table 4.1.

Table 4.1: Parameters of the simulated push-pull modules.

Module Power Rating	Parameter	Value
10 W	Transformer Turns Ratio	2:1
10 W	Input Capacitor	20 nF
10 W	Output Inductor	1 μH
10 W	Output Capacitor	100 pF
10 W	Inductor Series Resistance	10 mΩ
10 W	Power Rating Resistor	10 kΩ
20 W	Transformer Turns Ratio	4:1
20 W	Input Capacitor	20 nF
20 W	Output Inductor	0.5 μH
20 W	Output Capacitor	100 pF
20 W	Inductor Series Resistance	10 mΩ
20 W	Power Rating Resistor	20 kΩ

The switch interleaving scheme used in the simulations is a cycling reset approach. Each module has an input that will reset its digital PWM counter. Each module delays that reset input for an interval proportional to its share of the total input voltage. This delay is therefore proportional to the power the module provides. After delaying for some time, it will output a reset signal to the next module. This cycle of reseting results in switching signals that are staggered based on the power ratings on the modules. This is an example of neighbor information that can be used in local control. Also, if for some reason the interleaving scheme was interrupted, the modules would still be able to provide power to the load. The only adverse effect would be some periods of time where the output ripple

would be greater than other times. That is to say, the output ripple would be variable but bounded.

4.1.1 Uniform Load Sharing

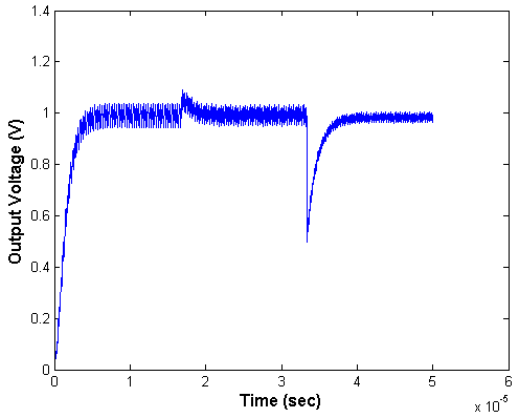
The first simulation focuses on uniform load sharing among the modules of the ISOP converter. They should have equal average input voltages and therefore equal average output currents. A converter with three 10 W modules was simulated under start-up, line step, and load step conditions. The output voltage, inductor currents, and module input voltages are shown in Fig. 4.3.

The load step doubles the load and causes the output voltage of the converter to dip to about 0.5 V but it soon recovers. The inductor current waveforms in Fig. 4.3 (b) exhibit a response time of less than 5 μs to the load change. All the modules have uniform average inductor current throughout disturbances in the load or line since their parameters are identical. The input voltages are minimally affected. A line step of 2 V has little effect on the output voltage as seen in Fig. 4.3 (a). Some small oscillations on the input voltage of the modules are observed but are seen to dampen out if simulated longer. The key point from these simulations is demonstration of even load sharing of locally controlled modules with switch interleaving.

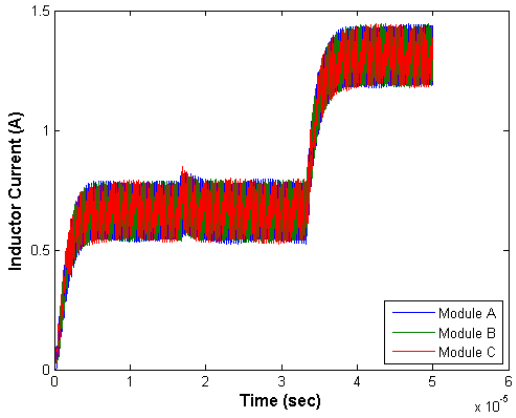
4.1.2 Non-Uniform Load Sharing

Two modules rated for 10 W and one module rated for 20 W were considered together. Since the 20 W module has twice the power rating of the other two, it should have twice the input voltage and twice the output current as compared to the 10 W modules. For more detail with the non-uniform load sharing case, the converter was simulated with load steps up and down and line steps up and down. The output voltage, inductor currents, and module input voltages are shown in Fig. 4.4.

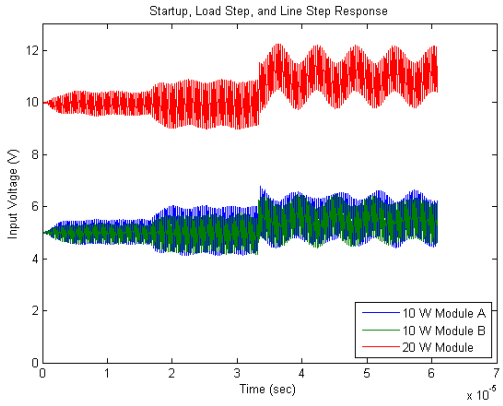
From the simulation results in Fig. 4.4, one can observe stable load sharing in the presence of both load steps and line steps. The output voltage deviation in the load step is larger than



(a) Output voltage

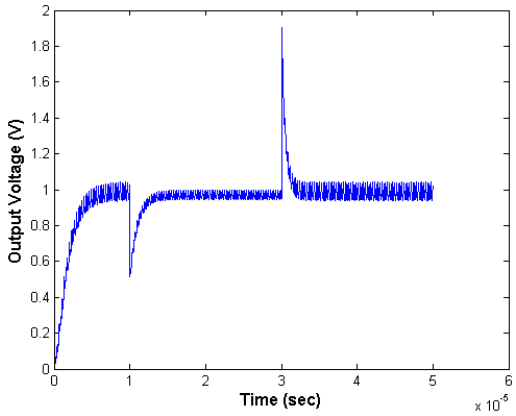


(b) Inductor currents

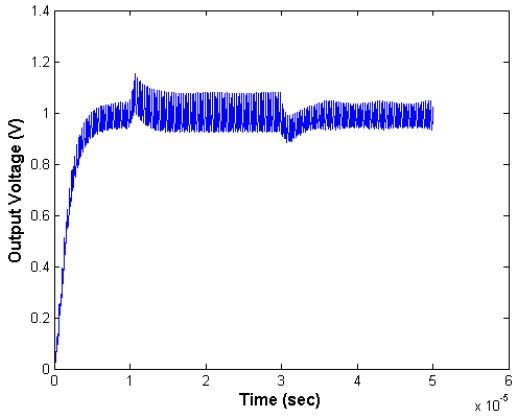


(c) Input voltages

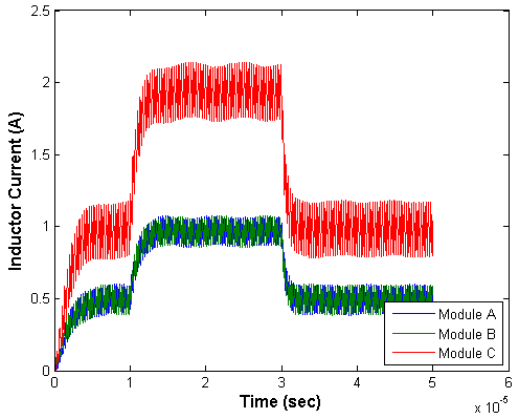
Figure 4.3: Simulated response of three module converter with uniform load sharing to a line step occurring at 16.7 μs and a load step occurring at 33.3 μs. Part (a) shows output voltage of the ISOP converter, part (b) displays the inductor current of each module, and part (c) shows the input voltage of each module.



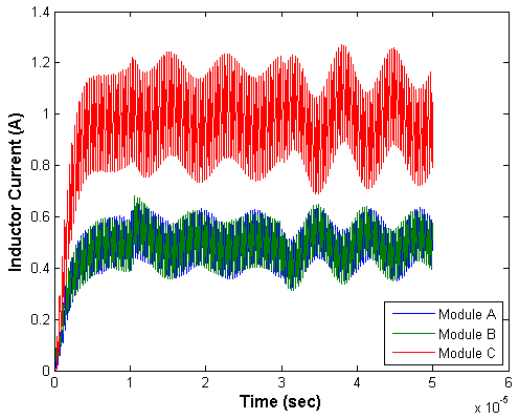
(a) Output voltage, load steps



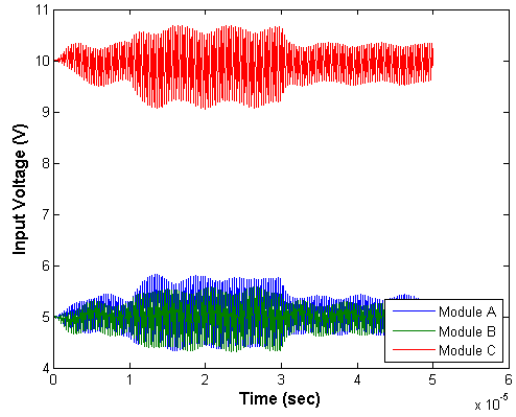
(b) Output voltage, line steps



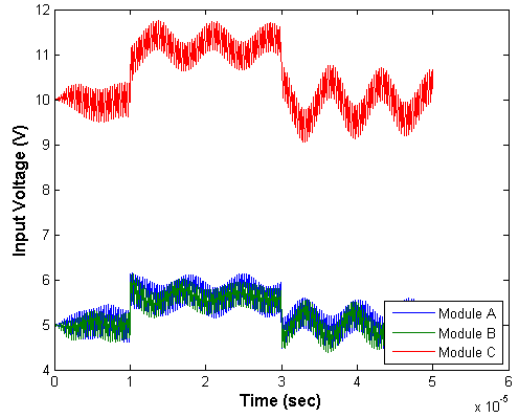
(c) Inductor currents, load steps



(d) Inductor currents, line steps



(e) Input voltages, load steps



(f) Input voltages, line steps

Figure 4.4: Simulated response of the output voltage, inductor currents, and module input voltages in three module converter with non-uniform power ratings. Part (a), (c), and (e) show the response to a load step-up occurring at 10 μs and a load step-down occurring at 30 μs. Part (b), (d), and (f) show the response to a line step-up occurring at 10 μs and a line step-down occurring at 30 μs.

the line step deviation since the simulated load steps are much larger in relative magnitude. The load step-up effectively doubles the load while the line steps are approximately 15 percent of the nominal input voltage. The inductor currents demonstrate swift response to load steps and exhibit uneven load sharing. The average input voltage of each module stays the same during load steps as is expected.

The converter response to line steps exhibits small oscillations in the input voltages and inductor currents. These oscillations dampen out if simulated for long enough. They are due to the relatively low impedance that the input capacitor of each module sees at its output. As will be seen in the experimental results, a physical converter does not exhibit continued oscillations in the input voltages. Other than the oscillations, the converter modules show resilience to the line steps. The inductor currents continue to provide uneven load sharing with the correct amount of average current. The output voltage also recovers quickly from the line steps.

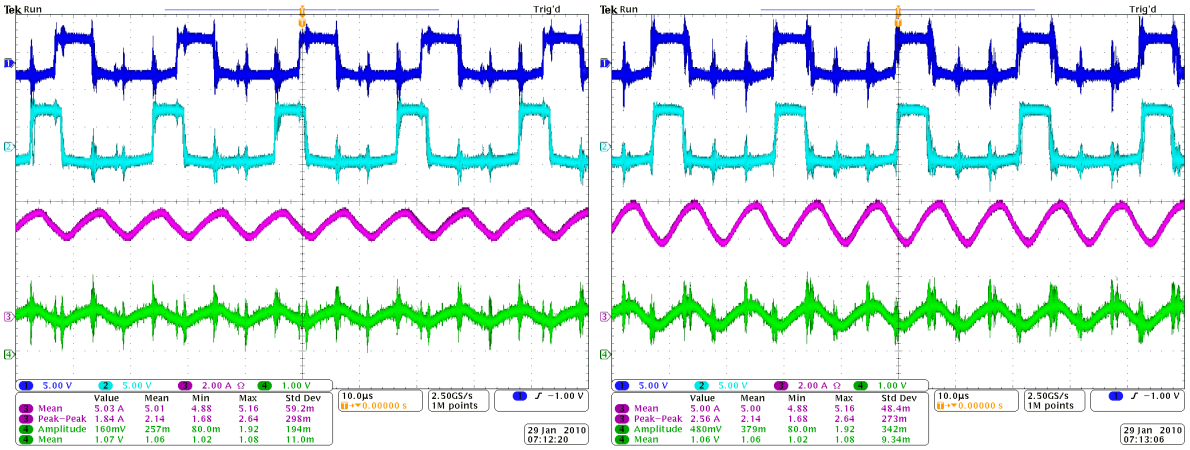
4.2 Experimental Results

In order to experimentally verify the simulation results, several push-pull modules were designed and built. Each module was locally controlled by implementing SCM control on an Altera Cyclone II FPGA with a base clock of 24 MHz. A 12 bit, successive approximation ADC was used to digitize the voltage across the rating resistor of each module. A signal conditioning circuit helped to protect each ADC, provide filtering, and linearly transform the signal when necessary. A global output voltage reference was supplied to each FPGA control board.

Experimental results demonstrate successful ratings-based load sharing of locally controlled modules. To begin with, two modules with different power ratings were connected in the ISOP configuration. Each module had a separate SCM controller. A resistor divider stack was used to prescribe power weights. The converter stepped 15 V down to 1 V with an approximately 5 W load. The main goal of this was to demonstrate some of the benefits of switch interleaving and stable, steady-state load sharing.

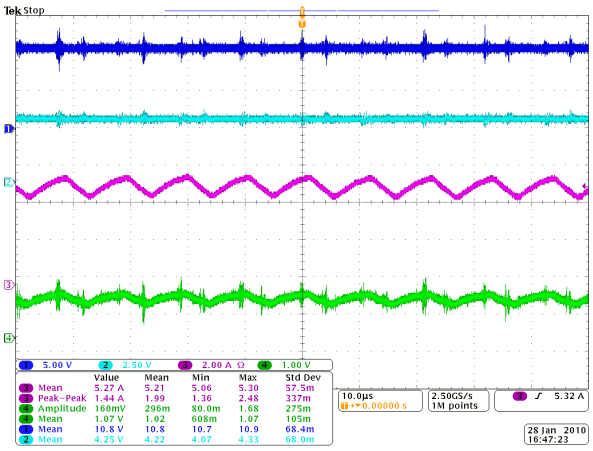
The decreased output ripple due to switch interleaving can been seen in Fig. 4.5 (a) and

(b). The peak-to-peak output current ripple is 2.56 A without interleaved switches and is 1.8 A when the switches are interleaved. This is an approximately 28% reduction in ripple gained from interleaving two modules. Stability of the converter can be seen in Fig. 4.5 (c) by observing each module's input voltage. Since one of the modules had twice the power rating of the other, the steady-state input voltage of that module is 10.6 V, approximately double the input voltage of the smaller module. This demonstrates stable, non-uniform load sharing in a simple application.



(a) Interleaved switching

(b) Synchronous switching



(c) Stable uneven load sharing

Figure 4.5: Operation of a locally controlled multiple module converter with uneven sharing. In (a) and (b), signals 1 and 2 are the gate signals for the switch $q1$ of both modules, signal 3 is the load current and signal 4 is the output voltage. In (c), signals 1 and 2 are the input voltages for the two modules in the converter.

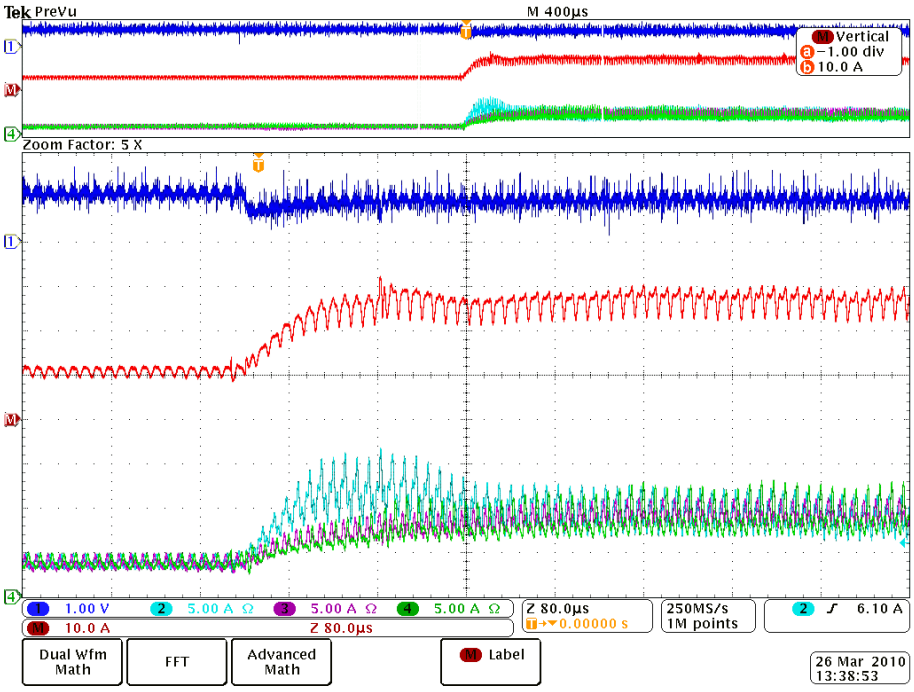
4.2.1 Uniform Load Sharing

More extensive experiments were performed to demonstrate uniform load sharing in a three module ISOP converter. In this case the total input voltage was 30 V and the output voltage was 1 V. The modules had rating resistors of equal value. There were, however, some significant differences in the actual modules themselves. Two modules were originally designed to provide up to 10 W and the third was designed for 20 W. This means that the turns ratio and the inductor were designed differently. Furthermore, since the transformers and inductors were hand wound, they exhibit considerable variation from the design. The turns ratio for the two 10 W modules was 1.64 : 1 and 2.13 : 1 while the turns ratio for the 20 W module was 5.2 : 1. The inductor of the 20 W module was approximately half the size of the other two modules and could respond to load changes more swiftly as a result. The response of the converter to a load step-up and step-down can be seen in Fig. 4.6.

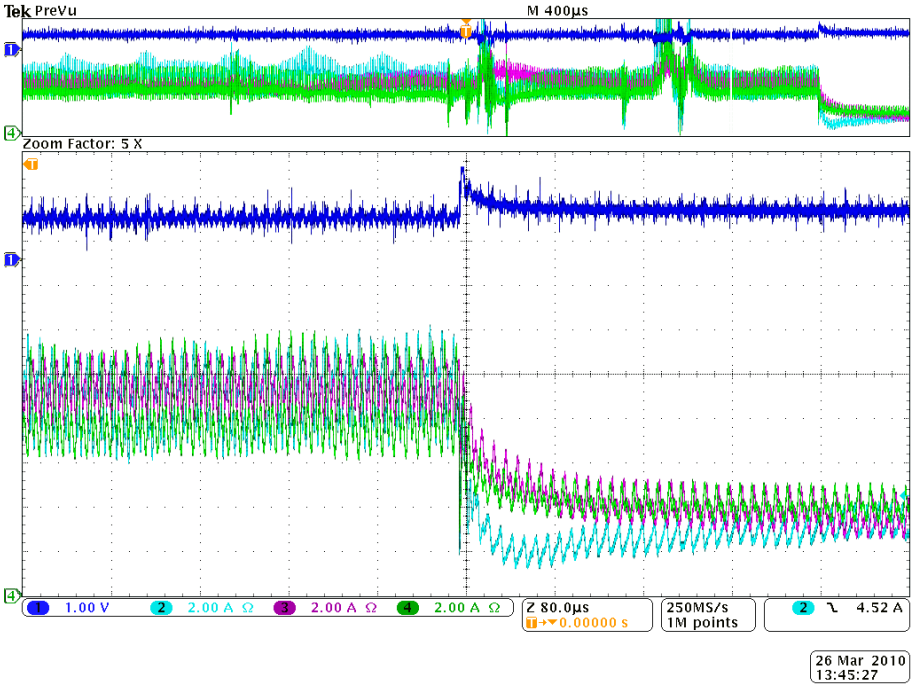
From the results, stable and even load sharing is observed. In steady-state operation before and after the load steps, the output current of every module is equal. As can be expected, the output voltage dips a little during the load step-up and increases during the load step-down. This is characteristic of converters operating with open-loop control. One can also see that one of the modules (the 20 W module) responds much faster to load changes than the other two. As mentioned before, this is due to the lower output inductance of the module designed with a higher power rating. Not only does the 20 W module respond faster, but it seems to overshoot in order to compensate for the other modules that have not reached the new operating point. It is important to note that, in spite of the relatively unintelligent nature of the modules and the wide variation in parameters, the modules work together to appropriately respond to load changes.

4.2.2 Non-Uniform Load Sharing

Non-uniform sharing was tested with a four module ISOP converter stepping 48 V down to 1 V. This is an example of an operation that might be needed in a computer data center where power is distributed on a 48 V bus and needs to be converted to the 1 V processor level. One 40 W module, one 20 W module, and two 10 W modules were connected together



(a) Increase load step



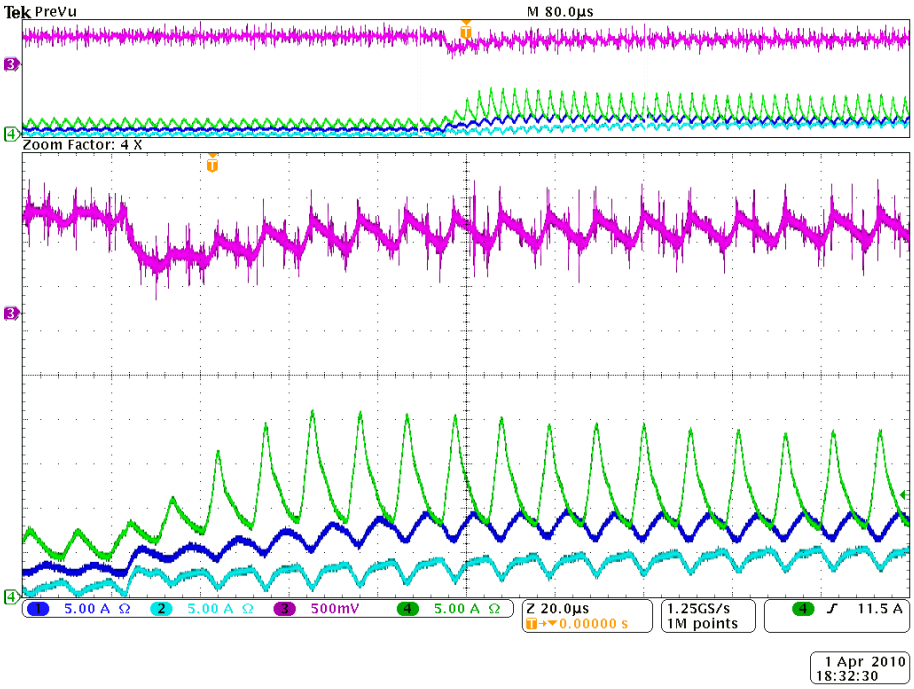
(b) Decrease load step

Figure 4.6: Response of a locally controlled ISOP converter with uniform sharing to load steps. In (a), the top signal is the output voltage, the middle signal is the total output current, and the bottom signals are output currents of the three modules. In (b), the top signal is the output voltage and the bottom signals are the output currents of each module in the converter.

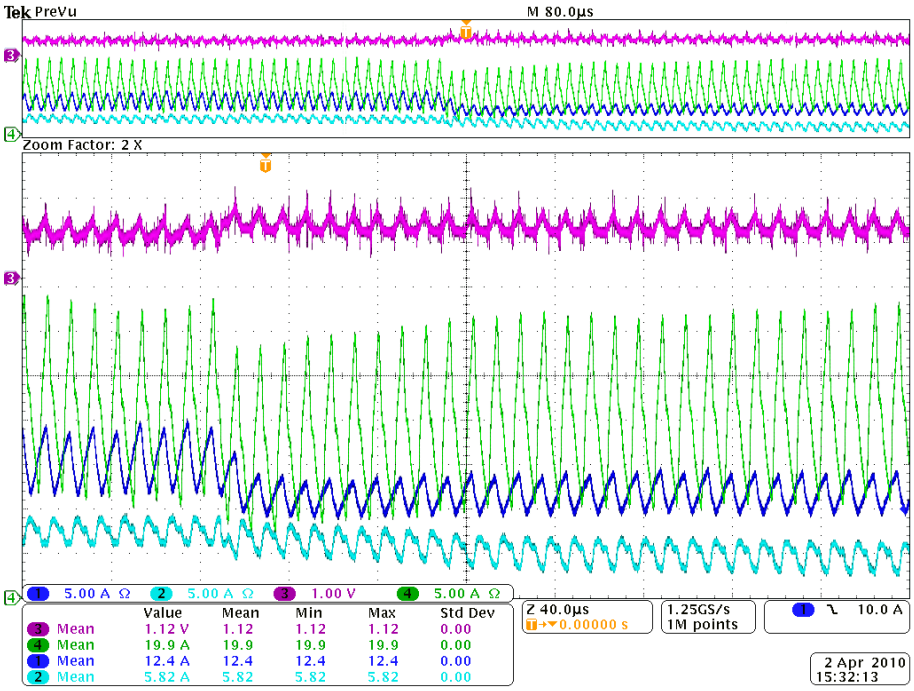
to perform this experiment. Each module's rating resistor was weighted in proportion to the power rating of the module. This resulted in an average input voltage of 24 V for the 40 W module, 12 V for the 20 W module, and 6 V for both of the 10 W modules. The modules' output inductance was designed based on a percentage ripple specification. Hence, the higher power modules had a lower output inductance. Waveforms showing the response of the converter to load steps are found in Fig. 4.7.

The results for the uneven load sharing case are quite similar to those for the even load sharing case. The modules in the converter demonstrate desired, stable load sharing in response to load steps. The output voltage profile follows that of a typical converter under open-loop SCM control. The output current of each module reaches steady state in approximately 160 μs. The total output current in this experiment was fairly high (on the order of 50 A) as might be expected in a server's central processing unit. The key point from this experiment is non-uniform load sharing among locally controlled modules based on module power ratings.

The modules with lower output inductance exhibit a swifter response to load changes. This has the effect of dynamic load sharing that deviates from the desired steady-state load sharing. Some might argue that dynamic load sharing is something that should be commanded, but the drawback of this strategy is that the converter response would be negatively affected. The modules' collective transient response would be limited by the slew rate of the slowest module. The output voltage would also deviate further from the desired level. Instead, by allowing the modules to respond to load changes based on their component parameters and not forcing dynamic sharing, the converter response will be faster. Of course, care must be taken to ensure that the modules do not violate component ratings.



(a) Increase load step



(b) Decrease load step

Figure 4.7: Response of a locally controlled ISOP converter with non-uniform sharing to load steps. In (a) and (b), the top signal is the output voltage and the bottom signals are output currents of three of modules. The output current of the second 10 W module is not shown.

CHAPTER 5

CONCLUSION

Multiple module converters offer considerable benefits in efficiency, performance, reliability, and maintainability. Considerably higher slew rates and lower output impedance are possible with multiple module converters. They can be designed to operate over a wide load range with high efficiency using module shedding techniques. Converters with high voltage ratios can be realized in one stage instead of traditional approaches that require multiple stages. There is also more flexibility when selecting components since the stress can be shared by the modules. In some cases this allows MOSFETs to be used in place of IGBTs. Due to benefits such as these, multiple module converters are being examined to address the increasing demands on energy conversion systems.

One design challenge in multiple module converters is making them truly modular without adding significant complexity. A modular design can improve reliability by introducing redundancy into the system. It also can support a converter that is easy to maintain and expand. This is useful in mission critical systems where the long term load can change considerably such as a computer data center. A modular design is based on independently controlled modules as opposed to modules that are centrally controlled. A fault-tolerant, distributed system that cooperatively meets the load demand is the general aim of modular converters.

Local control is a form of distributed control that provides the desired modular design benefits. Local control takes the perspective of the autonomous modules much like multi-agent frameworks do for larger systems. The emphasis in local control is placed on developing techniques that utilize inherent or local information in control algorithms that are implemented in each module. Limited or no communication between modules while still operating with global stability is a salient feature of this approach. Distributed synchronization tasks

like switch interleaving can be accomplished by using neighboring modules' information.

Load sharing in multiple module converters is important and can be especially challenging when the modules are controlled in a distributed fashion. Many approaches including master-slave, "democratic", and frequency based have been previously explored. These methods either require or are geared towards uniform load sharing. Non-uniform load sharing enables modules with disparate power ratings to work together and provides a flatter efficiency curve over a wide load range. This thesis presents a power ratings-based scheme that is simple and effective in controlling load sharing in a distributed converter. A resistive voltage divider creates a local input voltage reference for input series converters.

Simulation and experimental results presented in this thesis demonstrate local control with ratings-based load sharing. An ISOP push-pull converter with a high step-down ratio was selected for its practicality. Sensorless current mode control was digitally implemented on separate FPGAs to provide stable control of the modules. To decrease the output ripple and output filter size, the switching signals of the modules were interleaved. The simulated and physical converter exhibits a swift response to load and line disturbances. Both uniform and non-uniform load sharing are possible with ratings-based sharing and reach desired steady-state levels.

The current work could be extended in the future in a number of ways. Experimentation with ratings-based sharing for input parallel converters would provide greater depth. Further examination of how the converter responds to adding or removing a module is in order. Extending the paradigm presented here to address application specific difficulties faced in VRMs, telecommunication systems, data centers, and transportation systems is another important step. Fundamentally, developments in local control can continue to explore methods of utilizing local information that result in cooperative control of multiple module converters.

APPENDIX A

SIMULATION DETAILS

Figures A.1-A.4 show the MATLAB Simulink blocks used in simulating the ISOP push-pull converter. Figures A.5-A.7 show the Dymola blocks used in simulations.

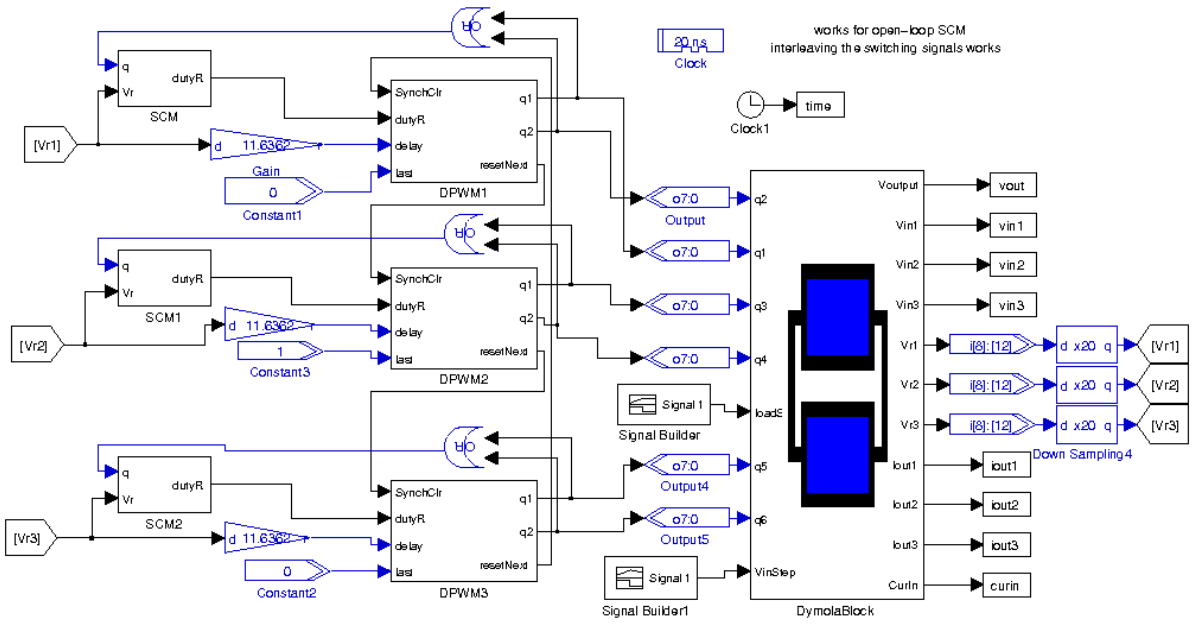


Figure A.1: Simulation block diagram of a three module ISOP converter. The SCM control block generates the duty ratio. The digital PWM block produces the switching signals and controls the switch interleaving. The Dymola block simulates the push-pull modules and power rating resistors stack. Converter response to load steps and line steps is examined.

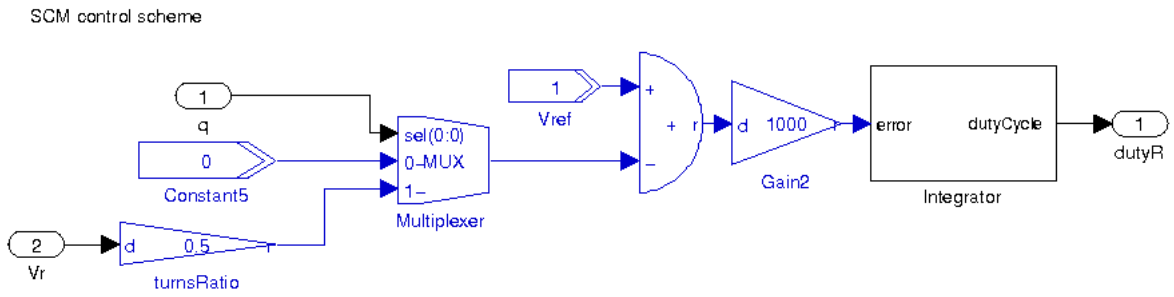


Figure A.2: SCM control block used in each module of the ISOP converter. The turns ratio will vary depending on the module. The gain before the integrator is necessary since the built-in integrator only accepts integer values and not fractionals.

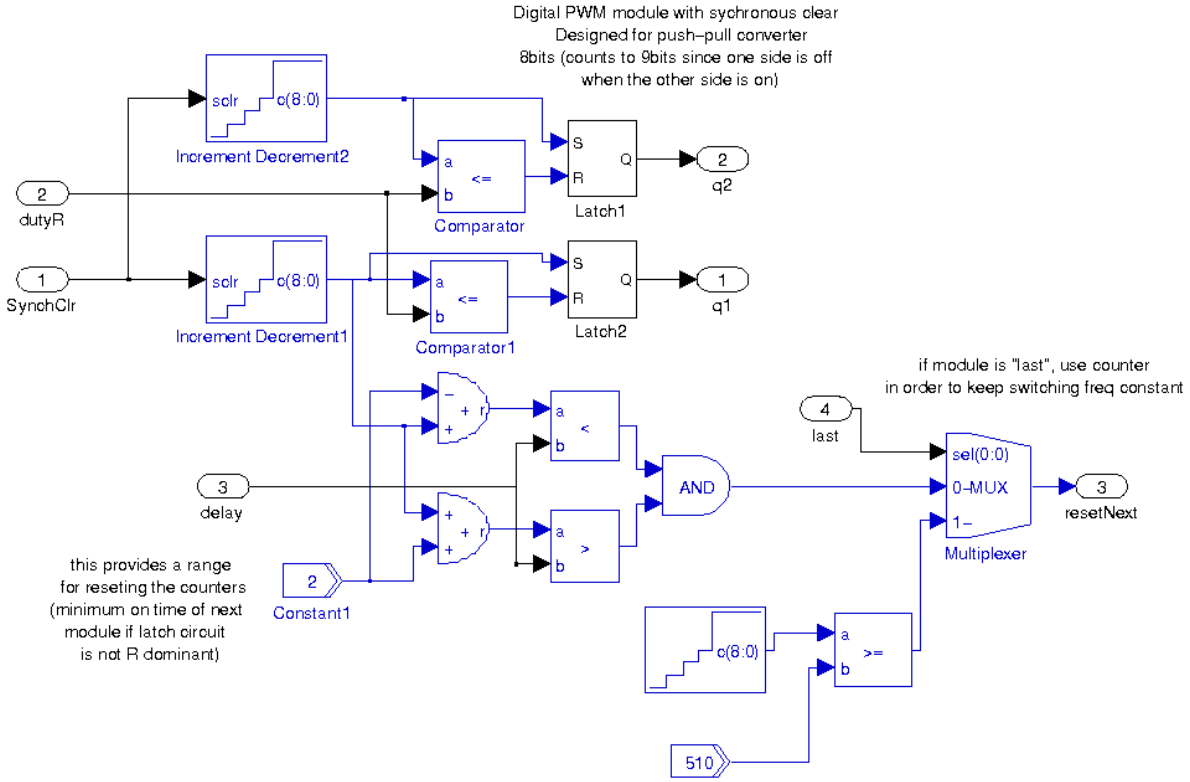


Figure A.3: Expanded view of the DPWM block used in simulating the ISOP converter. The output switch signals are generated by an 8 bit digital PWM process. The switch interleaving scheme is included in this block as well.

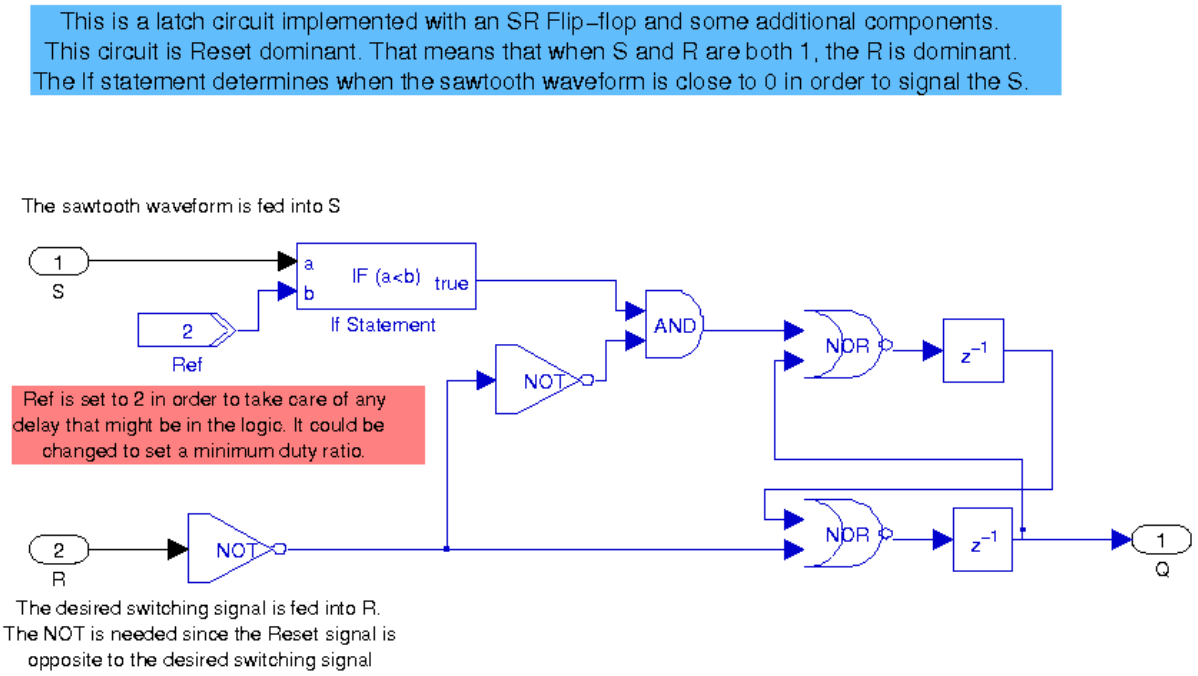


Figure A.4: Latch circuit used in simulations.

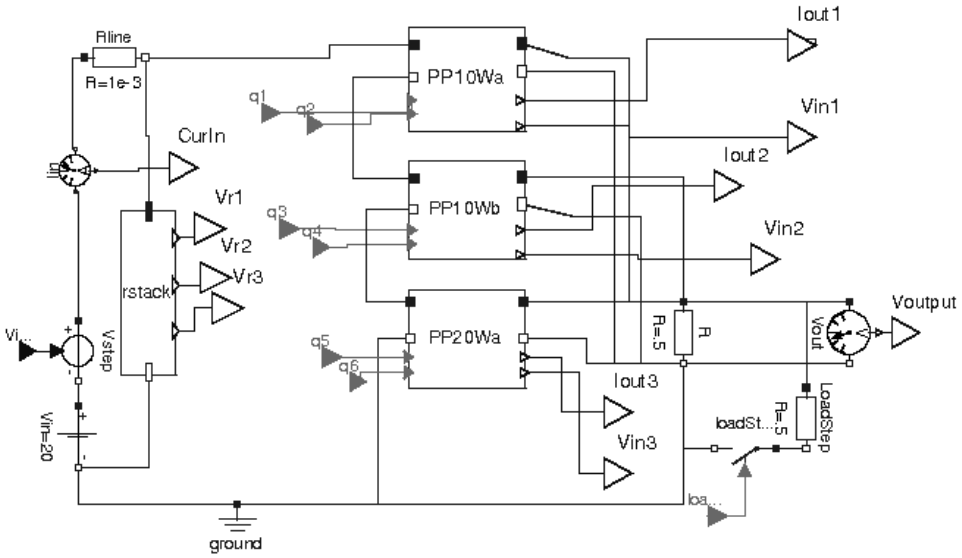


Figure A.5: ISOP push-pull converter with ratings resistors divider stack. This is the top level of the Dymola model.

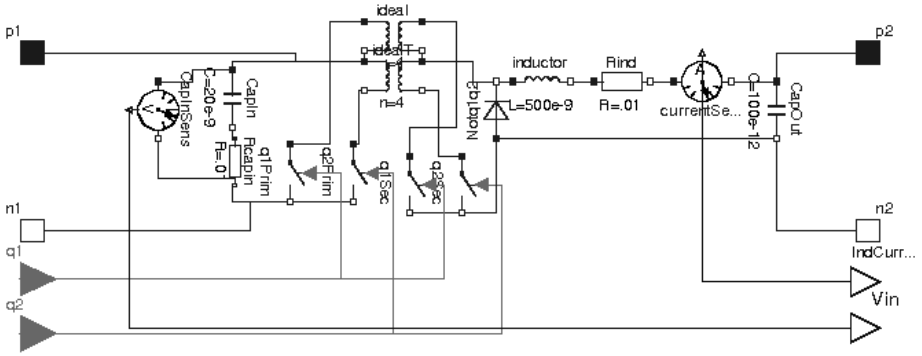


Figure A.6: The pull-pull module implemented in Dymola. An ideal transformer was used since a more detailed model is unnecessary. An ideal diode was selected to simplify the switching signals logic and has the same effect in simulations.

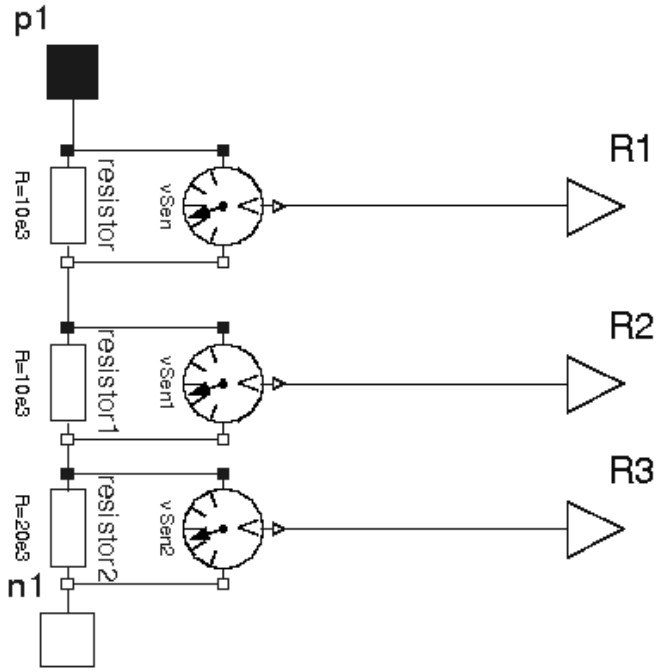


Figure A.7: The resistor divider stack with values of resistance selected based on each module's power rating.

Following is the MATLAB script used to postprocess the data from the simulations:

```
% post processing file

figure(1)
plot(time,vout)
ylabel('Output Voltage (V)');
xlabel('Time (sec)');
title('Startup, Load Step, and Line Step Response');

figure(2)
plot(time,iout1,time,iout2,time,iout3)
ylabel('Inductor Current (A)');
xlabel('Time (sec)');
title('Startup, Load Step, and Line Step Response');
legend('Small Module 1','Small Module 2','Large Module','Location','SouthEast')

figure(3)
plot(time,vin1,time,vin2,time,vin3)
ylabel('Input Voltage (V)');
xlabel('Time (sec)');
title('Startup and Load Step Response');
legend('Small Module 1','Small Module 2','Large Module','Location','SouthEast')
ylim([0 13]);

% figure(4)
% plot(time(1000000:1050000),iout1(1000000:1050000),time(1000000:1050000),
% iout2(1000000:1050000),time(1000000:1050000),iout3(1000000:1050000))
% ylabel('Inductor Current (A)');
% xlabel('Time (sec)');
% title('Effect of Switch Interleaving on Inductor Current');
% legend('Small Module 1','Small Module 2','Large Module','Location','NorthEast')
```

APPENDIX B

EXPERIMENTAL HARDWARE DETAILS

Tables B.1 and B.2 list the physical circuit parameters and the parts used to construct the ISOP converter. Figures B.1 and B.2 show the schematic and board layout used to create the push-pull modules.

Table B.1: Parameters of the physical push-pull modules used in experiments. Considerable variation in turns ratio and output inductance is due to the fact that both the transformers and inductors were hand wound.

Module	Power Rating (W)	Effective Turns Ratio	Output Inductance (μH)	Input Capacitance (mF)	Output Capacitance (μF)
S1	10	1.64:1	13.3	2.21	2.207
S2	10	2.13:1	7.7	2.21	1.888
M1	20	8.76:1	2.9	2.18	1.933
M2	20	5.2:1	4.7	2.19	1.897
L1	40	9.57:1	0.7	2.2	2.223
L2	40	6.8:1	3.7	2.21	3.295

Table B.2: Parts selected for the push-pull modules. The standard capacitors, resistors, Zener diodes, and wiring are not listed below since they were available in the lab.

Component	Manufacturer	Part Number
MOSFET	Fairchild	FDB8832
Gate Driver	Fairchild	FAN3122T
Gate Signal Transformer	Datatronics	SM76925
Transformer Core	Ferroxcube	P36/22-3B7-A400
Inductor Core	Ferroxcube	P36/22-3B7-A400
Load Resistors	Ohmite	20JR10E-ND
Instrumentation Amplifier	Analog Devices	AD620

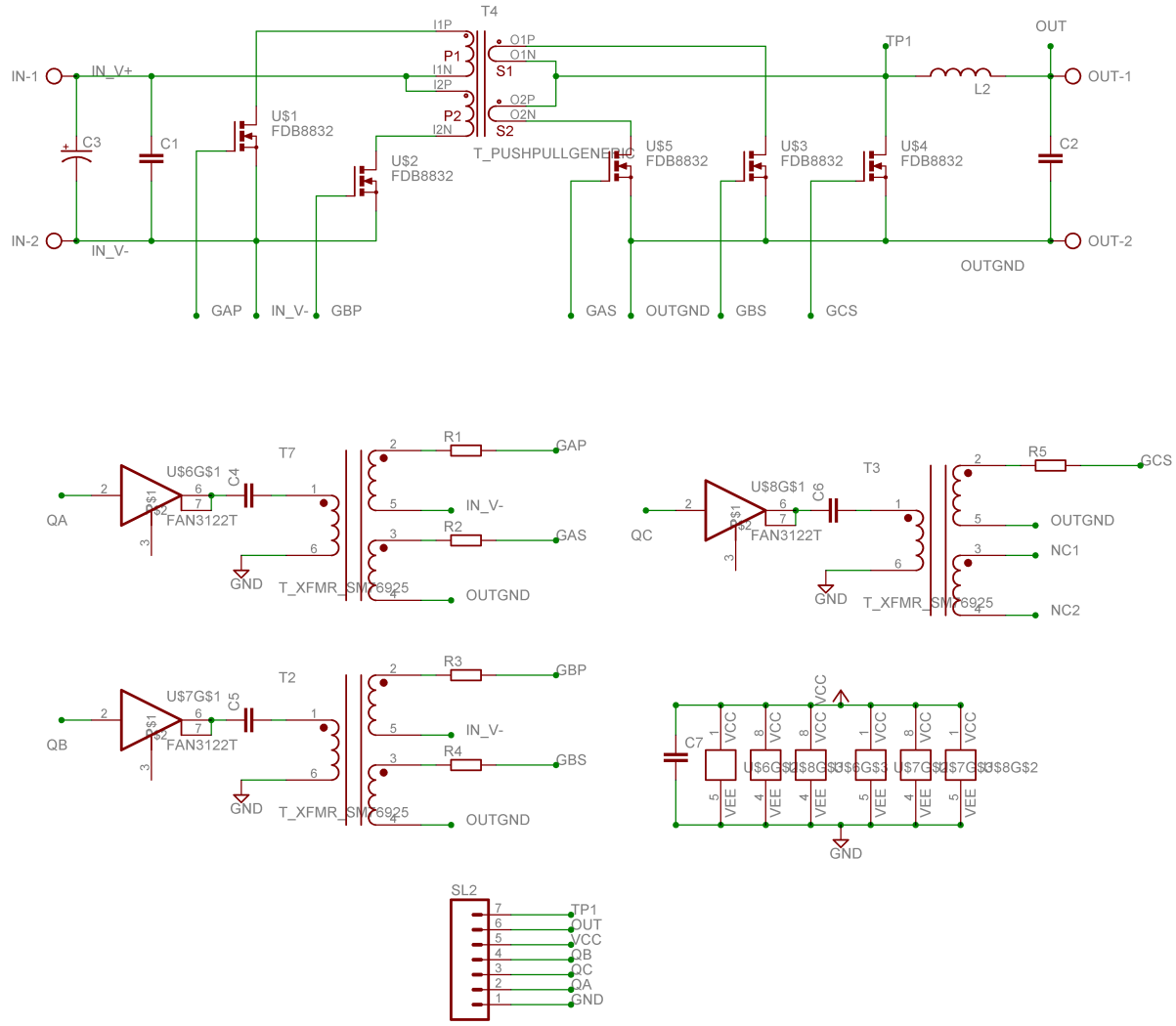


Figure B.1: Eagle schematic of a push-pull module. The top section displays the power paths. The lower parts are the gate drivers and connectors.

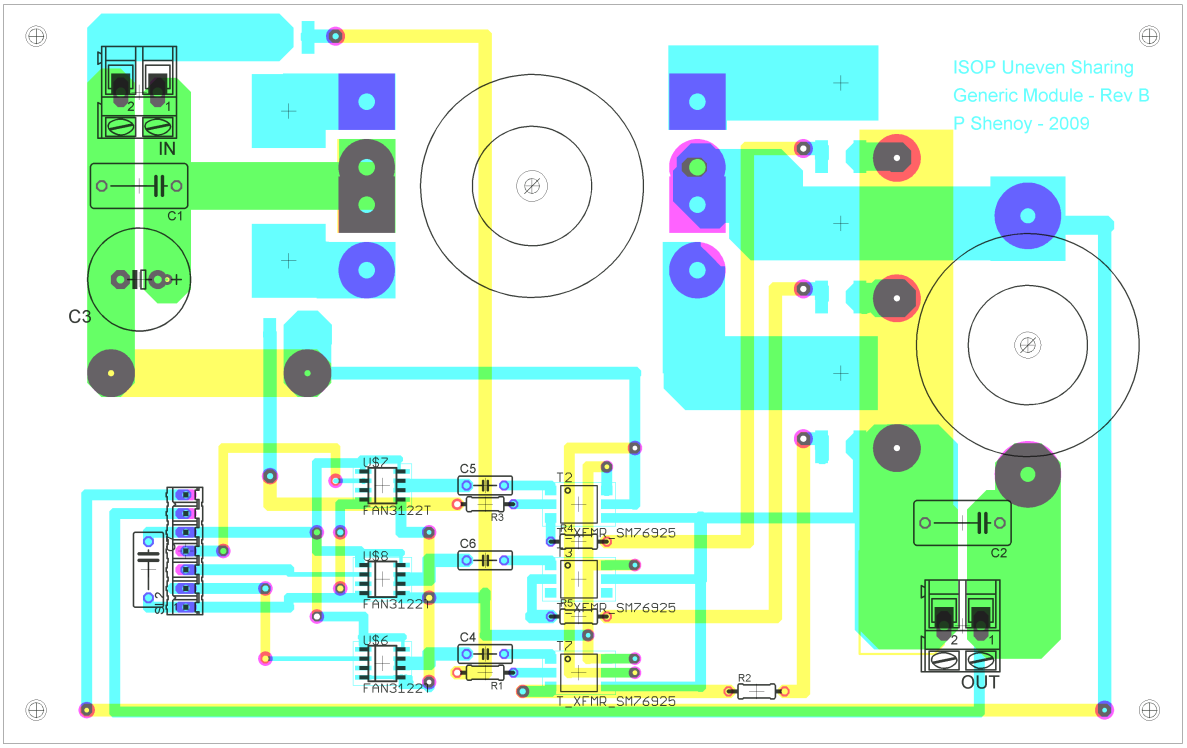


Figure B.2: Eagle board file of a push-pull module.

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