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ADVANCED PROCESS DEVELOPMENT FOR CONTACTS TO ALGAN/GAN
HIGH ELECTRON MOBILITY TRANSISTORS (HEMTS)

BY

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DISSERTATION

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ABSTRACT

High work function metals—Ni, Pt, Ir, and Au—were comparatively studied as Schottky metallizations to GaN and AlGaN/GaN heterostructures. Ni/Au, Ni/Pt/Au, Ir/Au, Ir/Pt/Au and Pt/Au Schottky diodes were fabricated on GaN and AlGaN/GaN substrates. Schottky barrier heights ranging from 0.8 to 0.9 eV were obtained as-deposited on GaN with ideality factors of about 1.05. The quality of the Schottky diodes was evaluated and their thermal stability also was studied. The interposition of Pt in Ni/Au and Ir/Au systems was found to improve the characteristics of the Schottky diodes. Ir/Pt/Au diodes were found to be more thermally stable than Ni/Pt/Au diodes. Ni/Au Schottky contacts exhibited good leakage response under thermal annealing for long periods. Microstructural studies were carried out on Ni/Pt/Au and Ni/Au Schottky contacts to elucidate the role of the intermediate layer, Pt, in the degradation of the Ni/Pt/Au metallization under long-term thermal anneal.

A selective-area silicon ion implantation process for ohmic contact resistance improvement to AlGaN/GaN high electron mobility transistors (HEMTs) was developed. Non-alloyed ohmic contacts with very low contact resistances of 0.2 - 0.24 Ω -mm were achieved with TLM pads fabricated using the Mo/Al/Mo/Au metallization. Simulations were carried out with SRIM to qualify the implantation process. Surface chemistry analysis was undertaken on the implanted AlGaN/GaN and GaN samples to determine the impact of implantation on the surface morphology of the AlGaN layer.

The developed ion-implantation process was used to propose fabrication schemes for novel high speed self-aligned and non-self-aligned AlGaN/GaN high electron

mobility transistors (HEMTs) employing Ir/Pt/Au or Ni/Au gate and non-alloyed ohmic contact metallizations.

To my family and friends, for their love and support in the most difficult times

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LIST OF ABBREVIATIONS

- 2-DEG – two-dimensional electron gas
- AES – Auger electron spectroscopy
- C-V – capacitance-voltage measurement
- CMOS – complementary metal-oxide semiconductor
- EDS – electron dispersive X-ray spectroscopy
- HEMT – high electron mobility transistor
- I-V – current-voltage measurement
- ICP RIE – inductively-coupled plasma reactive ion etch
- LPCVD – low pressure chemical vapor deposition
- MBE – molecular beam epitaxy
- MOCVD – metal-organic chemical vapor deposition
- PECVD – plasma-enhanced chemical vapor deposition
- SBH – Schottky barrier height
- SIMS – secondary ion mass spectroscopy
- STEM – scanning transmission electron microscopy
- TEM – transmission electron microscopy
- TLM – transfer line method
- XPS – X-ray photo-electron spectroscopy

CHAPTER 1

INTRODUCTION

1.1 High Power and High Speed Devices

The high band gap of III-nitride based materials (3.4 eV for GaN and 6.2 eV for AlN), high electrical breakdown voltage of the order of 10^6 V/cm and high saturated electron drift velocities of the order of 10^7 cm/s make these wide band gap materials suitable for high power applications. The formation of a 2-dimensional electron gas (2-DEG) in the AlGa_N/Ga_N system due to conduction band offsets and high piezoelectricity results in sheet concentrations of the order of 10^{13} cm⁻² and relatively high mobility values of the order of 1200 cm²/V · s [1, 2], making them suitable for high speed applications. Their low intrinsic carrier concentrations at high temperatures also provide for excellent performance at elevated temperatures.

Improvements in processing methods have led to the fabrication of AlGa_N/Ga_N HEMTs with very high speed performance [3]-[5]. Access resistance reduction is paramount in maximizing the speed of FETs. Leakage and barrier control are essential in maximizing the power output of HEMT devices. Contact resistance and channel resistance are the two resistances that are important in reducing the access resistance of AlGa_N/Ga_N HEMTs. Contact resistance minimization has led to the engineering of low resistance ohmic contacts to AlGa_N/Ga_N. Minimizing the source-drain spacing helps to reduce the total channel resistance . Since gates are usually fabricated after ohmic contact deposition, there is a constraint on the source-drain spacing.

The use of a self-aligned approach where the gate is deposited first and the side lobes of the gate are used to define the source drain region of the device gives better

saturation current performance and f_T . However, since ohmic contacts are usually annealed at about 850 °C on AlGaIn/GaN HEMTs, the gate metal degrades so much at this temperature that it becomes impractical to fabricate self-aligned devices in this manner. A two-step ohmic scheme with an initial ohmic annealed at 850 °C and the second at a lower temperature of 750 °C has been made by Lee et al. [6]. Recently, low temperature ohmic metallization using a Mo/Al/Mo/Au metallization scheme was demonstrated [7] and true self-aligned AlGaIn/GaN HEMTs based on this scheme having f_T of 82 GHz and f_{max} of 103 GHz were realized [8].

1.2 Motivation

Achieving the best performance for AlGaIn/GaN HEMTs would require the use of the best Schottky gate contact and the lowest access resistance possible. A systematic study of the viable Schottky metallization options and their Schottky barrier heights and leakage characteristics would be useful in determining the best Schottky gate contact. Thermal stability of these contacts and extra processing options that maximize their properties would assist in realizing the best gate control and very high power operation.

The reduction of the contact resistance of ohmic contacts and achieving the lowest access resistance is critical in fabricating high speed AlGaIn/GaN devices. Besides the engineering of metal choices and high temperature anneal to form low contact resistances, the employment of silicon implantation techniques to selectively dope the ohmic contact area very highly is a possible method of reducing the ohmic contact resistance. The formation of non-alloyed ohmic contact by silicon ion implantation on AlGaIn/GaN HEMTs opens the door to the realization of self-aligned AlGaIn/GaN HEMTs with very low access resistance [9]-[11].

The development of a process for making such devices is the motivation for this study. A successful process for reducing ohmic contact resistance using silicon ion implantation will be investigated. In addition, the best Schottky metallization and the process for fabricating these metallizations will be devised.

1.3 Organization

This study is divided into five chapters. A brief introduction to the problem will be presented in Chapter 1. In Chapter 2, various gate metallization options will be investigated. The thermal properties of these Schottky metallizations will also be systematically studied to determine the best Schottky metallization options among the high work function metals: Ni, Ir, Pt and Au. The performance of Pt metal interposition between Ni and Au and between Ir and Au will be discussed.

Simulation tools will be used to investigate the high dosage implantation ranges of low energy silicon ions in GaN and AlGaN in Chapter 3. Experiments which were conducted using GaN and AlGaN/GaN samples will be discussed. Secondary ion mass spectroscopy (SIMS) will be used to analyze the depth profiles of the implanted silicon. X-ray photoelectron spectroscopy (XPS) will also be used to analyze the surface chemistry of the implanted materials.

A systematic study of high temperature annealing of AlGaN/GaN heterostructures with different layer structures and substrate type will be undertaken in Chapter 4. SiC substrates which were found to be robust to temperature annealing as high as 1230 °C will be investigated. The 2-dimensional electron gas (2-DEG) of the AlGaN/GaN structure on sapphire, which was found to degrade at annealing temperatures of 1230 °C when the AlGaN barrier layer is thick and no AlN spacer layer is used, will be discussed.

In Chapter 5, a high-dosage, low-energy silicon ion implantation technique will be used to develop a process for low-resistance ohmic contacts using the Mo/Al/Mo/Au metallization to AlGaN/GaN HEMTs. The process will be qualified and taped out to achieve non-alloyed contacts with low contact resistances of 0.2 Ω -mm. Surface chemistry of the implanted AlGaN/GaN HEMT will also be analyzed using XPS.

Chapter 6 will conclude with future work to be done. Thermal stability of non-alloyed contacts at 500 °C and fabrication of silicon ion implanted HEMTs using the process devised in Chapter 3 will be outlined as the next study to embark on. The possible use of the same metallization for both Schottky and ohmic

contacts will be proposed. Several fabrication schemes for Si-implanted self-aligned and non-self-aligned AlGaN/GaN HEMTs will be proposed.

Finally, the benefits of applying silicon ion implantation to the fabrication of AlGaN/GaN HEMTs are immense. Low-resistance ohmic contacts would reduce significantly the access resistance of AlGaN/GaN HEMTs. Selective-area ion implantation can be used to make self-aligned AlGaN/GaN HEMTs with short source-drain spacing defined by the span of the gate side lobes. Thermally robust Schottky contacts are necessary for good gate control at high temperatures during high power operation.

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CHAPTER 2

SCHOTTKY CONTACT METALLIZATION TO GAN AND ALGAN/GAN

2.1 Carrier Transport in Schottky Contacts

Current transport at metal-semiconductor interfaces can occur by emission of electrons from the semiconductor over the barrier of the interface into the metal, or by quantum mechanical tunneling of electrons through the barrier, or by hole injection due to carrier recombination in the space-charge and neutral regions. Ideal Schottky contacts exhibit only emission over the barrier and are said to have ideality factors close to unity. Quantum mechanical tunneling tends to be common in ohmic contacts.

Rhoderick and Williams [1] provide extensive discussion on several theories that explain the emission of electrons over the barrier of a metal-semiconductor interface. Of all these theories, the thermionic emission and diffusion theories best explain the current transport mechanism in Schottky contacts.

2.1.1 Thermionic emission

Neglecting series resistance, the current density across a Schottky contact for a given applied voltage is given by the diode equation [1, 2]:

$$J = J_0 \left\{ \exp \left(\frac{qV}{nkT} \right) - 1 \right\} \quad (2.1)$$

By definition, the saturation current density J_0 is defined as

$$J_0 = A^{**} T^2 \exp \left(-\frac{q\phi_b}{kT} \right) \quad (2.2)$$

where $A^{**} = \frac{4\pi m^* q k^2}{h^3}$ is the Richardson constant, m^* is the effective mass of the semiconductor, ϕ_b is the Schottky barrier height (SBH), T is the temperature, the Boltzmann constant $k = 1.38 \times 10^{-23} \text{ m}^2 \cdot \text{kg} \cdot \text{s}^{-2} \cdot \text{K}^{-1}$, $q = 1.6 \times 10^{-19} \text{ C}$, Planck's constant $h = 6.626 \times 10^{-34} \text{ m}^2 \cdot \text{kg}/\text{s}$, n is the ideality factor of the Schottky diode, J is the current density and V the applied voltage. Under the assumption that $V \gg \frac{nkT}{q}$, which is almost always the case, the diode relation of Equation (2.1) can be written as

$$\ln(J) \simeq \ln(J_0) + \frac{q}{nkT}V \quad (2.3)$$

where the slope of the line in the linear region is given by $\text{slope} = \frac{q}{nkT}$ and the *intercept* = $\ln(J_0)$. The barrier height is extracted from

$$\phi_b = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{J_0}\right) \quad (2.4)$$

$$= \frac{kT}{q} \{\ln(A^{**}T^2) - \ln(J_0)\} \quad (2.5)$$

and the ideality factor, n , is extracted from $n = \frac{q}{kT} \times \frac{1}{\text{slope}}$.

2.1.2 Depletion capacitance

Under reverse bias, the Schottky contact to an n-type semiconductor has a depletion capacitance with the following expression [1, 2]:

$$\frac{1}{C^2} = \frac{2}{A^2 q \epsilon_s N_d} \left(\phi_b - V_n - V - \frac{kT}{q} \right) \quad (2.6)$$

where $V_n = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right)$, the effective density of states $N_c = 2 \left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}}$, A is Schottky cross-sectional area, ϵ_s is the electric permittivity of the semiconductor ($\epsilon_{GaN} = 9.5 \epsilon_0$; $\epsilon_{AlN} = 9.0 \epsilon_0$). A plot of $\frac{1}{C^2}$ vs. V gives the values of the electron carrier concentration N_d and the Schottky barrier height ϕ_b , respectively, as:

$$N_d = \frac{2}{A^2 q \epsilon_s} \times \frac{1}{\text{slope}} \quad (2.7)$$

and

$$\phi_b = |V_{intercept}| + \frac{kT}{q} \left[\ln \left(\frac{N_c}{N_d} \right) + 1 \right] \quad (2.8)$$

Owing to the interpolation involved, the Schottky barrier height extracted is that of flat band condition since as $\frac{1}{C^2} \rightarrow 0$ the depletion width goes to zero and image force lowering effects do not affect obtained values.

2.2 Schottky Contacts to GaN and AlGaN/GaN

The high bandgap of GaN and AlGaN semiconductors puts a restriction on the choice of metals for Schottky contacts to only high work function metals. n-GaN, for example, which has a bandgap of 3.4 eV and an electron affinity χ_{GaN} of 4.1 eV would require metals with work functions significantly higher than 4.1 eV to form Schottky contacts with appreciable Schottky barrier height. With increasing Al mole fraction in AlGaN, the electron affinity drops, so the barrier height is expected to increase for the same work function metals [3, 4]. However, high Al mole fractions would also make it difficult to form very good ohmic contacts due to the high barrier to metals. Although methods for enhancing the effective barrier heights by exploiting the piezoelectric effects can be explored [5], engineering the Schottky metal stack is always a more preferable approach.

Schmitz et al. undertook a comprehensive study of metal contacts to n-GaN [5, 6] and found that they were ohmic or rectifying depending on the metal work function. The high work function metals had strong rectifying behavior, but the best gate metallization for GaN-based HEMTs still remains to be determined.

2.2.1 Metallization options

Table 2.1 shows the metal work function for polycrystalline samples of selected metals. The choice of metals for Schottky metallization is then limited to Pd, Ir, Ni,

Au, and Pt. These are the metals that provide the highest barrier heights. However, some of these metals do not have good adhesion to GaN. Thermal stability concerns, as well, are factors which are important in selecting the best metallization for Schottky contacts.

Experimentally measured barrier heights on GaN indicate that the high work function metals give high barrier heights [6, 7]. The Schottky barrier height and leakage properties of the Schottky contacts determine which contacts will provide the best gate control in AlGaN/GaN high electron mobility transistors. Ni/Au and Pt/Au are the most commonly used [3] and [8]-[19]. Ir and Re Schottky contacts have also been investigated as possible gate metals with good thermal stability and leakage behavior [20, 21]. Despite having a lower metal work function, Ni is more often used than Pt as the Schottky metal of choice. One major reason for using Ni over Pt is the stronger adhesion of Ni to GaN than Pt. Au also has very poor adhesion to GaN.

Miura et al. [8, 9] have also investigated the interposition of Pt between Ni and Au as a possible gate metallization for GaN-based HEMTs. This serves two purposes. Firstly, these metals have the highest work functions and hence give the very high Schottky barrier necessary for good gate control. Secondly, a thin interfacial Ni layer ensures good metal-semiconductor adhesion and better contact. The performance of this contact scheme showed promise under thermal test in their study. A detailed study of these metallization schemes needs to be undertaken to determine the stack with the most ideal characteristics.

2.3 Experiments

A comprehensive investigation of Ni, Pt, Ir and Au metals on GaN and $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ Schottky contacts was carried out. The following five metallization options were studied:

1. Ni/Au (30/50 nm)

2. Ir/Au (30/50 nm)
3. Pt/Au (30/50 nm)
4. Ni/Pt/Au (2.5/30/50 nm, 7.5/30/50 nm)
5. Ir/Pt/Au (2.5/30/50 nm, 7.5/30/50 nm)

Schottky diodes were fabricated as shown in Figure 2.1. Optical lithography was used to define patterns with 300 μm diameter circular gaps. Mo/Al/Mo/Au (15/60/35/50 nm) ohmic contact metallization was deposited in the outer region by e-beam evaporation. Prior to ohmic contact deposition, SiCl_4 plasma treatment at -300 V for 1 min in a reactive ion etching (RIE) system was performed on the ohmic region. After lift-off, the ohmic metallization for the AlGaN/GaN layers was annealed at 575 $^\circ\text{C}$ for 20 minutes in a furnace under N_2 ambient and verified to have ohmic behavior. Schottky contact metallizations were then patterned and deposited by e-beam evaporation in the inner 250 μm diameter circle. Before ohmic and Schottky metal evaporation, surface oxide was removed by dipping samples in 2 : 1 DI water : HCl solution for 1 minute.

The layer structures of the samples used are shown in Figure 2.2.

2.4 Electrical Characterization

Current-voltage and capacitance-voltage measurements were used to characterize the diodes. The techniques of Sections 2.1.1 and 2.1.2 were used to extract the SBH, ideality factors, and carrier concentration N_d of the fabricated diodes on n-GaN. Thermionic emission theory was used to extract the SBH and ideality for the AlGaN/GaN HEMT using the electrical properties of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$. The electric permittivity of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ was calculated as:

$$\epsilon_{\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}} = 0.25 \epsilon_{\text{AlN}} + 0.75 \epsilon_{\text{GaN}} \quad (2.9)$$

where $\epsilon_{AlN} = 9.0 \epsilon_0$ and $\epsilon_{GaN} = 9.5 \epsilon_0$. The values extracted in this manner for AlGaN/GaN HEMTs are relative because the impact of polarization, and piezoelectric charges from the 2-DEG formation [10, 13, 14] were neglected. However, a relative comparison of the different metallizations would give an indication of the metallization with the best Schottky characteristics.

2.4.1 I-V and C-V measurements

I-V and C-V measurement results of the as-deposited and furnace-annealed diodes are presented in Figures 2.3 and 2.4 respectively. All metallizations show the same trend in behavior for diode samples annealed from 275 °C to 575 °C on both GaN and AlGaN/GaN. Initially, the SBH drops from its as-deposited value at 275 °C, then steadily increases to its maximum value at 500 °C, and then drops with further increase in temperature, implying that 500 °C is the optimal anneal temperature at which the Schottky contact to GaN and AlGaN maximizes its Schottky barrier height. Ir/Pt/Au and Pt/Au had the highest barrier height as-deposited. However after annealing at 500 °C for 2 minutes, the SBH for Pt/Au increased by 10% of its as-deposited value. Following Pt/Au are Ni/Au, Ir/Pt/Au and Ni/Pt/Au in terms of superior barrier height after 500 °C anneal for 2 minutes. Except for Ir/Au, which had the worst barrier height after 500 °C anneal for 2 minutes on GaN, the rest of the metallizations improved significantly after 500 °C anneal. The interposition of Pt between Ir and Au, and between Ni and Au, enhances the barrier height of the as-deposited diodes immensely when compared with the Schottky diodes without it.

For the AlGaN/GaN HEMT layer, the trend is basically similar to that of GaN except that the Ir-based Schottky contacts had similar SBH values after 500 °C anneal for 2 minutes with the Ni-based diodes. It is not clear why the SBH drops below the as-deposited value after 2 minutes of annealing at 275 °C for all the metallizations on n-GaN and AlGaN/GaN structures. However, as Figure 2.4 (b) shows, after annealing for a longer time at 275 °C, the SBH gradually increases above the as-deposited value, indicating that it is the quantity of heat applied to the

Schottky contacts that improves the barrier height. It is likely that annealing contributes in enabling the e-beam evaporated Schottky metallization form more intimate contacts to the GaN and AlGaN/GaN, creating enhanced barriers due to the difference of the metal work function and the semiconductor electron affinity.

A comparison of the results of this study with those of earlier study by Miura et al. [9] for n-GaN is presented in Table 2.2. A corresponding trend in the I-V SBH is seen. However, it is not clear why the C-V data in the work by Miura et al. show that the SBH from I-V measurements for the as-deposited Ni/Pt/Au diodes is greater than the corresponding SBH from C-V measurements. It is expected that the C-V values, representing flat band voltage conditions, should be greater than the I-V values as discussed in Section 2.1.2. Also, after annealing, their diodes show a huge difference between C-V and I-V obtained values. The extracted values from our study are also fairly accurate as the carrier concentration from the C-V measurements shows a value of $\sim 4 \times 10^{16} \text{ cm}^{-3}$, which is congruent with the specified value of $5 \times 10^{16} \text{ cm}^{-3}$.

2.4.2 Thermal storage in the furnace

The true test of the metallizations under study is their performance under thermal storage. Several authors have used different techniques to reduce leakage currents in n-GaN and AlGaN/GaN Schottky contacts [22]-[29]. Improvement in barrier height almost always implies reduction in leakage. Optimal thermal annealing generally gives improvements in SBHs and leakages for Schottky diodes to n-GaN and AlGaN/GaN [8, 9, 24]. Figures 2.5 and 2.6 show the performance of the different metallizations to n-GaN and AlGaN/GaN HEMT when subjected to thermal heating in the furnace at 500 °C for up to a cumulative time of 4 hours and 8 hours, respectively.

From the ideality factors of the cumulative thermal annealing of the Schottky contacts on n-GaN up to 4 hours at 500 °C , as shown in Figure 2.5, the degradation of the Ni/Pt/Au metallization is evident. The Ni/Pt/Au metallization with the

lowest Ni thickness (2.5 nm) degraded more in terms of the SBH values. Interposing Pt in Ir/Au metallization actually improves the barrier height significantly. The barrier for Ni/Au increased with annealing time, eventually attaining values higher than that of the Pt/Au contact after 2 hours of annealing time.

The Schottky barrier height of the metallizations in Figure 2.6 (a) shows that after 2 hours anneal, the Ni/Au metallization had SBH greater than 1.5 eV to the AlGaIn/GaN HEMT epilayer. This increase with annealing time follows the same pattern as the Ni/Au contacts to n-GaN. The interposition of Pt in the thin interfacial Ni/Au contacts (2.5 nm and 7.5 nm of Ni) resulted in SBH of around 1.0 eV after 4 hours of annealing and became constant at this value. The corresponding value of SBH for the equivalent Ni/Au was 50% more than that of Ni/Pt/Au. The drop in idealities of the Schottky diodes in the Ni/Pt/Au system shown in Figure 2.6 (b) implies that under thermal anneal the diode quality degraded. The smaller the thickness of the interfacial Ni, the sooner the degradation occurred under thermal anneal. For example, the SBH of the Ni(2.5 nm)/Pt/Au system dropped to 1.0 eV after 30 minutes anneal whereas the Ni(7.5 nm)/Pt/Au dropped to 1.0 eV after four hours anneal. Much like the case in n-GaN, the Ir/Au diode behaved similarly on AlGaIn/GaN. It had the lowest barrier height under thermal anneal. Interposition of Pt in the Ir/Au system improved its SBH quite significantly and presented a thermally stable contact with values close to the values of the Pt/Au system. The thickness of the interfacial Ir in the Ir/Pt/Au did not affect the SBH.

Figure 2.7 summarizes the Schottky barrier heights obtained for all the metallizations to AlGaIn/GaN: as-deposited, after 500 °C anneal for 2 minutes, and after cumulative anneal at 500 °C for 2 hours. The performance of the Ni/Au contact is worth noting. Even though the Pt/Au contact had the best values for as-deposited and after 2 minutes of annealing due to the higher metal work function value of Pt, as listed earlier in Table 2.1, after 2 hours of annealing, Ni/Au clearly had the most improved barrier height.

Although in the study of Miura et al. [8, 9] Ni/Pt/Au showed good performance, our study showed that Ni/Pt/Au Schottky diodes did not have better barrier height

compared to Ni/Au Schottky diodes under long-term thermal stress at 500 °C. The SBH of Ni/Au increased within the annealing time investigated. However, further thermal testing beyond 16 hours showed that Ir/Pt/Au maintained its stability while Ni/Au diodes failed. Therefore, it can be inferred that while Ni/Au has the best increase in Schottky barrier height with annealing time over all the other metallizations, Ir/Pt/Au (2.5, 7.5/30/50 nm) has the best thermal stability and Schottky barrier height combination. The leakage current of Ir/Pt/Au (2.5, 7.5/30/50 nm) also remained fairly constant after long-term thermal anneal.

The reason for the degradation of Ni/Pt/Au Schottky contact to AlGaIn/GaN is not clear. The drop in ideality of the diodes after a few hours of annealing needs to be investigated. Table 2.3 shows the leakage of the diodes as the ideality degrades. Ni/Au shows the best leakage response after 2 hours anneal in the furnace. This correlates well with the higher SBH observed. Hence, based on the thermal storage tests of the diodes, the Schottky contacts to AlGaIn/GaN from best to worst are: Ni/Au, Pt/Au, Ir/Pt/Au/, Ni/Pt/Au and Ir/Au. For long-term thermal usage, Ir/Pt/Au with thin interfacial Ir is a viable Schottky contact.

2.5 Microstructural Characterization

In order to investigate the behavior of the Schottky contacts, it is essential to undertake microstructural studies of select metallizations. Auger electron spectroscopy (AES), analytical cross-sectional scanning transmission microscopy (x-STEM) and energy dispersive X-ray spectroscopy (EDS) techniques were used to analyze the contacts for intermetallic and interfacial reactions after annealing. To elucidate the interfacial and intermetallic evolution after anneal, thicker interfacial metal layers were deposited. The following metal stacks were used:

1. Ni/Au (30/50 nm)
2. Ni/Pt/Au (30/30/50 nm)
3. Ir/Au (30/50 nm)

4. Ir/Pt/Au (30/30/50 nm)

5. Pt/Au (30/50 nm)

2.5.1 Ir/Au, Ir/Pt/Au and Pt/Au

Auger electron spectroscopy and analytical transmission electron microscopy studies on the Ir/Au, Ir/Pt/Au and Pt/Au Schottky contacts show that there was no intermetal mixing. It was not clear if there were interfacial reactions in the Ir-based metallizations. The metals probably require temperatures higher than 500 °C to form alloys. Moreover, these elements are atomically close (atomic numbers are 77, 78, and 79 for Ir, Pt, and Au, respectively) so it is possible that their mixing is not so favorable. Further studies are needed to understand the behavior of these contacts to n-GaN and AlGaN/GaN HEMTS.

2.5.2 Ni/Au and Ni/Pt/Au

Auger electron spectroscopy and analytical scanning transmission electron microscopy studies on the Ni/Au, Ni/Pt/Au Schottky explain the observed characteristics of these contacts under thermal anneal.

2.5.2.1 Auger electron spectroscopy (AES)

Auger electron spectroscopy analyses of the Ni/Au (30/50 nm) and Ni/Pt/Au (30/30/50 nm) to AlGaN/GaN Schottky contacts before and after 500 °C furnace anneal for 2 minutes and 1 hour are shown in Figure 2.8 (a)–(f). After 2 minutes anneal in the Ni/Au metal stack, a trace of out-diffusion of Ni to the surface is seen in Figure 2.8 (b). Complete mixing of Ni and Au occurred after 1 hour anneal as Figure 2.8 (c) shows. Up to 80% of the composition at the surface is Ni while Au had also spread towards the interface with AlGaN. Many Ni-Au phases form at 500 °C [30] and this explains the affinity of Ni with Au.

Comparing AES profiles of Figures 2.8 (d), (e) and (f) in the Ni/Pt/Au metallization stack, it is evident that there is mixing of the metals after 1 hour anneal with Ni out-diffusing through Pt all the way to the metal surface. Up to 70% composition of the surface is Ni. Significant concentration of Pt (40%) and Ni (30%) composition near the AlGaN interface suggests the possibility of Ni-Pt phase formation. There exists some Ni-Pt and Ni-Au alloy phases that form at 500 °C: NiPt, Ni₃Pt, Pt₃Ni, Ni_xAu_y [30] - [32]. This explains the diffusion of Ni into Pt during anneal. The formation of these Ni-Pt phases can be related to the degradation of the Schottky contact with time as the thin Ni layer gradually alloys with Au and Ni to form Ni-Pt and Ni-Au alloys. The Ni-Pt and Ni-Au alloys contact the AlGaN layer in parallel resulting in a mixed metal-semiconductor interface. This, consequently, changes the Schottky properties of the Ni/Pt/Au metallization.

2.5.2.2 Analytical cross-sectional scanning transmission electron microscopy (STEM) characterization

STEM analyses of the Ni/Au and Ni/Pt/Au contact metallizations to AlGaN confirm the intermetal mixing observed in the AES plots of Figure 2.8. Figure 2.9 shows the scanning transmission electron microscopy (STEM) images of the as-deposited Ni/Au and Ni/Pt/Au contacts to AlGaN/GaN.

In the Ni/Au contact, after 1 hour anneal at 500 °C, the low magnification STEM image of Figure 2.10 (a) shows the accumulation of Au at the interface. The high resolution image of Figure 2.11 (a) shows the in-diffusion inlet of gold to the AlGaN interface with Ni out-diffusing away from the surface, corroborating the observation in the AES of Figure 2.8 (c). Clearly, there is no interfacial reaction at the metal-AlGaN interface after 1 hour annealing at 500 °C as the high resolution STEM image of Figure 2.11 (b) indicates. A Z-intensity profile characterization of the interface area is shown in Figure 2.11 (c). The Z-intensity is proportional to the atomic number of the element Z. The atomic number of Au is 79 and that of Ni is 28. Given the high Z-intensity at the metal-AlGaN interface, it is conclusive that a thin Au-layer of at least 2 nm width had uniformly formed at the interface. The

sharpness of the Z-intensity profile at the interface concretely shows that there is no interfacial reaction with the AlGa_N. Therefore, the mechanism of improved Schottky barrier height in the Ni/Au Schottky contact to AlGa_N/Ga_N compared to all the other metals under thermal anneal as shown by the I-V results of Figure 2.6 can be explained from the observation of a sustained accumulation of gold at the interface which creates a uniform layer of Au contact to AlGa_N/Ga_N. As the height of the accumulated Au layer increases beyond the critical Debye length necessary for contacts, an increasing barrier height is obtained that approximates a Au-AlGa_N Schottky contact. Since the metal work function of Au is near that of Ni, a rise in SBH is seen when the metal contacting the AlGa_N (Ni_xAu_y) becomes more of Au. After 1 hour anneal, enough Au had accumulated to form a 2 nm Au-rich region at the interface ($y \gg x$). Away from the interface, the Ni concentration rises such that $x \gg y$ until we get into the very Au-rich regions as shown in Figures 2.8 (c), 2.11 (a) and 2.11 (b).

Under annealing, the Ni/Pt/Au metallization exhibited the formation of Ni-Pt phases as shown in Figure 2.10 (b). Au also accumulated at the interface, but unlike the case in the Ni/Au metallization, there is no uniform accumulation of Au at the interface. No interfacial reaction was observed as shown in the high resolution image of Figure 2.12 (a). The formation of mixed interface of Au-AlGa_N and (Ni-Pt)-AlGa_N explains the degradation of barrier height in this metallization as observed in the anneal results of Figure 2.6. The degradation of idealities further solidifies the impact of the observed mixed interfaces. Even though a thick Ni (30 nm) was used in the Ni/Pt/Au contact for STEM studies, mixed interfaces were observed; hence, in the Ni/Pt/Au Schottky contacts where Ni was 2.5 nm and 7.5 nm, it is expected that the Ni is more aggressively consumed in forming Ni-Pt such that a more mixed interface of Pt, Au, and thin Ni-Pt to AlGa_N results. The thicker the interfacial Ni, the degradation increased more with annealing time. The reason for this is due to the formation of Ni-Pt mixtures. The thicker the interfacial Ni, the more Ni there is for the formation of Ni-Pt alloys so, as the contact is continually annealed, a more mixed interface results degrading the Schottky contact

until all the interfacial Ni is consumed in forming Ni-Pt. In the thinner interfacial Ni metallization (2.5 nm) , this happens sooner than in the thicker interfacial Ni (7.5 nm) and so it reaches a fixed SBH value during annealing sooner as seen in Figure 2.6.

Due to the fact that the metallization on the AlGa_N interface is no longer uniform after annealing, the barrier seen is a mixture of many paths from the metal to the AlGa_N. This is like resistors in parallel where the net resistance is smaller than the smallest value. Hence the SBH is smaller that one would expect for either Ni, Ni-Pt, Pt or Au alone. Annealing thus creates multi-paths due to a mixed interface of (Ni-Pt)-AlGa_N and Au-AlGa_N as shown in the illustrative schematic of Figure 2.13. Also, the Ni-Pt phases form at the grain boundaries with dark spots segregated at these grain boundaries as shown in Figures 2.12 (b), (c) and (d). The dark spots are probably due to some kind of voids. These spots and the Ni-Pt mixture boundary structures may also contribute to the degradation in barrier height and diode idealities.

Hence the degradation of the Ni/Pt/Au metallization can be attributed to the presence of Ni-Pt and Ni-Au phases and the formation of mixed interface during thermal anneal, while the improved performance of the Ni/Au contact is due to the accumulation of uniform Au-rich areas at the interface. No interfacial reactions of the metal with the AlGa_N layer were observed even after 1 hour anneal for both metallization contacts.

2.5.2.3 Electron dispersive X-ray spectroscopy (EDS) elemental characterization

EDS quantification of the Ni/Au and Ni/Pt/Au contacts at selected points after 1 hour anneal at 500 °C is shown in Table 2.4 for the selected points in Figures 2.14 (a) and (b). The asterisked numbers are inaccurate and of negligible value since the detected signal is less than the sigma value, meaning that the elements at those points are almost non-existent or have very low trace values. Clearly this EDS-obtained elemental quantification is in complete agreement with the Auger

profile earlier obtained in Figure 2.8 (c) and (f). In both metallizations, Ni was detected near the metal surface and up to 20% of Au was observed near the interface. STEM showed that very Au-rich areas form at the interface that are about 2 nm in width in the Ni/Au Schottky contacts after anneal. EDS quantification points have dimensions bigger than this width so the EDS values are values close to the interface and not exactly at the interface. Hence, the lower Au percentages.

The EDS elemental map micrographs of Figures 2.15 and 2.16 support the AES and TEM observations that:

1. There is a clear AlGa_N interface
2. Au spreads along the interface after anneal
3. Ni out-diffuses to the surface
4. Pt and Ni mix up

Since Ga and Pt energy peaks overlap, the Ga map in the micrographs of Figure 2.16 contain noise and hence may seem as though Ga out-diffused into the metals. However, the clear interface seen in the STEM images and the fact that Ga was not detected in the AES profiles is further proof that the interface integrity is maintained in these contacts.

2.6 Conclusion

A comparative study of Ni/Au, Ni/Pt/Au, Ir/Pt/Au, Ir/Au and Pt/Au Schottky contact metallization to n-GaN and AlGa_N/Ga_N HEMT was conducted. These Schottky contacts exhibited the same behaviors as they were progressively annealed from 275 °C to 500 °C in the furnace for 2 minutes. Ir/Au had the worst Schottky barrier and leakage performance while Ni/Au gave the best performance under thermal storage until the diodes failed. The interposition of Pt improved the performance of the Ni/Au and Ir/Au Schottky metal schemes. However, the Ni/Pt/Au metallization performed poorly after annealing at 500 °C for a long time

because of the formation of Ni-Pt phases causing the Ni to diffuse upward into the Pt and creating mixed interfaces. This caused a lowering of the SBH. The uniform accumulation of Au at the interface of the Ni/Au contact after long hours of annealing is responsible for the increase in SBH of Ni/Au contact under thermal anneal.

2.7 Tables

Table 2.1: High work function metals [1, 33]

Metal	Metal Work function Φ_m [eV]	Calculated Max SBH $\Phi_B = \Phi_m - \chi_{GaN}$ [eV]	Contact good for
Ta	4.25	0.15	ohmic
Al	4.28	0.18	ohmic
Ti	4.33	0.23	ohmic
Mo	4.6	0.5	ohmic/Schottky
Au	5.1	1.0	Schottky
Pd	5.12	1.02	Schottky
Ni	5.15	1.05	Schottky
Ir	5.25	1.15	Schottky
Pt	5.65	1.55	Schottky

Table 2.2: Comparison with previous results

Schottky Metal	As Deposited				After Furnace Anneal (500 °C, 2min)			
	I-V SBH [eV]	Ideality	C-V SBH [eV]	N_d [cm^{-3}]	I-V SBH [eV]	Ideality	C-V SBH [eV]	N_d [cm^{-3}]
Ni/Pt/Au (2.5/30/50nm)	0.78	1.07	0.81	$3.94\text{E}+16$	0.89	1.07	0.94	$3.83\text{E}+16$
Ni/Au (30/50nm)	0.74	1.05	0.77	$3.93\text{E}+16$	0.91	1.06	0.96	$3.94\text{E}+16$
Ir/Pt/Au (2.5/30/50nm)	0.90	1.05	0.92	$4.12\text{E}+16$	0.90	1.04	0.90	$4.12\text{E}+16$
Ir/Au (30/50nm)	0.76	1.06	0.76	$3.93\text{E}+16$	0.84	1.05	0.85	$4\text{E}+16$
Pt/Au (30/50nm)	0.92	1.05	0.94	$4.04\text{E}+16$	0.98	1.05	0.99	$4.06\text{E}+16$

(a) I-V and C-V SBH on n-GaN results from this study

Electrical parameters of various Schottky diodes on n-GaN	as-deposited				After RTA (500 °C, 5 min)			
	ϕ_B ($J-I$) (eV)	ϕ_B ($C-I$) (eV)	Leak at -5 V (A/cm^2)	ϕ_B ($J-I$) (eV)	ϕ_B ($C-I$) (eV)	Leak at -5 V (A/cm^2)	Leak at -5 V (A/cm^2)	
Pt(30 nm)/Au	0.93	1.08	$2.1\text{E}-08$	1.10	1.25	$7.5\text{E}-09$		
Ni(30 nm)/Au	0.84	0.79	$5.6\text{E}-05$	1.01	1.07	$2.7\text{E}-07$		
Ni(10 nm)/Pt(30 nm)/Au	0.87	0.84	$1.6\text{E}-05$	1.07	1.47	$9.7\text{E}-11$		

(b) I-V and C-V SBH on n-GaN from Miura, N. et al [9]

Table 2.3: Leakage after 2 hours furnace anneal at 500 °C

Schottky Metal	As-Deposited			After Cumulative Furnace Anneal (500 °C, 2 hours)		
	SBH [relative]	Ideality [relative]	Leakage at -20V [A/cm ²]	SBH [relative]	Ideality [relative]	Leakage at -20V [A/cm ²]
Ni/Pt/Au (2.5/30/50nm)	1.06	1.18	7.45E-02	1.00	1.29	7.65E-02
Ni/Au (30/50nm)	1.02	1.17	1.47E-01	1.23	1.19	9.15E-04
Ir/Pt/Au (2.5/30/50nm)	1.14	1.17	1.17E-02	1.19	1.12	1.10E-02
Ir/Au (30/50nm)	1.05	1.11	3.61E-02	1.01	1.14	1.60E-01
Pt/Au (30/50nm)	1.13	1.19	1.15E-03	1.22	1.13	5.73E-03

Table 2.4: Elemental EDS composition at selected quantification points of Figure 2.14 in the annealed Ni/Au and Ni/Pt/Au contacts

Location point	Ni/Au Metallization		Ni/Pt/Au Metallization		
	% Ni	% Au	% Ni	%Pt	% Au
1	72.84	20.83	48.80	28.86	22.34
2	97.06	2.94	54.96	34.59	10.46
3	72.84	27.16	39.2	51.18	9.62
4	9.87	90.13	13.36	21.09	65.54
5	7.77	92.23	-0.53*	-4.65*	105.17
6	-	-	53.25	-2.92*	49.67

* shows very low signal (< sigma) meaning negligible value.

2.8 Figures

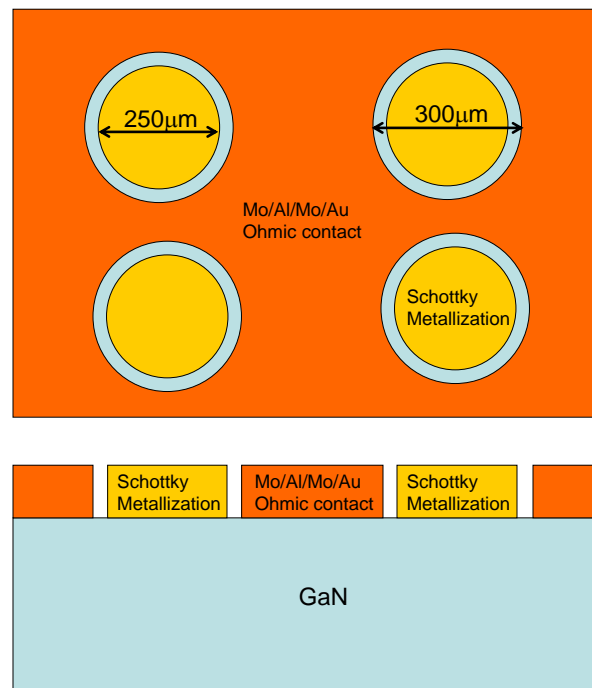


Figure 2.1: Schottky diode fabrication process.

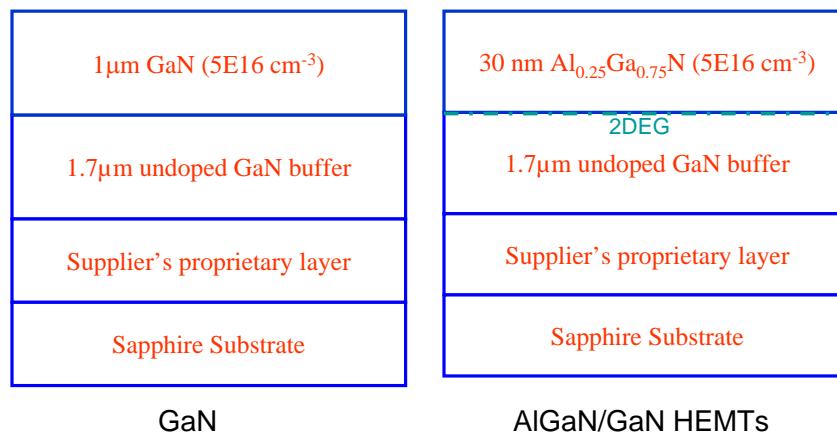
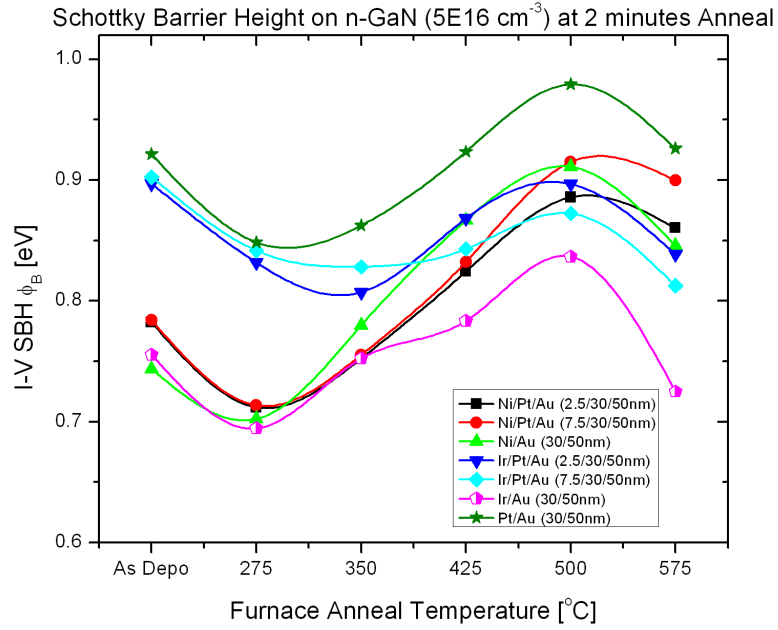
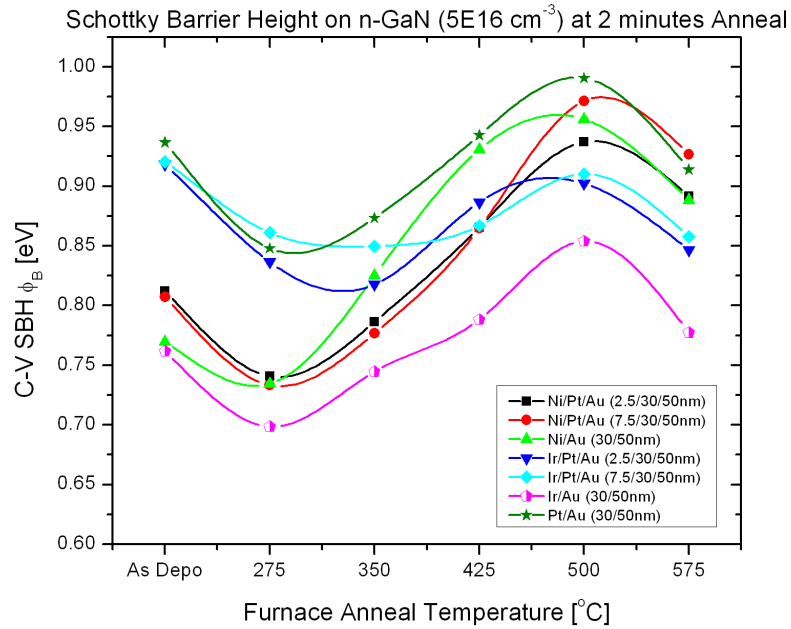


Figure 2.2: Layers used for fabrication of Schottky diodes.

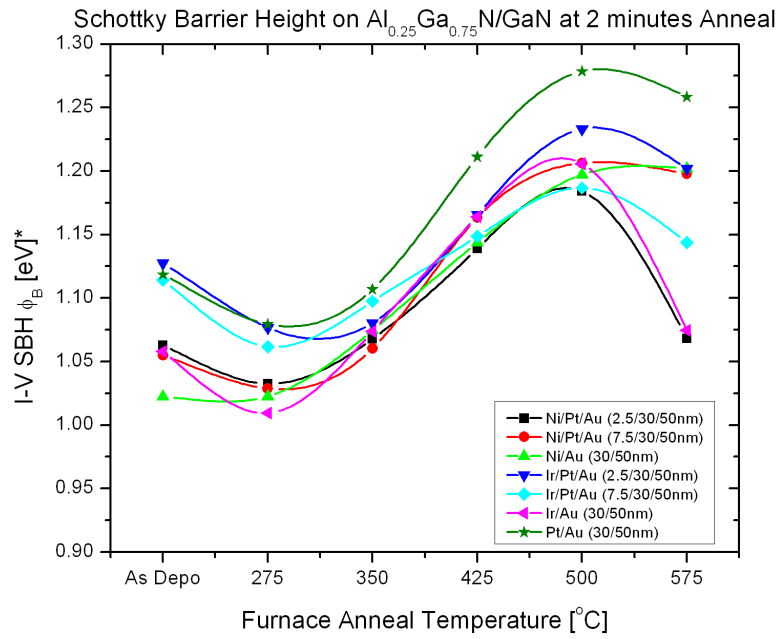


(a) I-V extracted values for SBH

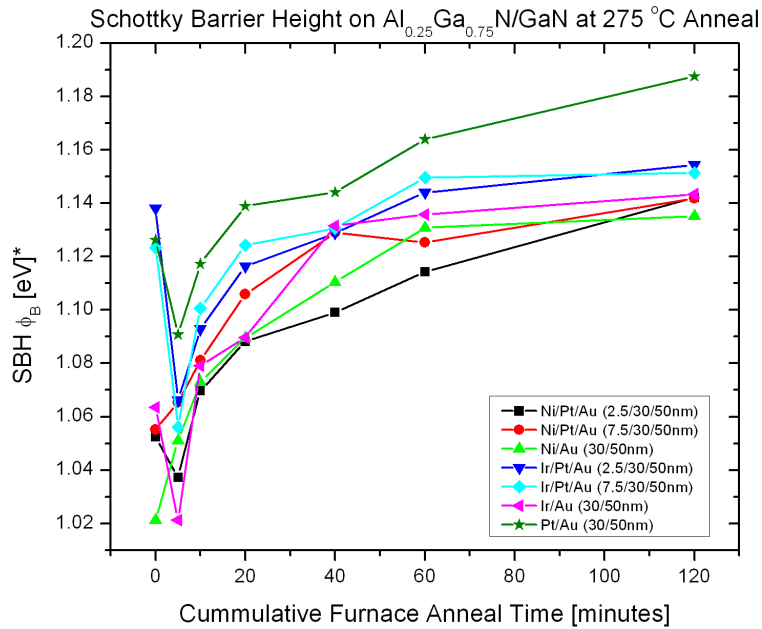


(b) C-V extracted values for SBH

Figure 2.3: I-V and C-V extracted Schottky barrier height ϕ_B on n-GaN under furnace anneal.

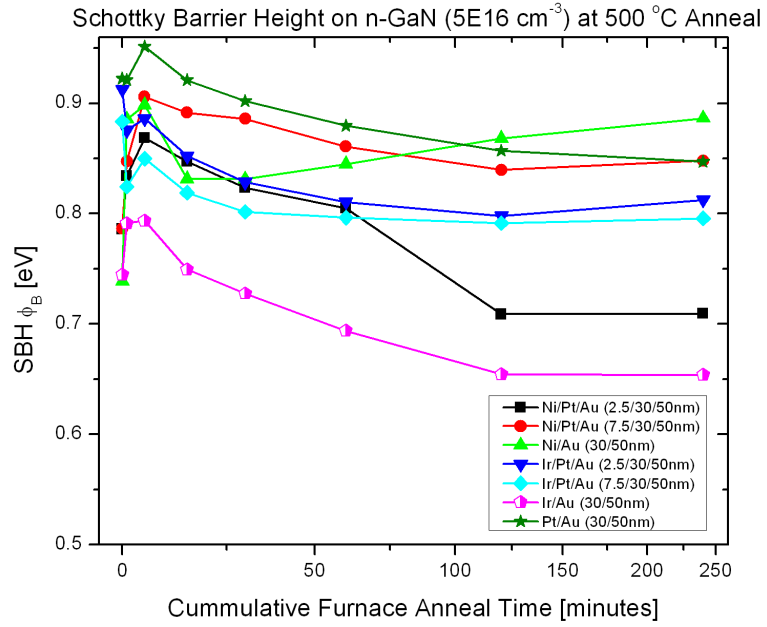


(a) *SBH calculated relative to $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ at 2 minutes Anneal

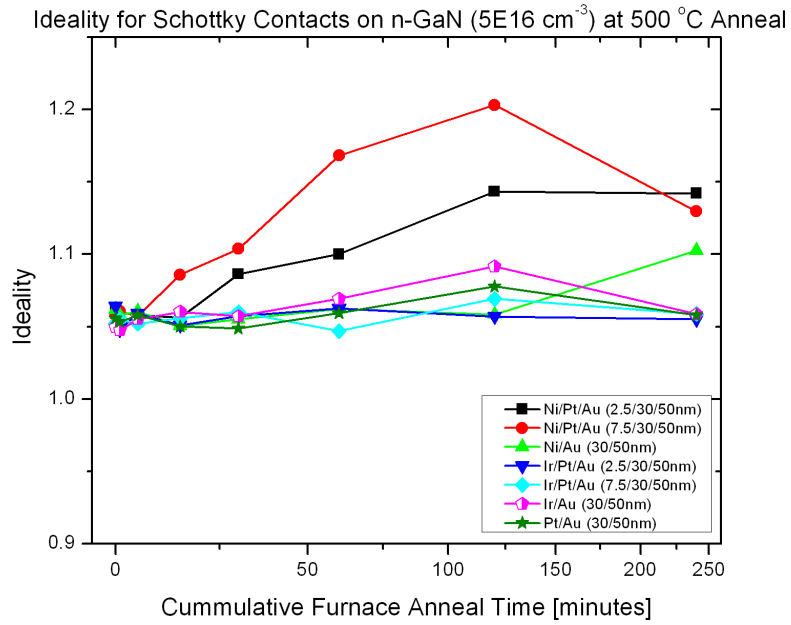


(b) *SBH calculated relative to $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ at 275 °C Anneal

Figure 2.4: Schottky barrier height ϕ_B of Schottky contacts to $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ under furnace anneal.

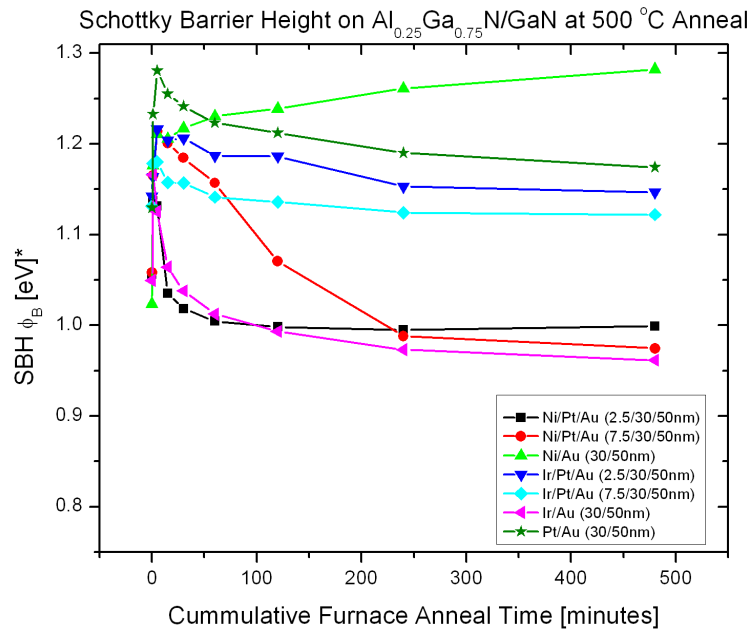


(a) Schottky barrier height

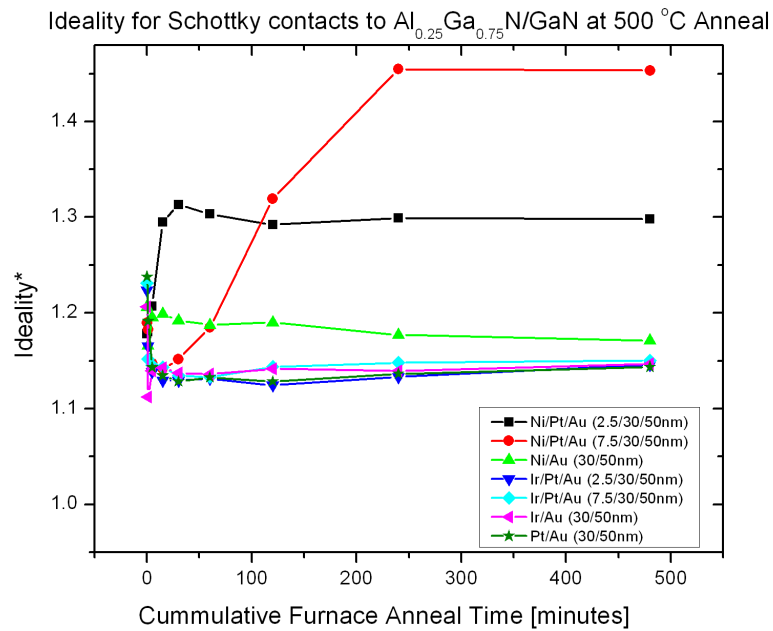


(b) Ideality

Figure 2.5: Schottky barrier height ϕ_B and ideality on n-GaN under cumulative furnace anneal at 500 °C.



(a) * Schottky barrier height calculated relative to $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$



(b) * Ideality calculated relative to $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$

Figure 2.6: Schottky barrier height ϕ_B and ideality on AlGaIn/GaN under cumulative furnace anneal at 500 °C.

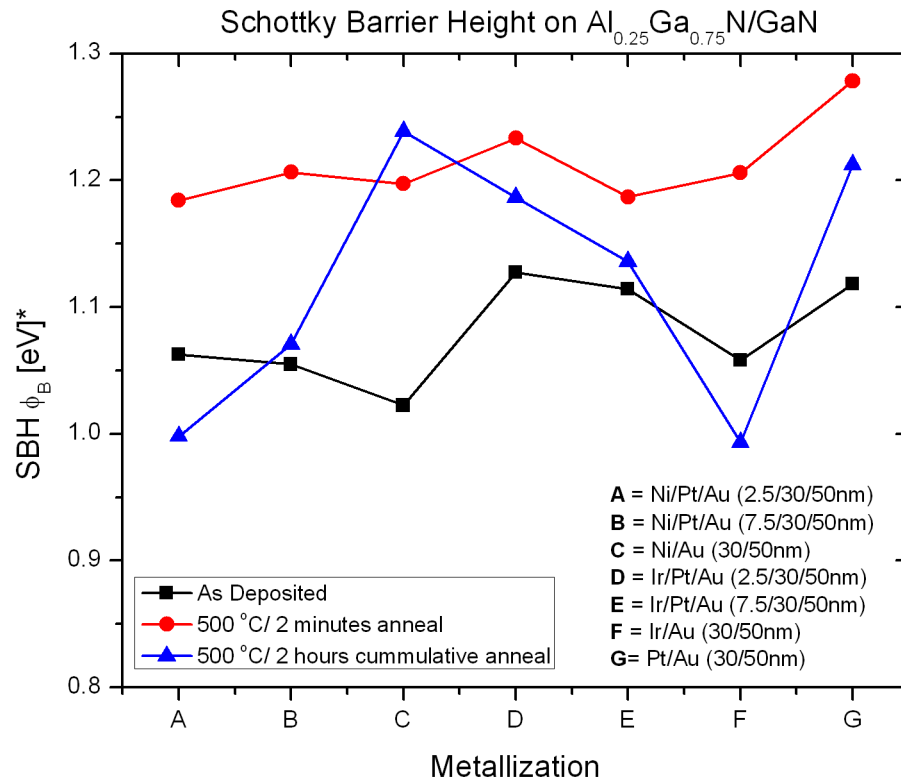


Figure 2.7: SBH of the various metallizations compared.

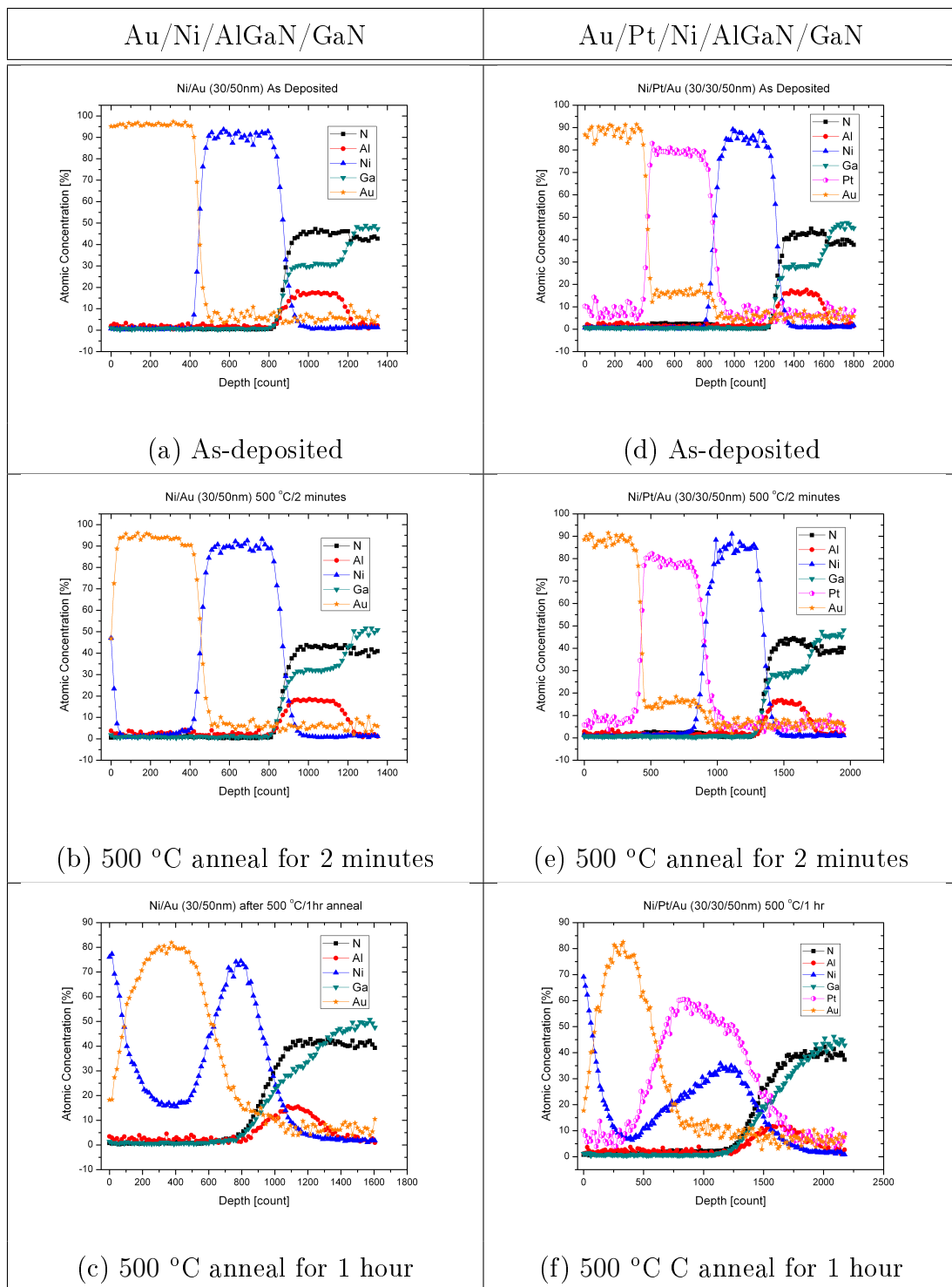
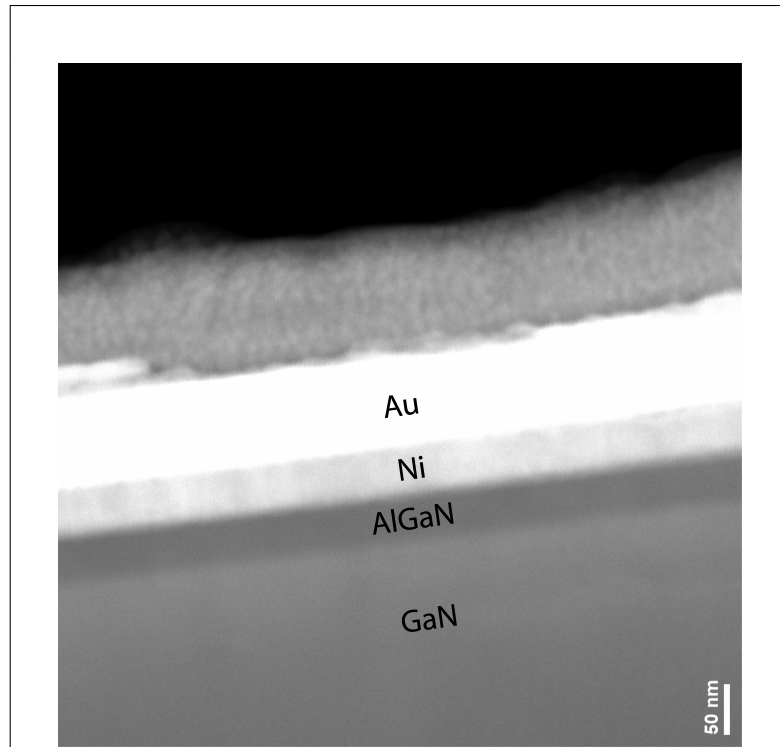
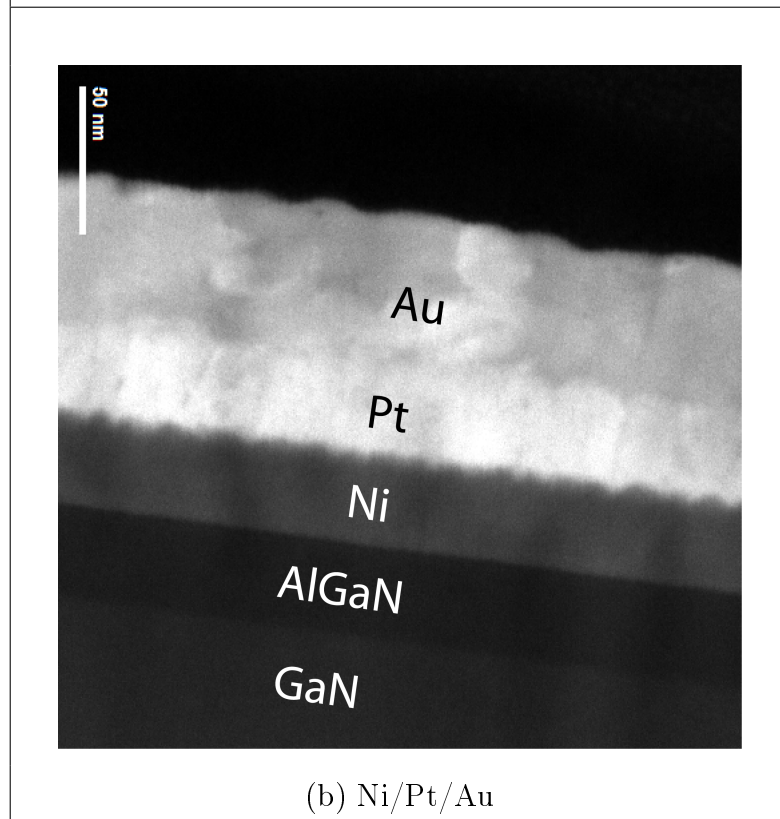


Figure 2.8: Auger electron spectroscopy profiles of Ni/Au (30/50 nm) (a) to (c) and Ni/Pt/Au (30/30/50 nm) (d) to (f) before and after anneal at 500 °C.



(a) Ni/Au



(b) Ni/Pt/Au

Figure 2.9: STEM images of (a) Ni/Au and (b) Ni/Pt/Au as-deposited on AlGaN/GaN epilayers.

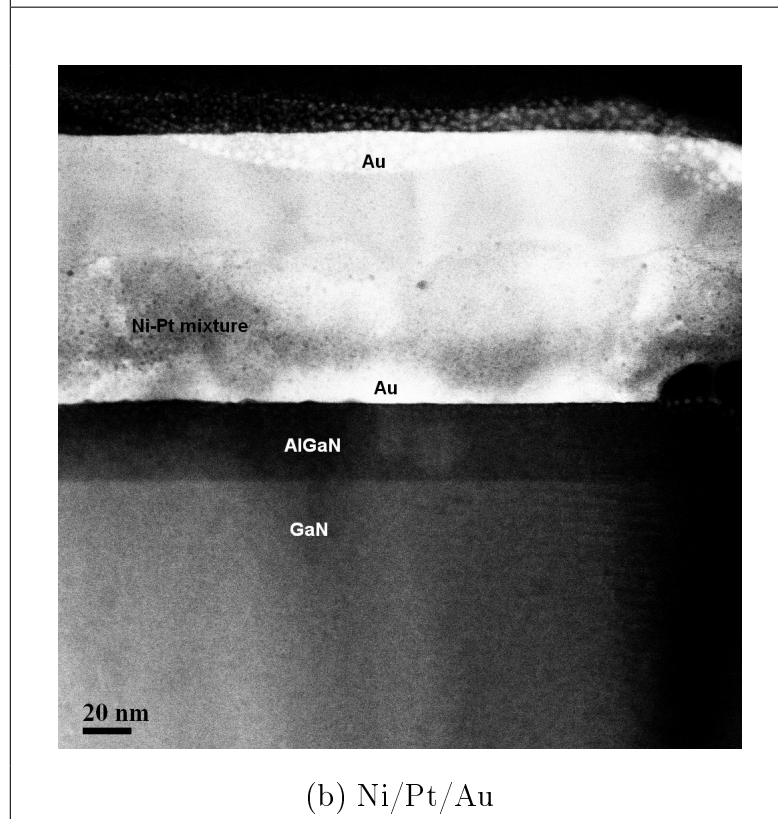
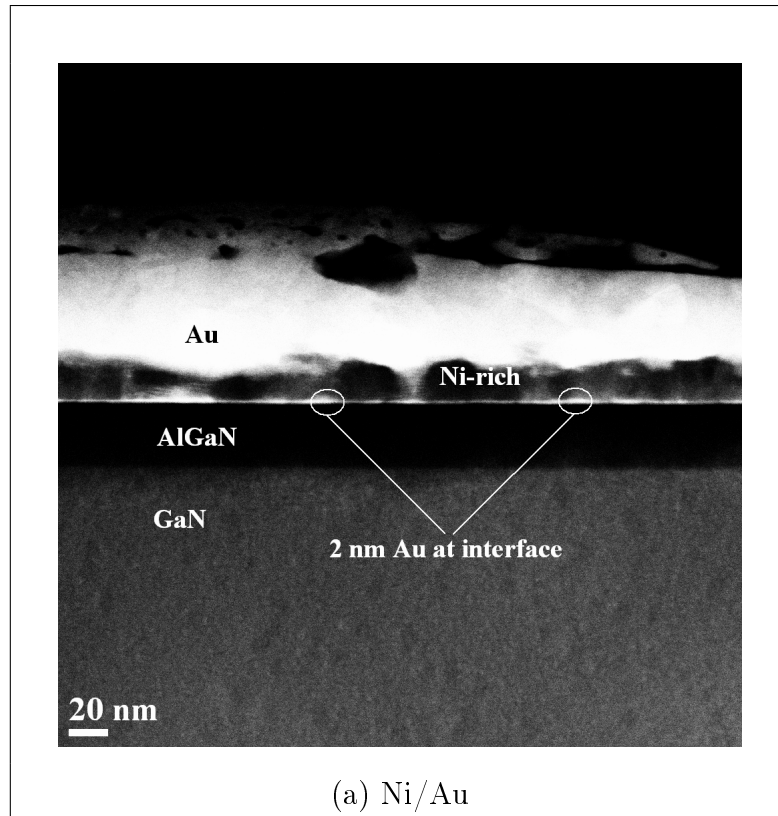


Figure 2.10: STEM images of (a) Ni/Au and (b) Ni/Pt/A on AlGaN/GaN after 500 °C annealing for 1 hour.

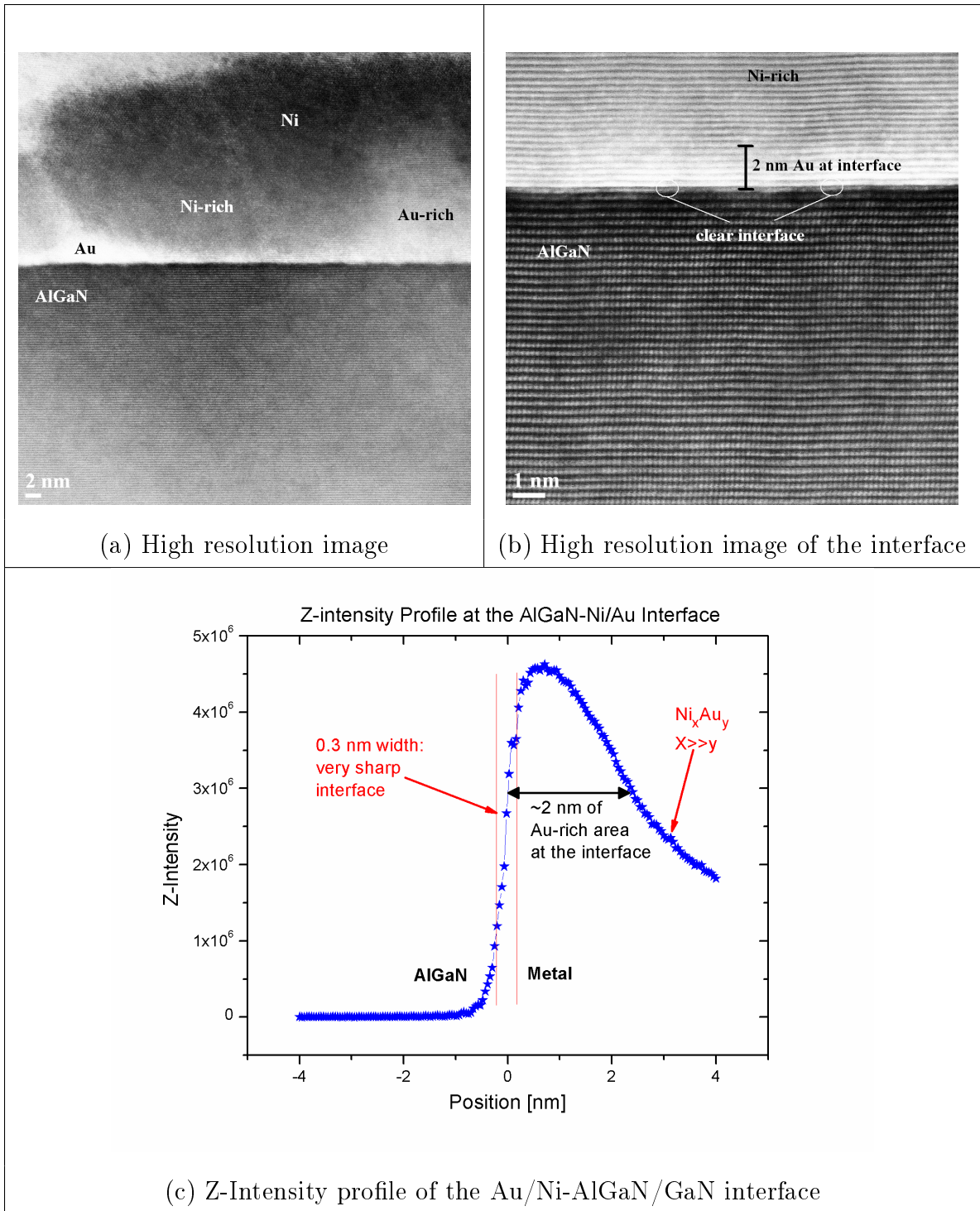


Figure 2.11: High resolution STEM images of Ni/Au on AlGaIn/GaN after 500 °C annealing for 1 hour showing accumulation of Au at the metal-AlGaIn interface.

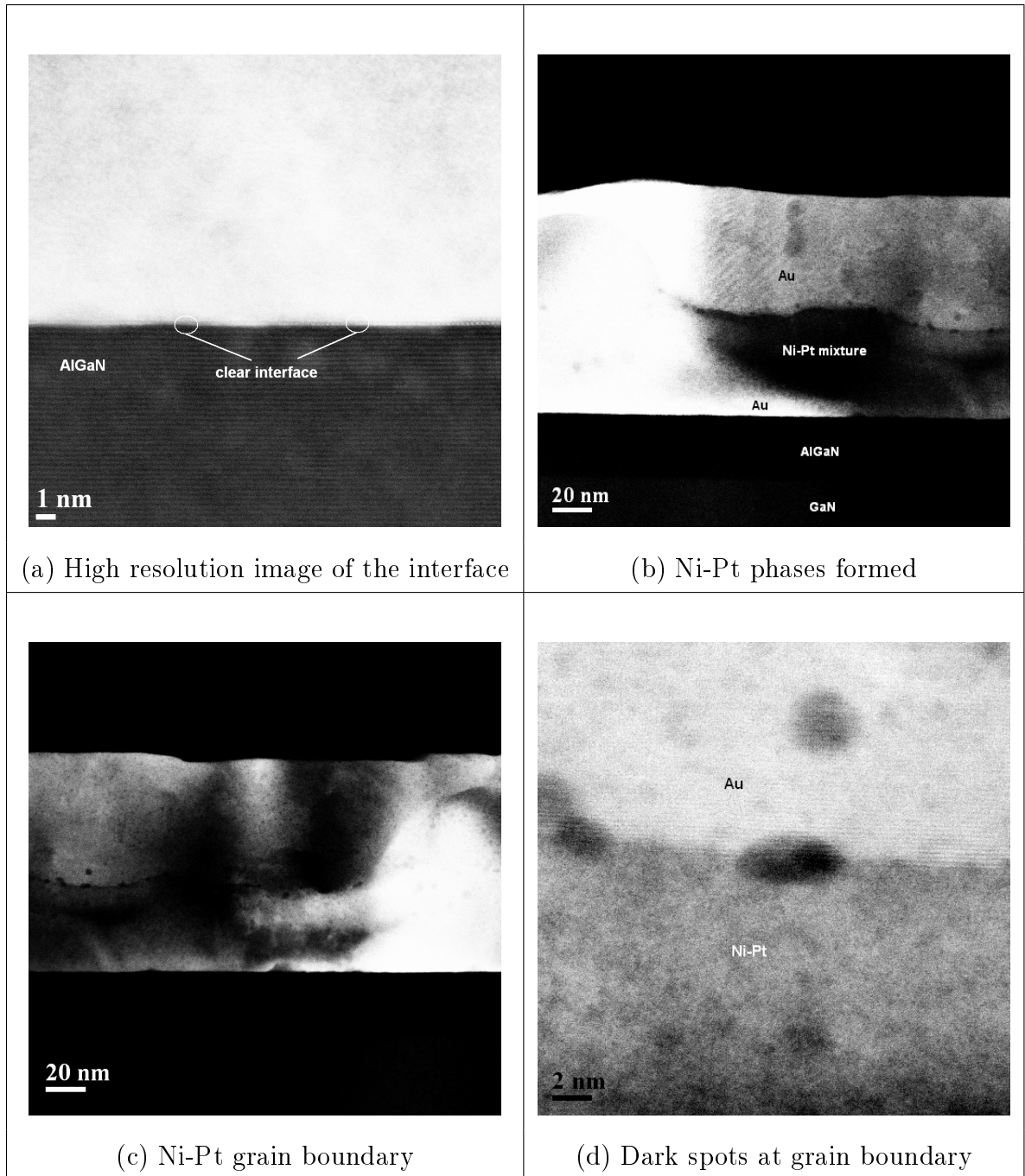


Figure 2.12: STEM images of Ni/Pt/Au on AlGaN/GaN after 500 °C annealing for 1 hour showing interface and Ni-Pt phases.

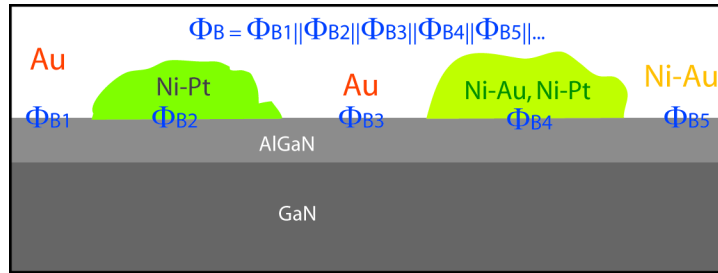


Figure 2.13: Schematic showing mixed interface in Ni/Pt/Au after 500 °C anneal for 1 hour.

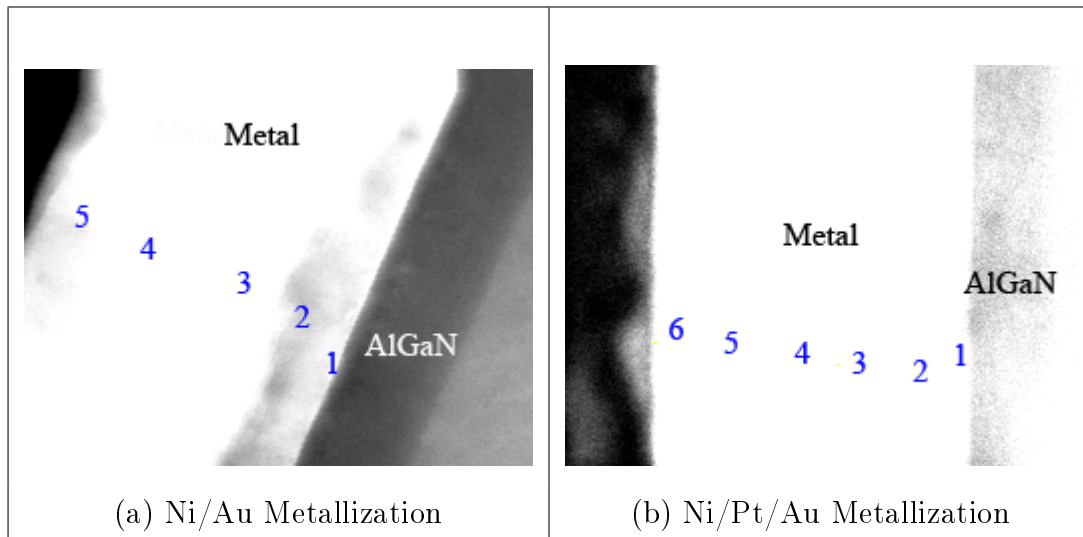


Figure 2.14: EDS quantification points in the annealed metallization.


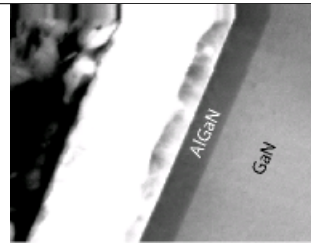
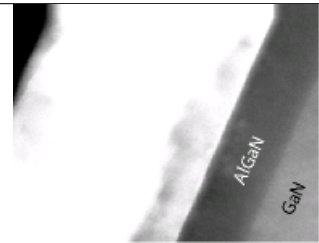
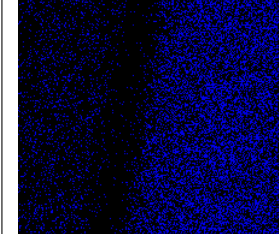
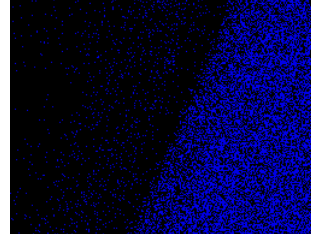
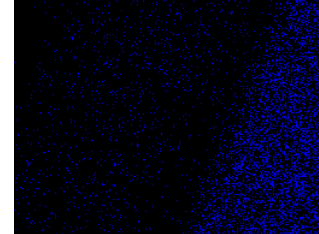
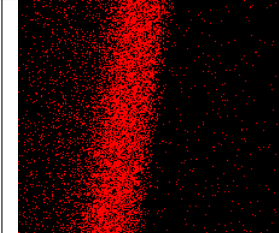
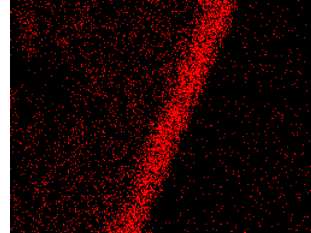
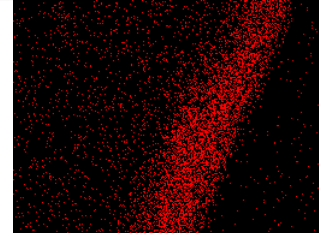
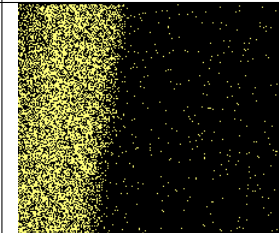
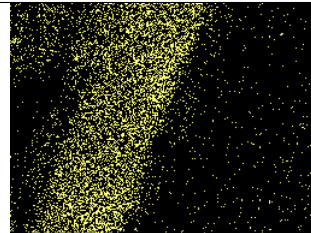
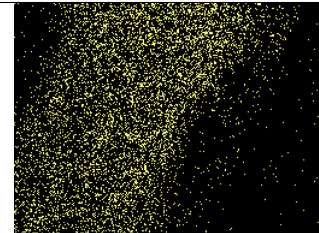
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STEM Image			
Ga Map			
Ni Map			
Au Map			

Figure 2.15: EDS map of Ni/Au with the corresponding STEM image.

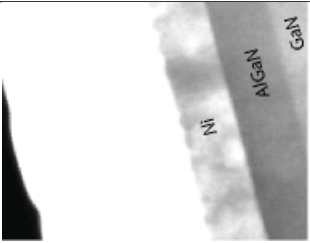
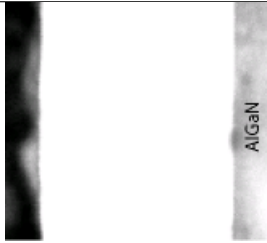
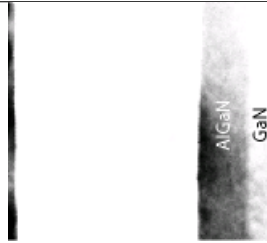
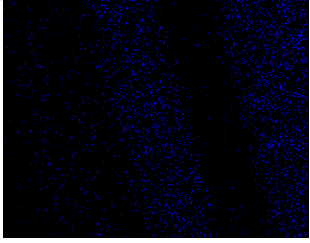
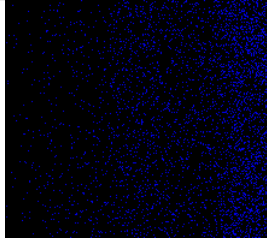
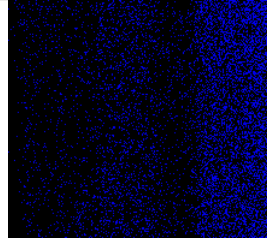
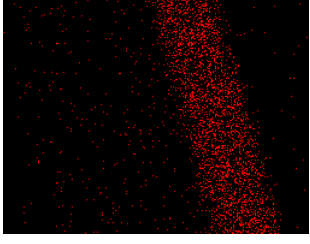
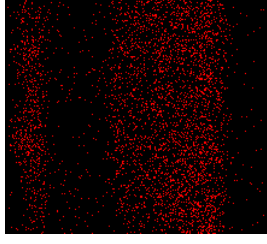
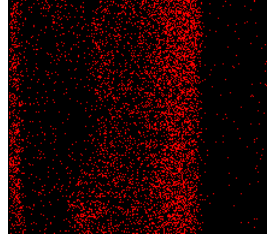
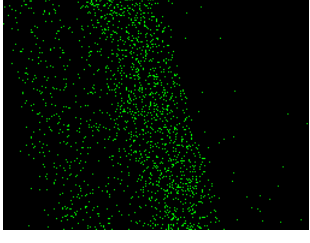
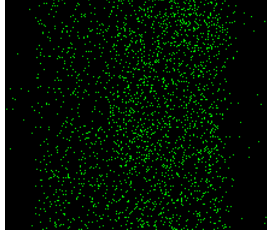
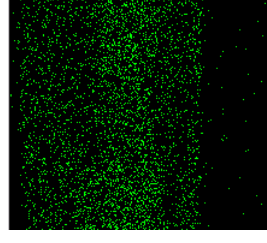
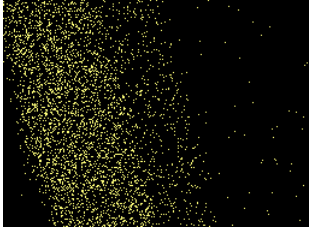
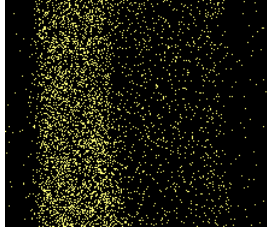
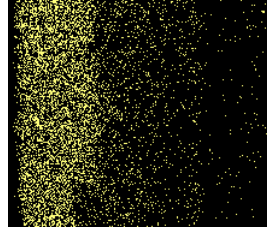
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STEM Image			
Ga Map			
Ni Map			
Pt Map			
Au Map			

Figure 2.16: EDS map of Ni/Pt/Au with the corresponding STEM image.

2.9 References

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CHAPTER 3

LOW VOLTAGE SILICON ION IMPLANTATION ON GAN AND ALGAN/GAN

3.1 Silicon as N-Type Dopant for Implantation in GaN

Dopant Implantation is used in the CMOS process for doping silicon n-type or p-type. This is essential because of the need to have both p-type and n-type regions in the planar process. GaN on the other hand is usually grown epitaxially. During growth, silicon can be used to dope GaN n-type. AlGaN/GaN high electron mobility transistors (HEMTs) do not require both p-type and n-type regions. The 2-DEG that results from the growth of the AlGaN barrier layer on the GaN buffer layer creates a sheet of highly mobile channel electrons near the AlGaN-GaN interface.

The inertness of GaN creates the need for annealing of metal contacts to give ohmic behavior. N-type doping enables the formation of good ohmic contacts by raising the Fermi level closer to the conduction band, thus reducing the metal-semiconductor interface barrier. A very good ohmic contact ensures good current conduction between source and drain of the HEMT device as the access resistance is considerably reduced.

However, doping the top AlGaN barrier layer very highly with silicon during growth may not be advisable. Firstly, it may create a lot of defects which are not desirable, and secondly, extremely high doping would make it difficult to have a good Schottky barrier for the Schottky gate metal necessary for gate control. Selective-area implantation of silicon into the source and drain regions during contact fabrication is a very desirable technique for increasing the doping levels and enhancing ohmic contact formation even without the need for high temperature contact annealing.

Low energy silicon ion implantation in GaN, AlGaN and AlGaN/GaN has been variously studied by researchers [1]-[17]. Selective source and drain area implantation was recently undertaken by the group at UCSB [14]-[16]. The promise of improvement to device performance by silicon implantation at high dose is immense. The possibility of having non-alloyed ohmic contacts that do not require annealing will reduce one step in the process and can also aid the fabrication of self-aligned AlGaN/GaN HEMT devices.

3.2 Ion Projected Range

Figure 3.1 shows the trajectory of ions in matter. The scattering events result in a stochastic value for the stopping distance and location. Thus the stopping range of ions in matter follows a stochastic distribution. The depth distribution profile for a given implant dose is given by the Gaussian profile [5]:

$$N(x) = \frac{\phi_1}{\Delta R_p (2\pi)^{\frac{1}{2}}} \exp \left[-\frac{1}{2} \left(\frac{x - R_p}{\Delta R_p} \right)^2 \right] \quad (3.1)$$

where $N(x)$ is the implant concentration in cm^{-3} at depth x , ϕ_1 is the implant dose in cm^{-2} , R_p is the projected range or average implantation depth and ΔR_p is the range straggling or standard deviation of the implantation depth. Figure 3.2 shows a typical ion range distribution.

The peak concentration is expected to be at the depth $x = R_p$ with the value of $N(R_p) = \frac{\phi_1}{\Delta R_p (2\pi)^{\frac{1}{2}}}$. The value of the peak concentration is proportional also to the implant dose ϕ_1 , so the higher the dose, the more the Si concentration at the projected range position. In order to achieve high doping, it is essential to implant at high enough dosage. However, the higher doses may lead to more damage events that can be difficult to anneal out even under very high thermal treatment. A knowledge of the projection range is a good asset in engineering implantation depths in semiconductors.

3.3 Damage and Activation

The penetration of ions in semiconductors results in the dislocation of constituent atoms and rearrangement of the crystal structure [2, 5]. The damage to the crystal structure of the semiconductor changes the properties of the semiconductor and could lead to the formation of different compounds. Figure 3.3 shows the simulated damage events in GaN after 30 keV Si ion implant. High temperature annealing beyond 1100 °C is usually employed to activate the implanted Si [3, 4, 6]. However, achieving full activation and recovery of the original crystalline structure may be difficult even after very high temperature anneal. This is especially true for AlGaN where the implant ions may displace the elements, disturbing the stoichiometry of the original material.

3.4 Simulation

The Stopping and Range of Ions in Matter (SRIM) tool [18] is a widely accepted resource for simulating the range and simulation profiles of ions in many materials. The simulated ion profile into GaN for a low voltage implantation of 40 keV is shown in Figure 3.4. The density of GaN used in the simulation was 6.1 g/cm³ and that of AlN was 3.26 g/cm³ giving a prorated density of 5.39 g/cm³ for Al_{0.25}Ga_{0.75}N in the simulation. The low energy ion ranges and straggling ranges of Si ion implanted at an offset angle of 7° (so as to avoid ion channeling) into GaN and Al_{0.25}Ga_{0.75}N samples are shown in Figures 3.5 and 3.6. From simulations, GaN has a projected range $R_p = 23.4$ nm and Al_{0.25}Ga_{0.75}N has a projected range $R_p = 24.9$ nm for 30 keV Si implantation. Hence if 30 keV silicon ions are directly implanted into GaN and Al_{0.25}Ga_{0.75}N, the maximum concentration of Si would be expected to be at 23.4 nm and 24.9 nm, respectively. Similarly for 50 keV, the depths would be at 39.7 nm and 40.1 nm, respectively.

The longitudinal straggling ranges are nearly half the projected ranges in both cases as shown in Figures 3.5 and 3.6. The lateral straggling ranges become

significant in scaling of submicron devices. Very high straggling values in the lateral direction will have serious consequences on the performance of submicron devices with nanometer source-drain spacings. For 50 keV energy implantation where lateral straggling values up to 20 nm were simulated using SRIM, source-drain spacings of at least 150 nm should be employed. For devices with shorter source-drain spacings, only very low implantation energies may be used.

3.5 Experiment

Experimentally evaluated ranges of the Si implanted in GaN and $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ sample structures of Figure 2.2 are also shown in Figures 3.5, 3.6, 3.7, and 3.8. Very high dose ($5 \times 10^{16} \text{ cm}^{-2}$) direct Si ion implantation was carried out at low energies of 10, 20, 30, 40, and 50 keV at implant angles of 7° to avoid ion channeling effects. Microstructural techniques were then used to analyze the samples after implantation.

3.5.1 Secondary ion mass spectroscopy (SIMS)

SIMS was used to analyze the profile of the implanted silicon. Figures 3.9 and 3.10 show a comparison of the atomic percentage of silicon concentration in the non-implanted control sample with the implanted samples at different energies for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ and GaN, respectively. Similarly, Figures 3.11 and 3.12 show a comparison of the non-implanted control sample with the silicon-implanted samples at different energies and thermal anneal in the furnace at 1200 °C for 3 minutes in N_2 ambient for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ and GaN, respectively. The samples were capped with 30 nm of low-pressure chemical vapor deposition (LPCVD) SiN_x before the high temperature annealing. The experimental range parameters of Figures 3.5 and 3.6 were extracted from the profile distributions of Figures 3.9 and 3.10 using a Gaussian fit algorithm written in MATLAB. The Gaussian profile of Equation (3.1) was employed in determining the range and straggling parameters.

The projected ranges of the implanted samples progressively increased with the implant energy in all cases as our simulations of Section 3.4 indicated. The offset of about 10-20 nm from simulated values at low energies as shown in Figures 3.5 and 3.6 may be due to the fact that the theoretical density value of 6.1 g/cm³ used for GaN in the simulations may be slightly higher than the density of our actual sample. Moreover, achieving high dose implantation at low energies required long implantation time. The effect of this on the range has not been fully studied. Simulating low energy implantation in the SRIM program may not be very accurate since most of the ion implantation theories are devised using high energy assumptions. Similar results are observed for the straggling values. Also, the comparison of simulated Al_{0.25}Ga_{0.75}N range parameters with experimental values from Al_{0.25}Ga_{0.75}N/GaN layers with only 30nm Al_{0.25}Ga_{0.75}N thickness may contribute to the higher deviation of the experimental range from simulated values in Figure 3.5 than in Figure 3.6 where GaN was used in both simulation and experiment.

After annealing the implanted samples at 1200 °C under N₂ ambient for 3 minutes and with SiN_x cap, the extracted range and straggling parameters of the samples of Figures 3.11 and 3.12, using a Gaussian fit script written in MATLAB, are shown in Figures 3.7 and 3.8 for Al_{0.25}Ga_{0.75}N/GaN and GaN, respectively. The SiN_x cap was removed with 49% HF after annealing. Diffusion during annealing may be responsible for the higher range values at 40 keV and 50 keV for Al_{0.25}Ga_{0.75}N/GaN and for 20 keV, 30 keV and 50 keV for GaN when compared with the as-implanted ranges parameters shown in Figures 3.5 and 3.6. The reason for the lower range at 10 keV, 20 keV and 30 keV for Al_{0.25}Ga_{0.75}N/GaN and 10 keV for GaN after anneal may be due to lower charge to mass ratios for Si in the SIMS experiment for these implant energies after anneal. The straggling range for the implanted Si in GaN was determined to be in close agreement with the simulated value while an offset of about 5-10 nm was observed in Al_{0.25}Ga_{0.75}N/GaN at higher implant energies. The discrepancies in the straggling ranges before and after annealing in the as-implanted GaN and Al_{0.25}Ga_{0.75}N/GaN may be due to diffusion and charge mass sensitivities

in the SIMS experiment. Further investigation needs to be carried out to explain the differences in the experimental range parameters values with the simulated values.

The SIMS profiles of the Si in the implanted samples are in agreement with the expected ion profile shape of Figure 3.2. However, SIMS evaluation of other elements showed significant presence of oxygen and carbon. Even though some oxygen was found at the surface of the implanted sample, most probably due to surface oxides, the significant concentration of these elements within the sample depth may change the properties of the samples. Significant depletion of the silicon concentration at the surface after activation was observed. Further studies using X-ray photoelectron spectroscopy (XPS) were carried out to understand this behavior at the surface of the implanted samples.

3.5.2 X-ray photoelectron spectroscopy (XPS)

XPS was used to characterize the surface of these samples. Figures 3.13 and 3.14 show the surface composition of the implanted GaN and $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ samples, respectively, for Si implant energies of 10 keV, 20 keV, 30 keV, 40 keV and 50 keV at $5 \times 10^{16} \text{ cm}^{-2}$ dose. Figures 3.15 and 3.16 show the surface composition of the original sample, after implantation and after thermal annealing for GaN and $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$, respectively. The comparison for GaN was for 40 keV while that for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ was performed for 30 keV implantation energy.

Clearly, there is a significant introduction of oxygen atoms at the surface after high dosage implant for all energies. After annealing, Figures 3.15 and 3.16 show that the oxygen concentration at the surface is reduced by about 50% and the nitrogen level rose by almost 50%. The silicon in both cases was substantially reduced. Further, it was observed that the Al composition percentage in the AlGaN layer decreased significantly after implantation and annealing. It is also expected that the silicon ions will push atoms at the surface further down as they are bombarded with high dosage. The presence of a significant composition of oxygen at the surface after annealing and after 49% HF treatment implies that the surface

chemistry has evolved and an oxygen-rich compound had formed.

3.6 Conclusion

Simulation and experiment show that the implantation of high-dose, low energy silicon ions can be used to dope GaN and AlGaN/GaN samples. Secondary ion mass spectroscopy profiles of the implanted samples show that the implanted silicon profile is in agreement with simulated profiles at higher energies. High levels of oxygen were observed in the implanted samples due to possible oxidation during high dosage implantation. X-ray photoelectron spectroscopy studies of the surface of the implanted and activated samples revealed the formation of oxygen-rich compounds.

Further studies are needed to determine exactly the exact compositional and the electrical properties of the compounds formed in the surface of the implanted samples.

3.7 Figures

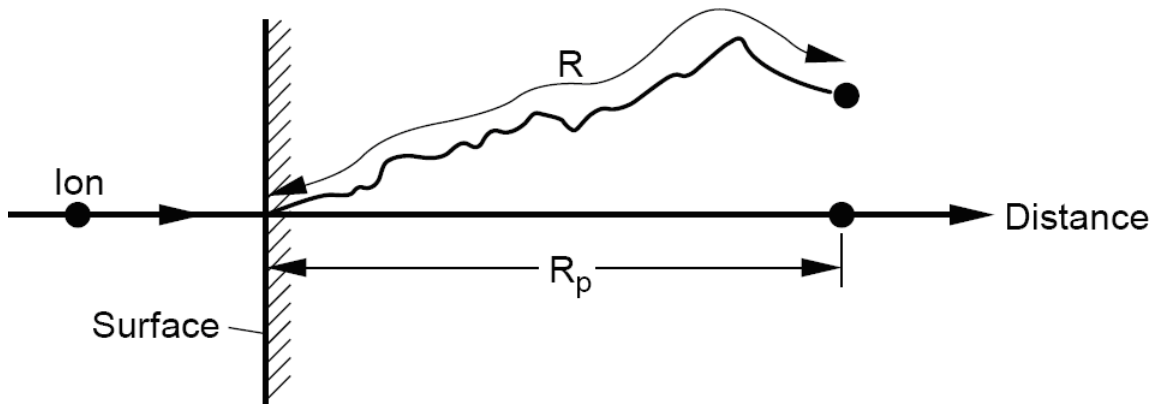


Figure 3.1: Ion incident on a semiconductor material and its trajectory within the semiconductor [5].

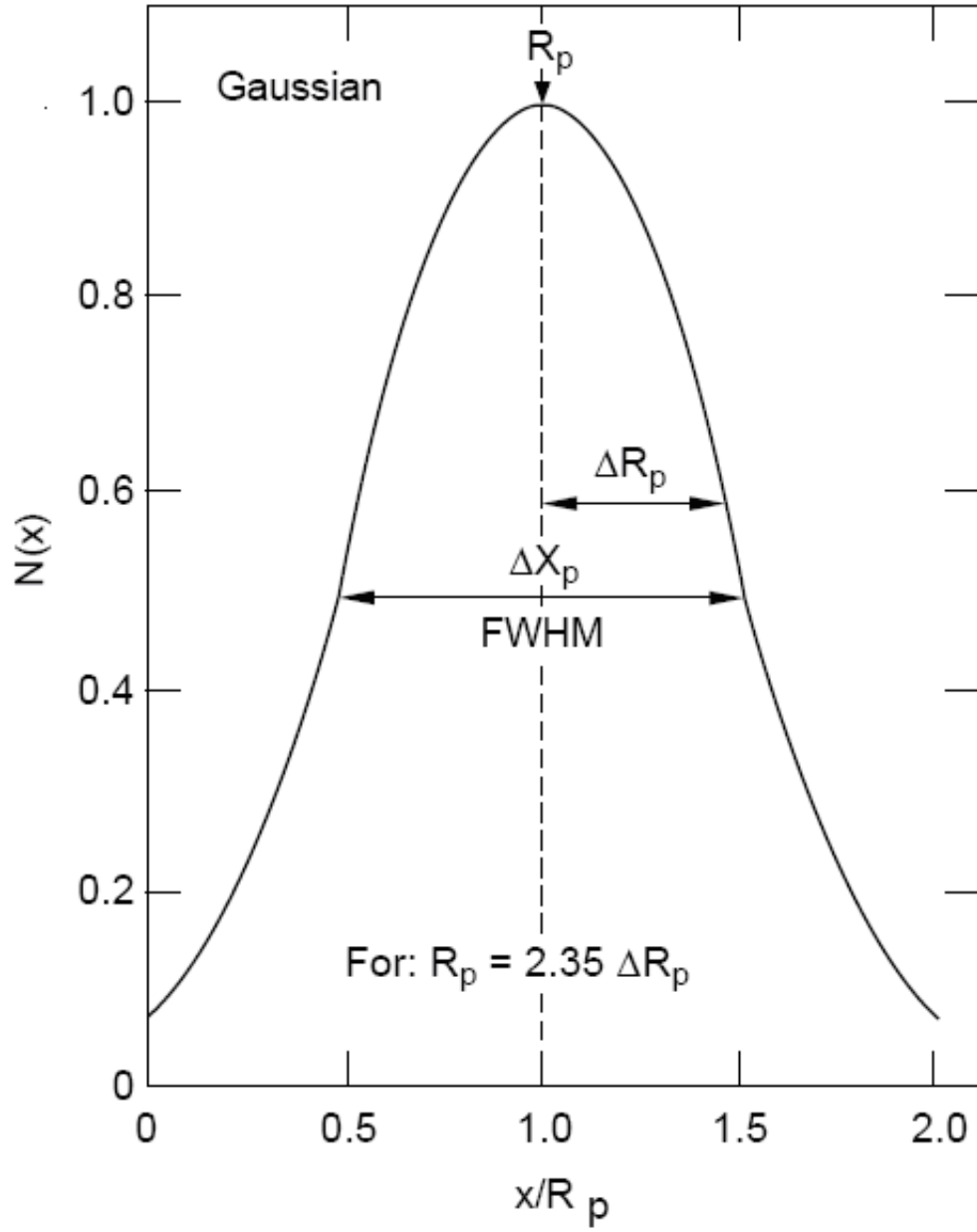


Figure 3.2: Gaussian range distribution for implanted ions with $R_p = 2.35\Delta R_p$ and a full-width at half-maximum (FWHM) of ΔX_p [5].

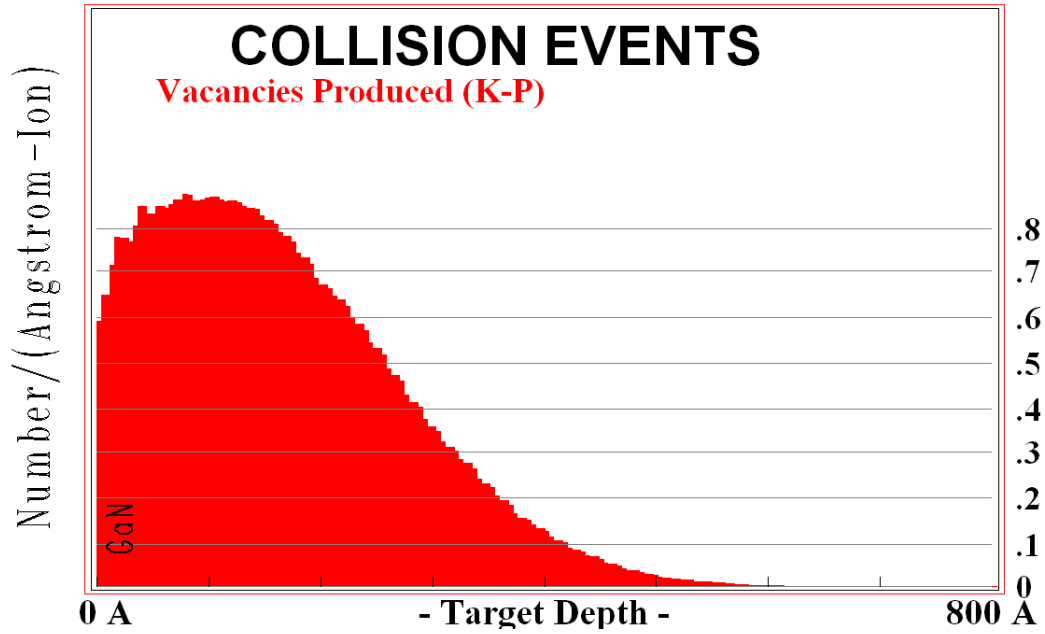


Figure 3.3: Simulated damage events to GaN after 30 keV Si ion implantation.

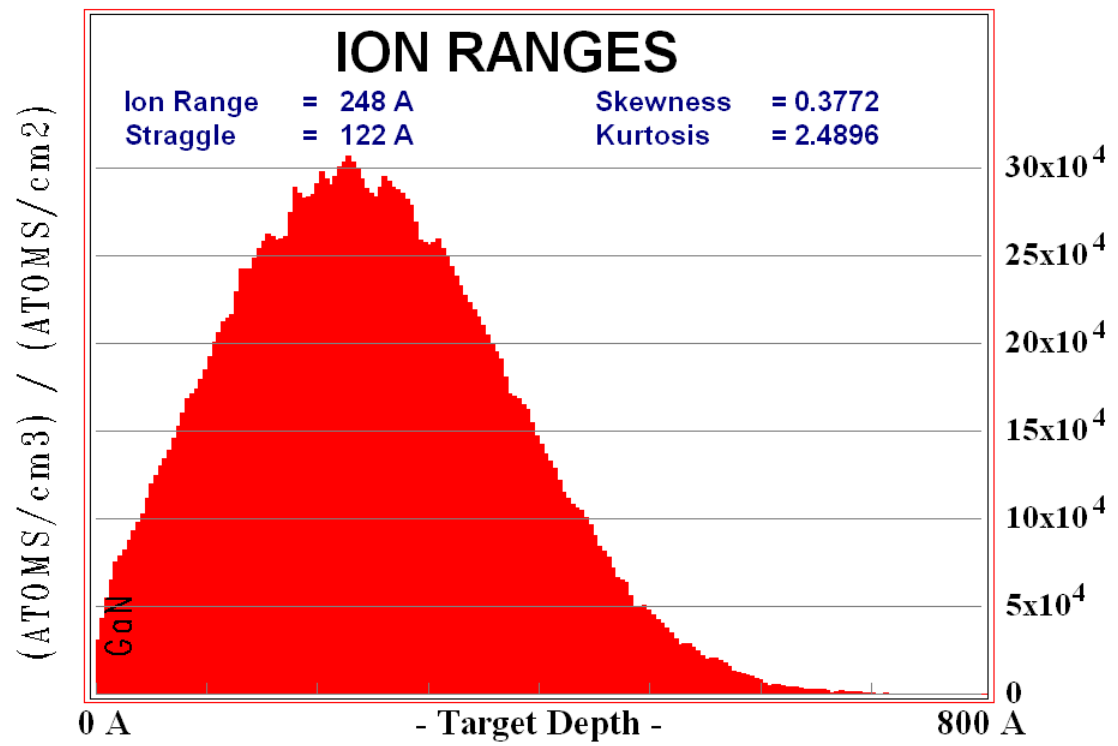


Figure 3.4: Simulated Si ion profile into GaN for 30 keV ion energy.

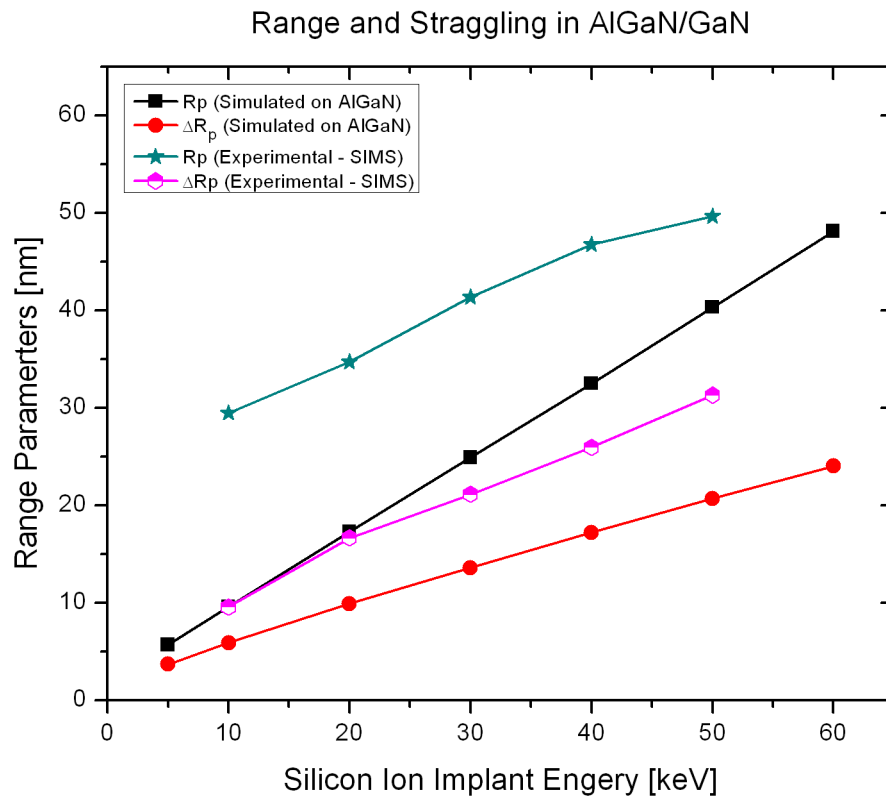


Figure 3.5: Simulated projection range and straggling of implanted Si ions in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ compared with experimentally determined range and straggling of implanted Si ions in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$.

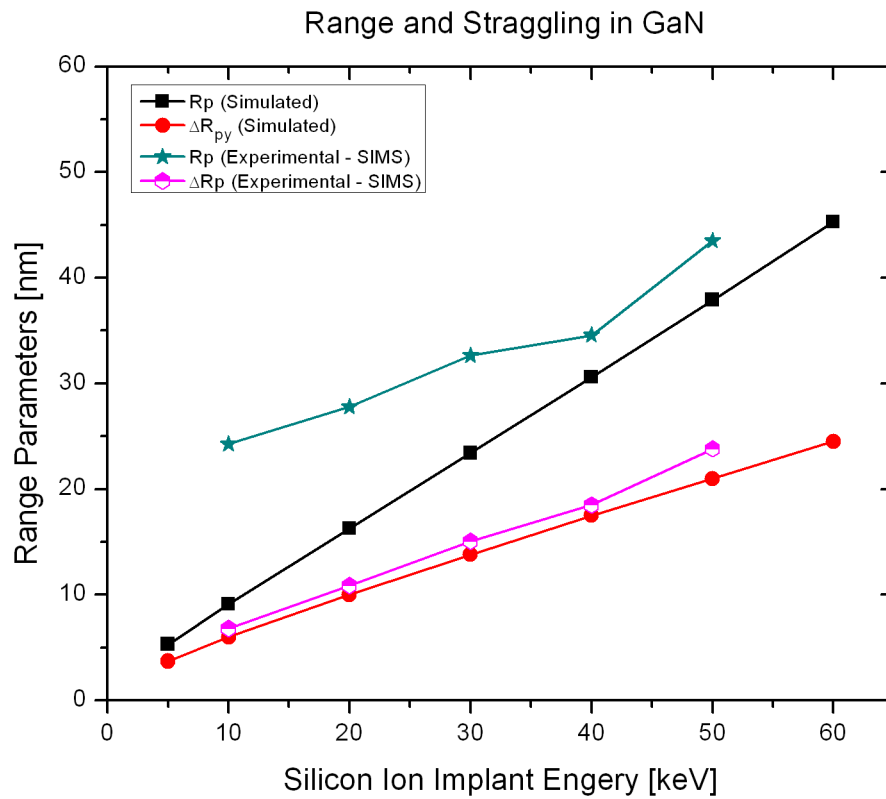


Figure 3.6: Simulated projection range and stragglng compared with experimentally determined range and stragglng of implanted Si ions in GaN.

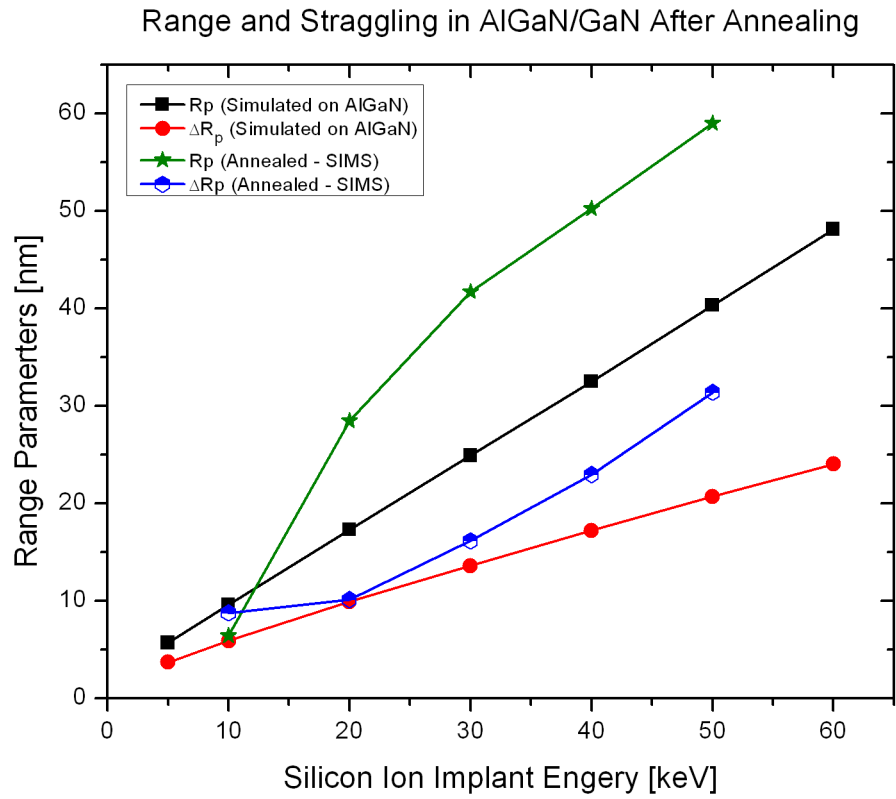


Figure 3.7: Simulated projection range and straggling of implanted Si ions in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ compared with experimental range and straggling from $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ samples implanted and annealed at 1200 °C for 3 minutes under N_2 ambient.

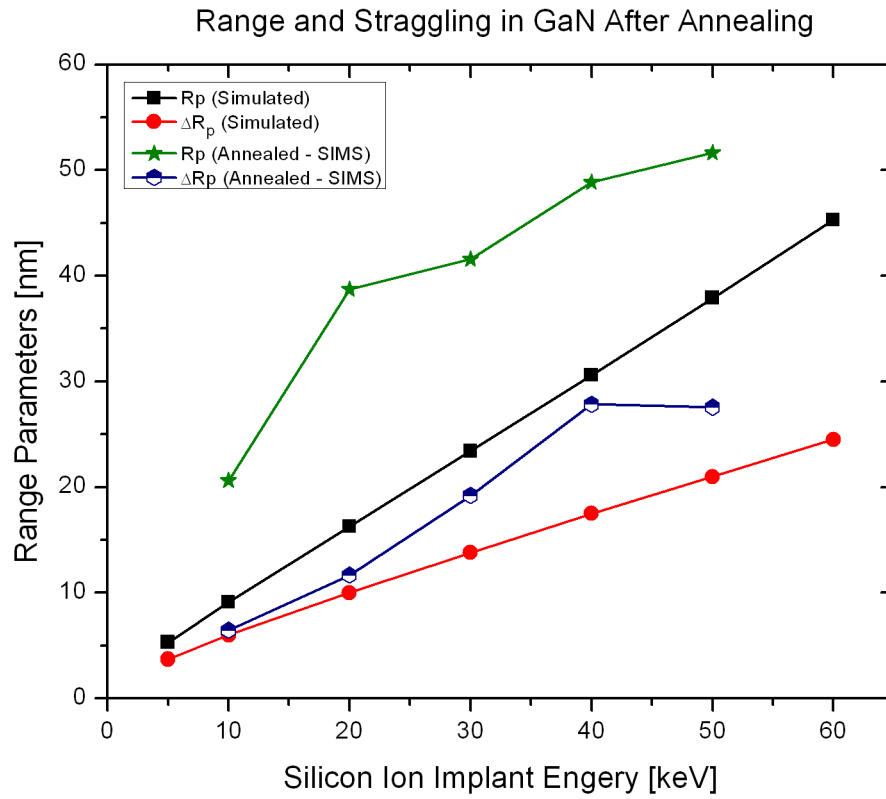


Figure 3.8: Simulated projection range and straggling of implanted Si ions in GaN compared with range and straggling from GaN samples implanted and annealed at 1200 °C for 3 minutes under N₂ ambient.

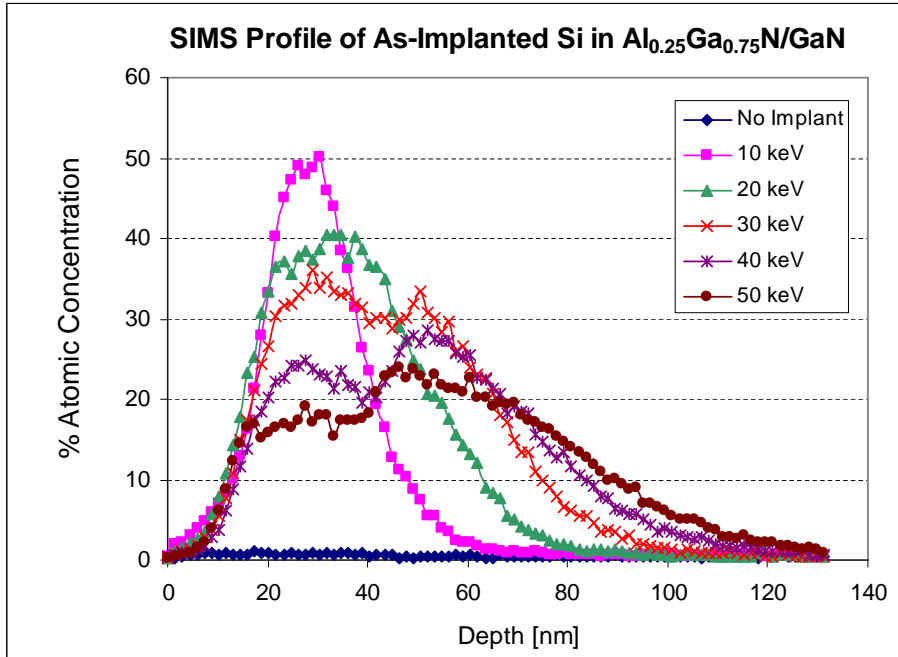


Figure 3.9: SIMS profile of Si in Al_{0.25}Ga_{0.75}N /GaN samples after Si ion implantation at low energies using $5 \times 10^{16} \text{ cm}^{-2}$ dose.

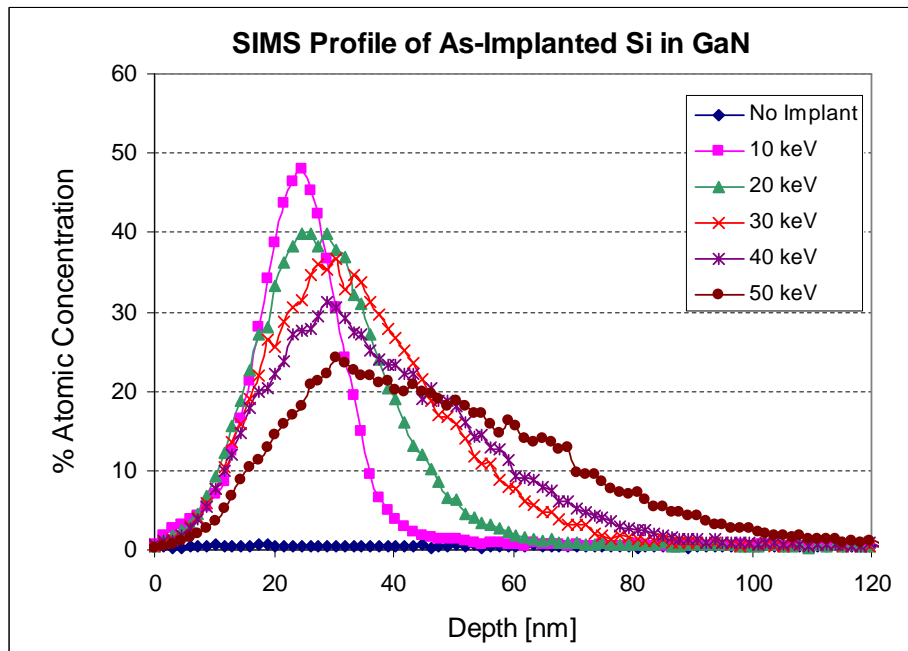


Figure 3.10: SIMS profile of Si in GaN samples after Si ion implantation at low energies using $5 \times 10^{16} \text{ cm}^{-2}$ dose.

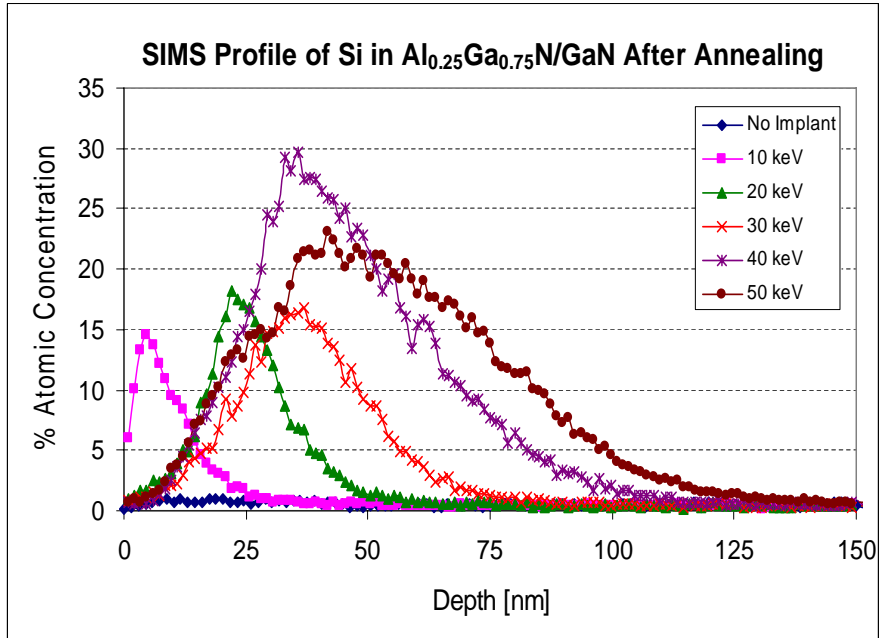


Figure 3.11: SIMS profile of Si in the AlGa_{0.25}N/GaN sample after implantation at $5 \times 10^{16} \text{ cm}^{-2}$ dose and annealing at 1200 °C for 3 minutes under N₂ ambient with SiN_x cap.

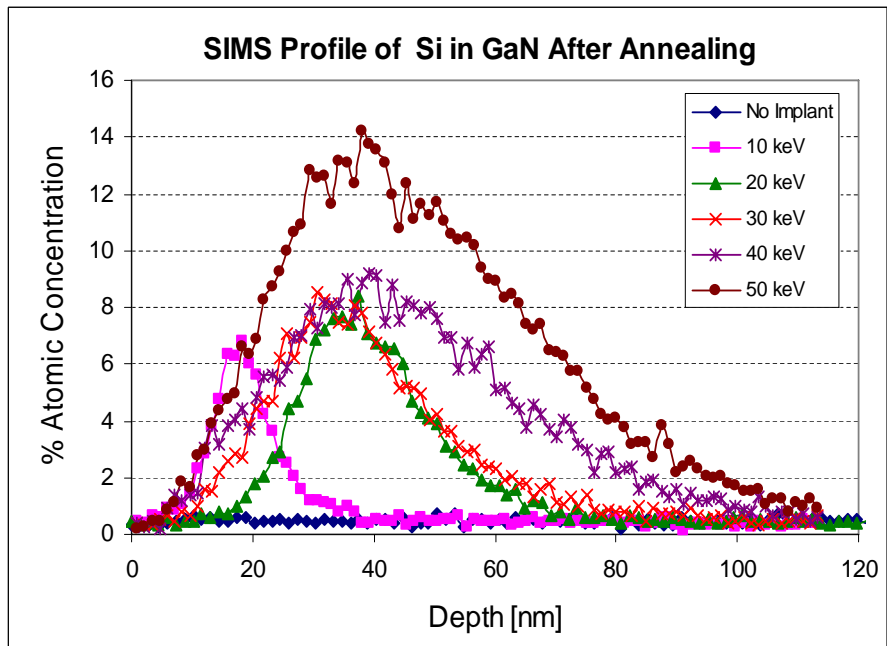


Figure 3.12: SIMS profile of Si in the GaN sample after implantation at $5 \times 10^{16} \text{ cm}^{-2}$ dose and annealing at 1200 °C for 3 minutes under N₂ ambient with SiN_x cap.

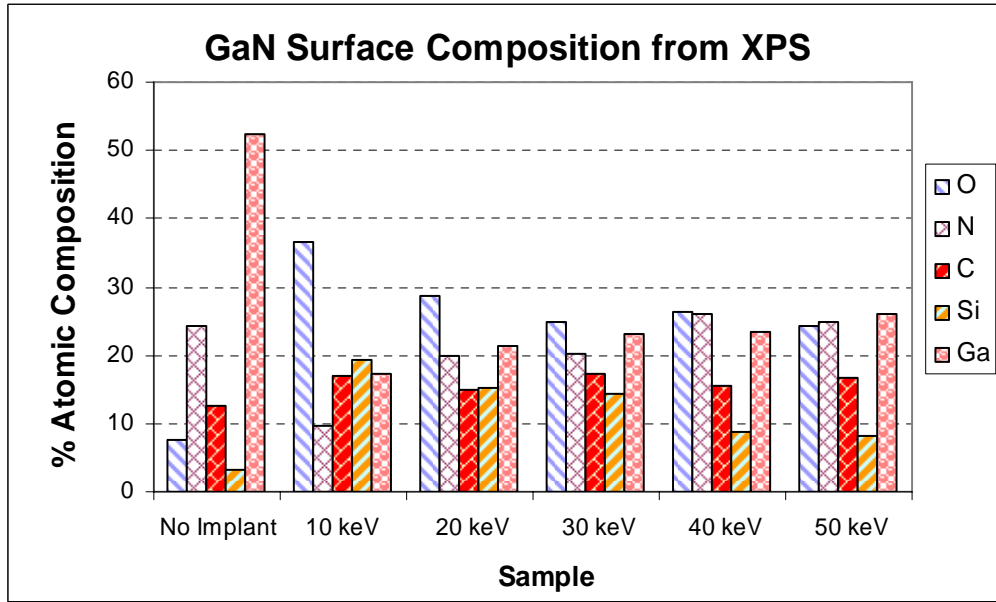


Figure 3.13: XPS data of GaN surface composition after Si implantation at $5 \times 10^{16} \text{ cm}^{-2}$ dose.

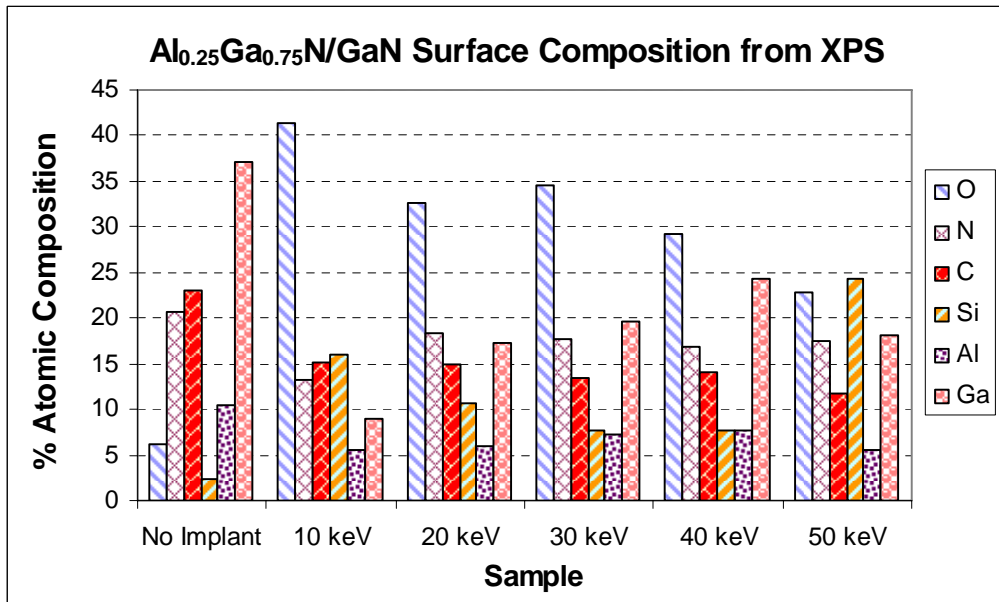


Figure 3.14: XPS data of Al_{0.25}Ga_{0.75}N/GaN surface composition after Si implantation at $5 \times 10^{16} \text{ cm}^{-2}$ dose.

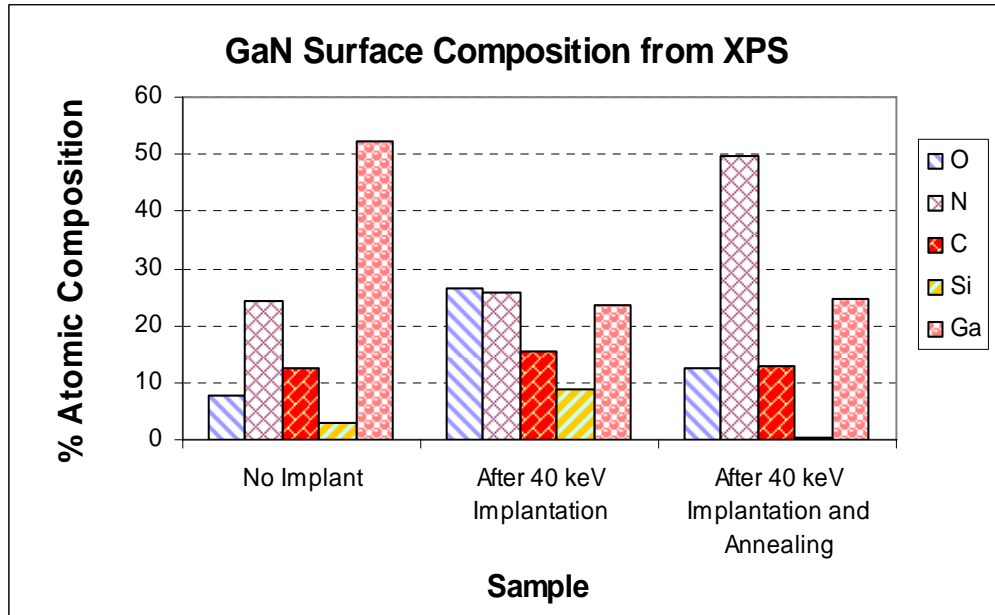


Figure 3.15: XPS data of GaN surface composition after implantation at 40 keV, $5 \times 10^{16} \text{ cm}^{-2}$ dose and annealing at 1200 °C using SiN_x cap.

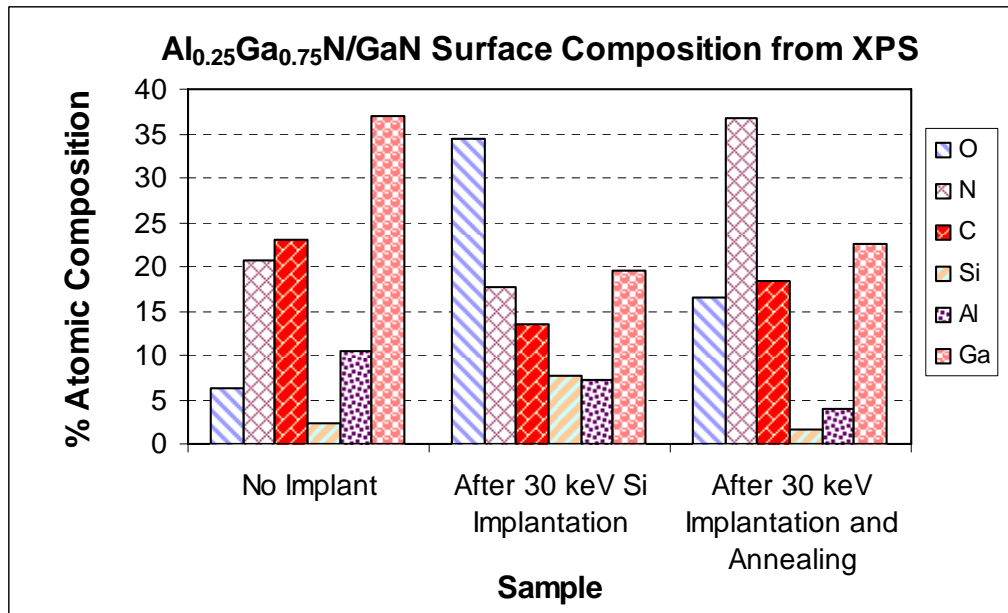


Figure 3.16: XPS data of Al_{0.25}Ga_{0.75}N/GaN surface composition after implantation at 40 keV, $5 \times 10^{16} \text{ cm}^{-2}$ dose and annealing at 1200 °C using SiN_x cap.

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CHAPTER 4

HIGH TEMPERATURE ANNEALING EFFECTS ON ALGAN/GAN SUBSTRATES

4.1 Introduction

AlGaN/GaN heterostructures are commonly grown by molecular beam epitaxy (MBE) at around 800 °C or by metal-organic chemical vapor deposition (MOCVD) at around 1000 °C-1150 °C. Barrier layers of AlGaN/GaN high electron mobility transistors (HEMTs) typically are grown with very low doping. However, it is usually desirable to have high doping in the ohmic contact areas to enable the formation of low contact resistances.

Silicon ion implantation is one viable method of increasing the doping concentration of GaN and AlGaN semiconductors. But activation of implanted dopants is usually done at temperatures higher than the growth temperatures to ensure complete or acceptable dopant activation. It is usual to anneal implanted bulk GaN and AlGaN at temperatures above 1150 °C to achieve substantial activation [1]-[9]. MBE-grown GaN on sapphire showed over 100% increase in mobility as the high dose Si⁺ implanted samples were annealed from 1050 °C to 1350 °C at $5 \times 10^{15} \text{ cm}^{-2}$ dose in the study in Ref. [1], and the MOCVD GaN also showed significant sheet resistance improvement at temperatures higher than 1250 °C [4]. Implanted AlGaN also had good activation at temperatures as high as 1350 °C [5]-[7]. Bulk MOCVD and MBE-grown AlGaN on sapphire was found to structurally deteriorate when annealed in air at 1100 °C or at 1200 °C in N₂ [8] and, for high aluminum mole fraction of 0.72, was found to decompose after annealing at 1150 °C in the presence of small amounts of oxygen [9]. Epilayer degradation during anneal is highly undesirable.

Annealing of implanted AlGa_N/Ga_N HEMTs at such high temperatures in order to activate the dopants, may impact the structure and mobility of the 2-dimensional electron gas (2-DEG). Previous studies on the robustness of the 2-DEG of AlGa_N/Ga_N HEMTs to thermal annealing have been performed at temperatures in the range of 500 °C to 900 °C in air. Annealing at 500 °C resulted in slight oxidation and non-reversible lattice relaxation in the AlGa_N due to oxygen incorporation at the surface after an extended anneal, resulting in a decrease in the 2-DEG mobility in the AlGa_N/Ga_N structure [10]. After annealing in air at 900 °C, it was observed that the 2-DEG sheet carrier density and mobility decreased [11]. It has been reported that the measured electron affinity of the annealed AlGa_N/Ga_N HEMT structures showed a decrease with annealing temperature due to more charge confinement [12]. Annealing studies at 500 °C with three separate MOCVD-grown HEMT structures on sapphire substrates, for a long time showed that both the 2-DEG density and mobility decreased due to strain relaxation in the AlGa_N layer. A 2 nm Ga_N capping layer was found to help stabilize the 2-DEG for up to 75 hours of thermal stress [13]. Thermal stability of AlGa_N/Ga_N heterostructures has also been studied at temperatures up to 800 °C. The observed increase in the sheet resistance was found to vary with the thickness of the Ga_N buffer layer [14].

Therefore, the impact of thermal annealing on the 2-DEG of AlGa_N/Ga_N HEMTs at elevated temperatures above the growth temperatures requires a systematic study. HEMT layers need to be carefully engineered to ensure that they do not degrade after thermal annealing at elevated temperatures above 1000 °C.

4.2 HEMT Layer Structure

The juxtaposition of higher bandgap AlGa_N and lower bandgap Ga_N creates a quantum well that favors the formation of 2-DEG. The polar nature of Ga_N, with the resulting polarization and piezo-electric charges, creates a sheet charge of high concentration near the AlGa_N/Ga_N interface. This sheet of highly mobile charges is responsible for channel conduction in high electron mobility transistors. The exact

location of the charges is hard to pinpoint but C-V measurements indicate that these charges are approximately around the interface of the higher bandgap AlGaN and lower bandgap GaN layers [15, 16]. A typical layer AlGaN/GaN layer structure with 2 nm GaN cap is shown in Figure 4.1.

4.3 Hall Measurement and Characterization

4.3.1 Hall bar

The Lorentz force on mobile charges is used to determine the mobility and concentration in bulk materials as shown in the Hall bar of Figure 4.2. Since there is no current in the z-direction, the electrical force in that direction, $F_z = qE_z$, is balanced by the magnetic force, $F_z = Bv_x = \frac{BI}{qwdn}$, where B is the magnetic field and n is the charge concentration. The Hall coefficient, R_H , is defined as $R_H = \frac{dV_H}{BI}$ and the Hall voltage $V_H = E_z d = \frac{R_H BI}{d}$. The concentration is given by

$$n = \frac{1}{qR_H} \quad (4.1)$$

and the mobility by

$$u = \frac{|R_H|}{\rho} \quad (4.2)$$

where ρ is the resistivity of the material.

4.3.2 Van Der Pauw measurement

Van Der Pauw measurement facilitates the determination of the mobility and sheet resistance of a material [17, 18]. Square samples with ohmic contacts at the edges of the four corners are employed in extracting these parameters. The setup of Figure 4.3 is used to perform sheet concentration, sheet resistance and mobility measurements. The resistivity measurement extracts the sheet resistance, R_S , as shown in Figure 4.3 (a) using:

$$R_A = \frac{V_{43}}{I_{12}} \quad (4.3)$$

$$R_B = \frac{V_{14}}{I_{23}} \quad (4.4)$$

and solving the Van Der Pauw equation,

$$\exp\left(\frac{-\pi R_A}{R_S}\right) + \exp\left(\frac{-\pi R_B}{R_S}\right) = 1 \quad (4.5)$$

to obtain the sheet resistance as [17]

$$R_S = \frac{\pi}{\ln 2} (R_A + R_B) F \quad (4.6)$$

where the fitting factor $F \approx 1$ if $R_A \approx R_B$.

With the arrangement of Figure 4.3 (b), Hall measurement is used to determine the mobility, μ , and sheet concentration, n_S . With Hall voltage $V_H = V_{24}$ and $I = I_{13}$, and B the magnetic field, the sheet concentration is calculated as

$$n_S = \frac{IB}{q |V_H|} \quad (4.7)$$

and the Hall coefficient, R_H , is given by

$$R_H = \frac{1}{qn_S} \quad (4.8)$$

and the mobility, μ , as

$$\mu = \frac{R_H}{R_S} = \frac{1}{qn_S R_S} \quad (4.9)$$

4.4 Experiment

Hall samples of dimension $7\text{ mm} \times 7\text{ mm}$ were used to do Van Der Pauw Hall measurements. Three different substrate layers were used and they were:

1. $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ on sapphire substrate (30 nm/1.7 μm /substrate)
2. $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{AlN}/\text{GaN}$ on sapphire substrate (20 nm/1 nm/1 μm /substrate)
3. $\text{GaN}/\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{AlN}/\text{GaN}$ on SiC substrate (2 nm/18 nm/1 nm/1 μm /substrate)

These layer structures are shown in Figure 4.4. Hall samples from these substrates were annealed from 1100 °C to 1230 °C in an MOCVD chamber under an NH_3/N_2 ambient with over-pressure. Before annealing, some of the samples were capped with 30 nm of plasma-enhanced chemical vapor deposition (PECVD) SiN_x . The SiN_x cap was removed with 49% HF after annealing. Mo/Al/Mo/Au ohmic contacts were then patterned and deposited at the four corners of the Van Der Pauw samples and annealed at 590 °C to form ohmic contacts. The sheet resistance, sheet concentration, and mobility of the samples were then measured using the Accent HP5500PC Hall effect measurement system.

The roughness of the samples before and after annealing were measured on $1\ \mu\text{m} \times 1\ \mu\text{m}$ areas of the samples using a Digital Instruments 3000 Atomic Force Microscopy system.

4.4.1 Annealing effect on mobility

The results on sheet concentration, sheet resistance and mobility of the capped and annealed samples are shown in Figures 4.5, 4.6 and 4.7. All the annealed samples were capped with 30 nm SiN_x . Figure 4.5 shows that there is a substantial degradation in the $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ on sapphire substrate (30 nm/1.7 μm /substrate) layer structure of Figure 4.4 (a) when annealed at elevated temperatures. Up to 40% degradation in mobility was observed after annealing at 1230 °C for 3

minutes when compared to the unannealed sample. A mobility value of 1220 $\text{cm}^2/\text{V}\cdot\text{s}$ in the unannealed sample was obtained compared with 660 $\text{cm}^2/\text{V}\cdot\text{s}$ after 1230 °C annealing for 3 minutes. The sheet resistance also increased from 402 Ω/\square in the unannealed sample to 862 Ω/\square after 1230 °C annealing. The sheet concentration did not change significantly having gone from $1.27 \times 10^{13} \text{ cm}^{-2}$ to $1.10 \times 10^{13} \text{ cm}^{-2}$ which represented a change of only 13%.

The second sapphire substrate layer structure, $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{AlN}/\text{GaN}$ on sapphire substrate (20 nm/1 nm/1 $\mu\text{m}/\text{substrate}$) of Figure 4.4 (b), showed a dramatic improvement in the mobility performance after thermal annealing. Firstly, it should be noted that the sample had a thinner $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer (20 nm) along with AlN (1 nm) spacer layer. Its mobility value was around 1600 $\text{cm}^2/\text{V}\cdot\text{s}$ (Figure 4.6) compared with 1200 $\text{cm}^2/\text{V}\cdot\text{s}$ in the sapphire based substrates with thicker $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer (30 nm) and no AlN spacer layer (Figure 4.5). Secondly, the incorporation of the thinner barrier layer with AlN spacer layer gave some stability to the 2-DEG after thermal annealing at 1230 °C. Only a slight drop of $\sim 10\%$ in mobility was observed in the sample annealed at 1230 °C when compared to the unannealed sample. The sheet resistance and sheet concentration remained fairly constant.

The third layer structure, grown on SiC substrate, had AlN (1 nm) spacer layer, a 2 nm GaN cap and 18 nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer. Figure 4.4 (c) shows this layer. The sheet resistance, sheet concentration, and mobility of this layer structure are shown in Figure 4.7. They did not exhibit observable degradation after annealing at elevated temperatures. The small variance in the values was probably due to wafer non-uniformity, so the various samples used would have slightly different values of sheet resistance, concentration and mobility. Mobility measurements in annealed ion-implanted AlGaIn/GaN HEMTs on SiC without both GaN cap and an AlN spacer layer, have shown robustness in mobility values at activation temperatures up to 1200 °C [19]. This implies that even without the GaN cap or AlN spacer layer, the AlGaIn/GaN structures on SiC substrates are stable under elevated thermal annealing.

4.4.2 Roughness

PECVD Si_3N_4 caps deposited on AlGaIn/GaN HEMTs with high radio frequency, have been shown in experiments performed at 500 °C, to maintain the integrity of the 2-DEG for up to 170 hours of thermal annealing [20]. Due to the thermal stability of the AlGaIn/GaN HEMT structures on SiC substrates, the layer structure of Figure 4.1 was used to evaluate the impact of 30 nm medium-frequency PECVD SiN_x cap on the surface roughness of the annealed samples at 1230 °C. Table 4.1 shows the measured RMS roughness of the samples that were capped before annealing and those that were not. RMS roughness of 0.25 nm was measured on the unannealed samples. Capped samples had approximately the same roughness as the unannealed samples. The impact of HF treatment on the samples was minimal. The slightly higher value of roughness was probably due to the removal of native oxides on the surface. RMS surface roughness of 1.3 nm was observed after 3 minutes annealing at 1230 °C. This is over 70% degradation in surface roughness. Figure 4.8 shows the AFM images of $1\ \mu\text{m} \times 1\ \mu\text{m}$ areas of the various samples on a depth scale of 10 nm. The increased roughness of the uncapped samples could be attributed to nitrogen vacancies that are created on the surface due to the breakdown of Ga-N bonds at the surface despite the NH_3/N_2 ambient.

It was also observed that roughness degraded mobility. Mobility of $1180\ \text{cm}^2/\text{V}\cdot\text{s}$ was measured for the sample with SiN_x cap compared to mobility of $903\ \text{cm}^2/\text{V}\cdot\text{s}$ for the sample without SiN_x cap after annealing at 1200 °C for 3 minutes – a reduction of almost 20% in mobility value. Roughness increases scattering events [21], which affects mobility. It is expected that the surface roughness would change the interfacial smoothness, resulting in more scattering along the path of the 2-DEG. This can explain the degradation of mobility in the samples without SiN_x cap. Annealing without a cap has also been shown to degrade Schottky diode ideality on n-GaN when the n-GaN was annealed at 1150 °C to 1200 °C prior to the formation of the Schottky contacts [22]. It is therefore necessary to cap AlGaIn/GaN layers during high temperature anneal to preserve their structural and electrical properties.

4.5 Conclusion

A systematic study of the effects of annealing at elevated temperatures on three different AlGaN/GaN HEMT structures with various layer thicknesses and structures was carried out. AlGaN/GaN heterostructures grown on SiC substrates were found to have the most robustness to high temperature annealing up to 1230 °C. Structures on sapphire substrates with thicker AlGaN barrier layers performed poorly under elevated temperature anneal. Severe degradation in mobility and sheet resistance was observed. Incorporation of a 1 nm AlN spacer layer with thinner AlGaN barrier layer of about 20 nm ensured the maintenance of the 2-DEG integrity after high temperature anneal.

Also, SiN_x cap layers were critical to maintain the surface morphology of AlGaN/GaN HEMTs during high temperature annealing. Samples that were not capped with SiN_x were found to have increased surface roughness up to five times the value of the unannealed samples and up to 20% degradation in mobility in comparison to capped samples.

4.6 Table

Table 4.1: RMS roughness of annealed samples

Sample	Heat Treatment	30nm SiN _x Cap	RMS Roughness of 1 μm × 1 μm Area [nm]
1	No Anneal	-	0.25
2	No Anneal/ 20 min HF Dip	-	0.43
3	1230 °C/ 3 minutes	Yes	0.24
4	1230 °C/ 10 minutes	Yes	0.37
5	1230 °C/ 3 minutes	No	1.3
6	1230 °C/ 10 minutes	No	1.15

4.7 Figures

GaN 2 nm
Al_{0.25}Ga_{0.75}N 18 nm
AlN 1 nm
GaN 1 μm
SiC Substrate

Figure 4.1: Typical AlGa_N/Ga_N layer structure.

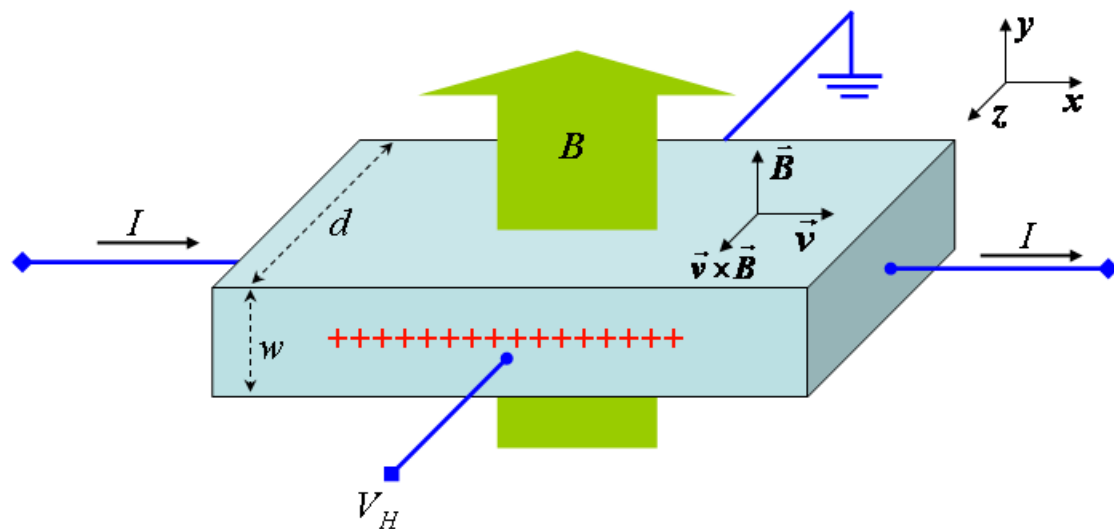
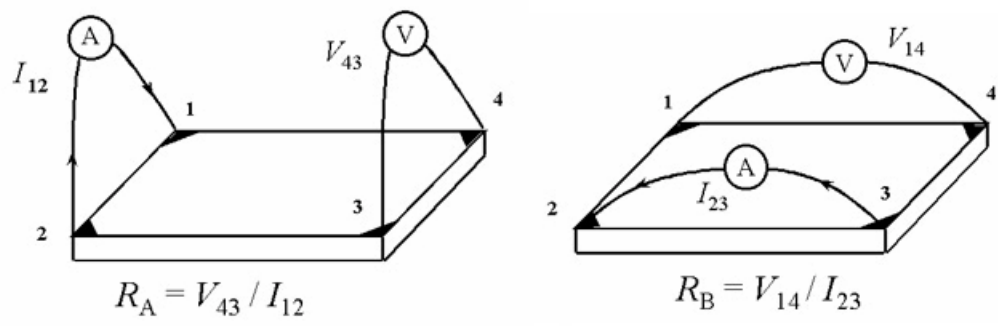
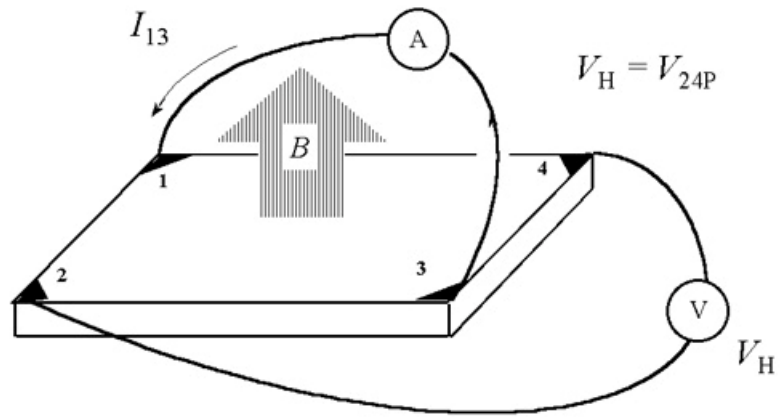


Figure 4.2: Hall bar measurement.

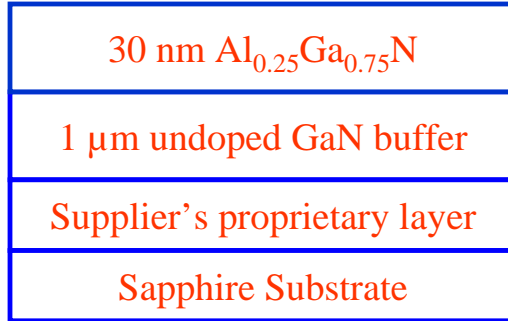


(a) Resistivity measurement

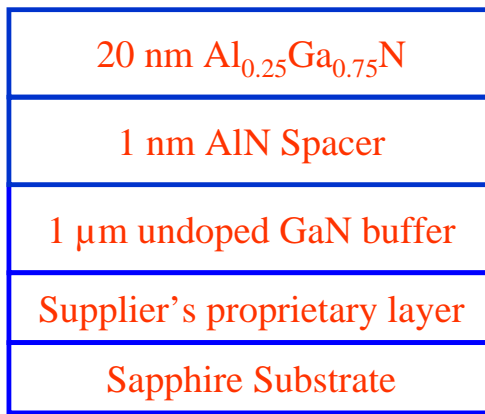


(b) Hall measurement

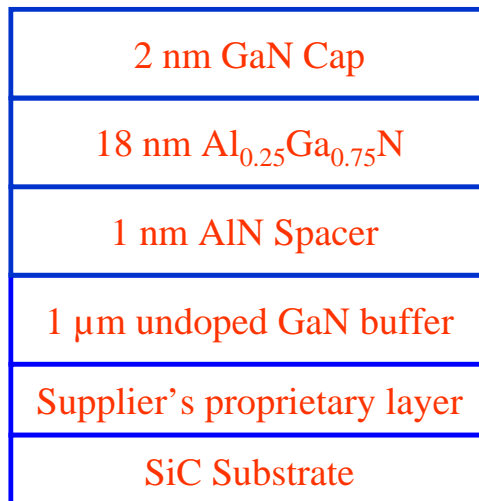
Figure 4.3: Van Der Pauw setup.



(a) $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ on sapphire substrate



(b) $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{AlN}/\text{GaN}$ on sapphire substrate



(c) $\text{GaN}/\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{AlN}/\text{GaN}$ on SiC substrate

Figure 4.4: Layer structures used in the elevated temperature experiment.

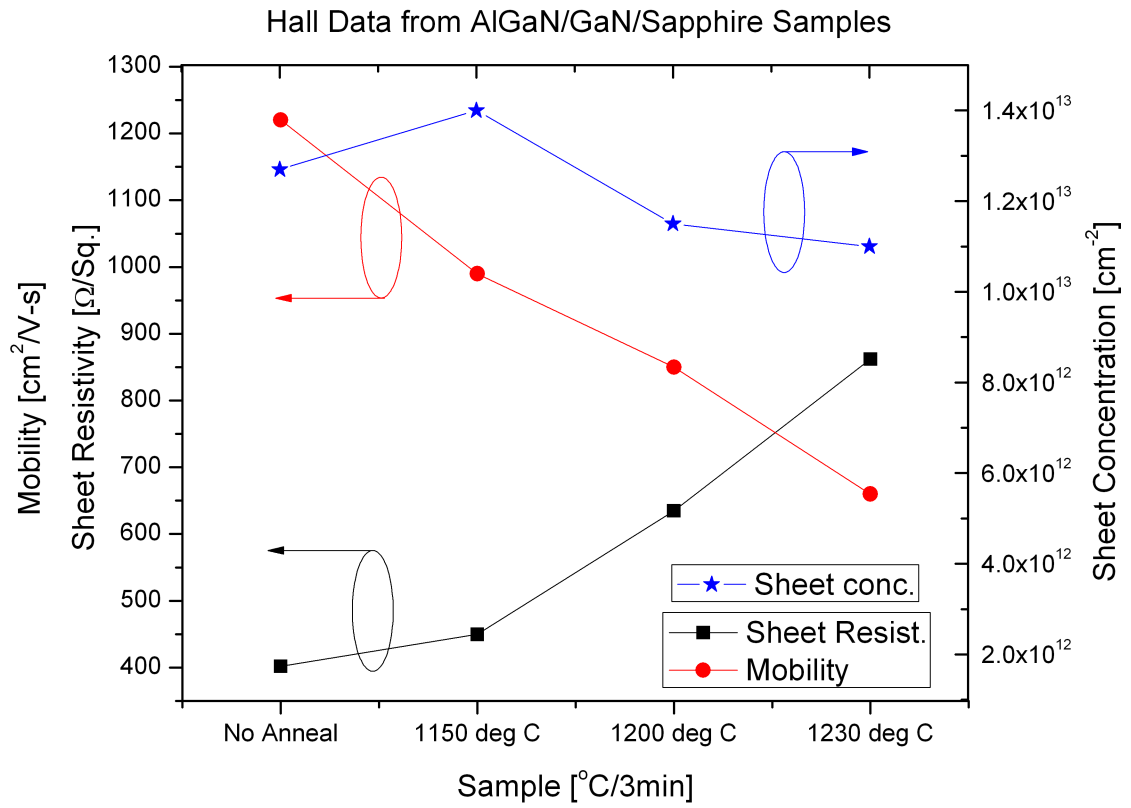


Figure 4.5: AlGaIn/GaN on sapphire.

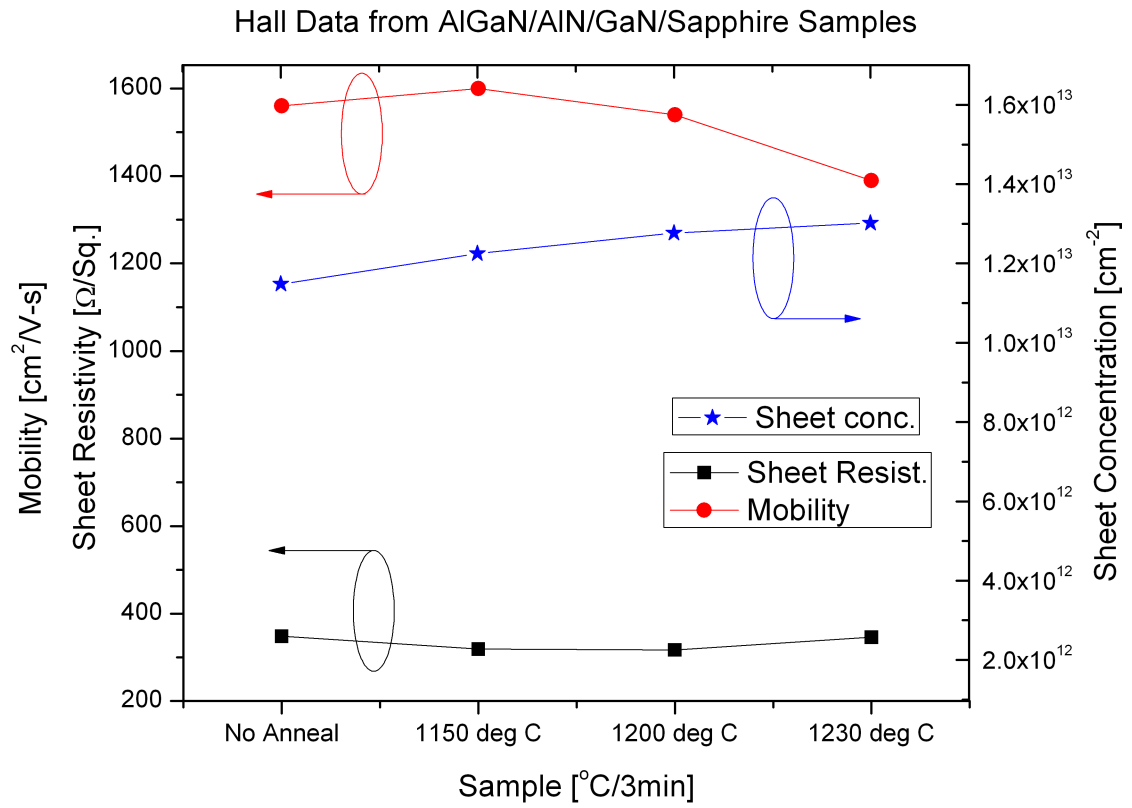


Figure 4.6: AlGa_N/AlN/GaN on sapphire.

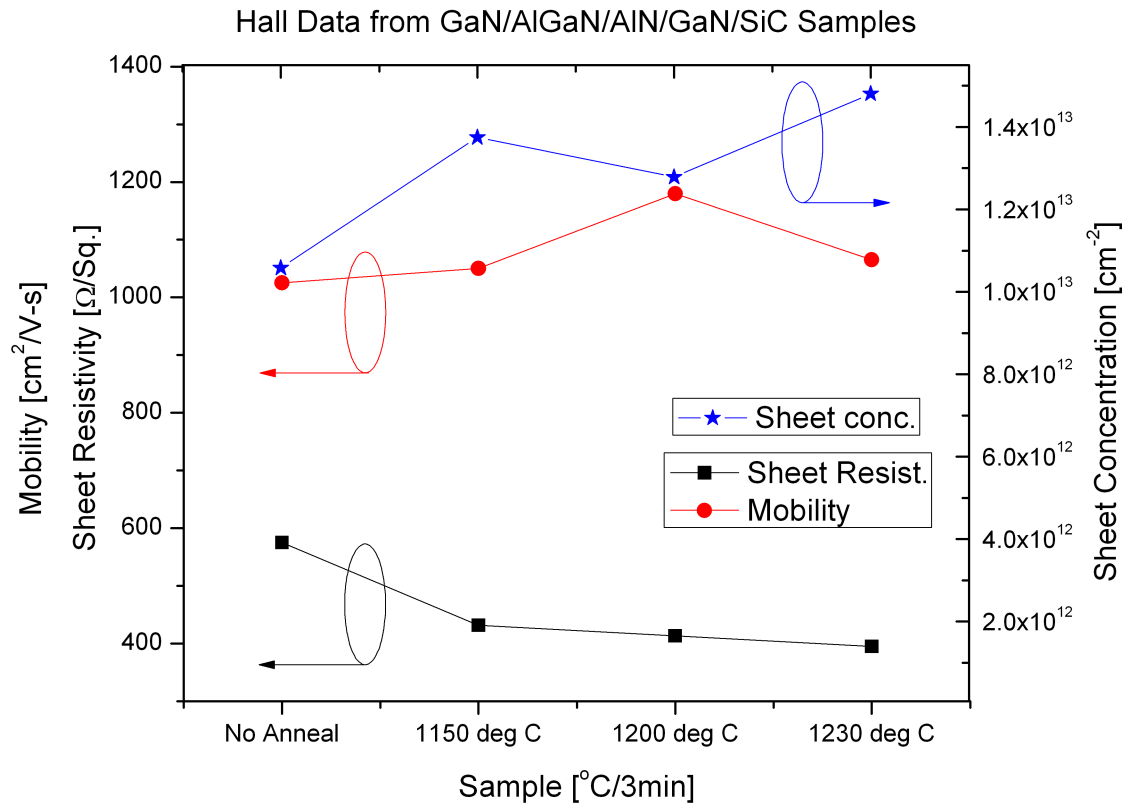


Figure 4.7: GaN/AlGaN/AlN/GaN on SiC.

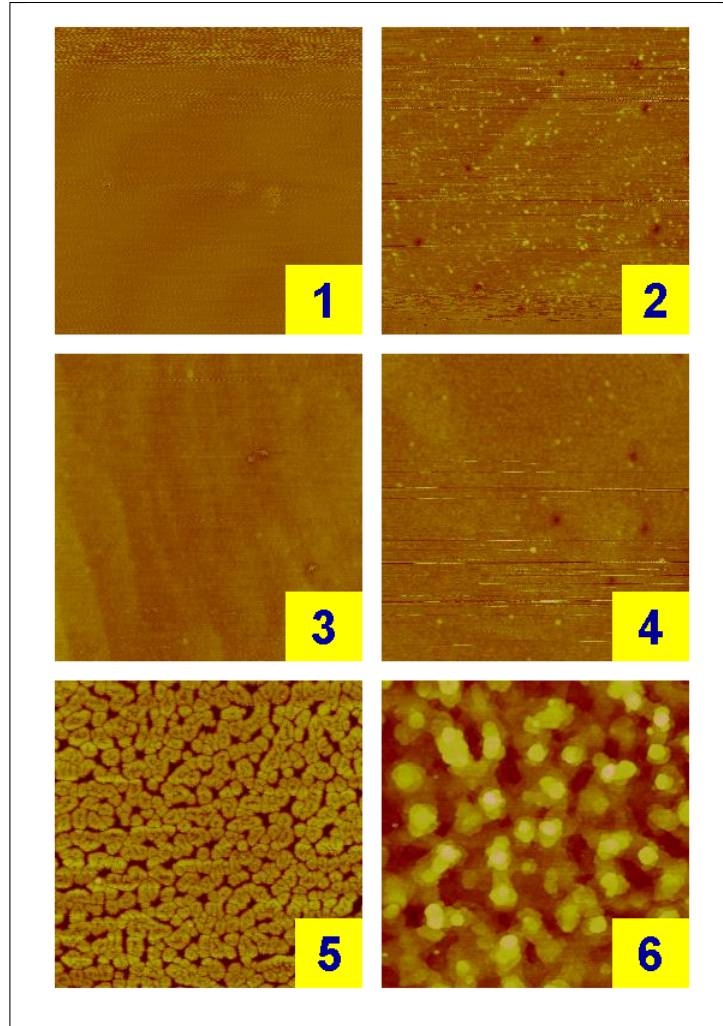


Figure 4.8: 2-D atomic force microscopy images of $1 \mu\text{m} \times 1 \mu\text{m}$ surface areas of samples 1-6.

4.8 References

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CHAPTER 5

ION IMPLANTATION FOR OHMIC CONTACTS TO ALGAN/GAN

5.1 Ohmic Contacts to AlGaN/GaN

Ti/Al/Mo/Au metallization alloyed at ~ 850 °C is usually the metallization of choice for ohmic contacts to n-GaN based systems because of their low contact resistance and excellent sidewall and surface roughness. Some other alternatives are Mo/Al/Mo/Au, Ta/Al/Mo/Au and V/Al/Mo/Au. Mo/Al/Mo/Au metallization with SiCl₄ plasma of the GaN and AlGaN surfaces treatment prior to metal evaporation has also shown excellent contact resistances at anneal temperatures as low as 650 °C [1]. Silicon incorporation in the Ti/Al/Mo/Au contact scheme has also been shown to yield ultra-low ohmic contact resistances [2, 3]. Recently, Basu et al. demonstrated excellent ohmic contacts at 500 °C anneal temperature with thin Mo/Al/Mo/Au metallization employing SiCl₄ plasma treatment [4]. However, the mechanism of ohmic contact formation at such low anneal temperatures is still not known and can vary for layers that are grown differently.

High-dose silicon ion implantation to AlGaN/GaN has recently been employed in making non-alloyed ohmic contacts in AlGaN/GaN heterostructures [5]-[7]. Contact resistances of 0.96 Ω -mm have been reported for these non-alloyed ohmic contacts to AlGaN/GaN on SiC substrate [6]. The potential for non-alloyed ohmic contacts in self-aligned AlGaN/GaN HEMT is immense and thus needs to be explored.

5.2 Selective-Area Implant Process Development

A process for selective-area implantation was developed. The process flow for implantation into the ohmic contact region is shown in Figure 5.1. Starting with the AlGaIn/GaN layer, a low-pressure chemical vapor deposition (LPCVD) SiN_x of 30 nm thickness was deposited at 800 °C. This layer served two purposes. Firstly, it served to protect the AlGaIn layer from the ambient, and secondly, it helped to make the projected range of the implanted Si ions lie within the AlGaIn layer ensuring very high concentration in the AlGaIn layer. As discussed in Sections 3.4 and 3.5, the range for 30 keV and 40 keV Si implantation into AlGaIn/GaN without any SiN_x cap is ~30 nm. Using SRIM, simulations were carried out with 30 nm of Si₃N₄ cap layer and the implant range was found to be around 30 nm from the Si₃N₄ surface, coinciding with the area covering the AlGaIn barrier layer. Using photolithography, 100 nm of Ni Mask was defined, patterned, and deposited by e-beam evaporation and lifted-off on the sample. The open regions were the areas where the ohmic contacts were fabricated. Next, high dose ($1 \times 10^{15} \text{ cm}^{-2}$, $1 \times 10^{16} \text{ cm}^{-2}$, $5 \times 10^{16} \text{ cm}^{-2}$) silicon ions were implanted in the open regions at multi-energies of 30 keV and 40 keV on one set of samples, and at 40 keV and 50 keV on another. The 100 nm Ni mask shielded the non-ohmic area from implantation.

After implantation, Ni etchant was used to remove the Ni mask and 49% HF was used to remove the SiN_x. A new layer of 30 nm LPCVD SiN_x was then re-deposited on the implanted samples. The samples were annealed in the furnace at 1200 °C for 3 minutes in flowing N₂ ambient at about 20 sscm. The SiN_x cap layer was utilized to protect the top surface of the AlGaIn/GaN from decomposition at elevated temperatures.

After annealing, the SiN_x was removed with 49% HF. Mesa patterns were then defined using Ar/Cl₂ inductively-coupled plasma reactive ion etch. Mo/Al/Mo/Au (15/60/35/50 nm) metallization stack was then patterned and deposited on the selectively implanted areas.

5.3 High Dose Multi-Energy Implantation in AlGa_N/Ga_N

In order to explore high-dose implantation in the fabrication of non-alloyed ohmic contacts, the layer structure of Figure 5.2 was used in this study. The selective-area implantation process described above was used to implant Si ions at multi-energies of 30 keV and 40 keV, and at 40 keV and 50 keV. Transfer length method (TLM) pads with 100 μm widths were patterned and selectively implanted. The gap of the TLM pads ranged from 2 μm to 10 μm . The implants were performed at a very high dosage of $5 \times 10^{16} \text{ cm}^{-2}$. Some of the implanted samples were subjected to SiCl_4 RIE plasma treatment at -300 V bias for 1 minute, 1.5 minutes, and 2 minutes, respectively, before ohmic contact deposition. It was determined that SiCl_4 RIE plasma treatment effectively etches Ga_N and AlGa_N at the rate of 10 nm/minute. Non-implanted control samples with and without SiCl_4 RIE plasma treatment were also processed. Mo/Al/Mo/Au was then deposited on the patterned TLMs. The control samples were annealed at 850 °C after ohmic contact deposition.

5.4 Results

Figure 5.3 shows a comparison of the current-voltage curve for the 10 μm gap of the TLM pads of the various samples. The non-implanted control samples had rectifying behavior before anneal. After RTA anneal at 850 °C, they had ohmic behavior as expected. A 1 minute SiCl_4 plasma treatment to the control sample prior to TLM metal deposition led to higher current levels because the SiCl_4 etches away about 10 nm of AlGa_N and hence brought the ohmic contact closer to the 2-DEG channel of the AlGa_N/Ga_N HEMT.

On the other hand, the implanted samples gave ohmic behavior even for as-deposited ohmic contacts. SiCl_4 plasma treatment did not significantly alter the current levels, but improved the ohmic contact resistance significantly as shown in Figure 5.4. The implanted sample with no SiCl_4 plasma treatment had an ohmic contact resistance of 3.59 $\Omega\text{-mm}$ and specific contact resistivity of $3.16 \times 10^{-5} \Omega\text{-cm}^2$

as deposited but improved to $0.24 \Omega\text{-mm}$ and $1.31 \times 10^{-7} \Omega\text{-cm}^2$, respectively, after $850 \text{ }^\circ\text{C}$ RTA anneal. An ohmic contact resistance of $0.20 \Omega\text{-mm}$ and specific contact resistivity of $1.06 \times 10^{-7} \Omega\text{-cm}^2$ was obtained for the implanted sample with 1 minute SiCl_4 plasma treatment. The lowest non-alloyed contact resistance to AlGaIn/GaN reported in the literature is $0.96 \Omega\text{-mm}$ [5]-[10]. Further SiCl_4 plasma treatment time did not yield further improvements in the contact resistance.

The sheet resistance of the implanted samples was found to be extremely high, as can be seen in Table 5.1. Despite annealing the samples at $1200 \text{ }^\circ\text{C}$, the sheet resistance was about 5 times the sheet resistance of the non-implanted sample. Structural damage during high dose ($5 \times 10^{16} \text{ cm}^{-2}$) implantation was shown to have caused evolution of the material into forming oxygen-rich compounds as discussed in Section 3.5.2. So this high value of the sheet resistance compared to non-implanted samples can be attributed to the damage in the selectively implanted AlGaIn.

Using lower implantation dose of $1 \times 10^{16} \text{ cm}^{-2}$ and 30 keV single energy Si implantation into the AlGaIn/GaN structure of Figure 4.1 which had a GaN cap, the developed selective-area silicon implantation process was applied. PECVD SiN_x instead of LPCVD SiN_x was employed. The sheet resistance of the resulting Mo/Al/Mo/Au ohmic contact was improved, but very good ohmic contacts were not obtained even on samples that were annealed at $590 \text{ }^\circ\text{C}$ for 3 minutes after depositing the ohmic metal. Figure 5.5 shows the results. Therefore, to achieve contacts with very low resistivities, more optimization of the implantation dose needs to be carried out. Multi-energy implantation at lower doses would be key in solving this problem.

5.4.1 XPS study of surface components

The sheet resistance of the implanted samples was higher than that of the non-implanted samples, as shown in Table 5.1. Despite activating the dopants in the implanted samples at $1200 \text{ }^\circ\text{C}$ for 3 minutes in the furnace in N_2 ambient, the sheet

resistance was still higher. It is probable that the high dose implantation had significantly changed the structure of the AlGa_N top layer. X-ray photoelectron spectroscopy was used to analyze the surface composition of the AlGa_N/Ga_N HEMT layer before and after implantation and annealing. Figure 5.6 shows the comparison. Very high percentages of oxygen and carbon were observed after implantation. The silicon atomic composition at the surface was surprisingly lower in comparison with the non-implanted sample. Since 49% HF was used to remove the protective SiN_x layer after activation, it is expected that any oxide at the surface will be completely removed. However, the high amount of oxygen present may be due to the heating up of the samples during implantation, causing the oxidation of the silicon. After activation, some of the near-surface oxide-based compounds are perhaps slightly different from the original AlGa_N top surface. This may also explain the changing sheet resistance observed for the annealed samples after implantation.

5.5 Conclusion

A process for high-dose silicon ion implantation into AlGa_N/Ga_N HEMTs for improved ohmic contact performance was developed and characterized. Non-alloyed ohmic contact with Mo/Al/Mo/Au (15/60/35/50 nm) metallization to AlGa_N/Ga_N layers with contact resistance as low as 0.2 Ω-mm and specific contact resistivity of 1.06×10^{-7} Ω-cm² was demonstrated. Given the improvements in the contact resistance of the material with the developed process, it is possible to fabricate non-alloyed ohmic contacts on AlGa_N/Ga_N HEMT layers.

The surface morphology of the implanted AlGa_N/Ga_N layer before and after annealing showed very oxygen- and carbon-rich surfaces. The composition after annealing indicated that materials different from AlGa_N formed at the surface. Possibly, these are compounds of AlGa_N with higher oxygen and carbon contents. Further studies need to be carried out to fully understand the chemical nature of these compounds.

5.6 Table

Table 5.1: Contact resistance of implanted and non-implanted samples

Sample	A	B	C	D	E	F	D
Implantation	No	No	40keV and 50keV	40keV and 50keV	40keV and 50keV	40keV and 50keV	40keV and 50keV
SiCl₄ Plasma	No	1 min	No	No	1 min	1.5 min	2 min
RTA Anneal at 850 C	Yes	Yes	No	Yes	No	No	No
Transfer Length L_T [μm]	3.72	6.12	0.88	0.06	0.05	0.14	0.37
Sheet Resistance [$\Omega/\text{Sq.}$]	1611.43	606.02	4078.80	4322.21	3916.86	4102.90	4479.19
Contact Resistance [$\Omega\text{-mm}$]	6.00	3.71	3.59	0.24	0.20	0.56	1.66
Specific Contact Resist. [$\Omega\text{-cm}^2$]	2.23E-04	2.27E-04	3.16E-05	1.31E-07	1.06E-07	7.57E-07	6.14E-06

5.7 Figures

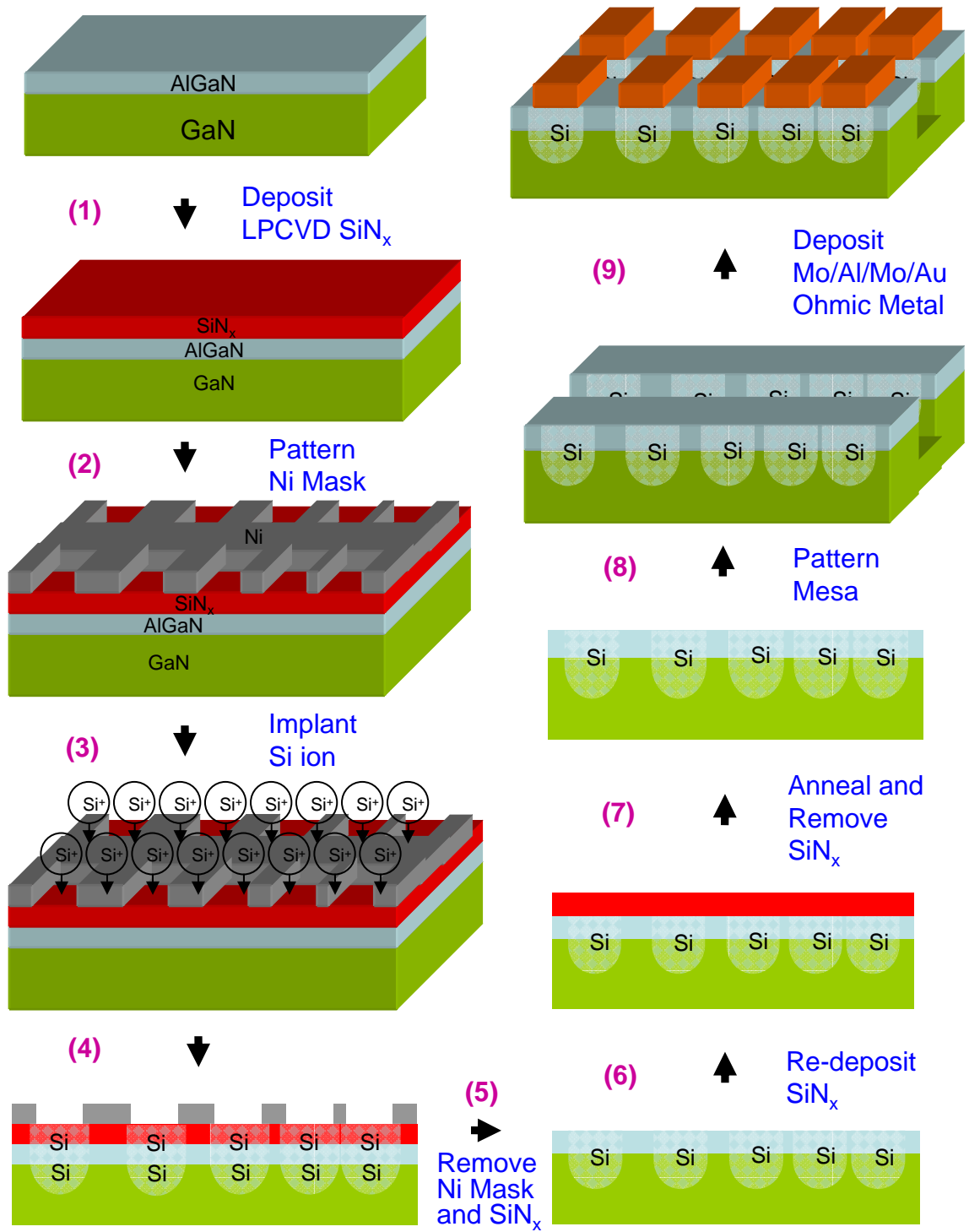


Figure 5.1: Selective-area Si ion implantation process flow.

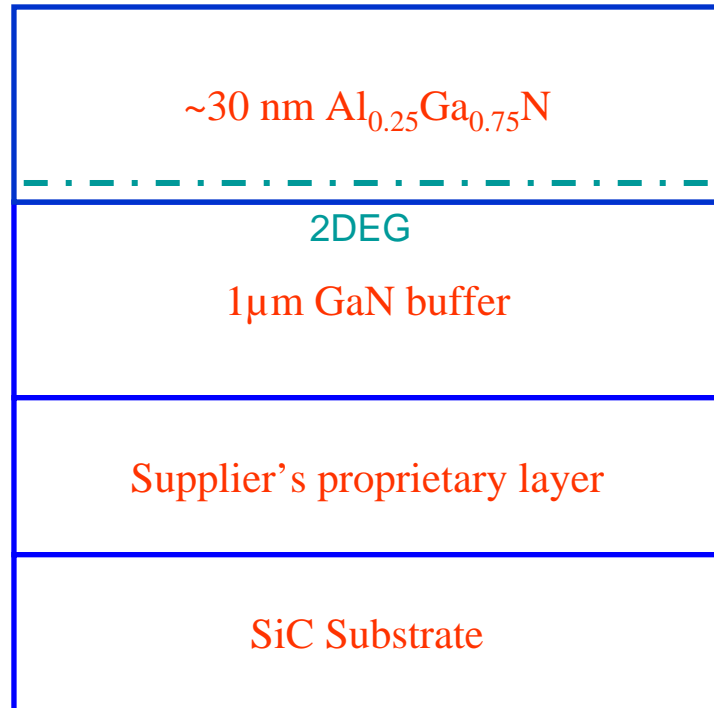


Figure 5.2: AlGaN/GaN HEMT on SiC substrate.

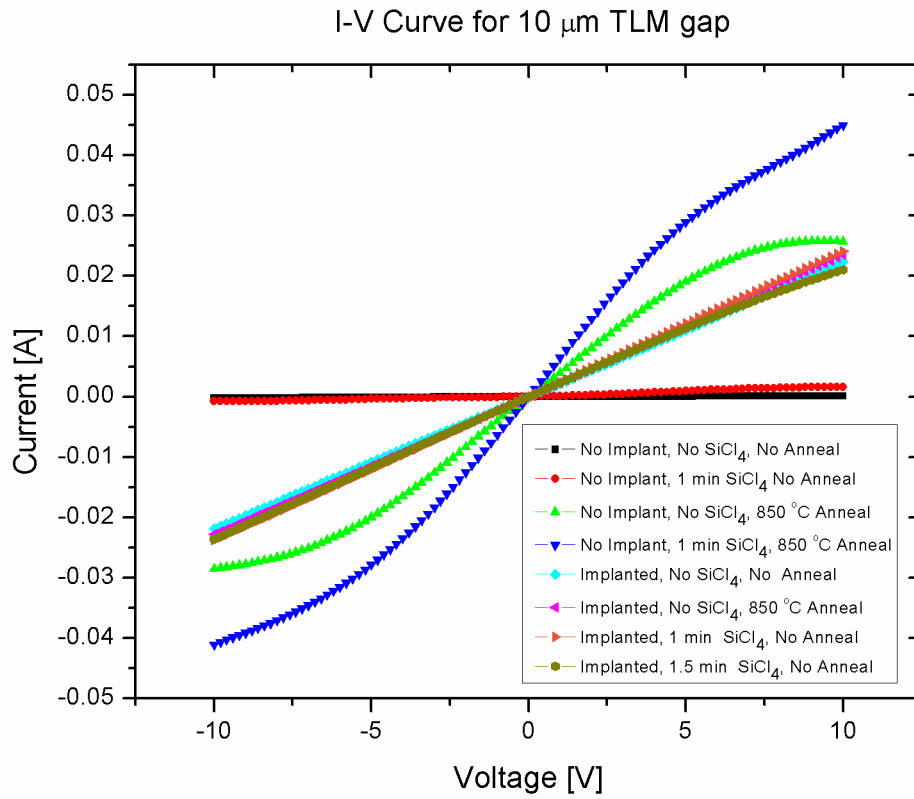


Figure 5.3: I-V curve for the AlGa_N/Ga_N layer structure of Figure 5.2 for non-implanted and selective-area, 30 keV and 40 keV multi-energy Si-ion-implanted samples at $5 \times 10^{16} \text{ cm}^{-2}$ dose.

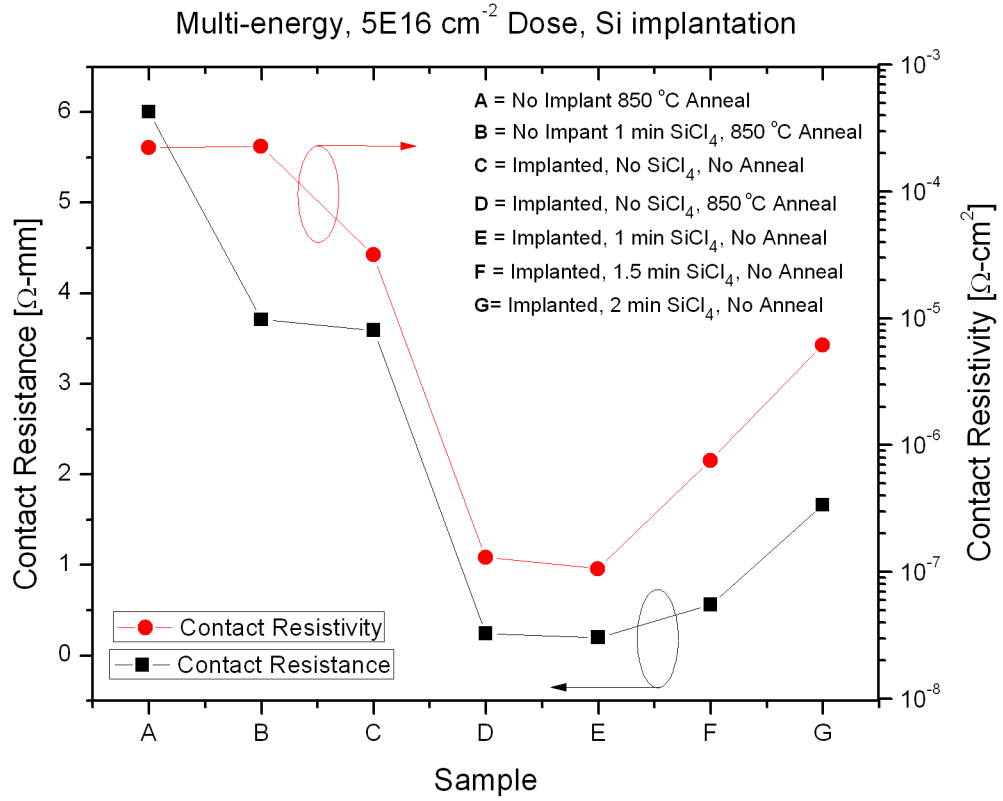


Figure 5.4: Contact resistance of non-implanted and selective-area, 30 keV and 40 keV multi-energy Si-ion-implanted samples at $5 \times 10^{16} \text{ cm}^{-2}$ dose using Mo/Al/Mo/Au ohmic metallization stack. AlGaN/GaN layer structure of Figure 5.2 was used.

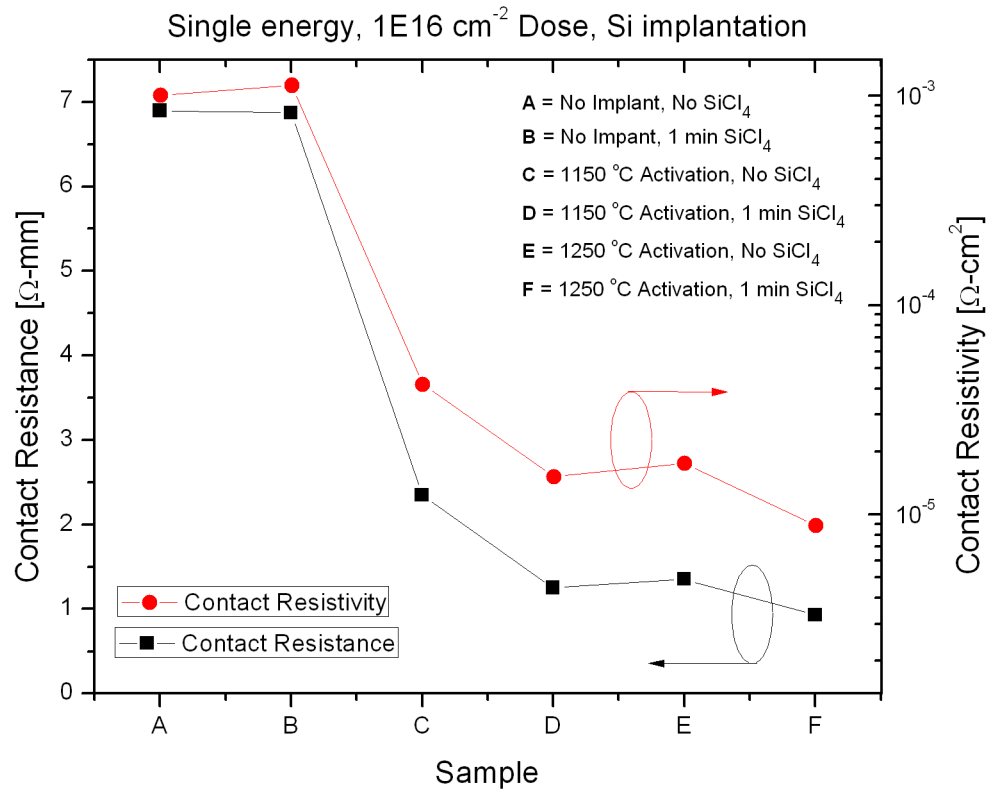


Figure 5.5: Contact resistance of non-implanted and selective-area, 30 keV single energy Si-ion-implanted samples at $1 \times 10^{16} \text{ cm}^{-2}$ dose using Mo/Al/Mo/Au metallization stack. AlGaN/GaN layer structure of Figure 4.1 was used. The contacts were annealed, after deposition, at 590 °C for 20 minutes under N_2 ambient.

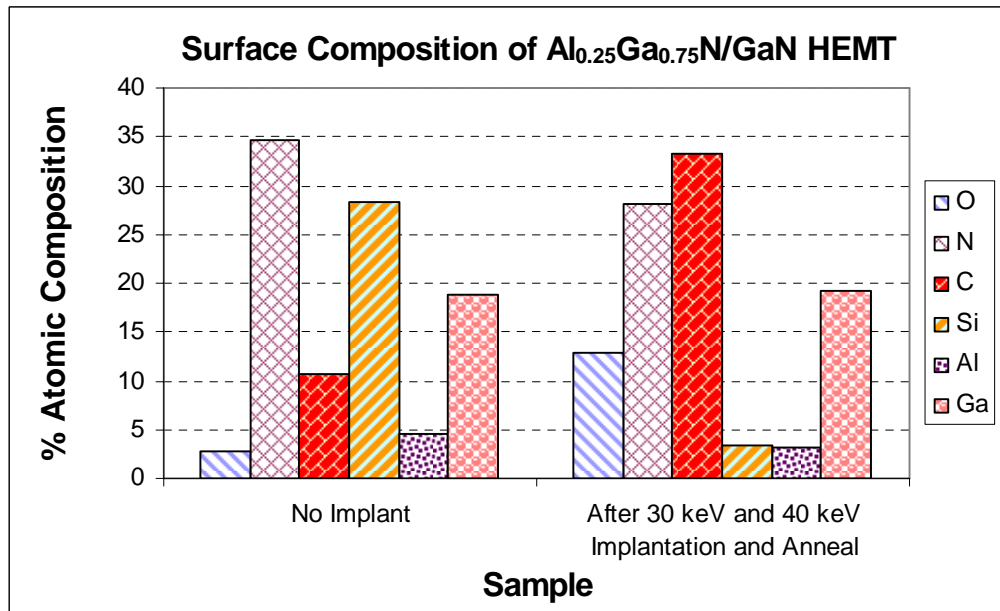


Figure 5.6: XPS surface composition data of AlGa_{0.25}N/GaN layer on SiC after annealing at 1200 °C for 3 minutes.

5.8 References

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CHAPTER 6

FURTHER WORK

6.1 Summary of Work

A process for selective-area silicon ion implantation to AlGaIn/GaN was used to fabricate TLM structures. Very low-resistance non-alloyed ohmic contacts with contact resistances of 0.20 Ω -mm were successfully fabricated and characterized. Schottky metallizations to AlGaIn/GaN HEMTs were also comparatively studied and the best and most robust metallizations were found to be Ni/Au, Ir/Pt/Au and Pt/Au metallizations.

6.2 Conclusion and Further Work

6.2.1 Thermal stability of silicon ion implanted contacts

The thermal stability of the implanted samples needs to be further investigated. Nonetheless, the annealed implanted sample at 850 $^{\circ}$ C showed improved contact resistance as shown in Table 5.1.

6.2.2 Reduction of sheet resistance

The high sheet resistance is not desirable as this would affect the ON-resistance of devices. More optimized annealing techniques in the activation step can be employed to improve the sheet resistance of the implanted samples. Also, multi-implants at lower doses to achieve a higher dose may actually be better than implanting at high doses directly. Multiple implants at 2×10^{16} cm^{-2} and 3×10^{16}

cm^{-2} may actually yield better results than implanting at $5 \times 10^{16} \text{ cm}^{-2}$ as this may reduce the surface effects of strong oxidation, which was observed during $5 \times 10^{16} \text{ cm}^{-2}$ dose studies of Section 3.5.2.

6.2.3 Co-implantation of Ti and Si ions

Co-implanting Ti ions with Si ions may improve the sheet resistance. Since TiN formation has been determined to be instrumental in the formation of low ohmic contacts for Ti/Al/Mo/Au metal stacks to AlGaN/GaN [1], it is possible that co-implanting Ti ions with Si ions would greatly improve the sheet resistivity and yield ohmic contacts with very low contact resistivities.

6.2.4 Silicon ion implanted AlGaN/GaN HEMTs

Having taped out the process for fabrication of non-alloyed ohmic contacts using selective-area implantation techniques and developed a very robust Schottky contact metallization to AlGaN/GaN HEMTs, the potential for the fabrication of traditional and self-aligned AlGaN/GaN HEMTs has been made possible. A potential process for these HEMTs is shown in Figure 6.1.

6.2.5 Implanted self-aligned AlGaN/GaN HEMTs

Recently, a true self-aligned AlGaN/GaN HEMT was demonstrated with low temperature Mo/Al/Mo/Au ohmic contacts [2]. Figure 6.2 shows a possible process for fabricating self-aligned HEMTs with implanted source and drain areas.

6.2.6 Implanted single metallization AlGaN/GaN HEMTs

Preliminary experiments not included in this dissertation have indicated that there is the possibility of having single metallization for both Schottky and ohmic contact metallization. Ni/Au deposited on high-dose silicon implanted GaN and

AlGaN/GaN shows ohmic behavior. This needs to be further investigated. Selective implantation of the ohmic region and deposition of Ni/Au on both the ohmic and Schottky gate in one process would be a very attractive application of selective-area implantation of high dose silicon ions. The proposed technique is outlined in Figure 6.3.

6.3 Figures

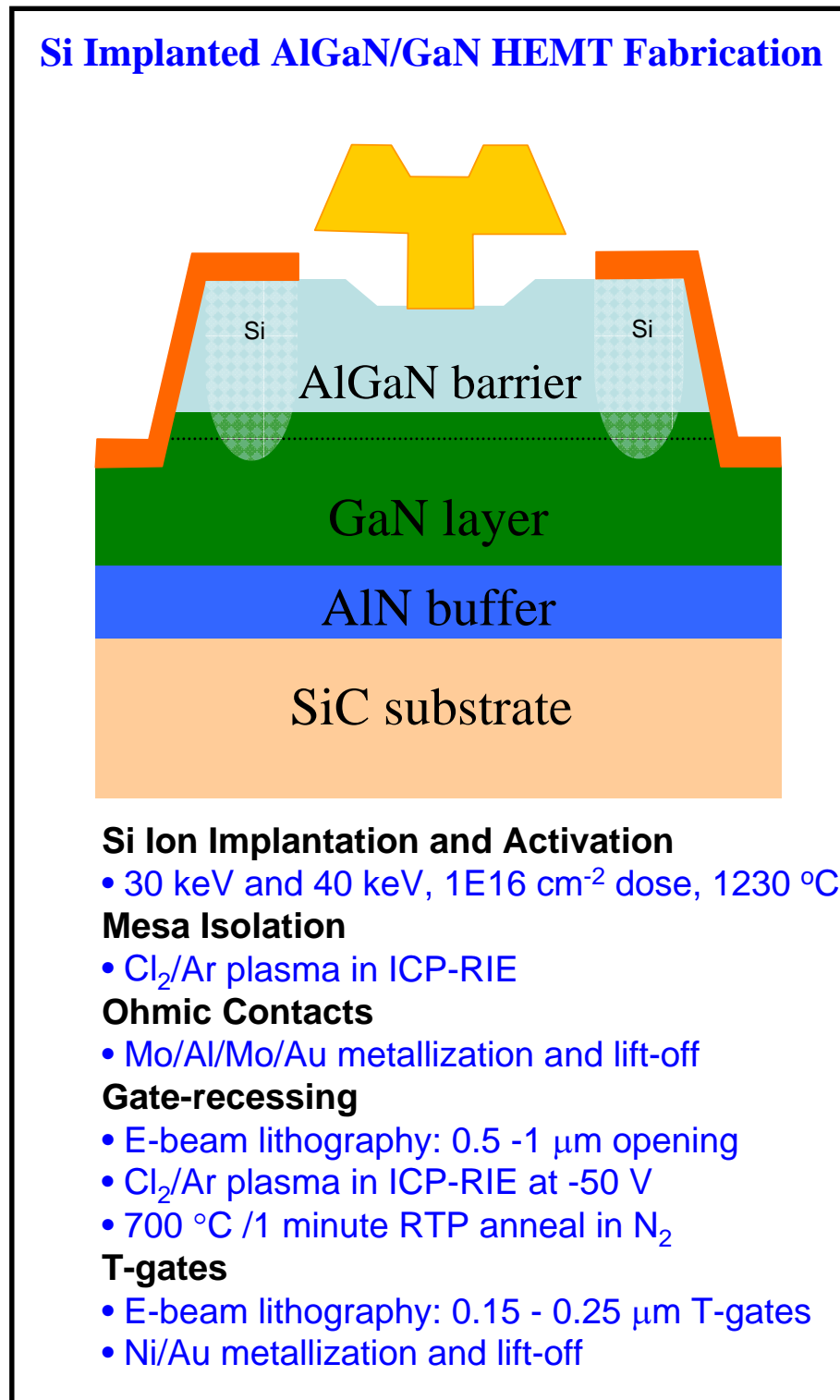
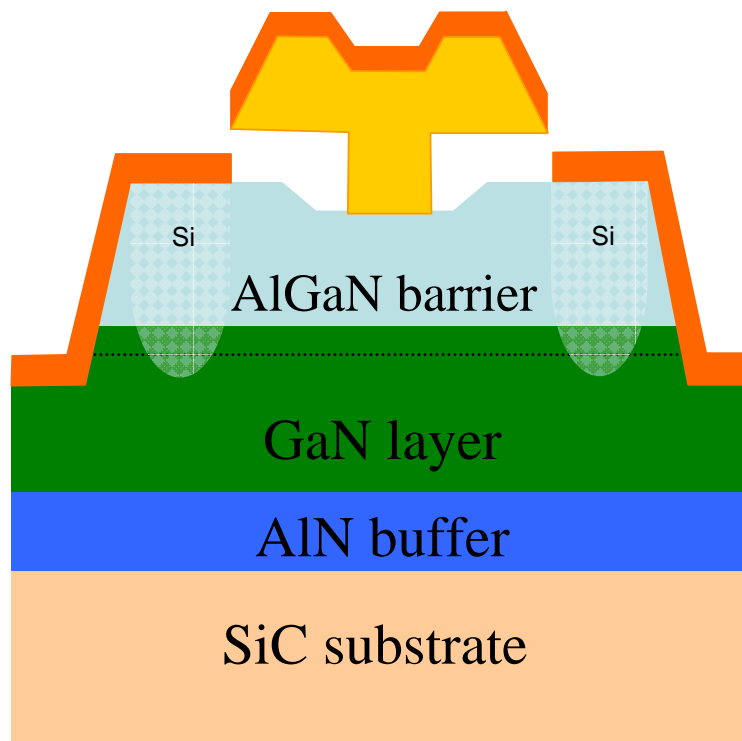


Figure 6.1: Process for implanted high speed HEMTs.

Self-Aligned AlGaN/GaN HEMT Fabrication



Si Ion Implantation and Activation

- 30 keV and 40 keV, $1E16 \text{ cm}^{-2}$ dose, 1230 °C

Mesa Isolation

- Cl_2/Ar plasma in ICP-RIE

Gate-recessing

- E-beam lithography: 0.5 -1 μm opening
- Cl_2/Ar plasma in ICP-RIE at -50 V
- 700 °C/1 minute RTP anneal in N_2

T-gates

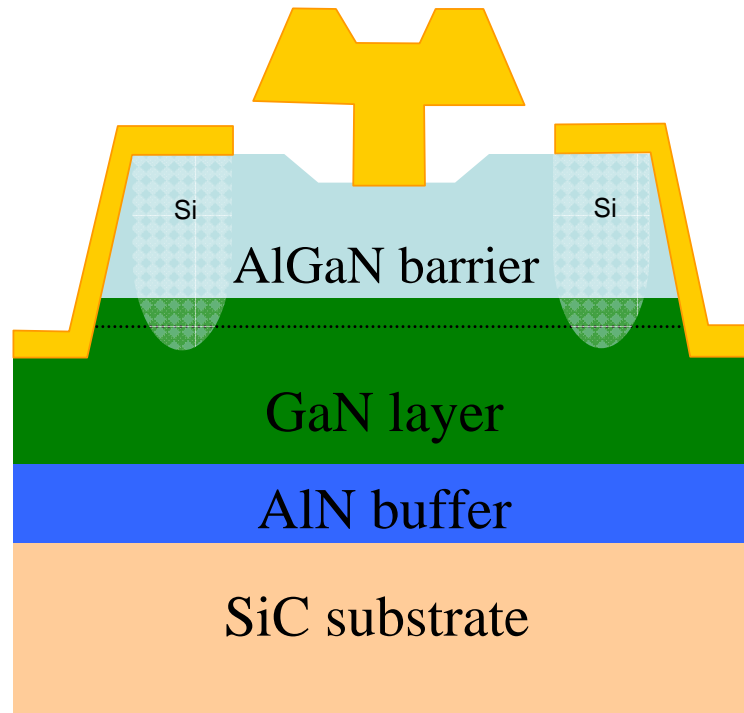
- E-beam lithography: 0.15 - 0.25 μm T-gates
- Ni/Au metallization and lift-off

Ohmic Contacts

- Mo/Al/Mo/Au metallization and lift-off

Figure 6.2: Scheme for high dose implanted self-aligned HEMTs.

Single Metal AlGaN/GaN HEMT Fabrication



Si Ion Implantation and Activation

- 30 keV and 40 keV, $1E16 \text{ cm}^{-2}$ dose, 1230 °C

Mesa Isolation

- Cl_2/Ar plasma in ICP-RIE

Gate-recessing

- E-beam lithography: 0.5 -1 μm opening
- Cl_2/Ar plasma in ICP-RIE at -50 V
- 700 °C/1 minute RTP anneal in N_2

T-gates and Ohmic Contacts

- E-beam lithography: 0.15 - 0.25 μm T-gates
- Ni/Au metallization and lift-off

Figure 6.3: Single metallization for gate, source and drain in extremely high dose implanted for AlGaN/GaN HEMTs.

6.4 References

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Benedict Chukwuka Ofuonye graduated, first class honors, from the University of Nigeria, Nsukka, in 1998 with the B.Eng degree, after studying Electronic Engineering for six years. He emerged the valedictorian in a graduating class of 6000. He received several awards including the singular distinction of delivering the valedictory speech at the convocation ceremony. He then obtained the MSc degree in Electrical and Computer Engineering from the University of Waterloo in 2003. Prior to attending the University of Waterloo, he worked in the Asset Management division of Chevron Texaco in Nigeria as an information analyst during his National Youth Service Corps (NYSC) program. Shortly before graduation from the University of Waterloo, he joined the IBM Toronto laboratory. At IBM, Benedict Ofuonye was a member of the core development team for the IBM VisualAge C/C++ compiler. He successfully contributed features to both versions 6.0 and 7.0 of the compiler. In August, 2004, Benedict Ofuonye joined the Nanoscale Processing and Devices Group at the Micro and Nanotechnology laboratory of the University of Illinois at Urbana-Champaign where his research focused on process development for ohmic and Schottky contacts to AlGa_N/Ga_N high electron mobility transistors. He has authored and co-authored a number of journal and conference papers in this area. In the summer of 2008, he also worked as an intern at the Novel Devices Group of Intel's Components Research division in Hillsboro, Oregon, where he validated substrate quality for next generation MOS inversion layer transistors. At Intel, he also designed, implemented and taped out novel ring and square donut transistors for easy characterization of mobility in Intel's next generation transistors.