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Multicrystalline Silicon Ribbons Grown Over a Dust Substrate

"Documento Definitivo"

Doutoramento em Sistemas Sustentáveis de Energia

Filipe Carreira Serra

Tese orientada por:
Professor Doutor João Manuel de Almeida Serra
Doutor José Almeida Silva

Documento especialmente elaborado para a obtenção do grau de doutor

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Abstract

The Silicon on Dust Substrate (SDS) is a gas-to-wafer process, developed to manufacture multicrystalline silicon ribbons directly from gaseous feedstock (silane), avoiding the standard industry stages of polysilicon deposition, crystal growth and wafering. It aims to achieve good quality material for solar cell manufacturing with a significant reduction of the overall photovoltaic systems cost.

The focus of the work presented in this thesis is the improvement of the entire SDS technique, which consists of three main steps: (i) production of silicon powder; (ii) chemical vapour deposition (CVD) of silicon over a silicon powder substrate; and (iii) zone melting recrystallization (ZMR) of the microcrystalline pre-ribbon obtained in the CVD step. Additionally, the best practices and optimal experimental parameters across the three steps were identified.

A new experimental setup to produce micrometric sized silicon powders from multicrystalline silicon wafers was tested, characterized and used to manufacture six silicon powders of well-defined particle size intervals, ranging from ≤25 to]180; 250] μm.

The powder substrate properties, such as particle size, mass per unit of area and porosity, have a preponderant influence on the success of the CVD process and the physical characteristics, like powder ratio, growth rate and porosity, of the microcrystalline pre-ribbon grown over the powder substrate. It was demonstrated that as the powder substrate particle size decreases, the CVD growth rate increases (up to 52.8 μm/min) and both pre-ribbon porosity and powder ratio decreases (down to 52.7 ± 7.3% and 0.60 ± 0.01, respectively).

The ZMR process performance is substantially impacted by the pre-ribbon physical characteristics, as the best crystallized material was obtained from pre-ribbons grown over powder substrates with smaller particle size (≤75 μm), which also have a lower porosity and powder incorporation from the substrate. Multicrystalline silicon ribbons were successfully produced, having large crystalline areas measuring approximately 2×4 cm^2, with visible columnar crystal growth and an average crystal size in the 1 to 10 mm range. The measured resistivity was 0.70 ± 0.05 Ω.cm, equivalent to a dopant concentration of 2.1×10^{16} cm^{-3} and a measured minority carrier lifetime of 0.3 ± 0.1 μs.

The ability to produce multicrystalline silicon ribbons by CVD over a powder substrate, previously obtained from grinding small silicon chunks, followed by a recrystallization step with a linear molten zone was demonstrated.

Keywords: Photovoltaic, Silicon Powder, Silicon Feedstock, Silicon Ribbons, Chemical Vapour Deposition, Zone Melting Recrystallization.

Resumo

O Silício sobre Substrato de Pó (SDS da sigla em inglês) é um processo desenvolvido para fabricar fitas de silício multicristalino directamente a partir de uma fonte gasosa (silano), evitando as etapas industriais de deposição de poli-silício, crescimento de cristal e corte em bolachas. Este processo tem por objectivo alcançar um material com boa qualidade cristalográfica para o fabrico de células solares, aliado a uma expressiva redução do custo global dos sistemas fotovoltaicos.

O foco do trabalho apresentado nesta tese é o aperfeiçoamento de toda a técnica SDS, a qual consiste em três passos principais: (i) produção de pó de silício; (ii) deposição química em fase de vapor (CVD da sigla em inglês) de silício sobre um substrato de pó de silício; e (iii) recristalização por zona fundida flutuante (ZMR da sigla em inglês) da fita microcristalina obtida no passo de CVD. Adicionalmente, foram identificadas as melhores práticas e parâmetros experimentais ideais para os três passos, que possibilitam obter fitas de silício multicristalino de melhor qualidade.

Um novo sistema experimental para a produção de pó de silício com granulometria micrométrica a partir de bolachas de silício multicristalino foi testado, caracterizado e usado na produção de seis pós de silício com intervalos bem definidos de dimensão de partículas, variando entre ≤25 e]180; 250] μm.

A dimensão das partículas, massa por unidade de área e porosidade são propriedades do substrato de pó que têm uma importante influência no sucesso do processo de CVD e nas propriedades físicas da pré-fita de silício microcristalino crescida sobre o substrato de pó, tais como rácio de pó, taxa de crescimento e porosidade. Foi demonstrado que à medida que a dimensão das partículas do substrato de pó diminui, a taxa de crescimento por CVD aumenta (até 52.8 μm/min) e ambos os valores de porosidade e rácio de pó da pré-fita diminuem (até 52.7 ± 7.3% e 0.60 ± 0.01, respectivamente).

Consequentemente, o êxito do processo ZMR é fortemente afectado pelas características da pré-fita, de tal modo que o material cristalizado de melhor qualidade foi obtido a partir de pré-fitas crescidas sobre substratos de pó com partículas de menor dimensão (≤75 μm), as quais também têm menor porosidade e incorporação de pó do substrato. Foram produzidas fitas de silício multicristalino com sucesso, tendo-se obtido largas áreas cristalinas, medindo aproximadamente 2×4 cm^2, com crescimento cristalino colunar e com uma dimensão média do

cristal no intervalo de 1 a 10 mm. O valor de resistividade obtido foi 0.70 ± 0.05 Ω.cm, equivalente a uma concentração de dopante de 2.1×10^{16} cm^{-3} e o valor obtido para o tempo de vida de portadores minoritários foi de 0.3 ± 0.1 µs.

Foi demonstrada a capacidade de produção de fitas de silício multicristalino, por CVD sobre um substrato de pó, previamente obtido a partir da moagem de pedaços silício, seguido de um passo de recristalização por zona fundida.

Palavras chave: Fotovoltaico, Pó de Silício, Matéria-prima, Fitas de Silício, Deposição Química em Fase de Vapor, Recristalização por Zona Fundida.

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List of Acronyms

a-Si	amorphous silicon
BOS	balance of system
CdTe	cadmium telluride
CH_3COOH	acetic acid
CO_2eq	CO_2 (carbon dioxide) equivalent
CP4	etching solution
$Cu(In,Ga)(Se,S)_2$ or CIGS	copper indium gallium diselenide
CVD	chemical vapour deposition
Cz	Czochralski
DS	directional solidification
EFG	edge-defined film-fed
FBR	fluidized bed reactor
FZ	floating zone
GaAs	gallium arsenide
GaInP	gallium indium phosphide
GDP	gross domestic product
HF	hydrofluoric acid
HNO_3	nitric acid
MG-Si	metallurgical grade silicon
PV	solar photovoltaics
RGS	ribbon growth on substrate

SDS	silicon on dust substrate
SEM	scanning electron microscopy
SF	silicon film™
SiO	silicon monoxide
SiO_2	silicon dioxide
STR	string ribbon
toe	ton of oil equivalent
UMG	metallurgical grade silicon
WEB	dendritic web
Wp	watt-peak
ZMR	zone melting recrystallization

Chapter 1

Introduction

1.1. World Energy Outlook

World primary energy consumption has been continuously growing over the last century, showing two distinct periods: the first one between 1900 and 1950, going from 1040 Mtoe (ton of oil equivalent) to 2405 Mtoe, with an average annual growth of 1.69% and a second period from 1950 to present date, reaching 13276 Mtoe in 2016, with a much higher average annual growth of 2.64% [1], [2].

The world primary energy demand is essentially driven by two key factors: population and GDP (gross domestic product) growths. During the first half of the 20th century, the world population went from 1642 million to 2525 million, with an average annual growth of 0.87%, and from 1950 to present date the average annual growth was 1.65%, culminating in 7349 million inhabitants [3]–[5]. The world GDP shows a similar behaviour, rising from 1.6×10^{12} in 1900, to 5.3×10^{12} in 1950 and 5.4×10^{13} in 2010 (all values in 1990 Int. GK$, international dollar), with an average annual growths of 2.43% and 3.95%, in those two consecutive time periods, respectively [6], [7]. The modest GDP and population growths observed in the first half of the 20th century can be explained by the two World Wars and the economic crisis in the 1930s, which had a global scale influence. After the Second World War, the reconstruction period was characterized by fast economic growth, high consumption of raw materials and primary energy, and from 1945 to 1973 the use of fossil fuels and GDP grew 4.48% and 4.18% yearly, respectively. In the following decades, between 1973 and 2005, the yearly GDP growth was 3.27% GDP and the fossil fuels consumption showed a slower pace growth of 1.63% [7], [8].

Despite the continuously increase in primary energy consumption, the world energy intensity (energy used per unit of GDP) has been decreasing since 1970, from 0.209 to 0.125 toe per thousand $2010 GDP in 2015 with an average annual decrease of -1.2% [2]. This decrease in world energy intensity is mainly due to improvements in productivity, greater energy efficiency, a progressive transition from high energy demanding economic activities to lower ones, and a

change in the fossil fuel mix with the substitution of less efficient fossil fuels like coal by liquid and gas fuels [2], [9].

Fossil fuels (coal, oil and natural gas) still account for 86% of global primary energy demand, nevertheless their share has been slowly decreasing in the last 50 years at an average annual rate of -0.2%. This behaviour was possible due to a slightly increase of hydro share and by the appearance of new primary energy sources like nuclear in the 1970s, and renewables (mostly solar and wind) from 2000 onwards. Currently, the fossil fuel mix is 28%, 33% and 24%, of coal, oil and natural gas, respectively, and the observed past trend of substituting the most carbon intensive fuels by natural gas is expected to continue in the next decades [2], [10]. Compared to renewables, fossil fuels show resource concentration, which increases the risk of long-term energy insecurity and price volatility, making them less resilient to economic and geopolitical disruptive events [11], [12]. Moreover, fossil fuel reserves are finite and considering the actual known reserves and the current annual extraction rate, the reserves to production ratio in 2015 are 114 years for coal, 50.7 years for oil and 52.8 years for natural gas [13].

Regarding final energy, two main sectors account for 74% of total consumption in 2016, industry with 45% and buildings sector (which includes agriculture, commercial, public services and residential buildings) with 29%. The remaining final energy consumption is due to the transport sector, which is heavily dependent on fossil fuels, and non-combusted uses, accounting for 19% and 6%, respectively [2], [14].

Electricity is the final energy product with the highest annual growth record in the past decades, mainly due to a shift in consumer preferences towards a product that is more convenient and easier to use. From 1975 to 2016 world electricity production rose from 6530 TWh to 24816 TWh, at an average annual growth of 3.32%. This behaviour caused an increase of the power sector share in primary energy consumption from 29% to 42% in the same period [2], [14]. The primary energy sources used on worldwide electricity generation are mainly fossil fuels, hydro and nuclear, accounting for 66.3%, 16.0% and 10.6% of share in 2015, respectively [15]. Nevertheless, renewable sources (besides large hydroelectricity plants) have been growing at a high pace during the last decades, due to policy support mechanisms and the development of more mature renewable technologies, making them competitive with conventional sources [16]. In the 2002-2016 period the world electricity production from renewable energy sources grew at an average annual rate of 5.2%, totalling 5877 TWh or a 23.7% share [2], [13], [17].

1.2. Global Warming

In 2010 the total anthropogenic greenhouse gas emissions reached 49 $GtCO_2eq/yr$ (CO_2 equivalent, a metric used to compare the emissions from various greenhouse gases, that converts the amounts of other gases to the equivalent amount of carbon dioxide with the same global warming potential). The main economic sectors responsible for these emissions were the use of non-renewable combustible energy sources for electricity and heat production (25%), agriculture, forestry and other land use (24%), industry (21%) and transports (14%) [18]. Since the beginning of the industrial revolution in 1750, the concentration of greenhouse gases like carbon dioxide, methane and nitrous oxide increased 40%, 150% and 20%, reaching concentrations of 390.5 ppm, 1803 ppm and 324.2 ppm in 2011, respectively [19].

The relation between this great increase of greenhouse gases atmospheric concentration and the warming of the climate system is unequivocal, and since the 1950s, there has been a set of observed changes which are unprecedented over decades to millennia. Global mean surface temperature has increased by 0.72 °C over the period 1951-2012; the upper ocean (above 700 m) have warmed with an increase in energy inventory of 27.4×10^{22} J between 1971 and 2010; the amount of snow and ice have diminished, with a total mass loss from all glaciers in the world of 226 Gt/yr in the period 1971-2009 and a decrease in snow cover extent over the 1967-2012 period with the largest change of -53%, occurring in June; and the sea level has risen by 0.19 m over the period 1901-2010 showing a higher increase rate of 3.2 mm/yr between 1993 and 2010 [19].

Climate change has already caused impacts on natural and human systems worldwide. Hydrological systems are being altered due to changes in precipitation patterns and melting of snow and ice; many terrestrial, freshwater, and marine species have shifted their geographic ranges, seasonal activities, migration patterns and abundances; and human systems are experiencing impacts from increasingly common climate extreme events, like heat waves, droughts, floods, cyclones, and wildfires [20], [21].

Adaptation to climate change, notably of human systems is key to reduce socio-economic impacts [22], especially of those most vulnerable and exposed, which in most cases live in underdeveloped communities and countries. In past years, adaptation to climate change has started to become embedded in national-level planning, and this trend is expected to develop as extreme events become more frequent and society awareness rises [23].

Mitigation efforts and sustainable development policies are also needed to reduce the sources and enhance the sinks of greenhouse gases. Without any additional efforts than those in place up to 2014, baseline scenarios predict a global mean surface temperature increase in 2100 from 3.1 °C to 4.8 °C compared to pre-industrial levels (the range is 2.1 to 7.8 °C when including climate uncertainty), which corresponds to an atmospheric concentration of 720 to >1000 ppm CO_2eq at the end of the current century [24].

The Paris Climate Agreement, adopted on 12 December 2015, is the most recent and unanimous agreement on climate change being signed by 195 nations. Although it recognizes the importance of "holding the increase in the global average temperature to well below 2 °C above pre-industrial levels and pursuing efforts to limit the temperature increase to 1.5 °C above pre-industrial levels", and expresses the desire on "increasing the ability to adapt to the adverse impacts of climate change and foster climate resilience and low greenhouse gas emissions development", it does not set a global cap on CO_2eq atmospheric concentration since the emission targets are not legally binding and will be determined by nations themselves [25]. As for the national plans already presented by the parties, outlining their post-2020 climate action, they constitute an improvement on business as usual scenarios, but still imply a median warming of 2.6 to 3.1 °C by 2100 [26], [27]. Further submissions of national contributions must be increasingly ambitious towards an effective economy decarbonization, especially the implementation of strong mitigation strategies during the 2030-2050 period [28].

1.3. Renewable Energy

The development and implementation of renewable technologies are an important and crucial instrument to decouple the correlation between energy use and growth of greenhouse gas emissions, thus playing a key role on climate change mitigation and sustainable development strategies [29]. Moreover, renewable energy sources can contribute to mitigate other environmental problems like finite resource depletion or ecosystem's pollution, and promote social and economic development, especially in developing countries and poor communities by improving the access to clean, decentralized and secure energy [30], [31].

In 2016 renewable energy sources including hydro, accounted for 10% of world primary energy consumption, adding up to 1330 Mtoe. While hydro is still the most used renewable source, with a 68.5% share, other renewables like wind, solar, geothermal and biomass have recorded the largest combined growth of all energy sources, with an average annual increase of 14% in

the 2000-2016 period [2]. Regarding primary energy consumption by end-use sector, renewables have a share of 20.1% in the power and heat sector, 11.9% in buildings (excluding traditional use of biomass), 11.5% in industry and 3.0% in transports [10].

Renewables have a greater importance in the power sector, providing 5877 TWh or 23.7% of the world's electricity in 2016, with an average annual growth of 4.5% in the 2000-2016 period. Non-hydro renewables already account for 7.5% of the world's electricity in 2016, while in 2000 their share was only 1.4%. These fast flourishing renewables such as wind, solar, biomass and others, with shares of 3.9%, 1.3% and 2.3% in 2016, respectively, had a combined average annual growth of 14.0% in the 2000-2016 period, and contributed for 40% of global power generation growth in 2016 [2], [13].

OECD countries have been the main promoters of renewable power generation, being responsible for 64% of world total in 2016, nevertheless non-OECD had registered a strong increase on renewable capacity during the last decade, exceeding the OECD annual growth rate [13]. This trend will continue, as forecasts until 2022 show global renewables electricity generation reaching 8169 TWh, equal to the total electricity consumption of China, India and Germany combined, thus pushing the worldwide share of renewables in power generation to 30% [17].

During the 2017-2022 period, the growth in renewable generation is expected to be twice as large as that of gas and coal combined, causing the gap with coal to be reduced by half, down to only 17% in 2022. Global renewable electricity capacity may expand by over 920 GW, a 43% increase, being solar photovoltaics (PV) and wind responsible more than 80% of the capacity growth, with 438 GW and 321 GW of additional capacity, respectively. Two main factors are responsible for this increase: China, India and United States are fast-growing markets, accounting for two thirds of global renewable expansion, and countries are gradually moving from feed-in-tariffs set by policy makers, to competitive auctions with long-term power purchase agreements for utility-scale projects, which contribute for significant electricity cost reductions [17].

The expansion of renewable electricity poses both challenges and opportunities in grid management and system integration. In developing countries with less reliable grids, off-grid systems like PV with batteries or local mini-grids built upon renewable electrification programmes can provide until 2022, basic electricity services up to almost 70 million more people in Asia and sub-Saharan Africa [17], [32]. On the other hand, system integration in

developed countries is becoming more important, as renewables share continues to raise. New measures to increase system robustness and flexibility, like demand-side management, storage and higher level of grid interconnections, are essential to allow high shares of renewable electricity and avoid the loss of market value of variable renewables, especially in periods of abundant production but lower demand [33], [34].

In the road transport sector renewables still have a small share, accounting for only 4% in 2016 and expected to marginally grow to 4.5% in 2022. The use of biofuels will remain dominant, representing 93% of total renewable energy consumption in road transport by 2022. Electric vehicles sales will continue to rise, and the electricity consumed by them is forecasted to double by 2022, although it will be less than 1% of total electricity generation [17]. The development and implementation of electric mobility systems is required to achieve sector decarbonization, nevertheless it must be done in close relation with an increase in share of renewable power generation. Higher amounts of renewable electricity will decrease CO_2 footprint of electric vehicles, while vehicle-to-grid technology can provide decentralized grid battery storage, enabling high shares of variable renewables, and increased grid flexibility [35], [36].

1.4. Solar Photovoltaics Market Outlook

The annual influx of solar radiation reaching the Earth is 1083 EWh/yr, but considering cloud coverage and irradiance data, the available value reduces to 175 EWh/yr. The technical potential, which is the maximum energy that theoretically could be converted to useful energy, may vary between 13.9 to 77.8 EWh/yr, depending on different assumptions made to estimate the potential [31], [37]. Nevertheless, even the lower estimate is two to three orders of magnitude greater than other renewables and 90 times the world primary energy consumption in 2016.

The development of the first practical solar cell by Bell Labs in 1954 [38], marked the beginning of solar photovoltaics (PV) era. During its early stage, PV technology was mostly used for space applications like powering satellites and space stations. In the 1970s PV modules started being used in terrestrial applications, especially in off-grid systems for powering remote areas. Later in the mid-1990s, as a response to increasing environmental concerns and willingness to diversify energy sources, on-grid PV markets started to become relevant, nevertheless this market expansion was made possible by the availability of more mature PV technologies and initially driven by political initiatives in the form of support schemes such as feed-in tariffs.

From late 2000s onwards, PV market entered a new exponential growth stage, as medium to large utility-scale PV power plants become increasingly common. Economies of scale on the production side, arising from the development of MW and most recently GW capacity solar cell and module assembly factories, have plunged down PV modules costs, which led to a decrease of the PV levelized cost of electricity. Therefore, grid-parity is achieved in most countries in the world, during the 2015-2020 period [39].

Worldwide installed capacity of solar photovoltaics has grown greatly over the last decade, at an average annual growth of 47.1% and reaching a 13.7% share in 2016, just behind hydro and wind with 58.5% and 21.9% shares, respectively. Figure 1.1 shows the cumulative installed capacity over the 2005-2016 period, detailed by geographic region [40].

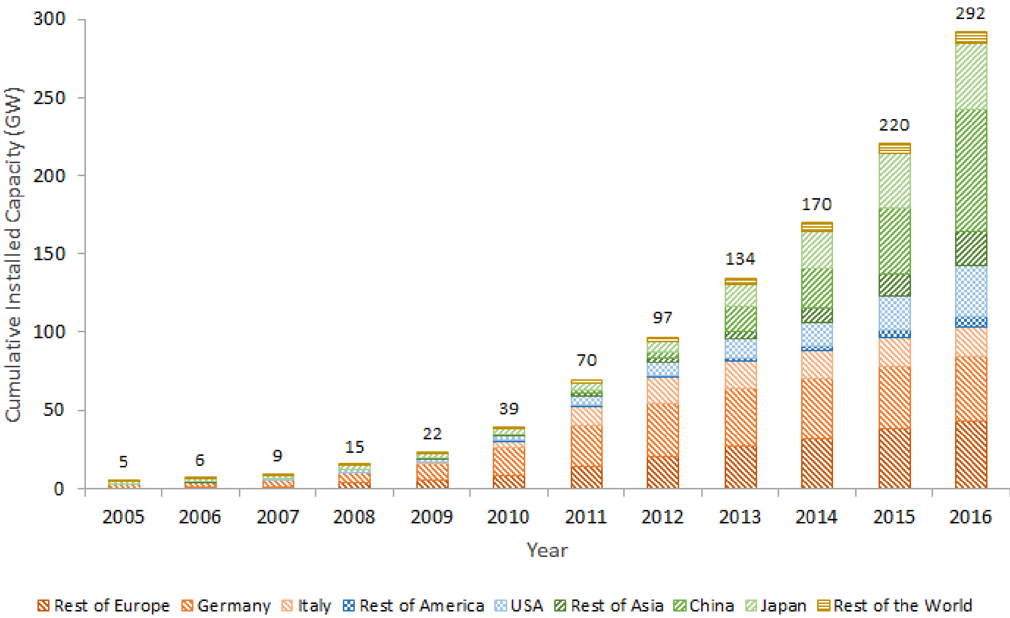


Figure 1.1 - Cumulative capacity (in GW) of solar photovoltaics by region, over the 2005-2016 period.

Until 2015, Europe was in the lead with 97.0 GW of cumulative installed capacity (headed by Germany with 39.2 GW and Italy with 18.9 GW), followed by Asia (90.7 GW) and America (26.3 GW). European PV market began flourishing in 2008 driven by political will in the form of legislation and roadmaps elaborated by the European Commission and Parliament [41]–[45], which established a 20% target of renewable energy sources on the total energy production in 2020, and by economic and fiscal incentives such as feed in tariffs [46]–[49].

In 2016, Europe had 102.3 GW of cumulative installed capacity, but in the same year and for the first time, it was overcome by Asia that reached 141.8 GW, mainly due to China almost doubling its installed capacity during 2016. This growth is due to support policies in the form

of feed-in tariffs, that started being implemented after 2011 in China [50] and after 2012 in Japan [51], thus contributing for domestic photovoltaic market expansion during the following years. Moreover, the development of China's PV industry, fuelled by technology transfer from the European industry and investment on new MW-scale factories, which already had 60% of global PV module production in 2011, was also a key driver for the growth of domestic installed capacity [52], [53].

PV electricity generated has grown exponentially over the 2005-2016 period, in line with the cumulative installed capacity growth. From only 3.8 TWh in 2005, worldwide PV electricity reached 317.7 TWh (or 5.4% share of all renewable electricity) in 2016, increasing at an average annual growth of 50.5%. Germany has been the world leader in PV electricity generation (around 38 TWh in 2015 and 2016), until it was surpassed by China in 2015 (39 TWh and 68 TWh in 2016) and both USA and Japan in 2016 (with 47 TWh and 51 TWh, respectively) [40].

1.5. Solar Photovoltaics Technology Outlook

World's PV market is dominated by crystalline silicon technology [54], [55], with a 94.2% share or 73.5 GWp of worldwide PV module production in 2016, and the remaining market share of 5.8% or 4.5 GWp is comprised of thin-films, particularly cadmium telluride (CdTe), amorphous silicon (a-Si) and copper indium gallium diselenide ($Cu(In,Ga)(Se,S)_2$ or CIGS) [56], [57]. Figure 1.2 presents the total annual PV module production (in GWp) and the share by technology (in %), over the 2005-2016 period [58].

In just over a decade, PV module production went from 1.5 GWp in 2005 to 78.1 GWp in 2016, at an average annual growth of 46.4%. During the same time period, crystalline silicon registered an annual average market share of 90.1%, being multicrystalline silicon the most used technology with an average market share of 60.7%, nevertheless, monocrystalline silicon had the highest share since the beginning of PV market diffusion and was only surpassed by multicrystalline silicon in 2000. Thin-films have a marginal weight with an annual average market share of 9.9%.

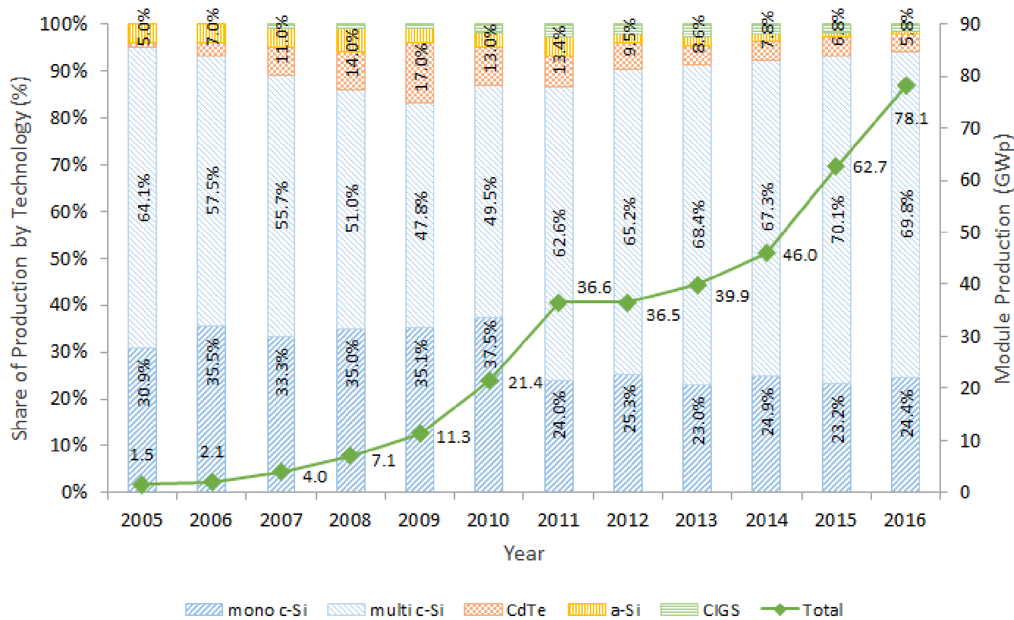


Figure 1.2 - PV module production (in GWp) and share by technology (in %), over the 2005-2016 period.

The assessment and comparison of different technologies is essential to understand the PV market behaviour or to draw forecasts, and it can be achieved using some key parameters, such as: module price, final conversion efficiency, raw materials availability and scaling (or growth) potential.

PV module price has continuously decreased over time, falling from 23.67 $€_{2016}$/Wp in 1980 to 3.074 $€_{2016}$/Wp in 2005 and reaching the lowest value of 0.438 $€_{2016}$/Wp during 2016 (all past prices converted to 2016 prices accordingly to inflation per watt-peak of module power), while cumulative production has increased from just 8.2 MWp in 1980 to 341 GWp in 2016. This relation, known as learning (or experience) curve, is presented in Figure 1.3 [58]. A linear fit of the data over the 1980-2016 period returns a learning rate of 24%, which was the amount of module price decrease every time the cumulated production doubled, evidencing cost reductions from economies of scale and technological improvements at the production level.

Although the module price data shown in Figure 1.3 includes all commercially available PV technologies, the graph is a good indicator for crystalline silicon module price evolution, since it is the dominant market technology. It is clearly visible the mid-2000s demand increase for PV modules, which led to a silicon feedstock shortage, causing module prices to rise and temporarily halted its historical decreasing trend [59]. The PV manufacturing industry recovered from this shortage period through research and development (R&D) to improve material utilization, either by increasing silicon material yield (such as kerf loss recycling [60],

diamond-wire sawing [61], [62] and more cost-effective ways to produce solar grade silicon [63], [64]) or by increasing solar cell conversion efficiency [65]. Moreover, new investments were made in expanding silicon feedstock production capacity as well as in new MW size silicon solar cell and module assembly factories [66].

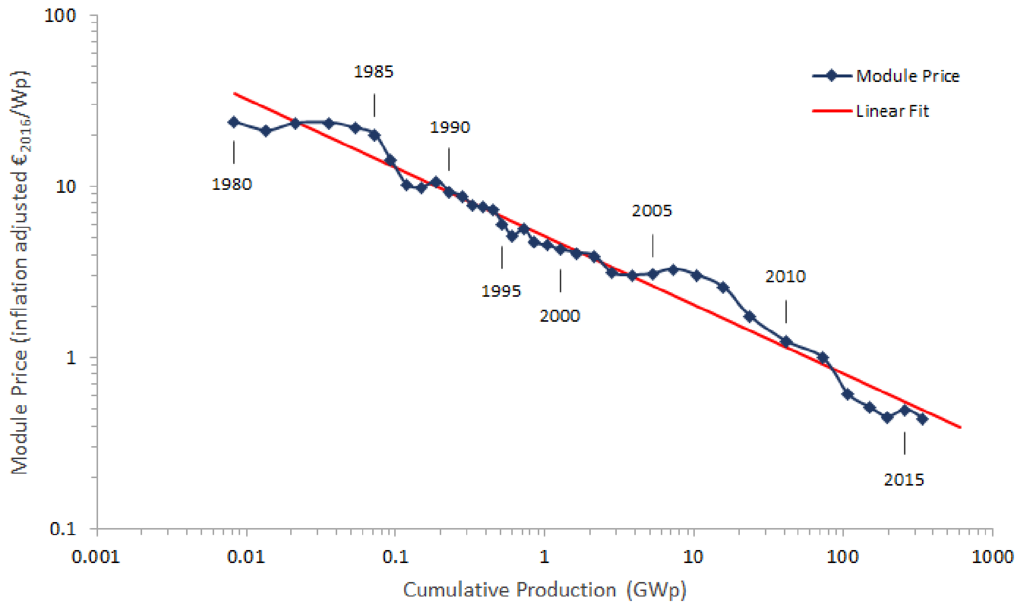


Figure 1.3 - PV module price (in $€_{2016}$/Wp) as a function of the cumulative production (in GWp), encompassing all commercially available PV technologies, over the 1980-2016 period.

Thin-film technologies flourished during the silicon feedstock shortage, as new investments on R&D and expansion of industry production capacities resulted in the reduction of manufacturing costs [59], [67], with a market share peak of 17.0% in 2009, as shown in Figure 1.2. Hence, thin-film module average price was lower than crystalline silicon modules during the 2006-2012 period, dropping from 3.381 $€_{2016}$/Wp to 0.642 $€_{2016}$/Wp, while crystalline silicon modules price went from 4.276 $€_{2016}$/Wp to 0.693 $€_{2016}$/Wp. In the 2013-2014 period module prices continued to decrease as both technologies attained roughly the same prices within the 0.48-0.57 $€_{2016}$/Wp range, although slightly lower for thin-film modules, but from 2015 onwards crystalline silicon modules become cheaper as they reached 0.500 $€_{2016}$/Wp and further decreasing to 0.439 $€_{2016}$/Wp in 2016 [58].

Energy conversion efficiency of PV systems is a vital driving force in reducing costs. For the same output power, a PV system with higher module efficiency will be smaller and the balance of system (BOS) costs will be lower, thus reducing the levelized cost of electricity during the system’s lifetime. Moreover, in environments where space is a constraint, such as urban areas, a higher energy generation per unit area is advantageous.

Crystalline silicon is a mature technology with over 60 years of R&D, so efficiency improvements in recent years were small and gradual, ranging from 0.04 to 0.09%/yr. Record efficiencies reached, as of 2017, 24.4% and 19.9% for mono and multicrystalline silicon modules, respectively. From all commercially available thin-films technologies, polycrystalline compounds have made considerable efficiency improvements over the past few years: 0.9%/yr for CdTe and 0.2%/yr for CIGS, attaining module efficiency records of 18.6% and 19.2% as of 2017, respectively. Contrarily, a-Si technology still has low efficiency (module record of 10.2%), requiring more R&D on reducing recombination losses and improving light management. Other technologies are either deployed at a small scale with PV modules already manufactured and field-tested, like gallium arsenide (GaAs) (24.8%), dye-sensitized (8.8%) and organic (9.7%) or under development at a solar cell level such as indium phosphide (InP) (24.2%), gallium indium phosphide (GaInP) (21.4%), Perovskite (19.7%) and copper zinc tin sulfide (CZTS) (10.0%) [68], [69].

The comparison of various PV technologies can also be done by assessing the raw material availability, since it is an important parameter for evaluating the scalability potential. Silicon, in the form of silicon dioxide (SiO_2), is the most abundant mineral on the Earth's crust, and considering the current industrial status and expected trends, crystalline silicon technologies will remain dominant in the manufacture of PV modules over the coming decades, as solar grade silicon should be available at an affordable cost, while meeting the expected demand growth of the PV market [70].

Thin-film technologies were seen during the mid-2000s silicon feedstock shortage, as a promising alternative path to crystalline silicon, with some studies predicting a 25% market share in 2010 [71]. Nevertheless, to become a strong player in the PV market during the following years, thin-films had to attain several objectives, such as: improve conversion efficiency, be durable and based on non-toxic and abundant materials [72]. Commercially available thin-film technologies, like CdTe and CIGS modules, despite having achieved higher efficiency, long-term durability and field reliability are based on metals which are obtained as by-products of other metals' production and are either toxic (Cd and As) or rare (Cd, Ga, In, Se and Te). The continuous fast-paced growth of installed PV capacity, outlined by several projections up to 2030, will require a considerable increase in the supply of some metals, to match PV industry demand. Assuming a scenario with 8% of worldwide electricity in 2030 produced by PV and if most of the capacity additions are made of CdTe and CIGS modules, the needed annual production levels for In, Se, and Te will exceed the projected potential levels

by a large margin and would require unprecedented annual growth rates. Moreover, in such scenario, by 2030 the annual Te production would exceed its known reserves and the annual In production would approach the estimated reserves, undermining the scalability potential for CdTe and CIGS thin-films [73], [74]. Other factors like geographic distribution, political stability or sudden changes in typical supply and demand patterns, also influence the scaling up of thin-film technologies with greater impact than on crystalline silicon technologies [75].

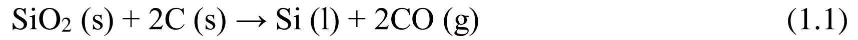
As a result of increasing maturity of PV module technologies, the relative cost of modules in PV systems has been decreasing over the last decade, while the costs of BOS components (inverters, mounting structures, wiring and all non-module components) and the soft costs (install labour, land acquisition, taxes, net profit and other non-hardware items), became more relevant. In 2010 the module costs accounted on average for 35% in residential, 47% in commercial and 53% in utility-scale PV systems, while in 2016 those ratios decreased to 21%, 30% and 45%, respectively. Significant improvements in systems integration and on-site assembly are required especially in residential and commercial PV systems, where soft costs (58% and 49% in 2016, respectively) tend to be higher [76].

The future of PV looks promising, with continuous R&D in new concepts and in the improvement of available technologies, but also a considerable worldwide growth of PV systems deployment is expected by several energy scenarios. Global PV electricity could represent between 7.0% and 15.4% (2.4 to 5.1 GWh) in 2030, 8.1% and 28.0% (3.1 to 13.5 GWh) in 2040 and up to 36.4% (23.8 GWh) in 2050 of total electricity generation, depending on the scenario's assumptions. Nevertheless, even in the most conservative scenarios, PV has one of the highest annual growth of all renewable sources [77]–[80].

1.6. Solar Grade Silicon Feedstock

Silicon (Si) is the second element of the group IV in the periodic table, never occurring free in nature but rather in combination with oxygen, forming oxides and silicate minerals (silicon and oxygen together with calcium, aluminium, iron or other metals). The Earth's crust is mostly composed of silica (SiO_2) and various silicate minerals, with silicon being the second most abundant element, just after oxygen, with around 28% in crust's weight.

The first stage for producing purer silicon, consists in the carbothermic reduction of silica (oxygen is removed), according to the reaction:



$$SiO_2 (s) + 2C (s) \rightarrow Si (l) + 2CO (g) \qquad (1.1)$$

Metallurgical grade silicon (MG-Si) or silicon metal with a minimum of 96% and typical purity of 98.5%, is obtained in submerged electric arc furnaces, where a mixture of silica in the form of quartz and carbon raw materials such as metallurgical grade coal or charcoal, is heated at a temperature in the range of 1800 to 2100 °C, by means of an intense electric arc between carbon electrodes and the bottom of the furnace. The liquid silicon is tapped in large ladles and further refining can be done by adding sand silica to form oxides compounds with metals like aluminium, calcium or manganese, with the slag containing most of the impurities being mechanically removed or by gravity. After being put on cast-iron moulds to solidify, the multicrystalline MG-Si with grain size typically from 1 mm (near the iron mould wall) to more than 100 mm, is crushed into small lumps up to 100 mm. The entire process is highly energy and material demanding, with best industrial plants having a specific energy consumption of 10-11 MWh/t of silicon metal produced and a 90% silicon yield. MG-Si is not suitable to be used in PV applications, since the concentration of some contaminants like carbon, oxygen, boron, phosphorus and metals such as iron, aluminium or calcium is still high, between 1 to 10^4 ppm(w) [81].

Silicon of photovoltaic and electronic grade, also called polycrystalline silicon or polysilicon, is an ultra-high purity material with lower concentration of impurities (in the ppb(a) to ppt(a) range), used in the PV and semiconductor industry. Besides the existence of two distinct industrial processes, each with several chemical variants and optimization pathways, the production of polysilicon is based on four fundamental steps: the synthesis of a volatile silicon hydride, its purification followed by the decomposition to elemental silicon and finally the recycling of by-products.

The dominant process, with approximately 90% of global polysilicon output, is the Siemens process in which trichlorosilane/TCS ($SiHCl_3$) is obtained from MG-Si, purified through several distillation and condensation steps and decomposed in U-shaped polysilicon rods in a thermal chemical vapour deposition inside a metal bell jar Siemens reactor, as shown in Figure 1.4(a).

Two processes are used to produce TCS: (i) low pressure (1-5 bars) and temperature (300 °C) hydrochlorination of MG-Si:

$$Si\ (s) + 3HCl \rightarrow SiHCl_3 + H_2 \quad (1.2)$$

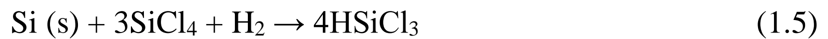
also producing silicon tetrachloride/STC, according to the competing reaction:

$$Si\ (s) + 4HCl \rightarrow SiCl_4 + 2H_2 \quad (1.3)$$

which is recycled to TCS by thermal hydrogenation at 1300 °C:

$$SiCl_4 + H_2 \rightarrow SiHCl_3 + HCl \quad (1.4)$$

and (ii) high pressure (20-25 bars) and temperature (500 °C) hydrochlorination of MG-Si and silicon tetrachloride/STC ($SiCl_4$) in one reaction:



$$Si\ (s) + 3SiCl_4 + H_2 \rightarrow 4HSiCl_3 \quad (1.5)$$

Inside the Siemens reactor, high purity TCS is decomposed in Si on the surface of electric heated (1100 °C) seed rods, according to the following main reactions:

$$2SiHCl_3 \rightarrow SiH_2Cl_2 + SiCl_4 \quad (1.6)$$

$$SiH_2Cl_2 \rightarrow Si + 2HCl \quad (1.7)$$

$$SiHCl_3 + H_2 \rightarrow Si + 3HCl \quad (1.8)$$

$$SiHCl_3 + HCl \rightarrow SiCl_4 + H_2 \quad (1.9)$$

The Siemens process has a couple of main disadvantages, such as: high energy consumption (over 90% of the input energy is lost to the cold walls of the reactor), electrical contacts of the seed rods are made of graphite, being a contamination source, and there is a large quantity of by-products (mainly HCl, H_2 and several chlorosilanes), which need to be recycled or put back in the overall closed-loop process. Recent reactors with up to 48 seed rods and the best optimization strategies lead to an annual production of 450-600 t, consuming less than 50 kWh/kg, and deliver polysilicon cylindrical rods measuring up to 2.5 m in length and 150 mm in diameter [70].

An alternative process uses silane (SiH_4) in a fluidized bed reactor (FBR), presented in Figure 1.4(b), where fine silicon particle seeds are continuously loaded from the top, while silane and hydrogen enter near the bottom of the reactor, as nearly all the silane feed can be converted to polysilicon granules with hydrogen being the only by-product:

$$SiH_4 \rightarrow Si\ (s) + 2H_2 \tag{1.10}$$

The ascending gas mixture passes through the silicon beds, which behave like a fluid as the gas stream equals their gravity, favouring a uniform chemical vapour deposition. This process has several advantages when compared to a Siemens reactor: the conversion efficiency is higher, no corrosive compounds are formed, the 0.5 to 2 mm polysilicon granules are ready to use (crushing is not required, avoiding possible contamination), it can be operated on a continuous cycle of 60-120 days, and the energy consumption during decomposition is reduced by 80% because the silane pyrolysis occurs at a lower temperature of around 800 °C. Modern FBRs are able to annually produce 1000 t of polysilicon with an energy consumption of only 5-10 kWh/kg [70]. The main disadvantages are the generation of fines and powders in the reactor's free space due to homogeneous decomposition of silane and the deposition of silicon on the reactor walls, contributing to lower silicon yield and product contamination (impurities concentration can be up to one order of magnitude higher than the Siemens process).

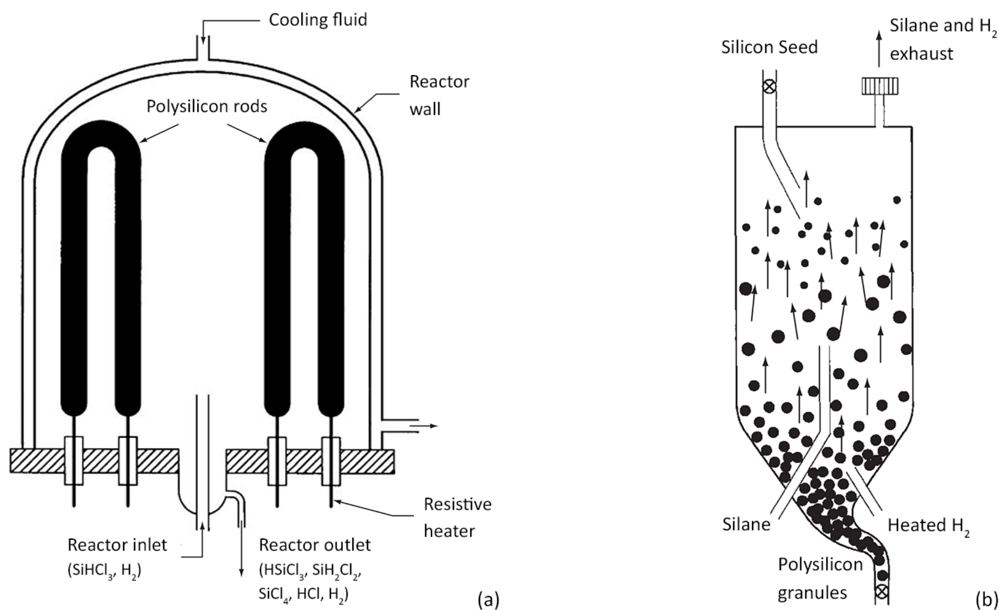


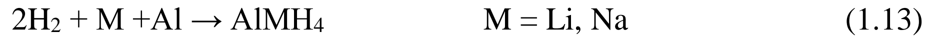
Figure 1.4 - Polysilicon production processes [81]: (a) schematic of a Siemens reactor; and (b) schematic of fluidized bed reactor.

The silane is obtained from two distinct processes: (i) redistribution of purified trichlorosilane through two catalytic columns, using quaternary ammonium ion exchange resins as catalyst, according to the reactions:

$$2SiHCl_3 \rightarrow SiH_2Cl_2 + SiCl_4 \tag{1.11}$$

$$3SiH_2Cl_2 \rightarrow SiH_4 + 2SiHCl_3 \quad (1.12)$$

with the products being separated by distillation after each catalytic column; and (ii) hydrogenation of silicon tetrafluoride (SiF_4) using metal hydrides like lithium-aluminium or sodium-aluminium:



$$2H_2 + M + Al \rightarrow AlMH_4 \qquad M = Li, Na \quad (1.13)$$

$$SiF_4 + AlMH_4 \rightarrow SiH_4 + AlMF_4 \quad (1.14)$$

with SiF_4 coming either from the fluorination of natural silica or from the sublimation of natural alkaline fluorosilicates (M_2SiF_6, M is an alkaline element), that are a by-product waste of the fertiliser industry, being largely available at a low cost.

A third way to produce solar grade silicon, named upgraded metallurgical grade silicon (UMG), gained visibility during the mid-2000s silicon feedstock shortage, with multiple R&D projects and companies building pilot plants to further refine and purify MG-Si, bypassing the synthesis of a volatile silicon hydride [82]. Despite begin a promising alternative, with lower costs and reduced energy consumption, the obtained silicon had a high content of impurities, especially phosphorous and boron dopants, therefore, most of the UMG projects are currently halted and a fully commercial phase was never accomplished [70].

1.7. Crystalline Silicon Ingots

The highest efficiency silicon solar cells are made from monocrystalline silicon ingots, which can be obtained by two techniques: Czochralski (Cz) and floating zone (FZ). The Cz process consists in the growth of a cylindrical-shape single crystal pulled directly from molten silicon, as shown in Figure 1.5(a), representing a typical industrial set-up of a Cz puller.

Inside a vacuum-proof cylindrical chamber with water-cooled steel walls, polycrystalline silicon chunks are put into a bowl-shaped silica crucible surrounded by a susceptor graphite shell to stabilize the crucible walls at higher temperatures. The silicon is then melted with the help of lateral and bottom graphite heaters and maintained at a temperature range slightly above the melting point (1413 °C), in an argon inert gas atmosphere with a pressure range of 20 to 500 mbar. The crucible, apart from the polysilicon, is a major source of impurities since it is in direct contact with the silicon melt. Silicon monoxide (SiO) from the crucible is dissolved into the melt, causing oxygen contamination, nevertheless it is possible to keep the oxygen

concentration bellow the solubility limit, avoiding the formation of SiO_2 precipitates. As the dissolved oxygen reaches the free melt surface, transported by convention flows, the high vapour pressure of the SiO and a downward argon flow towards the melt, favours the strong evaporation of SiO, with nearly 99% of the oxygen being removed out of the melt [83].

After the stabilization of the melt temperature a monocrystalline silicon seed, mounted on a movable seed holder (typically made from molybdenum), is brought close to the melt surface for preheating and then dipped into the melt, while keeping a seed rotation of 10-20 rpm and a crucible counterrotation of 0.5-20 rpm. A small portion of the seed is melted, forming a melt-seed interface where the growth of a new crystal with the same orientation of the seed (usually <100>) is started by adding Si melt atoms to the seed interface. As the seed is pulled out of the melt, dislocations are formed due to thermal stress, nevertheless their propagation is halted by applying the Dash procedure: the growing of a long thin neck (with a constant 2-4 mm diameter) at a high pulling speed up to 6 mm/min, causing the dislocation lines to end at the surface of the neck and resulting in a dislocation-free neck just after a grown length of around 30 mm [84], [85]. Then, the pulling speed is reduced to gradually increase the crystal's diameter, turning into a conical shape called the crystal shoulder or the seed cone. When the desired value for the cylindrical body is reached (usually within the 100-450 mm range), a sudden and short duration increase of the pulling speed occurs, starting the growth stage of the crystal body, during which the diameter is maintained constant by monitoring the meniscus shape at the triple point of the melt-crystal interface and feedback that information to pull, rotation and heat controls systems [86]. Finally, with most of the melt consumed, the crystal diameter is gradually decreased until is small enough to be detached from the melt without dislocation formation in the crystal body, following a cooling stage and removal of the grown crystal that can measure up to 2 m in length.

The Cz process is a mature and cost-effective technology, with several advantages: (i) it is a semi-automated process where one operator can simultaneously control several pullers; (ii) feedstock material can have a variety of different shapes, purity grades and doping levels; (iii) it is a quality control step as it delivers dislocation-free monocrystalline ingots with the same crystal orientation of the seed, which in solar cell processing a <100> orientation allows for an economical surface texture by wet chemical etching [87]; and (iv) the feedstock is purified during the growth process since most metals have a segregation coefficient, the ratio of an impurity concentration in the solid phase to that in the liquid phase, much lower than 1 (in the range of 10^{-4} to 10^{-6}), so impurity atoms will diffuse to the liquid region of the melt-crystal interface, being continuously segregated to the remaining silicon melt [85].

The FZ Si growth is a contactless vertical zone melting technique [88], [89] developed to overcome the main disadvantage of Cz growth: the direct contact of the melted silicon with the crucible, since the quartz walls erode at high temperatures with a rate of 10-40 µm/h [90], releasing oxygen into the melt and forming SiO_2 precipitates. The FZ process does not require a crucible as observed in Figure 1.5(b), depicting a typical industrial set-up of a FZ puller.

Inside a vacuum-tight vessel, a polysilicon feed rod is mounted on a pulling shaft, while at the bottom shaft a silicon seed crystal is secured, with both shafts capable of independently vertically translate and rotate. The key component that delivers heat for melting the silicon and determines the yield and success of the growth process, is a flat, ring-shaped and one-turn induction coil connected to a radiofrequency (RF) power generator and to a water-cooling system. The growth process, occurring in an argon inert gas atmosphere, starts with the preheating of the polysilicon feed rod bottom and as the temperature rises above 450 °C, the increase of silicon's electric conductivity facilitates the inductive heat by the magnetic field of the coil, until it reaches the melting point (1413 °C). The seed crystal is then moved upward, through the circular opening of the coil, close to the melt drop suspended by adhesion and surface tension, where after heating is dipped into the melt. When a stable melt-seed interface is attained, the seed is moved downwards out of the melt at a high pulling speed of 8-16 mm/min, following the same Dash procedure originally developed for Cz Si growth, of growing a thin and long crystal neck to cease the propagation of dislocations [84], [91]. Having a dislocation-free crystal neck, its diameter is increased by gradually raising the inductor current and the feed rate, resulting in a greater melt flow as the crystal gets a conical shape. When the desired diameter is reached, the pulling speed is lowered to 2-5 mm/min, starting the cylindrical crystal growth stage with the impurities of the feed rod being continuously segregated to the molten zone and away from the solidifying crystal. Finally, as the molten zone travelling upwards approaches the end of the feed rod, the inductor current is lowered, and the shrinking molten zone divides due to the downward pulling of the silicon crystal.

The FZ Si growth is possible because of silicon's high surface tension and low density, leading to a waist-shaped molten zone with a narrow (around 20 mm in diameter) but high enough melt neck (up to 17 mm), capable of going through the inductor hole without contacting with it. This needle-eye technique allows the growth of large crystals, up to a maximum diameter of 200 mm, that could be greater than the polysilicon feed rod, since the final crystal diameter is almost independent of the molten zone dimensions [92]. Compared to Cz Si growth the FZ technique delivers purer monocrystalline silicon ingots with typical impurity concentrations

two to three orders of magnitude lower, being suitable for high power electronics, as well as for applications requiring high purity silicon such as the seed rods used by the Siemens process. Currently, the global production of monocrystalline silicon by FZ, although continuously rising over the last decades, represents roughly 5% of the market [91].

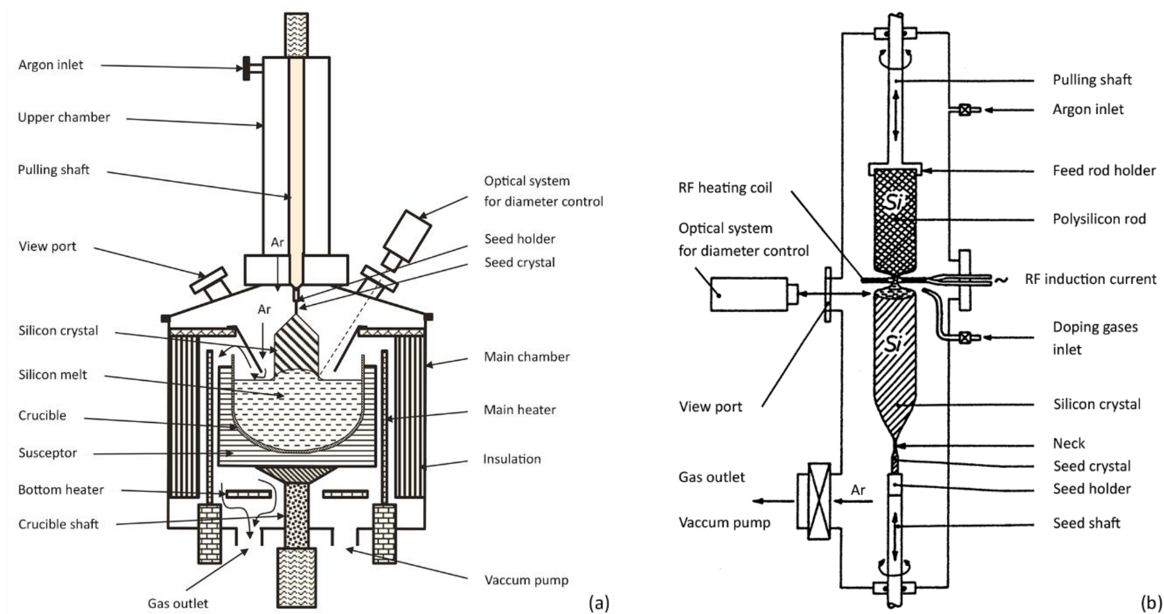


Figure 1.5 - Monocrystalline silicon ingot growth: (a) schematic of a Czochralski puller [85]; and (b) schematic of a floating zone puller [93].

Multicrystalline silicon, despite delivering solar cells with slightly lower efficiency, offers several advantages over monocrystalline silicon, such as: lower manufacturing costs, higher production throughput, greater feedstock tolerance and better utilization of the PV module area since monocrystalline solar cells are square-shaped but with truncated corners. There are two main manufacturing techniques for producing multicrystalline silicon ingots with weights up to 450 kg or measuring up to 90×90×30 cm^3: directional solidification (DS) and block-casting [87], [94].

The DS process, shown in Figure 1.6, uses a quartz crucible coated with silicon nitride (Si_3N_4) acting as a non-sticking layer, which is loaded with polysilicon and doping material, placed inside a graphite case and then covered with a graphite plate. The furnace containing the crucible is closed, vacuumed and maintained in an argon inert gas atmosphere during the entire process. A crystal growth cycle begins with the rapid increase of the temperature, using top and side induction heaters, until complete melt and stabilization is achieved, followed by a slightly decrease of the heating power and the upward movement of the side insulation basket to initiate the growth from the bottom of the crucible, at a controlled crystal growth rate of 1-2 cm/h.

When complete solidification of the ingot is achieved, the insulation is lowered for annealing and relaxation of thermal stress and dislocations, causing the whole ingot to reach a uniform temperature and as the temperature is below 800 °C the insulation is moved up again for faster cooling. The whole growth process can take up to 60-70 h of which 10-20 h for melting, 30-40 h for crystal growth and the remaining for annealing and cooling [94], [95].The main difference of the block-casting process is the use of two crucibles, one for melting the silicon and a second crucible with a Si_3N_4 coating for the crystallization step, and just like in the DS process, the silicon is directionally solidified starting from the crucible bottom [94].

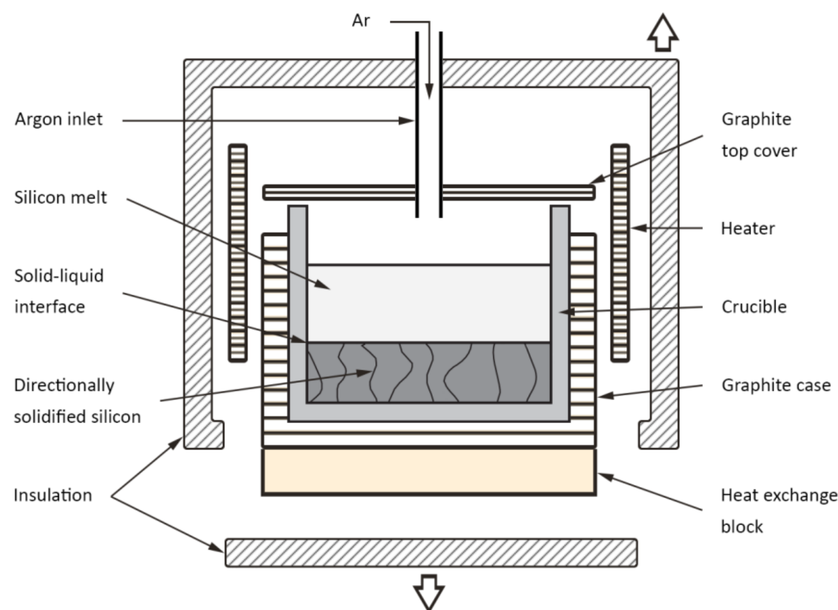


Figure 1.6 - Multicrystalline silicon ingot growth: schematic of a directional solidification furnace [87], [94].

The multicrystalline silicon ingots have a columnar crystal growth due to the upward movement of the liquid-solid interface, and segregation during the crystallization stage causes impurity concentrations to vary along the ingot height, with the highest values at the top. The bottom of the ingot, having a longer contact with the crucible, and the side walls are also contaminated by solid state diffusion [96], so top, side and bottom volumes up to an ingot depth of around 3 cm (also called red zones) are not used for solar cell manufacture.

Impurity concentrations are much higher than in monocrystalline silicon ingots, arising out of several sources: carbon from the graphite parts inside the furnace, nitrogen and oxygen from the Si_3N_4 coating and the silica crucible, and metals, such as aluminium, iron, copper, calcium and others, coming mainly from the crucible and coating materials, as well as from the solar grade polysilicon used as feedstock. Their presence in the silicon melt is responsible for metal point defects, precipitates (if supersaturation occurs), microdefects and inclusions formations

especially near the ingot borders [97], although the extent of impurities can be minimized and managed during crystallization applying various strategies: (i) using higher quality crucibles and purer Si_3N_4 coatings to reduce metal contamination [98], [99]; (ii) controlling both growth rate (that influences the shape of the liquid-solid interface) and melt convection, to reduce carbon and nitrogen accumulation at the interface and consequently their precipitates (SiC and Si_3N_4) [100], [101]; and (iii) using an argon gas flow above the melt to facilitate SiO evaporation and a crucible cover to reduce carbon incorporation into the melt [102], [103].

Grain boundaries and dislocations are the most common crystal defects of multicrystalline silicon, and their concentration and electrical activity greatly influence solar cell efficiency. Regarding grain boundaries and size, the average grain size increases with the ingot's height, but the overall dimension is mainly dependent on the crystallization speed, with lower speeds resulting in larger grains throughout the ingot. Modern manufacturing techniques can produce silicon ingots with grains large enough not to degrade solar cell efficiencies. Dislocations are formed and propagated during crystallization and cooling stages due to thermal stress caused by temperature inhomogeneities, thus controlling these temperature variations is essential to reduce the dislocation formation and improve crystal quality. High dislocation density as well as grain boundaries and dislocations both electrically charged, have a negative impact on solar cell efficiency since they attract minority charge carriers, being highly active recombination centres of photo-generated charge carriers. The electrical activity of grain boundaries and dislocations depends on their impurity decoration, especially by transition metals, and increases with higher impurity concentrations. This effect is amplified by the fact of crystal defects being the locations where metals tend to accumulate and found with the highest concentrations, leaving few active metals in the intragrains [104]–[106].

1.8. Wafering

Mono and multicrystalline silicon ingots must be cut into wafers for solar cell production, using multi-wire slicing technology. A single wire, fed from a supply spool, passes through a pulley and tension control unit and is led into four wires guides with parallel grooves of constant pitch, forming a wire net of multiple strands [107]. This configuration allows for a high throughput with almost no restrictions on the size of the silicon ingots to be cut into 10×10 or 15×15 cm^2 wafers with a minimum thickness of 150-180 μm. The cut is accomplished by an abrasive slurry, usually silicon carbide, supplied through nozzles over the wire, followed by its recycling

which can reach up to 80%. Despite being the dominant method over the last decades, slurry-based wafering is being replaced by diamond wire sawing technology, which in 2017 already accounted for approximately 79% and 28% of mono and multicrystalline silicon wafers cut, respectively. The main disadvantage of multi-wire slicing technology is the kerf losses, which currently is about 125 μm per wafer for slurry-based methods and 90 μm for diamond wire-based sawing [108].

1.9. Crystalline Silicon Ribbons

The established methods of producing crystalline silicon wafers for solar cell manufacture, based on Cz growth or directional solidification, followed by wafering using multi wire sawing, account for around one third of PV module cost [109]. Silicon ribbon and foil technologies, which R&D have been under way for more than four decades, are an alternative pathway with potential for reducing costs, as silicon ribbons can be grown directly from the silicon melt, bypassing the wafering step. During the mid-1970s oil crisis, the need for low-cost substrates that could be used in solar cell manufacture, incited the first large scale efforts in R&D, taking place in United States under the Flat Plate Array Project conducted by the Jet Propulsion Laboratory (JPL) between 1975 and 1985 [110]. The know-how acquired in this project and further worldwide investments, set the early seeds of crystalline silicon ribbon and foil production methods, developed and improved in the subsequent years, reaching more than a dozen different techniques [111].

The process studied in this thesis is a ribbon technology, aiming to produce multicrystalline silicon ribbons directly from gaseous feedstock, therefore the most relevant ribbon technologies will be briefly discussed. Ribbon technologies can be divided into two main groups, vertical and horizontal growth methods, regarding the relation between growth and pulling directions. In vertical ribbon growth, the pulling direction is perpendicular to the liquid-solid interface, thus, the pull and interface growth speeds have the same direction and equal order of magnitude. The crystal growth is columnar, similar to directional solidification with elongated and wide grains, nevertheless crystalline quality is highly dependent on the pulling speed, as very high dislocation densities, due to thermal stress, will be formed if growth rate exceeds several centimetres per minute [112]. In horizontal ribbon growth, pulling and interface growth speeds (v_p and v_i, respectively) are related by the equation:

$$v_p = \frac{v_i}{\cos\theta} \quad (1.15)$$

where θ is the angle between the substrate and the growth interface. A very small angle during ribbon growth results in high growth rates, as v_i approaches v_p. This can be achieved by controlling the temperature gradient with heat being predominantly transferred to the supporting substrate, instead of flowing to the already crystallized ribbon, and by creating a large interface crystallization area. Consequently, in horizontal ribbon growth, new grains are repeatedly created by nucleation starting on the substrate's surface and growing nearly perpendicular to the substrate pulling direction, resulting in grain lengths of the order of the film thickness [113]. This large crystallization area, characteristic of horizontal growth methods, allows a very efficient extraction of the latent heat during ribbon growth, therefore, pulling speeds three to four orders of magnitude higher than in vertical growth are achievable [114], [115].

The most relevant and developed ribbon technologies are: (i) in vertical growth, dendritic web (WEB), string ribbon (STR) and edge-defined film-fed (EFG); and (ii) in horizontal growth, ribbon growth on substrate (RGS) and Silicon Film™ (SF). Their schematics (except for SF) are presented in Figure 1.7.

In WEB process, the ribbon is grown directly from melted silicon inside a crucible, without using any shaping device, as show in Figure 1.7(a) [87], [116]. A wire-like dendrite seed is lowered into the melt surface, and melt temperature is adjusted so the seed neither melts nor freezes. Then, by lowering the melt temperature several degrees so that the melted silicon in the vicinity of the seed becomes supercooled, the seed grows laterally, forming a button at the melt surface. When the seed is pulled upwards, two needle-like dendrites propagate from the ends of the button into the melt surface, forming a frame that supports the growing multicrystalline ribbon. As the ribbon grows, it gradually widens until reaching a steady state width determined by the thermal conditions in the melt, therefore, a very accurate control of melt temperature, within a few tenths of a degree, is needed for maintaining a supercooled interface, to ensure ribbon thickness, width uniformity and to prevent ribbon pull-out by voiding of the meniscus at the liquid-solid interface [116]. The growth rate is limited by the rate of latent heat removal into the ribbon and conducted through the meniscus to the melt, thus, to minimize stresses generated from the temperature profile which the ribbon is subjected after growth, typical pull speeds are in the 1-2 cm/min range. WEB ribbons have a thickness range from 75 to 150 μm, with widths up to 8 cm and can be grown up to 17 m in length with

continuous replenishment of the crucible. Solar cells made with WEB ribbons achieved a record efficiency of 17.2% with average cell efficiency of 14.0% [112], [117].

In STR technique, formerly known as edge stabilized ribbon (ESR), the ribbon is grown directly from the silicon melt. The process is geometrically similar to WEB, but instead of using dendrites, the ribbon edges are maintained by two strings fed through holes in the crucible bottom, as shown in Figure 1.7(b) [87], [118]. The two heat resistant strings, usually made of quartz or carbon, are drawn upward out of the melt and after seeding with a piece of silicon wafer placed into the melt surface, along the width delimited by the strings, a continuous multicrystalline silicon ribbon is grown. The ribbon width, set by the distance between the strings, is independent of the melt temperature, a feature that permits a less critical temperature control of the liquid-solid interface (± 10 K range is tolerated), delivering greater process stability and reliability, and also allows the use of more cost-effective furnace designs [118], [119]. The growth rate is determined by the upward pull rate of the strings and the ribbon thickness is controlled by surface tension, heat loss from the ribbon and pull rate. At the liquid-solid interface, three heat fluxes are present: the heat conducted up the meniscus, the heat of fusion released at the interface and the heat conducted up the ribbon. Once a radiative steady state is achieved, thickness control is attained by varying the pulling speed, and the thickness profile along the ribbon width is controlled by the local melt temperature profile [118], [120]. STR ribbons are produced with a typical pull speed of 1-2 cm/min, can have widths up to 8 cm and thickness down to 100 µm, and solar cells made with these ribbons achieved a record efficiency of 17.8% with efficiencies of production-line lots averaging 13.5% [112], [120]–[122].

The EFG process is based on the control of the ribbon geometry by a slotted graphite die through which molten silicon in a crucible is fed via capillary action, as shown in Figure 1.7(c) [87]. A seed crystal is lowered into the silicon melt within the graphite slot, and the silicon spreads out over the top of the die to the edges where it is hold in place by surface tension. Then, the seed is pulled upwards, forming a liquid-solid interface with the meniscus shape being set by the die slot and having a height of same the order of magnitude of the ribbon thickness. Since the die separates the growth interface from the main melt surface, as the grown multicrystalline ribbon is pulled, more silicon enters trough the bottom of the graphite die, ascending by capillary [123], [124]. The ribbon thickness depends on several factors: the width of the die top, the distance between the die top and melt level, the meniscus shape, the heat loss from the ribbon and the pull rate. Similar to other ribbon technologies, to minimize thermal stresses the growth rate is

limited by how fast the heat can be removed through radiation and conduction, away from the solidifying ribbon [87], [124]. As a response to solve the edge stabilization problem on single line-shaped dies, new die geometries like octagonal or circular shapes were developed, allowing the growth of closed edge hollow octagons or cylinders, hence, increasing the rate of throughput as more ribbon material is crystallized per furnace. Hollow octagons with 8 to 12.5 cm wide faces (equivalent to growth of up to a 100 cm wide ribbon), lengths up to 5 m and wall thickness in the 150-300 μm range were successfully grown with a pull speed of 1.7 cm/min [112], [125], [126]. Hollow cylindrical silicon ribbons were also successfully grown, having 50 cm in diameter, length up to 1.2 m and wall thicknesses ranging from 75 to 300 μm [127]. Solar cells made with silicon ribbons from EFG octagon, achieved a record efficiency of 18.2% with average cell efficiency of 14.7% [121], [125].

The RGS process is a horizontal growth technique, that uses a silicon melt reservoir and die placed in close contact with the top surface of a cooler substrate, over which the ribbon grows, as shown in Figure 1.7(d) [87], [128]. The substrate, usually in graphite, ceramic or quartz, is pulled along the bottom of the crucible, creating a large, wedge-shaped crystallization front, with crystal growth being nearly perpendicular to both substrate plane and pull direction. The die acts not only as a melt container, but also as a shaper, determining the ribbon width and the crystallization time. Ribbon thickness, with values between 100 and 400 μm being achieved, is controlled by the heat removal rate to the substrate, pull speed and surface tension, and is independent of the ribbon width. [87], [128]. The large area of the liquid-solid interface, in direct contact with the substrate and ascending to the ribbon surface as it crystalizes, allows for a higher rate of latent heat extraction from the ribbon to the substrate by heat conduction. Thus, thermal gradients near the solidifying interface are small, reducing thermally induced stresses in the ribbon, being possible to set very high pull speeds, as values in the 4-9 m/min range have been demonstrated [128], [129]. Solar cells made with RGS ribbons reached a record efficiency of 14.4% [130].

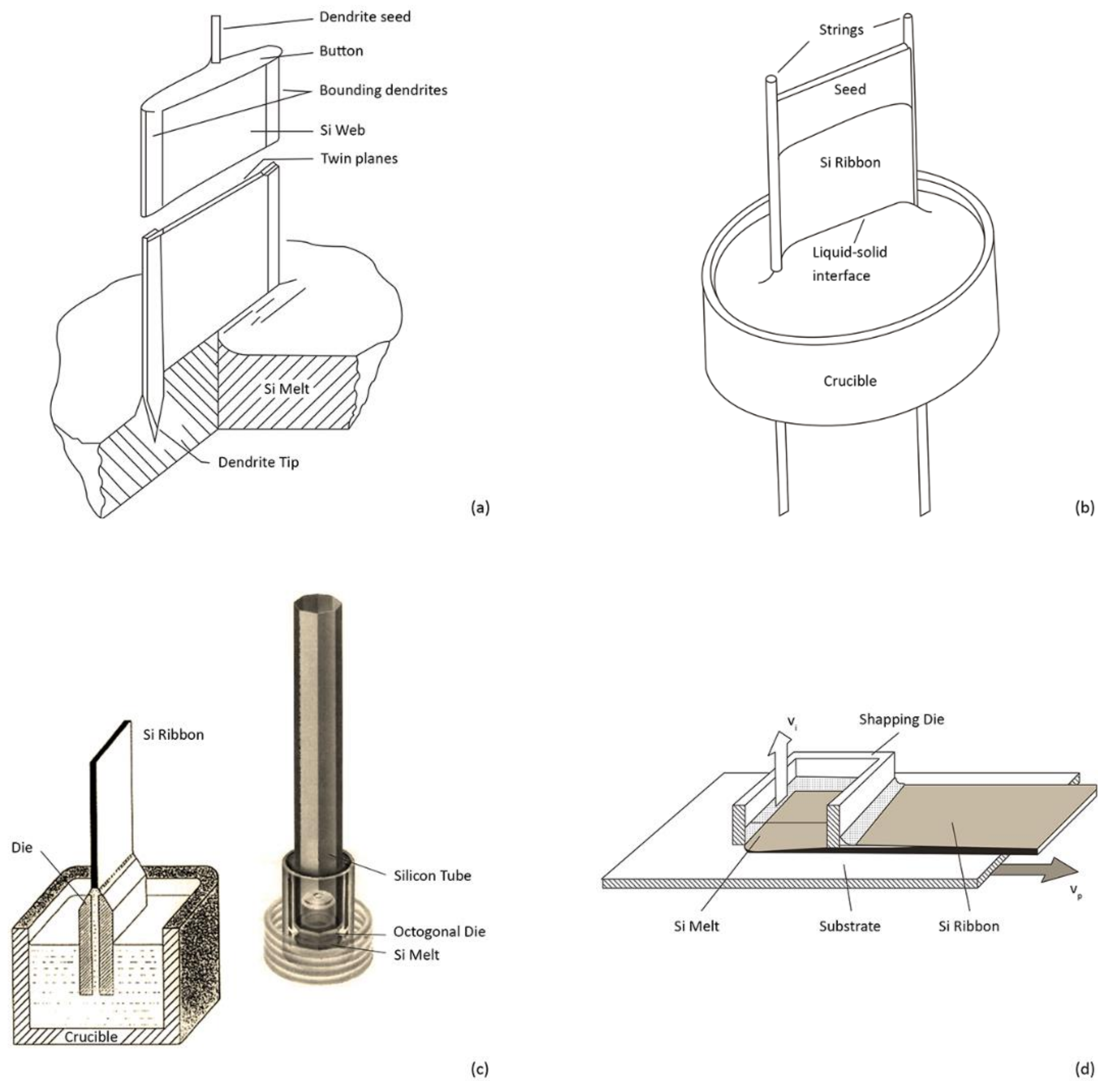


Figure 1.7 - Schematics of ribbon growth technologies [87]: (a) dendritic web (WEB); (b) string ribbon (STR); (c) edge-defined film-fed (EFG); and (d) ribbon growth on substrate (RGS).

The SF process details are proprietary, hence comprehensive information about the process is not as abundant as in other ribbons technologies. A silicon crystal thin layer is grown directly upon either an insulating or a conducting substrate, with a barrier layer promoting nucleation. Unlike other ribbon technologies, the substrate is not detached, being an active part of the solar cell. Very thin silicon layers (below 100 µm) were successfully grown over various substrates, including steel, ceramics and graphite cloth, having a barrier layer to prevent the transport of impurities from the substrate into the silicon [87]. Solar cells made with polycrystalline silicon ribbons obtained with the SF process, achieved a record efficiency of 16.6% and average cell efficiency of 10.0% [131], [132].

Table 1.1 summarizes the key material characteristics and production metrics of ribbon technologies grown directly from molten silicon.

Table 1.1 - Production metrics and material characteristics of ribbon technologies, compared with Cz and DS crystal growth.

Process[a]	Pull Speed (cm/min)	Width (cm)	Throughput (cm^2/min)[b]	Thickness (µm)	Grain Width (mm)	Dislocation Density (cm^{-2})	Efficiency (typ., best) (%)
Cz	0.05-0.2	⌀10-45	243-973	150-180	∞	0	20, 26.7
DS	0.01-0.06	up to 90	779-4673	150-180	1-50	10^4-10^6	18, 21.9
WEB	1-2	5-8	5-16	75-150	∞[c]	10^4-10^5	14.0, 17.2
STR	1-2	5-8	5-16	100-300	1-10	10^4-10^6	13.5, 17.8
EFG octagon	1.65	8-12.5	165	150-300	1-10	10^5-10^6	14.7, 18.2
RGS	600-1000	12.5	7500-12500	100-400	0.1-0.5	10^5-10^7	10.1, 14.4
SF	310	20	7500-9000	50-100	0.1-0.5	10^4-10^5	10.0, 16.6

[a] References: Cz [69], [85], [87], [108], DS [69], [87], [94], [108], WEB [112], [116], [117], STR [112], [113], [118], [120]–[122], EFG octagon [112], [113], [121], [125], [126], RGS [112], [113], [128]–[130] and SF [87], [112], [113], [131], [132].

[b] Throughput for Cz and DS calculated from pull speed, assuming 50% of kerf loss, 156×156 mm^2 size wafers and a DS ingot made of 4 by 4 blocks.

[c] The WEB ribbons are not single crystals since they contain two or more twin planes (arising from the growth of the dendrites) parallel to the face of the crystal.

All these ribbon technologies have reached pilot demonstration phases, but only EFG (by RWE Schott Solar in the United States and Germany) and STR (by Evergreen Solar in the United States) have been commercialized. To become commercially competitive, ribbon technologies need to meet the challenges of a highly the competitive photovoltaic market and overcome several technical barriers, such as: increase the productivity on a per furnace basis, to drive down labour and overhead costs, improve mechanical and electronic quality of ribbon wafers and reduce ribbon thickness while maintaining high material yields [87], [112], [133], [134].

1.10. Silicon Solar Cells

Solar cells are conceptually simple devices, relying on the photovoltaic effect for generating electricity from absorbed light. The photovoltaic effect was demonstrated by Bequerel in 1839, by illuminating platinum electrodes coated with AgCl or AgBr inserted into an acidic solution [135]. The next breakthrough occurred in 1876 when Adams and Day showed that it was possible to generate a current in a selenium bar, just by the action of light [136], leading to the first thin-film Se solar cell fabricated in 1883 by Fritts [137]. The first p-n junction solar cells,

with grown-in junctions formed by impurity segregation in recrystallised silicon melts,[1] where presented in 1941 by Russel Ohl of Bell Labs [138], followed by the development of the first practical solar cell by the same institution in 1954 [38].

Most solar cells produced until now have been based on silicon pn-junctions, a semiconductor material from group IV of the periodic table. Each silicon atom has four valence electrons shared with four surrounding Si atoms, forming covalent bonds within a regular and periodic diamond cubic lattice structure. Two energy levels are present: the valence band where the electrons of the covalent bounds do not have enough energy to escape from the atom's vicinity, and the conduction band made by electrons that gained enough energy to move freely within the crystal lattice and participate in conduction. The empty space left behind by an electron is called a hole, allowing a covalent bond to move from one electron to another, similar to a positive charge moving through the crystal lattice. The minimum amount of energy required to excite an electron from the valence to the conduction band is called the band gap, being a defining characteristic of a semiconductor material.

Intrinsic semiconductors are pure material with no dopant species added, thus the concentration of free carriers (electrons in the conduction band and holes in the valence band) depends only on the band gap and temperature. At a temperature of 25 °C, intrinsic silicon has a free carrier concentration of around 8×10^9 cm^{-3}, increasing with temperature as thermally excited electrons are able to move into the conduction band [139], [140]. The free carrier concentration can be changed by doping, a technique consisting in the addition of foreign atoms to the semiconductor. Regarding silicon, n-type silicon is obtained by doping with atoms from group V, such as phosphorous, while p-type silicon material is obtained by doping with atoms from group III, such as boron. Phosphorous forms four covalent bonds with a silicon atom, leaving an extra electron that is free to participate in conduction, thus in n-type silicon the majority carriers are electrons. On the other hand, boron only forms three covalent bonds with a silicon atom, leaving an extra hole, hence in p-type silicon the majority carriers are holes. In doped semiconductors, since dopant concentration is much higher than intrinsic carrier concentration, and nearly all the dopant atoms are ionized, the concentration of majority carriers is

[1] During the solidification of the silicon ingot within a silica crucible, the different segregation coefficients of dopant species led to the formation of three distinct zones: (i) a p-type zone with columnar crystalline structure in the upper portion of the ingot; (ii) a n-type zone that is non-columnar in the lower portion of the ingot; and (iii) a "barrier" zone between the two previous zones, where the p-n junction is formed. When illuminated, devices made with this material showed good photovoltaic response, developing a positive thermoelectric potential in the upper region and a negative one in the region bellow the "barrier" (hence named as "P" zone and "N" zone, respectively) [138].

approximately equal to the doping. This leads to majority carrier concentration being several orders of magnitude higher than minority carrier concentration (for example, on n-type silicon with dopant concentration of $N_D = 10^{16}$ cm^{-3}, hole concentration will be $p = 10^4$ cm^{-3}), thus, conductivity becomes dependent on the number of dopant atoms rather than the temperature [141], [142].

When illuminating a semiconductor, only photons with energy equal or higher than the band gap, are able to be absorbed and create an electron-hole pair, nevertheless the photon energy excess above the band gap is wasted as excited electrons will thermalize back down to the conduction band edge. The absorption coefficient, a measure of how far into a material light of a particular wavelength can penetrate before being absorbed, is proportional to the probability of the transition of an electron from the initial state to the final state, the density of electrons in the initial state and the density of available final states and summed over all possible transitions between states [143], [144]. In an illuminated solar cell, the number of minority carriers is basically equal to the number of light-generated carriers, since the number photo-generated minority carriers is several orders of magnitude above the minority carriers existing in the same solar cell in the dark.

Light-generated carriers will eventually return to their equilibrium state, as electrons fall from the conduction to the valence band and consequently eliminating a valence band hole, in a process named recombination. There are three main recombination mechanisms: recombination through defect levels in the band gap also known as Shockley-Read-Hall, radiative (band-to-band) and Auger. In radiative recombination, an electron in the conduction band directly combines with a hole in the valence band, emitting a photon with an energy similar to the band gap. Radiative recombination is dominant on direct band gap semiconductors, such as GaAs, CdTe, GaInP, while in indirect band gap semiconductors, such as Si and Ge, it is an unlikely event, playing a minor role on the overall recombination mechanism [142], [145]. The Shockley-Read-Hall recombination happens in semiconductors with impurities (unintentionally introduced or deliberately added to the material, for example in doping) or crystalline defects, which introduce defect levels with energy levels that could lie within the band gap. These defect levels are responsible for a two-step recombination process, where an electron (or a hole) is trapped by an energy level in the forbidden region. Then, if a hole (or an electron) moves to the same trap level, before the previous electron (or a hole) being emitted to the conduction (or valence) band, it recombines. This is the dominant recombination mechanism in silicon solar cells and very effective when the energy of the trap level is near the

middle of the bandgap [142], [146], [147]. The Auger recombination is a three-particle process, where an electron in the conduction band recombines with a hole in the valance band, giving its energy to a third carrier, an electron in the conduction (or a hole in the valance) band that will then thermalize back to its original energy state. Auger recombination becomes dominant in semiconductors with high carrier concentrations [142], [148].

The minority carrier lifetime of a material, often referred as lifetime and denoted by τ, is the average time which a minority carrier can spend in an excited state after an electron-hole pair generation, before it recombines. Lifetime is dependent on the several recombination rates present in the material, which in turn are related with the carrier (both minority and majority) concentrations [142], [144]. Since each of the recombination processes occurs in parallel, the total recombination rate is the sum of rates due to each process, and the effective minority carrier lifetime for a doped material is given by:

$$\frac{1}{\tau} = \left(\sum_{traps\ i} \frac{1}{\tau_{SRH,i}} \right) + \frac{1}{\tau_{\lambda}} + \frac{1}{\tau_{Auger}} \tag{1.16}$$

Lifetime is a proxy indicator of solar cell efficiency, as for the same solar cell structure and manufacture techniques, cells made with silicon wafers of higher lifetime will have greater efficiencies.

For a semiconductor in thermal equilibrium the carriers move freely and randomly trough the lattice with no net overall movement of carriers in any direction. However, when an external electric field is applied or under incident light, drift and diffusion currents arise. Drift current is the charged particle's reaction to an applied electric field, thus electrons in the conduction band, being negatively charged, move in the opposite direction of the applied field, while holes in the valence band, being positively charged, move in the same direction. The drift current densities for holes and electrons are directly proportional to the electric field, carrier mobility and density. Diffusion current is a response to carrier concentration gradients that may emerge from light generated carriers not being uniformly distributed along the semiconductor depth, therefore, through random motion, carriers will have a net movement from areas of high concentration to areas of low concentration. Diffusion current is directly proportional to the carrier diffusion coefficients and to the gradient of the carrier concentrations [142], [144].

The basis of a solar cell and many semiconductor devices is the pn-junction, obtained by joining n-type material with p-type material, causing the excess electrons from the n-type side to diffuse

to the p-type material and excess holes in the p-type side to diffuse to the n-type material. This movement of carriers exposes positive ion cores in the n-type side and negative ion cores in the p-type side, resulting in an electric field at the junction that counteracts the diffusion of carriers. The transition region between the two materials is called space-charge region or depletion region, since the electric field quickly sweeps free carriers out, becoming depleted of them. The equations describing the electric potential, electric filed, energy levels and charge density in a pn-junction and across the depletion region are thoroughly explained elsewhere [144], [149].

A schematic of a simple conventional solar cell is presented in Figure 1.8(a). The pn-junction is asymmetrically doped, as in p-type cells the p-type base is 10^2 to 10^3 times thicker than the n-type emitter and in n-type cells the same applies for the n-type base. Two metallic contacts are present, in this case located in the front and rear of the cell, and the front surface is textured to increase light trapping. Light-generated minority carriers on both junction sides will only exist for a time period of the order of magnitude of the respective minority carrier lifetime. The collection of these minority carriers by the pn-junction prevents recombination, as excited electrons flow from the p-type to the n-type side, while holes flow in the opposite direction. If the solar cell is connected to an external load, the light-generated minority carriers can be gathered by a metallic contact, flow through the external circuit and latter recombining on the other pn-junction side. Although this flow of minority carriers through the space-charge region is in the direction where it is assisted by the field, the main source of this directionality is due to the fact that the n-type region allows selective contact to the conduction band (excited states), while the p-type region allows selective contact to the valence band (ground state) [150].

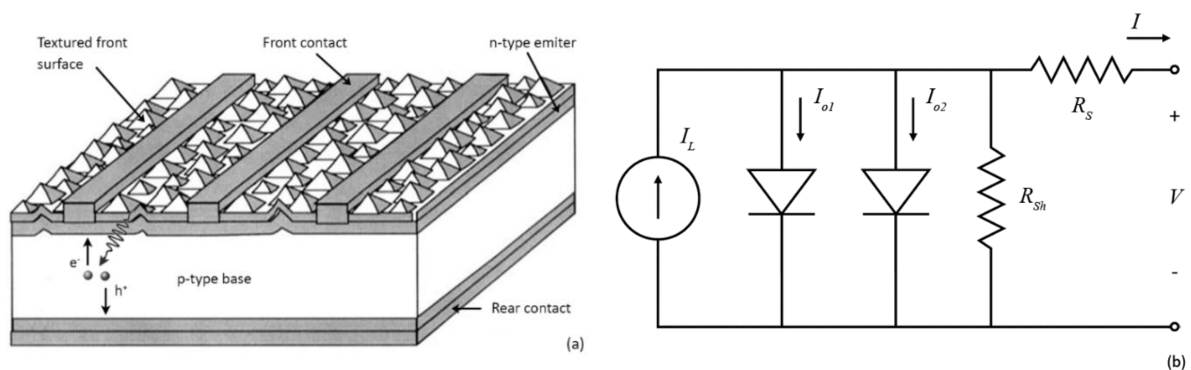


Figure 1.8 - Silicon solar cell: (a) schematic of a simple conventional cell [150]; and (b) equivalent electric circuit.

The two-diode model equivalent electric circuit of a solar cell consists in a current source, two diodes and two resistances, as shown in Figure 1.8(b). The current source is the light-generated current in p-type and n-type regions (I_L), the two diodes in parallel represent the dark saturation

current due to recombination in the base and emitter (I_{o1}) and depletion region (I_{o2}) and the two resistances arising from non-idealities in cell structure and manufacture, a series resistance (R_S) and another in parallel (shunt resistance, R_{Sh}). The series resistance comes from contact resistance between metal contacts and silicon, and ohmic resistances both in the metal contacts and in silicon material, while the shunt resistance is caused by manufacturing defects leading to leaking currents along the solar cell edges [151].[2]

The current-voltage characteristic of a solar (or I-V curve) is given by equation (1.17). The equations for I_L, I_{o1} and I_{o2} are complex and depend on solar cell structure, material properties and operating conditions, being explained in detail elsewhere [144], [151].

$$I = I_L - I_{o1}\left(e^{q(V+IR_S)/kT} - 1\right) - I_{o2}\left(e^{q(V+IR_S)/2kT} - 1\right) - \frac{(V + IR_S)}{R_{Sh}} \qquad (1.17)$$

The design and fabrication of silicon solar cells has greatly evolved [152] since the first prototypes in the late 1940s and 1950s with efficiencies of around 6% [38], and is currently approaching the Shockley-Queisser efficiency limit of 29.4% for a single junction silicon solar cell under a one-sun AM1.5 spectrum [153]–[155], as most recent monocrystalline single junction n-type silicon cell reached a record efficiency of 26.1% [156]. R&D on silicon solar cells has been driven by addressing non-ideal behaviours that cause efficiency losses, namely optical losses, excess bulk and surface recombination, resistive and contact losses [157]. Therefore, the main design objectives are increasing the amount of light collected by the cell, improve the collection of light-generated carriers in the pn junction, reducing carrier recombination and extracting the current from the cell with minimal resistive losses.

The most common and mature solar cell structure is known as Al-BSF, having as unique feature a screen-printed aluminium paste on the rear surface, which creates a back surface field (BSF) [158]. It was first developed in the 1970s and presently dominates the market of p-type modules for terrestrial photovoltaic applications. The main advantage of this technique is delivering a fairly good cell efficiency in a simple and cost-effective process [159]. It starts with surface texturing to reduce reflection, followed by a phosphorous diffusion at 800-1000 °C on a p-type wafer (previously cleaned in an alkaline etch bath to remove saw damaged), creating a thin n-type layer and forming the pn-junction. The junction at the wafer edges is then removed, usually by laser edge isolation. On monocrystalline silicon substrates, pyramids on the wafer surface

[2] A low series resistance and a high shunt resistance are targeted during the fabrication of solar cells.

are formed by anisotropic etching with a chemical solution [160], while on multicrystalline silicon, due to random grain orientation, other methods such as mechanical texturing [161], isotropic chemical etching [162] or plasma etching [163] are used. An antireflection coating (ARC) of silicon nitride (SiN_x), is applied by atmospheric pressure (or plasma-enhanced) chemical vapour deposition, which also passivates the front surface reducing surface recombination [164], [165]. The BSF is obtained by screen-printing an aluminium paste over the entire rear surface, followed by a second screen-printing of an Al/Ag paste with the rear contact pattern and subsequent alloying through firing. The front silver contact is also screen-printed, in a line pattern to prevent cell shading, and the firing processes allows the metal contacts to pierce through the ARC and bond to the underlying silicon.

1.11. Summary and Motivation

The focus of this PhD thesis is the Silicon on Dust Substrate (SDS) process, a unique and innovative approach for producing silicon ribbons directly from gaseous feedstock.

Chapter 2 describes the theoretical basis and concepts supporting the SDS process as well as the experimental setup and procedure. Computational simulation results, that characterize the experimental setup and processes, are presented.

Chapter 3 presents and discusses the results obtained by the SDS experimental setup, specifically: (i) the micrometric sized silicon powders prepared by the SDS-grinding mill; (ii) the pre-ribbons produced in the chemical vapour deposition (CVD) step; and (iii) the final multicrystalline ribbons achieved with the zone melting recrystallization (ZMR) technique.

Finally, Chapter 4 presents key concluding remarks about the developed work and suggests future research topics towards the SDS process improvement.

Chapter 2

Silicon on Dust Substrate Process

2.1. Process Overview

The Silicon on Dust Substrate is a gas-to-wafer process, aiming to produce multicrystalline silicon ribbons directly from gaseous feedstock, bypassing the standard industry steps of polysilicon deposition, crystal growth and wafering. Figure 2.1 presents the SDS process diagram compared with crystalline silicon wafer production for solar applications.

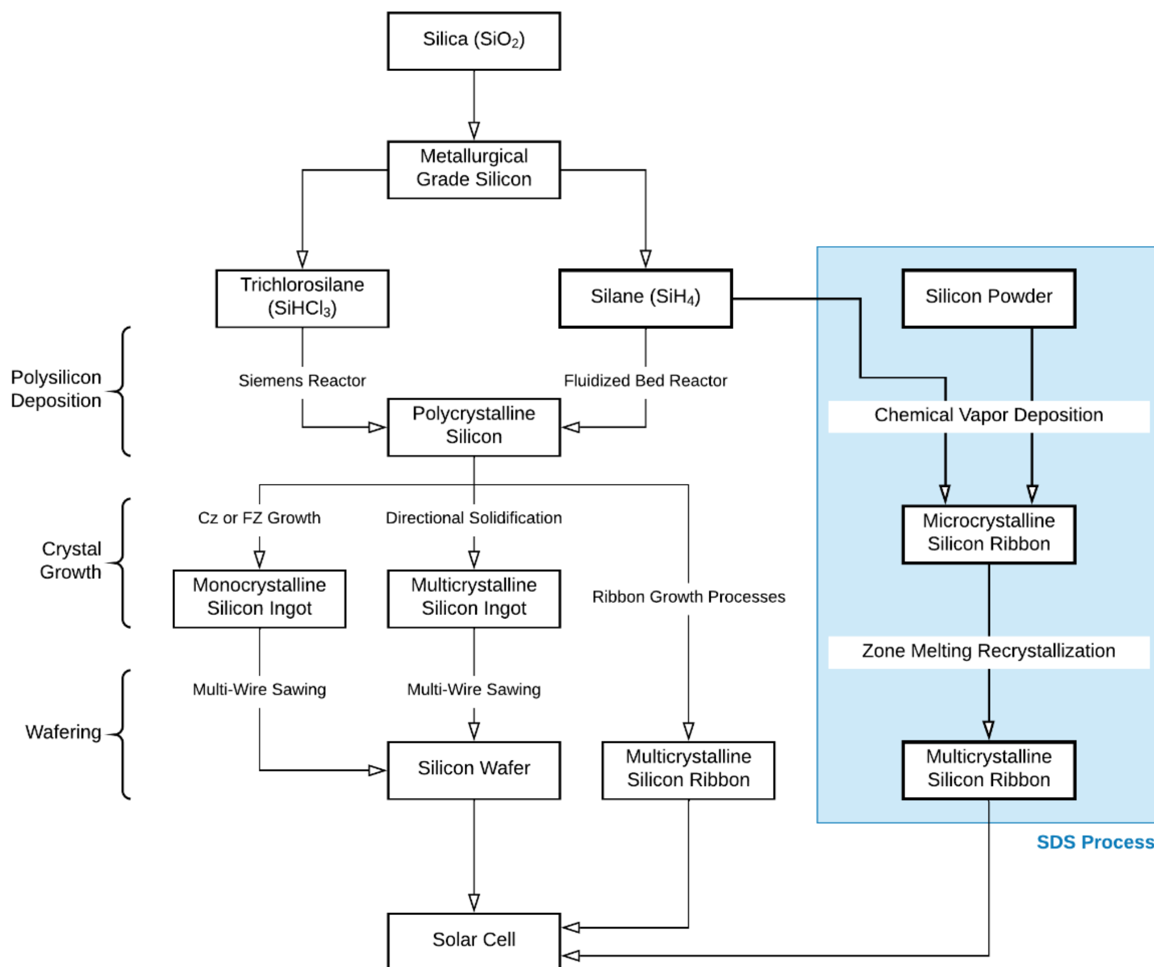


Figure 2.1 - SDS process diagram compared with industrial standard production of crystalline silicon wafers.

The SDS technique consists in three main steps: (i) production of silicon powder; (ii) chemical vapour deposition (CVD) of silicon over a silicon powder substrate; and (iii) zone melting

recrystallization (ZMR) of the microcrystalline pre-ribbon obtained in the CVD step. These three main steps are described in sections 2.2, 2.3 and 2.4, respectively, regarding the theoretical background, setup characterization and experimental procedure.

Initially, a layer of silicon powder is placed on top of a quartz holder, acting both as a deposition substrate during the CVD and as a sacrificial layer for easy detachment from the quartz. The silicon powder can be obtained either as a by-product of a fluidized bed reactor, or by grinding silicon wafers on a silicon mill. Next, a fast CVD at low temperature (< 900 K), atmospheric pressure and using silane as gaseous feedstock, deposits a thick layer of silicon over the powder substrate, resulting in a mechanically self-sustained, porous and microcrystalline silicon pre-ribbon. Finally, the pre-ribbon is subjected to ZMR, as a narrow horizontal molten zone with 2 mm height, travels along the pre-ribbon and turning into a multicrystalline silicon ribbon. Figure 2.2 shows a concise diagram of the SDS experimental process.

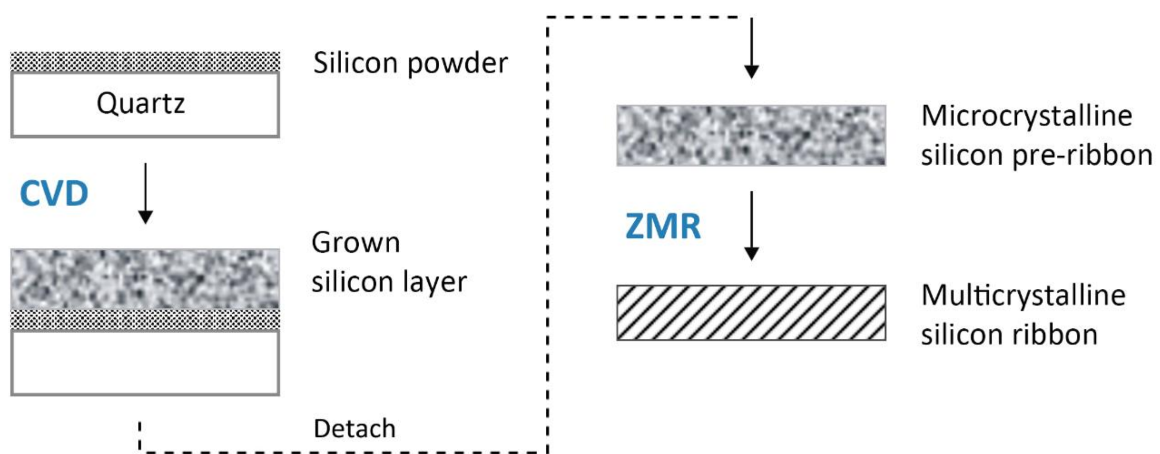


Figure 2.2 - SDS experimental process diagram.

The well-established production of silicon wafers, based on cutting either Czochralski grown monocrystalline or directional solidification grown multicrystalline silicon ingots, using multi-wire sawing techniques, is responsible for global material losses going up to over 40% [108] consequently, feedstock and wafering processes can represent up to one third of the final cost of ingot-based silicon PV modules [109]. This situation justifies the research on alternative methods to produce silicon substrates that increase material yield and allow for further cost reductions of PV devices. Therefore, the SDS is part of a broader group of different approaches to the current PV industry standards, such as ribbon technologies [112], [119], thin-films grown over a substrate [67], [166], [167], kerf-free wafering processes [168]–[170] and diamond-wire sawing followed by kerf recycling [61], [62].

The SDS process is similar to several ribbon technologies, by avoiding the usual crystal growth methods, namely the use of a crucible, and multi-wire sawing. However, some key differences set it apart from them: (i) in theory, SDS is a contamination free process, since no foreign material is in contact with the silicon powder substrate during CVD or the molten silicon during ribbon recrystallization and assuring that both gaseous feedstock and silicon powder have a high purity level; (ii) no high structural quality substrate is required; and (iii) low energy budget due to low temperature and atmospheric pressure used in the CVD process and due to the small volume of the molten zone during the ZMR process.

In summary, the SDS process has the potential to deliver good quality material for solar cell manufacturing with a significantly reduction of the overall cost.

2.2. Silicon Powder Preparation

2.2.1. Overview

The most common industrial processes for obtaining silicon powders and fines are: (i) silane pyrolysis on CVD reactors; and (ii) mechanical grinding of solid silicon.

Silane pyrolysis on CVD reactors may result in homogenous decomposition of silane and nucleation in the gas-phase, producing amorphous silicon powders (fines) or dust with particle size in the nanometre to a few micrometres range [171]. The growth of polysilicon granules in fluidized bed CVD reactors is well-known for having fines formation, an undesirable but always present by-product that contributes to material loss, increases the risk of contamination due to high specific surface area and adds additional reactor maintenance and handling time for recovering wall deposited fines [172]–[174]. Nevertheless, there is a substantial interest in studying the mechanism of silicon particles nucleation from silane pyrolysis, in order to synthesize nano or microcrystalline silicon powders or to produce silicon nanocrystals and nanostructures, with possible applications in electronics, energy and biology areas [175]–[178].

Opposed to silane pyrolysis on CVD reactors, which is a bottom-up approach, mechanical grinding of solid silicon is the simplest top-down manufacturing technique to produce silicon powders. Depending on experimental variables like the milling method (e.g., ball miller, rod miller), the applied power, the milling medium (e.g., tungsten carbide ball, silicon nitride ball),

speed and time, powders with different physical characteristics and purity can be obtained [179].

2.2.2. Silane Pyrolysis

The first type of powder used on the SDS process was supplied by a company that produces polysilicon granules. The powder was collected from scraping wall deposited fines on a fluidized bed CVD reactor, since this by-product must be removed from the reactor to assure optimal operation conditions. This powder is very fine having a particle size in the nanometre range and a high specific surface area, thus being very difficult to handle and prone to oxidize under normal atmosphere. Table 2.1 summarises key physical properties of the nanometric powder such as particle size, thermal conductivity and reflectivity, which were obtained on previous characterization studies [180], [181].

Table 2.1 - Particle size, thermal conductivity and reflectivity of the nanometric powder [180], [181].

Physical Property	Value
Particle size	700-800 nm
Conductivity	0.040 ± 0.001 $Wm^{-1}K^{-1}$
Reflectivity	[4; 5]% for [700; 1100] nm

It is important to highlight that thermal conductivity at a room temperature of 298 K is four orders of magnitude lower than of crystalline silicon [182], indicating that during CVD, the heat on the substrate is confined to well-defined heated regions where deposition occurs, while the rest of the powder remains at a lower temperature.[3] The reflectivity is one order of magnitude lower than of a polished monocrystalline silicon wafer (34% to 31% in the 700-1000 nm wavelength range [183]), an expected value since the powder has a dark grey to almost black colour as shown in Figure 2.3(a). Despite being obtained from silane pyrolysis, the nanometric powder does not have the required purity level for solar applications: an X-ray photon electron spectroscopy (XPS) analysis, shown in Figure 2.3(b), revealed a high concentration of iron and traces of calcium [184], and inductively coupled plasma mass spectrometry (ICP-MS) analysis measured a concentration of 750 ppb for iron, 590 ppb for

[3] While thermal conductivity of crystalline silicon decreases by one order of magnitude within the temperature range experienced during a CVD run, it is expected the variation in silicon powder to be much lower, almost negligible, due to the high amount of interstitial air.

nickel and 62 ppb for chromium [181]. The presence of these metals on concentrations such high concentrations on the substrates, can severely degrade the solar cell conversion efficiency [185].

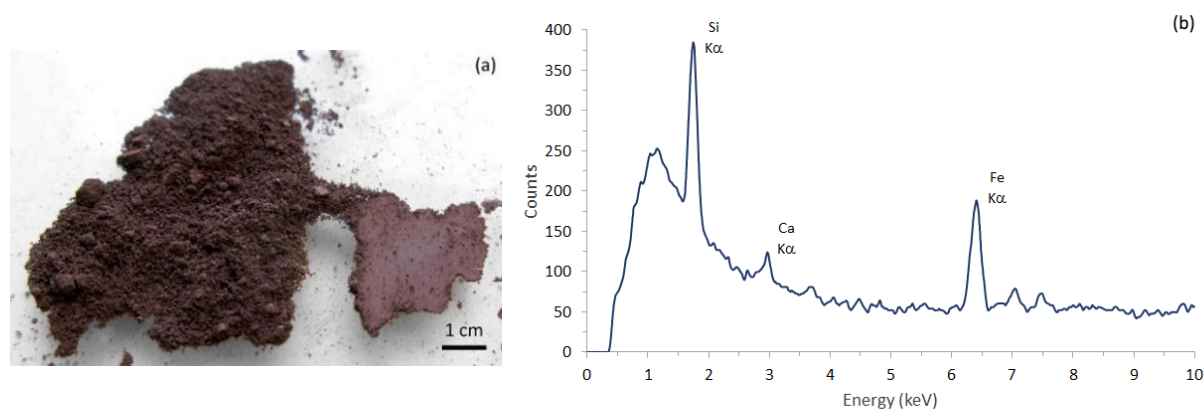


Figure 2.3 - Silicon nanometric powder: (a) visual appearance; and (b) XPS spectrum [184].

The presence of metal impurities in the silicon powder is the most significant source of contamination throughout the SDS process, since CVD and ZMR steps are designed to prevent the contact of the powder substrate and the silicon pre-ribbon with foreign materials during deposition and recrystallization stages, respectively. Moreover, both steps are performed under controlled atmospheres with high purity gaseous species. To address this issue, an in-house powder production system was previously developed, being able to produce silicon powders from multicrystalline silicon wafers while having a better control on impurities and physical properties of the powders, especially the particle size.

2.2.3. Mechanical Grinding

The SDS powder production system is based on comminution, the oldest mechanical operation for size reduction of solid materials and the most widely used method of powder production for hard metals and oxide powders [179]. Comminution is also used in mining operations for liberating the minerals from the rock or ore and progressively reducing the particle size, without changing the chemical properties of the material [186]. It consists of two main stages, starting with the crushing of large solid material into a particle size that can be fed to the second stage, the grinding process which delivers a powder with the desired particle size distribution. The final product is a silicon powder without any chemical or solid-state changes as opposed to high-energy mechanical milling, used to produce several types of powders with different

properties from the feeding materials, including amorphous alloy powders, nanocrystalline powders, intermetallic powders, or composite and nanocomposite powders [187].

During crushing and grinding, four types of forces combined act on the material: impact, attrition, shear and compression. Impact forces arise from the collision of two bodies, attrition produces new smaller particles by the rubbing action between solids, shear is the cutting or cleaving of solids, contributing for breaking them with minimum fines formation, and compression is the gradual application of compressive loads to a solid. At an atomic level, in materials with a crystalline lattice such as silicon, the inter-atomic bonds are effective only at small distances and can be broken when tensile or compressive loads are applied. Under an external deforming load, lattice defects are able to displace from one part of a crystal to another and as they accumulate in the same area, local stresses appear, which contribute to the formation of embryonic microcracks. The development and joining of embryonic microcracks results in the formation of main disruption cracks, and as the crack grows in size, two distinct moments are identified: the initial crack growth where more surface energy is consumed than released energy from relaxation of the stresses that designate its stability, and a second stage when reaching a critical crack length, the crack begins to release more energy than it consumes, propagating in the material at high speed, forming a new break surface [179], [188].

2.2.4. SDS-Crusher

The first mechanical stage of the powder production system is the crushing of multicrystalline silicon wafers measuring 15×15 cm^2 with a 240 μm thickness, resulting in a sand-like product with a particle size not greater than 2×2 mm^2. The SDS-crusher, a previously in-house developed equipment, is made in stainless steel with a silicon nitride surface coating, measures approximately $41\times12\times24$ cm^3 and its operating principle is the same of a jaw crusher [189]. The jaw crusher was firstly introduced by E.W. Blake in 1858 [190], consisting in a pair of rigid jaws set at an acute angle, one fixed and the other movable, between which the stones are to be broken. The material is fed at the top, repeatedly compressed and broken between the two jaws and when the particle size is small enough to pass through the discharge opening, it falls by gravity to a collecting tray. While in the Blake crusher the moving jaw is pivoted at the top, with a fixed receiving area and a variable discharge opening, the SDS-crusher is based in the Dodge crusher, commonly used in laboratory environment, with the moving jaw pivoted at the bottom, thus giving it a variable feed area but a fixed delivery area [189].

Figure 2.3(a) presents the SDS-crusher and Figure 2.3(b) a detailed view of the silicon nitride jaws.

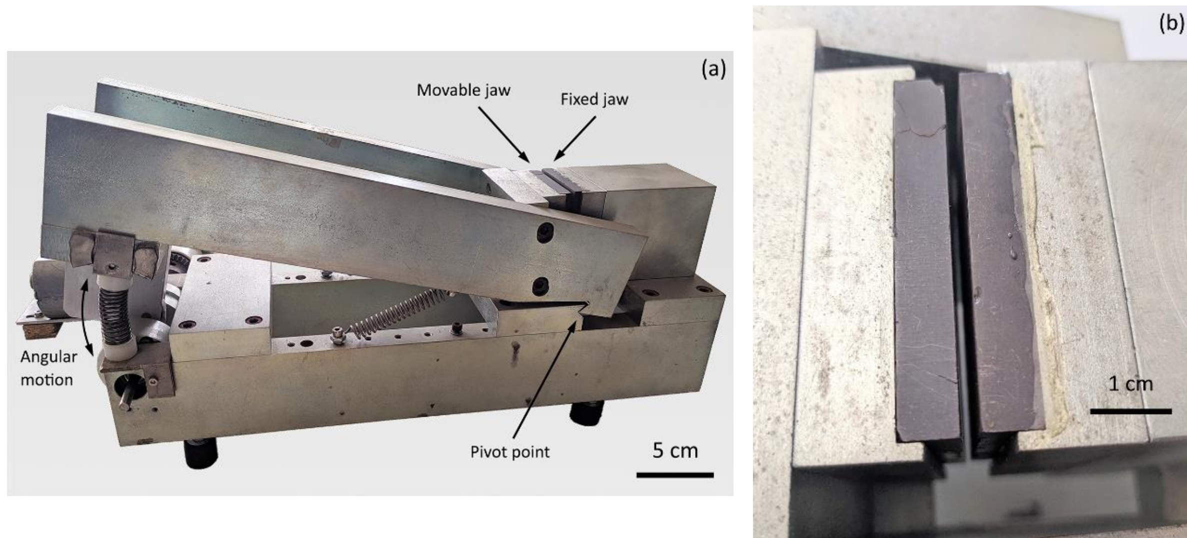


Figure 2.4 - SDS-crusher: (a) photo of the crusher; and (b) detailed view of the silicon nitride jaws.

The jaws of the SDS-crusher are made of silicon nitride, measure 55×48 mm^2 and the distance between them can be set before a crushing run, being possible to change the lengths of the top receiving area from 58 to 21 mm and of the bottom discharge opening from 38 mm to 50 µm. The moving jaw rests on an oscillating arm linked to a cam shaft driven by an AC motor with variable speed, and system underdamping is prevented by using a set of four springs connected between the arm and the crusher base.

On a typical run, the distance between jaws is initially set to a desired value, usually in the 50 to 800 µm range at the bottom opening, then chunks of multicrystalline silicon wafers are manually fed to the top opening and crushed into smaller particles. During a crushing cycle, larger particles in the collecting tray can be manually refed to the crusher receiving area until the desired particle size distribution is obtained, or a second crushing run with a lower distance between jaws can also be performed.

2.2.5. SDS-Grinding Mill

The last mechanical stage of the powder production system is the grinding of the silicon material prepared by the SDS-crusher. Industrial grinding mills are usually classified into two types: tumbling mills and stirred mills. In tumbling mills, the mill shell rotates, and motion is transferred to the material via the mill shell, with the grinding medium being steel rods, balls or the material to be grinded. Tumbling mills operating in mineral industry are commonly used

for primary grinding (grind material obtained by crushers), in which particles between 5 and 250 mm are reduced to sizes between 25 and 300 μm. The particle size of the obtained powder can be controlled by the grinding medium size, as smaller grinding medium results in finer powders. In stirred mills, the stationary mill shell is mounted either horizontally or vertically, and motion is transferred to the material by the movement of an internal stirrer, comprised of a central shaft to which the grinding medium (may be screw-shaped, pins, rods, discs or other designs) is attached. Another major difference is that while in tumbling mills both impact and shear forces are equally present, in stirred mills the predominant forces are attrition and shear, which are more effective for fine grinding, therefore stirred mills are more energy efficient than tumbling mills when the aimed product size is below 100 μm. Hence, stirred mills usually operate as second or third stage grinders, regrinding previous grinded material to obtain fine and ultrafine powders, from 40 μm to below 15 μm [191].

The design and operation principle of the SDS-grinding mill is based on the stirred mill concept, firstly introduced by P. Klein and A. Szegvari in 1934 [192], with a device to produce fine powders on a liquid (wet grinding), using an agitator and spherical grinding media. Further developments on stirred mill technology contributed to a wide range of fine to ultrafine grinding applications on several industries from electronics, mining, chemical and pharmaceutical [193].

The SDS-grinding mill, a previously in-house developed equipment, is an aluminium cylindrical structure with 14.0 cm in diameter, composed of two coaxial cylinder pieces: a base of 10.0 cm in height and the top with 3.4 cm. The top cylinder is held within the 44.40 to 45.60 mm range above the base with the help of three threaded rods and respective locking nuts. A vertical shaft, driven by an AC motor, passes through the axis of the cylindrical base and a silicon nitride ball secured at the shaft end rests inside a silicon nitride spherical shell housed at the top cylinder. The ball has a diameter of 27.90 mm and in practical terms it can be as close to the spherical shell surface as 10 μm, a distance that can be adjusted by moving and securing the top cylinder along three threaded rods. A circular opening through the top cylinder and spherical shell, allows the material to enter the grinder, and as the particles fall through the space between the ball and the spherical shell, they are grinded mostly due to attrition and shear forces transferred from the rotating ball.

Figure 2.5 presents the SDS-grinding mill and a detailed view of the silicon nitride milling ball and spherical shell.

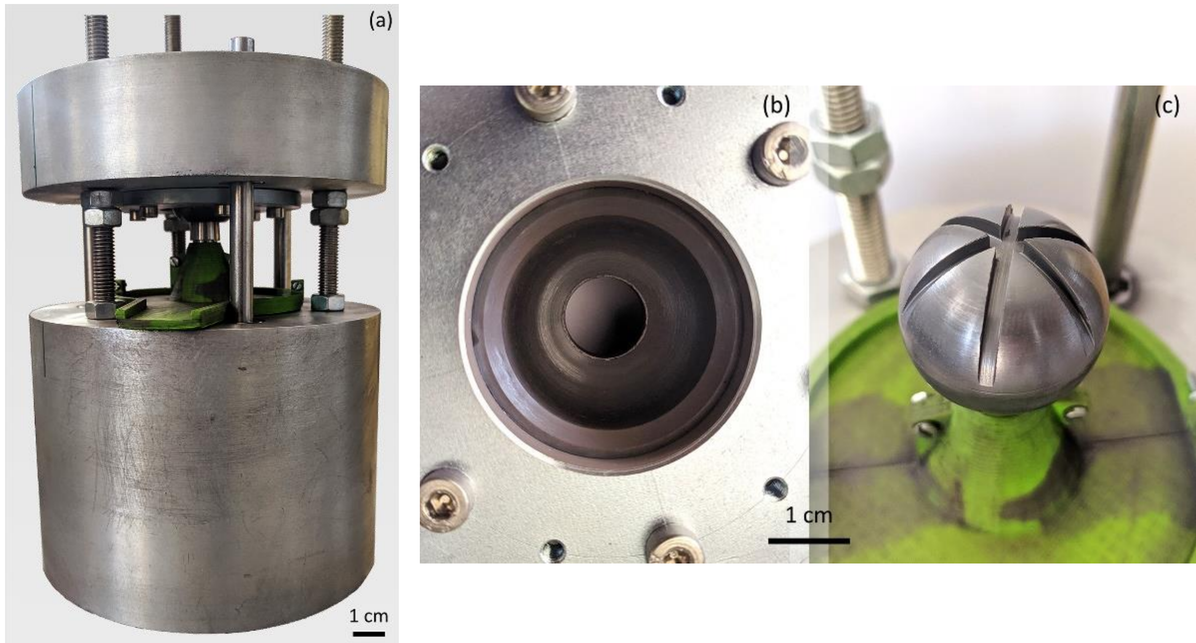


Figure 2.5 - SDS-grinding mill: (a) photo of the grinding mill; and detailed views of (b) the spherical shell and (c) the silicon nitride milling ball.

While the silicon nitride top shell has a perfect spherical shape with 28.00 mm of inner diameter, the milling ball has six longitudinal surface grooves running from the top to the equator with a decreasing depth, as seen in Figure 2.5(c). This intentionally developed design provides two main advantages: (i) allows for more material to be feed at the top opening; and (ii) as the material falls along the narrowing space between the ball and the spherical shell, there is an increasing intensity of attrition and shear forces which enhances the effectiveness of the grinding process. When the grinded particles are small enough to pass through the bottom discharge opening, they fall to the collecting tray, a 3D-printed cone with a circular base in polylactic acid (PLA) material, surrounding and shielding the vertical shaft.

The SDS powder production system was designed to minimize metal contamination, thus all parts in direct contact with the silicon are made of ultra-pure silicon nitride. Silicon nitride grinding mills were already used and demonstrated to produce silicon powders [194] and silicon nitride powders [195], without introducing metal contaminants.

On a typical run, the distance between the two cylindrical pieces is set around 44.60 mm, the AC motor drives the shaft at a constant angular velocity and the silicon obtained from the SDS-crusher is manually fed to the top receiving area of the grinder. As the silicon is grinded by the rotating ball, a fine silicon powder is collected on the tray bellow.

2.2.6. Powder Characterization

The particle size of the silicon powder obtained after the SDS-grinding mill, ranges approximately from coarse (around 300 μm) to ultrafine (<25 μm) particles. The size distribution depends on the configuration of the SDS-grinding mill, particularly the distance between the top cylinder and the base.

The silicon powder can be used directly as a substrate for CVD, or it can pass through an additional, although optional, step of mechanical segregation to separate the particles into narrower size distributions. To characterize the powder size distribution, two methods of segregation were employed: (i) a set of test sieves with different mesh sizes; and (ii) a manually vibrated tray with particles being segregated by push-away mechanism and impact effects, since particles bouncing against each other, heavy particles will push away the lighter ones that have already settled down at the centre [196]. In the first method, seven sieves with mesh sizes of 25, 45, 75, 106, 180, 250 and 355 μm separated the silicon powder in seven well-defined particle size intervals. The second method is not as accurate as the sieves, although it was possible to obtain coarse, medium and fine silicon powders.

The silicon powder's thermal conductivity at room temperature of 298 K was measured, using a thermal properties analyser tool for solids and other porous materials. A glass tube was filled with compressed silicon powder and a needle-shaped probe, containing a resistive heater and a temperature sensor inside, was inserted into the powder. Powder conductivity was automatically calculated by the device, after passing current through the heater and measuring the resulting temperature profile.

2.3. Chemical Vapour Deposition

2.3.1. Overview

CVD is a widely used process in electronic and chemical industries, to grow thin films for applications such as dielectrics, conductors, passivation layers, protective coatings and epitaxial layers. It belongs to a group of processes where a solid material is deposited from vapour phase by a chemical reaction taking place on or near a heated surface substrate, resulting in a solid material in the form of a thin film, powder or single crystal. By varying the experimental conditions, like substrate material, temperature, pressure, flow rate and chemical composition

of the reaction gas mixture, it is possible to grow a wide variety of materials with different chemical and physical properties [197].

In every CVD, there are three main reaction areas and two interfaces between them: (i) the substrate; (ii) the grown film; and (iii) the stagnant boundary layer at the top. As the gas mixture passes over the substrate and grown film areas, fluid dynamics of the process results in a fairly stable and stagnant boundary layer that transports both reactant gases and reaction products. Homogenous reactions may occur either in the gas flow or in the stagnant boundary layer, resulting in homogeneous nucleation and the formation of a solid thin powder, which is not convenient for most CVD applications. Heterogeneous reactions take place in the solid/vapour phase interface, contributing to the film growth, and their behaviour plays a decisive role on the growth rate and the properties of the grown film.

The heterogeneous reactions dynamics on a gas-solid interface are complex, still the range of processes happening in a gas-solid interaction are summarized by Figure 2.6 diagram, being as follows: (i) convective transport of the gaseous reactants to the boundary layer above the solid substrate; (ii) transport by diffusion and convection of the gaseous reactants across the boundary layer to the surface of the substrate; (iii) reactants adsorption on the surface of the substrate; (iv) chemical reactions (surface reactions between adsorbed species, between adsorbed species and reactants in the vapour or between reactants in the vapour); (v) nucleation and film growth; (vi) desorption of some reaction products from the surface of the substrate; and (vii) transport of desorbed reaction products to the gas mixture in the boundary layer and then away from it. These processes may happen simultaneously during a CVD run [197].

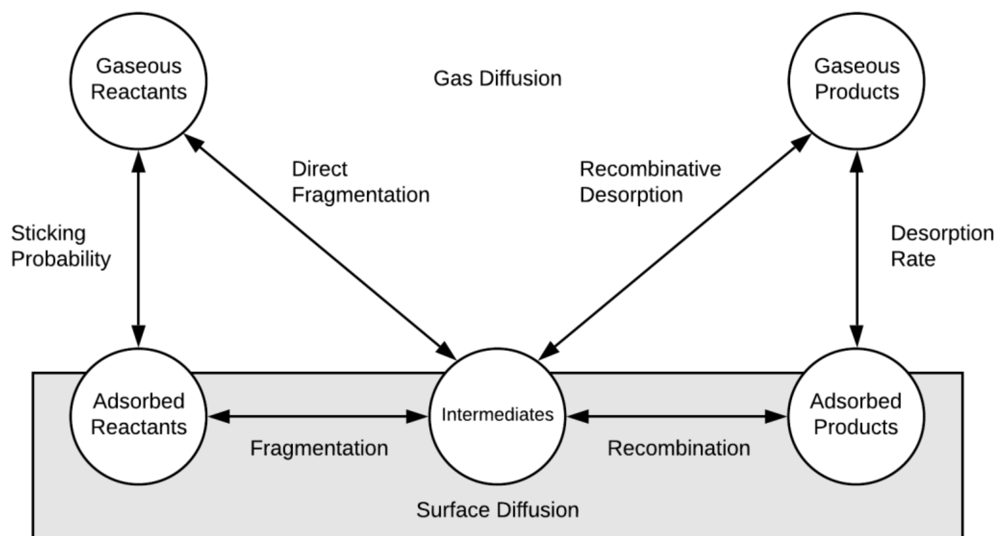


Figure 2.6 - Diagram of gas-solid interactions [198], [199].

The CVD reactor used in the SDS technique (SDS-CVD), operates in a regime where surface kinetics or nucleation is the limiting step, since the silicon deposition rate is: (i) lower than the silane mass input rate; and (ii) lower than the species mass transport rate in the vapour to or from the substrate. This regime is characterized by fast diffusion in the vapour and slow surface reaction.

For silicon nucleation to occur over the substrate, gaseous silane molecules must be activated, and the silicon powder substrate cannot inhibit the deposition, the growth rate will then depend on the number of activated reactant molecules striking the substrate. In an equilibrium state the number of reactant molecules interacting with a unit area of the substrate is given by the Maxwell distribution, but in an actual CVD run other factors impact the striking rate of reactants, like the fluid dynamics behaviour, partial pressures of gaseous species or temperature.

Activation energy is the threshold energy value that reactant gaseous molecules should have to fragment and deposit when they strike the substrate. Assuming the gas phase behaves like an ideal gas (potential energy is zero) and reactant molecules are not excited (their intrinsic energy is constant), therefore their kinetic energy has to be higher than the activation energy [200], [201]. The activation energy also depends on the operating conditions inside a CVD reactor, and several studies with similar conditions as the SDS-CVD process, have reported an activation energy for silane pyrolysis, within the 30-56 kcal/mol range [202]–[206].

2.3.2. Chemical Reactions

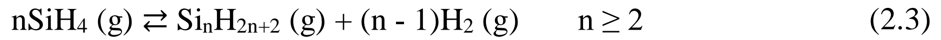
Inside the SDS-CVD reactor, the thermal decomposition or pyrolytic reaction of silane dissociates it in solid silicon and gaseous hydrogen, according to:

$$SiH_4\ (g) \rightarrow Si\ (s) + 2H_2\ (g) \qquad (2.1)$$

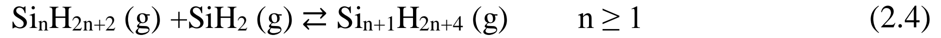
Nevertheless, the whole reaction mechanism is more complex, with homogeneous reactions of silane and by-products in the gas phase and heterogeneous decomposition on the substrate. The initial and most common reaction is the silane homogeneous dissociation into SiH_2 and H_2:

$$SiH_4\ (g) \rightleftarrows SiH_2\ (g) + H_2\ (g) \qquad (2.2)$$

Silane and SiH_2 will contribute to the formation of disilane (Si_2H_6), trisilane (Si_3H_8) and other polysilanes (Si_nH_{2n+2}):



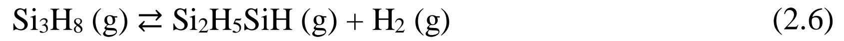
$$nSiH_4\ (g) \rightleftarrows Si_nH_{2n+2}\ (g) + (n-1)H_2\ (g) \qquad n \geq 2 \qquad (2.3)$$



$$Si_nH_{2n+2}\ (g) + SiH_2\ (g) \rightleftarrows Si_{n+1}H_{2n+4}\ (g) \qquad n \geq 1 \qquad (2.4)$$

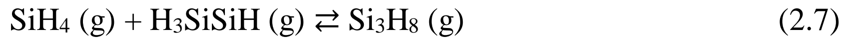
Polysilanes can dissociate resulting in the formation of substituted silylenes, such as:

$$Si_2H_6\ (g) \rightleftarrows H_3SiSiH\ (g) + H_2\ (g) \qquad (2.5)$$

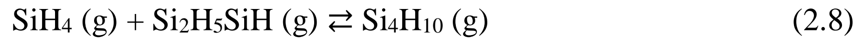


$$Si_3H_8\ (g) \rightleftarrows Si_2H_5SiH\ (g) + H_2\ (g) \qquad (2.6)$$

Substituted silylenes react with silane, producing again polysilanes like trisilane and tetrasilane:



$$SiH_4\ (g) + H_3SiSiH\ (g) \rightleftarrows Si_3H_8\ (g) \qquad (2.7)$$



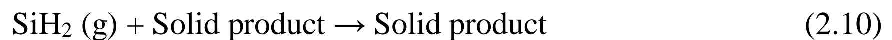
$$SiH_4\ (g) + Si_2H_5SiH\ (g) \rightleftarrows Si_4H_{10}\ (g) \qquad (2.8)$$

Also occurring simultaneously are reversible isomerization reactions of the silylenes:

$$H_3SiSiH\ (g) \rightleftarrows Si_2H_4\ (g) \qquad (2.9)$$

These homogeneous reactions in the gas phase are well known and thoroughly studied over the last decades [201], [207]–[211]. Contrarily, the elementary steps of silane heterogeneous decomposition on a solid silicon substrate are not fully understood, except for the growth of amorphous silicon films [201], [203]–[205]. There are several possible reactions when silane and other gaseous intermediates interact with the many dangling bonds of a silicon surface (-Si), thus operating conditions inside a CVD reactor determine the reactions probability and the gaseous species that contribute the most for the growth of solid silicon film.

In the case of existing unsaturated intermediates, such as silylenes, they play a substantial role in the formation of a solid product [208]:



$$SiH_2\ (g) + \text{Solid product} \rightarrow \text{Solid product} \qquad (2.10)$$

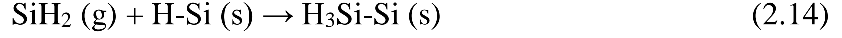
$$H_3SiSiH\ (g) + \text{Solid product} \rightarrow \text{Solid product} \qquad (2.11)$$

The dangling bonds on amorphous and powder-like substrates are usually filled with hydrogen due to the strong Si-H bond, however the breaking of one or two bonds leads to silane adsorption and decomposition according to the following equations, respectively [205]:

$$SiH_4\ (g) + \text{-}Si\ (s) \rightarrow H\ (g) + H_3Si\text{-}Si\ (s) \qquad (2.12)$$

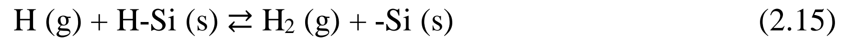
$$SiH_4\ (g) + H\text{-}Si\ (s) \rightarrow H_2\ (g) + H_3Si\text{-}Si\ (s) \quad (2.13)$$

Reaction (2.12) is more likely than reaction (2.13) because only one Si-H bond has to be broken resulting in a lower activation energy. It is also possible that the adsorption of SiH_2 causes the breakage of one Si-H bond [203]:



$$SiH_2\ (g) + H\text{-}Si\ (s) \rightarrow H_3Si\text{-}Si\ (s) \quad (2.14)$$

The hydrogen atom released in reaction (2.12) can break a Si-H bond in the growing solid surface, freeing a silicon dangling bond, nevertheless, it is a reversible reaction, since molecular hydrogen can also be adsorbed onto the surface [205]:



$$H\ (g) + H\text{-}Si\ (s) \rightleftarrows H_2\ (g) + \text{-}Si\ (s) \quad (2.15)$$

Reactions between surface H-Si bonds result in H_2 desorption to the gas phase [203]:

$$H\text{-}Si\ (s) + H\text{-}Si\ (s) \rightarrow Si\text{-}Si\ (s) + H_2\ (g) \quad (2.16)$$

Silicon growth in the SDS-CVD reactor is achieved by heterogeneous reactions (2.10) to (2.14) while reactions (2.15) and (2.16) only contribute to surface Si-H bonds reorganization by H_2 desorption.

2.3.3. Growth Rate

The local growth rate of silicon, in a horizontal cold wall reactor using silane as gas source and hydrogen as a carrier gas, is given by the expression [212]:

$$G(x) = \frac{AP_0}{T_s(R_1 + R_2)} \exp\left(\frac{-T_0 x}{v_0 T_s b(R_1 + R_2)}\right) \quad (2.17)$$

where $G(x)$ is the silicon growth rate along the x-axis, A is a reactor constant, P_0 the silane input pressure, T_s the substrate temperature, T_0 the room temperature, v_0 is the mean gas velocity at room temperature, b the free height above the susceptor, R_1 and R_2 are the diffusion and transfer resistances, given by the expressions:

$$R_1 = \frac{\delta T_0^2 \ln(T_s/T_b)}{D_{12} T_s (T_s - T_b)} \quad (2.18)$$

$$R_2 = \frac{1}{k_d} \quad (2.19)$$

where δ is the thickness of the diffusion boundary layer, D_{12} the binary diffusion coefficient of the reactant in the carrier gas at room temperature, T_b the bulk gas temperature and k_d the mass transfer coefficient.

At low temperatures (< 1000 K), k_d is small and so the concentration gradient on the boundary layer is negligible. In these circumstances, the silicon growth rate is limited by the chemical kinetics on the silicon surface ($R_2 \gg R_1$) and with $k_d = k_d^0 \exp(-\Delta E/RT)$, equation (2.17) can be rewritten as:

$$G(x) = G_0 \exp(-\Delta E/RT) \tag{2.20}$$

where $G_0 = AP_0k_0/T_s$ is a constant factor and ΔE is the activation energy for silane pyrolysis in hydrogen at atmospheric pressure. At high temperatures (> 1000 K), surface reaction rate increases to an extent where the gas phase diffusion of silane towards the surface turns into the limiting step ($R_1 \gg R_2$). This regime is outside the operating range of the SDS-CVD reactor and thus not worth further analysis.

The total pressure of the gas mixture and the carrier gas used (either hydrogen or inert gases such as helium, nitrogen or argon) also influences the silicon growth rate. Assuming that equation (2.17) is also valid for inert carrier gases at atmospheric or lower pressures, and based on several experimental data from cold wall CVD reactors, it is possible to draw the silicon growth rate as a function of temperature, from silane source in hydrogen or in inert ambient gas (both at atmospheric pressure) and for a reduced pressure of 10^{-2} bar, as shown in Figure 2.7.

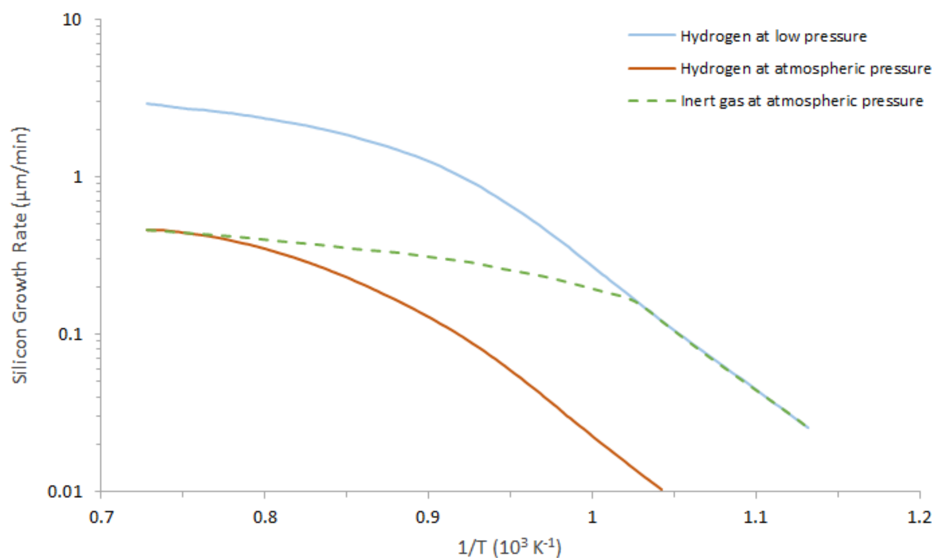


Figure 2.7 - Silicon growth rate from silane (at 10^{-3} bar of partial pressure) as a function of temperature for different carrier gases and total pressures [212].

The silicon growth rate in the gas phase diffusion-controlled regime (at high temperatures), is independent of the carrier gases and inversely proportional to the total pressure, since silane diffusion is easier at reduced pressures [212]–[214]. In the surface reaction-controlled regime (at low temperatures), the silicon growth rate is mostly influenced by the carrier gas: at atmospheric pressure, if an inert gas is used, the growth rate greatly increases when compared to the rate with hydrogen carrier, being similar to the case with hydrogen at low pressure as carrier gas [202], [215], [216]. It was also demonstrated that the silicon growth rate is proportional to the input concentration of silane, nevertheless the growth rate tends to flatten at higher concentrations due to the increase probability of homogenous nucleation in the gas flow [216]–[218]. The use of an inert gas as carrier increases the silicon growth rate, because with lower concentrations of hydrogen in the gas phase, reaction (2.15) equilibrium shifts in the forward direction, resulting in more Si-H surface bonds being broken, which leave -Si dangling bonds available for silicon deposition [201]. Silane as precursor gas also provides two main advantages over other precursors such as chlorosilanes ($SiCl_4$, $SiHCl_3$ or SiH_2Cl_2): for the same conditions the growth rate is higher for silane, both in low and high temperature regimes, because there is no etching effect caused by chlorine (corrosive when combined with hydrogen) [219], [220].

2.3.4. SDS-CVD Reactor

2.3.4.1. Overview

The current SDS-CVD reactor is the third generation of in-house developed reactors, designed to produce microcrystalline silicon pre-ribbons from silane. The first generation CVD reactor was a tubular quartz used to study the deposition parameters and ideal pre-ribbon growth conditions, while the second generation was an aluminium cylindrical reactor, which delivered the first pre-ribbons good enough to be recrystallized and used in solar cell manufacture [184]. Both previous reactors had cold walls and used optical systems comprised of halogen lamps and mirrors to generate heat for silane pyrolysis. The gaseous precursors were a mixture of silane and hydrogen and operated in batch mode with the powder bed being stationary below the heating region [180].

In order to overcome the major drawbacks of batch reactors, namely low throughput and deposition inhomogeneity, the current SDS-CVD reactor, previously developed and

characterized [181], is an inline optical system, with a movable substrate, capable of continuous operation. A schematic of the SDS-CVD reactor concept is presented in Figure 2.8(a).

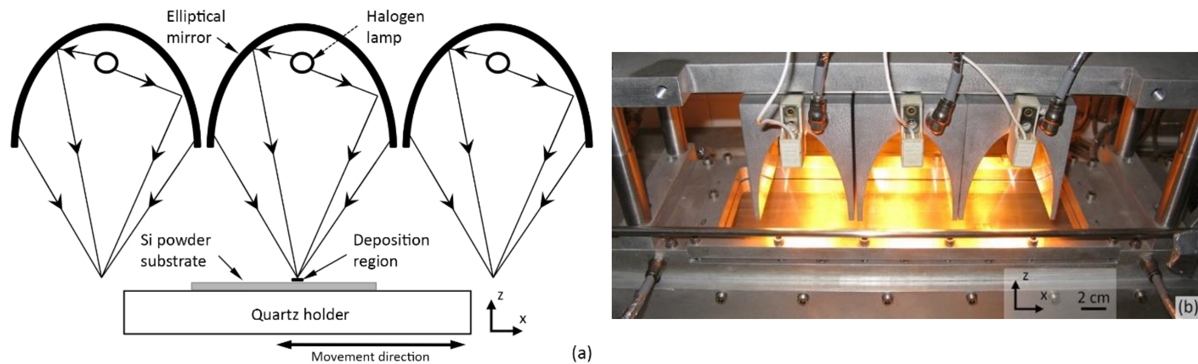


Figure 2.8 - SDS-CVD reactor: (a) schematic of the reactor concept; and (b) photo of the reactor.

The cold-wall reactor is made in aluminium, has a top 300×90 mm^2 clear quartz window and internal dimensions of 700 mm long, 90 mm width and 65 mm high. Focused radiation from three elliptical mirrors with tubular halogen lamps of 1000 W each, passes through the quartz window, creating three heating regions where deposition occurs. Each deposition region is 75 mm distanced apart from the closest one, measures 2 mm wide (x direction) and 90 mm long (y direction), being a well-defined hot band with a constant temperature. A photo of the actual SDS-CVD reactor is shown in Figure 2.8(b).

Improvement of deposition homogeneity is achieved by two major changes from past reactors: (i) the moving substrate holder which forces all regions of the substrate to undergo the same deposition conditions along the displacement direction; and (ii) elliptical mirrors wide enough to ensure a uniform radiation profile along the direction perpendicular to the substrate movement.

Higher throughput is in part accomplished by the continuous nature of the deposition, since the substrate can cross the three deposition regions as many times as desired without the need to open the reactor for maintenance or preparation procedures. Additionally, growth rate also contributes for a higher throughput, as previous reactors reached a maximum value of 6 μm/min [221], while the design and operation conditions of the current SDS-CVD reactor allowed for a growth rate increase over ten times, up to 90 μm/min [222]. This growth rate gain is attained by two factors: (i) the addition of an inert carrier gas (in this case argon) to the gas phase; and (ii) the heating regions geometry creates well-defined convection flow cells, which are responsible for increasing the striking rate of gaseous reactants with the substrate [222], [223].

2.3.4.2. Optical Characterization

The key component of the optical system is the set of three aluminium elliptical mirrors, each one focusing the radiation of a 1000 W tubular halogen lamp. All three mirrors have the same optical properties, with a focal distance of 72.5 mm, ellipse semi-axes of 80.5 mm and 35.0 mm, and an optical efficiency of 65.4% [181].

The radiation intensity distribution, along the x and y directions (according to the coordinate system in Figure 2.8(a)), were thoroughly described in a previous work [224] and are briefly presented here. Along the y direction it is assumed a lamp filament with a uniform temperature, a cylindrical shape of radius R and length L and the distance to the substrate is much greater than the filament radius ($R \ll D$). A schematic of the filament and the sample, seen from the yz plane, is presented in Figure 2.9. The radiation in each point of the substrate is the integral of the radiation from the whole filament length. Therefore, the integral value varies along the y direction, because of a different substrate view angle to the filament.

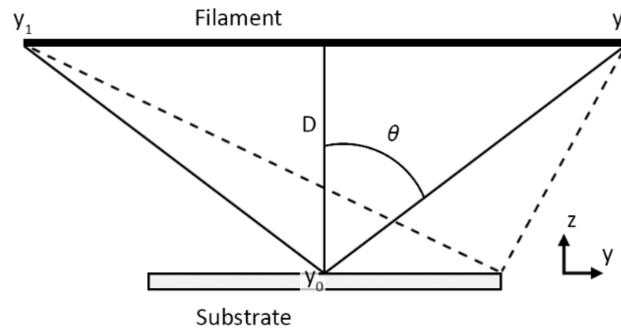


Figure 2.9 - yz plane view of the lamp filament and substrate.

In the general case of radiation emitted $\mathrm{d}P$, by a surface element $\mathrm{d}A_i$ and received by a surface element $\mathrm{d}A_k$, the relation can be written as:

$$\mathrm{d}P = I_0 \mathrm{d}A_i \cos\theta_i \,\mathrm{d}\omega \tag{2.21}$$

where $\mathrm{d}\omega$ is the solid angle which $\mathrm{d}A_i$ sees $\mathrm{d}A_k$ and I_0 is the radiation emitted by $\mathrm{d}A_i$ per unit area in a given direction per unit of solid angle. The solid angle element can be written as:

$$\mathrm{d}\omega = \frac{\mathrm{d}A_k \cos\theta_k}{r^2} \tag{2.22}$$

where r is the distance between the two surfaces. The total radiation received on the surface with area A_k is:

$$P_{i\to k} = \int_{A_i}\int_{A_k} \frac{I_0 \cos^2\theta}{r^2} \mathrm{d}A_k \mathrm{d}A_i \tag{2.23}$$

Regarding the particular case of the filament and accordingly with Figure 2.9, the following relations are valid:

$$\theta = \tan^{-1}\left(\frac{y - y_0}{D}\right) \tag{2.24}$$

$$\mathrm{d}A_i = 2\pi R \mathrm{d}y \tag{2.25}$$

The total radiation from the whole filament incident on the substrate per unit of area is:

$$E_{i\to k} = \int_{y_1}^{y_2} 2\pi R I_0 \frac{D^2}{[D^2 + (y - y_0)^2]^2} \mathrm{d}y \tag{2.26}$$

Integrating (2.26) gives the radiation intensity distribution, along the y direction:

$$\begin{aligned} E(y_0) = \frac{I_0 \pi R}{D}\Bigg[\tan^{-1}\left(\frac{y_2 - y_0}{D}\right) - \tan^{-1}\left(\frac{y_1 - y_0}{D}\right) + \cdots \\ + D\left(\frac{y_2 - y_0}{D^2 + (y_2 - y_0)^2} - \frac{y_1 - y_0}{D^2 + (y_1 - y_0)^2}\right)\Bigg] \end{aligned} \tag{2.27}$$

The value of I_0 constant is obtained by considering a cylinder of radius D with infinite length, hence the incident power on its surface must be equal to the power radiated by the lamp filament:

$$P_{cylinder} = \int_{-\infty}^{+\infty} 2\pi D E(y_0) \mathrm{d}y_0 = P_{lamp} \;\Leftrightarrow\; I_0 = \frac{P_{lamp}}{4\pi^3 R D} \tag{2.28}$$

According to equation (2.27), the halogen lamp with an 80 mm long filament has a symmetrical radiation intensity profile about the y_0 point, being flat for 20 mm on each side of y_0 and then quickly decreasing as it approaches the filament ends. Since the silicon pre-ribbon obtained by the SDS-CVD reactor has a width lower than 40 mm, deposition homogeneity along the y direction is successfully guaranteed.

Along the x direction, the global incident power P_g on a given substrate point is the sum of two terms:

$$P_g = P_{dif} + P_{foc} \tag{2.29}$$

where P_{dif} is the diffuse component (radiation that is not reflected by the mirror and directly reaches the substrate) and P_{foc} is the reflected and focused radiation by the mirror. Figure 2.10 presents a schematic of the filament and the sample, seen from the xz plane.

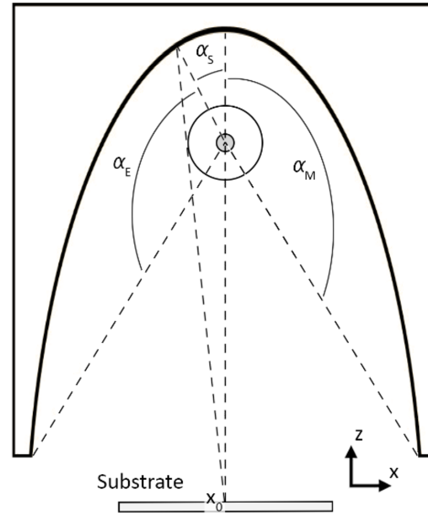


Figure 2.10 - xz plane view of the lamp filament and substrate.

Assuming an infinite length filament, emitting a power per unit of length P_{lamp}/L, the focused radiation component can be approximated by a gaussian distribution [224]:

$$P_{foc} = \frac{P_{lamp}}{\sqrt{2\pi} w_0 L} \exp\left(-\frac{x^2}{2w_0^2}\right) \tag{2.30}$$

where w_0 is the distribution width, representing the x coordinate where the power drops to $1/\sqrt{e}$ of the maximum power value. The diffuse component is given by [224]:

$$P_{diff} = \frac{P_{lamp}}{2\pi D L} \frac{1}{1 + \left(\frac{x - x_0}{D}\right)} \tag{2.31}$$

The focused and diffuse radiation components of equation (2.29) need to have a weighting factor to express their actual relative contribution to the total radiation power, which depends on the geometric properties of the mirror and lamp. Based on Figure 2.10, the geometric efficiency of the mirror is the ratio between the effective focus angle α_E and the total angle $\alpha_T = 180°$:

$$\eta = \frac{\alpha_E}{\alpha_T} = \frac{\alpha_M - \alpha_S}{180} \tag{2.32}$$

Therefore, it is possible to write the power components solely based on geometric factors:

$$P_{diff} = (1-\eta)\frac{P_{lamp}}{L} \qquad \text{and} \qquad P_{foc} = \eta\frac{P_{lamp}}{L} \tag{2.33}$$

which also gives the P_{diff}/P_{foc} ratio:

$$\frac{P_{diff}}{P_{foc}} = \frac{180-\alpha_E}{\alpha_E} = \frac{1-\eta}{\eta} \tag{2.34}$$

The elliptical mirror and halogen lamp configuration in the SDS-CVD optical system, has an effective focus angle of $\alpha_E = \alpha_M - \alpha_S = 154.2° - 36.5° = 117.7°$, which results in a geometric efficiency of $\eta = 65.4\%$ and a diffuse to focus power ratio of $P_{diff}/P_{foc} = 0.529$. Based on equations (2.30) and (2.31) the diffuse component is practically constant along the x direction within a 30 mm range around x_0 point, while the focused component radiation profile rapidly falls as it moves away from the x_0 point.

The radiation intensity distribution over the substrate was also studied using a ray tracing software. While the two-dimensional analytical model described, only accounts for in-plane radiation from the filament and mirror, a three-dimensional ray tracing model can include the contribution from other sources, such as diffused radiation reflected in the reactor aluminium walls. The following parameters were used to model the radiation behaviour: (i) the mirror surface is an aluminium coated film, having an average reflection coefficient of 0.95 and no scattering; (ii) the reactor material is unpolished aluminium with an average reflection coefficient of 0.60 and a gaussian scattering model; (iii) the number of analysis rays is 2×10^6 for each lamp filament; and (iv) the target detector is a 300×60 mm rectangle with a 100% absorption rate, placed in the same z axis position as the powder substrate.

Figure 2.11 presents the ray tracing simulation results obtained. Figure 2.11(a) shows the normalized radiation intensity map in the xy plane at a vertical distance from the lamp filaments of two times the mirror focal distance, while Figure 2.11(b) shows the normalized radiation intensity profile along the x coordinate at $y = 0$, compared with the two-dimensional analytical model from equations (2.30), (2.31) and (2.34). Figure 2.11(c) shows the normalized radiation intensity profile along the y coordinate at $x = 0$, for two different cases: ray tracing simulation only with the optical system and ray tracing simulation with the optical system and the whole reactor encase.

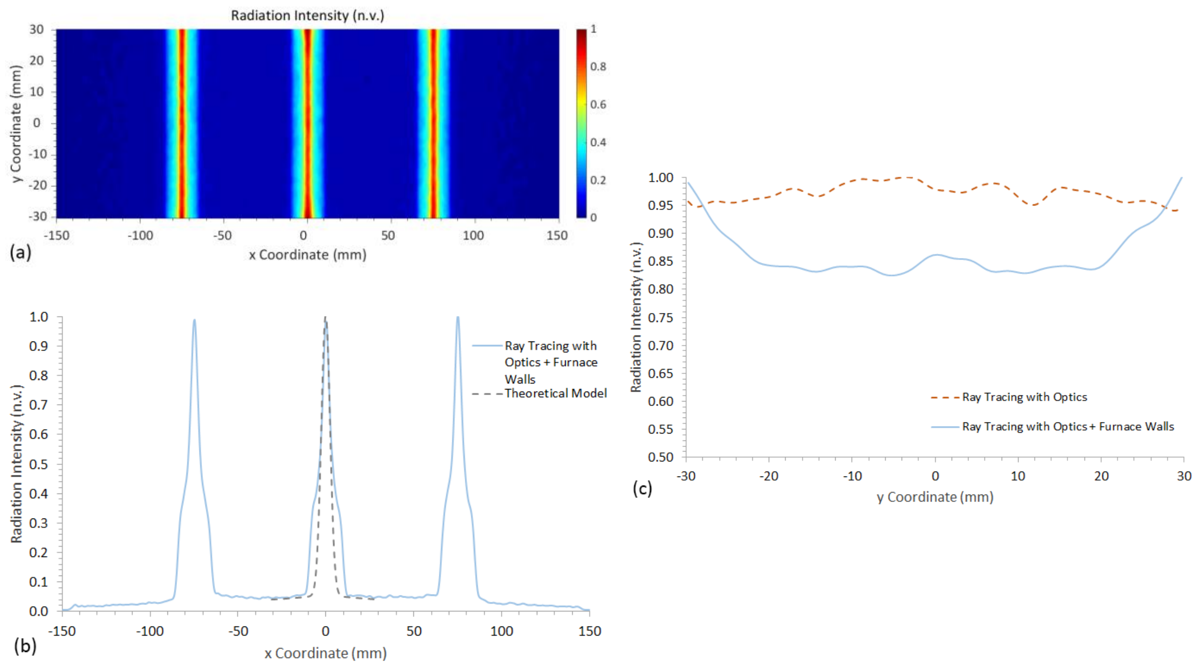


Figure 2.11 - Normalized radiation intensity, over the substrate inside the SDS-CVD reactor, obtained by ray tracing simulation: (a) intensity map in the xy plane; (b) profile along the x coordinate; and (c) profile along the y coordinate.

The radiation intensity map in the xy plane, as well as the radiation intensity profile along the x coordinate, show the expected three intensity peaks due to focused radiation from the elliptical mirrors, with values higher than $1/\sqrt{e}$ being located in a 5.0 mm narrow region that extends across the y direction. The theoretical intensity profile along the x coordinate was plotted, against the ray tracing simulation results, with a distribution width of 25 mm for the focused radiation component given by equation (2.30), and a diffuse to focus power ratio of 0.529. The theoretical model gives a good fit of the normalized intensity values above 0.5 but underestimates the intensity profile for values bellow it. The radiation intensity profile along the y coordinate evidences the influence of the reactor encase, which reflects radiation that otherwise would not have reached the xy plane: while ray tracing results considering only the optical system show a nearly flat intensity profile across a 60 mm length, the addition of the reactor encase produces an intensity profile that is flat in a 40 mm central region, but increases from 0.85 to 1.0 at both 10 mm regions closer to the reactor walls. Nevertheless, the simulation results prove that, for the dimensions of the silicon pre-ribbon (lower than 120×40 mm) obtained by the SDS-CVD reactor, deposition homogeneity either along the x or y directions is successfully assured.

2.3.4.3. Temperature Profile

The temperature on the substrate depends on several factors such as: (i) the input power on the halogen lamps; (ii) the substrate material; and (iii) the number of times a substrate crosses the heating regions.

Previous reactor characterization studies showed that the temperature of a stationary substrate placed in one radiation intensity peak, increases in the 400-950 K range for an equivalent increase in applied power (on each lamp) from 100 W to 900 W. It was also observed that for substrate materials like silicon powder, silicon pre-ribbon obtained after CVD or multicrystalline silicon, the temperature gap between these different substrate types, becomes more significant as the applied power increases. At around 700 W, the input power where deposition occurs, the temperature on the powder substrate is around 870 K, 30 K higher than in a pre-ribbon after CVD and 70 K higher than in multicrystalline silicon [181]. This behaviour is due to thermal conductivity which is lower for the powder substrate and due to a greater reflectivity of the multicrystalline silicon substrate.

The temperature profile along the x direction was measured with a type-K thermocouple attached to the back of a solid multicrystalline silicon substrate, using a low thermal conduction clay-based glue, as shown in Figure 2.12.

Figure 2.12 - Type-K thermocouple glued to the back surface of a multicrystalline silicon substrate.

The quartz holder where the substrate rests, was then moved at a constant speed of 10 mm/min and crossing the three radiation peaks several times. Figure 2.13 exhibits the temperature profile along the x coordinate at $y = 0$, for an input power of 700 W, plotted against the normalized radiation intensity profile obtained by ray tracing simulation.

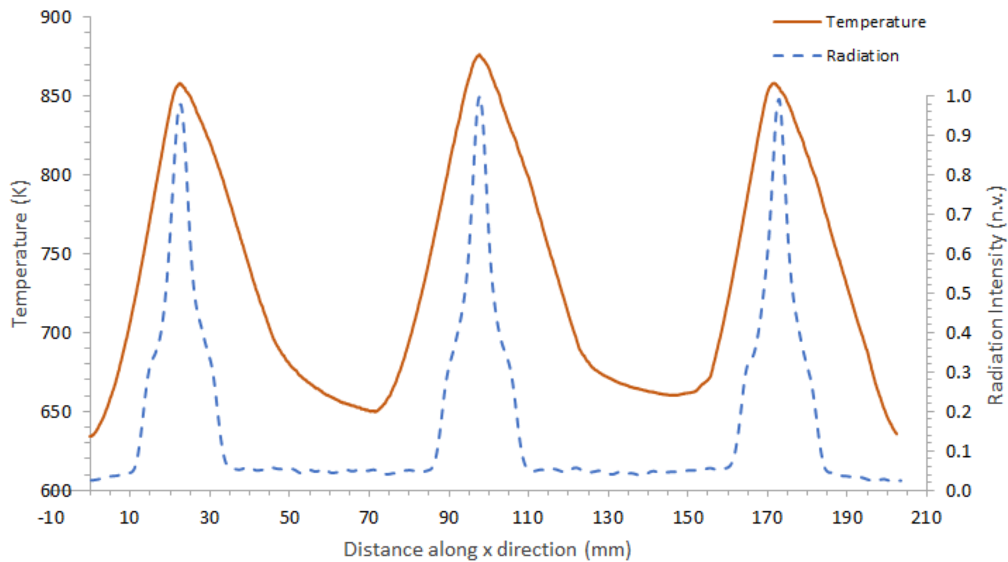


Figure 2.13 - Temperature profile along the x coordinate at the reactor centre, for an input power of 700 W, superimposed to the normalized radiation intensity profile obtained by ray tracing simulation.

Both temperature and radiation intensity profiles have maximum values at the same location and minimum value regions between them. Hence, the three heating regions are confined to an area around the radiation intensity peaks, although the temperature does not drop as sharply as the radiation intensity in the out of focus regions, with substrate temperatures varying within the 600-870 K range.

The dynamic nature of the reactor internal conditions, with a gas flow and a moving substrate, creates a slightly asymmetrical temperature profile, having different temperature values (although never greater than 5%) for regions with the same radiation intensity conditions. If temperature data is collected when moving the substrate from the gas inlet to the gas outlet, the temperature profile shows a value increase from the first to the last radiation peak, while in the opposite direction the same behaviour is also observed but in a lesser degree. This is an indication that heat transport is present and being assisted by the gas and the substrate. Both the gas and substrate contribute for the temperature increase when the substrate travels from the gas inlet to the gas outlet, but in the opposite direction the gas has a lower contribution since the flow direction is contrary to the substrate movement [181]. Collecting the temperature data after several travels, minimizes temperature profile asymmetries as the system tends to a thermal equilibrium.

The temperature profile along the y direction has a very small variation of 1 to 2% in a 60 mm length, thus not affecting deposition homogeneity.

2.3.4.4. Fluid Dynamics

The SDS-CVD reactor was designed to have a fluid dynamics pattern that improves the growth rate over past generation reactors [223], [225]. The flow pattern of a gas is determined by several factors, such as: gravitational field, temperature gradient, species concentration gradient and species velocity. These factors are dependent on each other and simultaneous influence the fluid dynamics inside the reactor, hence the complexity of the fluid dynamics behaviour was studied using computational fluid dynamics (CFD) simulation software.

The existence of three well-defined heating regions, confined to an area around the radiation intensity peaks, creates high temperatures gradients, that increase the gas velocity. Combined with the internal reactor geometry and a constant gas flow input, a steady flow circulation regime is achieved, in which several convection flow cells are present. Convection flow cells are advantageous as they boost growth rate by: (i) increasing the time reactants spend inside the reactor; (ii) efficiently carrying the reactants in close contact with the substrate surface (better diffusion); and (iii) increasing the striking rate of reactants with the substrate (higher adsorption probability).

The CFD model used for reactor characterization is based on finite element analysis that calculates the heat exchanges between the system and silicon sample by conductive, radiative, and convective phenomena. Calculations rely on Favre averaged Navier-Stokes and Newton law equations for convective, on Fourier law for conductive, and on discrete ray Monte-Carlo approach for radiative heat exchanges.

Previous CFD studies made during the design phase of the current SDS-CVD reactor [181], [225], proved that in a three-heating region configuration, a total of six cylindrical-shaped convection flow cells are obtained if the distance between the substrate surface and the top quartz window is half the distance between two consecutive heating regions (a 1/2 ratio). With a ratio lower than 1/2 the convection flow cells are distorted along the x direction, while for ratios higher than 1/2 the convection flow cells are elongated along the z direction. Thus, the SDS-CVD reactor has a 75 mm distance between consecutive heating regions and 40 mm of distance between the substrate surface and the top quartz window.

Figure 2.14 presents the results of the CFD simulations performed. Figure 2.14(a) shows the gas flow trajectories, while the gas velocity isolines and temperature isolines are shown in Figure 2.14(b) and Figure 2.14(c), respectively.

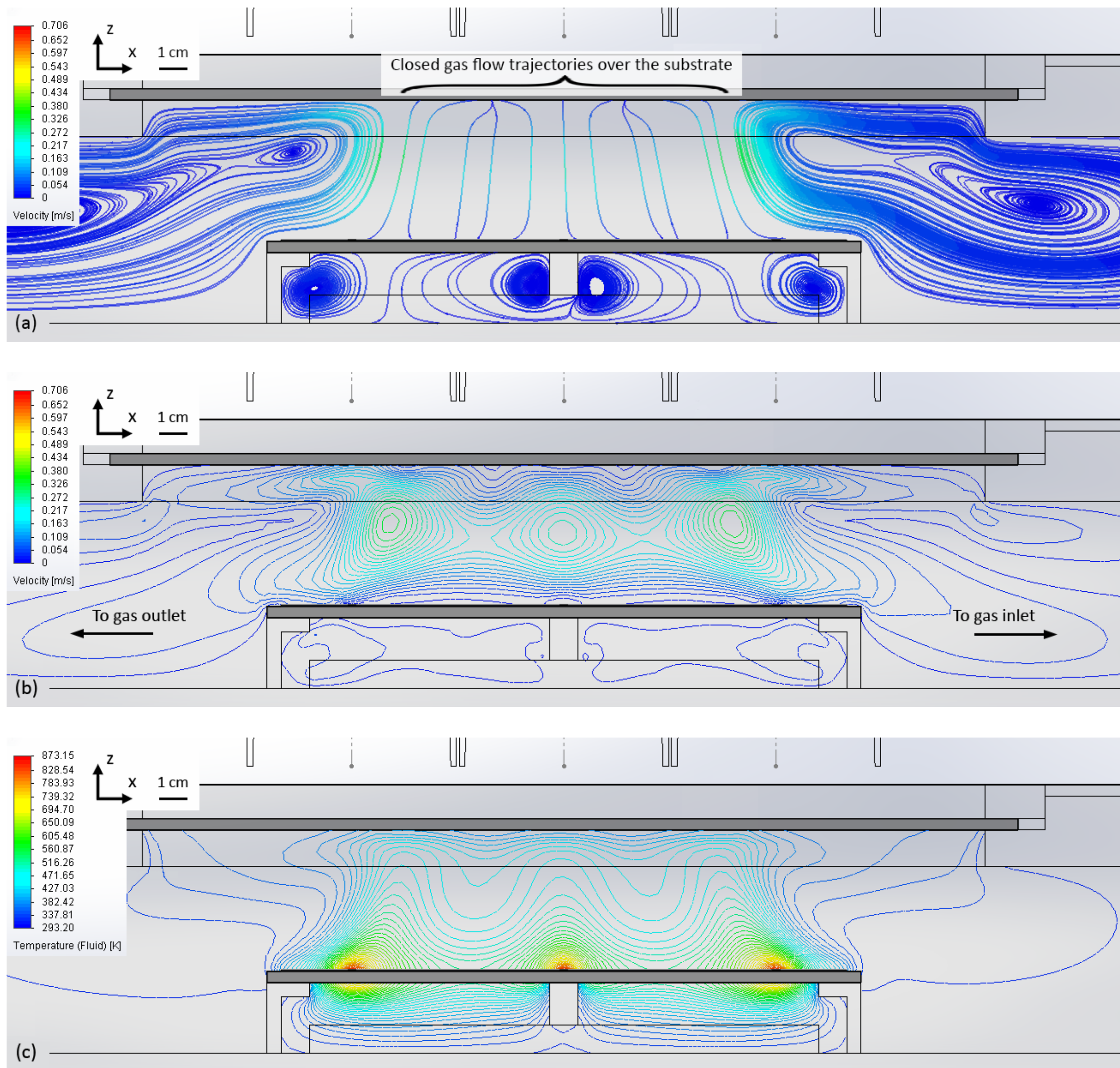


Figure 2.14 - Cross-section front view of the reactor interior, showing the results obtained by CFD simulation: (a) gas flow trajectories; (b) particle velocity isolines; and (c) gas temperature isolines.

The following simulation conditions were imposed: (i) room temperature of 293.15 K; (ii) gas mixture of argon (60 vol%) and hydrogen (40 vol%); (iii) constant input gas flow of 1 L/min, at room temperature and atmospheric pressure; (iv) reactor gas outlet kept at atmospheric pressure; and (v) temperature profile on the substrate along the x direction, like the one presented in Figure 2.13, with three heating regions at 873 K.

The fluid dynamics simulation results prove that the combination between reactor geometry and the heating regions arrangement favours a steady state flow circulation regime, characterized by the existence of clear-cut convection flow cells. These convection cells are responsible for closed gas flow trajectories over the substrate and circular shaped velocity

isolines (Figure 2.14(a) and Figure 2.14(b), respectively), thus increasing the time reactants spend in contact with the substrate.

2.3.4.5. Experimental Procedure

A typical CVD run starts with the preparation of the silicon powder substrate. Silicon powder obtained by the SDS-grinding mill (or from another source such as the nanometric powder from scraping wall deposited fines on a fluidized bed CVD reactor), is placed over a quartz substrate holder. The powder is then pressed with the help of a second quartz plate and shaped into a rectangular substrate, measuring up to 25×100 mm^2. The applied pressure on the powder serves to increase substrate homogeneity and decrease both substrate porosity and thickness which ideally should not be greater than 300 µm. Shaping the substrate into a rectangle is done using a piece of multicrystalline silicon wafer, to avoid contamination and preserve its structural integrity. The preparation of the silicon powder substrate is the most important step of the experimental procedure since the physical characteristics of the substrate will influence the quality of the silicon pre-ribbon produced by the SDS-CVD furnace, as it will be further discussed in section 3.2.2.

The quartz holder containing the silicon powder substrate is then placed over a moving car inside the reactor, which is closed and remains hermetically sealed during the whole deposition run. The reactor is initially purged with a constant argon flow of 1 L/min for 70 minutes, since silane is extremely flammable and pyrophoric when in contact with oxygen at room temperature. During the final period of the reactor purged stage, voltage is applied to the halogen lamps, being gradually raised until reaching the desired value in the 170-190 V range is reached, corresponding to an applied power per lamp of 660 to 750 W.

Deposition starts when the substrate edge is below the first heating region, as it starts moving at a constant speed of 10 mm/min and crossing the three heating regions several times, depending on the desired amount of silicon to be deposited. During this continuous operation of the reactor, the inner atmosphere is kept at a constant pressure of 1 atm, with a mixture of silane diluted in hydrogen and argon (60 vol% of argon, 36 vol% of hydrogen and 4 vol% of silane), flowing at a constant global rate of 1 L/min (0.6 L/min for argon and 0.4 L/min for silane diluted in 90% of hydrogen) [222]. This precise management of the reactor atmosphere is accomplished by a newly installed mass flow meter and controller system, capable of

monitoring and control the mass flow rate of each gaseous species entering the reactor. Table 2.2 summarizes the key deposition conditions during a typical CVD run.

Table 2.2 - Most important parameter values of a typical CVD run.

Argon Flow Rate (L/min)	Silane (10%) + Hydrogen (90%) Flow Rate (L/min)	Pressure (atm)	Electric Power per Lamp (W)	Substrate Moving Speed (mm/min)
0.6	0.4	1	660-750	10

After completing a deposition run, the moving car is stopped close to the reactor entrance, applied voltage is decreased to 0 V, silane and hydrogen flow is terminated, and the reactor is purged with a constant argon flow of 1 L/min for 70 minutes, after which is safe to take out the silicon pre-ribbon.

The current procedure, based on experimental runs from previous studies [181], delivers the most reliable results, nevertheless, a fundamental difference was introduced: the additional step between two consecutive depositions, in which the excess substrate powder was manually removed and the pre-ribbon placed again inside the reactor for a second CVD run, was eliminated from the present work. This choice turns the CVD process into a simpler and continuous step, requiring lower operator intervention and greatly reducing the process duration, which ultimately makes the SDS process closer to an industrial demonstration stage.

2.4. Zone Melting Recrystallization

2.4.1. Overview

The ZMR technique was introduced in the early 1950s [88] as crucible-free method for metal recrystallization, being followed by the development of experimental apparatus to grow silicon single crystals [89]. The developed technique showed three main advantages: (i) low energy input when compared to ingot or ribbon growth from a silicon melt, owing to the small molten zone volume; (ii) lower impurity presence due to the absence of contact of the molten silicon with foreign materials; and (iii) it acts as a purification stage, since metal impurities are continuously segregated to the molten zone and away from the solidifying crystal interface.

The FZ growth of cylindrical mono-crystalline silicon ingots with a diameter up to 200 mm, using inductive heating generated by a radiofrequency magnetic field is the most common and widely used method based on the vertical zone melting principle [91]. Nevertheless, multicrystalline silicon films and ribbons can also be grown by ZMR, either to avoid the wafering of large ingots or in applications that require the crystallization of deposited a-Si films.

In general, ZMR processes use two main modes of heating: dynamic and static. Dynamic mode can be further divided into two heating types: pulse modes (alternating in time) and movable modes (alternating in space). Finally, movable modes can be subdivided into two categories: an extended linear molten zone crossing a silicon substrate at relatively low velocities, within the 0.1-5 mm/sec range; and a small-spot molten zone scanning along the substrate at high velocities, up to several hundred centimetres per second. In static processes the entire substrate is preheated to a high temperature, close to the silicon melting point (in the 1100-1300 °C range), with rather long dwell times at the melting point of around $1\text{-}10^2$ seconds. Productivity and crystalline quality of the recrystallized films can be relatively high, and without experiencing intense temperature gradients during recrystallization. On the other hand, dynamic processes have a substrate preheated at lower temperatures (around 400-600 °C), with short dwell times at the melting point, in the $10^{-5}\text{-}10^{-1}$ seconds range. Thermal gradients in the film are strong due to a high concentration of energy in a small area, which can have a negative impact on the crystalline quality of the recrystallized material.

The ZMR technique has been successfully applied in the production of silicon films and ribbons, and solar cells made with substrates processed by ZMR have also been developed. Different sources of energy can be used (single used or in combination) to create a molten zone: strip heaters, laser beams, electron or ion beams, radio-frequency heaters and incoherent-light sources [226].

Strip-heater systems consist of a lower broad immovable heater and an upper long and narrow movable strip-heater, both in graphite and with a large current passing through, recrystallizing the silicon material placed between them [227], [228]; thin film polycrystalline silicon solar cells, measuring up to 10×10 cm^2 and reaching efficiencies in the 14.2% to 16% range, were prepared using chemical vapour deposited silicon thin films over a SiO_2 layer and further recrystallized by zone melting using a strip-heater system [229], [230].

Laser beam techniques have been used for processing silicon, employing a wide range of laser types, operating both in pulsed and continuous modes [231]; using short pulse lasers, a-Si films

deposited by high rate electron beam evaporation on glass or polymer substrates have been laser crystallized, to produce a multicrystalline silicon film with grains ranging from 10 nm to about 1 µm in size [232]; solar cells made with these films achieved a conversion efficiency of 4.8% without light trapping [233].

Electron beam sources, like lasers, can scan at high velocities along the surface film to be recrystalized and deliver a high power density, nevertheless, they require a vacuum environment. The electron beam can be a line-shaped beam, usually 20-40 mm long and 0.1-1 mm wide operating in pulsed mode (typically 1-10 ms in duration) [234] or a pseudo-line-shaped beam in which a spot electron beam is sinusoidally oscillated in one direction at a high frequency (typically 1 kHz to 50 MHz), simulating an actual line source [235]; electron-beam-crystallization [236] of amorphous and nanocrystalline silicon layers deposited over a SiC:B layer covering a glass substrate, resulted in a large-grained (1×10 mm^2) polycrystalline silicon layer used as absorber in thin film hetero-emitter solar cells, reaching conversion efficiencies up to 4.7% [237].

Radiofrequency heating techniques, common in semiconductor industry, can also be used for ZMR applications and in this case, their implementation becomes rather similar to strip-heater systems, since the heating sources are graphite susceptors heated by a RF-coil; films recrystallized with this technique were not used for solar cell processing [238], [239].

Incoherent-light sources such as incandescent lamps are commonly used in ZMR applications, especially linear halogen lamps, typically of 1-2 kW power, 8-15 mm in diameter and 80-250 mm long. Two different approaches of the heating system can be implemented, one is to uniformly maintain the entire film at high temperatures (around 1000-1300 °C) using a set of several linear halogen lamps along the film movement, combined with an elliptical reflector to focus radiation in a narrow molten region [240], and a second approach is having two elliptical reflectors on both sides of the film, focusing each lamp radiation on a narrow molten region, about 1-2 mm wide [241]; coarse grained silicon sheets were obtained by ZMR of silicon powder thin layers (a process named silicon sheets from powder), followed by epitaxial growth of an active silicon layer and further processing into crystalline silicon thin-film solar cells, resulting in solar cell efficiencies up to 13.1% [242]–[244].

Table 2.3 compares several characteristics of the silicon ribbons after ZMR, using different types of heat sources [226].

Table 2.3 - Qualitative comparison of silicon ribbons characteristics after ZMR by different heat sources.

Heat Source	Graphite Strip	Laser Beam	Electron Beam	Incoherent-Light[a]
Temperature Gradient	Low	High	High	Low to High
Grain Size	mm-cm	µm-mm	µm-mm	mm-cm
Defect Density	Medium	High	High	Medium to High
Film Contamination	Carbon and Oxygen	Oxygen	Oxygen	Oxygen
Investment Costs	Low	High	Very High	Low

[a] On incoherent light sources, temperature gradient and defect density depend on the type of optical system used: maintaining the entire film at high temperatures will result in a lower temperature gradient and thus a lower defect density when compared to a system that concentrates the entire radiation on a narrow molten region.

2.4.2. ZMR Principles

2.4.2.1. Impurity Segregation

When an entire melted material progressively solidifies from one end, a process known as normal freezing, there usually will be a segregation mechanism that concentrates any solute species in one of the ingot ends. A key parameter is the distribution (or segregation) coefficient, denoted by k, and defined as the ratio of the solute concentration in the solid to that in the liquid at equilibrium. The segregation caused due to normal freezing can be expressed by the following equation [88]:

$$C = kC_0(1-g)^{k-1} \tag{2.35}$$

where C is the solute concentration in the solid, g is the fraction which has solidified and C_0 is the initial solute concentration in the melt. Equation (2.35) is valid under the following conditions: (i) diffusion in the solid is negligible; (ii) diffusion in the liquid is complete; and (iii) the value of k is constant. These set of conditions are achievable by having a freezing rate large enough when compared to the solute's diffusion rate in the solid but yet small compared to the diffusion rate in the liquid [245]. The segregation process is particularly efficient when k is small (lower than 0.1) and diffusion in the solid is limited.

Opposed to normal freezing, in zone melting recrystallization only a small molten zone of length l, much smaller than the total length L of the ingot or ribbon to be recrystallized, slowly

travels across the whole solid material, redistributing the solutes within the solid. The advancing molten zone has two solid-liquid interfaces, as one layer $\mathrm{d}x$ freezes into a solid, a second layer $\mathrm{d}x$ is being melted from the ingot (or ribbon). The first solid layer to freeze has a concentration of kC_0, where C_0 is the average solute concentration before zone melting, and in the case of $k < 1$, kC_0 is lower than C_0, meaning that the liquid phase is enriched by the soluble impurity. The molten zone progression causes a continuous enrichment of the liquid, although at a decreasing rate, until it reaches a concentration of C_0/k, after which the concentrations of impurities entering and leaving the zone are equal and resulting in a constant concentration of C_0 in the remaining freezing solid. The behaviour of impurity concentration C, in a single pass zone melting recrystallization is expressed by equation (2.36), which is usually valid for 90% of the initial length of the solid while in the last part normal freezing prevails [88], [245]:

$$C/C_0 = 1 - (1 - k)\exp(-kx/l) \tag{2.36}$$

where x is the length of solidified material, measured from the starting end. As in normal freezing, impurity segregation from the solidifying solid to the liquid phase (when $k < 1$) is also present, although a lower degree of purification is achieved by one zone pass than by one normal freezing step.

2.4.2.2. Thermal Stress

The linear thermal expansion coefficient α, describes the change in length l of a material due to a temperature change, and is defined by:

$$\alpha = \frac{1}{l}\frac{\partial l}{\partial T} \tag{2.37}$$

For an initial temperature T_0 and length l_0, the length at a temperature T is:

$$l(T) = l_0 \exp\left(\int_{T_0}^{T} \alpha(T)\,\mathrm{d}T\right) \tag{2.38}$$

In the case where α is independent of temperature, equation (2.38) reduces to an exponential function that can be expanded in a series and truncated at its second order term, yielding:

$$l(T) = l_0 \exp[\alpha_0(T - T_0)] = l_0[1 + \bar{\alpha}(T - T_0)] \tag{2.39}$$

where $\bar{\alpha}$ is the mean thermal expansion coefficient, usually listed in literature. If the $\alpha(T)$ coefficient is temperature dependent, it can be approximated by a polynomial expression:

$$\alpha(T) = a_0 + a_1 T + a_2 T^{-2} \tag{2.40}$$

where a_0, a_1 and a_2 are constants determined by fitting the experimental data [246].

During crystal growth, the ribbon thermal expansion and contraction, as well as the time-dependent temperature profile, play an important influence on: (i) the thermal induced stress; (ii) the period of time during which thermal stresses are able to relax plastically; and (iii) the eventual formation of cracks in the cooling phase. Above the brittle-ductile transition temperature of silicon (which is between 775 to 1275 K), lattice stresses are able to partly or totally relax by plastic deformation, such as in-plane and out-of-plane creep or bending and the formation of dislocations. Below this temperature, the ribbon incorporates the remaining thermal induced stresses. The magnitude of thermal stresses present in the final ribbon, recrystallized by a molten zone travelling at a constant speed, is proportional to the thermal gradients during the cooling process, particularly the second derivative of the temperature profile ($\mathrm{d}^2 T/\mathrm{d}x^2$). A second order thermal profile ($\mathrm{d}^2 T/\mathrm{d}x^2 \neq 0$) will result in a non-linear thermal expansion, thus across the ribbon thickness, unique infinitesimal layers will have different variations of thickness that can only be accommodated into a final homogenous ribbon by stressing the lattice [247], [248].

2.4.3. SDS-ZMR Reactor

2.4.3.1. Overview

The current SDS-ZMR reactor is the fifth iteration of in-house developed reactors, built to perform zone melting recrystallization in silicon ribbons, using focused incoherent-light as heat source. The first ZMR experiments were conducted in a system comprised of two 150 W halogen lamps with built-in elliptical reflectors, later evolving to a four lamp system. These two systems delivered a small molten zone area (up to 10 mm in length) and a recrystallized ribbon with uneven thickness, due to a non-uniform radiation profile on both two and four lamps systems. In a second generation reactor, two tubular halogen lamps with elliptical mirrors were used, allowing for a wider molten zone (from 20 to 30 mm in length), nevertheless, the close distance between lamps caused excessive system overheating. A third reactor implementation had an optical system with a total of six tubular halogen lamps, four lamps used with plane mirrors for ribbon pre-heating and two lamps on elliptical mirrors to focus the radiation, although it was not possible to control the atmosphere around the molten zone. Finally, the

fourth reactor was the most similar to the current one in terms of design and operating principle, giving an important contribute for the development of the current SDS-ZMR reactor using focused incoherent-light as heat source, which also benefited from the extensive know-how acquired in previous reactors to address the main shortcomings already identified [224]. A simplified schematic of the reactor concept is presented in Figure 2.15(a).

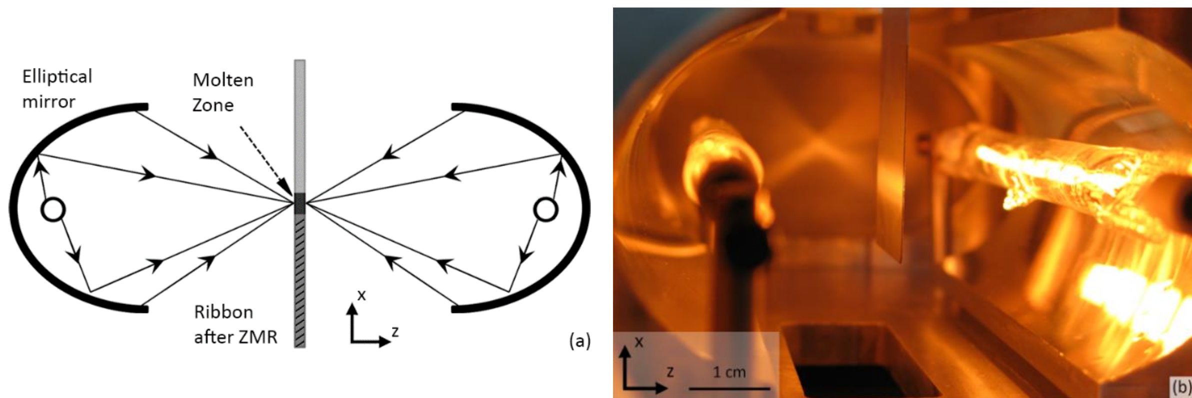


Figure 2.15 - SDS-ZMR reactor: (a) schematic of the reactor concept; and (b) close-up photo of the reactor interior.

The SDS-ZMR reactor, already developed and comprehensively tested, is built in aluminium and comprised of two parts: (i) the main body, which measures 220×140×76 mm^3 and contains the optical system with two elliptical mirrors and two tubular halogen lamps of 1000 W each; and (ii) the upper and lower chambers which allow the vertical displacement of the recrystallizing ribbon and facilitate system cooldown. Silicon pre-ribbons from the SDS-CVD reactor, measuring up to 40 mm wide, can be recrystallized by a stable molten zone traveling at a speed in the 1 to 10 mm/min range and under a controllable inner atmosphere.

The recrystallization process was improved over past reactors, as the current optical system creates a stable and uniform molten zone, for up to 40 mm wide (along the pre-ribbon length in the y direction) and 0.5 to 2.0 mm in height (x direction). Moreover, the reactor is airtight, being possible to control the flow rate and gaseous species, which reduces the chance of contamination. A close-up photo of the SDS-ZMR reactor interior is presented in Figure 2.15(b), showing the optical system and a silicon pre-ribbon with focused radiation over the surface.

2.4.3.2. Optical Characterization

The optical system, a crucial component of the reactor, creates two heating regions at the same height on both sides of the silicon pre-ribbon surface, melting the entire ribbon material on a

well-defined linear molten zone. The two mirrors have the same optical properties, with a focal distance of 30.6 mm and ellipse semi-axes of 39.9 mm and 25.5 mm. The halogen lamps are equal to the ones in the SDS-CVD reactor, having a glass tubular encase and an 80 mm long linear filament. Optical characterization methods, both analytical and ray tracing simulation are the same as used to describe the SDS-CVD optical system, which were thoroughly described in section 2.3.4.2.

In the SDS-ZMR reactor each elliptical mirror has an effective focus angle of $\alpha_E = \alpha_M - \alpha_S = 140.3° - 34.7° = 105.6°$, resulting in a geometric efficiency of $\eta = 58.7\%$ and a diffuse to focus power ratio of $P_{diff}/P_{foc} = 0.704$. The radiation intensity distribution over the pre-ribbon was computed with a ray tracing software, and the following parameters were used: (i) the mirror surface is an aluminium coated film, having an average reflection coefficient of 0.95 and no scattering; (ii) the reactor material is unpolished aluminium with an average reflection coefficient of 0.60 and a gaussian scattering model; (iii) the number of analysis rays is 2×10^6 for each lamp filament; and (iv) the target detector is a 60×30 mm rectangle with a 100% absorption rate, placed in the same z axis position as the pre-ribbon.

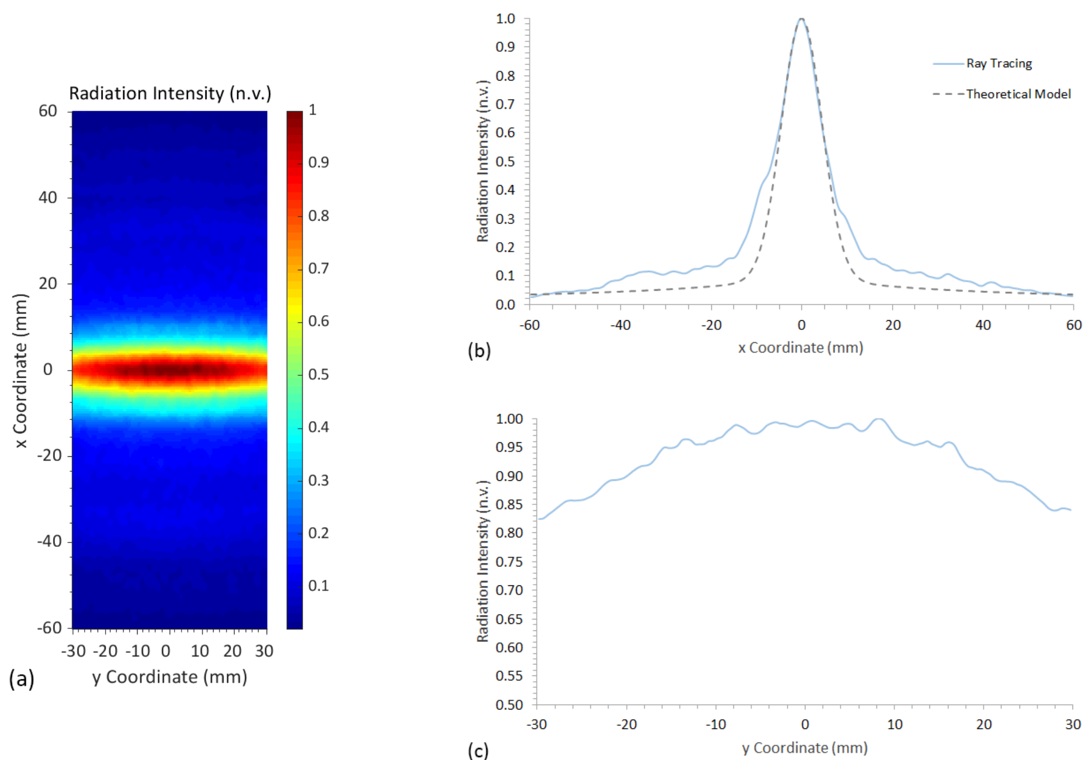


Figure 2.16 - Normalized radiation intensity, over the pre-ribbon inside the ZMR-CVD reactor, obtained by ray tracing simulation: (a) intensity map in the xy plane; (b) profile along the x coordinate; and (c) profile along the y coordinate.

Figure 2.16 shows the ray tracing simulation results obtained. Figure 2.16(a) presents the normalized radiation intensity map in the xy plane at the z coordinate where the pre-ribbon is placed. Figure 2.16(b) shows the normalized radiation intensity profile along the x coordinate at $y = 0$, compared with the two-dimensional analytical model from equations (2.30), (2.31) and (2.34) and Figure 2.16(c) shows the normalized radiation intensity profile along the y coordinate at $x = 0$.

Along the x direction there is an intensity peak due to focused radiation that progressively decreases as moving away from the focal origin point in x coordinate. Normalized intensity values higher than $1/\sqrt{e}$ are located within a 10.0 mm wide region. The theoretical model, as in the SDS-CVD optical characterization results, gives a good fit of the normalized intensity values above 0.5 but underestimates the intensity profile for values bellow it. Along the y direction the radiation profile in the focused area (at $x = 0$), uniformly extends for 40 mm, only decreasing to 0.90 at a distance of 20 mm away from the centre. These radiation profiles create a narrow linear heating region across the pre-ribbon width, as shown in the in the xy plane intensity map.

Compared to the SDS-CVD optical system, the SDS-ZMR reactor delivers a greater temperature, reaching the silicon melting point of 1683 K, because of two main factors: (i) the optical system is closer to the pre-ribbon surface; and (ii) the two coincident heating regions at the same volume of the pre-ribbon, results in an energy density twice as high. Moreover, the radiation profiles along x and y directions also have some noticeable differences: (i) the radiation profile along the x coordinate is wider, since it has a distribution width of 45 mm (the profile width at the point where the power drops to $1/\sqrt{e}$ of the maximum power value), almost twice the value for the SDS-CVD optical system; and (ii) the radiation profile along the y coordinate slightly decreases towards the edges, reaching a normalized intensity value of 0.83 at 30 mm away from the centre. Since recrystallized pre-ribbons are not wider than 40 mm, this radiation profile is adequate for the ZMR process.

2.4.3.3. Temperature Profile

The ribbon's temperature profile after recrystallization and while in the cooling stage, can provide valuable information on the extent of stresses present during crystal growth and in the final multicrystalline ribbon.

Previous studies calculated the ribbon's temperature profile, employing the same CFD model used to characterize the fluid dynamics in the SDS-CVD system (presented in section 2.3.4.4), and later validated with a thermocouple attached to a multicrystalline silicon sample [248]. Both cases, simulation and experimental validation, were conducted under equal circumstances: same power supplied to the halogen lamps to obtain a stable molten zone, an argon atmosphere feed to the reactor with a constant flow rate of 3 L/min at room temperature of 300 K, and a ribbon travelling at a constant speed of 2 mm/min. Figure 2.17 presents a graphical comparison of measured and simulation thermal profiles on a multicrystalline silicon sample (temperature as a function of molten zone distance) and also the second derivative ($\mathrm{d}^2T/\mathrm{d}x^2$) computed from the simulation temperature profile [248].

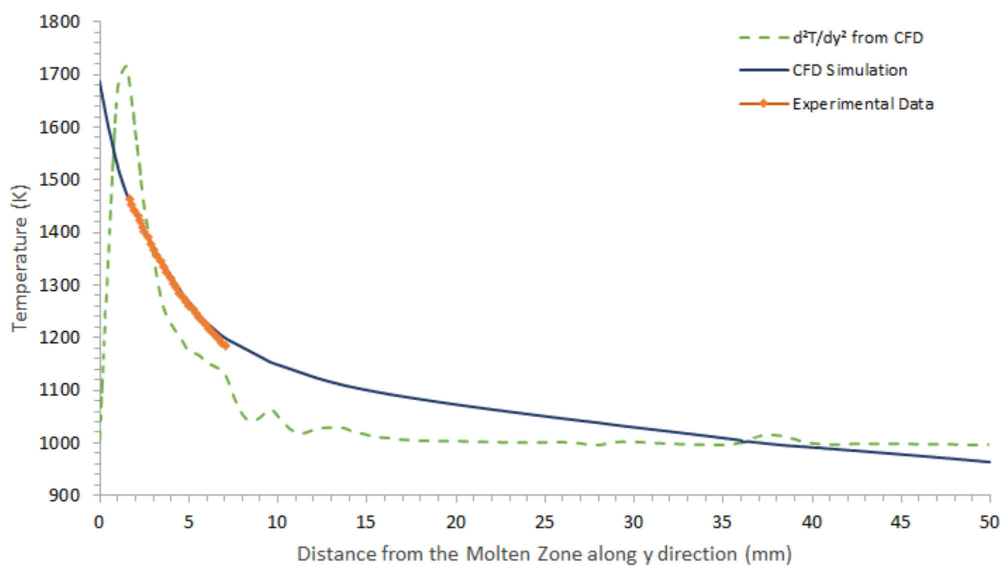


Figure 2.17 - Multicrystalline silicon sample thermal profiles (CFD simulation and experimental data) along the y direction [248].

The temperature gradient of the SDS-ZMR system is around 60 K/mm for 5 mm next to the molten zone. The thermal profile during the cooling stage results in a large value of $\mathrm{d}^2T/\mathrm{d}x^2$ near the molten zone, and rapidly decreasing in the first 10 mm away from it. These high values of $\mathrm{d}^2T/\mathrm{d}x^2$ while above the brittle-ductile transition temperature of silicon, are an indication that stresses could develop at the solid-liquid interface, resulting in plastic deformations such as dislocations. The measurement of thermally induced stress and dislocation etch-pit counting on silicon ribbons recrystallized by the reactor is explained in detail elsewhere [248].

2.4.3.4. Experimental Procedure

The preparation of the silicon pre-ribbon obtained after CVD is the first step of a typical ZMR run, consisting in two consecutive chemical baths to remove metallic and organic impurities, that might be present due to contamination occurring during pre-ribbon handling, after being taken out of the CVD reactor. The first bath is a CP4 etching solution [249], a mixture of nitric (HNO_3), acetic (CH_3COOH) and hydrofluoric (HF) acids in the 45:15:6 proportion, for 2 minutes, followed by an HF bath at 2 vol% for 1 minute. After each acid bath the pre-ribbon is rinsed with deionized water for 1 minute.

Access to the reactor interior is achieved by removing the upper chamber, thus exposing the ribbon motion mechanism, which contains a sample holder where the pre-ribbon is securely attached. The pre-ribbon is then lowered until its surface is illuminated by concentrated radiation, setting the input power value as low as possible, just enough to perform focus adjustments, as shown in Figure 2.15(b).

The reactor is re-assembled and closed, remaining hermetically sealed during the whole recrystallization run. After the initial reactor purge with a constant argon flow of 1 L/min for 20 minutes, the applied voltage to the halogen lamps is gradually increased, following a pre-defined heating ramp that minimizes pre-ribbon breaking probability and allows a more uniform heating: 10 V/2min in the [50; 80] V range, 5 V/2 min in the [80; 120] V range and 5 V/min from 120 V until a stable molten zone is obtained. The argon flow is also gradually increased and can reach 4-5 L/min during recrystallization. Increasing the argon flow favours the decrease of oxide content in the reactor atmosphere, as discussed in section 3.3.1.

When a stable molten zone is attained, usually within the 175-195 V range, the pre-ribbon starts moving downwards (or upwards if the molten zone begins at the other end of the pre-ribbon near the sample holder) at a constant speed in the 2-4 mm/min range, while the molten zone travels in the opposite direction recrystallizing the whole pre-ribbon into a multicrystalline silicon ribbon. Table 2.4 summarizes the key parameter values during a typical ZMR run.

Table 2.4 - Most important parameter values of a typical ZMR run.

Argon Flow Rate (L/min)	Pressure (atm)	Electric Power per Lamp (W)	Molten Zone Moving Speed (mm/min)
4-5	1	680-780	2-4

After a complete ribbon recrystallization, the moving sample holder is stopped, applied voltage is slowly and gradually decreased to avoid ribbon breakage, while the argon flow is reduced to 1 L/min, remaining at this set-point for more 15 minutes after voltage cut-off. When the reactor reaches room temperature, the silicon ribbon can be taken out and handled safely.

Chapter 3

Results

3.1. Silicon Powder

Silicon powder was obtained from multicrystalline p-type silicon wafers, through two mechanical processes: in the first step, 15×15 cm^2 and 240 μm thick silicon wafers were crushed by the SDS-crusher, resulting in an intermediate product with a particle size not greater than 2×2 mm^2, which is then fed into the SDS-grinding mill to deliver a finer silicon powder. Every SDS-grinding mill run was performed under the same experimental conditions: (i) fixed distance of 44.60 mm between the top cylinder and the base; (ii) constant feed rate of silicon at the top opening; and (iii) no re-feed of the silicon powder after being ground by the rotating ball and collected in the tray bellow (the input silicon sand-like product is only grinded once).

3.1.1. Size Distribution

The particle size of the produced powder by the SDS-grinding mill ranged approximately from 10 up to 300 µm, therefore a set of test sieves with mesh sizes of 25, 45, 75, 106, 180 and 250 µm, was used to separate the whole silicon powder in six powders of well-defined particle size intervals. Their visual appearance is shown in Figure 3.1.

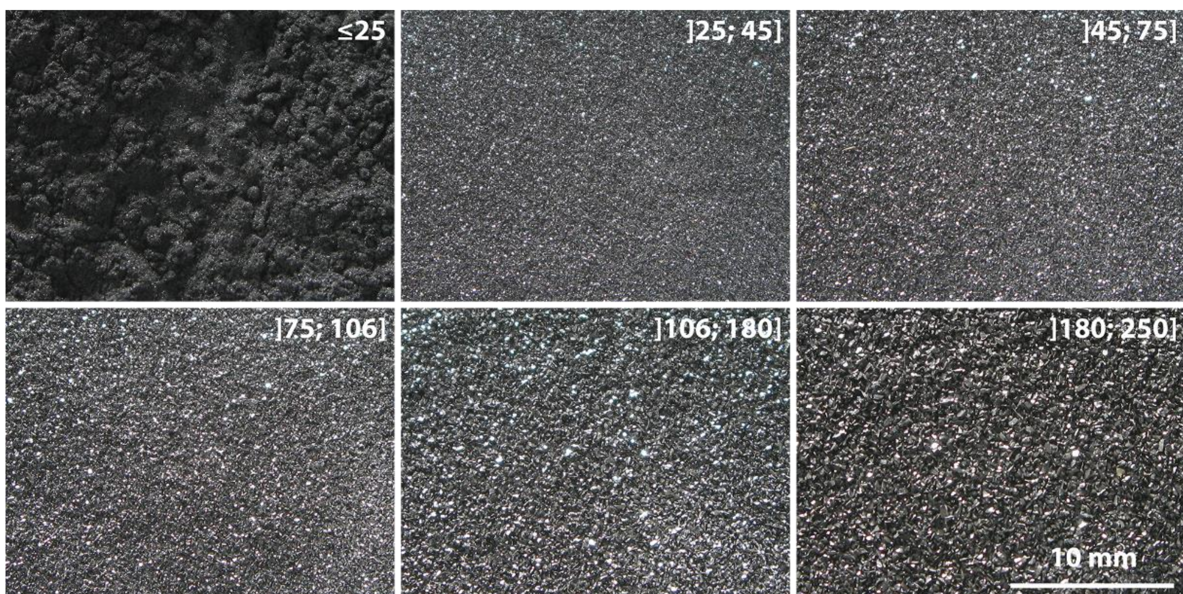


Figure 3.1 - Silicon powders of different granulometry. Particle size in µm.

Since the size calibrated powders came from multicrystalline p-type silicon wafers, they present a certain degree of crystallinity which becomes greater as the particle size increases. This fact is also noticeable to the naked eye, as lower particle size powders are darker and have a more dust-like appearance, while a more shinny and lighter grey appearance is progressively perceptible with the particle size increase. Regarding mechanical properties, finer powders are more compressible than coarser ones, nevertheless, while higher compressibility of the powder substrate may be advantageous for the CVD step, as it will be discussed in more detail in section 3.2.2, it also introduces some inconveniences such as powder being stickier, harder to handle and more prone to contamination.

The mass of each size calibrated powders was measured and normalized to the total mass of silicon wafers used for the powder production, resulting in a particle size distribution of the silicon powder produced by the SDS-grinding mill, which is presented in Figure 3.2.

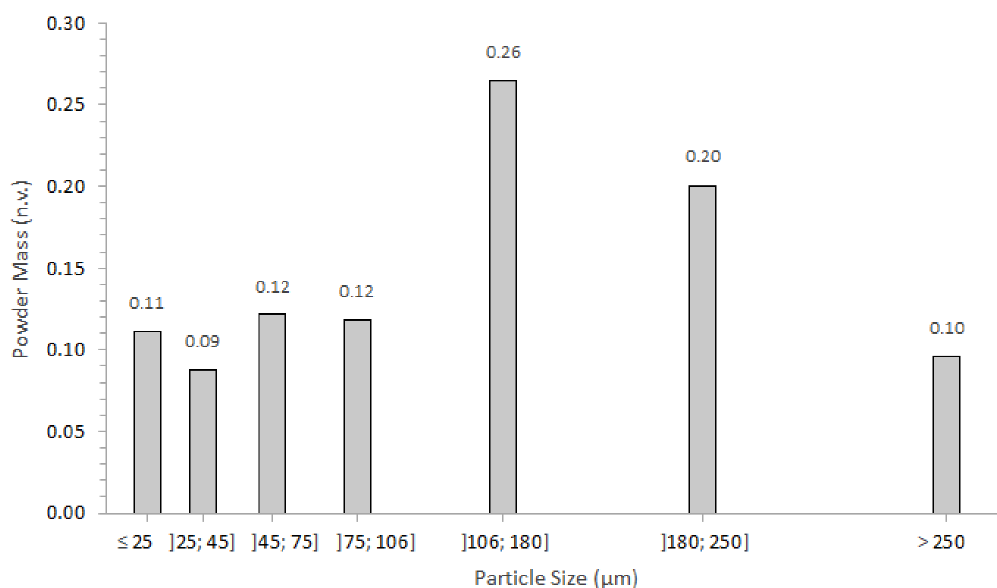


Figure 3.2 - Particle size distribution of the silicon powder produced by the SDS-grinding mill.

The powder production peak is located at the]106; 180] μm size range with a 26% occurrence, while particle sizes greater than 180 μm have a 30% prevalence and lower than 106 μm represent 44% of total powder production. The particle size distribution in Figure 3.2 is for a specific SDS-grinding mill configuration with a 44.60 mm distance between the top cylinder and the base. Changing the distance between the top and base would result in a horizontal shift of the particle size distribution: with a lower distance the relative weight of finer powders would increase, while with a higher distance the result will be the opposite.

3.1.2. Thermal Conductivity

The silicon powder thermal conductivity at room temperature of 298 K was measured for the]106; 180] µm particle size powder. The obtained thermal conductivity value was 0.144 ± 0.001 $Wm^{-1}K^{-1}$, which is three orders of magnitude lower than solid silicon [182] and one order of magnitude higher than the nanometric powder, previously used in the SDS process [180], [181]. This result is in line with other studies for micro and nano silicon [250] and silica [251] powders, which also showed a reduction in thermal conductivity as the particle size decreases. The decrease in thermal conductivity can be explained by a higher surface to volume ratio, which as particle size decreases, favours the presence of more void spaces between the powder particles, and being air a bad conductor, therefore, the overall powder conductivity is reduced. This has crucial implications during the CVD process, as the heated zones rise fast in temperature and are also wider, since the heat content transferred away from these zones by conduction is lower.

3.2. Chemical Vapour Deposition Experiments

The SDS-CVD reactor has proved to be a reliable system, capable of delivering consistent deposition results across a broad range of substrate types, either solid substrates like multicrystalline and sintered silicon samples, or powder silicon substrates of different particle sizes. First substrates used in CVD runs were made with a nanometric particle sized silicon powder [181], [222], later solid substrates were also tested [252] and finally, several micrometric particle sized silicon powders were studied [253].

3.2.1. CVD over Solid Substrates

Two types of solid substrates were used: multicrystalline silicon from p-type wafers and sintered silicon. Sintered silicon sheets had a 500 µm thickness with a shiny and reflective light grey surface. Both materials were laser cut into samples measuring 20×50 mm^2, and their surface was also laser textured, since untextured samples led to very low deposition rates, below the order of magnitude of 1 µm/min.

3.2.1.1. Texturing Patterns

In order to raise the growth rate of the CVD process, the solid substrates where laser textured to reduce the surface reflectivity and increase the effective surface area. A SPI G3.1 SM series pulsed fiber laser with a scan controller SC500 from Cambridge Technology, was used for texturing the solid substrates. The characteristics of the laser waveform are: 35 kHz pulse rate, 20 W average power, 8.2 kW peak power, 0.57 mJ pulse energy, 42 ns pulse width-fwhm and 1060 nm wavelength.

Before laser texturing the multicrystalline substrates were cleaned with an etching solution of HNO_3, CH_3COOH and HF, mixed with a 75:10:15 ratio, for 1 minute, while the sintered substrates were not pre-cleaned, since with a 10% average porosity, there was a substantial risk of changing their morphology. Table 3.1 presents the value pairs of the laser scanning speed (S) and the distance between consecutive scanning lines (D), the two main laser parameters which were used to create four distinct surface patterns (named A to D).

Table 3.1 - Laser parameters of the texturing patterns.

Pattern Type	S[a] (mm/s)	D[b] (mm)
A	3360	0.10
B	336	0.17
C	336	0.08
D	336	0.02

[a] Scanning speed.

[b] Distance between consecutive scanning lines.

The laser patterns on the samples were easily distinguishable to the naked eye, becoming darker and more surface disorganized with the increase of the pattern's laser intensity, as proved by a visual comparison of four textured multicrystalline silicon samples, shown in Figure 3.3. While in samples A and B, the crystalline grains are still visible, both samples C and D present a dust-like and chaotic surface appearance, with no noticeable grains.

Figure 3.4 presents the scanning electron microscope (SEM) images of multicrystalline silicon sample surfaces for the four pattern types. The laser parameters of pattern A created a surface with sequential small round craters, 10 µm deep and 50 µm wide, organized along the scanning lines. B and C patterns are both U-shaped parallel grooves, 30 µm deep and 50 µm wide, with

a valley distance of 170 µm and 80 µm, respectively, in agreement with the distance between consecutive scanning lines set by the laser parameters for those two texturing patterns. Sample D exhibits a powder-like surface morphology without any organized structure. The pattern shape is independent of the substrate material, meaning that both multicrystalline and sintered silicon samples will present equal surface arrangement for the same texturing pattern.

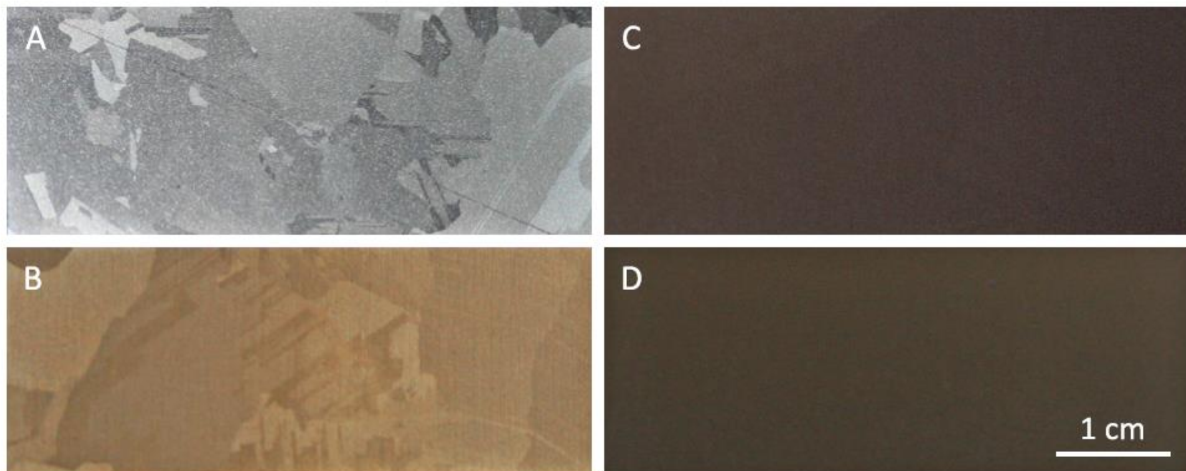


Figure 3.3 - Visual appearance of the multicrystalline silicon samples after being laser textured by four different patterns.

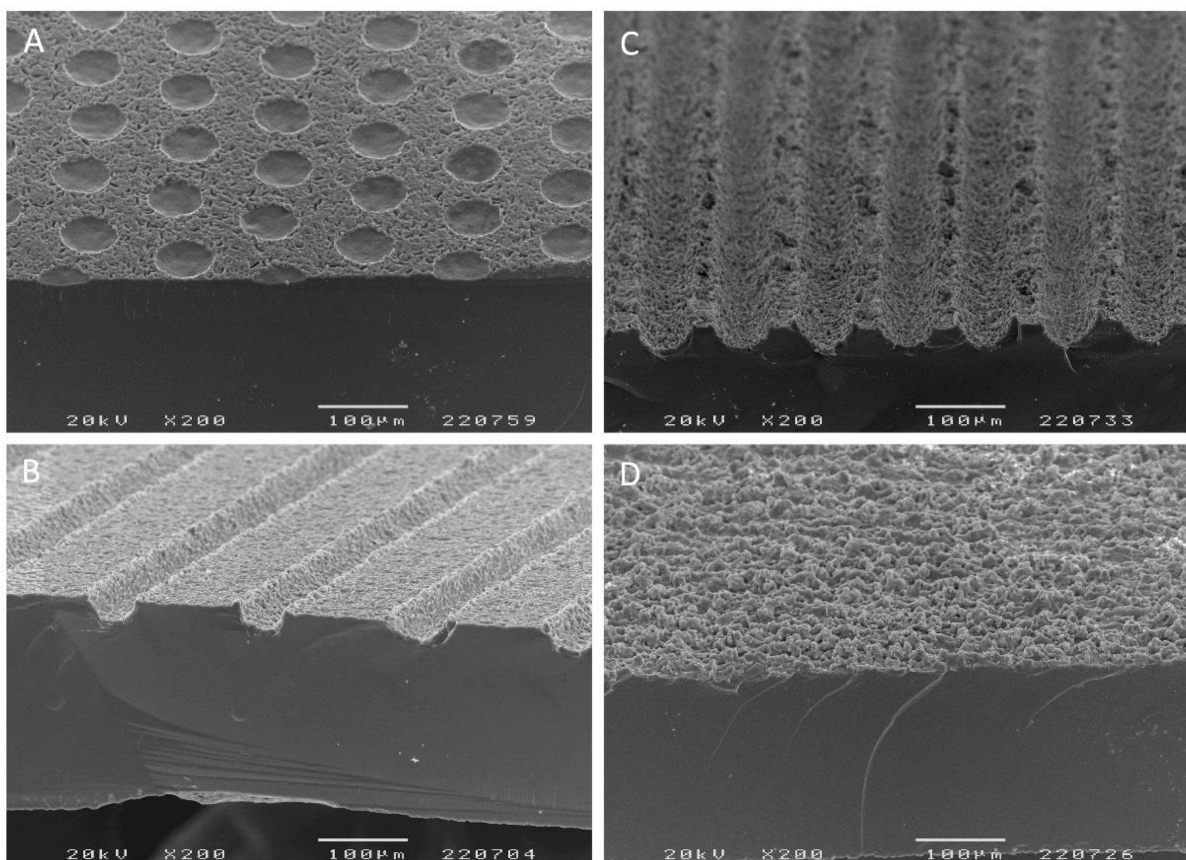


Figure 3.4 - SEM images of the multicrystalline silicon samples after being laser textured by four different patterns.

3.2.1.2. Results and Discussion

The multicrystalline and sintered silicon samples, both with the four texturing patterns, were used as substrates in the SDS-CVD reactor, following the same deposition procedure as described in section 2.3.4.5. Sample reflectivity was measured prior to deposition, with an integrating sphere, by averaging (arithmetic mean) the reflectivity values over the 700 to 1100 nm wavelength range, since it is the interval of interest for the halogen lamps. Growth rate (GR) was calculated using the equation:

$$GR = \frac{\Delta m}{\rho_{Si} A_{dep} t_{HR} N_{HR}} \quad (3.1)$$

where Δm is the silicon mass difference before and after the CVD process, ρ_{Si} is the crystalline silicon density (2.329 g/cm^3), A_{dep} is the deposition area of the solid or powder substrate, t_{HR} is the time of exposure to a deposition region, and N_{HR} is the total number of deposition regions crossed by the substrate.

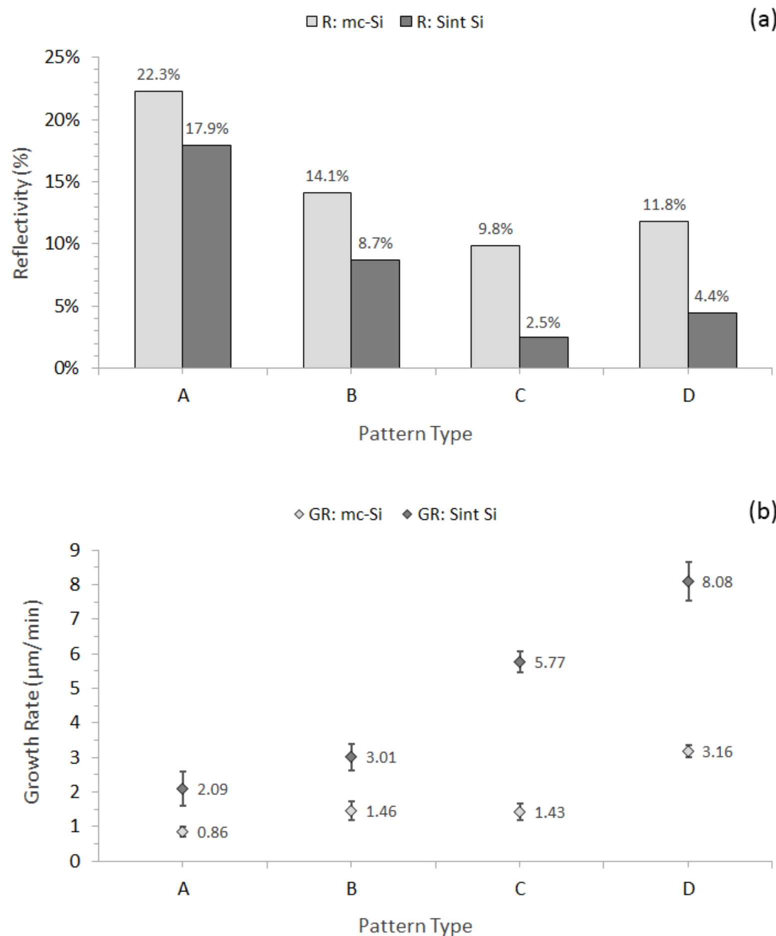


Figure 3.5 - Reflectivity (R) measurements before CVD (a) and growth rate (GR) results (b), of both multicrystalline silicon (mc-Si) and sintered silicon (Sint Si) samples, for the four different texturing patterns.

Figure 3.5(a) shows the measured reflectivity and Figure 3.5(b) the growth rate calculated by equation (3.1) of the four texturing patterns on each two substrate materials. In addition, Table 3.2 includes the values of both silicon mass and film thickness deposited over the substrates. Deposition conditions were kept the same across all CVD runs.

Table 3.2 - Growth rate, silicon mass and film thickness deposited over the substrates, of both multicrystalline silicon and sintered silicon samples, for the four different texturing patterns.

Sample Material	Pattern Type	Growth Rate (µm/min)	Deposited Silicon	
			Mass Variation Δm (mg)[a]	Film Thickness (µm)
Multicrystalline Silicon	A	0.86 ± 0.16	2.40	1.03 ± 0.12
	B	1.46 ± 0.27	3.98	1.75 ± 0.17
	C	1.43 ± 0.24	4.00	1.72 ± 0.16
	D	3.16 ± 0.18	8.84	3.80 ± 0.31
Sintered Silicon	A	2.09 ± 0.49	5.70	2.51 ± 0.22
	B	3.01 ± 0.37	8.20	3.62 ± 0.30
	C	5.77 ± 0.31	15.90	6.92 ± 0.53
	D	8.08 ± 0.56	22.30	9.69 ± 0.72

[a] Error of silicon mass variation is ± 0.10 mg for all values.

The substrates present a fairly uniform light to medium grey colour, a visual indication that a silicon film was deposited. A comparison of two multicrystalline silicon substrates, with patterns B and D, before and after CVD is presented in Figure 3.6.

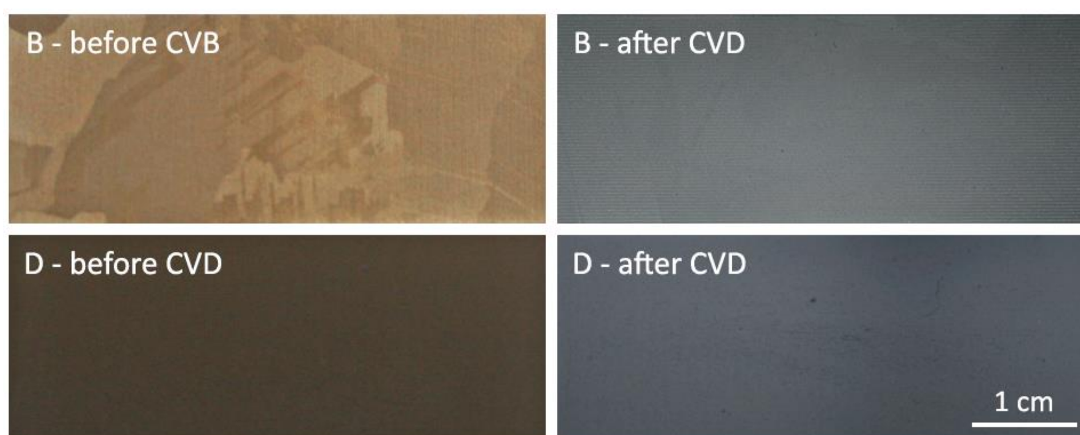


Figure 3.6 - Visual appearance of the multicrystalline silicon samples with pattern B and D, before and after CVD.

Laser texturing caused a clear decrease in reflectivity values, from around 32-33% on both sample materials to as low as 2.5% and 9.8% in sintered and multicrystalline silicon samples with pattern C, respectively. Moreover, sintered samples have always lower reflectivity than multicrystalline samples, for the same pattern. This behaviour is probably due to the fact that inner regions of sintered samples, exposed by the texturing process, are porous and darker without the shiny finishing of the surface, thus reducing more the reflectivity. The laser texturing process is also responsible for changing the effective surface area, which becomes greater with the increase of the pattern's laser intensity.

The growth rate is both influenced by reflectivity and effective surface area. Lower reflectivity increases the substrate temperature as more radiation is absorbed, favouring silane pyrolysis and higher effective surface area increases the surface density of deposition sites capable of supporting the silane heterogeneous decomposition on the solid substrate.

For the same texturing pattern, growth rate is always higher for substrates with lower reflectivity (sintered silicon samples), as their darker and porous interior revealed by the texturing process, gives a major contribution in decreasing the reflectivity when compared with the same pattern of a multicrystalline silicon sample. For the same substrate material, the growth rate also increases with the pattern's laser intensity, even though from pattern C to D there is a slight increase in reflectivity. In this particular case, the much higher effective surface area of pattern D gives a greater contribution than reflectivity, hence, the growth rate of substrates with pattern D are the greatest for both sample materials.

This set of CVD runs proved that the SDS-CVD reactor is able to successfully perform silicon deposition on solid substrates, producing a thin film over the substrate with thickness varying from 1.03 ± 0.12 to 3.80 ± 0.31 μm in multicrystalline silicon samples and 2.51 ± 0.22 to 9.69 ± 0.72 μm in sintered silicon samples.

3.2.2. CVD over Powder Substrates

One defining principle of the SDS process outlined in section 2.1, is the use of a silicon powder layer, serving both as a deposition substrate during the CVD and as an expendable layer for easy detachment of the pre-ribbon from the quartz. Thus, the first substrates used in CVD were made with silicon powder, particularly the nanometric sized powder previously described in section 2.2.2. The growth rates obtained are one order of magnitude higher than in solid silicon substrates, varying from 40 to 90 μm/min, this value range is due to the use of different

experimental conditions, such as the total number of deposition regions crossed by the substrate or the electric power per lamp. These growth rate values are explained by the higher effective surface area of the nanometric sized powder substrates [181], [222].

The development of both SDS-crusher and SDS-grinding mill (sections 2.2.4 and 2.2.5, respectively), allowed the production of several micrometric particle sized silicon powders from p-type wafers (section 3.1), which served as substrates for multiple CVD runs. An analysis of the produced pre-ribbons provided a better comprehension of the CVD step, and how it influences the final multicrystalline silicon ribbons delivered by the SDS-ZMR reactor.

3.2.2.1. Powder Substrate Preparation

Powder substrates are prepared by manually pressing the silicon powder against the quartz substrate holder, using a second smaller quartz plate, and shaped into a rectangle with a piece of multicrystalline silicon wafer. Several substrates measuring approximately 25×40 mm^2 were prepared, each one being made of six different micrometric sized silicon powders with particle sizes of ≤25,]25; 45],]45; 75],]75; 106],]106; 180] and]180; 250] µm, and subsequently feed to CVD runs. Table 3.3 presents the measured mass, area and calculated porosity for a typical group of five substrates made with powders of particle sizes ranging from ≤25 to]106; 180] µm.

Table 3.3 - Mass, area, mass per unit area and porosity, for five substrates made with powders of particle sizes ranging from ≤25 to]106; 180] µm.

Particle Size (µm)	Silicon Mass (g)[a]	Area (cm^2)	Mass per Unit Area (mg/cm^2)	Porosity (%)
≤25	0.446	10.33 ± 0.66	43.2 ± 3.3	71.8 ± 4.3
]25; 45]	0.572	9.57 ± 0.64	59.8 ± 4.5	70.1 ± 4.0
]45; 75]	0.506	10.22 ± 0.66	49.5 ± 3.7	70.7 ± 4.2
]75; 106]	0.498	9.73 ± 0.65	51.2 ± 3.9	69.2 ± 4.5
]106; 180]	0.619	10.27 ± 0.66	60.3 ± 4.4	67.3 ± 4.4

[a] Error of silicon mass measurement is ± 0.005 g for all values.

The substrate porosity was calculated after CVD,[4] measuring the pre-ribbon thickness and assuming that the initial powder substrate has approximately the same thickness. Knowing the substrate thickness, the respective volume and density were determined, which allowed a comparison with solid silicon density and consequently obtain the substrate porosity ϕ, using the equation:

$$\phi = 1 - \frac{\rho_{sub}}{\rho_{Si}} \qquad (3.2)$$

where ρ_{sub} is the calculated substrate density and ρ_{Si} is the crystalline silicon density (2.329 g/cm^3).

This approximation is valid because of two main aspects: (i) the deposited silicon contributes much more for substrate powder aggregation and incorporation than for increasing the substrate thickness, as it will be further explained in section 3.2.2.2; and (ii) even assuming that 10 µm of the pre-ribbon total thickness results from a silicon film deposited on top of the powder substrate (as for the deposition over the solid substrate with the highest growth rate), the re-calculated porosity considering only the remaining pre-ribbon thickness is just a couple of tenths lower than the one achieved with the contribution of the whole thickness.

The compaction of powders at low temperature (without sintering), consists of four main stages: (i) rearrangement of loose particles by sliding, rotation and re-collocation after pouring and shaking until a mechanically stable aggregate is formed; (ii) densification by local plastic deformation at the interparticle contacts; (iii) densification by global plastic deformation of the particles; and (iv) bulk deformation of the powder compact once a state of closed porosity is attained [254].

During the preparation of powder substrates, a unidirectional pressure is manually applied (approximately within the 25 to 50 kPa range[5]), decreasing substrate porosity and thickness, while giving special attention to maintain a constant homogeneity and distribution of the powder material across the whole substrate. Only stages (i) and (ii) are reached, since the two final stages require higher pressure values, solely possible with a machine tool, such as a press. The more pressure applied the better for decreasing porosity, nevertheless, structural integrity

[4] It is not feasible to measure the powder substrate volume in order to calculate its porosity.

[5] The pressure range values were computed by measuring both the applied force with a scale placed beneath the quartz substrate holder, and the area of the powder substrate after being compressed.

of the powder substrate becomes harder to be assured, since as the substrate gets more compressed the risk of powder adhesion to the smaller quartz plate becomes higher, which would create void areas in the substrate after pulling the compressing quartz plate. It was also observed that powders with particle sizes lower than 75 μm are harder to handle, as they are stickier, thinner and lighter, posing a greater effort on manually preparing pristine powder substrates.

The obtained powder substrates have a porosity in the 67.3 ± 4.4 to 71.8 ± 4.3% range, showing a tendency to increase with the decrease of powder particle size. At first glance, these results may seem counterintuitive, nevertheless, they are in line with several studies on powder compaction, showing that finer powders are harder to compact, and that initial relative density of loose powders can be very low and affected by particle size, as smaller particle powders tend to form low-density aggregates. Moreover, it was experimentally proved for iron and nickel powders within the 15 nm to 100 μm particle size range (approximately the same range as the silicon powders used by the SDS process), that: (i) for each powder the relative density increased (or porosity decreased) with the applied pressure; and (ii) the finer the particle size, the lower the relative density (or higher porosity) for the same applied pressure [254], [255].

Another relevant substrate property is the powder mass per unit area, which varied from 43.2 ± 3.3 to 60.3 ± 4.4 mg/cm^2, not showing any correlation or noticeable trend with the powder particle size. These values are a direct consequence of the operator's procedure during the preparation of the powder substrate, particularly the total mass of powder placed on the quartz substrate holder and how the powder spreads over an area when being compressed.

Ideally, the substrate making technique should aim for the minimum amount of powder, spread over the highest area, while maintaining a homogeneous, low thickness and highly compressed silicon powder substrate. Hence, the preparation of the silicon powder substrate is an important and decisive step of the SDS process, since the physical properties of the substrate, such as porosity, thickness and powder mass per unit area, will have a preponderant influence on the microcrystalline silicon pre-ribbon characteristics, discussed in section 3.2.2.2, and consequently on the final multicrystalline ribbon quality, discussed in section 3.3.

3.2.2.2. Results and Discussion

Several microcrystalline silicon pre-ribbons were produced by the SDS-CVD reactor, under the same deposition conditions, while using the powder substrates of different particle sizes. Figure

3.7 presents a group of five microcrystalline silicon pre-ribbons made with the powder substrates described in Table 3.3. They exhibit an almost smooth light to medium greyish surface and showed little or no visual signs of surface porosity.

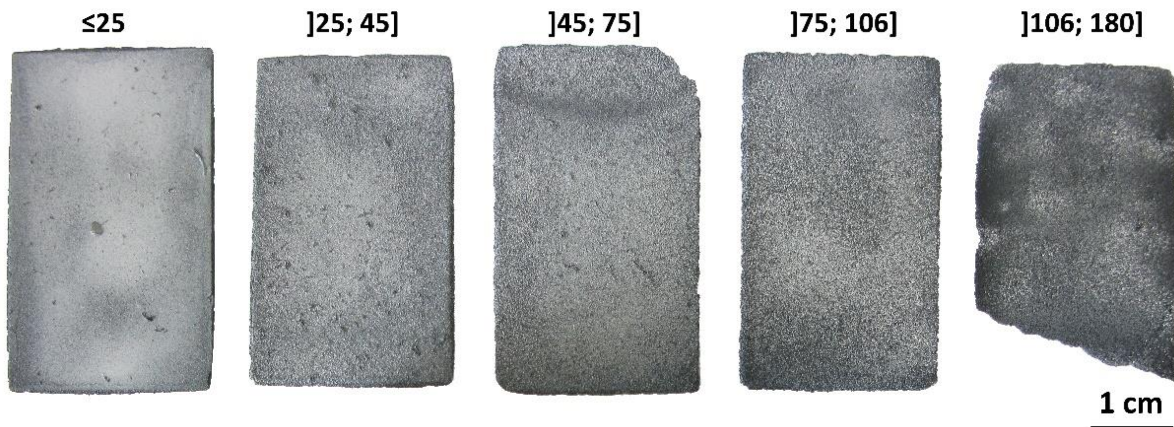


Figure 3.7 - Visual appearance of the microcrystalline silicon pre-ribbons, obtained after CVD over powder substrates of particle sizes ranging from ≤25 to]106; 180] µm.

All pre-ribbons produced using powder substrates with particle sizes lower than 106 µm were easily detached from the quartz substrate holder, while the pre-ribbon grown with the]106; 180] µm particle size powder substrate could not be removed intact, since its edge was firmly glued to the quartz sample, as seen in Figure 3.7. Additionally, substrates made with the]180; 250] µm particle size powder, the largest powder produced by the SDS-grinding mill, showed an even stronger adhesion effect, being impossible to detach the pre-ribbon from the quartz without completely destroying it. For this reason, neither the photo of the pre-ribbon was presented in Figure 3.7, nor the properties of the corresponding powder substrate were included in Table 3.3. The results for the two larger particle size powders, suggest that silicon from the gaseous phase can travel throughout the powder substrate thickness and be deposited in the quartz-powder interface, permanently bonding the pre-ribbon to the quartz surface. Hence, for the employed experimental conditions during the CVD runs combined with the physical properties of the substrates used, there is a maximum value for particle size powder, in this case around 100 µm, above which the pre-ribbons cannot be handled and separated to be used in the next SDS step.

The growth rate results in Figure 3.8(a), computed by equation (3.1), clearly indicate that the particle size of the silicon powder substrate has a major impact on the growth rate, exhibiting a trend of growth rate decrease with increasing particle size. For the smallest particle size powder substrate (≤25 µm) a growth rate of 52.8 ± 6.2 µm/min was achieved, decreasing for higher

particle sizes, following an apparent exponential decay[6] down to a value of 26.4 ± 4.0 µm/min for the]106; 180] µm particle size powder. On the substrate made with the largest powder tested,]180; 250] µm, despite the pre-ribbon being completely stuck to the quartz, it was possible to determine a growth rate of 13.4 ± 1.8 µm/min, which gets closer to the highest value obtained for a solid substrate (8.08 ± 0.56 µm/min on the sintered silicon sample with laser pattern D). This particular result confirms that, regarding growth rate, larger particle size powder substrates tend to have similar behaviour to the solid silicon sintered substrate with powder-like surface morphology.

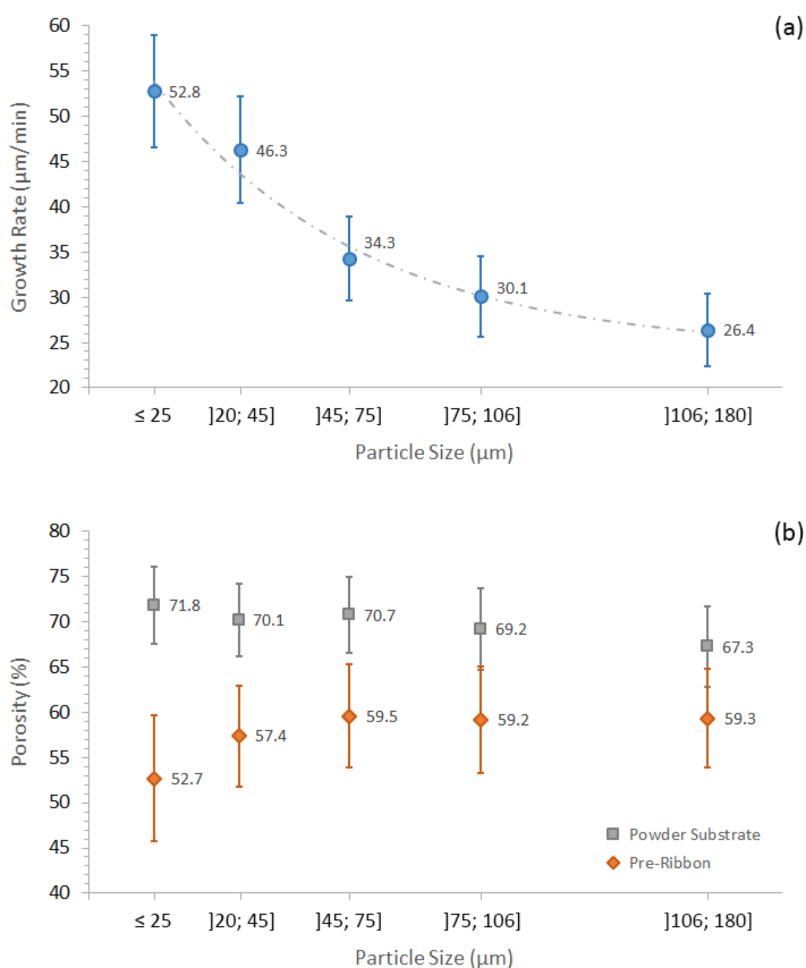


Figure 3.8 - Growth rate (a) and porosity (b) of both powder substrate and pre-ribbon, as a function of substrate particle size.

In Figure 3.8(b) the variation of the pre-ribbon porosity with substrate powder particle size is plotted, together with the corresponding powder substrate porosity, for comparison purposes. The powder substrates have approximately the same porosity, varying within the 67.3 ± 4.4 to 71.8 ± 4.3% range, marginally increasing with the decrease of powder particle size. After CVD,

[6] The dashed line shown in the graph of Figure 3.8(a) is an exponential fit of the growth rate data.

the resulting pre-ribbon has always a lower porosity as expected, being evident a slight raise of pre-ribbon porosity with increasing particle size, from 52.7 ± 7.3% for the ≤25 μm powder substrate until stabilizing around 59% for higher particle size powders. The porosity variation between the powder substrate and the pre-ribbon is greater for the three finer powders, with the highest decrease occurring in the ≤25 μm powder substrate, going from a 71.8 ± 4.3% substrate porosity to a 52.7 ± 7.3% pre-ribbon porosity.

Table 3.4 shows the calculated growth rate and porosity, as well as two relevant indicators, the silicon mass variation (amount of deposited silicon by CVD) and the powder ratio (share of substrate powder present in the final pre-ribbon) for pre-ribbons made with the five different powder substrates.

Table 3.4 - Mass variation, powder ratio, growth rate and porosity, for five microcrystalline silicon pre-ribbons obtained after CVD over powder substrates of particle sizes ranging from ≤25 to]106; 180] μm.

Particle Size (μm)	Silicon Mass Variation Δm (g)[a]	Powder Ratio	Growth Rate (μm/min)	Porosity (%)
≤25	0.302	0.60 ± 0.01	52.8 ± 6.2	52.7 ± 7.3
]25; 45]	0.245	0.70 ± 0.01	46.3 ± 5.9	57.4 ± 5.8
]45; 75]	0.194	0.72 ± 0.01	34.3 ± 4.7	59.5 ± 6.0
]75; 106]	0.162	0.75 ± 0.01	30.1 ± 4.5	59.2 ± 6.2
]106; 180]	0.150	0.80 ± 0.01	26.4 ± 4.0	59.3 ± 5.7

[a] Error of silicon mass variation is ± 0.010 g for all values.

The behaviour of both growth rate and pre-ribbon porosity can be attributed to the increase of the effective deposition area when powder particle size decreases. Powder substrates with larger effective areas have a higher density of dangling bonds, either Si-H or -Si, hence a higher number of deposition sites are available, increasing the rate of occurrence of the heterogeneous reactions responsible for silicon deposition on a solid substrate, as explained in section 2.3.2. This results in a greater amount of deposited silicon, thus a higher growth rate, for the lower particle size powders. The porosity decrease between the powder substrate and the respective pre-ribbon is greater on lower particle size powder substrates, being a direct consequence of the greater amount of deposited silicon (or higher growth rate) occurring in those powder substrates. As seen in Table 3.4, the silicon mass variation for the ≤25 μm powder substrate is

0.302 ± 0.010 g, practically twice as much as the mass variation on the coarser (]106; 180] μm) powder substrate.

An important finding of the CVD runs using micrometric particle sized silicon powders is that almost all the silicon powder used as substrate is incorporated in the pre-ribbon, with minimal to no powder being left on the quartz substrate holder after pre-ribbon detach. The deposited silicon acts as a gluing agent of the powder, providing mechanical sustainability to the substrate and reducing its porosity. The powder ratio values shown in Table 3.4, varying between 0.60 ± 0.01 and 0.80 ± 0.01, are a clear proof that the majority of the silicon material present in the pre-ribbon came from the powder substrate. The decrease of the powder ratio values with decreasing powder particle size is due to growth rate being greater for those finer powders, and consequently more silicon from the gaseous phase is deposited.

The obtained results suggest that: (i) the use of even smaller particle size powders could benefit the CVD process, as higher growth rates and lower pre-ribbon porosities would be attained, nevertheless, it must be considered that in very small particle sized powders like nanometric powders, the handling is more challenging, being more difficult to obtain a homogeneous substrate and there is an increased environment contamination risk due to a greater effective area; and (ii) the technique for preparing a powder substrate, particularly the powder compaction step, determines its physical properties, which will later have a dominant influence on the characteristics of the pre-ribbons produced by the SDS-CVD reactor. An experimental procedure aimed for improving the quality and reproducibility of the powder substrates is briefly presented in section 4.2.

3.3. Zone Melting Recrystallization Experiments

The SDS-ZMR reactor is an effective and versatile system, which has been used for processing different ribbon materials, depending on the main objective to achieve, such as: (i) recrystallization of silicon pre-ribbons from the SDS-CVD reactor, obtained from silicon powder substrates, either nanometric particle sized [181] or micrometric particle sized [256], [257]; and (ii) recrystallization of multicrystalline silicon ribbons, either for analysing the temperature profile of the reactor and its influence on the ribbon's crystalline quality [248] or for studying dopant incorporation profiles on ribbons sprayed with boric or phosphoric acids and further recrystallized [258], [259].

3.3.1. Pre-Ribbon Recrystallization

Multiple recrystallization runs were performed by the SDS-ZMR reactor, using both pre-ribbons obtained in the CVD step, and multicrystalline ribbons cut from solar grade p-type silicon wafers, to serve as reference and assess the furnace operation parameters and the quality of the recrystallization process. Solar grade multicrystalline silicon ribbons are easier to recrystallize, having nearly a 100% successful rate, since the sample homogeneity allows a more stable molten zone that can travel along the ribbon without collapsing. Moreover, the presence and extent of an oxide layer over the molten zone, is less severe in solar grade multicrystalline silicon ribbons, than in the CVD grown pre-ribbons.[7] Some SDS-ZMR runs with pre-ribbons had a significant amount of oxide, most probably due to higher level of impurities, and the failure to remove the superficial oxide (which is common on pre-ribbons) increases the difficulty in monitoring and controlling the molten zone, with a detrimental impact on the quality of recrystallization process, resulting either in incomplete (or superficial) recrystallization or in a collapsed molten zone.

Figure 3.9 presents two pre-ribbons, grown with]75; 106] and]106; 180] µm particle size powder substrates, after being subjected to a ZMR run. Light and delicate oxide structures in the form of thin filaments and hairy agglomerates, with a white to light cream colour, are clearly visible. Also present are void areas in the samples surface, due to the collapse of the molten zone during recrystallization.

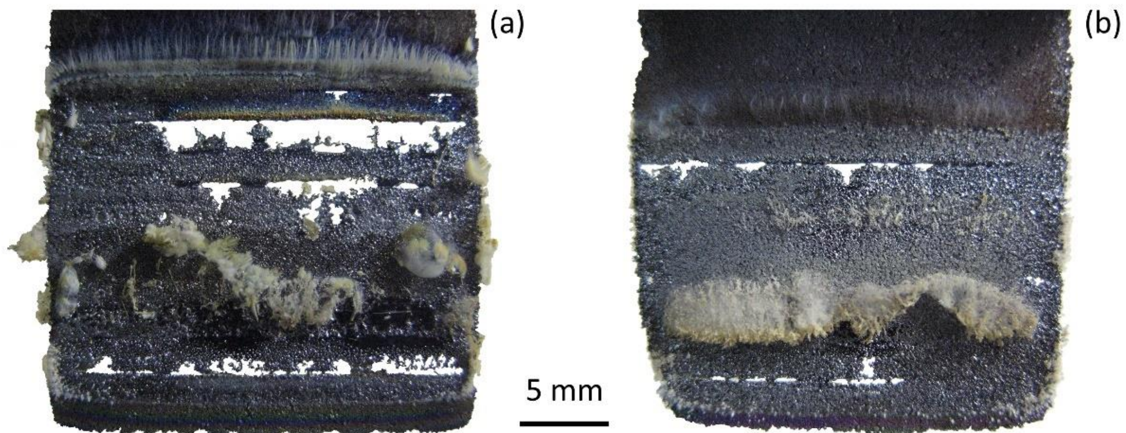


Figure 3.9 - Pre-ribbons after being recrystallized, which were grown with two particle size powder substrates: (a)]75; 106] µm powder; and (b)]106; 180] µm powder.

[7] Superficial oxide on multicrystalline silicon ribbons can be easily removed by a CP4 etching solution, followed by an HF bath. Since multicrystalline silicon ribbons are not porous, this cleaning procedure is more effective than when performed in the SDS pre-ribbons.

Recrystallized ribbons without or with low oxide content can be obtained if at least one of the following conditions are met: (i) pre-ribbon oxide content is low enough to avoid saturation of the reactor atmosphere during the recrystallization process; (ii) existing oxide layers over the molten zone are removed by varying experimental conditions, like increasing lamp power (higher incident energy per unit area), and/or increasing the argon flow rate. Therefore, if no oxide is present, a well-defined line-shaped molten zone, brighter than the surrounding material and extending across almost the pre-ribbon width, is formed as shown in Figure 3.10 (marked by two arrows).

The molten zone height can vary within the 0.20 to 2.00 mm range,[8] depending on both the applied lamp power and focusing accuracy of the optical system. When the molten zone starts to appear, as one or more small molten spots that quickly spread laterally until they form a line-shaped molten zone, its height in this early stage is around 0.20-0.50 mm (as in the molten zone presented in Figure 3.10). After a stable molten zone is attained, a slight raise in the applied voltage to the halogen lamps causes an increase of the molten zone height up to 2.00 mm, above which there is a high chance of collapse.

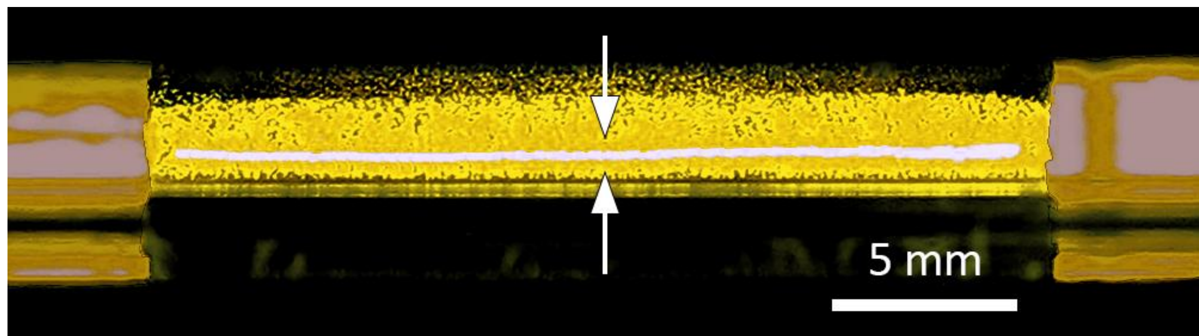


Figure 3.10 - Line-shaped molten zone in a CVD grown pre-ribbon, measuring approximately 22.7×0.25 mm^2.

During the recrystallization of a first group of pre-ribbons, measuring approximately 25×41 mm^2, obtained with micrometric sized powders ranging from ≤25 to]75; 106] µm and also with a nanometric sized powder, there was a thin superficial layer of oxide over the molten zone, which did not allow the complete recrystallization of the pre-ribbons. Small areas of the pre-ribbons, measuring around 5-20 mm^2, were successfully crystalized, leading to an average crystal size in the 0.1 to 1.0 mm range. Figure 3.11 shows multicrystalline areas from ribbons obtained with powder substrates of]75; 106] µm (Figure 3.11 (a)) and nanometric range (Figure

[8] Molten zone height is determined by digital imaging.

3.11(b)) particle sizes, being also visible the presence of bright white superficial oxide agglomerates, mainly located in the edges of those crystalline areas.

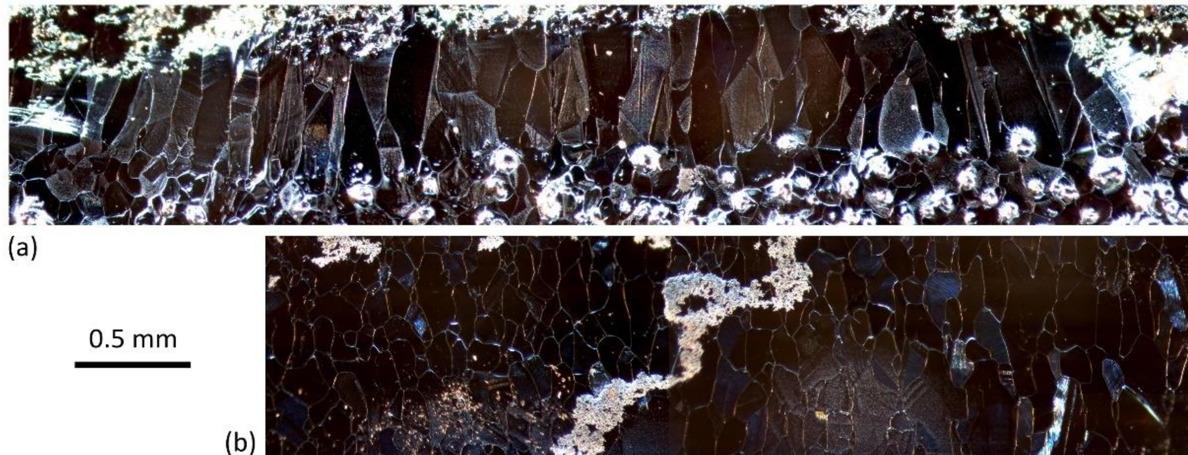


Figure 3.11 - Multicrystalline silicon ribbon areas obtained by zone melting recrystallization from pre-ribbons grown with powder substrates of (a)]75; 106] μm; and (b) nanometric range particle sizes.

SEM images of these two ribbons, presented in Figure 3.12, confirm the existence of three distinct regions: (i) solid surface areas with well-defined crystals in Figure 3.12(b) and (c); (ii) porous powder-like areas where recrystallization was not successful in Figure 3.12(a); and (iii) interface regions between the porous pre-ribbon and the solid crystalline areas in Figure 3.12(a).

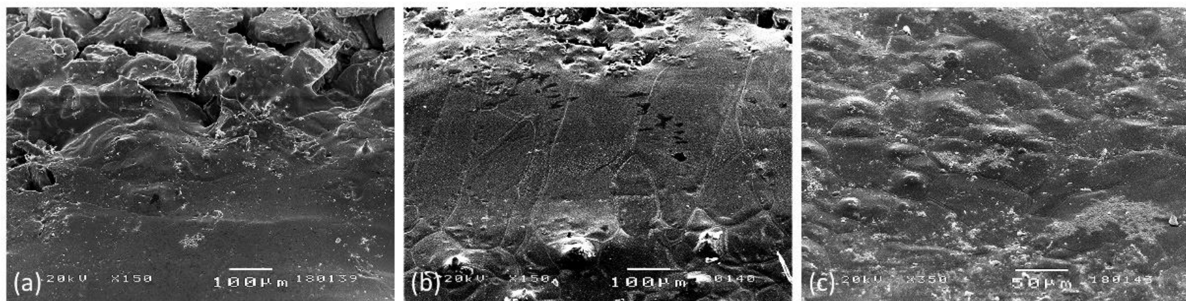


Figure 3.12 - SEM images of recrystallized areas: (a) porous-solid crystalline interface; and ribbons grown with powder substrates of (b)]75; 106] μm; and (c) nanometric range particle sizes.

The smaller and round shape crystals visible in the ribbon obtained with a nanometric powder substrate are a proof of superficial recrystallization on both surfaces, while the inner porous structure was not fully recrystallized. On the contrary, the elongated crystals and equal crystal orientation at the same location on both surfaces of the]75; 106] μm powder substrate ribbon, confirms a complete melting of the silicon pre-ribbon and crystal growth along the whole ribbon thickness and pulling direction, as seen in Figure 3.11(a) and Figure 3.12(b). This assumption was verified by a cross section view of the crystalized area on the ribbon obtained with a powder substrate of]75; 106] μm, depicted in Figure 3.13, and showing a solid silicon material without

any signs of porosity across the whole ribbon thickness. The difference in crystallization behaviour is probably due to porosity being lower in the nanometric pre-ribbon, thus requiring more heat than the actual amount provided during the ZMR run, to achieve a complete material melting. Also, oxide content tends to be higher on nanometric pre-ribbons when compared with micrometric powder's pre-ribbons, making harder to get an adequate recrystallization.

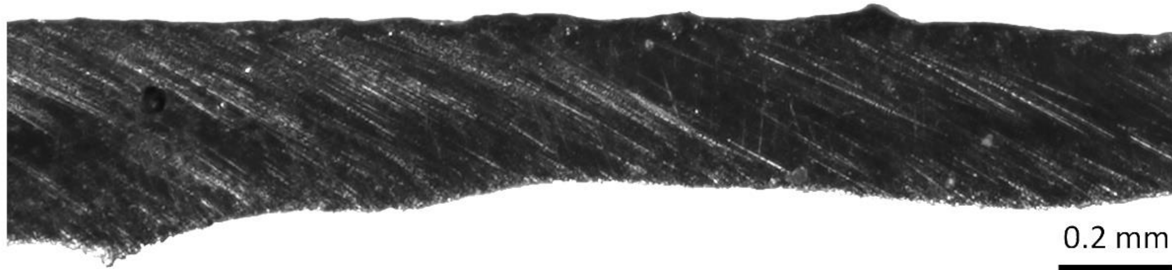


Figure 3.13 - Cross section view of a ribbon, grown with a]75; 106] μm particle size powder substrate, obtained by mechanical polishing a recrystalized area.

The thickness of recrystallized areas varies from 240 to 300 μm and 330 to 350 μm in ribbons obtained with powder substrates of]75; 106] μm and nanometric range particle sizes, respectively. Hence, the thickness reduction due to the ZMR run is around 58-66% and 19-23% for the]75; 106] μm and nanometric powder pre-ribbons, respectively, which is consistent with the corresponding pre-ribbon porosity values. These results suggest that the thickness reduction observed during ZMR is primarily the consequence of an extensive densification of the crystallized material.

The presence of oxide during the ZMR of this group of pre-ribbons, made the crystallization process more challenging and even impossible to accomplish in some pre-ribbon areas, since persistent oxide layers over the pre-ribbon made more difficult to create a stable and continuous molten zone. Oxide contamination may come from several sources: (i) pre-ribbons, although they undergo a 2 vol% HF bath before recrystallization, it is extremely probable that, due to its high porosity, a rapid re-oxidation occurs prior to the ZMR process; (ii) contamination of inner ZMR reactor walls; and (iii) leaking of atmospheric oxygen into the reactor during the ZMR process, even if before starting the heating stage the reactor was proved to be airtight, the presence of small air leaks during recrystallization cannot be excluded.

A second group of pre-ribbons, measuring approximately 26×67 mm^2 and grown over micrometric sized powder substrates ranging from ≤25 to]75; 106] μm, was subjected to ZMR runs. In this case the recrystallization process was not greatly affected by oxide formations, thus

creating and maintaining a stable molten zone was possible, which allowed the crystallization of larger areas of the pre-ribbons. The low oxide content can be attributed to the fact that powders used in the preparation of the substrates, came from a different batch produced with a small amount of silicon wafers, therefore the contact time between the powders and both the test sieves and the atmosphere was greatly reduced.

When oxide is not present, the stability of the molten zone depends mostly on the characteristics of the pre-ribbon, such as: substrate powder particle size, substrate powder incorporation into the pre-ribbon, and pre-ribbon porosity and thickness. It was observed that the following features of the pre-ribbons favoured the maintenance of a steady molten zone for longer periods of time: (i) lower values of porosity and thickness; (ii) grown over powder substrates with smaller particle size (≤75 µm), resulting in lower porosities after the CVD step; and (iii) lower powder ratio (also contributing for decreasing the porosity).

Figure 3.14 shows a successfully recrystallized pre-ribbon, grown with a]45; 75] µm particle size powder substrate, clearly evidencing the difference between the non-recrystallized area at the top and the multicrystalline growth obtained after the ZMR step.

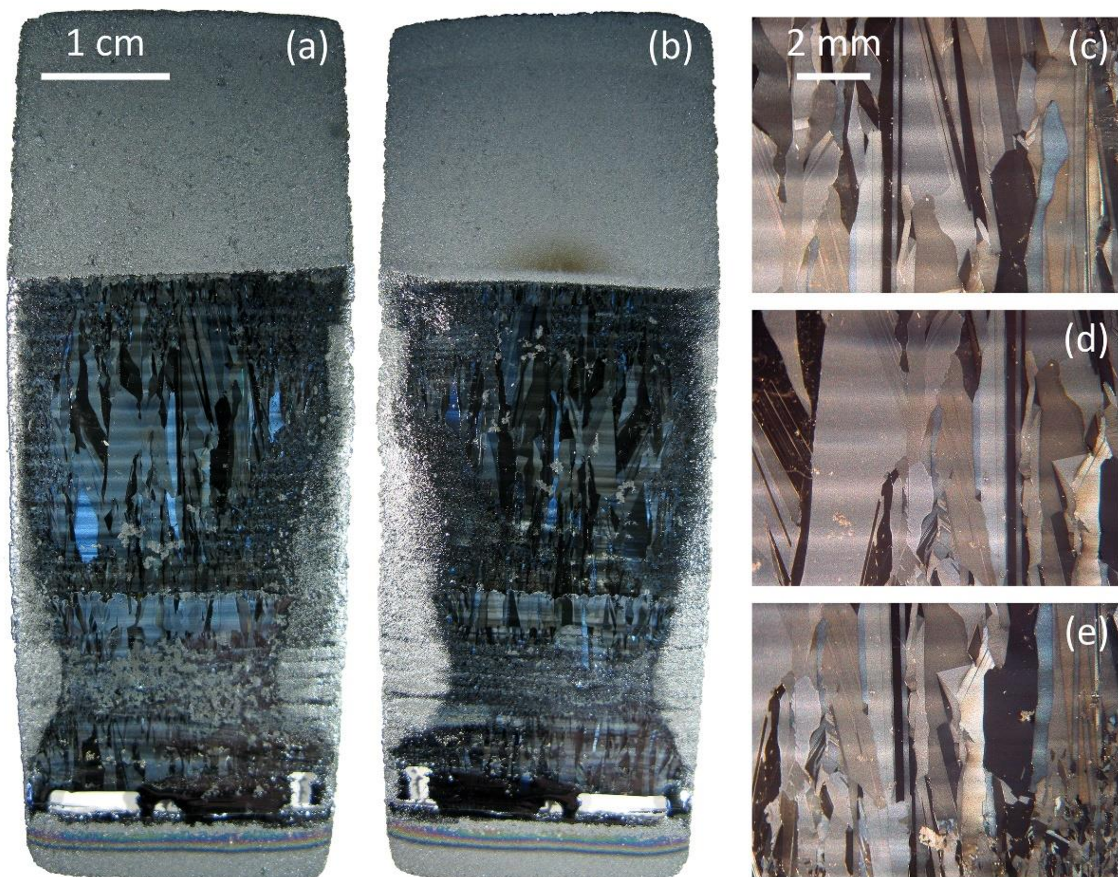


Figure 3.14 - Silicon ribbon after ZMR: (a) front and (b) back-side; and (c), (d) and (e) close-up views of crystallized areas.

The ribbon has a multicrystalline area of approximately 2×4 cm^2, with visible columnar crystal growth on both sides. The crystals on the upper part of the recrystallized area, have an average crystal size in the 1 to 10 mm range, being bigger and more elongated than the ones on the bottom part since the molten zone travel on the upper region was done continuously without stopping, while on the bottom region, due to the appearance of some superficial oxide, the molten zone travel was stopped multiple times to allow the evaporation of oxide, but resulting in smaller and rounder crystals. On the bottom region, the presence of superficial impurities is also visible,[9] resulting from insufficient impurity segregation during the recrystallization process in that ribbon area. Regarding the recrystallization process, this is the best result ever achieved with SDS ribbons, outperforming the previous record of a 2.2×2.2 cm^2 multicrystalline area [181], equivalent to a 65.3% increase in recrystallized area.

3.3.2. Ribbon Characterization

The best multicrystalline silicon ribbons obtained by the SDS-ZMR reactor were characterized using non-destructive methods, such as four-point probe resistivity measurement and contactless microwave photoconductance decay (μ-PCD) lifetime characterization technique. Resistivity measurements were performed using a collinear four-point probe system [260]. Recombination lifetime was measured on a Semilab WT-1000 device with a 3 mm laser spot diameter. The samples were previously cleaned in a 4 vol% HF solution, followed by chemical passivation of the surface with an iodine in ethanol solution, to minimize surface recombination [261].

For comparison purposes, resistivity and lifetime measurements, were performed on three different types of multicrystalline silicon materials: (i) p-type silicon wafers (with a resistivity in the 0.5-2.0 Ω.cm range) of the same industrial batch used to produce the silicon powder substrates; (ii) ribbons from the same material described in (i) but recrystallized by the ZMR reactor; and (iii) multicrystalline silicon ribbons obtained by the SDS process. Boron concentration was calculated from the measured resistivity values, combined with the relation of bulk carrier mobility and doping concentration [262]. Table 3.5 presents the measured resistivity and lifetime values, and the calculated values of boron concentration, with errors obtained by computing the standard deviation of the measured values.

[9] Superficial impurities are small solid agglomerates with a bright white or grey colour.

Table 3.5 - Resistivity, average dopant concentration and lifetime values for three types of multicrystalline silicon ribbons.

Sample	Resistivity (Ω.cm)	Dopant Concentration (cm^{-3})	Lifetime (μs)
p-type wafer	1.12 ± 0.02	1.3×10^{16}	2.0 ± 0.1
p-type wafer + ZMR	1.28 ± 0.02	1.1×10^{16}	4.4 ± 0.8
SDS ribbon	0.70 ± 0.05	2.1×10^{16}	0.3 ± 0.1

The dopant concentration of the SDS ribbon sample has the same order of magnitude as the p-type wafers (~10^{16} cm^{-3}) used in the silicon powder production, confirming a very substantial powder incorporation from the substrate during the CVD step. This result is consistent with the previously calculated values of pre-ribbon powder ratio, presented in Table 3.4, which are in the 60 to 80% interval, for the size range of tested powder substrates. Since the majority of silicon material existing in the pre-ribbon came from the p-type silicon powder, and since the ZMR step does not change the dopant concentration level, its value on the final ribbon is directly linked to the p-type silicon powder doping level.[10]

The lifetime of the p-type silicon wafer after being recrystallized by the SDS-ZMR reactor is 2.2 times more than the value of the p-type wafer, which is an unexcepted result, as it should have been equal or less. Adding a ZMR step to an industrial silicon wafer which has low impurity concentration and high crystalline quality, will not improve the material properties and will likely introduce more lattice defects such as thermally induced dislocations. Hence, this result can be attributed to the variability of the crystalline quality in multicrystalline silicon, and the fact that the wafers used were not equivalent (i.e., not the same crystal distribution). The lifetime of the recrystallized SDS ribbon is small compared to the other samples, 85% lower than the value of the p-type wafer, suggesting an inferior crystal quality and the possible presence of metallic impurities and also oxygen aggregates acting as recombination centres.

3.3.3. Ribbon Doping

Classic bulk doping methods of silicon are based on introducing dopant species during the crystal growth stage, either crucible-based techniques in which the feedstock is contaminated

[10] Despite the dopant concentration value of the SDS ribbon being slightly higher than the one for the p-type wafer, it is within the dopant concentration range (7.2×10^{15} to 3.3×10^{16} cm^{-3}) of the p-type wafer batch from which silicon powder was produced. This is an indication that the p-type wafers used to produce the silicon powder had on average, a higher dopant concentration than the p-type wafer presented in Table 3.5.

by heavily doped silicon granules, or gas-to-solid techniques where dopants in gaseous form are added to the atmosphere. Unlike the classic doping methods, in the SDS process, the growth and doping steps do not occur at the same time, as the CVD grown pre-ribbon is doped during the final recrystallization step.

The doping method for the SDS pre-ribbons, previously developed and characterized [263], consists in spraying boric acid (H_3BO_3) for p-doping [258], or phosphoric acid (H_3PO_4) for n-doping [259], over the pre-ribbon surface, before the ZMR step.

The doping procedure begins by cleaning the pre-ribbon, with CP4 and HF solutions and rinsing with deionized water. Then, an in-house spraying system, previously developed, comprised of a polymethyl methacrylate (PPMA) cylinder serving as deposition chamber, and a nebulizer fed by constant nitrogen (N_2), is used. A schematic of the spraying system is shown in Figure 3.15 [259]. The pre-ribbon is placed inside the deposition chamber, at the centre of its base, a diluted solution of H_3BO_3 (or H_3PO_4 for n-doping) is put in the nebulizer reservoir and a constant flow of N_2 creates an aerosol, entering at the top of the cylinder and filling the entire chamber. After being uniformly coated and dried the pre-ribbon is placed inside the SDS-ZMR reactor.

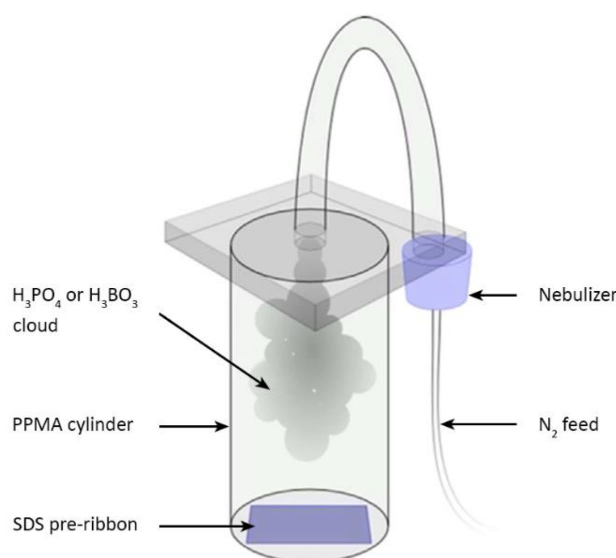


Figure 3.15 - Schematic of the spraying system used for doping the pre-ribbon [259].

In p-doping, during the heating stage as the pre-ribbon temperature increases, the water molecules evaporate and the H_3BO_3 is decomposed into metaboric acid (HBO_2) according to equation (3.3). The direct formation of boron oxide (B_2O_3) is also possible:

$$H_3BO_3 \rightarrow HBO_2 + 2H_2O \quad (3.3)$$

$$2HBO_2 \rightarrow B_2O_3 + H_2O \quad (3.4)$$

$$H_3BO_3 \rightarrow B_2O_3 + 3H_2O \quad (3.5)$$

For temperatures above 1000 °C, B_2O_3 dissociates and boron is incorporated into the ribbon by diffusion across the surface, forming SiO_2 according to the equation:

$$2B_2O_3 + 3Si\ (s) \rightarrow 3SiO_2\ (s) + 4B\ (s) \quad (3.6)$$

The resulting SiO_2 turns into volatile SiO at the silicon melting point, thus leaving the ribbon surface:

$$SiO_2\ (s) + Si\ (s) \rightarrow 2SiO\ (g) \quad (3.7)$$

In n-doping, with the temperature increase the water molecules evaporate, the H_3PO_4 dehydrates and forms a mixture of different polyphosphoric acids. During the heating stage the phosphorous incorporation in the silicon occurs by solid-state diffusion as shown in the equation:

$$H_aP_bO_c + dSi\ (s) \rightarrow Si_xP_y\ (s) + Si_wO_z\ (s) \quad (3.8)$$

For higher temperatures, a complete dehydration of the H_3PO_4 occurs, resulting in phosphorous oxide (P_4O_{10}) being the only compound left. At the melting point the phosphorous incorporation is done according to:

$$P_4O_{10} + 5Si\ (s) \rightarrow 5SiO_2\ (s) + 4P\ (s) \quad (3.9)$$

The produced SiO_2 follows the behaviour of equation (3.7).

To obtain a n-type ribbon with 10^{16} cm^{-3} phosphorous concentration, an SDS pre-ribbon was sprayed for 60 seconds with a 0.13 mol/L H_3PO_4 solution, producing a uniform coating of the pre-ribbon surface [259]. After drying the pre-ribbon was recrystalized.

Resistivity measurements of the recrystallised areas returned very high values (>10 Ω.cm), suggesting a doping level much lower than the targeted one. To understand this result it must be recalled that SDS pre-ribbons powder ratio is in the 0.60 to 0.80 range, and the powder used resulted from grinding silicon wafers with 10^{16} boron atoms/cm^3. Hence the obtained pre-ribbons have a boron concentration of the order of 10^{16} cm^{-3}, and since a similar concentration

of phosphorous atoms was introduced during the doping process, a dopant compensation will occur between the n- and p-type dopants, characterized by the filling of the excess of holes by excess of electrons added by the phosphorous doping, therefore reducing the net doping concentration and increasing the ribbon resistivity.

Since that currently the SDS pre-ribbons produced have very high powder ratios, and already have a boron concentration of the order of 10^{16} cm^{-3}, there is no point in introducing a doping step. However, since the objective is to produce pre-ribbons with much lower powder incorporation (<0.10), a dopant (either p- or n-type) will have to be introduced in the silicon pre-ribbons, and for that purpose one of the previously described methods can be used to obtain either boron or phosphorous doped ribbons.

Chapter 4
Conclusions

4.1. Key Findings

The experimental work done during this thesis encompassed the whole SDS technique, from the initial step of silicon powder production, followed by CVD over a powder substrate, and the final ZMR process to deliver a multicrystalline silicon ribbon. All the three steps are closely related, with each step influencing the next one, as well as the quality of the final silicon ribbon.

A newly in-house developed system for producing silicon powder, proved to be an effective way to obtain micrometric particle sized powder ranging approximately from 10 to 300 µm. Silicon p-type wafers were used as feedstock material, although other types of silicon sources could have been employed. A set of test sieves was then used to separate the obtained silicon powder in six groups of powders with well-defined particle size intervals, from ≤25 to]180; 250] µm.

Substrate powders were manually prepared by pressing the silicon powder against the quartz substrate holder, using a smaller quartz plate. The powder substrate preparation is one of the most important processes of the SDS technique, since the substrate properties will have a preponderant impact on the CVD and ZMR processes, specifically on the success of those processes and on the properties of both microcrystalline pre-ribbons and multicrystalline ribbons.

Substrates (measuring approximately 25×40 mm^2) made using powders with particle sizes of ≤25,]25; 45],]45; 75],]75; 106] and]106; 180] µm had a porosity varying within the 67.3 ± 4.4 to 71.8 ± 4.3% range, evidencing a tendency to increase with the decrease of powder particle size. The powder mass per unit area was within the 43.2 ± 3.3 to 60.3 ± 4.4 mg/cm^2 range, not showing any trend or correlation with the powder particle size.

The several microcrystalline silicon pre-ribbons, produced by the CVD system, had an almost smooth light to medium grey surface and showed little or no visual signs of surface porosity. Only pre-ribbons grown over powder substrates with particle size lower than 106 µm could be removed intact from the quartz substrate holder. Pre-ribbons grown over]106; 180] µm powder

substrates became partially glued, and pre-ribbons grown on]180; 250] µm powder substrates became completely glued to the quartz surface. Therefore, with the current CVD setup and experimental procedure, the actual size range of silicon powders that can be used as a substrate goes from nanometric sized up to around 100 µm.

A clear relation between pre-ribbon and CVD process properties such as growth rate, porosity or powder ratio and the substrate particle size was proved.

The growth rate was 52.8 ± 6.2 µm/min for the smallest particle size powder substrate (≤25 µm), decreasing as the particle size increases, following an apparent exponential decay down to 26.4 ± 4.0 µm/min for the]106; 180] µm particle size powder. Therefore, the growth rate of micrometric sized powders ranges between the nanometric sized powder's (up to 90 µm/min) and the solid substrates' (varying from 1.03 ± 0.12 to 9.69 ± 0.72 µm/min).

The pre-ribbons porosity is always lower than the porosity of the corresponding powder substrate over which the pre-ribbon was grown. It is also evident a slight raise of pre-ribbon porosity with increasing particle size, from 52.7 ± 7.3% for the ≤25 µm powder substrate until stabilizing around 59% for higher particle size powders.

The powder ratio varied between 0.60 ± 0.01 and 0.80 ± 0.01, increasing with the powder particle size, a trend due to growth rate being greater on finer powder and for this reason more silicon from the gaseous phase is deposited. These values prove that most of the silicon material in the pre-ribbon came from the powder substrate.

Both growth rate and pre-ribbon porosity distribution, can be explained by the increase of the effective deposition area when powder particle size decreases, since the higher density of dangling bonds, either Si-H or -Si, acting as deposition sites, increases the rate of occurrence of the heterogeneous reactions responsible for silicon deposition on a solid substrate.

The success of the ZMR process was influenced by two main factors: the concentration of oxide in the pre-ribbon surface and the pre-ribbon properties.

If a high concentration of oxide was present over the molten zone, the inability to remove it would result in an increased difficulty in monitoring and controlling the recrystallization, with an adverse impact on the quality of the process, resulting either in incomplete (or superficial) recrystallization or in a collapsed molten zone.

The most probable sources of oxide contamination were the silicon powder substrate due to its high surface area and the pre-ribbon. Despite pre-ribbons going through a 2 vol% HF bath before recrystallization, although an incomplete oxide removal cannot be excluded, it is possible that a rapid re-oxidation occurs prior to the ZMR process.

When the molten zone is not affected by oxide, its stability depends mostly on the substrate powder particle size, powder incorporation into the pre-ribbon, and pre-ribbon porosity and thickness. Pre-ribbons grown over smaller particle sized powder substrates (≤75 μm) delivered better results, since they have lower porosity and lower powder ratio. Moreover, pre-ribbons with lower thickness resulted in more stable molten zones.

Regarding the oxide presence, the recrystallized ribbons could be divided into two groups: a first group of pre-ribbons, measuring approximately 25×41 mm^2, where oxide was present and hindered the ZMR process, and a second group of pre-ribbons, measuring approximately 26×67 mm^2, in which oxides levels were low, allowing large ribbon areas to be recrystallized.

In the first group of pre-ribbons, small areas measuring around 5-20 mm^2, were successfully crystalized, leading to an average crystal size in the 0.1 to 1.0 mm range. The thickness of recrystallized areas varied from 240 to 300 μm and 330 to 350 μm in ribbons obtained with powder substrates of]75; 106] μm and nanometric range particle sizes, respectively.

In the second group of pre-ribbons, the largest recrystallized area was obtained with a pre-ribbon grown over a powder substrate of]45; 75] μm, having a multicrystalline area of approximately 2×4 cm^2, with visible columnar crystal growth on both sides, and a crystal size in the 1 to 10 mm range. In terms of crystallized area, this is the best result ever achieved by the SDS technique, surpassing the previous record of a 2.2×2.2 cm^2 multicrystalline area.

The lower oxide content in the second group of recrystallized pre-ribbons can be explained by the use of a different batch of powders, prepared with a smaller amount of silicon wafers, therefore the exposure time of the powders to the test sieves and the atmosphere was substantially decreased.

Non-destructive methods were used to characterize the best multicrystalline silicon material obtained, not submitted to a doping step: the measured resistivity and minority carrier lifetime were 0.70 ± 0.05 Ω.cm and 0.3 ± 0.1 μs, respectively.

The resistivity value is equivalent to a dopant concentration of 2.1×10^{16} cm^{-3}, the same order of magnitude as the p-type wafers (~10^{16} cm^{-3}) used to produce the silicon powders. It is a clear evidence of a very significant powder incorporation from the substrate during the CVD step, in accordance with the calculated values of pre-ribbons powder ratio (between 0.60 ± 0.01 and 0.80 ± 0.01), hence, the powder represents 60 to 80% of the final ribbon material.

The lifetime of the recrystallized ribbon was 85% lower than the value for a p-type wafer, an indication of an inferior crystalline quality and possible presence of metallic impurities and also oxygen aggregates acting as recombination centres.

On the recrystallized areas of the phosphorous doped ribbon, very high resistivity values (>10 Ω.cm) were measured. This is a clear evidence of dopant compensation between the n- and p-type dopants, since the pre-ribbons powder ratio is in the 0.60 to 0.80 range and the powder substrate was obtained from grinding silicon wafers with 10^{16} boron atoms/cm^3.

The feasibility of the SDS technique has been clearly demonstrated, with the three processes (powder production, CVD and ZMR) being able to operate continuously and delivering the base material to be used in the next step. Nevertheless, some important aspects have to be addressed, in order to improve SDS technique and increase the quality of the powder substrates, pre-ribbons and final multicrystalline silicon ribbons.

4.2. Future Work

Solar cells are currently being produced with the best multicrystalline silicon ribbons obtained during the experimental work of this thesis. Their properties will serve as a baseline for comparison with future silicon ribbons produced after new improvements being made to the SDS technique.

The first step, the production of silicon powders, requires a greater effort on reducing contaminants, especially oxide compounds. Both the mechanical grinding, performed with the SDS-crusher and SDS-grinding mill, and the mechanical segregation of the powders into narrower size distributions, using test sieves, should be carried out under a controlled atmosphere with low or no oxygen content. Additionally, the test sieves with metallic meshes must be replaced by a non-metal mesh material (e.g., plastic or polymer), to reduce metal contamination.

The second step, the production of microcrystalline silicon pre-ribbons by CVD, holds the most critical process, that influences the remaining process up to the final multicrystalline silicon ribbon: the preparation of powder substrates.

The powder substrate making technique should be entirely reworked, going from a manual and operator dependent process to a more automated and reliable technique capable of delivering reproducible substrates under the same experimental parameters. The production of powder substrates should aim for the minimum amount of powder, spread over the highest area, while maintaining a homogeneous, low thickness and highly compressed silicon powder substrate. This could be achieved by putting a frame over the quartz substrate holder, pouring a fixed amount of powder optimized for the area of the frame, vibrating the system with an ultrasonic agitator to homogenize the powder and finally compacting the substrate with a press. Compaction pressure values within the 1 to 10^3 MPa range could be reached, being 2 to 5 orders of magnitude higher than the values obtained when manually compressing the substrate, but well below the Young's modulus value for quartz (70-75 GPa), thus ensuring the substrate holder structural integrity during powder compaction.

The third step does not require major optimizations, since the success of the ZMR process depends mostly on the properties of the pre-ribbon to be recrystallized.

Pre-ribbons should have the following properties: (i) low porosity as it increases the stability of the molten zone and the success rate of the ZMR process: (ii) lower powder ratio (no greater than 0.1), as it will deliver an intrinsic silicon pre-ribbon that could be either p or n-doped in an extra step by an already develop method of spraying boric or phosphoric acids over the pre-ribbons; and (iii) thickness around 250-500 μm, since during the ZMR the pre-ribbon thickness reduction is around 40-60%, resulting in a final multicrystalline ribbon thickness of 150-200 μm, in accordance with industry requirements. These objectives for pre-ribbon properties could be achieved with an enhanced process to produce powder substrates, as previously stated.

Finally, the CVD and ZMR processes could be redesigned to become a fully inline system, operating in a continuous mode, hence reducing the handling time of the pre-ribbons. This is a challenging objective as it will require an extensive modification of both SDS-CVD and SDS-ZMR reactors or even newly built reactors.

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