Low Phase Noise Frequency Synthesis for Ultra-Stable X-Band Oscillators

Waddah A. Al-Ashwal *Member, IEEE*, Ashby Hilton, Andre N. Luiten, John G. Hartnett

***Abstract*—In this paper the design of a low phase noise frequency synthesizer is presented. The synthesizer was designed to produce four frequencies: 10 MHz, 100 MHz, 1 GHz and 10 GHz. The 1 GHz and 10 GHz signals are produced by frequency division whereas the 100 MHz output is generated by phase-locking a low phase noise oscillator to the 1 GHz signal, hence significantly reducing its phase noise. Both residual and total phase noise measurements are presented.**

***Index Terms*—Frequency Synthesis; Frequency Meteorology.**

I. Introduction

Clocks and oscillators are the most accurate and precise devices ever constructed by mankind. The performance of the best of these devices is exploited by modern communication systems, radar and radio astronomy [1]–[4].

Whispering gallery mode cryogenic sapphire oscillators have very high frequency stability [4]. The disadvantage of this technology is that, unlike an atomic clock, it does not deliver a signal at a precisely defined frequency. It is thus necessary to take the output of the oscillator, which in a cryo-cooled sapphire oscillator (CSO) is at X-band, and reliably synthesize the desired signal frequencies without significant loss of signal fidelity.

Here we introduce a simpler architecture for frequency synthesis that has improved the performance of the synthesized signals from our X-band CSO.

II. Frequency Synthesis

We have constructed several cryogenic sapphire oscillators [5]–[7]. The dielectric resonator is a HEMEX grade cylindrical sapphire crystal with an unloaded quality factor $\mathrm{Q}_0 > 1 \times 10^9$ at the operating temperature ≈5–6 K [7]. The oscillators operate on the $\mathrm{WGH}_{16,0,0}$ mode of the resonator[1] which has a resonance frequency of about 11.2 GHz. The manufacturing tolerances mean that the mode frequency is within ±2 MHz of this nominal value. The fractional frequency stability of the oscillators are in the 10^{-15} to 10^{-16} range. Our design is intended to generate exactly 10 MHz, 100 MHz, 1 GHz and 10 GHz from this arbitrary oscillation frequency while preserving most of the outstanding performance.

Manuscript received March 9, 2016; revised July 28, 2016, and September 14,2016; accepted January 16, 2017. This work is supported by the Australian Government Defence Science and Technology Group.

The authors are with the Institute for Photonics and Advanced Sensing (IPAS), School of Physical Sciences, University of Adelaide, Adelaide, Australia. Email: waddah.al-ashwal@adelaide.edu.au

[1]WGH is the whispering gallery mode in which the magnetic field (H) is perpendicular to the cylinder axis.

The initial synthesis step is to shift the microwave mode frequency to be exactly 11.2 GHz by summing the output of the resonator with a user-defined frequency derived from a direct digital synthesizer (DDS). The output of the DDS is mixed with a buffered copy of the output of the oscillator we use an I-Q mixer and the correct sideband is chosen [4]. We drive the DDS with a signal derived from the microwave signal itself. The noise contribution from the DDS and the Analog Devices dividers has been discussed in [4]. Unlike [4] we have used the harmonics of the divide-by-7 frequency divider, hence greatly simplifying the design when compared to that previous work. In addition we have used a low phase noise quartz oscillator to clean up the signal synthesized from the CSO output. A simplified schematic of the frequency synthesis system is shown in Fig. 1.

For example, to generate 1 GHz, the 11.2 GHz signal is divided by 2 then by 4 to generate 1.4 GHz. The 1.4 GHz signal is divided by 7 using a programmable digital divider. The output of the divider is a 200 MHz square wave. The fundamental (200 MHz) and the second harmonic (400 MHz) are used. The 1.4 GHz signal is mixed with the 400 MHz signal to generate 1 GHz. The 200 MHz signal is used to clock the DDS and is mixed with the 1 GHz signal to generate 1.2 GHz, which is mixed with 11.2 GHz to generate 10 GHz. In the above design the 100 MHz and 10 MHz signals cannot be generated directly. To generate 100 MHz directly the digital divider could be programmed to divide by 14 resulting in a 100 MHz fundamental and the second and fourth harmonics could be used to generate the 200 MHz and 400 GHz signals.

The phase noise can be improved by using a phase-lock loop (PLL). Following the analysis in [2], [8] it can be shown that the phase noise of the output of the PLL is approximated by:

$$\mathcal{L}_{\mathrm{out}}(f) = \begin{cases} \mathcal{L}_{\mathrm{ref}}(f) - 20\log\left(1 + \frac{f_{\mathrm{ref}}}{f_{\mathrm{out}}}\right) & \text{if } f < f_c, \\ \mathcal{L}_{\mathrm{vco}}(f) & \text{if } f > f_c, \end{cases}$$

where $\mathcal{L}_{\mathrm{ref}}(f)$, $\mathcal{L}_{\mathrm{vco}}(f)$ and $\mathcal{L}_{\mathrm{out}}(f)$ are the single sideband (SSB) phase noise of the reference (derived from the CSO), the voltage controlled oscillator and the output respectively. The parameter f represents the offset frequency and f_c the cutoff frequency of the PLL filter. Hence, by phase-locking a low phase noise oscillator to a higher frequency 'reference' derived from the CSO we can reduce the phase noise within the bandwidth of the PLL (provided that the residual phase noise of the PLL is much lower than that of the divided down signal), while the phase noise outside the bandwidth of the

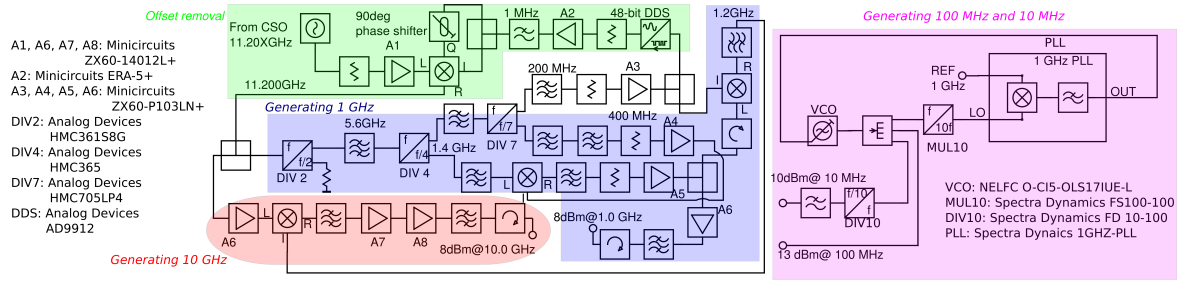

Fig. 1. Generating 10 GHz, 1 GHz, 100 MHz and 10 MHz. The phase noise contribution of the Analog Devices dividers, DDS and Minicircuits amplifiers has been discussed in [4]. The effect of other devices is discussed in the text.

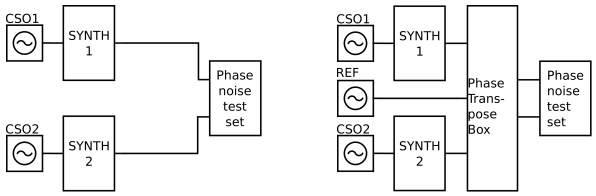

Fig. 2. Measuring the total phase noise of the synthesizers, left when the signal is less than 400 MHz and right when the signal is greater than 400 MHz.

PLL filter is set by the free running VCO. In our case we phase-locked a low phase noise 100 MHz VCO, which has SSB thermal noise floor better than −187 dBc/Hz and pull range of ±3 ppm, to the 1 GHz signal derived from the CSO as shown in Fig. 1. The PLL system, including the multiplier, has a residual phase noise of around −139 dBc/Hz @1 Hz which results in an overall phase noise of −131 dBc @1 Hz. The 10 MHz signal is then derived by frequency dividing the 100 MHz signal by 10. The divider has a SSB residual phase noise of −141 dBc/Hz @ 1 Hz.

III. Frequency Stability Results

Two independent CSOs were used in the measurements as shown in Fig. 2. For residual phase noise measurements the output from a single CSO was split and used to drive both synthesizers. The data were recorded using a Symmetricom 5125 A phase noise test set. When the signal frequency was higher than the bandwidth of the test set of 400 MHz, the method described in [9] was used, see Fig. 2. The phase noise of the phase noise transfer system was at least 10 dB better than that of the signal being measured at all frequency offsets. The Allan deviation was computed using the test set with a noise equivalent bandwidth of 0.5 Hz.

In Figs. 3 and 4 we present the residual and total SSB phase noise ($\mathcal{L}(f)$) and fractional frequency stability ($\sigma_y(\tau)$) of the synthesized signals. A comparison between the residual phase noise and Allan deviation of the 10 MHz and the 100 MHz signals with and without the PLL is shown in Fig. 3. As can be seen from the top panel of Fig. 3 the close-in phase noise was improved by more than 5 dB for the 10 MHz signal and around 4 dB for the 100 MHz when using the PLL compared to when using the programmable divider only. The improvement in the thermal noise was more than 20 dB and the measurement was limited by the noise floor of the test set. The white noise floor of the VCO used is about −187 dBc/Hz for $f > 10$ kHz.

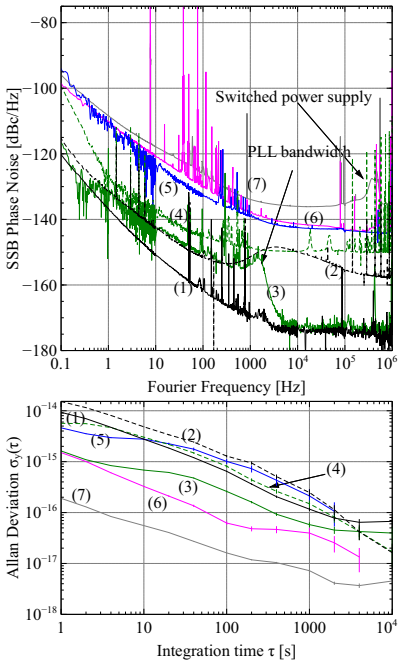

Fig. 3. Residual phase noise and fractional frequency stability measurement of synthesized signals. Top panel phase noise and bottom panel Allan deviation. (1) 10 MHz using a PLL, (2) 10 MHz without using a PLL, (3) 100 MHz using a PLL, (4) 100 MHz without using the PLL, (5) 400 MHz, (6) 1 GHz and (7) 10 GHz. In the phase noise plot the hump in (1) and (3) is due to the PLL, the spikes at 1.4 Hz and its multiples are due to the cyro-cooler and the hump at high frequency in (7) is due to the switching regulator noise leaking though the clean up linear regulators. Note that (1) and (3) are at the noise floor of the phase noise test set.

It is also worth noting from Fig. 3 that the phase noise of the 100 MHz signal within the bandwidth of the PLL is around 18 dB lower than that at 1 GHz. It can also be seen that the phase noise at 1 GHz is very close to that at 400 MHz. This indicates that the programmable divider sets the limit for the 1 GHz signal since it is generated by mixing its output with 1.4 GHz. The improvement is also reflected in the Allan deviation plots in the bottom panel of Fig. 3 which clearly shows that the frequency generated using a PLL has significantly better short term and long term stability.

The temperature of the synthesizers is not actively controlled. Fig. 3 shows that room temperature variations have negligible effect at the current level of performance.

The total phase noise and fractional frequency stability of the synthesized signals are presented in Fig. 4. The total phase

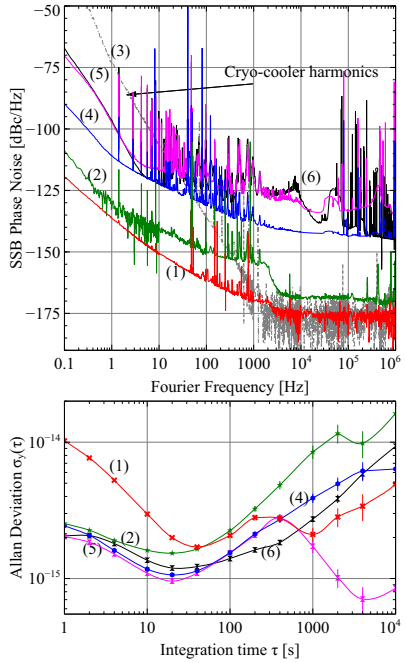

Fig. 4. Total phase noise and fractional freqeuncy. Top panel phase noise and bottom panel Allan deviation. (1) 10 MHz using a PLL, (2) 100 MHz using a PLL, (3) Free running 100 MHz oscillator, (4) 1 GHz, (5) 10 GHz and (6) CSO at 11.2 GHz. In the phase noise plot the hump in (1) and (2) is due to the PLL, the spikes at 1.4 Hz and its multiples are due to the cyro-cooler and the hump at a frequency offset about 300 kHz in (5) is due to the switching regulator noise leaking through the clean up linear regulators. Note that (1) and (2) are at the noise floor of the phase noise test set. Also note that setting the corner of the PLL loop filter below 1 kHz would have resulted in higher phase noise in the output signal at offset frequencies < 1 kHz.

TABLE I
SUMMARY OF TOTAL PHASE NOISE AT 1 HZ OFFSET.

Signal frequency	$\mathcal{L}$(1 Hz)
10 MHz	−137 dBc/Hz
100 MHz	−130 dBc/Hz
1000 MHz	−112 dBc/Hz
10 000 MHz	−97.4 dBc/Hz
11.2 GHz	−97.4 dBc/Hz

noise is almost identical to the residual phase noise except at 10 GHz. This is consistent with the phase noise of the CSO, referred to the measured frequency, being lower than the residual phase noise of the synthesizer except at 10 GHz. This confirms that the method used to cancel the offset from 11.2 GHz has a negligible effect. The phase noise results are summarized in Table I.

The increase in frequency instability at integration times > 100 s, as seen in Fig. 4, is due to the resonator sensitivity to room temperature as the data were recorded during different days with different ambient temperatures and at different times after the startup of the CSOs. In addition, Figs. 3 and 4 show a number of narrow spikes associated with ambient electrical and vibration environments. Although the peak phase noise values for the spikes are high, the total energy carried by these unwanted signals is small due to their narrowness.

Our results compare well with other published results. In reference [10], 8 GHz was generated from an optical frequency comb then divided down to various RF frequencies using a combination of off-the-shelf frequency dividers and specially designed divide-by-2 regenerative frequency dividers. The close-in phase noise of the signals synthesized is comparable to our results, whereas the white noise floor of our approach is around 10 dB lower. Vaillant *et. al.* [11] used a CSO using $WGH_{15,0,0}$ mode which has a resonant frequency around 10 GHz. They also used regenerative frequency dividers to ensure low phase noise. The close-in phase noise in [11], outperform our results by around 3 dB at 1 Hz offset at 100 MHz, while our thermal noise floor is better by more than 25 dB, except at 10 GHz.

IV. CONCLUSIONS

The design of an ultra low phase noise frequency synthesizer is presented and results analyzed. The aim of the synthesizer is to convert the output frequency of an ultra-stable X-band CSO to other desired frequencies. The techniques presented can be used to produce almost any desired RF or microwave frequency.

By using a PLL, a system could be built where a 1 GHz signal is transmitted long distances using rf-over-fiber. On the receiver side a PLL as shown in Fig. 1, can be used to phase-lock a low phase noise 100 MHz VCO for frequency dissemination. The bandwidth of the synthesis chain is limited by the tuning bandwidth of the VCO. Nonetheless, the synthesizers have sufficient bandwidth such that it is possible to syntonize the output to a specific reference such as a GPS receiver.

REFERENCES

[1] R. Rao and B. Daneshrad, "Analog impairments in MIMO-OFDM systems," *IEEE Transactions on Wireless Communications*, vol. 5, no. 12, pp. 3382–3387, Dec 2006.

[2] S. J. Goldman, *Phase Noise Analysis in Radar Systems Using Personal Computers*. Wiley, 1989, pp. 60–62.

[3] R. Raven, "Requirements on master oscillators for coherent radar," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 237–243, Feb 1966.

[4] N. Nand, J. Hartnett, E. Ivanov, and G. Santarelli, "Ultra-stable very-low phase-noise signal source for very long baseline interferometry using a cryocooled sapphire oscillator," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 11, pp. 2978–2986, 2011.

[5] J. G. Hartnett and N. R. Nand, "Ultra-low vibration pulse-tube cryocooler stabilized cryogenic sapphire oscillator with 10^{-16} fractional frequency stability," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3580–3586, 2010.

[6] J. G. Hartnett, N. R. Nand, and C. Lu, "Ultra-low-phase-noise cryocooled microwave dielectric-sapphire-resonator oscillators," *Applied Physics Letters*, vol. 100, no. 18, p. 183501, 2012.

[7] A. Hillton, "High-performance cryogenic sapphire oscillators," Master's thesis, The University of Western Australia, 2014.

[8] V. Kroupa, "Noise properties of PLL systems," *IEEE Trans. Commun.*, vol. 30, no. 10, pp. 2244–2252, 1982.

[9] J. Hartnett, S. Parker, and E. Ivanov, "Frequency transposing measurement technique for oscillator comparisons," *Electronics Letters*, vol. 49, no. 15, pp. 947–949, Jul 2013.

[10] A. Hati, C. W. Nelson, C. Barnes, D. Lirette, T. Fortier, F. Quinlan, J. A. DeSalvo, A. Ludlow, S. A. Diddams, and D. A. Howe, "State-of-the-art RF signal generation from optical frequency division," *IEEE tran. Ultra., Ferroelect., and Freq. Control*, vol. 60, no. 9, pp. 1796–1803, 2013.

[11] E. Vaillant, F. Sthal, J. Imbaud, Y. Gruson, C. Fluhr, S. Grop, V. Giordano, E. Rubiola, G. Cibiel *et al.*, "Frequency synthesis from cryogenic sapphire oscillator," in *European Frequency and Time Forum (EFTF2016)*, 2016.