Unveiling the Impact of IR-drop on Performance Gain in NCFET-based Processors

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***Abstract*—Negative Capacitance Field-Effect Transistor (NCFET) pushes the sub-threshold swing beyond its fundamental limit of 60 mV/decade by incorporating a ferroelectric material within the gate stack of transistor. Such a material manifests itself as a negative capacitance (NC) that provides an internal voltage amplification for the transistor resulting in higher ON current levels. Hence, the performance of processors can be boosted while the operating voltage still remains the same. However, having a negative capacitance makes the total gate terminal capacitance larger. While, the impact of that on compensating the gained performance has already been studied in literature, this work is the first to explore the impact of negative capacitance on exacerbating the IR-drop problem in processors. In fact, voltage fluctuation in the Power Delivery Network (PDN) due to IR-drops is one of the prominent sources of performance loss in processors, which necessitates adding timing guardbands to sustain a reliable operation during runtime. In this work, we study NC-FinFET standard cells and processor for the 7 nm technology node. We demonstrate that NC, on the one hand, results in larger IR-drops due to the increase in current densities across the chip, which leads to a higher stress on the PDN. However, the internal voltage amplification provided by NC, on the other hand, compensates to some degree the voltage reduction caused by IR-drop. We investigate, from physics all the way to full-chip (GDSII) level, how the overall performance of a processor is affected under the impact that NC has on *magnifying* and *compensating* IR-drop.**

***Index Terms*—Negative capacitance, NCFET, FinFET, IR drop, circuit simulation, processor performance, voltage fluctuation**

I. Introduction

NCFET: Negative capacitance FET (NCFET) is rapidly emerging as one of the promising technologies that can surmount the so-called Boltzman tyranny (i.e. the distribution of charge carriers at the source of transistor), which fundamentally limits the sub-threshold swing (SS) of transistors to be lower than 60 mV/decade at room temperature [1]. NCFET integrates a ferroelectric layer within the gate stack that exhibits a negative capacitance (NC). Recently, Krivokapic et al. [2] demonstrated the compatibility of NCFET with current CMOS technology through the integration of a doped HfO_2 ferroelectric layer in their state-of-the-art industrial 14 nm FinFET technology. [3] reported that in doped HfO_2 ferroelectrics, the intrinsic delay due to polarization damping in NCFET can be quite small ($\approx$ 270 fs) showing that NCFET is able to respond fast enough to voltage even circuits that have frequency switching in the GHz range like processors.

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Digital Object Identifier: DOI

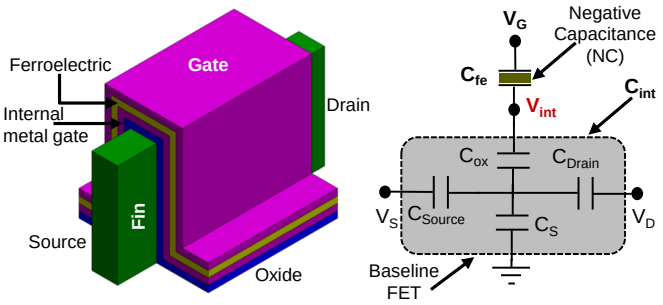

Fig. 1. The employed schematic of metal-ferroelectric-metal-insulator-semiconductor (MFMIS) and the corresponding equivalent circuit of the gate stack of NC-FinFET.

The configuration of metal-ferroelectric-metal-insulator-semiconductor (MFMIS) in NCFET can be represented as in Fig. 1, which also shows the equivalent capacitance divider circuit of the ferroelectric capacitance (C_{fe}) and the internal baseline FET capacitance (C_{int}). The voltage amplification (A_V) at the internal gate can be then expressed as in (1).

$$A_V = \frac{\partial V_{int}}{\partial V_g} = \frac{|C_{\text{fe}}|}{|C_{\text{fe}}| - C_{\text{int}}} \tag{1}$$

To ensure no hysteresis: $|C_{\text{fe}}| > C_{\text{int}} \Rightarrow A_V > 1$

$$V_{int} = A_{avg} V_g \quad \text{for a fixed } V_d; \quad A_{avg} = \frac{1}{V_g} \int_0^{V_g} A_V \, dV_g \tag{2}$$

In turn, the provided voltage amplification by the ferroelectric layer will enable the NCFET to always reach a higher internal gate voltage V_{int} according to (2) and hence, a higher ON current (I_{ON}) at the same voltage. The maximum frequency of circuit is governed by the I_{ON} of transistors that form its critical path. Therefore, NCFET-based processors have, at the same voltage, higher performance compared to conventional FET that has no ferroelectric layer [4].

Switching Power: The switching power ($P_{switching}$) of a circuit is determined by the switching activity (α), total capacitance (C), operating voltage (V_{DD}) and frequency (f), as (3) shows.

$$P_{switching} = \alpha \frac{V_{DD}}{T} \int_0^T I_{DD}(t)dt = \alpha C V_{DD}^2 f \quad (3)$$

If the C_{fe} exhibits a negative value and the condition of $|C_{\text{fe}}| > C_{\text{int}}$ is always met in the range of operating voltages to ensure no hysteresis, then the total capacitance of NCFET is always larger than the baseline FET (C_{int}), as (4) shows.

$$C_{NCFET} = \frac{C_{\text{fe}} \cdot C_{\text{int}}}{C_{\text{fe}} + C_{\text{int}}} > C_{\text{int}} \quad (4)$$

Therefore, compared to conventional FET, NCFET-based circuits will dissipate a higher switching energy as it will exhibit a larger total capacitance at the same V_{DD}.

IR-drop: Voltage drop in metal lines is a fundamental property of any circuit due to the non-ideality in the Power Delivery Network (PDN), which originates from the intrinsic parasitics (e.g., resistances and capacitances of power lanes) inside PDN [5]. IR-drop results in sudden reductions in V_{DD} that reaches cells and hence reduction in I_{ON} of transistors because the latter is proportional to $(V_{DD} - V_T)$. With each clock, the simultaneous switching of standard cells results in peaks in driving current and due to the inability of PDN to deliver the required currents, both V_{DD} and V_{SS} fluctuate at the terminals of standard cells leading to increase in delay. To protect against IR-drop effects and thus sustain reliable operation, a timing guardband (i.e. an extra time slack) should be included on top of the maximum delay of processor to prevent unpredictable timing violations during runtime. Such a guardband directly leads to a loss in performance as the processor will be clocked at a lower frequency than its full potential.

Key focus on this work: NCFET exhibits a larger gate capacitance and therefore the total capacitance of standard cells in NCFET technology are larger compared to conventional FET. Such an increase results in higher current densities across the chip. Thus, NCFET-based processors will be, in general, subjected to higher IR-drops leading to unforeseen performance losses. Evaluating the performance gain in circuits, obtained by NCFET technology, in isolation from IR-drop – as done in state of the art [6], [7] – might lead to overestimating the potential impact of NCFET on circuit's performance. At the same time, the voltage amplification at the internal gate offered by the ferroelectric layer provides a compensation for the voltage reduction caused by induced IR-drop. This, in turn, can mitigate to some degree the deleterious impact that IR-drop has on the circuit's delay.

II. Modeling the Impact of NCFET from Physics to Full-Chip (GDSII) Processor Level

Fig. 2 demonstrates the overview of our implemented design flow in which the effects of NC are modeled and analyzed from physics to standard cell libraries all the way to the full-chip design where the effect of IR-drop on processor are accurately analyzed along with incurred losses in performance.

Physics and Device Modeling: We consider an NC-FinFET with a configuration of MFMIS as shown in Fig. 1. The structure can be equivalently divided into the ferroelectric capacitor (C_{fe}) and the internal baseline FinFET (C_{int}). The voltage amplification due to the ferroelectric layer is calculated as in (1). The baseline FinFET part of the device is modeled by the industry standard BSIM-CMG model, which considers both the short-channel and quantum-mechanical effects in small geometries [8], [9]. The ferroelectric layer is modeled as shown in (5), which is based on Taylor series as in the Landau-Khalatnikov (L-K) theory [10], [11].

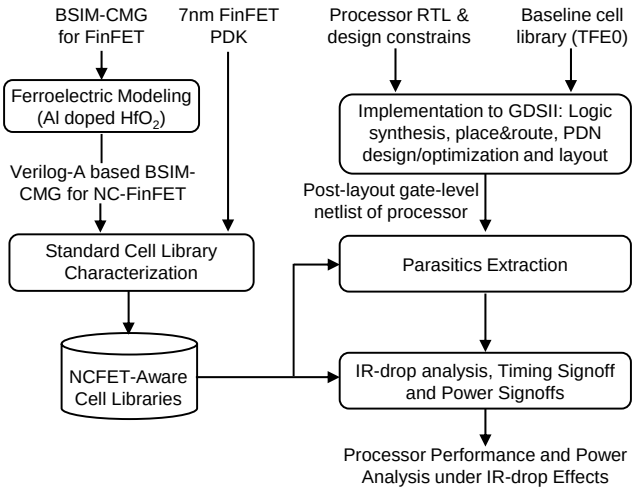

Fig. 2. Our implemented design flow. NC effect is modeled within the Verilog-A code of BSIM-CMG for FinFET. The modified model is used to create NCFET-aware standard cell libraries for the 7nm technology node. Using commercial synthesis and layout tool flows, a processor is implemented to the GDSII level. Finally, IR-drop, delay and power are accurately analyzed, using commercial timing and power signoff tool flows, for the final processor's layout including full parasitics.

$$V_{\text{fe}} = t_{\text{fe}}(2\alpha Q + 4\beta Q^3) \quad (5)$$

Where V_{fe} is the voltage across ferroelectric, Q is the gate terminal charge per unit area, t_{fe} is the thickness of ferroelectric. α and β are ferroelectric material dependent parameters [10], [12]. The L-K equation is then solved in a self-consistent manner within the Verilog-A code of BSIM-CMG model of FinFET [9] using a commercial SPICE simulator [13]. To model the FinFET parameters, we employ the $7\,\text{nm}$ Process Design Kit (PDK) [14]. Regarding the ferroelectric layer, we adopt Al doped HfO_2 material as it is a CMOS compatible material [15]. To calculate the α and β in the L-K equation, we use the remnant polarization of 0.05 μC/cm^2 and the coercive field of 1 MV/cm based on the experimental data in [15].

NCFET Standard Cell Libraries: The Verilog-A code of NC-FinFET, obtained from the previous step, is then employed within a commercial cell library characterization tool flows [16] to create NCFET-aware cell libraries in which the delay and power of standard sequential and combinational cells are extracted under the effects of NC. The post-layout cells' netlists (which include the parasitics information), obtained from the used $7\,\text{nm}$ PDK [14], are employed during the characterization to create the NCFET-aware cell libraries. Every cell is characterized under 7 input signal slews and 7 output load capacitances, as done in the original cell library.

Full-Chip Design: The created NCFET-aware cell libraries are compatible with the existing commercial EDA tool flows like [17], [18]. Therefore, we can employ them directly within the standard flow of chip design. First, we synthesize the

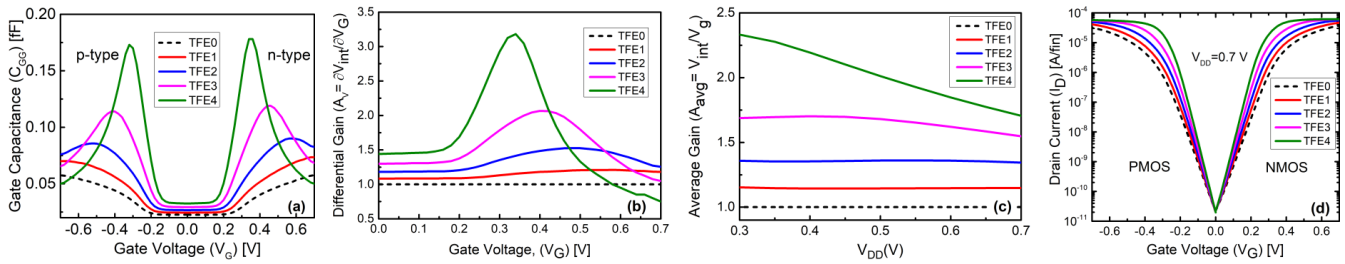

Fig. 3. Device-level analysis for the effects of different ferroelectric layers with varied thicknesses. (a) shows the increase in the gate capacitance due to the negative capacitance. (b) shows the differential gain over V_g. (c) shows the average gain. (d) presents the I_d current over V_G (at $V_{DS} = 0.7$V) demonstrating the increases in I_{ON} and the reductions in SS. In general, the thicker the ferroelectric layer, the higher the gain but, as a result, C_{GG} becomes much larger.

Register-Transfer Level (RTL) of processor using the baseline/original (i.e. conventional FinFET) cell library using a commercial logic synthesis tool [17]. Then, we implement the full design all the way to the GDSII level using commercial layout tool flows [18]. Because starting from a well-optimized PDN is important to have proper IR-drop analysis, the PDN has been iteratively optimized until the static IR drop becomes 0 and the dynamic IR-drop becomes around 2% (i.e. merely 0.017V at the nominal V_{DD} of 0.7V). For accurate investigation of the effects of NCFET on IR-drop and delay/power of processor, commercial power signoff [19] and delay signoff [20] tools are used for the post-layout processor's gate-level netlist along with our created NCFET-aware cell libraries. In this work, we study the 32-bit processor [21], which is based on state-of-the-art RISC-V architecture [22].

Case Studies: We consider, in addition to the baseline (TFE0) where no ferroelectric layer is in use, four different NCFET cases, namely TFE1, TFE2, TFE3, TFE4 corresponding to four thicknesses of the ferroelectric layers: t_{fe}= 1, 2, 3 and 4 nm, respectively. For $t_{\text{fe}} \geq 5$ nm, we observed that a hysteresis-free operation, which is necessary for CMOS logic applications, cannot be anymore ensured. For fair comparisons, the four NC-FinFET devices are calibrated through gate work-function tuning in which iso-I_{OFF} condition is acquired (i.e. same OFF current as that of the baseline TFE0 at the nominal voltage of $V_{DD} = 0.7$ V). Every created cell library (i.e. TFE0, TFE1, TFE2, TFE3 and TFE4) is characterized under the nominal V_{DD} of 0.7V (as specified in the employed 7 nm PDK), in addition to 0.6V and 0.5V for a comprehensive analysis. Since the IR-drop characteristic is subject to the switching activities (α) running on top of the processor, we study two different scenarios: $\alpha = 20\%$ and 30%. We selected these values in which the resulting IR-drop is within the IR-drop range caused by several representative application benchmarks (i.e. workloads) which we examined on top of the processor. In our analysis, we always extract the occurring IR-drop in all gates/cells across the processor's chip and then we report the maximum (i.e. worst-case) IR-drop.

III. Device-Level and Gate-Level Analysis

Fig. 3 summaries the device-level analysis. As can be noticed in Fig. 3(a), the existence of NC makes the total gate capacitance (C_{GG}) of NC-pFinFET and NC-nFinFET larger [23]. As expected, the thicker the ferroelectric layer, the larger the NC is and hence the C_{GG} becomes larger as well [23]. In general, the increase in C_{GG} is higher at lower V_G with a sharp peak at around 0.35V for the case of TFE4. Fig. 3(b) demonstrates the differential gain ($A_V = \partial V_{int}/\partial V_G$) obtained by NC. Note that even though the differential gain might be less than 1 (see A_V at $V_G \geq 0.6$V), the average gain (A_{avg}) is always greater than 1 as shown in Fig. 3(c), which results in decreasing the sub-threshold swing and increasing the ON current, as Fig. 3(d) shows. In summary, the thicker the ferroelectric layer, the higher the gain is but, as a result, the C_{GG} becomes much higher (see TFE4 in comparison to other cases). Such an increase in C_{GG} will lead later to higher current densities across the chip and thus larger IR-drops, which, in turn, causes performance loss as will be demonstrated in Section IV.

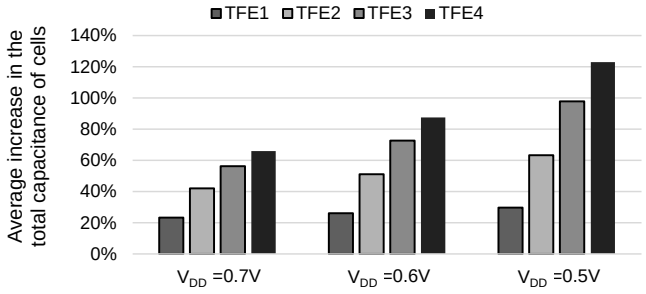

Fig. 4. Analyzing the increase in the cells' capacitance in the 7 nm FinFET standard cell library due to the integration of NC at varied voltages. The average increase across all standard cells is reported. The thicker the ferroelectric layer, the larger the increase in the cells' capacitance becomes. This is consistence with the previous observation in Fig. 3(a).

In Fig. 4 we present the average increase in the total capacitance of gates across all standard cells within the used 7 nm FinFET standard cell library. As can be noticed, the thicker the ferroelectric layer, the larger the increase in the cells' capacitance and the standard cells exhibit a larger increase in the total capacitance at lower voltages. Both observations are consistent with the presented results earlier in Fig. 3(a).

IV. Processor-Level Analysis

As motivated in Section I, NCFET magnifies IR-drops across the chip due to the larger current densities across the chip leading to a higher stress on the PDN. However, the voltage amplification provided by the NC compensates to some degree the reduction in voltage caused by IR-drop. In the following, we study the aforementioned *magnification* and *compensation* effects of NCFET w.r.t IR-drop along with the overall impact on the performance of processor.

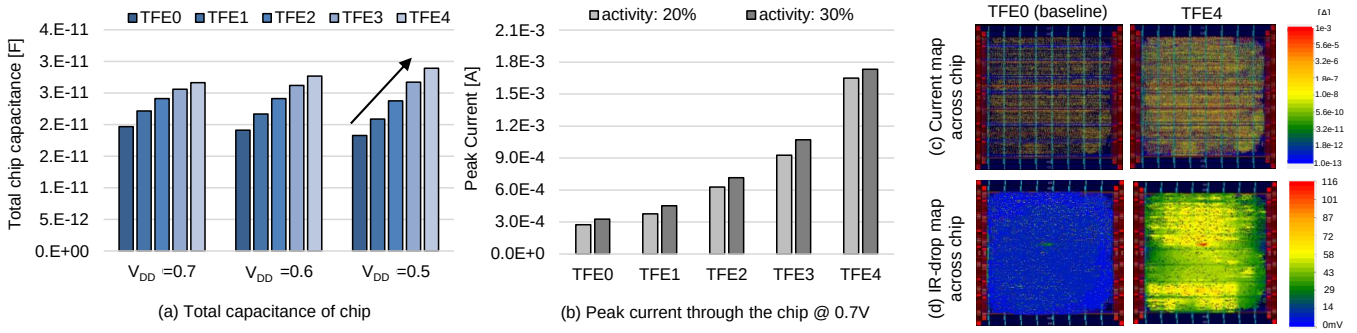

Fig. 5. (a) shows the total chip capacitance at different voltages for the four NCFET cases compared to the baseline (TFE0). (b) reports the peak current through the chip at two different switching activities (α=20% and 30%) and (c) shows an example of the current map across the chip for the case of TFE4 (t_{fe}=4nm) compared to the baseline (no ferroelectric) for α=20% and V_{DD}=0.7V. As shown in (a, b) the NC results in increases in the total capacitance and current of chip. This increases the stress on the PDN and hence the IR-drop in NCFET becomes larger as the IR-drop map in (d) demonstrates.

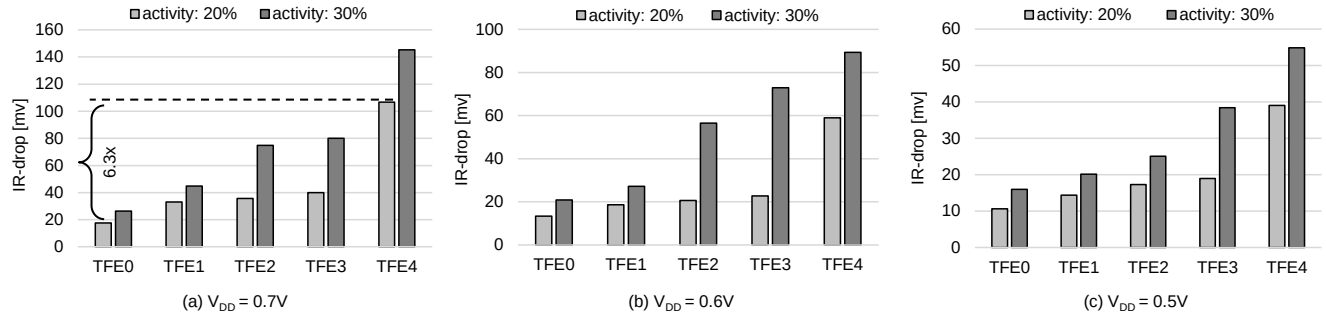

Fig. 6. IR-drop analysis for different NCFET cases compared to the baseline TFE0 for different V_{DD} and α cases. The higher the V_{DD} and/or α, the larger the IR-drop is. NCFET always results in much larger IR-drops which reaches around 6.3x in the case of TFE4 compared to TFE0, in the case of V_{DD}=0.7V.

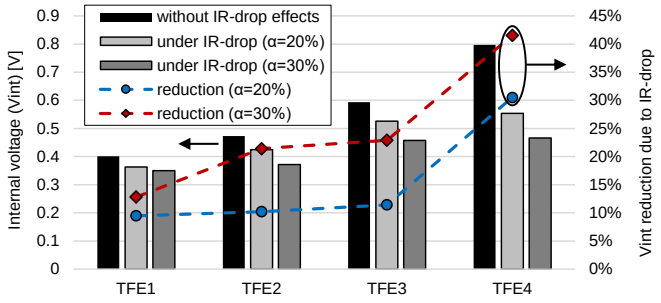

Fig. 7. Impact of IR-drop on reducing the internal voltage (V_{int}) of NCFET under different ferroelectric thicknesses. In this analysis, $V_G = V_{ds} = V_{DD}/2$ is considered, which approximately corresponds to the peak IR-drop condition during CMOS switching. Larger t_{fe} (e.g., TFE4) and/or higher α, IR-drop becomes larger (see Fig. 6) leading to a higher reduction in V_{int}.

A. Magnification Impact

Fig 5 demonstrates the NCFET effects at the chip level. As shown in Fig 5(a) the total chip capacitance increases when a thicker ferroelectric layer is in use. This is expected because the cells' capacitance become larger (see Fig. 4) due to the effect of NC on increasing the gate terminal capacitance of NC-FinFET (see Fig. 3(a)). The increase in the total chip capacitance results in higher currents as can be seen in Fig. 5(b), which shows the peak current across the chip for the two analyzed switching activities ($\alpha = 20\%$ and 30%) at $V_{DD} = 0.7$V. For instance, the chip in the case of TFE4 has around 4x higher current than the baseline TFE0 that has no ferroelectric. To clarify further, we show in Fig 5(c) a comparison of the current density map across the chip between TFE0 and TFE4 at $V_{DD} = 0.7$V and $\alpha = 20\%$. Such an increase in the current densities across the chip, in turn, increases the stress on the PDN because the power lanes need to provide higher currents to standard cells, leading to drops in the supply voltage that reaches cells, i.e. drops in both V_{DD} and V_{SS} from their ideal/nominal levels, which are 0.7V and 0V, respectively in the studied 7 nm PDK. This can be observed in Fig 5(d), which shows a comparison for the IR-drop map across the chip between TFE0 and TFE4.

In Fig. 6, we summarize the maximum IR-drop across the chip for the two different switching activities at the three different voltages (0.7V, 0.6V and 0.5V). As shown, using NC always leads to a larger IR-drop. The thicker the ferroelectric layer, the higher the IR-drop is. At higher α, the IR-drop becomes even larger due to the larger currents (see Fig. 5(b)). For instance, as shown in Fig. 6(a), at the nominal voltage (V_{DD}=0.7V) and α=20%, the maximum IR-drop in the baseline case (TFE0) is just 17mV[1]. However, using TFE4 leads to a maximum IR-drop of 107mV, which is 6.3x more than the baseline. Even for a thinner ferroelectric layers; TFE1, TFE2 and TFE3, the maximum IR-drop due to NC effects is already quite high, which reaches 89%, 104% and 128%, respectively, compared to the IR-drop at the baseline TFE0. On the other hand, when the voltage is scaled down, the IR-drop becomes, as expected, lower. However, the trend of having larger IR-drops, when NCFET is used, remains.

[1]This is merely 2.4% drop from the nominal voltage (V_{DD}=0.7V). Such a low IR-drop in the baseline shows that we start from a well-optimized PDN.

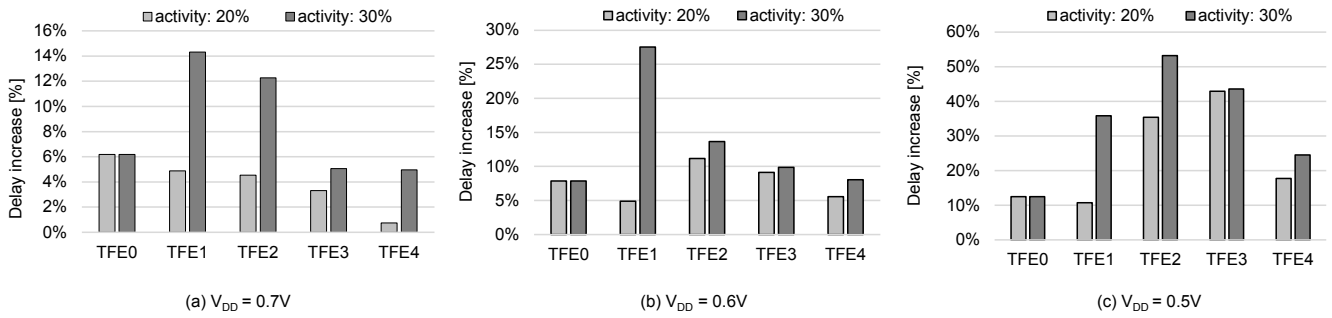

Fig. 8. The relative delay increase in processor due to the IR-drop for different $_{DD}$. Lower V_{DD} magnifies the effects of IR-drops due to the higher susceptibility of cells' delay to voltage reductions. For NCFET with thicker ferroelectric (e.g., TFE3 and TFE4), the higher voltage amplification provided by NC can compensate more the reduction in V_{DD} caused by IR-drop. This is despite the fact that IR-drop becomes higher at thicker ferroelectric (see Fig. 6).

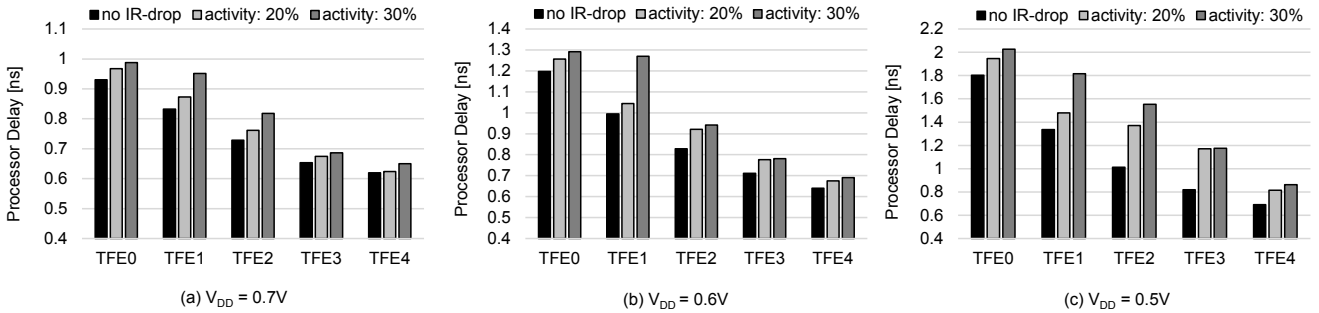

Fig. 9. Processor performance evaluation in the scope of *considering* and *neglecting* IR-drop effects. Considering IR-drop effects leads to reducing the potential gain from NCFET. Hence, neglecting IR-drop effects can lead to overestimating the potential gain of NCFET. The higher the IR-drop (i.e. due to higher switching activity α), the larger incurred loss. In Fig 10, we summarize the performance loss at each V_{DD} for the different NCFET cases.

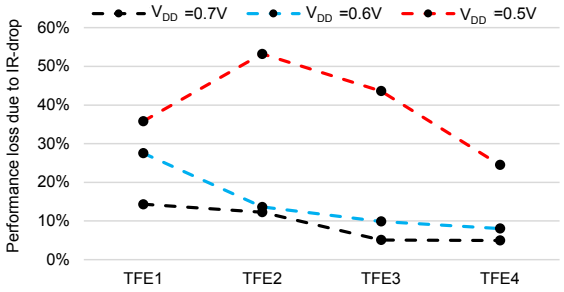

Fig. 10. Performance loss summary for the case of switching activity of $\alpha = 30\%$ caused by IR-drop demonstrating that neglecting IR-drop when investigating the gain of NCFET w.r.t processor's performance leads to noticeable overestimations. The maximum overestimation is at TFE2. After which (i.e. at thicker ferroelectrics in TFE3 and TFE4) the performance loss becomes smaller due to the higher gain/amplification provided by NC.

B. Compensation Impact

When IR-drop occurs, the gate terminal in transistors will receive a lower voltage than what it should be. At the same time, the negative capacitance provides a voltage amplification A_V (see (1)) that increases the internal voltage of gate V_{int} (see (2) and Fig. 1). Such an amplification can, in turn, compensate to some degree effect of IR-drop. Note that regardless the amplification impact due to NC, the internal voltage V_{int} after IR-drop is less than what it should be in the absence of IR-drop. Hence, a performance loss will properly be there, which depends on the intensity of the occurring IR-drop and the ability of NC to compensate. In Fig. 7, we show the reduction in V_{int} in NCFET. Note that V_{int} is calculated at $V_G = V_{ds} = V_{DD}/2$ (i.e. 0.35V), which approximately corresponds to the peak IR-drop condition during CMOS switching. For a thicker ferroelectric layer, the loss in V_{int} is higher because the IR-drop is larger (see Fig. 6). At a higher switching activity, the IR-drop is stronger leading to a further reduction in V_{int}. The reduction in V_{int} reaches around 30% and 41% in TFE4, which has the thickest ferroelectric layer (t_{fe}=4nm), for the case of α=20% and α=30%, respectively.

C. Timing Guardband Analysis

As explained in Section I, fluctuations in the voltage due to IR-drops cause sudden increases in the delay of critical paths of processor during runtime. This leads to an unreliable operation because timing constraints might be violated resulting in catastrophic timing errors. To keep the deleterious effects of IR-drops at bay, a timing guardband is typically added, during design time, on top of the maximum delay of processor in which any sudden delay increase caused by IR-drop during runtime is compensated and overcome. However, including a timing guardband results in a loss in the processor's performance and inefficiency because the processor will be clocked at a lower frequency than its potential. To put the impact of NCFET on IR-drop in context, it is necessary to also evaluate the resulting relative delay increase of the processor, which determines the required timing guardband and thus the incurred performance loss. Fig. 8 summarizes our analysis for the different V_{DD} and α. The relative delay increase due to IR-drop is much higher at lower V_{DD} even though the IR-drop itself is smaller at lower V_{DD} (see Fig. 6). This is expected because of the higher susceptibility of cells' delay to voltage

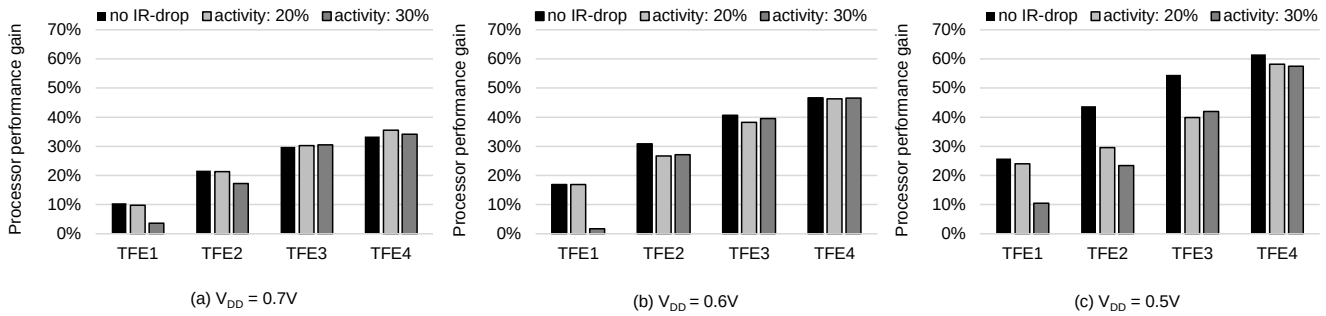

Fig. 11. Analysis of processor performance gain due to NCFET (relative to the baseline TFE0) with and without IR-drop under different V_{DD} and switching activities. IR-drop leads, in general, to a loss in the performance gain. However, despite such a loss, NCFET always boosts the processor's performance. The performance improvement is higher at lower V_{DD} due to the higher gain from NC (see Fig. 3(b, c)) as well as with the increase in the ferroelectric thickness.

reductions when V_{DD} is scaled down. Importantly, NCFET results in higher IR-drops (as shown in Fig. 6), however, the relative delay increase depends on the provided amplification voltage by NC (i.e., thickness of the ferroelectric). As shown in Fig. 8, when a thicker ferroelectric (e.g., TFE3, TFE4) is used, the relative delay increase becomes smaller compared to using a thinner layer (e.g., TFE1, TFE2), i.e. the deleterious effects of IR-drop are mitigated due to the larger V_A obtained from the thicker ferroelectric layer (Fig. 3(b, c)). *Therefore, even though a thicker ferroelectric leads to a larger IR-drop, the higher voltage amplification provided by NC can compensate that and the delay of processor will not be, at the end of the day, highly affected. Hence, a trade-off exists and finding the optimal thickness of ferroelectric necessitates considering IR-drop effects.*

D. Overall Processor's Performance Analysis

In Fig. 9 we present the processor's delay which, in practice, dictates the maximum clock frequency. Any increase in the processor's delay will lead to performance and efficiency losses due to the operation at lower clocks. As shown, NCFET always provides an improvement in the processor's performance that becomes more considerable as the thickness of the ferroelectric layer increases. This is expected due to the higher gain obtained by NC (see Fig. 3(c, d)). The improvement in performance becomes even larger as V_{DD} scales down due to the increase in the gain of NC (see Fig. 3(b, c)). When IR-drop effects are considered in the analysis, an increase in the processor's delay (i.e. a performance loss) is observed. Such a loss in performance becomes larger at a higher switching activity because of the higher induced IR-drop. In Fig. 10 we summarize the performance loss due to IR-drop for every NCFET case and V_{DD} case. The loss is between 5% and 14% when V_{DD}=0.7V and it becomes larger at lower V_{DD} reaching 50% when V_{DD}=0.5V. Note that the performance loss becomes smaller at thicker ferroelectric layers (TFE3, TFE4) because the provided gain by NC becomes larger compensating more IR-drop effects. *This again shows the necessity of considering IR-drop effects when investigating the impact of NCFET on processor's performance for accurate analysis.* Finally, we summarize in Fig. 11 the processor performance gain with and without IR-drop. Despite the performance loss caused by IR-drop, NCFET still always provides a boost in the performance and the gain becomes higher with the increase in the thickness of the ferroelectric layer.

V. Summary and Conclusions

In this work, we studied the impact of negative capacitance in $7\,\mathrm{nm}$ FinFET on increasing the IR-drop akin to the incurred increase in the gate capacitance of transistors and the consequences of that on the performance of processors. Our analysis starts from physics all the way to the final (GDSII) chip level. Using standard signoff tool flows for chip design, we investigated the impact of different NCFET technologies (represented by different ferroelectric layer thicknesses) on IR-drop and delay of a fully-implemented processor. We demonstrated that thicker ferroelectric leads to larger IR-drop due to the increase in the cells' capacitance but it, at the same time, provides higher voltage amplification that compensates to some degree the reduction in V_{DD} induced by IR-drop. Analyzing accurately the performance gain due to NCFET in processors necessitates considering the impact of NCFET on IR-drop effects.

References

[1] V. Zhirnov and R. K. V. Cavin, "Negative capacitance to the rescue?" *Nature Nanotechnology*, vol. 3, Feb. 2008, doi: 10.1038/nnano.2008.18.

[2] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz *et al.*, "14nm ferroelectric finfet technology with steep subthreshold slope for ultra low power applications," in *International Electron Devices Meeting (IEDM)*, Dec 2017, doi:10.1109/IEDM.2017.8268393.

[3] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *Electron Device Letters (EDL)*, vol. 38, no. 9, Sept 2017, doi:10.1109/LED.2017.2731343.

[4] H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative capacitance transistor to address the fundamental limitations in technology scaling: Processor performance," *IEEE Access*, vol. 6, pp. 52 754–52 765, 2018.

[5] P. Benediktsson, J. A. Flandrin, and C. Zheng, "Non uniform on chip power delivery network synthesis methodology," *Computing Research Repository (CoRR)*, 2017, doi:abs/1711.00425.

[6] S. K. Samal, S. Khandelwal, A. I. Khan, S. Salahuddin, C. Hu *et al.*, "Full chip power benefits with negative capacitance fets," in *International Symposium on Low Power Electronics and Design (ISLPED)*, July 2017, doi:10.1109/ISLPED.2017.8009170.

[7] H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative capacitance transistor to address the fundamental limitations in technology scaling: Processor performance," *IEEE Access*, vol. 6, 2018, doi:10.1109/ACCESS.2018.2870916.

[8] Y. S. Chauhan, D. D. Lu, S. Vanugopalan, S. Khandelwal, J. P. Duarte *et al.*, "Finfet modeling for ic simulation and design." Oxford: Academic Press, 2015, doi:https://doi.org/10.1016/B978-0-12-420031-9.00012-9.

[9] "BSIM-CMG Technical Manual," October 2018. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIMCMG

[10] D. Landau and I. M. Khalatnikov, "On the anomalous absorption of sound near a second order phase transition point," in *Dokl. Akad. Nauk SSSR*. Pergamon, 1954, doi:https://doi.org/10.1016/B978-0-08-010586-4.50004-3. [Online]. Available: http://www.sciencedirect.com/science/article/pii/B9780080105864500043

[11] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, "Physics of ferroelectrics: a modern perspective," vol. 105, 2007, doi:https://doi.org/10.1007/978-3-540-34591-6.
[12] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters*, vol. 8, no. 2, 2008, doi:10.1021/nl071804g. [Online]. Available: https://doi.org/10.1021/nl071804g
[13] "Synopsys HSPICE simulator," October 2018. [Online]. Available: https://www.synopsys.com/verification/ams-verification/circuit-simulation/hspice.html
[14] L. T. Clark, V. Vashishtha, L. Shifren, A. Gujja, S. Sinha *et al.*, "Asap7: A 7-nm finfet predictive process design kit," *Microelectronics Journal*, vol. 53, 2016, doi:https://doi.org/10.1016/j.mejo.2016.04.006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S002626921630026X
[15] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist *et al.*, "Incipient ferroelectricity in al-doped HfO2 thin films," *Advanced Functional Materials (ADFM)*, vol. 22, no. 11, pp. 2412–2417, mar 2012, doi:10.1002/adfm.201103119. [Online]. Available: https://doi.org/10.1002%2Fadfm.201103119
[16] "Synopsys SiliconSmart for cell library characterization," October 2018. [Online]. Available: https://www.synopsys.com/implementation-and-signoff/signoff/siliconsmart.html
[17] "Synopsys EDA Tool Flows," October 2018. [Online]. Available: https://www.synopsys.com/
[18] "Cadence EDA tool flows," October 2018. [Online]. Available: https://www.cadence.com/
[19] "Tempus Timing Signoff Solution," October 2018. [Online]. Available: https://www.cadence.com/content/cadence-www/global/en_US/home/tools/digital-design-and-signoff/silicon-signoff/tempus-timing-signoff-solution.html
[20] "Voltus IC Power Integrity Solution," October 2018. [Online]. Available: https://www.cadence.com/content/cadence-www/global/en_US/home/tools/digital-design-and-signoff/silicon-signoff/voltus-ic-power-integrity-solution.html
[21] "PULPino Processor Platform," December 2017. [Online]. Available: http://www.pulp-platform.org/
[22] "The RISC-V Foundation's Web Site," December 2017. [Online]. Available: https://riscv.org/
[23] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin *et al.*, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance – Part II: Model validation," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986–4992, Dec. 2016.

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