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A master clock for the Speed School impulse clock system using WWV time information

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A MASTER CLOCK FOR THE SPEED SCHOOL IMPULSE CLOCK SYSTEM USING WWV TIME INFORMATION

By

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ABSTRACT

Since approximately February of 1979, the Speed School impulse clock system has not functioned due to a worn-out master clock that was never replaced because of a lack of funds. For this thesis project, a solid-state master clock that performs the same functions as the old mechanical master clock was built for less than $200. The new clock features accuracy traceable to the National Bureau of Standards, automatic reset after a power-down and subsequent power-up, and a daylight savings time provision. A decoder that recovers time information broadcast by radio station WWV from Fort Collins, Colorado was built and interfaced to the master clock to provide the accuracy traceable to the National Bureau of Standards.

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I. INTRODUCTION

The Speed School impulse clock system has not been working since approximately February of 1979, when an old mechanical master clock that controlled the school clocks wore out. Shortly after the clocks stopped working, a bid of $900 was submitted to make the clocks operational again. No funds were available at the time and the clocks were never repaired. The goal of this thesis project was to build another more advanced master clock that could be hooked up to the existing clock system, yet be all solid-state.

The new master clock was designed to have automatic reset capability after a power-down, a daylight-savings-time provision, and more accuracy than the old master clock. A microprocessor-based system was chosen for implementing the desired functions, since the cost of such systems has become very low, considering the flexibility that such a system provides. An MC6802 microprocessor was chosen since it has an internal clock-generating circuit and on-chip RAM that can be maintained during a power-down. Additional support devices included a microprocessor-compatible real-time clock, Erasable Programmable Read Only Memory (EPROM), and address decoding logic. Software for the master clock was developed with the Tektronix 8002A Development System.

In addition to this microcomputer unit, a separate WWV decoder was built to retrieve time information broadcast by radio station WWV. This decoder was then interfaced to the microcomputer to provide periodic updating of the real-time clock. In the following chapters, specifics of school clock operation, new master clock design, and WWV decoder design are presented.

II. CLOCK SYSTEM DESCRIPTION

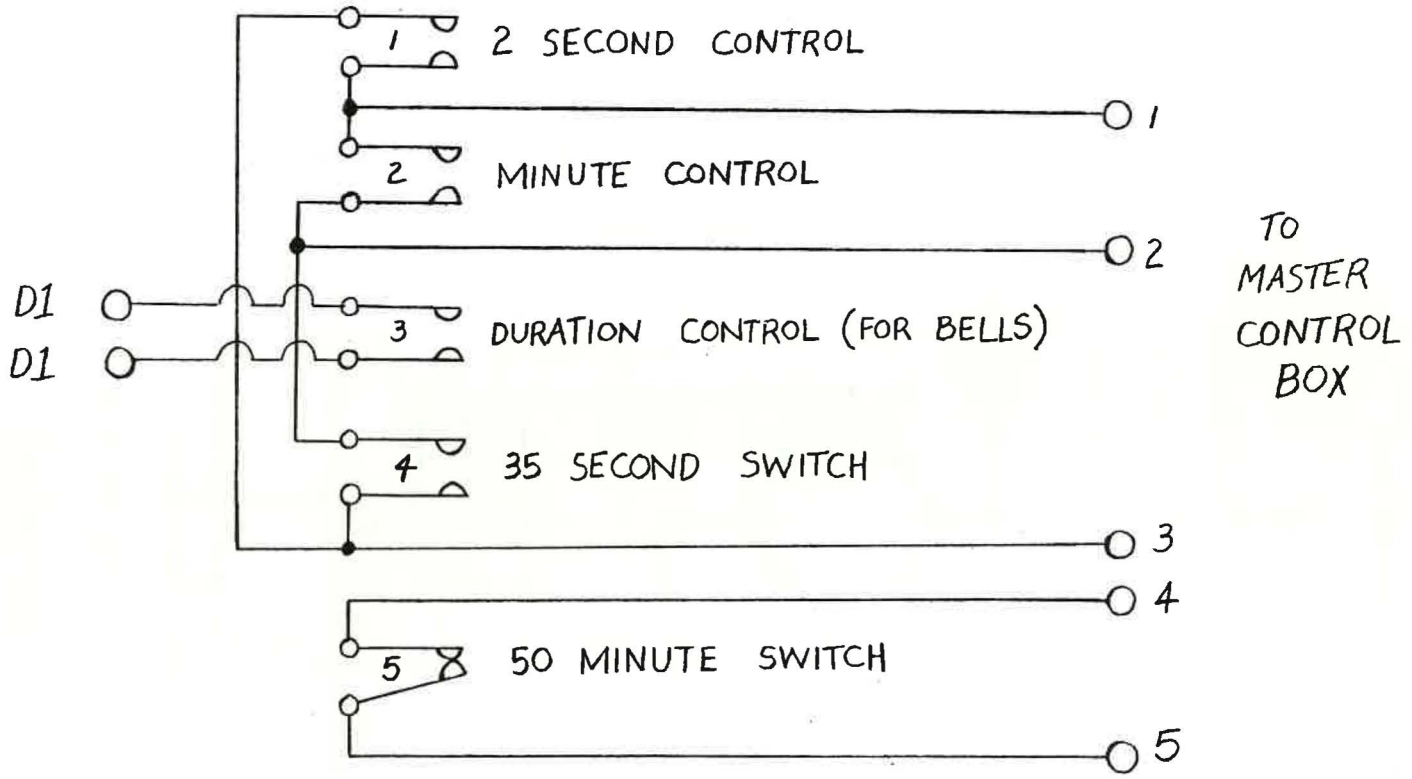
The Speed School impulse clock system consists of a master clock, a master control box, two relay boxes, and the individual wall clocks. A brief description of each subsystem follows.

A. Master Clock

The old master clock, shown in FIGURE 1, consisted of a series of cam-actuated mechanical switches that opened and closed at different intervals. Switches one through four controlled an AC voltage, while switch five controlled a DC voltage. The time base for the master clock was a large pendulum connected to a series of gears that turned the switch cams. Originally located in Room 102 of W. S. Speed Hall, the master clock was connected to a master control box in Room 3 of W. S. Speed by seven wires in a section of conduit. In 1979, this mechanical clock apparently wore out and has never been replaced. The new master clock built for this thesis project will replace the old master clock.

B. Master Control Box

The master control box, shown in FIGURE 2, contains an AC relay, a selenium rectifier, and an unconnected program unit that at one time controlled bells. The relay is energized when the proper switches in the master clock



CONTACT NO. 1 CLOSES EVERY TWO SECONDS
CONTACT NO. 2 CLOSES EVERY MINUTE (58" TO 60") - IMPULSE
CONTACT NO. 3 CLOSES EVERY MINUTE (01" TO MAX 16") - DURATION
CONTACT NO. 4 CLOSES 59'10" OPENS 59'45" - 35 SECONDS
CONTACT NO. 5 CLOSES 59'45" OPENS 49'45" - 50 MINUTES

FIGURE 1 - Old Master Clock

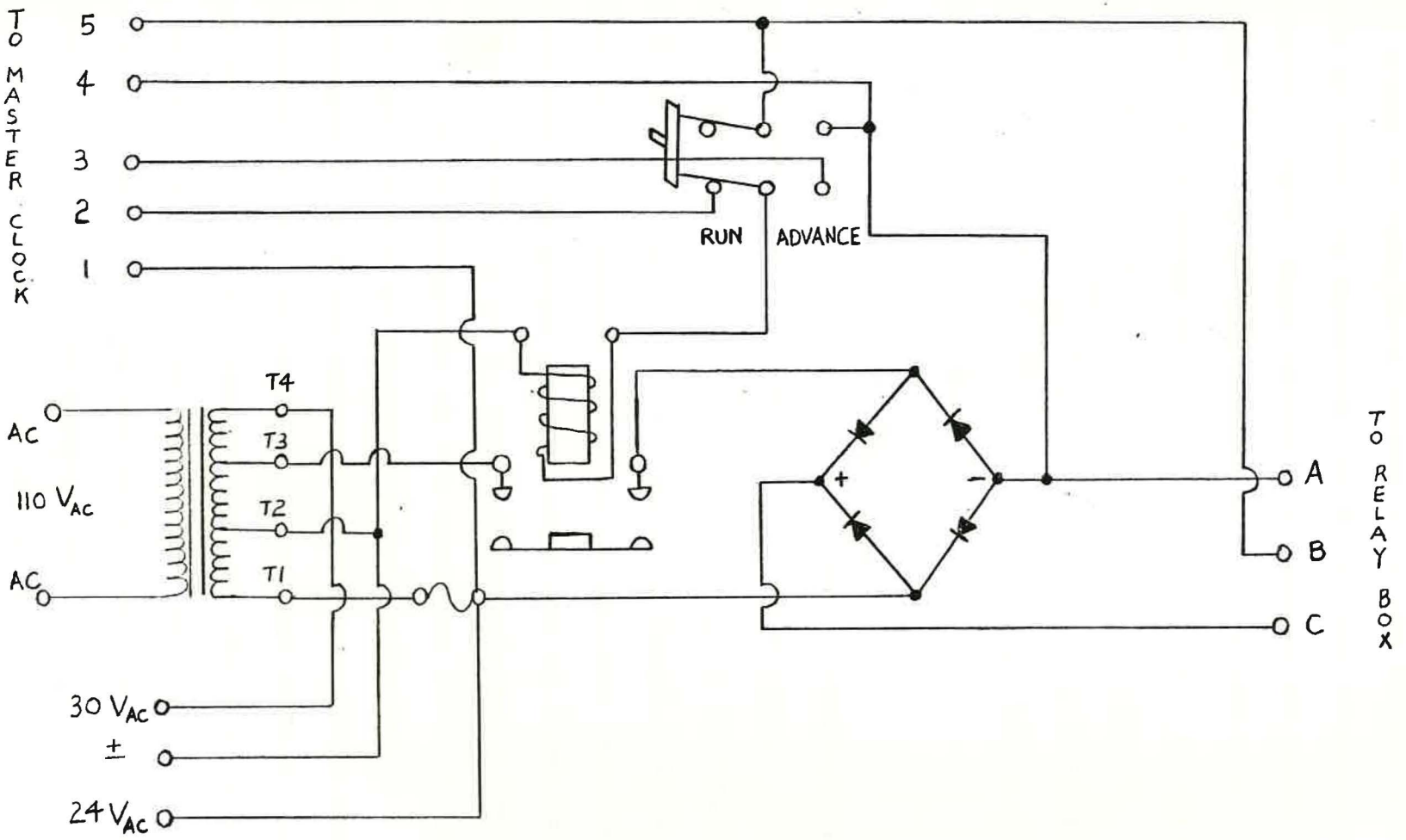


FIGURE 2 - Master Control Box

are closed (either #2 is closed or #1 and #4 are closed). When the relay is energized, an AC voltage is applied to the rectifier input, which causes a DC voltage to appear across terminals A and C. The potential of terminal B is determined by switch #5 in the master clock. If the switch is closed, $V_{CB} = V_{CA}$, but if the switch is open, $V_{CB} = 0$. These three output terminals are used as inputs to a relay box located immediately to the right of the master control box in Room 3 of W. S. Speed Hall.

C. Relay Box

The relay box, shown in FIGURE 3, receives inputs from the master control box. These three inputs control two relays that determine the status of outputs 1A, 1B, and 1C, which go to the school clocks in W. S. Speed Hall, J. B. Speed Hall, and Sackett Hall, and to another relay box in Ernst Hall. By having another relay box in Ernst Hall, the load on the unit in W. S. Speed is significantly reduced.

The program unit in the relay box in W. S. Speed Hall controls all of the Speed School bells and is programmed by breaking off tabs from metal strips and then inserting the strips into a cylinder that rotates each time the school clocks are incremented. At the programmed times, a switch closes and rings the bells. If the toggle switches at the bottom of the box are in the "off" position, the bells are disabled. The program unit should still work with the new master clock, but no attempt has been made to make

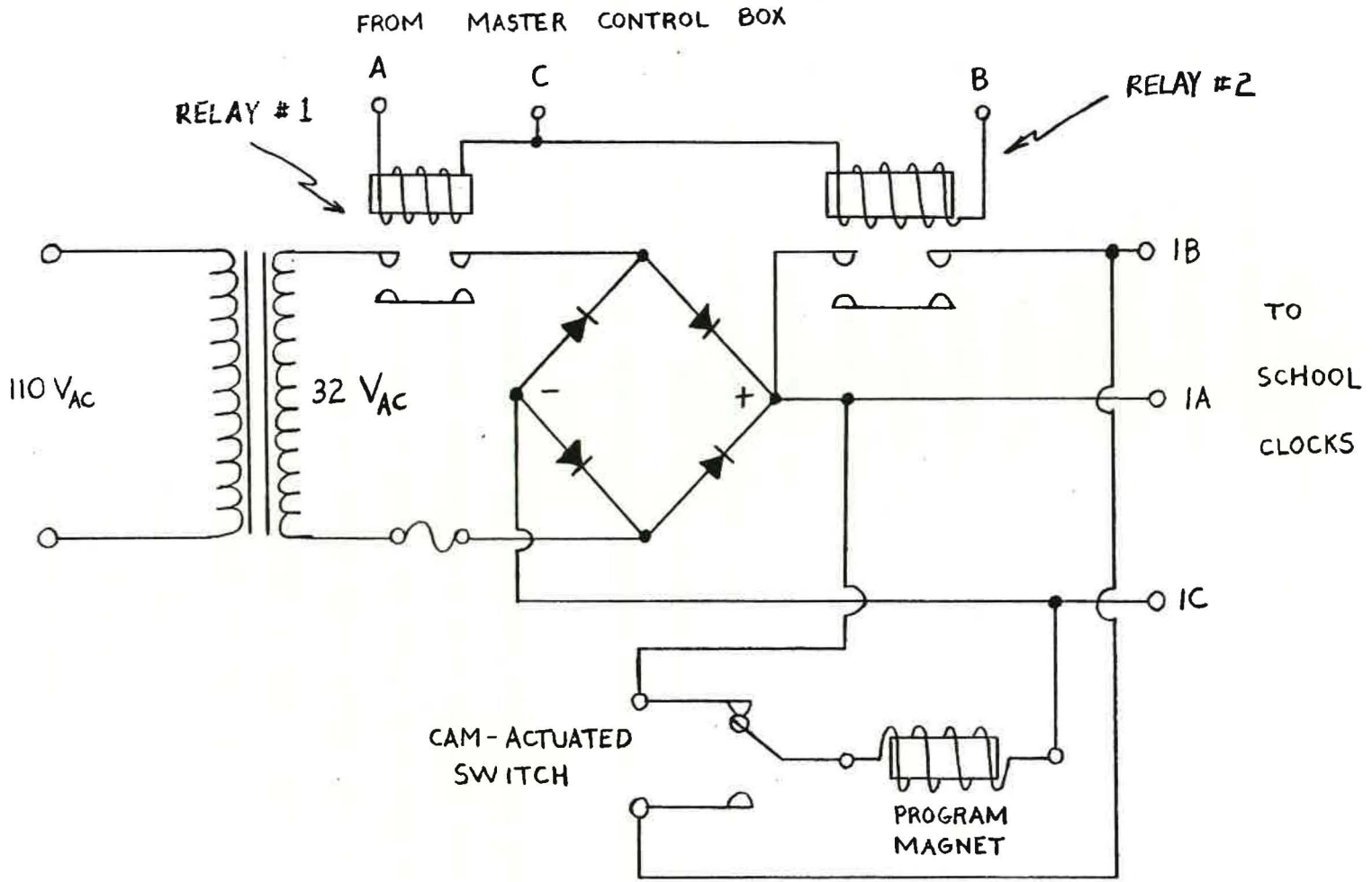


FIGURE 3 - Relay Box

the bells work again, since the desirability of bell-ringing is controversial.

D. School Wall Clocks

All Speed School clocks contain a 24-volt DC coil that when energized and subsequently de-energized, allows a ratchet mechanism to advance the clocks by one minute. Each clock has three wires (A, B, and C), one of which (wire C) is always connected to one terminal of the coil. The other coil terminal is switched between wires A and B by a cam-actuated switch inside the clock (see FIGURE 4). From four minutes after the hour until 58 minutes after the hour, the coil is connected from A to C. From one minute before the hour until three minutes after the hour, the coil is connected from B to C. With this arrangement, all clocks can be synchronized at one minute before the hour using the following procedure:

1. From 00 minutes to 49 minutes after the hour, 24-volt pulses (duration = 0.5 second) are applied between C and A as well as C and B.
2. From 50 minutes to 59 minutes after the hour, pulses are applied between C and A only. If any school clock is ahead of the master clock by ten minutes or less, then the school clock will stop advancing at 59 minutes after the hour and "wait" for the master clock to catch up.

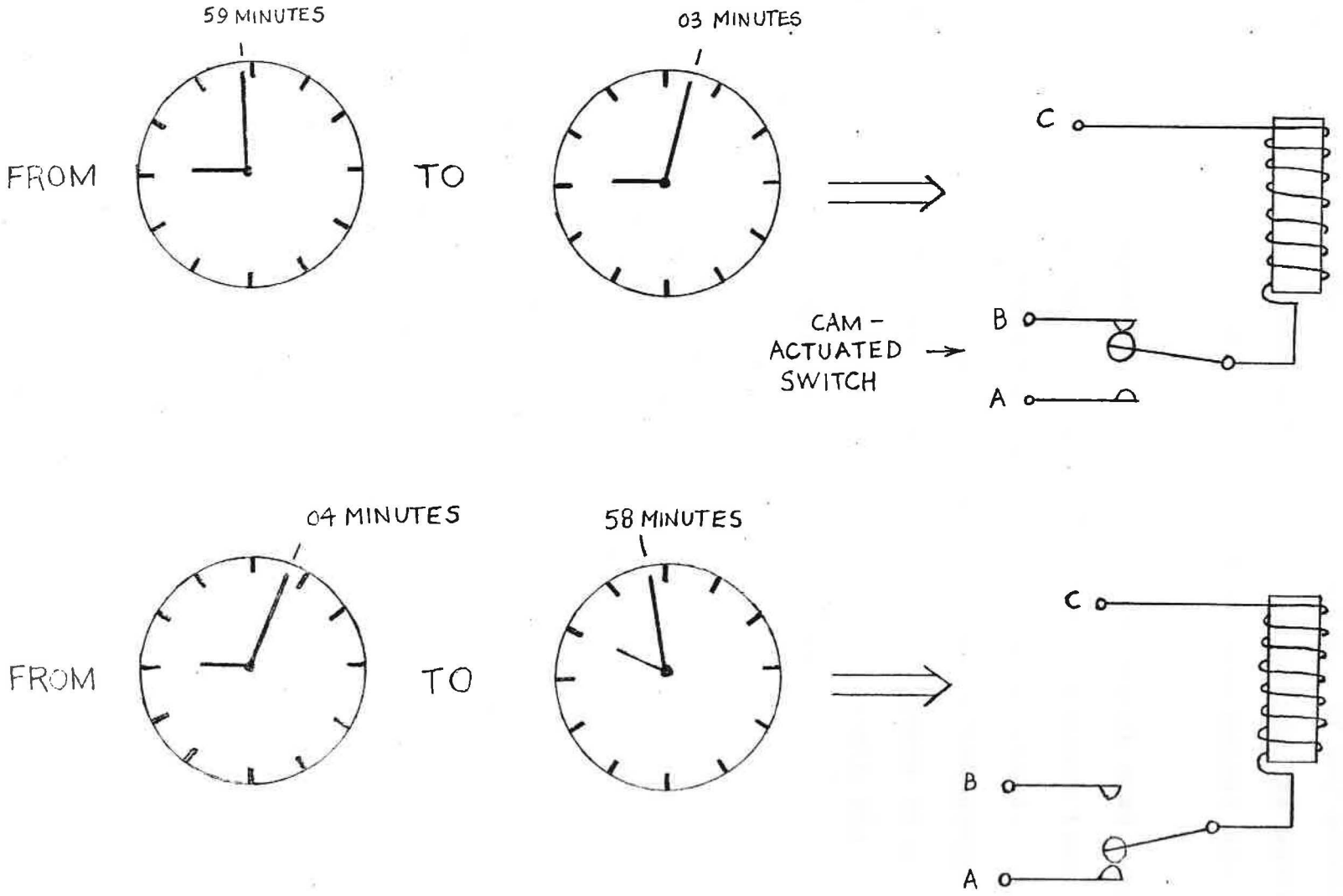


FIGURE 4 - Wall Clock Coil Connections

3. At 59 minutes after the hour, ten consecutive pulses are sent between C and A. If any school clock is less than ten minutes behind the master clock, it will catch up when these pulses are sent.

Using the above procedure, any clocks that are at most ten minutes ahead of or one hour behind the master clock time will eventually be resynchronized to the master clock.

The power consumed by each clock is approximately equal to three watts, which at 24-volts corresponds to a current requirement of about 125 ma. TABLE I lists the locations of all Speed School impulse clocks.

TABLE I

SPEED SCHOOL IMPULSE CLOCK SYSTEM

Master Clock, Room 102, W. S. Speed Hall
Program Machine Room 3, W. S. Speed Hall

Secondary Clocks:

Sackett Hall, 3 Secondary Clocks:
1st floor hall, 2nd floor front hall, 2nd floor rear hall

Main Speed Building, 3 Secondary Clocks:
Basement Center hall, Room 201, Library

W. S. Speed Hall, 9 Secondary Clocks:
Basement Laboratory, Basement Rear Hall, Basement Front Hall
1st floor Laboratory, 1st floor rear hall, 1st floor front hall
2nd floor Laboratory, 2nd floor rear hall, 2nd floor front hall

R. C. Ernst Hall, 9 Secondary Clocks:
1st floor west hall, 1st floor center hall, 1st floor east hall
1st floor Departmental Office, 1st floor Auditorium
2nd floor Central Hall (2 clocks), 3rd floor Central Hall (2 clocks)

Totals: 24 Secondary Clocks not including several that have been removed from both Sackett Hall and Main Speed Buildings when these buildings were remodeled from time to time.

III. NEW MASTER CLOCK

A. General Function

The hardware and software for the new master clock simply control two switches, and thus simulate the old master clock. A triac is used in place of switch #2 in the old master clock and an SCR is used in place of switch #5 (see FIGURE 5). Switches #1, #3, and #4 in the old master clock are not needed.

Whenever the school clocks are to be advanced or synchronized, the triac switch is closed. This energizes the relay in the master control box, which causes relay #1 in the relay box to close. A DC voltage now appears across output terminals A1 and C1, which go to the school clocks. If the SCR switch is not closed, terminal B1 of the relay box is floating and there is no current path between B1 and C1. If the SCR switch is closed, a voltage appears across terminals B and C of the master control box. This energizes relay #2 in the relay box and now $V_{A1C1} = V_{B1C1}$ since $V_{A1B1} = 0$.

B. Master Clock Hardware

A block diagram of the system hardware is shown in FIGURE 6. A functional description of each block follows.

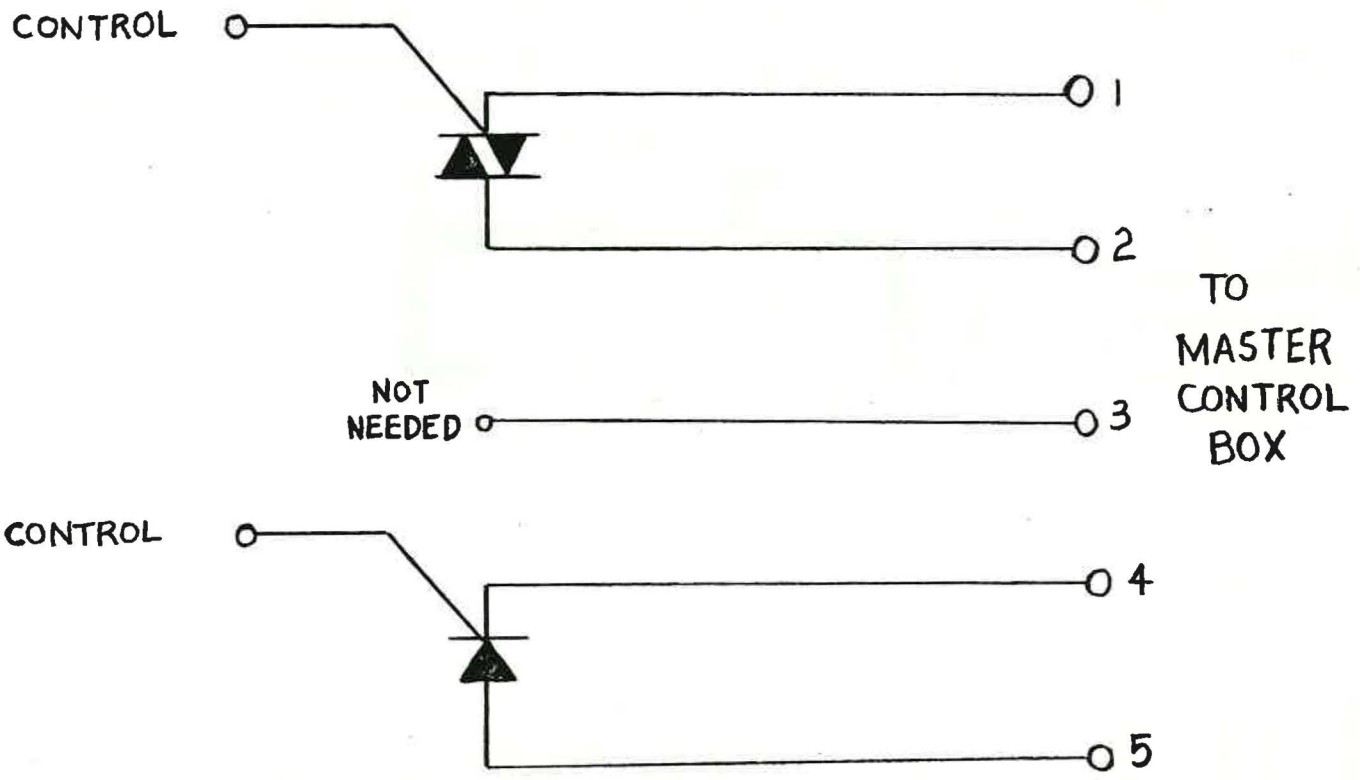


FIGURE 5 - New Master Clock

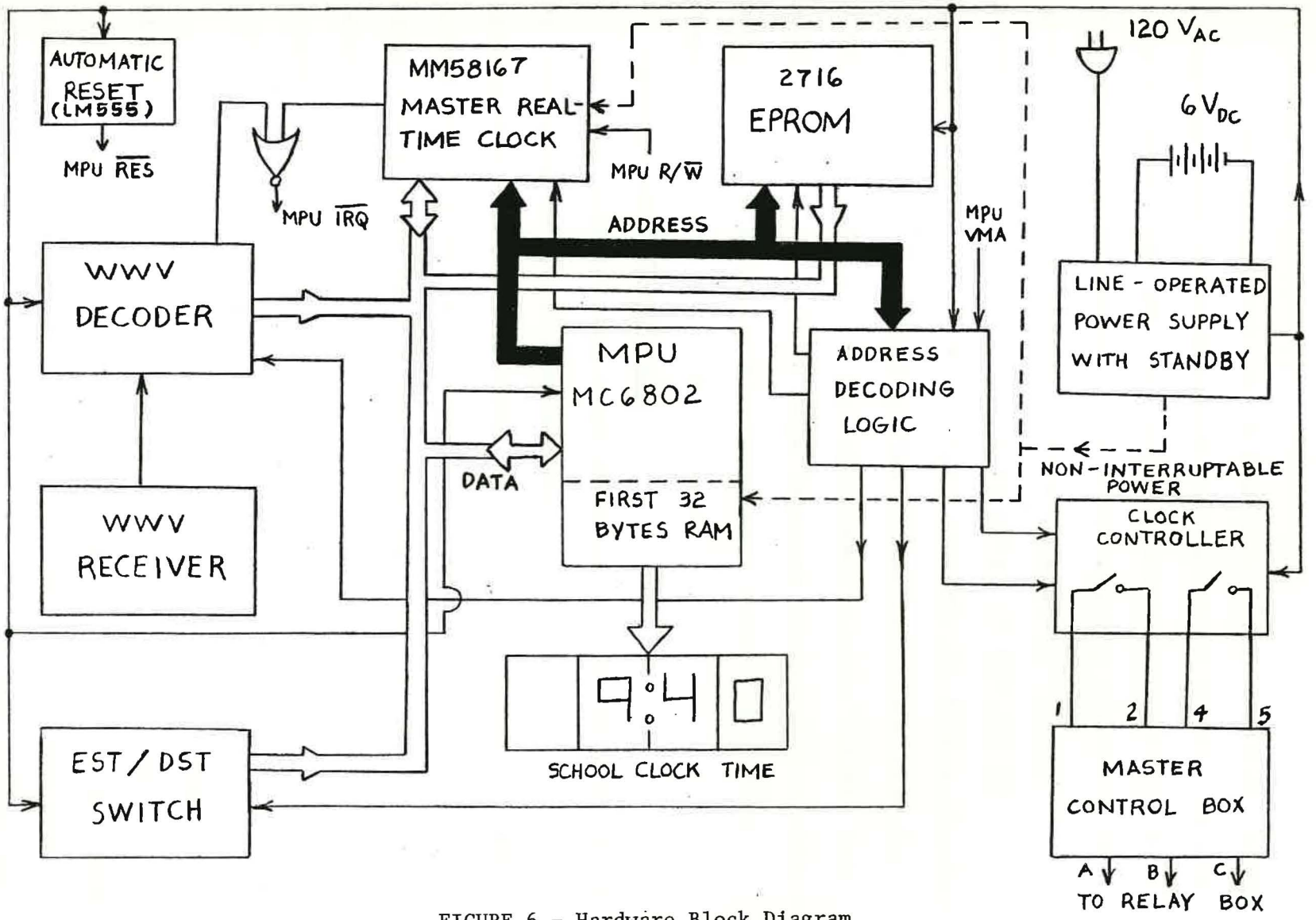


FIGURE 6 - Hardware Block Diagram

1. MC6802 Microprocessor

The microprocessor is the heart of the system, since it decides when to send pulses to the school clocks and how many to send. The 6802 is totally software compatible with the MC6800 microprocessor, but also features 128 bytes of on-chip RAM and an internal clock generating circuit. During a power-down, the first 32 bytes of RAM can be maintained with very little power consumption from a standby source (batteries). This allows the school clock time to always be in RAM, so the microprocessor always "knows" the school clock time. For a more detailed description of the processor, the Motorola Microprocessor Manual should be consulted.

2. MM58167 Real-Time Clock

The MM58167 real-time clock can either be written to or read from by the microprocessor. A 32.768 KHz crystal is used as the clock's time base. The clock is microprocessor compatible and has eight data lines (the 6802 is an eight-bit processor) and five address lines to select among 24 internal registers. Time is kept in a BCD format, which is advantageous since WWV time frames are also given in a BCD format.

The 58167 also features a power-down mode that allows the chip to keep time even during a line-power failure, provided a standby power source is available. With the real time always available, and the school clock time always in RAM, the difference between the school clocks and

real-time clock can be computed when a power-down and subsequent power-up have occurred, and the school clocks can be updated. A full description of the MM58167 can be found in the data sheets in APPENDIX II.

3. WWV Decoder

Operation of the WWV decoder is explained in Chapter IV of this thesis. The decoder is interfaced to the processor by four 74LS125 three-state buffers. The buffers are enabled by decoding logic when 3000H or 3001H is placed on the address bus. WWV time data can only be read by the microprocessor, whereas the real-time clock can be read from or written into. The end-of-frame 0.1 second pulse generated by the decoder is used as a hardware interrupt to the processor.

4. EST, EDT Switch

This feature allows the school clocks to adjust automatically to what amounts to a change in time zones every six months. This switch must be thrown manually once every six months to allow for the time change. WWV transmits UTC (Coordinated Universal Time), which is referenced to Greenwich, England. Data at the switch location (either four or five hours) is subtracted from the decoded time to obtain Eastern Daylight or Eastern Standard Time. In order for the clocks to adjust themselves, a valid WWV decode (see WWV routine in software section) must be received after the switch is thrown.

5. MC6821 PIA (Peripheral Interface Adapter)

The MC6821 PIA is used to latch and display the school clock time that is stored in RAM via four seven-segment displays. Since a BCD format requires 16 bits to represent a time and the PIA has 16 lines that can be configured as outputs, the 6821 is ideal for this application. The PIA output lines are used to drive four BCD to seven-segment decoders which, in turn, drive the four seven-segment displays.

6. 2716 EPROM (Erasable Programmable Read Only Memory)

The 2716 contains 2048 eight-bit-wide memory locations for storing the system software. A PROLOG programmer was used to program the EPROM. A single +5 volt power supply is required for operation of the EPROM.

7. Address Decoding

Since the microprocessor can only "communicate" with one external device at a time, address decoding is needed to assign each device a unique address. A 74LS154 four-to-sixteen-line decoder is used for this purpose. The four inputs to the chip are tied to the four most significant bits of the address bus (A12 - A15), which means that these four bits are completely decoded. If, for example, an address of 2000H is placed on the address bus, then output number two of the 74LS154 goes low (all outputs are active low), while all other outputs remain high and the real-time clock is addressed. A diagram of the address decoding scheme is shown in FIGURE 7.

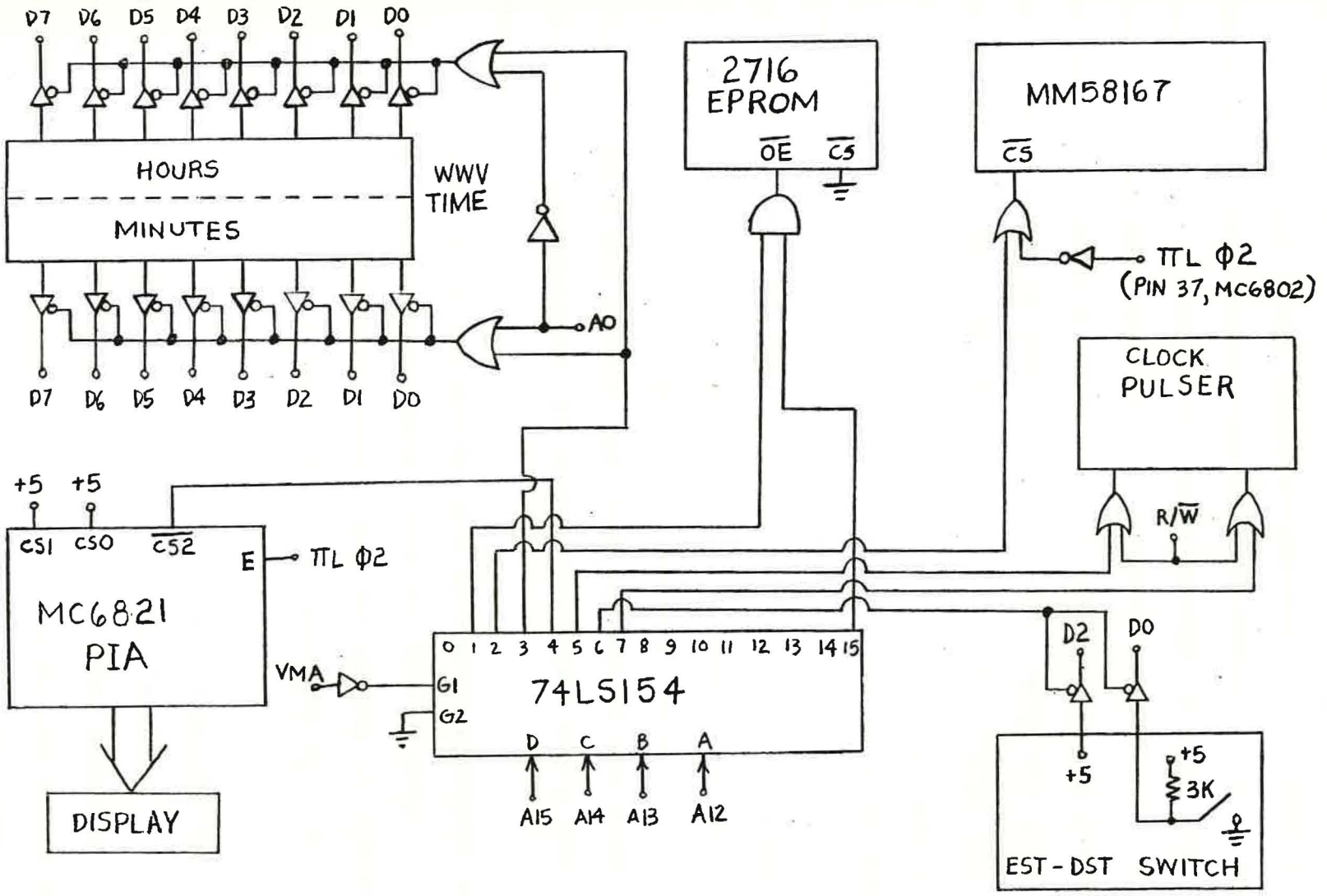


FIGURE 7 - Address Decoding

8. Clock Pulser

The clock pulser hardware consists of two LM555's operating in the one-shot mode, an opto-isolator with an SCR output, an opto-isolator with a triac output, an SCR, and a triac. A diagram of the circuit is shown in FIGURE 8. When an address of 5000H is placed on the address bus, output #5 of a 74LS154 goes low and triggers 555 #1. When the output of the 555 is high, the LED in the opto-isolator turns the triac output on, which provides a path for gate current in triac #1. Triac #1 now allows current to flow through the inductive load, which is the relay coil in the master control box, thus closing the relay. The relay will remain closed for the time out period of the 555 (approximately 0.5 seconds). Under normal operation, location 5000H is addressed once each minute, but when the clocks are being advanced or synchronized, it is addressed once every two seconds.

Operation of the SCR circuit is almost identical to that of the triac circuit except that the SCR is only required to switch a DC voltage. The SCR switch is closed by addressing location 7000H and is closed from 00 - 49 minutes after the hour.

To protect the devices from false triggering due to line transients and inductive kickback, RC "snubber" networks are placed across the devices. These networks limit the rate of voltage rise (dV/dt) across the device and thus greatly reduce any C (dV/dt) charging current that

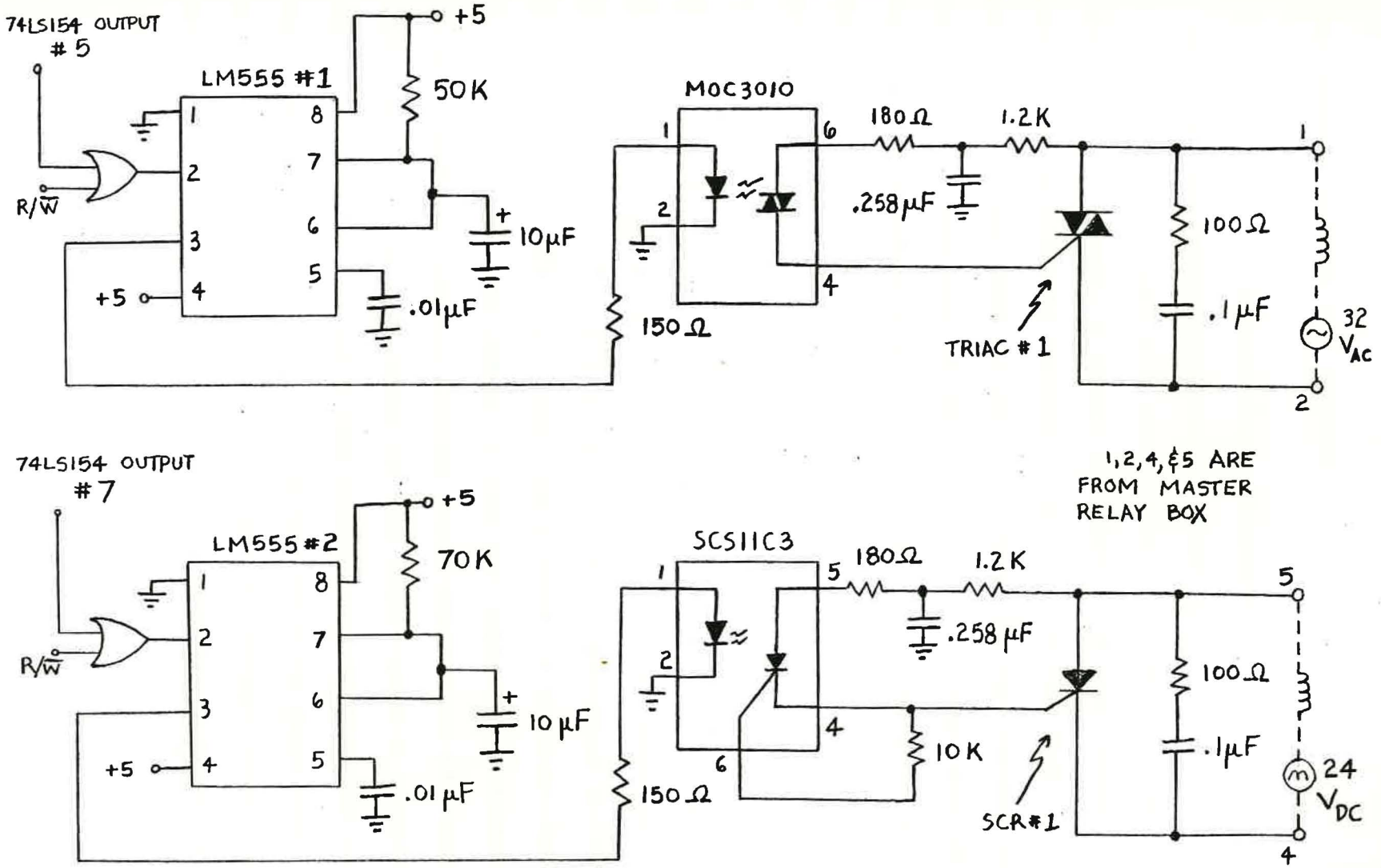


FIGURE 8 - Clock Pulser

might falsely trigger the device.[1]

C. Master Clock Software

1. Addition and Subtraction of BCD Numbers

Since all times are represented in a BCD (binary coded decimal) format, a brief explanation of how these numbers are manipulated follows. Addition of two BCD numbers is accomplished by using the DAA (decimal adjust the A accumulator) instruction immediately after either the ABA (add A and B accumulators) or ADD A (add A accumulator to a memory location) instructions. BCD subtraction is performed using ten's complement addition. The ten's complement of the subtrahend is obtained by adding 66H (hexadecimal) to the subtrahend, complementing the result, and adding one. This result is added to the minuend to give the result of the subtraction. If there is an end carry generated by the ten's complement addition, then the minuend is greater than the subtrahend and the answer is the BCD difference between the two numbers. However, no end carry means that the true answer is the ten's complement of the result with a negative sign attached. If two equal BCD numbers are subtracted, the result is "positive zero" since an end carry is generated. The status of the carry bit in the microprocessor condition code register can therefore be used to test for a positive or negative result after a BCD subtraction.

2. Description of Software

The software for controlling the Speed School clocks is divided into 14 subprograms. A description of each subprogram follows.

a. Initialization. The initialization program is executed every time a power-down and subsequent power-up occur. The first section of the program configures all 16 PIA lines as outputs and allows access to peripheral data registers A and B. The stack pointer is then initialized so that the processor will not get "lost" when jumping to and from the various subroutines. After initialization is completed, the processor determines if the power-up is the first by reading the first location in RAM. If the number in this location is 52H, then it is not the first power-up. If it is the first power-up, the MM58167 real-time clock and school clock RAM locations are set to 15:00, since this is the time that the school clocks are manually set to before the master clock is ever turned on. If the system has been working previously, then the "first power-up" sequence is skipped and, instead, the processor executes the reset subroutine.

b. Reset Subroutine. During a power-down condition, standby power from batteries allows retention of the first 32 bytes of internal RAM in the 6802, where the school clock time is stored. The backup power also allows the MM58167 real-time clock to keep time during a line power failure. When power is restored, the reset routine will

calculate the difference between the school clocks and real-time clock, and send out the appropriate number of pulses to the school clocks to synchronize them with the real-time clock. Once the clocks are synchronized, the monitor routine is executed.

c. Monitor Subroutine. The monitor subroutine waits for a change in the real-time clock minutes counter or a WWV decode. Both of these events will generate an interrupt to the processor. When the interrupt is generated, the processor will start executing an interrupt program at the address specified by the contents of memory locations FFF8H and FFF9H. When this program has been executed, the monitor routine will be returned to until another interrupt occurs.

d. Interrupt Program. At the end of each frame of WWV time code information, a 0.1 second pulse that is used as an interrupt pulse is generated by the decoding circuitry. Likewise, at the end of each minute, the real-time clock generates an interrupt signal. If a CLI (clear interrupt mask bit) instruction has been executed and an interrupt occurs, then the processor starts executing the interrupt program.

The interrupt program first determines if the real-time clock or the WWV decoder has generated the interrupt by reading the real-time clock interrupt status register. If bit three of the register is a "1", then the real-time clock has generated the interrupt. An interrupt

from the real-time clock instructs the processor to send out a pulse to the school clocks to advance them by one minute. Program control is then returned to the monitor routine. If, on the other hand, the WWV decoder generated the interrupt, then the WWV interrupt routine is serviced.

The WWV interrupt routine determines if the most recent decode is valid by comparing the time to the previous decode time plus one minute and then to the second previous decode time plus two minutes. If all three times are equal, then the most recent decoded time is assumed to be valid. If the three times are not equal, the frame is assumed to be invalid and one minute is added to the previous decode-time-plus-one-minute value, which is then stored in the second-previous-decode-plus-two location. Likewise, one minute is added to the most recent decode time and the result is stored in the previous decode-plus-one-minute location. The program is now set up for the next WWV interrupt.

Due to the nature of the decoding circuitry and the WWV broadcast format, the actual local time when an interrupt occurs (assuming a valid decode) is the decoded time plus one minute, plus 1.15 seconds and minus four or five hours. These differences are accounted for by adding two minutes to a valid decode time and then subtracting four or five hours (depending on the position of the EST, EDT switch). This adjusted time is then used to determine the difference between the school clocks and the actual time. After this difference is determined, the program waits 58

seconds to send out the calculated number of pulses. When all pulses are sent, the school clock time is placed in the appropriate real-time clock locations and program control is returned to the monitor routine. This correction procedure assures that every time a valid WWV time is received, the real-time clock is reset accordingly.

e. Pulser Routine. The pulser routine sends out the number of pulses necessary to synchronize the school clocks with either WWV or the real-time clock at the rate of one pulse every two seconds. If the school clocks need to be advanced by more than eleven hours, the pulser routine will wait for the real-time clock or WWV to catch up. If the hours difference is less than eleven, 62 pulses are sent for each hour of difference. The extra pulses account for the two minute delay inherent in sending 60 pulses. The pulser routine also controls the self-correcting feature of the school clocks by executing the FIFMIN (fifty minute switch) and CATUP (catch-up) subroutines.

f. Second Delay Routine. The second delay routine generates a time delay of approximately one second, since delays of integer multiples of one second are needed for various other subroutines.

g. Twelve-Hour Format Routine. The 12-hour format routine converts a 24-hour format time to a 12-hour format time by subtracting 12 hours from the 24-hour format time. If the result is positive, then the computed time is the correct 12-hour format time. If the result is negative,

then the original time was already in a 12-hour format.

h. Minutes Difference Routine. The minutes difference routine determines the number of minutes pulses that must be sent to the school clocks so that the school clock minutes and WWV or real-time clock minutes are the same. This is accomplished by counting the number of times the school clock minutes must be incremented to equal the WWV or real-time clock minutes. If the school clock minutes reach 60, then the school clock hours are incremented to prepare for the hours difference calculation, the minutes are set equal to zero, and the process continues. The result is a true binary number, not a BCD number.

i. Hours Difference Routine. This subroutine calculates the number of hours that the school clocks must be advanced to equal the WWV or real-time-clock time. This is done by subtracting the 12-hour format adjusted (refer to minutes difference routine) school-clock time from the 12-hour WWV or real-time clock time. If the result is positive, then the result is the hours difference, but if the result is negative, then the hours difference is the result plus 12.

j. Update Routine. The update routine adds one minute to the school-clock 24-hour format time and displays this time on the seven-segment displays by writing the time to the PIA. This routine is executed immediately after a pulse is sent to the school clocks.

k. Add One Minute to a Time Routine. This routine

adds one minute to a 24-hour format time. If the minutes are equal to 60 after addition of one minute, then the hours are incremented and the minutes are reset to zero. If the hours are equal to 24 after being incremented, they are reset to zero.

l. Fifty-Minute Switch Routine. This routine determines if the school-clock minutes are equal to 00 to 49 minutes. If they are, a switch is closed by writing to location 7000H.

m. Catch-up Routine. The catch-up routine determines if the school-clock minutes are equal to 59. If they are, a switch at location 5000H is opened and closed ten times by writing to this location ten times at two second intervals.

n. Short Delay Routine. This routine is used to provide a short delay between the time a switch at 5000H closes and the time a switch at 7000H closes.

IV. WWV DECODER

A. Background On Time Services

Radio station WWV is operated by the National Bureau of Standards and broadcasts from Fort Collins, Colorado on carrier frequencies of 2.5, 5, 10, 15, and 20 MHz. Among the services offered by WWV are weather announcements, voice time announcements, standard time intervals, standard audio frequencies, and a BCD (binary coded decimal) time code. The entire WWV broadcast format is shown in FIGURE 9.

Of particular interest in this thesis is the BCD time code, which is continuously broadcast on a 100 Hz subcarrier with a modified version of the IRIG-H time code format. With the IRIG-H, a binary zero is represented as 20 cycles of 100 Hz amplitude modulation (0.2 seconds), a binary one is 50 cycles of 100 Hz amplitude modulation (0.5 seconds), and a position marker (used for synchronization purposes) is 80 cycles of 100 Hz amplitude modulation (0.8 seconds). However, WWV also transmits a five millisecond burst of 1000 Hz (which sounds like the tick of a clock) to mark the beginning of each second. This burst has a guardband around it (see FIGURE 10) that deletes the first 30 milliseconds of the time code so, in this modified version, a binary zero is 17 cycles of 100 Hz AM, a binary one is 47 cycles of 100 Hz AM, and a position marker is 77 cycles of 100 Hz AM. If the 100 Hz subcarrier is

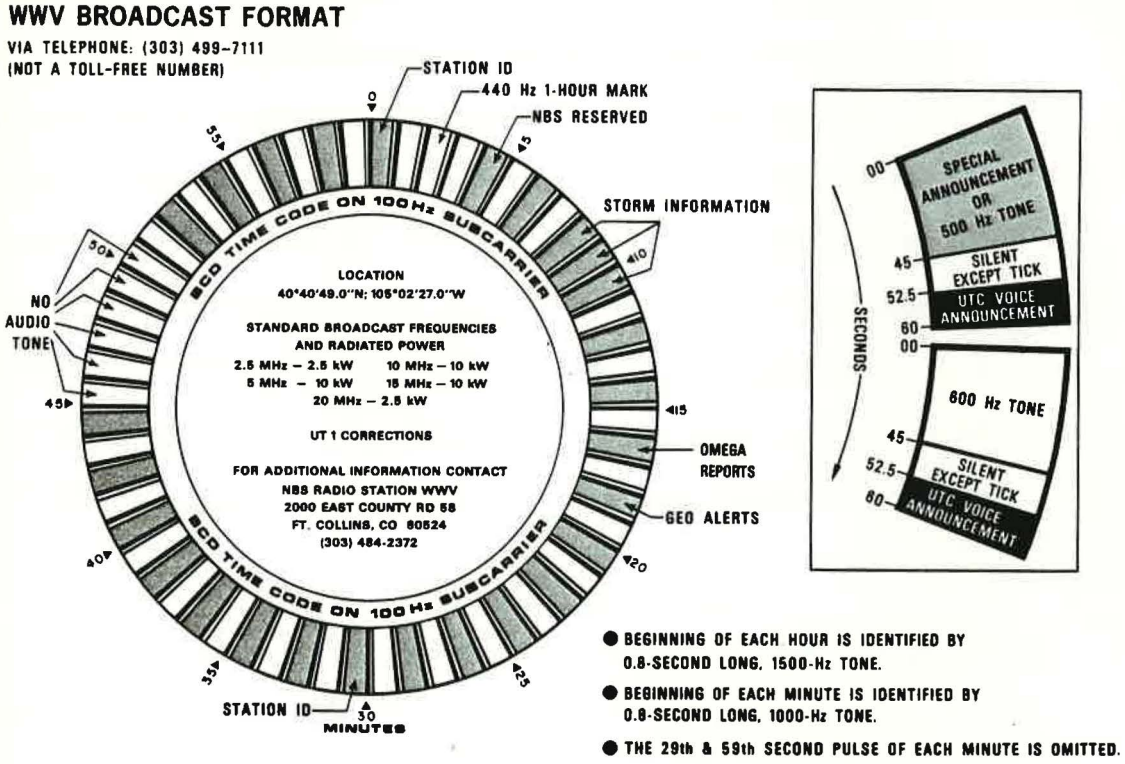


FIGURE 9 - WWV Broadcast Format (see Ref. 2)

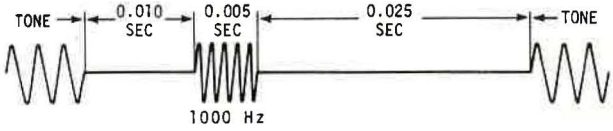


FIGURE 10 - WWV Guardband (see Ref. 3)

demodulated, the rectangular pulse train shown in FIGURE 11 is obtained. The beginning of each one minute frame is denoted by a 1.03 second hole in the code during which no pulse is transmitted. The positive-going edges of consecutive pulses are spaced exactly one second apart, but are 30 milliseconds late with respect to the actual time due to the guardband around the five millisecond 1000 Hz burst. By decoding the proper sequence of pulses, hours, minutes, and day of year information can be recovered.

B. Decoding Circuitry

The circuitry used to reconstruct the rectangular pulse train from the 100 Hz subcarrier is shown in FIGURE 12. Recovered audio (containing the 100 Hz code) at the output of the detector of the receiver being used is amplified and applied to the input of an active bandpass filter with a center frequency of 100 Hz and a Q of 10. This filter attenuates unwanted frequencies such as the 500 or 600 Hz audio tones and voice frequencies, but allows the 100 Hz subcarrier to be passed unattenuated. The center frequency (ω_o) of the filter is adjusted by varying potentiometer R5, while the Q is adjusted independently of ω_o by varying potentiometer R9.[4] The output of the bandpass filter is then applied to the input of an envelope detector that uses an operational amplifier to eliminate the forward voltage drop of the detector diode.[5] FIGURE 13 shows input and corresponding output waveforms for the envelope

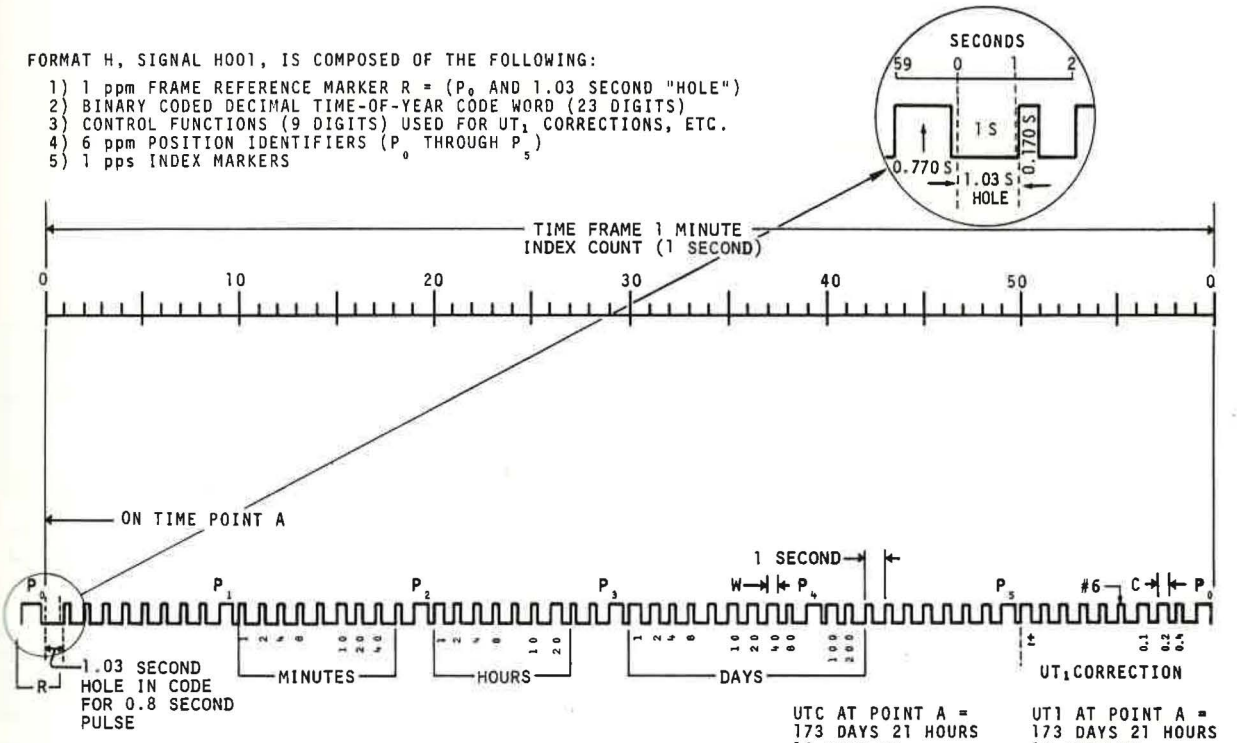
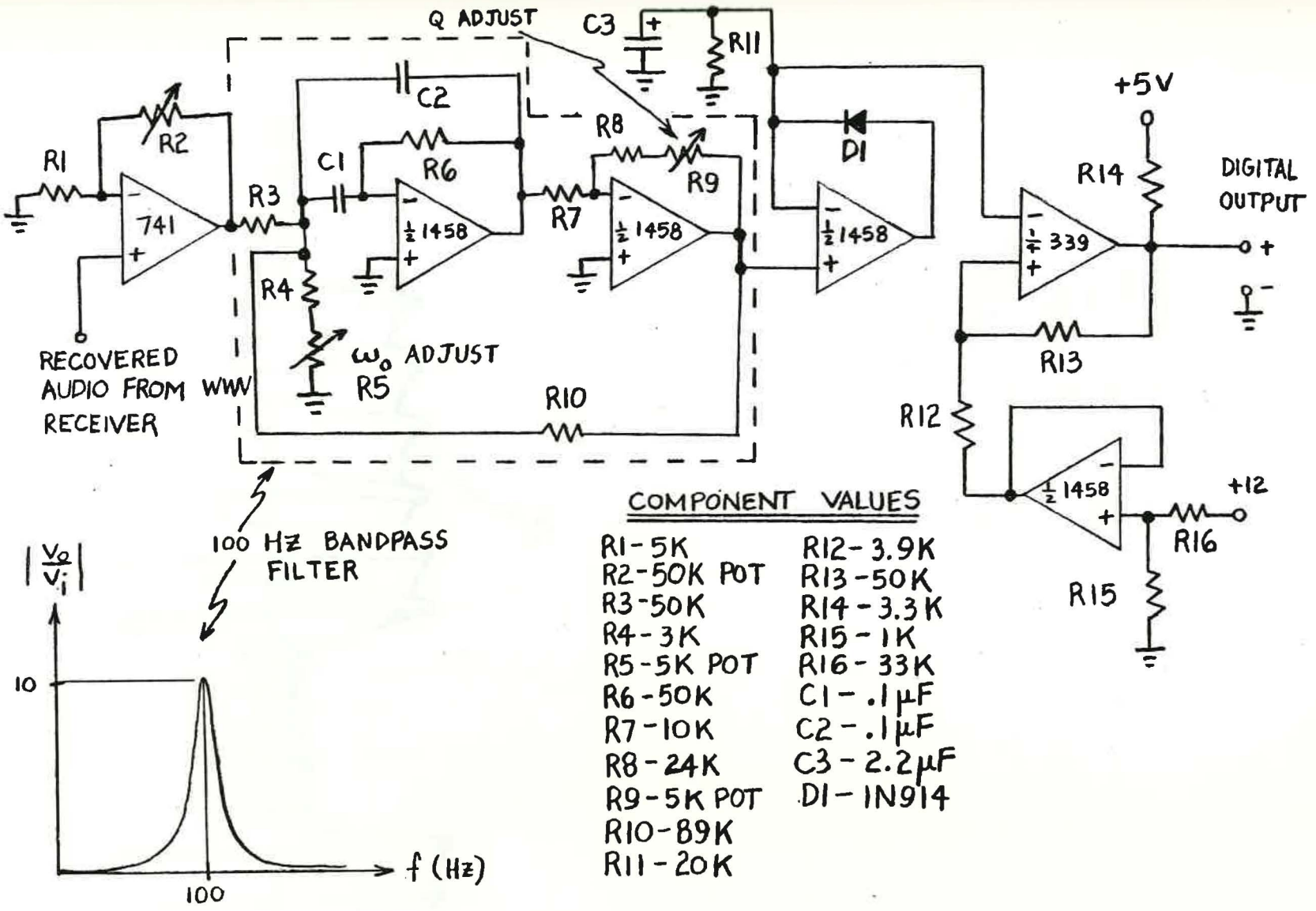


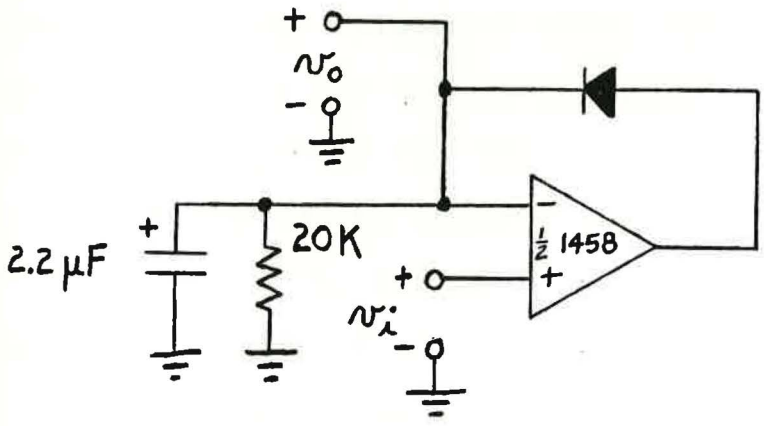
FIGURE 11 - WWV Time Code (see Ref. 6)



COMPONENT VALUES

R1 - 5K	R12 - 3.9K
R2 - 50K POT	R13 - 50K
R3 - 50K	R14 - 3.3K
R4 - 3K	R15 - 1K
R5 - 5K POT	R16 - 33K
R6 - 50K	C1 - .1μF
R7 - 10K	C2 - .1μF
R8 - 24K	C3 - 2.2μF
R9 - 5K POT	D1 - IN914
R10 - 89K	
R11 - 20K	

FIGURE 12 - Analog Decoding Circuitry



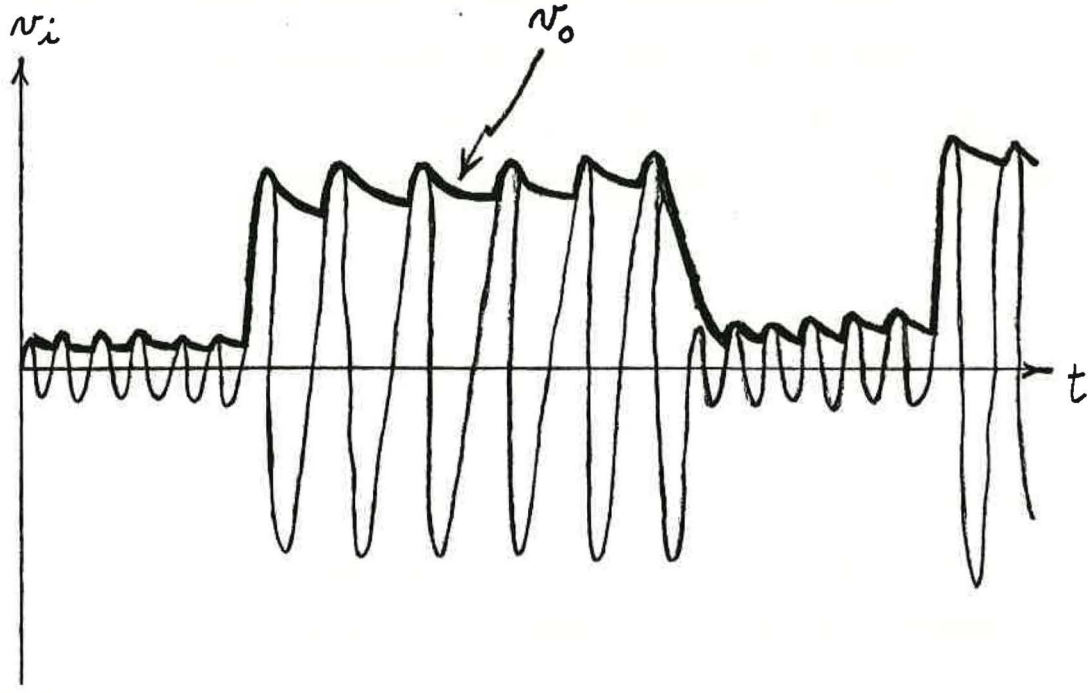


FIGURE 13 - Envelope Detector

detector. The low-level output (approximately one volt) of the detector is then converted to standard TTL levels using a Schmitt trigger. FIGURE 14 shows the transfer characteristic of the Schmitt trigger. In order to get the proper level input to the Schmitt trigger, potentiometer R2 (see FIGURE 12) can be adjusted without affecting the rest of the circuit. The output of the Schmitt trigger is the logical complement of the BCD time code.

Decoding of the BCD time code is accomplished with the circuit shown in FIGURE 15. The Schmitt trigger output is inverted (to give the time code in its uncomplemented state) and applied to the inputs of positive edge triggered monostables and flip-flops. MSMV (monostable multivibrator) #1 and FF (flip-flop) #1 form a "1-0" detector, while MSMV #2A and FF #2 form a position marker detector. Upon a positive edge (corresponding to the beginning of each second), both monostables are triggered and time out. At the end of each respective time out period (t = 0.35 sec. or 0.65 sec.), the $\overline{Q}$ outputs of the monostables supply a positive edge to the clock inputs of the D flip-flops, which latch whatever is at the input at that instant. MSMV #3 and 4 and FF #3 are needed to detect the beginning of each minute, which is signified by a position marker followed by a 1.03 second period during which no pulse is transmitted. When this occurs, a pulse that resets the counter (74LS90) is generated.

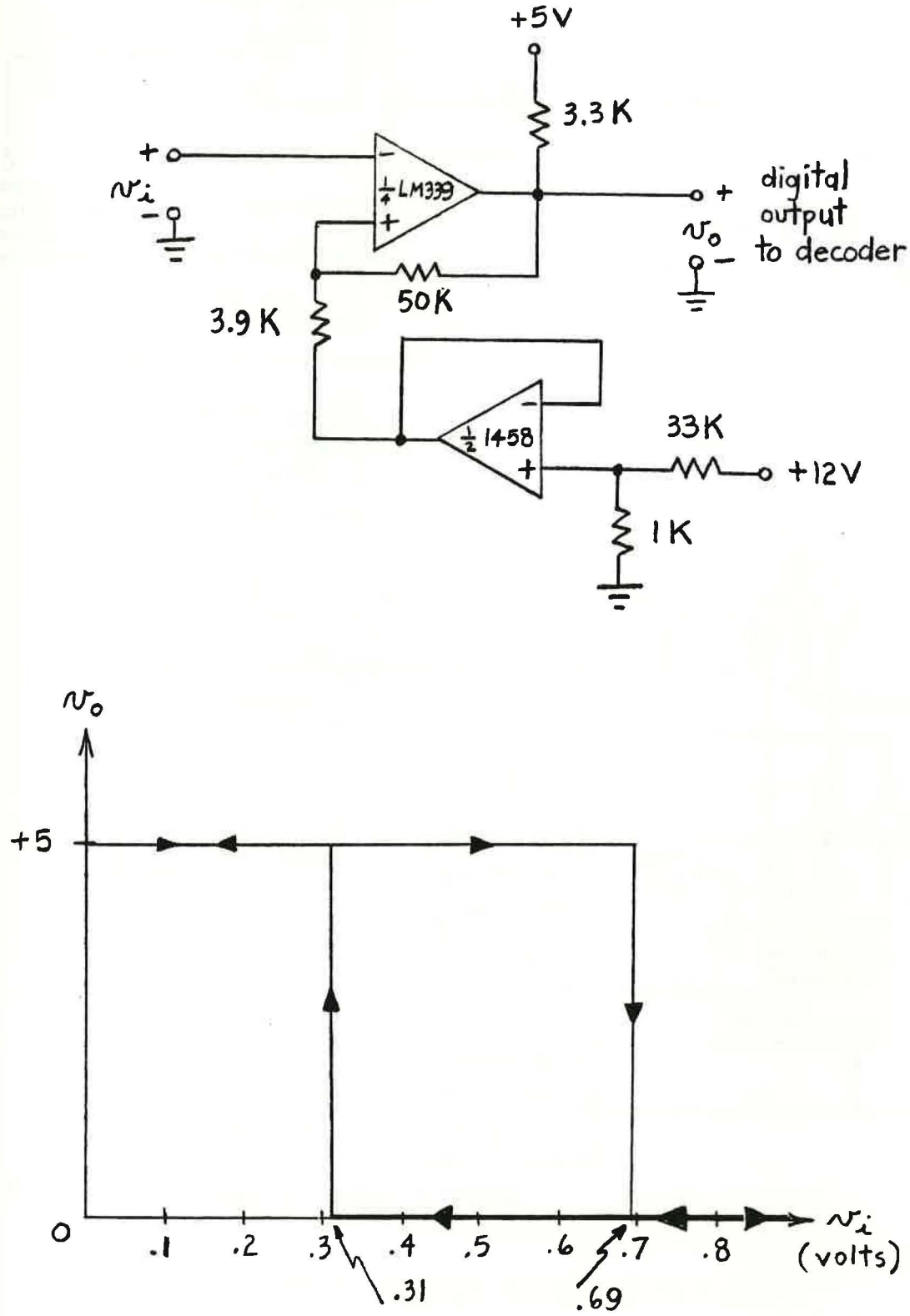


FIGURE 14 - Schmitt Trigger Characteristics

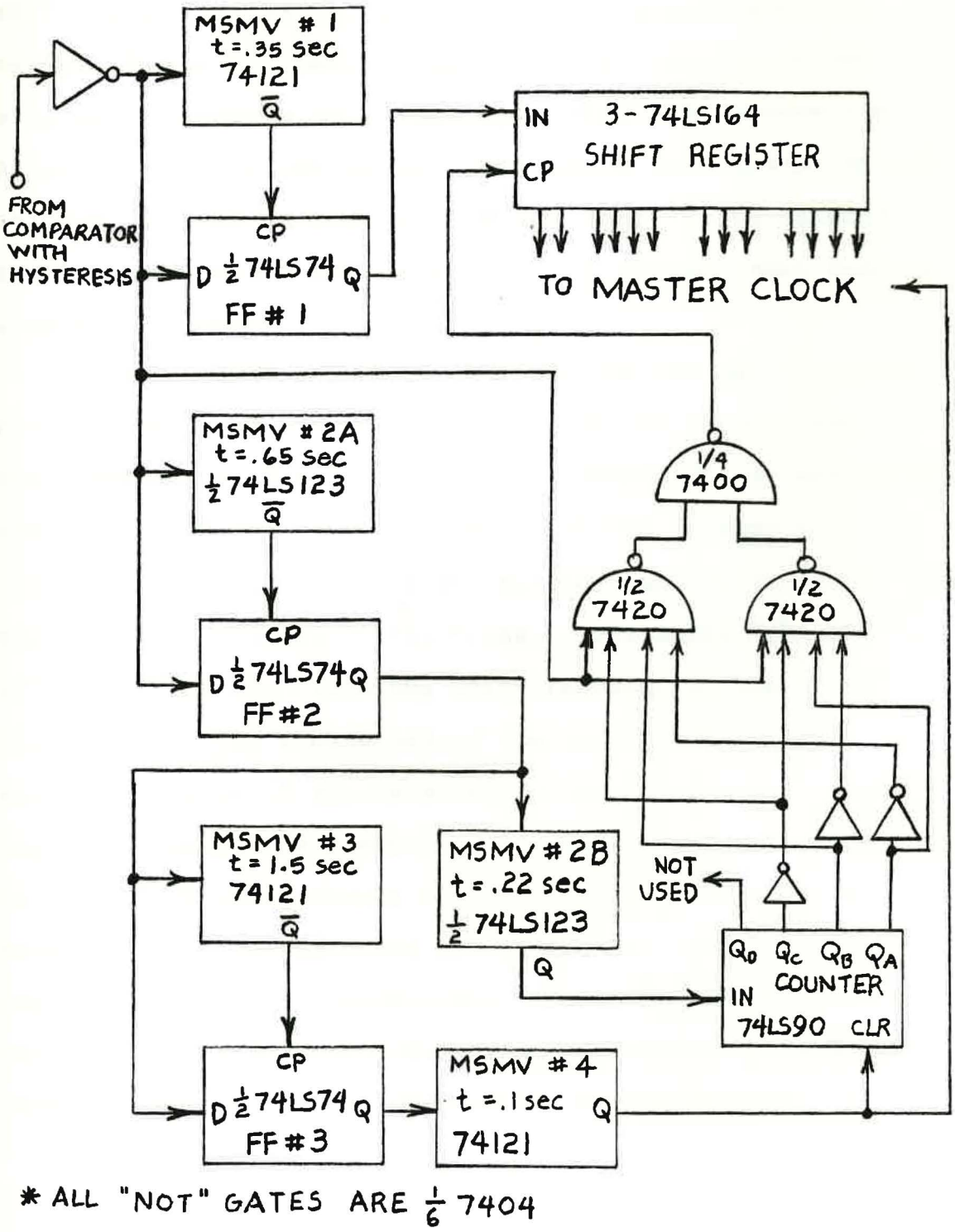


FIGURE 15 - Digital Decoding Block Diagram

The counter is used to supply clock pulses to the shift register only during the interval between position markers P1 and P3 (see FIGURES 11 and 16) when hours and minutes information is transmitted. MSMV #2B reduces the pulse length into the counter from one or two seconds to .22 seconds, so that no bits of data are lost. Three 74LS164 shift registers are used to convert the serial input code to a parallel output.

Due to the method of decoding and the WWV broadcast format, the decoded time will be behind the actual time. The reasons for this are most easily understood by examining FIGURES 11 and 16. From FIGURE 11, it can be seen that the time transmitted during the one minute frame is actually the time at the beginning of the frame. This means that the information latched into the shift register at the end of the minute is one minute behind the actual time. An additional error of approximately 1.15 seconds is incurred due to the method of decoding. As can be seen from FIGURE 16, the pulse that strobes the latches is generated 1.15 seconds after the beginning of the minute. Both of these sources of error are unimportant, since the decoder will be interfaced to a microprocessor that will easily account for such errors (see "Interrupt Routine" in CHAPTER III).

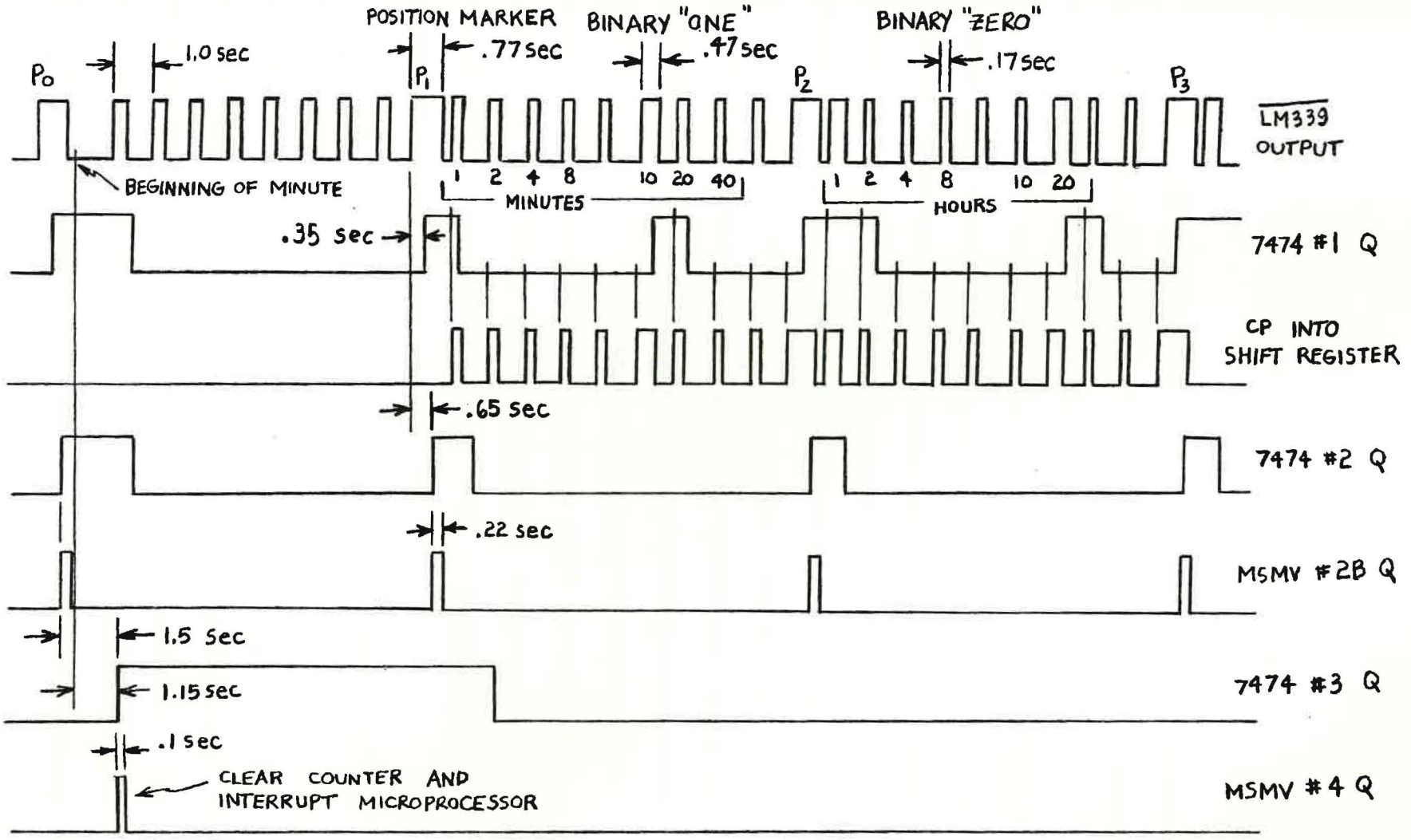


FIGURE 16 - Timing Diagram

V. CONCLUSIONS AND RECOMMENDATIONS

The new master clock and WWV decoder were built and worked as originally planned. There are, however, several areas for improvement that should be mentioned.

The WWV receiver uses a simple half-wave dipole antenna that is designed for reception of 15.0 MHz only. While it is felt that this arrangement provides adequate reception, a more broadband antenna would allow for better reception of the 5.0 and 10.0 MHz signals that the receiver is capable of receiving. To change the reception frequency, buttons on the presently installed receiver must be pushed manually. Receivers that automatically switch to the strongest carrier signal are commercially available and would be nice to have, but such a receiver might be too expensive to be practical. None of the above modifications would necessitate disabling the master clock at any time.

The real-time clock chip (MM58167) also contains a calendar that could be used for some specialized functions such as eliminating the EST / EDT switch or even ringing the bells on days and times that could be programmed into the EPROM now used to store the master clock software. The only disadvantage to undertaking such projects is that the master clock would have to be disabled while making any modifications.

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1. Ramshaw, R. S., Power Electronics, Chapman and Hall, London, 1973, pp. 37-39.

2. Howe, S. L., NBS Time and Frequency Dissemination Services, NBS Special Publication 432, U. S. Government Printing Office, Washington, DC, 1979, p. 2.

3. Ibid., p. 3.

4. Graeme, J. B., Operational Amplifiers, Design and Application, McGraw-Hill, 1971, pp. 293-295.

5. Schilling, D. L., Belove, C., Electronic Circuits, 2nd ed., McGraw-Hill, 1979, pp. 373-374.

6. Howe, S. L., p. 14.

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APPENDIX I

MASTER CLOCK OPERATION PROCEDURE AND MASTER CLOCK AND WWV DECODER DISASSEMBLY GUIDE

OPERATING PROCEDURE

First Power-Up Procedure

This procedure must be performed any time the master clock display time and school clock time do not match. All clocks must read within ten minutes of 3:00. This is accomplished by connecting normally open switches from wire 1 to wire 2 (switch #1) and from wire 4 to wire 5 (switch #2) (see FIGURE 17). Switch #1 should be opened and closed 70 times (0.5 second closed, 1.5 seconds open each time) while switch #2 remains open. All clocks should now read one minute before the hour. To advance to the next hour, close switch #2 and open and close switch #1 six times (same duty cycle as before). Now open switch #2, and then open and close switch #1 70 times. The clocks should now read one minute before the hour. Keep advancing to the next hour until the clocks read 2:59. If any clocks read, say, 1:59 or 3:59 while the majority of the others read 2:59, the clocks with erroneous readings must be manually advanced to read 2:59.

System Connections

When making connections, the power supply and WWV receiver should be OFF and UNPLUGGED.

1. Set the EST-DST switch on the master clock to the proper position.

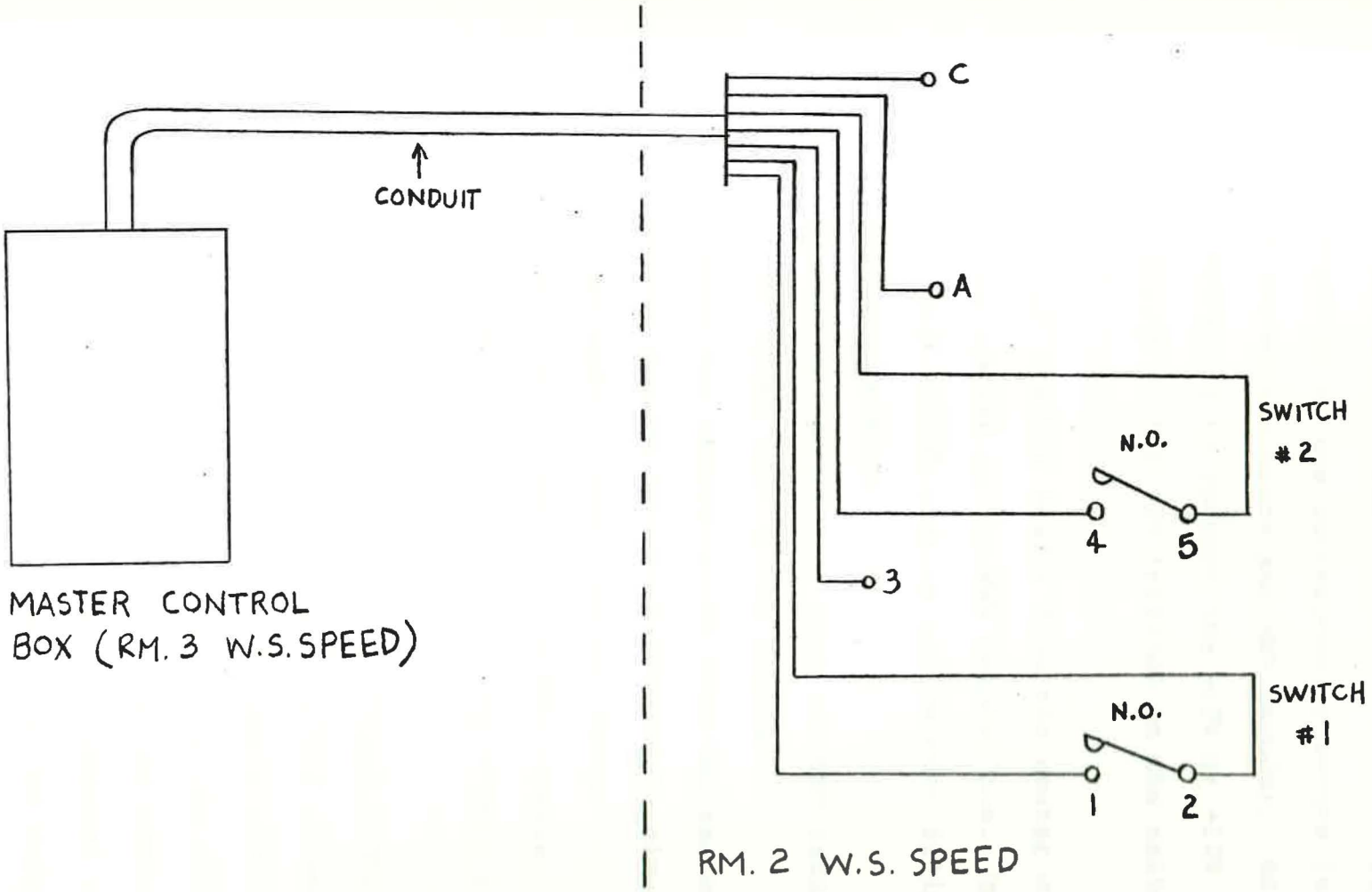


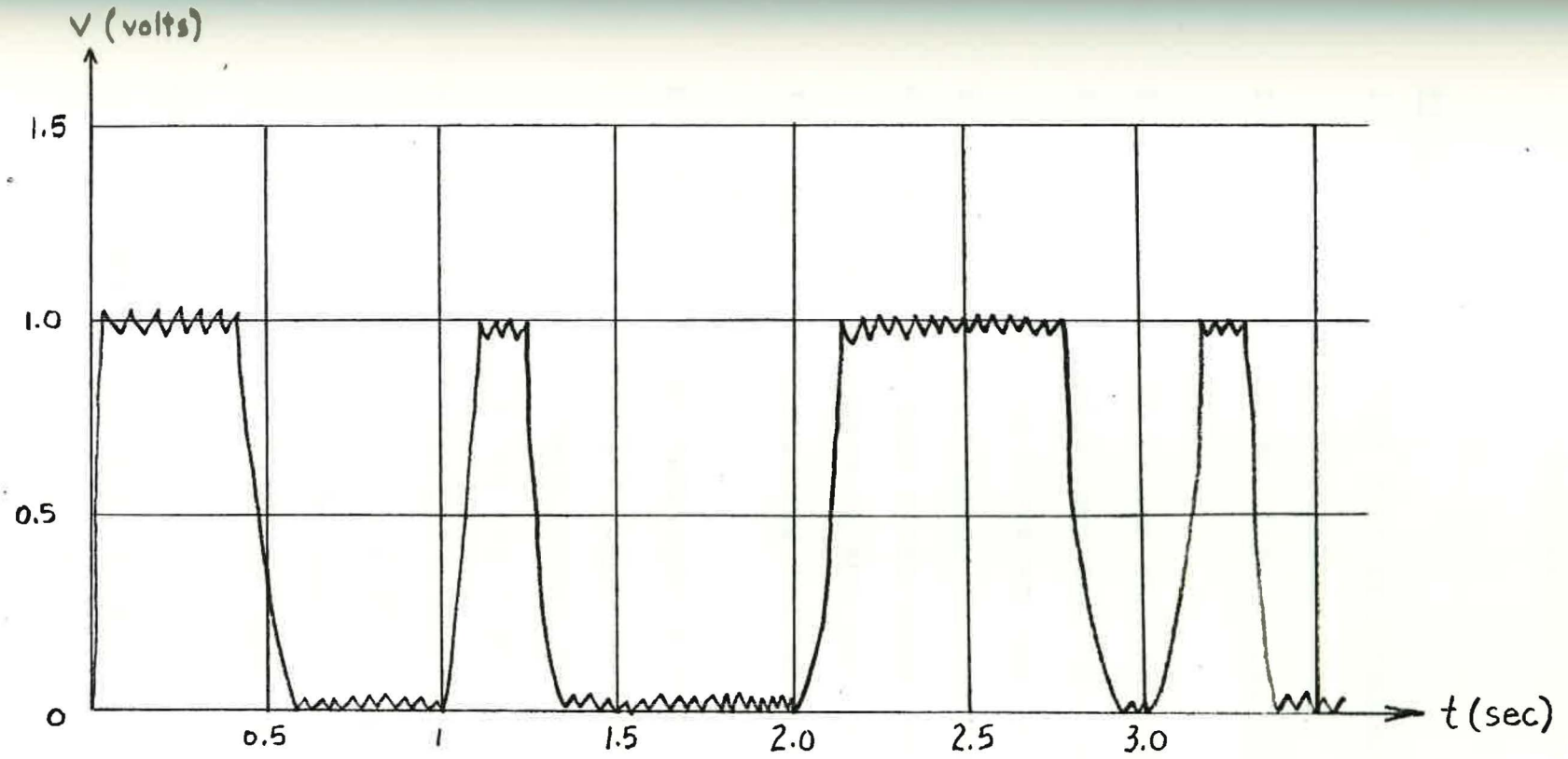
FIGURE 17 - Clock Advancement Connections

2. Using banana leads, connect the power supply terminals to the corresponding banana jacks on the master clock and WWV decoder. BE CAREFUL not to connect the -12V or +12V supplies to the +5V terminal on the master clock.
3. Connect the DIP header from the master clock to the socket on the WWV decoder box. Turn the GAIN ADJUST knob on the decoder fully counterclockwise.
4. Connect the phone plug from the WWV receiver to the phone jack on the decoder.
5. Connect the labeled wires from the master control box to the corresponding terminals on the master clock terminal strip.
6. Connect the antenna to the WWV receiver.
7. Plug the line cord of the power supply into a wall outlet.
8. Turn the power supply on by flipping the switch on the supply to the "on" position at exactly 3:00 PM. The system is now operational.
9. Connect the negative terminal of the standby battery to the GND terminal on the power supply and then connect the positive terminal of the battery to the STBY terminal on the supply.

10. Turn on the shortwave receiver and tune it to WWV at 15 MHz. The volume setting is unimportant, since the input to the decoder is taken before the volume control. When a clear, non-fading signal is present, probe the terminal of the decoder adjacent to the input jack with an oscilloscope. The GAIN CONTROL knob on the decoder should be adjusted so that the signal at this point resembles FIGURE 18. No further adjustment should be necessary unless a different receiver is used in the future.

If something happens to the receiver or decoder, the decoder can be disconnected from the master clock at any time without affecting master clock operation.

The system is now fully operational and should not require any further servicing other than replacing the standby battery once a year. To replace the battery, reverse the procedure of step 9 to remove the old one and install the new battery (refer to step 9).



PULSE WIDTHS ≈ .2, .5, OR .8 SEC

ADJUST GAIN CONTROL FOR PULSE HEIGHT OF ≈ 1.0 VOLT

FIGURE 18 - Proper Decoder Waveform

DISASSEMBLY GUIDE

Master Clock

1. The master clock must be disconnected from any power source during disassembly.
2. Remove the six Phillips screws from the top panel of the master clock.
3. Remove the two screws that hold the display in place.
4. Remove the two screws that hold the EST-DST switch in place. The top cover may now be removed.
5. Remove the four banana jacks from the cabinet.
6. Unsolder the four wires going from the main board to the smaller board in the left rear of the cabinet.
7. Remove the six screws that hold the main board in place.
8. Pull up on the left side of the board and, at the same time, feed the DIP jumper through the grommet enough to allow the board to be turned over, so that the solder connections are accessible.
9. To remove the smaller board, unsolder the four wires going to the triac and SCR, and then remove the two screws that hold the board in place.
10. To install the board(s), reverse the above procedure.

WWV Decoder

1. The WWV decoder must be disconnected from any power source during disassembly.

2. Remove the four screws from the top of the decoder.
3. Remove the four banana jacks from the cabinet.
4. Remove the two screws that hold the socket on the side of the decoder in place and push the socket toward the inside of the cabinet.
5. Unscrew the input jack retainer and push the jack toward the center of the cabinet.
6. Remove the screw next to the input jack by unscrewing it from the cabinet.
7. Remove the five nuts from the bottom of the box and pull the board from the cabinet.
8. To reinstall the board, reverse the above procedure.

APPENDIX II

MM58167* AND MC6802** DATA SHEETS

*MM58167 data sheets were taken from 1980 National Semiconductor MOS/LSI Databook.

**MC6802 data sheets were taken from 1980 Motorola Microprocessor Manual.

National Semiconductor

Electronic Data Processing

MM58167 Microprocessor Compatible Real Time Clock

General Description

The MM58167 is a low threshold metal-gate CMOS circuit that functions as a real time clock calendar in bus-oriented microprocessor systems. The device includes an addressable counter, addressable latch for alarm-type functions, and 2 interrupt outputs. A power-down input allows the chip to be disabled from the outside world for standby low power operation. The time base is generated from a 32,768 Hz crystal-controlled oscillator.

Features

- Microprocessor compatible
- Thousandths of seconds, hundredths of seconds, tenths of seconds, seconds, minutes, hours, day of the week, day of the month, and month counters with corresponding latches for alarm-type functions
- Interrupt output (maskable) with 8 possible interrupt signals:
  - Latch and counter comparison
  - Every tenth of a second
  - Every second
  - Every minute
  - Every hour
  - Every day
  - Every week
  - Every month
- Power-down mode that disables all outputs except for an interrupt output that occurs on a counter latch comparison. This is not the same as the maskable interrupt output
- Don't care states in the latches
- Status bit to indicate clock rollover during a read
- 32,768 Hz crystal reference, with only the input tuning capacitor and load capacitor needed externally
- Four year calendar

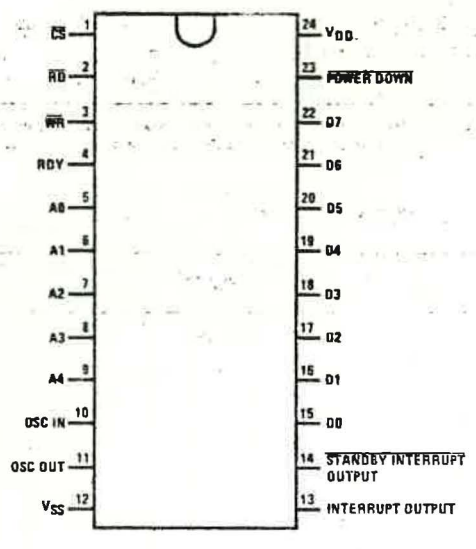
Functional Description

The MM58167 is a microprocessor oriented real time clock. The circuit includes addressable real time counters and addressable latches, each for thousandths of seconds through months. The counter and latch are divided into bytes of 4 bits each. When addressed, 2 bytes will appear on the data I/O bus. The data, in binary coded decimal, can be transferred to and from the counters via the data I/O bus so that each set of 2 bytes (1 word) can be accessed independently as grouped in Table I.

If either of the bytes in the above 8-bit counter words do not legally reach 4-bit lengths (e.g., day of the week uses only the 3 least significant bits) the unused bits will be unrecognized during a write and held at V_{SS} during a read. If any illegal data is entered into the counters during a write cycle, it may take up to 4 clocks (4 months in the case of the month counter) to restore legal BCD data to the counter during normal counting. The latches will read and write all 4 bits per byte. Each of the counter and latch words can be reset with the appropriate address and data inputs. The counter reset is a write function. The latches can be programmed to compare with the counters at all times by writing 1's into the 2 most significant bits of each latch, thus establishing a don't care state in the latch. The don't care state is programmable on the byte level, i.e., tens of hours can contain a don't care state, yet unit hours can contain a valid code necessary for a comparison.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number MM58167N
See Package 22

Absolute Maximum Ratings

Voltage at All Inputs and Outputs	V_{DD} + 0.3 to V_{SS} − 0.3
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
$V_{DD} - V_{SS}$	6V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{SS} = 0V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage					
V_{DD}	Outputs Enabled	4.0		5.5	V
V_{DD} (Note 1)	Power Down Mode	2.0		5.5	V
Supply Current					
I_{DD}, Static	Outputs TRI-STATE, f_{IN} = DC, V_{DD} = 5.5V			10	μA
I_{DD}, Dynamic	Outputs TRI-STATE, f_{IN} = 32 kHz, V_{DD} = 5.5V, $V_{IH} \geq V_{DD} - 0.3V$, $V_{IL} \leq V_{SS} + 0.3V$			20	μA
I_{DD}, Dynamic	Outputs TRI-STATE, f_{IN} = 32 kHz, V_{DD} = 5.5V, V_{IH} = 2.0V, V_{IL} = 0.8V			12	mA
Input Voltage					
Logical Low		0.0		0.8	V
Logical High		2.0		V_{DD}	V
Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$			1	μA
Output Impedance	(I/O and Interrupt Output)				
Logical Low	V_{DD} = 4.75V, I_{OL} = 1.6 mA			0.4	V
Logical High	V_{DD} = 4.75V, I_{OH} = −400 μA,	2.4			V
	I_{OH} = −10 μA	0.8 V_{DD}			V
TRI-STATE®	V_{OUT} = 0V,			−1	μA
	V_{OUT} = V_{DD}			1	μA
Output Impedance	(Ready and Standby Interrupt Output)				
Logical Low, Sink	V_{DD} = 4.75V, I_{OL} = 1.6 mA			0.4	V
Logical High, Leakage	$V_{OUT} \leq V_{DD}$			10	μA

Note 1: To insure that no illegal data is read from or written into the chip during power up, the power down input should be enabled only after all other lines (Read, Write, Chip Select, and Data Bus) are valid.

Functional Description (Continued)

TABLE I

COUNTER ADDRESSED	UNITS D0	D1	D2	D3	MAX USED BCD CODE	TENS D4	D5	D6	D7	MAX USED BCD CODE
Ten Thousandths of a Second	0	0	0	0	0	I/O	I/O	I/O	I/O	9
Tenths and Hundredths of Seconds	I/O	I/O	I/O	I/O	9	I/O	I/O	I/O	I/O	9
Seconds	I/O	I/O	I/O	I/O	9	I/O	I/O	I/O	0	5
Minutes	I/O	I/O	I/O	I/O	9	I/O	I/O	I/O	0	5
Hours	I/O	I/O	I/O	I/O	9	I/O	I/O	0	0	2
Day of the Week	I/O	I/O	I/O	0	7	0	0	0	0	0
Day of the Month	I/O	I/O	I/O	I/O	9	I/O	I/O	0	0	3
Month	I/O	I/O	I/O	I/O	9	I/O	0	0	0	1

Functional Description (Continued)

TABLE II. ADDRESS CODES AND FUNCTIONS

A4	A3	A2	A1	A0	FUNCTION
0	0	0	0	0	Counter — Thousandths of Seconds
0	0	0	0	1	Counter — Hundredths and Tenths of Seconds
0	0	0	1	0	Counter — Seconds
0	0	0	1	1	Counter — Minutes
0	0	1	0	0	Counter — Hours
0	0	1	0	1	Counter — Day of the Week
0	0	1	1	0	Counter — Day of the Month
0	0	1	1	1	Counter — Months
0	1	0	0	0	Latches — Thousandths of Seconds
0	1	0	0	1	Latches — Hundredths and Tenths of Seconds
0	1	0	1	0	Latches — Seconds
0	1	0	1	1	Latches — Minutes
0	1	1	0	0	Latches — Hours
0	1	1	0	1	Latches — Day of the Week
0	1	1	1	0	Latches — Day of the Month
0	1	1	1	1	Latches — Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	Latch Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	"GO" Command
1	0	1	1	0	Standby Interrupt
1	1	1	1	1	Test Mode

All others unused.

TABLE III. COUNTER AND LATCH RESET FORMAT

D0	D1	D2	D3	D4	D5	D6	D7	COUNTER OR LATCH RESET
1	0	0	0	0	0	0	0	Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Days of the Week
0	0	0	0	0	0	1	0	Days of the Month
0	0	0	0	0	0	0	1	Months

FOR COUNTER RESET A4—A0 MUST BE 10010

FOR LATCH RESET A4—A0 MUST BE 10011

Functional Description (Continued)

Following a read of any real time counter a status bit read should be done. If during a counter read cycle the clock rolls over, the data read out could be invalid. Thus, during a read if the clock rolls over the status bit will be set. The status bit will appear on D0 when read, D1 through D7 will be zeros.

To synchronize the clock with real time a "GO" command exists which can be used to reset the thousandths of seconds, hundredths and tenths of seconds, and seconds counters. After setting the lower frequency counters (minutes through months), the appropriate address and a write pulse can be sent to reset all counters mentioned above. This allows the clock to be started at an exactly known time. It can also be used as a stopwatch function. The "GO" command is the start and a counter read is the stop point. The clock does not stop during or following a read, so each read would be a split time.

A second special command will enable the standby interrupt output. The standby interrupt output is the only input or output enabled during the power down or standby mode. Power down occurs when the power down input goes to a logical zero level. In this mode the outputs are TRI-STATED and the inputs ignored regardless of the state of the chip select. The standby interrupt is enabled by writing a 1 on the D0 line with the standby interrupt address selected. On the next counter-latch comparison the open drain output device turns on, sinking current. The output will be turned on immediately upon writing a 1 on D0 if the comparison occurred before the write, yet is still in effect. To disable the output a zero on D0 is written at the standby interrupt address. The write cycles must occur during normal operation, but the output can become active during power down. This feature can be used to turn the power back on during a power down mode (see *Figure 4* for a typical application). Refer to Tables II and III for the address input codes and functions and for the counter and latch reset format.

The interrupt output is controlled by the interrupt status register (8 bits) and the interrupt control register (8 bits). The status register contains the present state of the comparator (compares the counters and latches) and the outputs (1 bit each) of the tenths of seconds, seconds, minutes, hours, week, day of the month, and month counters *(Figure 1)*. The interrupt status register can only be read. The interrupt control register is a mask register that regulates which of the 8 bits in the status register goes out as an interrupt. The control register cannot be read from. A 1 is written into the control register to select the appropriate interrupt output. If more than a single 1 exists in the control register each selected bit will come out as an interrupt. This will appear as an interrupt occurring at the highest frequency selected. The interrupt is acknowledged by addressing and reading the status register. Once acknowledged the interrupt output and status register are reset. The only way to disable the interrupt output is to write all 0's into the control register or to enable the power down input.

The I/O bus is controlled by the read, write, ready and chip select lines. During a read cycle ($\overline{RD}$ = 0, $\overline{WR}$ = 1, $\overline{CS}$ = 0, RDY = 0) the data on the I/O bus is the data contained in the addressed counter or latch. During a write cycle ($\overline{RD}$ = 1, $\overline{WR}$ = 0, $\overline{CS}$ = 0, RDY = 0) the data on the I/O bus is latched into the addressed counter or latch. At the start of each read or write cycle the RDY signal goes low and will remain low until the clock has placed valid data on the bus or until it has completed latching data in on a write. The chip select line is used to enable or disable the device outputs. When the chip is selected the device will drive the I/O bus for a read or use the I/O bus as an input for a write. The I/O bus will not be affected when the chip is deselected. The outputs driving the bus will go to the TRI-STATE or high impedance state. The chip will not respond to any inputs when deselected. Refer to *Figures 2 and 3* for read and write cycle timing.

The clock's time base is a 32,768 crystal controlled oscillator. Externally, the crystal, the input tuning capacitor, and the output load capacitor are required. Included internally are a high gain inverter, an RC delay, and the bias resistor. To tune the oscillator a constant read can be done on one of the higher frequency counters. For example, a constant read of the thousandths of seconds counter will place an average 500 Hz signal on the D4 bus line. The period varies slightly due to disable of latches during counter roll.

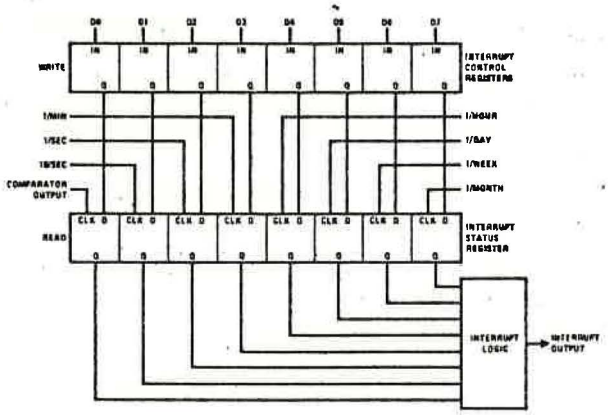


FIGURE 1. Interrupt Register Format

Read Cycle Timing Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 4.0V$ to $5.5V$, $V_{SS} = 0V$

	PARAMETER	MIN	TYP	MAX	UNITS
t_{AR}	Address Bus Valid to Read Strobe	100			ns
t_{CSR}	Chip Select ON to Read Strobe	0			ns
t_{RRY}	Read Strobe to Ready Strobe			150	ns
t_{RYD}	Ready Strobe to Data Valid			800	ns
t_{AD}	Address Bus Valid to Data Valid			1050	ns
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	0			ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode			250	ns
t_{RYH}	Read Hold Time After Ready Strobe	0			ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50			ns

Data bus loading is 100 pF
Ready output loading is 50 pF
Input and output AC timing levels are:
Logical "1" = 2.0V
Logical "0" = 0.8V

Write Cycle Timing Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 4.0V$ to $5.5V$, $V_{SS} = 0V$

	PARAMETER	MIN	TYP	MAX	UNITS
t_{AW}	Address Valid to Write Strobe	100			ns
t_{CSW}	Chip Select ON to Write Strobe	0			ns
t_{DW}	Data Valid Before Write Strobe	100			ns
t_{WRY}	Write Strobe to Ready Strobe			150	ns
t_{RY}	Ready Strobe Width			800	ns
t_{RYH}	Write Hold Time After Ready Strobe	0			ns
t_{WD}	Data Hold Time After Write Strobe	110			ns
t_{WA}	Address Hold Time After Write Strobe	50			ns

Data bus loading is 100 pF
Ready output loading is 50 pF
Input and output AC timing levels are:
Logical "1" = 2.0V
Logical "0" = 0.8V

Switching Time Waveforms

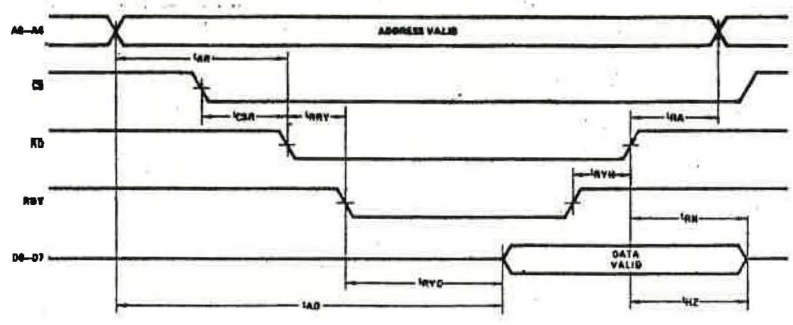


FIGURE 2. Read Cycle Waveforms

Switching Time Waveforms (Continued)

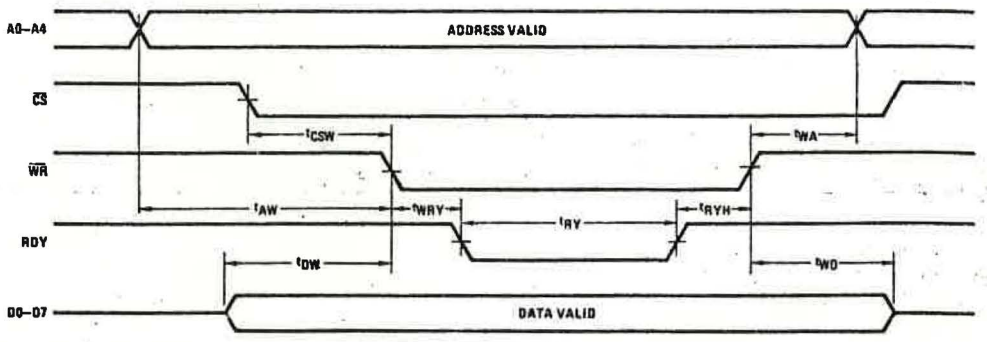


FIGURE 3. Write Cycle Waveforms

Typical Application

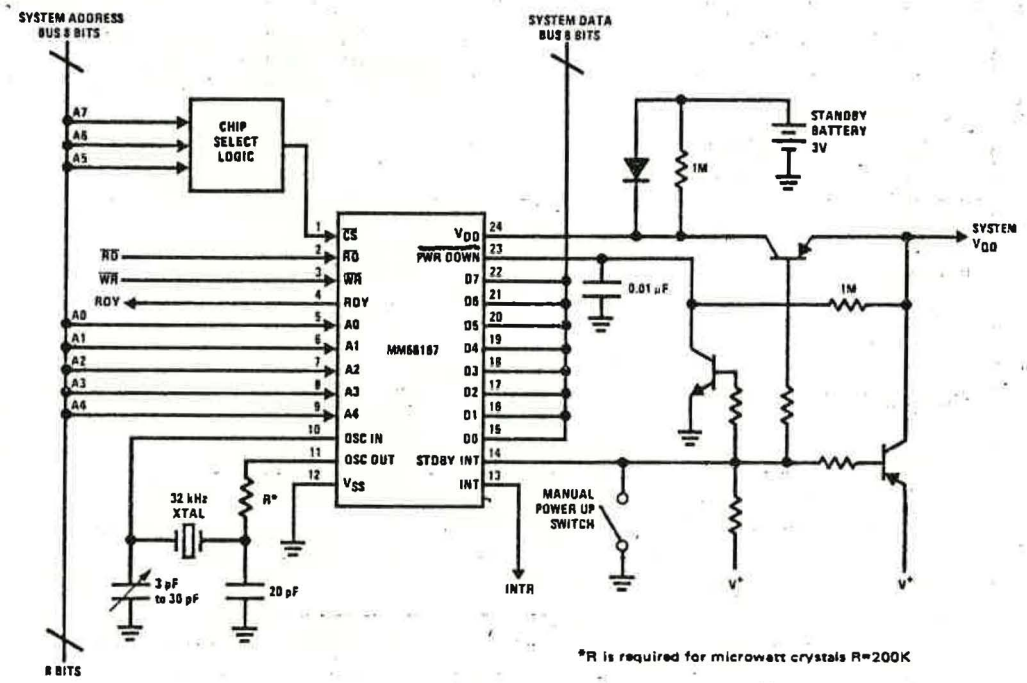


FIGURE 4. Standby Interrupt is Enabled (ON) for Normal Operation and Disabled for Standby Operation

MOTOROLA

MC6802
MC6808
MC6802NS

MICROPROCESSOR WITH CLOCK AND OPTIONAL RAM

The MC6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present MC6800 plus an internal clock oscillator and driver on the same chip. In addition, the MC6802 has 128 bytes of on-board RAM located at hex addresses $0000 to $007F. The first 32 bytes of RAM, at hex addresses $0000 to $001F, may be retained in a low power mode by utilizing V_{CC} standby, thus, facilitating memory retention during a power-down situation.

The MC6802 is completely software compatible with the MC6800 as well as the entire M6800 family of parts. Hence, the MC6802 is expandable to 64K words.

The MC6802NS is identical to the MC6802 without standby RAM feature. The MC6808 is identical to the MC6802 without on-board RAM.

- On-Chip Clock Circuit
- 128 × 8 Bit On-Chip RAM
- 32 Bytes of RAM are Retainable
- Software-Compatible with the MC6800
- Expandable to 64K Words
- Standard TTL-Compatible Inputs and Outputs
- 8-Bit Word Size
- 16-Bit Memory Addressing
- Interrupt Capability

PART NUMBER DESIGNATION BY SPEED

MC6802 (1.0 MHz)	MC6808 (1.0 MHz)	MC6802NS (1.0 MHz)
MC68A02 (1.5 MHz)	MC68A08 (1.5 MHz)	
MC68B02 (2.0 MHz)	MC68B08 (2.0 MHz)	

MOS

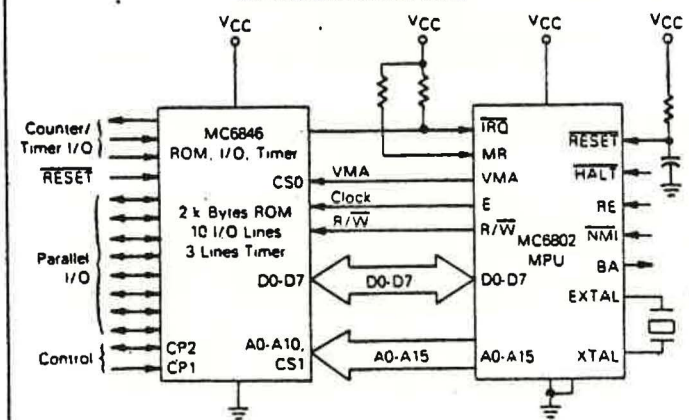
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

MICROPROCESSOR WITH CLOCK AND OPTIONAL RAM

L SUFFIX
CERAMIC PACKAGE
CASE 715

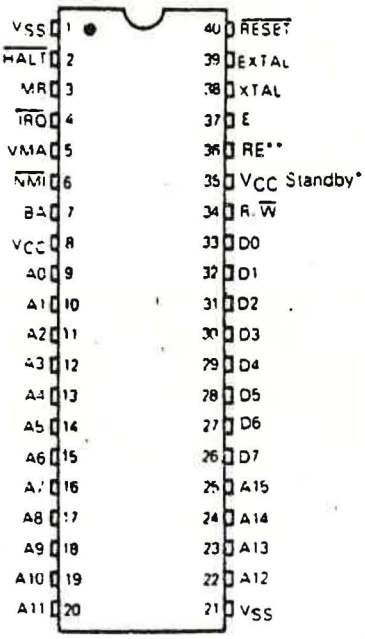
P SUFFIX
PLASTIC PACKAGE
CASE 711

TYPICAL MICROCOMPUTER



This block diagram shows a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

PIN ASSIGNMENT



*Pin 35 must be tied to 5 V on the 6802NS
**Pin 36 must be tied to ground for the 6808

OPERATING TEMPERATURE RANGE

Device	Speed	Symbol	Value	Unit
MC6802P,L MC6802CP,CL	(1.0 MHz) (1.0 MHz)	T_A	0 to +70 −40 to +85	°C
MC68A02P,L MC68A02CP,CL	(1.5 MHz) (1.5 MHz)	T_A	0 to +70 −40 to +85	°C
MC68B02P,L MC68B02CP,CL	(2.0 MHz) (2.0 MHz)	T_A	0 to +70 −40 to +85	°C
MC6802NSP,L	(1.0 MHz)	T_A	0 to +70	°C
MC6808P,L MC68A08P,L MC68B08P,L	(1.0 MHz) (1.5 MHz) (2.0 MHz)	T_A	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = 0 to 70°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, EXTAL, $\overline{RESET}$	V_{IH}	V_{SS} + 2.0 V_{SS} + 4.0	–	V_{CC} V_{CC}	V
Input Low Voltage	Logic, EXTAL, $\overline{RESET}$	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic	I_{in}	–	1.0	2.5	μA
Output High Voltage (I_{Load} = − 205 μA, V_{CC} = min) (I_{Load} = − 145 μA, V_{CC} = min) (I_{Load} = − 100 μA, V_{CC} = min)	D0-D7 A0-A15, R/$\overline{W}$, VMA, E BA	V_{OH}	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	– – –	– – –	V
Output Low Voltage (I_{Load} = 1.6 mA, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	0.600	1.0	W
V_{CC} Standby	Power Down Power Up	V_{SB} V_{SB}	4.0 4.75	–	5.25 5.25	V
Standby Current		I_{SB}		–	8.0	mA
Capacitance # (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7 Logic Inputs, EXTAL A0-A15, R/$\overline{W}$, VMA	C_{in} C_{out}		10 6.5 	12.5 10 12	pF pF

*In power-down mode, maximum power dissipation is less than 42 mW

#Capacitances are periodically sampled rather than 100% tested

CONTROL TIMING (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Characteristics	Symbol	MC6802NS, MC6808		MC68A02 MC68A08		MC68B02 MC68B08		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_o	0.1	1.0	0.1	1.5	0.1	2.0	MHz
Crystal Frequency	f_{XTAL}	1.0	4.0	1.0	6.0	1.0	8.0	MHz
External Oscillator Frequency	$4xf_o$	0.4	4.0	0.4	6.0	0.4	8.0	MHz
Crystal Oscillator Start Up Time	t_{rc}	100	–	100	–	100	–	ms
Processor Controls (HALT, MR, RE, RESET, IRQ NMI) Processor Control Setup Time Processor Control Rise and Fall Time (Does Not Apply to $\overline{RESET}$)	 t_{PCS} t_{PCr}, t_{PCf}	 200 –	 – 100	 140 –	 – 100	 110 –	 – 100	 ns ns

WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

INTERRUPT REQUEST ($\overline{IRQ}$)

A low level on this input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being excuted before it recognizes the request. At that time, if the interrupt mask bit in the condition code register is not set, the machine will begin an interrupt sequence. The index register, program counter, accumulators, and condition code register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit vectoring address which is located in memory locations $FFF8 and $FFF9 is loaded which causes the MPU to branch to an interrupt routine in memory.

The $\overline{HALT}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{HALT}$ is low.

A nominal 3 kΩ pullup resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. $\overline{IRQ}$ may be tied directly to V_{CC} if not used.

$\overline{RESET}$

This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the information in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two ($FFFE, $FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{IRQ}$. Power-up and reset timing and power-down sequences are shown in Figures 9 and 10, respectively.

$\overline{RESET}$, when brought low, must be held low at least three clock cycles. This allows adequate time to respond internally to the reset. This is independent of the t_{rc} power-up reset that is required.

When $\overline{RESET}$ is released it *must* go through the low-to-high threshold without bouncing, oscillating, or otherwise causing an erroneous reset (less than three clock cycles). This may cause improper MPU operation until the next valid reset.

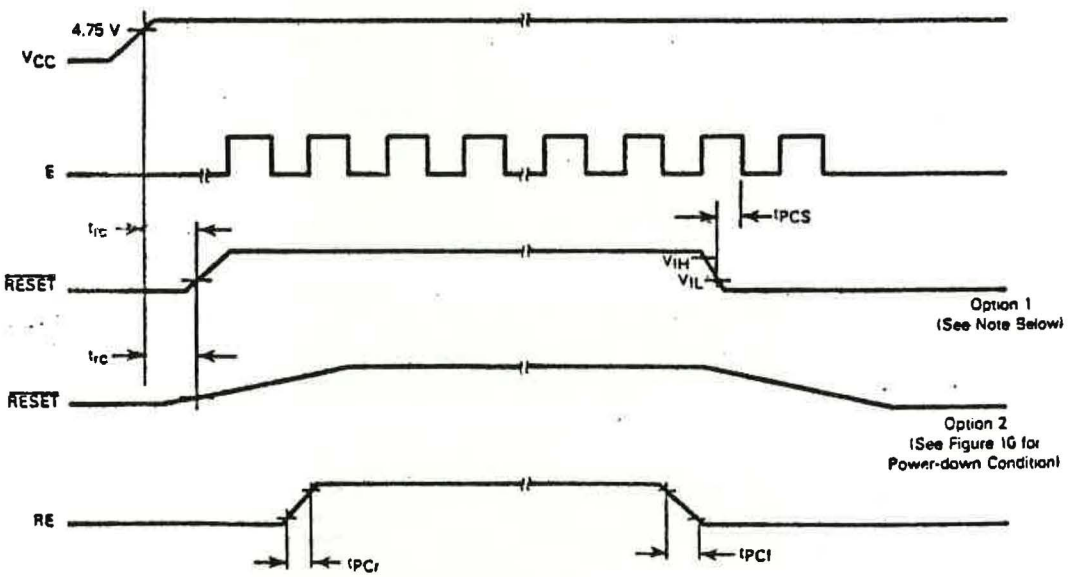
NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A low-going edge on this input requests that a nonmaskable interrupt sequence be generated within the processor. As with the interrupt request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{NMI}$ signal. The interrupt mask bit in the condition code register has no effect on $\overline{NMI}$.

The index register, program counter, accumulators, and condition code registers are stored away on the stack. At the end of the cycle, a 16-bit vectoring address which is located in memory locations $FFFC and $FFFD is loaded causing the MPU to branch to an interrupt service routine in memory.

A nominal 3 kΩ pullup resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. $\overline{NMI}$ may be tied

FIGURE 9 — POWER-UP AND RESET TIMING



NOTE: If option 1 is chosen, $\overline{RESET}$ and RE pins can be tied together.

RAM ENABLE (RE — MC6802 + MC6802NS ONLY)

A TTL-compatible RAM enable input controls the on-chip RAM of the MC6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during a power-down situation. RAM Enable must be low three cycles before V_{CC} goes below 4.75 V during power-down. RAM enable must be tied low on the MC6808. RE should be tied to the correct high or low state if not used.

EXTAL AND XTAL

These inputs are used for the internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal (see Figure 12). (AT-cut.) A divide-by-four circuit has been added so a 4 MHz crystal may be used in lieu of a 1 MHz crystal for a more cost-effective system. An example of the crystal circuit layout is shown in Figure 13. Pin 39 may be driven externally by a TTL input signal four times the required E clock frequency. Pin 38 is to be grounded.

An RC network is not directly usable as a frequency source on pins 38 and 39. An RC network type TTL or CMOS oscillator will work well as long as the TTL or CMOS output drives the on-chip oscillator.

LC networks are not recommended to be used in place of the crystal.

If an external clock is used, it may not be halted for more than $t_{PW\phi L}$. The MC6802, MC6808 and MC6802NS are dynamic parts except for the internal RAM, and require the external clock to retain information.

MEMORY READY (MR)

MR is a TTL-compatible input signal controlling the stretching of E. Use of MR requires synchronization with the $4xf_o$ signal, as shown in Figure 14. When MR is high, E will be in normal operation. When MR is low, E will be stretched integral numbers of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Figure 15.

MR should be tied high (connected directly to V_{CC}) if not used. This is necessary to ensure proper operation of the part. A maximum stretch is t_{cyc}.

ENABLE (E)

This pin supplies the clock for the MPU and the rest of the system. This is a single-phase, TTL-compatible clock. This clock may be conditioned by a memory read signal. This is equivalent to $\phi 2$ on the MC6800. This output is capable of driving one standard TTL load and 130 pF.

V_{CC} STANDBY (MC6802 ONLY)

This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus, retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed. Maximum current drain at V_{SB} maximum is I_{SBB}. For the MC6802NS this pin must be connected to V_{CC}.

APPENDIX III

SYSTEM SOFTWARE ASSEMBLED LISTING AND FLOWCHARTS

```
00001                   ;JAY PFEIFER, THESIS PROJECT
00002                   ;    THIS IS THE SOFTWARE FOR CONTROLLING THE SPEED SCHOOL
00003                   ;CLOCKS.  TIMES FROM A REAL-TIME CLOCK, WWV, AND THE
00004                   ;SCHOOL CLOCKS ARE CONTINUOUSLY COMPARED AND PULSES TO
00005                   ;THE SCHOOL CLOCKS ARE GENERATED AT THE PROPER INSTANTS.
00006                   ;*************************************************************
00007                   ;TABLE OF MEMORY LOCATIONS
00008                   ;*************************
00009                   ;00H-7FH - RANDOM ACCESS MEMORY (RAM)
00010                   ;00H     - USED TO CHECK FOR FIRST POWER-UP
00011                   ;01H,02H - 24 HR SCHOOL CLOCK TIME (02H=HRS, 01H=MIN)
00012                   ;03H,04H - 24 HR REAL-TIME CLOCK TIME (04H=HRS, 03H=MIN)
00013                   ;05H,06H - 24 HR WWV TIME (06H=HRS, 05H=MIN)
00014                   ;07H,08H - PREVIOUS 24 HR WWV TIME + 1 MIN (08H=HRS, 07H=MIN)
00015                   ;09H,0AH - SECOND PREVIOUS 24 HR WWV TIME + 2 MIN (0AH=HRS, 09H=MIN)
00016                   ;0BH,0CH - TEMPORARY 24 HR WWV, RTC, OR SCHOOL CLOCK LOCATION
00017                   ;          (0CH=HRS, 0BH=MIN)
00018                   ;0DH,0EH - 12 HR SCHOOL CLOCK TIME (0EH=HRS, 0DH=MIN)
00019                   ;13H,14H - TEMPORARY 12 HR WWV, RTC, OR SCHOOL CLOCK LOCATION
00020                   ;          (14H=HRS, 13H=MIN)
00021                   ;15H     - NUMBER OF MINUTES DIFFERENCE IN HEX
00022                   ;16H     - NUMBER OF HOURS DIFFERENCE IN BCD
00023                   ;7FH     - INITIAL STACK POINTER LOCATION AND LAST ADDRESS OF RAM
00024                   ;1000H-17FFH - READ ONLY MEMORY (ROM)
00025                   ;2000H-2016H - REAL-TIME CLOCK
00026                   ;3000H-3001H - WWV TIME (FROM DECODER)
00027                   ;4000H-4003H - PERIPHERAL INTERFACE ADAPTER (PIA)
00028                   ;5000H       - ONE MINUTE SWITCH
00029                   ;6000H       - EST,DST SWITCH
00030                   ;7000H       - FIFTY MINUTE SWITCH
```

```
00031                    ;*****************************************************************
00032                    ;THIS IS THE POWER-UP SEQUENCE.  ON THE FIRST POWER-UP, THE
00033                    ;SCHOOL CLOCKS ARE ASSUMED TO BE AT 15:00  AND  THE REAL-TIME
00034                    ;CLOCK IS SET TO 15:00.  ON SUBSEQUENT POWER-UPS, THE DIFFERENCE
00035                    ;BETWEEN THE SCHOOL CLOCKS AND THE REAL-TIME CLOCK IS COMPUTED
00036                    ;AND THE SCHOOL CLOCKS ARE UPDATED.
00037                    ;*****************************************************************
00038      1000     >          ORG              1000H    ;BEGINNING ADDRESS IS 1000H.
00039 1000 0F                 SEI                       ;SET INTERRUPT MASK.
00040 1001 4F                 CLR      A                ;DISABLE RTC
00041 1002 B72016             STA      A       2016H    ;STANDBY INTERRUPT.
00042 1005 8608               LDA      A       #08H     ;GENERATE AN INTERRUPT .
00043 1007 B72011             STA      A       2011H    ;EVERY MINUTE.
00044 100A 86FF               LDA      A       #0FFH    ;CONFIGURE ALL PDRA &
00045 100C B74000             STA      A       4000H    ;PDRB LINES
00046 100F B74002             STA      A       4002H    ;AS OUTPUTS.
00047 1012 8604               LDA      A       #04H     ;SET BIT 2 OF CRA & CRB
00048 1014 B74001             STA      A       4001H    ;TO ALLOW ACCESS TO
00049 1017 B74003             STA      A       4003H    ;PDRA & PDRB.
00050 101A 8E007F             LDS              #007FH   ;INITIALIZE STACK POINTER.
00051 101D 8652               LDA      A       #52H     ;SEE IF THIS
00052 101F 9100               CMP      A       00H      ;IS THE FIRST
00053 1021 2721               BEQ              RESET    ;RESET OF THE SYSTEM.
00054 1023 B72015             STA      A       2015H    ;RESET RTC SECONDS.
00055 1026 8600               LDA      A       #00H     ;SET SCHOOL CLOCK MIN =00.
00056 1028 B72003             STA      A       2003H    ;WRITE TO RTC MINUTES.
00057 102B 9701               STA      A       01H      ;SCHOOL CLOCK MIN IN RAM.
00058 102D B74000             STA      A       4000H    ;PUT MIN ON DISPLAY.
00059 1030 9703               STA      A       03H      ;RTC MIN IN RAM.
00060 1032 8615               LDA      A       #15H     ;SET SCHOOL CLOCK HRS =15.
00061 1034 B72004             STA      A       2004H    ;WRITE TO RTC HOURS.
00062 1037 9702               STA      A       02H      ;SCHOOL CLOCK HOURS IN RAM.
00063 1039 B74002             STA      A       4002H    ;PUT HOURS ON DISPLAY.
00064 103C 9704               STA      A       04H      ;RTC HOURS IN RAM.
00065 103E 8652               LDA      A       #52H     ;SKIP THIS PART AFTER
00066 1040 9700               STA      A       00H      ;FIRST POWER-UP.
00067 1042 2038               BRA              MONITR   ;SKIP RESET.
```

```
00068                    ;*************************************************************
00069                    ;THIS IS THE RESET ROUTINE THAT IS EMPLOYED AFTER
00070                    ;EVERY POWER-UP EXCEPT THE FIRST.  UPON A POWER-UP, THE
00071                    ;REAL-TIME CLOCK AND SCHOOL CLOCK TIMES ARE COMPARED SO
00072                    ;THAT THE SCHOOL CLOCKS CAN BE RESET TO THE CORRECT TIME.
00073                    ;*************************************************************
00074 1044 B62010       RESET  LDA     A       2010H   ;CLEAR RTC INTERRUPT BIT.
00075 1047 DE01                LDX             01H     ;SCHOOL CLOCK TIME.
00076 1049 DF0B                STX             0BH     ;PREPARE TO CONVERT TO 12 HR FORMAT.
00077 104B BD1087  >           JSR             HRS12   ;12 HOUR FORMAT.
00078 104E DE13                LDX             13H     ;GET RESULT AND
00079 1050 DF0D                STX             0DH     ;STORE AT 0DH,0EH.
00080 1052 B62003       BADRD  LDA     A       2003H   ;RTC MINUTES.
00081 1055 F62014              LDA     B       2014H   ;   VALID
00082 1058 C501                BIT     B       #01H    ;   READ
00083 105A 26F6                BNE             BADRD   ;    ?
00084 105C 9703                STA     A       03H     ;IF YES, STORE MINUTES.
00085 105E 9713                STA     A       13H     ;
00086 1060 B62004              LDA     A       2004H   ;RTC HOURS.
00087 1063 F62014              LDA     B       2014H   ;   VALID
00088 1066 C501                BIT     B       #01H    ;   READ
00089 1068 26E8                BNE             BADRD   ;    ?
00090 106A 9704                STA     A       04H     ;IF YES, STORE HOURS.
00091 106C DE03                LDX             03H     ;PUT RTC TIME
00092 106E DF0B                STX             0BH     ;AT 0BH,0CH.
00093 1070 BD1087  >           JSR             HRS12   ;CONVERT RTC TIME TO 12 HR FORMAT.
00094 1073 BD10C3  >           JSR             MINCAL  ;CALCULATE MIN DIFFERENCE.
00095 1076 BD1097  >           JSR             HRSCAL  ;CALCULATE HRS DIFFERENCE.
00096 1079 BD1109  >           JSR             PULSER  ;UPDATE SCHOOL CLOCKS.
```

```
00097                    ;*****************************************************************
00098                    ;THIS IS THE MONITOR ROUTINE WHICH WAITS FOR A CHANGE IN
00099                    ;THE REAL-TIME CLOCK MINUTES OR A WWV END-OF-FRAME PULSE.
00100                    ;WHEN EITHER OF THESE OCCURS, AN INTERRUPT ROUTINE IS
00101                    ;SERVICED.
00102                    ;*****************************************************************
00103 107C 0E          MONITR CLI                          ;CLEAR INTERRUPT MASK.
00104 107D 3E                 WAI                          ;WAIT FOR AN INTERRUPT FROM
00105                                                      ;EITHER WWV OR RTC.
00106 107E 20FC               BRA              MONITR      ;AFTER INTERRUPT HAS BEEN
00107                                                      ;SERVICED, WAIT FOR ANOTHER.
00108                    ;*****************************************************************
00109                    ;THIS ROUTINE GIVES A DELAY OF .9990 SECONDS AND IS USED
00110                    ;WHEN EITHER SENDING PULSES TO THE SCHOOL CLOCKS OR WAITING
00111                    ;FOR THE SCHOOL CLOCKS TO CATCH UP.
00112                    ;*****************************************************************
00113 1080 CEF3E5      SECDLY LDX              #62437      ;THIS LOOP GIVES
00114 1083 09          LOOP1  DEX                          ;A DELAY OF
00115 1084 26FD               BNE              LOOP1       ;.9990 SEC.
00116 1086 39                 RTS                          ;GO BACK.
00117                    ;*****************************************************************
00118                    ;THIS ROUTINE CONVERTS A 24-HOUR FORMAT TIME TO A 12-HOUR
00119                    ;FORMAT TIME.
00120                    ;*****************************************************************
00121 1087 960C         HRS12  LDA      A       OCH         ;HRS TO BE CONVERTED.
00122 1089 8B88               ADD      A       #88H        ;TENS COMPLEMENT OF 12.
00123 108B 19                 DAA                          ;BCD RESULT.
00124 108C 2502               BCS              GTTH12      ;IF POS, GO TO GTTH12.
00125 108E 960C               LDA      A       OCH         ;IF NEG, HRS ARE ALREADY
00126 1090 9714         GTTH12 STA      A       14H         ;IN A 12 HR FORMAT.
00127 1092 960B               LDA      A       OBH         ;MOVE MINUTES INFORMATION
00128 1094 9713               STA      A       13H         ;TO 12 HR LOCATION.
00129 1096 39                 RTS                          ;GO BACK.
```

```
00130                    ;*****************************************************************
00131                    ;THIS ROUTINE CALCULATES THE NUMBER OF HOURS THAT THE SCHOOL
00132                    ;CLOCKS MUST BE ADVANCED IN ORDER TO BE SYNCHRONIZED WITH
00133                    ;EITHER THE REAL-TIME CLOCK OR WWV.
00134                    ;*****************************************************************
00135 1097 960E         HRSCAL LDA      A       0EH     ;SCHOOL CLOCK HOURS TO BE SUBTRACTED
00136                                                    ;FROM WWV OR RTC HRS.
00137 1099 8B66                ADD      A       #66H    ;    FORM
00138 109B 43                  COM      A               ;    TENS
00139 109C 8B01                ADD      A       #01H    ;    COMPLEMENT.
00140 109E 19                  DAA                      ;BCD RESULT.
00141 109F D614                LDA      B       14H     ;WWV OR RTC HOURS.
00142 10A1 1B                  ABA                      ;(WWV OR RTC)HRS - SCHOOL CLK HOURS.
00143 10A2 19                  DAA                      ;BCD RESULT.
00144 10A3 2705                BEQ              HRSDIF  ;NEEDED IF BOTH 12 HR TIMES HRS=00.
00145 10A5 2503                BCS              HRSDIF  ;C=1 IMPLIES POS RESULT.
00146 10A7 8B12                ADD      A       #12H    ;IF NEG RESULT, ADD 12.
00147 10A9 19                  DAA                      ;BCD RESULT.
00148 10AA 9716         HRSDIF STA      A       16H     ;STORE HRS DIFF.
00149 10AC 39                  RTS                      ;GO BACK.
00150                    ;*****************************************************************
00151                    ;THIS ROUTINE UPDATES THE VISUAL DISPLAY OF THE SCHOOL CLOCK
00152                    ;TIME LOCATED IN RAM.  THIS ROUTINE IS ACCESSED IMMEDIATELY
00153                    ;AFTER A PULSE HAS BEEN SENT TO THE CLOCKS.
00154                    ;*****************************************************************
00155 10AD DE01         UPDATE LDX              01H     ;SCHOOL CLK INFO.
00156 10AF DF0B                STX              0BH     ;TEMPORARY REGISTER.
00157 10B1 BD10EA    >         JSR              ADDMIN  ;INCREMENT TIME.
00158 10B4 DE0B                LDX              0BH     ;GET INCREMENTED TIME.
00159 10B6 DF01                STX              01H     ;PUT SCHOOL CLOCK TIME IN RAM.
00160 10B8 9601                LDA      A       01H     ;SCHOOL CLOCK MINUTES.
00161 10BA B74000              STA      A       4000H   ;MINUTES TO PIA.
00162 10BD 9602                LDA      A       02H     ;SCHOOL CLK HOURS.
00163 10BF B74002              STA      A       4002H   ;HOURS TO PIA.
00164 10C2 39                  RTS                      ;GO BACK.
```

```
00165                   ;*****************************************************************
00166                   ;THIS ROUTINE CALCULATES THE NUMBER OF MINUTES THAT THE
00167                   ;SCHOOL CLOCKS MUST BE ADVANCED IN ORDER TO CATCH UP WITH
00168                   ;EITHER WWV OR THE REAL-TIME CLOCK.
00169                   ;*****************************************************************
00170 10C3 5F         MINCAL CLR     B                    ;CLEAR COUNTER.
00171 10C4 960D              LDA     A       0DH          ;SCHOOL CLOCK MINUTES.
00172 10C6 9113       ZERMIN CMP     A       13H          ;SEE IF WWV OR RTC MINUTES
00173 10C8 271D              BEQ             FINISH       ;ARE THE SAME AS SCHOOL CLOCK MINUTES.
00174 10CA 8B01              ADD     A       #01H         ;INCREMENT SCHOOL TIME 1 MINUTE.
00175 10CC 19                DAA                          ;BCD RESULT.
00176 10CD 5C                INC     B                    ;INCREMENT COUNTER.
00177 10CE 8160              CMP     A       #60H         ;HOUR ROLLOVER?
00178 10D0 2702              BEQ             EOHOUR       ;IF YES, MAKE ADJUSTMENTS.
00179 10D2 20F2              BRA             ZERMIN       ;IF SAME, KEEP DETERMINING DIFFERENCE.
00180 10D4 960E       EOHOUR LDA     A       0EH          ;GET SCHOOL CLK HOURS.
00181 10D6 8B01              ADD     A       #01H         ;INCREMENT HOURS.
00182 10D8 19                DAA                          ;BCD RESULT.
00183 10D9 8112              CMP     A       #12H         ;HOURS = 12?
00184 10DB 2705              BEQ             ZERHR        ;IF YES, MAKE HOURS = 00.
00185 10DD 970E              STA     A       0EH          ;IF NOT, STORE RESULT.
00186 10DF 4F                CLR     A                    ;SET MIN = 00.
00187 10E0 20E4              BRA             ZERMIN       ;KEEP DETERMINING MIN DIFFERENCE.
00188 10E2 4F         ZERHR  CLR     A                    ;HRS= 00.
00189 10E3 970E              STA     A       0EH          ;STORE HRS= 00.
00190 10E5 20DF              BRA             ZERMIN       ;KEEP DETERMINING MIN DIFFERENCE.
00191 10E7 D715       FINISH STA     B       15H          ;STORE MIN DIFFERENCE.
00192 10E9 39                RTS                          ;GO BACK.
```

```
00193                   ;*****************************************************************
00194                   ;THIS ROUTINE ADDS ONE MINUTE TO A 24 HOUR FORMAT BCD TIME,
00195                   ;TAKING INTO ACCOUNT MINUTES ROLLOVER, HOURS ROLLOVER, AND
00196                   ;TENS OF HOURS ROLLOVER.  EX;  23:59 + 00:01 = 00:00
00197                   ;*****************************************************************
00198 10EA 960B   ADDMIN LDA     A       OBH     ;MINUTES TO BE INCREMENTED.
00199 10EC 8B01         ADD     A       #01H    ;INCREMENT MINUTES.
00200 10EE 19           DAA                     ;BCD RESULT.
00201 10EF 8160         CMP     A       #60H    ;END OF HOUR?
00202 10F1 2703         BEQ             ENDHR   ;IF YES, SET MINUTES= 00.
00203 10F3 970B         STA     A       OBH     ;IF NO, STORE RESULT
00204 10F5 39           RTS                     ;AND GO BACK.
00205 10F6 4F     ENDHR CLR     A               ;CLEAR MINUTES
00206 10F7 970B         STA     A       OBH     ;AND ADD
00207 10F9 960C         LDA     A       OCH     ;ONE TO
00208 10FB 8B01         ADD     A       #01H    ;HOURS.
00209 10FD 19           DAA                     ;BCD RESULT.
00210 10FE 8124         CMP     A       #24H    ;MIDNIGHT?
00211 1100 2703         BEQ             MIDNT   ;IF YES, SET HRS= 00.
00212 1102 970C         STA     A       OCH     ;IF NO, STORE RESULT AND
00213 1104 39           RTS                     ;GO BACK.
00214 1105 4F     MIDNT CLR     A               ;CLEAR HOURS SINCE
00215 1106 970C         STA     A       OCH     ;IT IS MIDNIGHT.
00216 1108 39           RTS                     ;GO BACK.
00217                   ;*****************************************************************
00218                   ;THIS ROUTINE SENDS THE NUMBER OF PULSES NEEDED TO SYNCHRONIZE
00219                   ;THE SCHOOL CLOCKS TO EITHER WWV OR THE REAL-TIME CLOCK.
00220                   ;IF THE NUMBER OF PULSES IS > 682 (11 HRS WORTH), THEN IT WILL
00221                   ;JUST WAIT FOR THE SCHOOL CLOCKS TO CATCH UP.  IF THE SCHOOL
00222                   ;CLOCK MINUTES ARE = 59, A SWITCH AT 5000H IS OPENED AND
00223                   ;CLOSED 10 TIMES TO SYNCHRONIZE ALL CLOCKS.  IF THE SCHOOL
00224                   ;CLOCK MINUTES ARE = 00-49, A SWITCH AT 7000H IS CLOSED.
00225                   ;*****************************************************************
```

```
00226 1109 9616        PULSER LDA     A       16H     ;NUMBER OF HOURS DIFFERENCE.
00227 110B 2727               BEQ             PLSMIN  ;SKIP HRS PULSES IF =0.
00228 110D 8111               CMP     A       #11H    ;IF HRS DIFF= 11,
00229 110F 2742               BEQ             WAIT    ;THEN WAIT.
00230 1111 C63E        PLSHRS LDA     B       #62     ;# PULSES TO BE SENT.
00231 1113 36          PLSOUT PSH     A               ;SAVE
00232 1114 37                 PSH     B               ;DATA.
00233 1115 B75000             STA     A       5000H   ;SEND OUT A PULSE.
00234 1118 BD119D  >          JSR             SHTWAI  ;WAIT FOR .05 SEC.
00235 111B BD1176  >          JSR             FIFMIN  ;SEE IF SCHOOL CLOCK
00236                                                 ;TIME = 50-58 MINUTES.
00237 111E BD10AD  >          JSR             UPDATE  ;UPDATE DISPLAY.
00238 1121 BD1080  >          JSR             SECDLY  ;WAIT TWO
00239 1124 BD1080  >          JSR             SECDLY  ;SECONDS.
00240 1127 BD1185  >          JSR             CATUP   ;TIME TO CORRECT CLOCKS?
00241 112A 33                 PUL     B               ;RECOVER
00242 112B 32                 PUL     A               ;DATA.
00243 112C 5A                 DEC     B               ;ONE LESS PULSE TO SEND.
00244 112D 26E4               BNE             PLSOUT  ;ALL 62 PULSES SENT ?
00245 112F 8B99               ADD     A       #99H    ;SUBTRACT 1 FROM HOURS.
00246 1131 19                 DAA                     ;BCD RESULT.
00247 1132 26DD               BNE             PLSHRS  ;HOURS CAUGHT UP ?
00248 1134 9615        PLSMIN LDA     A       15H     ;MINUTES DIFFERENCE.
00249 1136 2730               BEQ             ALSENT  ;MINUTES TO BE SENT = 0 ?
00250 1138 36          MINAGN PSH     A               ;SAVE DATA.
00251 1139 B75000             STA     A       5000H   ;SEND A PULSE.
00252 113C BD119D  >          JSR             SHTWAI  ;WAIT FOR .05 SEC.
00253 113F BD1176  >          JSR             FIFMIN  ;SEE IF SCHOOL CLOCK
00254                                                 ;TIME = 50-58 MINUTES.
00255 1142 BD10AD  >          JSR             UPDATE  ;UPDATE DISPLAY.
00256 1145 BD1080  >          JSR             SECDLY  ;WAIT TWO
00257 1148 BD1080  >          JSR             SECDLY  ;SECONDS.
00258 114B BD1185  >          JSR             CATUP   ;TIME TO CORRECT CLOCKS?
00259 114E 32                 PUL     A               ;RECOVER DATA.
00260 114F 4A                 DEC     A               ;ONE LESS PULSE TO SEND.
00261 1150 26E6               BNE             MINAGN  ;ALL PULSES SENT?
00262 1152 39                 RTS                     ;GO BACK.
```

```
00263 1153 863C        WAIT   LDA     A       #60     ;WAIT FOR
00264 1155 9015               SUB     A       15H     ;(60-MINPUL) MIN.
00265 1157 C63C        ANMIN  LDA     B       #60     ;COUNTER, 60 SEC= 1 MIN.
00266 1159 36          PAUSE  PSH     A               ;SAVE
00267 115A 37                 PSH     B               ;DATA.
00268 115B BD1080    >        JSR                     SECDLY  ;WAIT A SECOND.
00269 115E 33                 PUL     B               ;RECOVER
00270 115F 32                 PUL     A               ;DATA.
00271 1160 5A                 DEC     B               ;ONE LESS SECOND TO WAIT.
00272 1161 26F6               BNE                     PAUSE   ;WAITED A MINUTE?
00273 1163 4A                 DEC     A               ;ONE LESS MINUTE TO WAIT.
00274 1164 26F1               BNE                     ANMIN   ;WAITED APPROPRIATE # OF MINUTES?
00275 1166 200D               BRA                     PULSNT  ;GO BACK.
00276 1168 9601        ALSENT LDA     A       01H     ;GET SCHOOL CLOCK MINUTES.
00277 116A B74000             STA     A       4000H   ;DISPLAY MINUTES.
00278 116D 9602               LDA     A       02H     ;GET SCHOOL CLOCK HOURS.
00279 116F B74002             STA     A       4002H   ;DISPLAY HOURS.
00280 1172 BD1080    >        JSR                     SECDLY  ;WAIT A SECOND.
00281 1175 39          PULSNT RTS                     ;GO BACK.
00282                  ;*****************************************************************
00283                  ;THIS ROUTINE DETERMINES IF IT IS NECESSARY TO CLOSE A SWITCH
00284                  ;BEFORE A PULSE IS SENT TO THE SCHOOL CLOCKS.  THE SWITCH WILL
00285                  ;BE CLOSED FROM 00 MINUTES TO 49 MINUTES.
00286                  ;*****************************************************************
00287 1176 9601        FIFMIN LDA     A       01H     ;SCHOOL CLOCK MINUTES.
00288 1178 8159               CMP     A       #59H    ;IF MIN = 59,
00289 117A 2705               BEQ                     CLOSSW  ;THEN CLOSE THE SWITCH.
00290 117C 8B51               ADD     A       #51H    ;SEE IF SCHOOL CLOCK
00291 117E 19                 DAA                     ;MINUTES ARE = 49-58.
00292 117F 2503               BCS                     QED     ;IF THEY ARE, DO NOT CLOSE SWITCH.
00293 1181 B77000      CLOSSW STA     A       7000H   ;CLOSE SWITCH.
00294 1184 39          QED    RTS                     ;GO BACK.
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00295                    ;*****************************************************************
00296                    ;THIS ROUTINE DETERMINES IF THE SCHOOL CLOCKS MINUTES ARE = 59.
00297                    ;IF THEY ARE, THEN 10 PULSES ARE SENT OUT SO THAT THEY MAY ALL
00298                    ;BE SYNCHRONIZED TO ACTUALLY READ 59 MINUTES AFTER THE HOUR.
00299                    ;*****************************************************************
00300 1185 9601         CATUP   LDA     A       01H     ;SCHOOL CLOCK MINUTES.
00301 1187 8159                 CMP     A       #59H    ;TIME TO SYNCHRONIZE
00302 1189 2701                 BEQ             ADVNC   ;SCHOOL CLOCKS?
00303 118B 39                   RTS                     ;IF NOT, GO BACK.
00304 118C 860A         ADVNC   LDA     A       #0AH    ;TEN PULSES TO SEND.
00305 118E B75000       ANOTHR  STA     A       5000H   ;SEND A PULSE.
00306 1191 36                   PSH     A               ;SAVE DATA.
00307 1192 BD1080   >           JSR             SECDLY  ;WAIT TWO
00308 1195 BD1080   >           JSR             SECDLY  ;SECONDS.
00309 1198 32                   PUL     A               ;RECOVER DATA.
00310 1199 4A                   DEC     A               ;ONE LESS PULSE TO SEND.
00311 119A 26F2                 BNE             ANOTHR  ;ALL PULSES SENT?
00312 119C 39                   RTS                     ;IF YES, GO BACK.
00313                    ;*****************************************************************
00314                    ;THIS ROUTINE GIVES A DELAY OF .05 SECOND AND IS USED IMMEDIATELY
00315                    ;BEFORE DETERMINING IF A PULSE NEEDS TO BE SENT TO 7000H.
00316                    ;*****************************************************************
00317 119D CE0C35       SHTWAI  LDX             #3125   ;THIS LOOP
00318 11A0 09           REDUCE  DEX                     ;GIVES A DELAY
00319 11A1 26FD                 BNE             REDUCE  ;OF .05 SEC.
00320 11A3 39                   RTS                     ;GO BACK.
```

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00321                    ;*****************************************************************
00322                    ;THIS IS THE INTERRUPT PROGRAM.  AN INTERRUPT IS GENERATED IF
00323                    ;EITHER THE REAL-TIME CLOCK MINUTES ROLL OVER OR THE WWV DECODER
00324                    ;HAS A NEW FRAME THAT HAS JUST BEEN DECODED.  THIS PROGRAM
00325                    ;DETERMINES WHICH DEVICE GENERATED THE INTERRUPT AND TAKES THE
00326                    ;APPROPRIATE ACTION FOR EACH CASE.  IF THE REAL-TIME CLOCK
00327                    ;GENERATED THE INTERRUPT, THEN THE SCHOOL CLOCKS ARE SIMPLY
00328                    ;ADVANCED BY ONE MINUTE.  IF, ON THE OTHER HAND, THE WWV DECODER
00329                    ;GENERATED THE INTERRUPT, THEN THE DIFFERENCE BETWEEN WWV AND
00330                    ;THE SCHOOL CLOCKS IS COMPUTED AND THE SCHOOL CLOCKS ARE
00331                    ;UPDATED (ASSUMING THE WWV TIME IS DETERMINED TO BE VALID).
00332                    ;*****************************************************************
00333 11A4 B62010       INTRPT LDA     A       2010H   ;CHECK RTC INTERRUPT
00334 11A7 8508                BIT     A       #08H    ;STATUS REGISTER.
00335 11A9 270A                BEQ             WWVINT  ;IF BIT 3 IS NOT SET,
00336                                                  ;WWV GENERATED THE INTERRUPT.
00337 11AB 4F                  CLR     A               ;PREPARE TO
00338 11AC 9716                STA     A       16H     ;SEND ONE
00339 11AE 4C                  INC     A               ;PULSE TO
00340 11AF 9715                STA     A       15H     ;SCHOOL CLOCKS.
00341 11B1 BD1109    >         JSR             PULSER  ;SEND ONE PULSE TO CLOCKS.
00342 11B4 3B                  RTI                     ;GO BACK TO MONITOR PROGRAM.
00343 11B5 DE01        WWVINT  LDX             01H     ;CONVERT SCHOOL
00344 11B7 DF0B                STX             0BH     ;CLOCK TO
00345 11B9 BD1087    >         JSR             HRS12   ;12 HOUR FORMAT
00346 11BC DE13                LDX             13H     ;AND STORE
00347 11BE DF0D                STX             0DH     ;AT 0DH.
00348 11C0 FE3000              LDX             3000H   ;WWV TIME.
00349 11C3 DF0B                STX             0BH     ;PREPARE TO ADD 1 MINUTE.
00350 11C5 DF05                STX             05H     ;WWV TIME LOCATIONS.
00351 11C7 9C07                CPX             07H     ;2 SUCCESSFUL DECODES
00352 11C9 2647                BNE             NOGOOD  ;IN A ROW ?
00353 11CB 9C09                CPX             09H     ;3 SUCCESSFUL DECODES
00354 11CD 2643                BNE             NOGOOD  ;IN A ROW ?
```

```
00355 11CF BD10EA  >          JSR          ADDMIN  ;IF YES, ADD 2 MINUTES
00356 11D2 BD10EA  >          JSR          ADDMIN  ;TO WWV TIME.
00357 11D5 D60C               LDA     B    OCH     ;WWV HOURS (24).
00358 11D7 B66000             LDA     A    6000H   ;EST, DST SWITCH.
00359 11DA 8405               AND     A    #05H    ;MASK ALL BUT D0, D2.
00360 11DC 8B66               ADD     A    #66H    ;    FORM
00361 11DE 43                 COM     A            ;    TENS
00362 11DF 8B01               ADD     A    #01H    ;    COMPLEMENT.
00363 11E1 19                 DAA                  ;BCD RESULT.
00364 11E2 1B                 ABA                  ;WWV HOURS - (4 OR 5).
00365 11E3 19                 DAA                  ;BCD RESULT.
00366 11E4 2503               BCS          WVTIME  ;IF POS RESULT, PROCEED AS NORMAL.
00367 11E6 8B24               ADD     A    #24H    ;ADD 24 TO GET A POSITIVE #.
00368 11E8 19                 DAA                  ;BCD RESULT.
00369 11E9 970C        WVTIME STA     A    OCH     ;24 HOUR WWV LOCAL TIME.
00370 11EB BD1087  >          JSR          HRS12   ;CONVERT TO 12 HR FORMAT.
00371 11EE BD10C3  >          JSR          MINCAL  ;CALCULATE MIN PULSES.
00372 11F1 BD1097  >          JSR          HRSCAL  ;CALCULATE HRS PULSES.
00373 11F4 C63A               LDA     B    #58     ;    **********
00374 11F6 BD1080  > SECAGN   JSR          SECDLY  ;      DELAY OF
00375 11F9 5A                 DEC     B            ;      58 SECONDS.
00376 11FA 26FA               BNE          SECAGN  ;    **********
00377 11FC BD1109  >          JSR          PULSER  ;SEND OUT APPROPRIATE # OF PULSES.
00378 11FF B72015             STA     A    2015H   ;RESET RTC SECONDS.
00379 1202 DE01               LDX          01H     ;PUT SCHOOL CLOCK
00380 1204 FF2003             STX          2003H   ;TIME IN RTC,
00381 1207 DF03               STX          03H     ;RTC IN RAM.
00382 1209 8602               LDA     A    #02H    ;PUT 2 SECONDS INTO REAL-TIME CLOCK TO
00383 120B B72002             STA     A    2002H   ;ACCOUNT FOR THE SECONDS LOST IN PULSER.
00384 120E B62010             LDA     A    2010H   ;MAKE SURE INTERRUPT STATUS
00385                                              ;REGISTER IS CLEARED.
00386 1211 3B                 RTI                  ;GO BACK TO MAIN PROGRAM.
```

```
00387 1212 DE07        NOGOOD LDX             07H      ;ADD 1 MIN TO
00388 1214 DF0B               STX             0BH      ;SECOND MOST RECENT
00389 1216 BD10EA  >          JSR             ADDMIN   ;WWV TIME AND
00390 1219 DE0B               LDX             0BH      ;STORE AT THIRD
00391 121B DF09               STX             09H      ;MOST RECENT LOCATION.
00392 121D DE05               LDX             05H      ;ADD 1 MIN TO
00393 121F DF0B               STX             0BH      ;MOST RECENT WWV
00394 1221 BD10EA  >          JSR             ADDMIN   ;TIME AND STORE AT
00395 1224 DE0B               LDX             0BH      ;SECOND MOST
00396 1226 DF07               STX             07H      ;RECENT LOCATION.
00397 1228 CE30D4             LDX             #12500   ;WAIT UNTIL WWV
00398 122B 09          WWVDLY DEX                      ;INTERRUPT PULSE
00399 122C 26FD               BNE             WWVDLY   ;IS OVER.
00400 122E 3B                 RTI                      ;GO BACK TO MAIN PROGRAM.
00401                         END                      ;END OF CODE
```

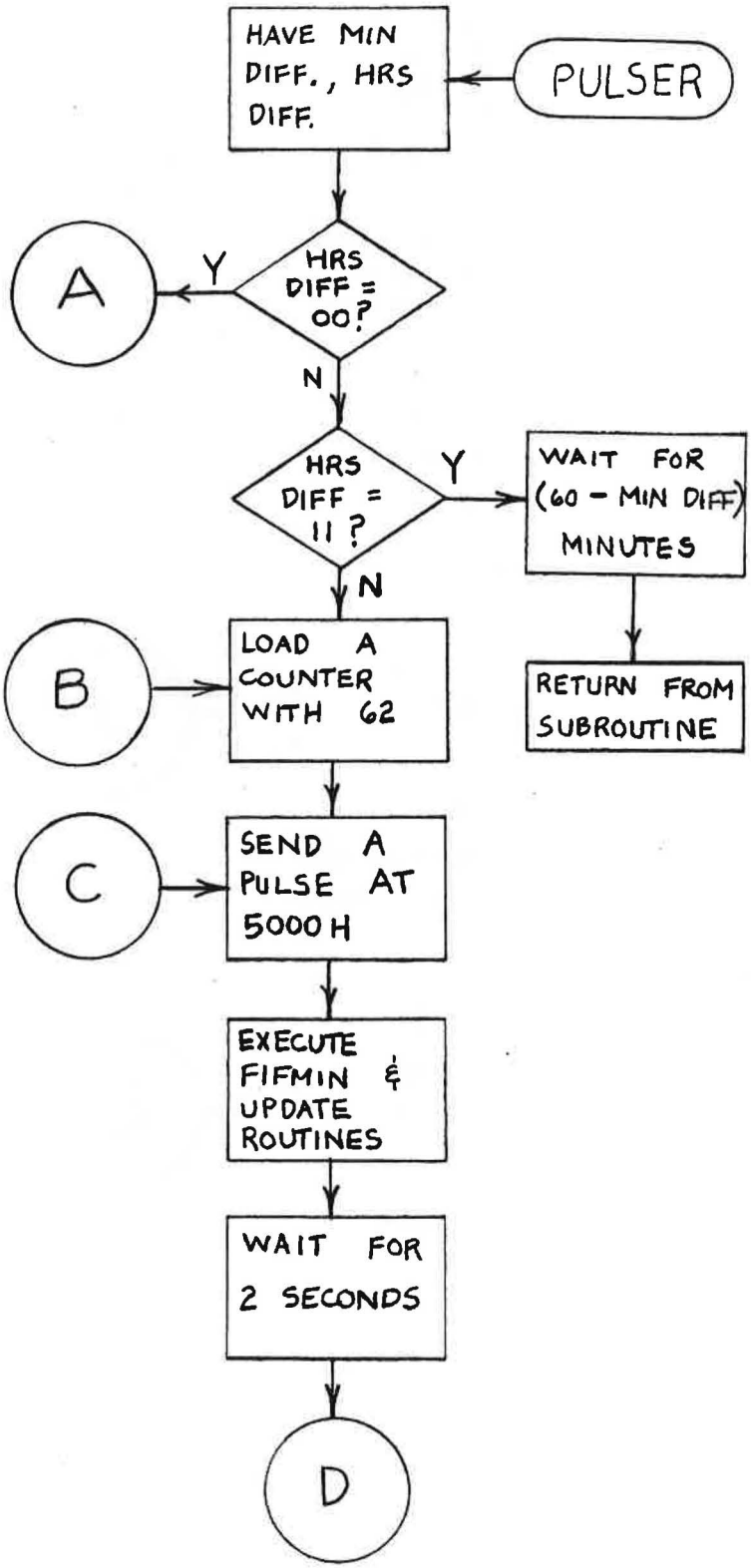
```
Tektronix      M6800 ASM V3.3  Symbol Table

%WWV0 (default) Section (122F)

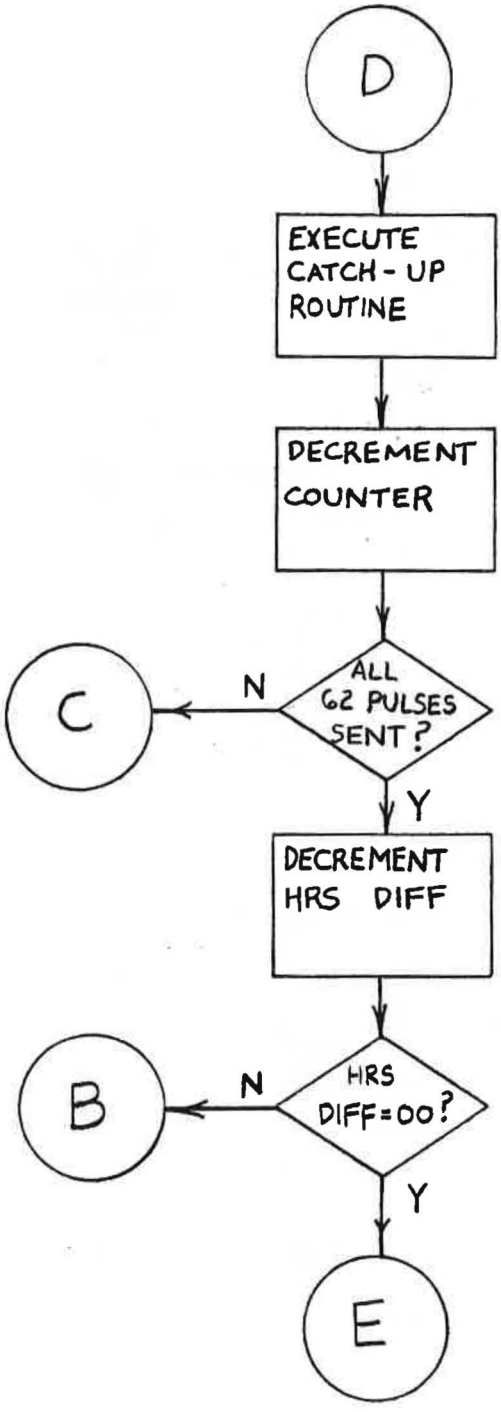
   ADDMIN - 10EA          ADVNC -- 118C          ALSENT - 1168          ANMIN -- 1157          ANOTHR - 118E
   BADRD -- 1052          CATUP -- 1185          CLOSSW - 1181          ENDHR -- 10F6          EOHOUR - 10D4
   FIFMIN - 1176          FINISH - 10E7          GTTH12 - 1090          HRS12 -- 1087          HRSCAL - 1097
   HRSDIF - 10AA          INTRPT - 11A4          LOOP1 -- 1083          MIDNT -- 1105          MINAGN - 1138
   MINCAL - 10C3          MONITR - 107C          NOGOOD - 1212          PAUSE -- 1159          PLSHRS - 1111
   PLSMIN - 1134          PLSOUT - 1113          PULSER - 1109          PULSNT - 1175          QED ---- 1184
   REDUCE - 11A0          RESET -- 1044          SECAGN - 11F6          SECDLY - 1080          SHTWAI - 119D
   UPDATE - 10AD          WAIT --- 1153          WVTIME - 11E9          WWVDLY - 122B          WWVINT - 11B5
   ZERHR -- 10E2          ZERMIN - 10C6

  401 Source Lines      401 Assembled Lines    14077 Bytes available

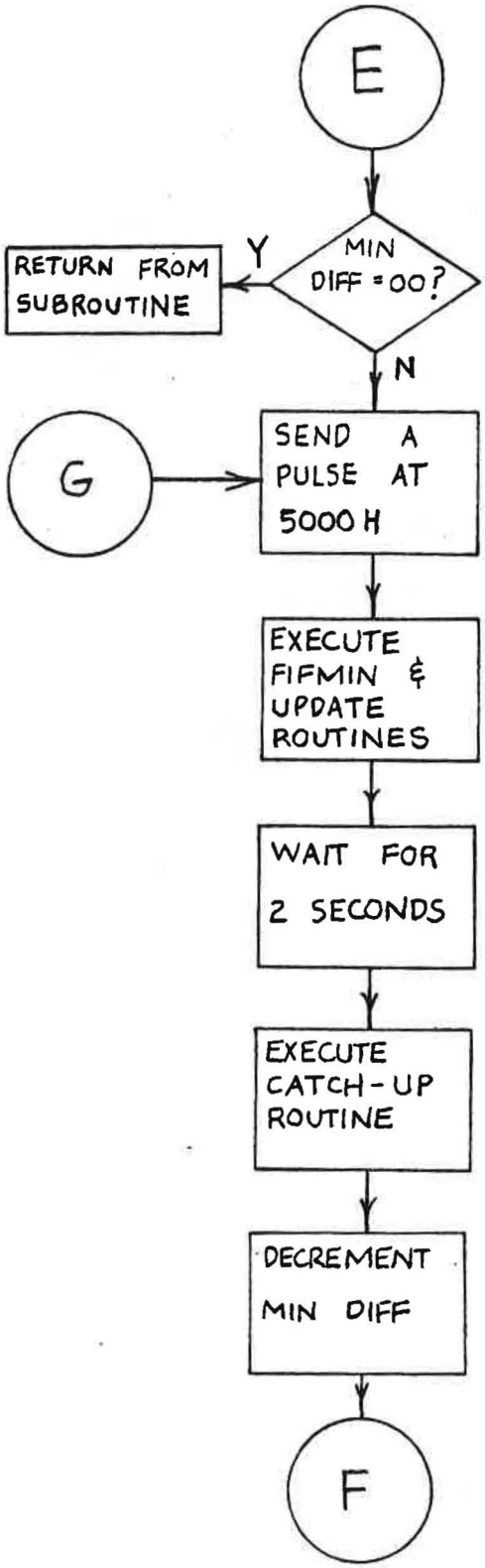
          >>> No assembly errors detected <<<
```



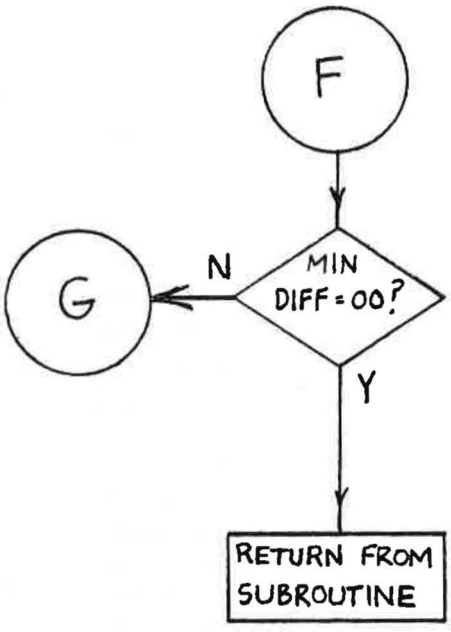
Pulser Routine



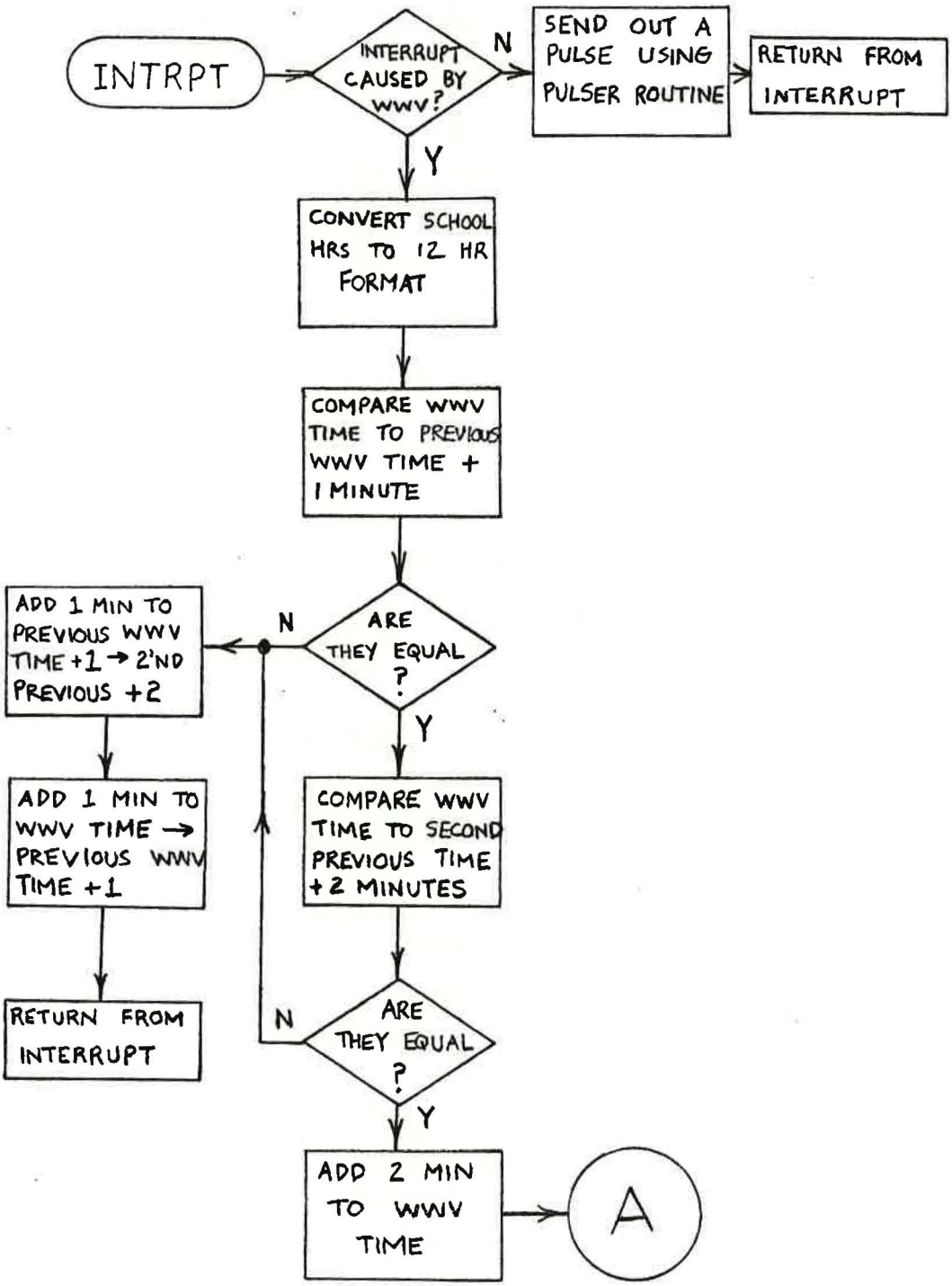
Pulser Routine - Cont.



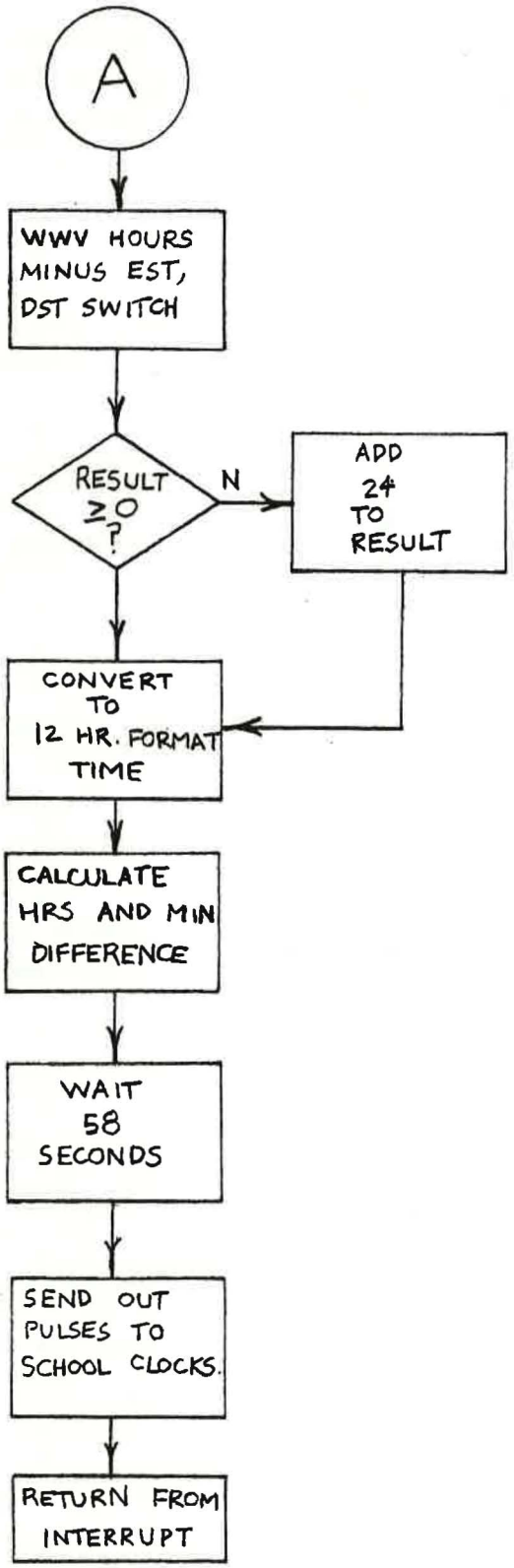
Pulser Routine - Cont.



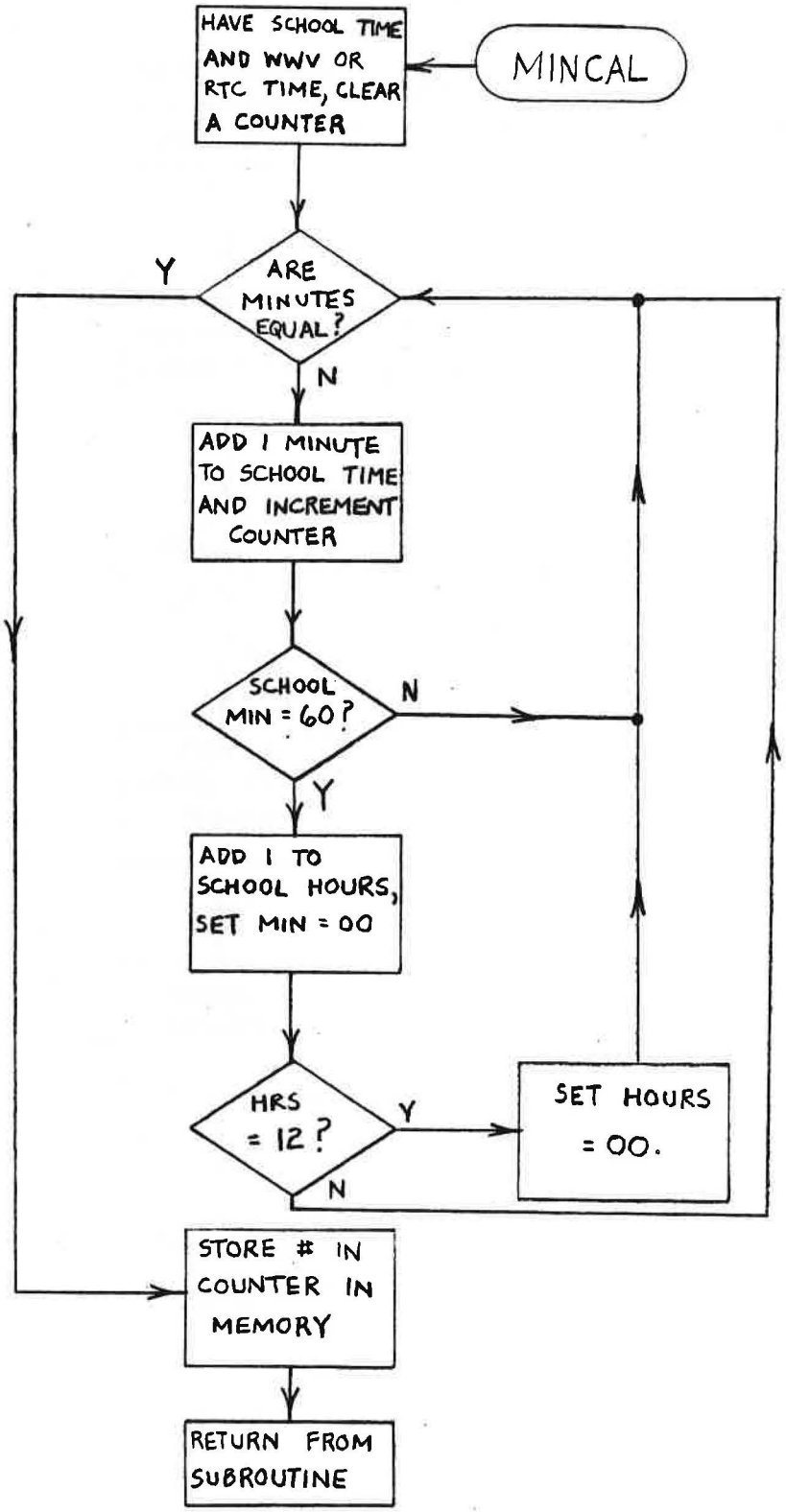
Pulser Routine - Cont.



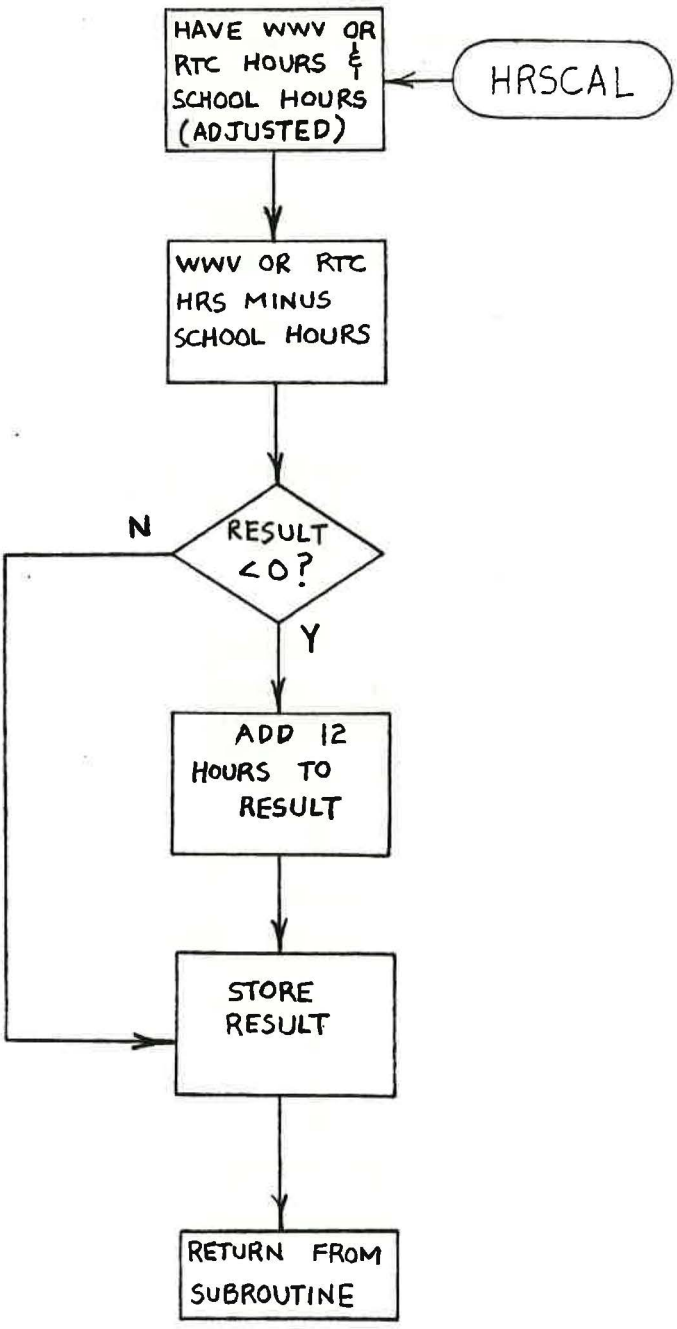
Interrupt Routine



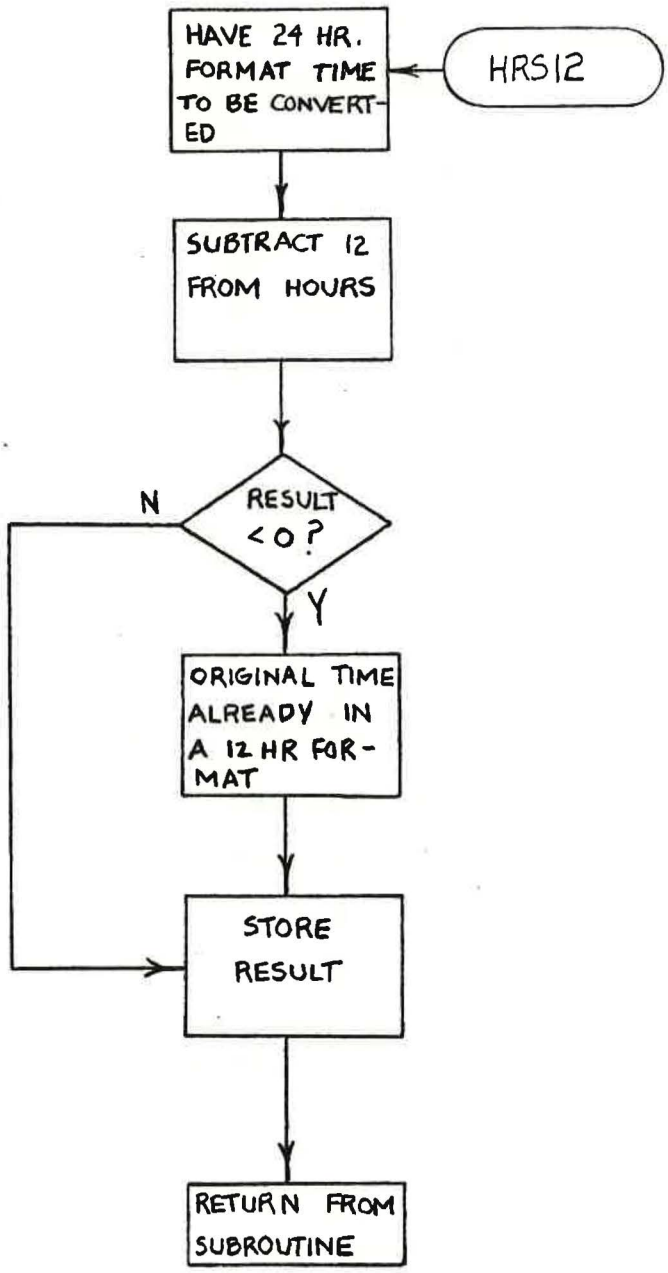
Interrupt Routine - Cont.



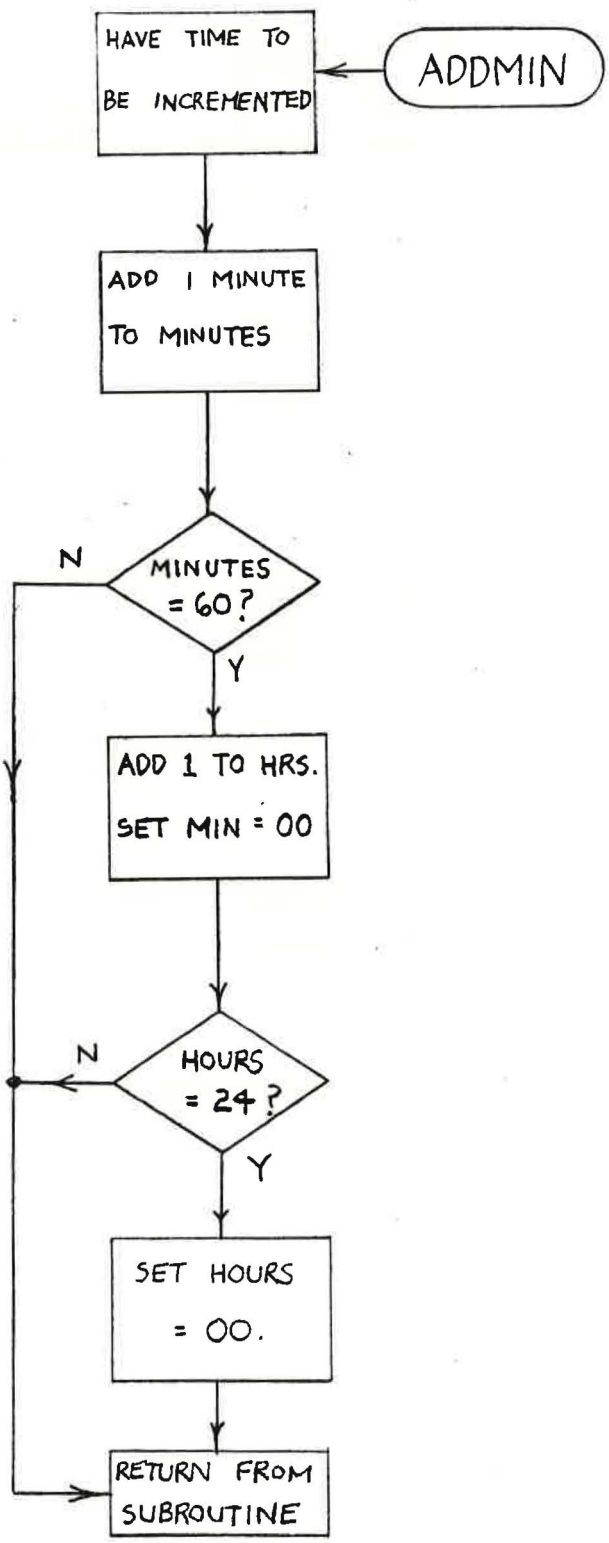
Determine Minutes Difference Routine



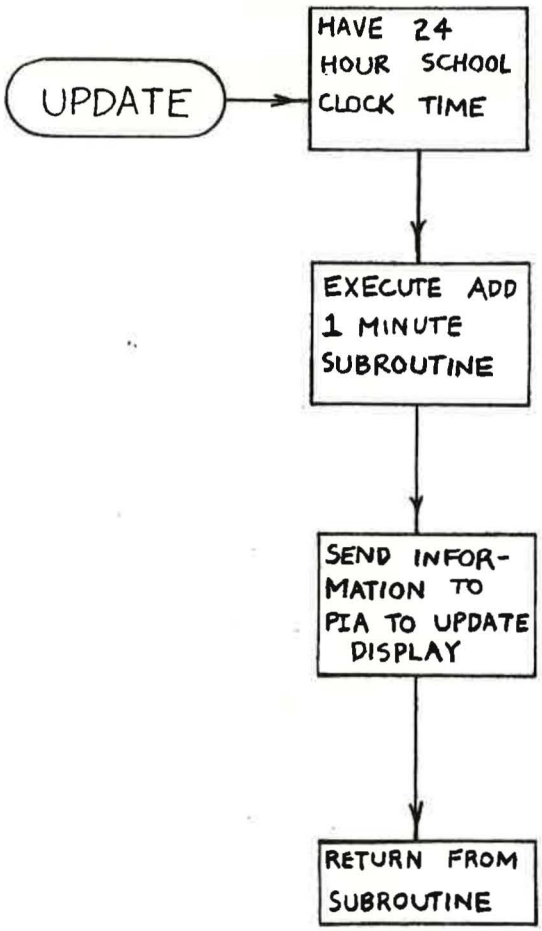
Hours Difference Routine



24 Hr. Format Time to 12 Hr. Format Time Routine



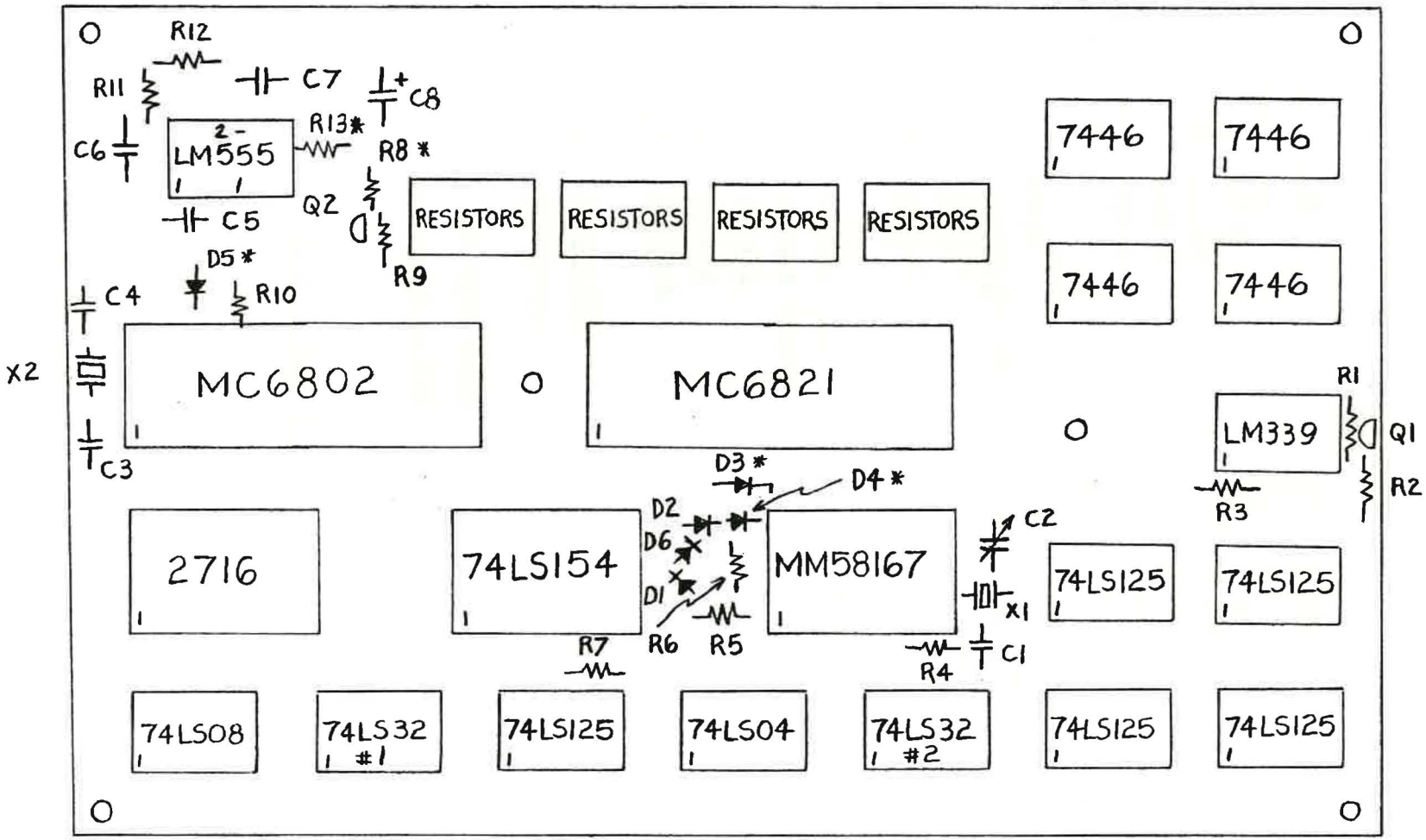
Add One Minute to a 24 Hr. Format Time Routine



Update Display Routine

APPENDIX IV

BOARD LAYOUTS AND PIN DIAGRAMS OF NEW MASTER CLOCK AND WWV DECODER



* - ON BACK SIDE OF BOARD

Board Layout - Master Clock

R1 - 10K
R2 - 1K
R3 - 3.3K
R4 - 200K
R5 - 154K
R6 - 390K
R7 - 3.3K
R8 - 3.3K
R9 - 10K
R10 - 4.7K
R11 - 1M
R12 - 1M
R13 - 1M

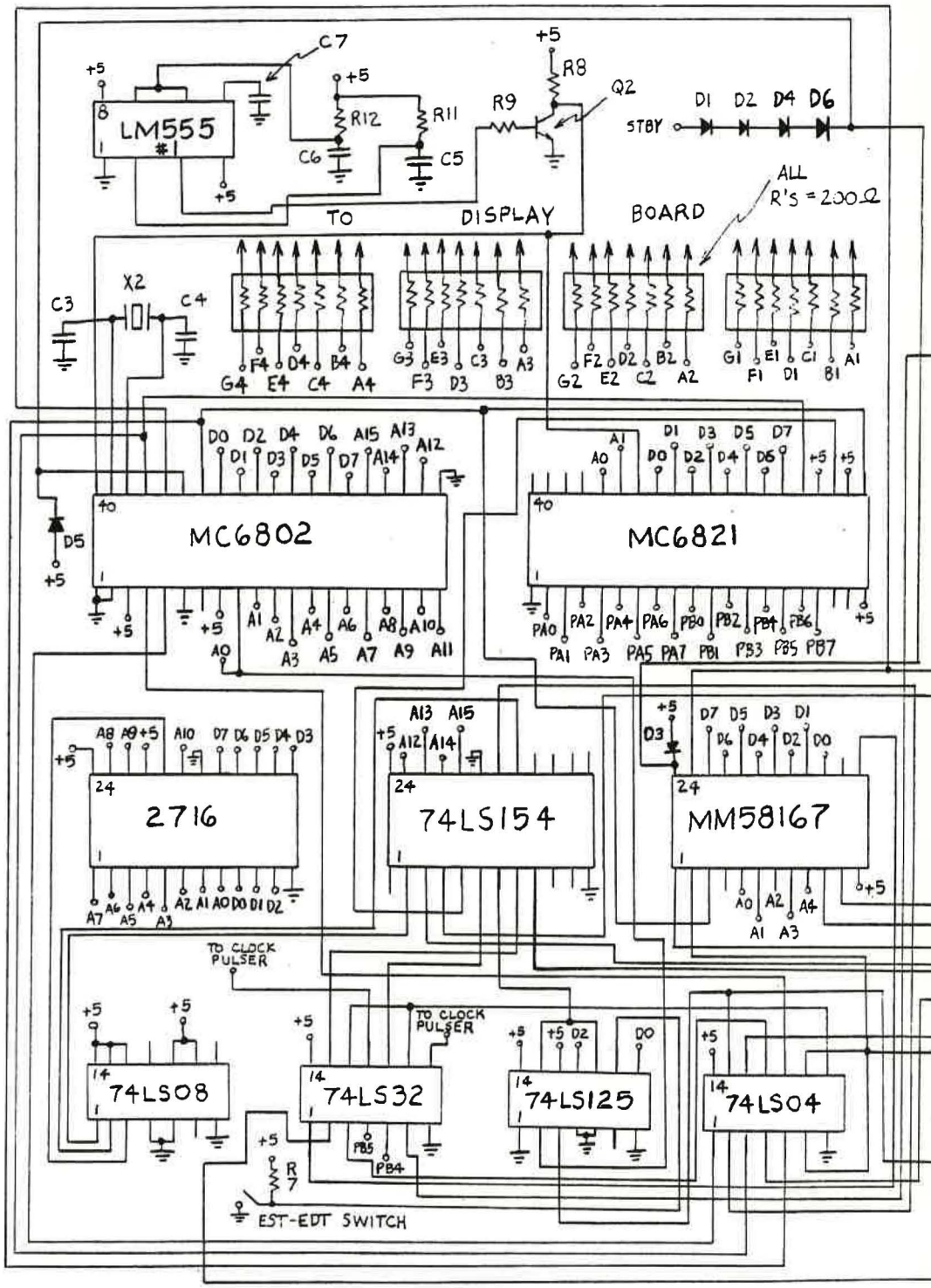
C1 - 20pF
C2 - 9-35pF var.
C3 - 20pF
C4 - 20pF
C5 - .1μF
C6 - .46 μF
C7 - .01μF
C8 - 500 μF

D1 - IN914 (Si)
D2 - IN34A (Ge)
D3 - IN34A
D4 - IN914
D5 - IN34A
D6 - IN914

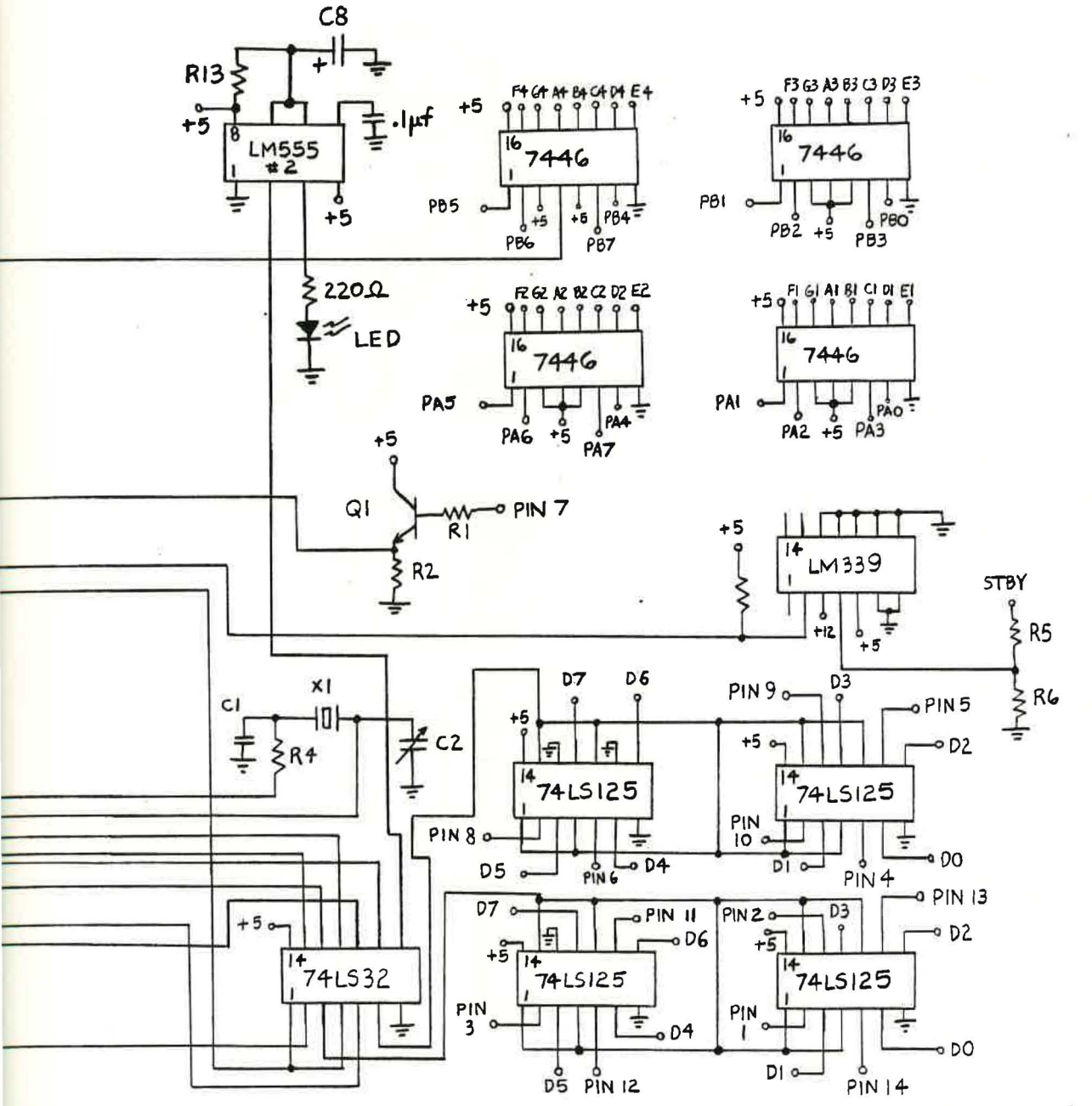
Q1 - 2N2222
Q2 - 2N2222

X1 - 32.768 KHz
X2 - 2.000 MHz

Master Clock Discrete Components

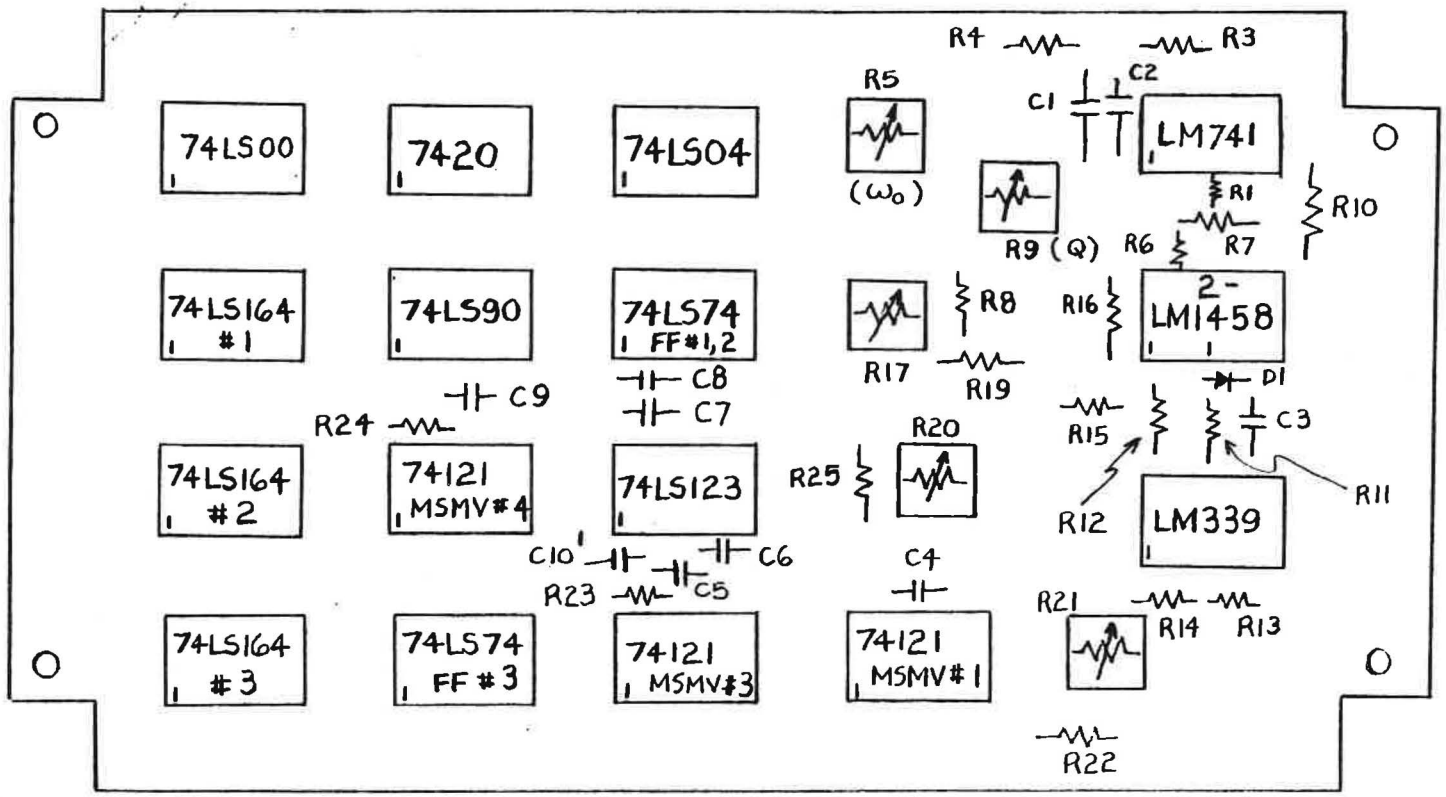


Pin Diagram - Master Clock



PIN "x" REFERS TO PIN #X ON DIP HEADER TO DECODER

Pin Diagram - Master Clock

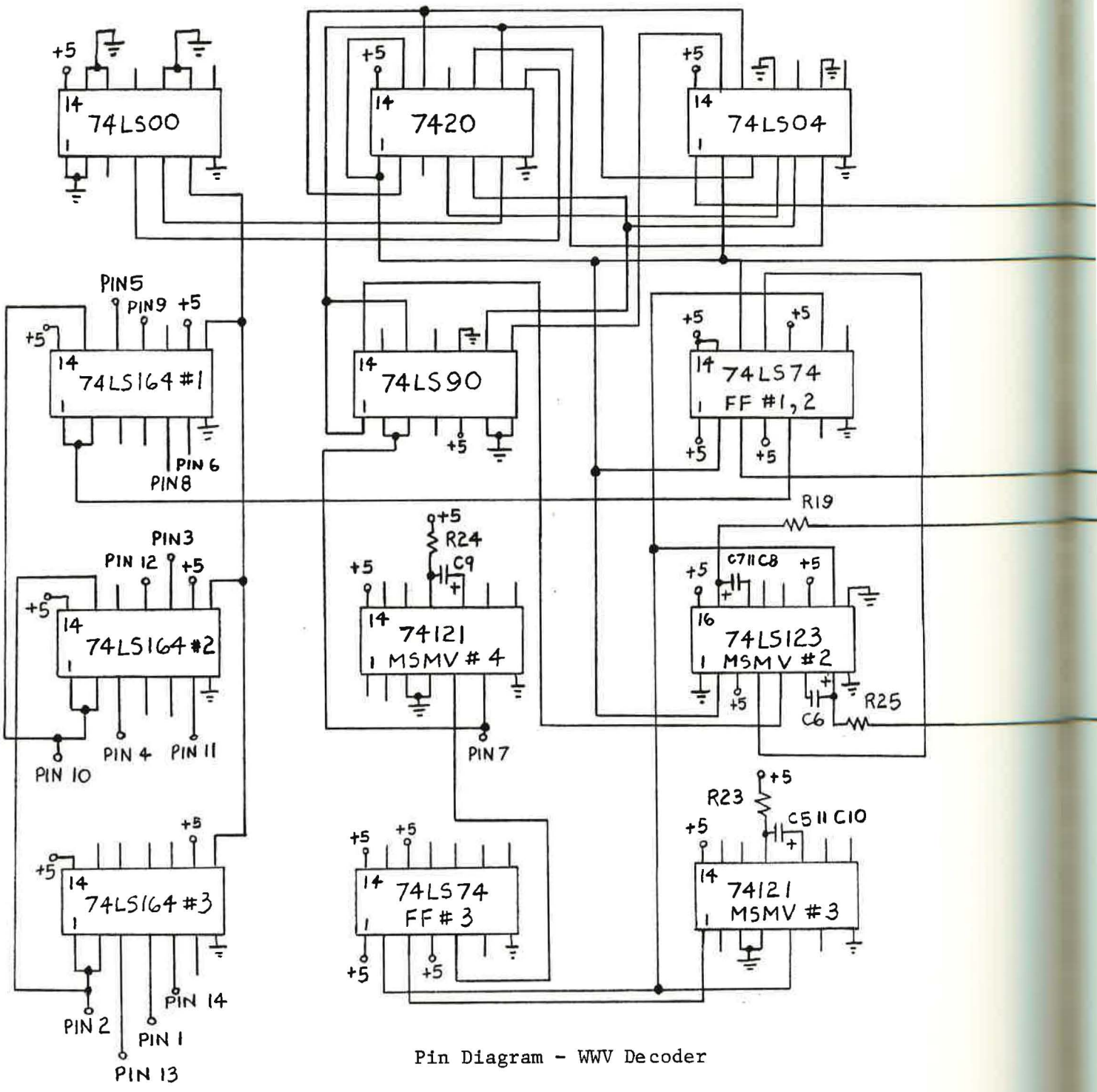


*NOTE - CAPACITORS NOT SHOWN ARE .1μF BYPASS
REFER TO FIGURE 12 OR PIN DIAGRAM FOR COMPONENT VALUES
1 - BACK OF BOARD

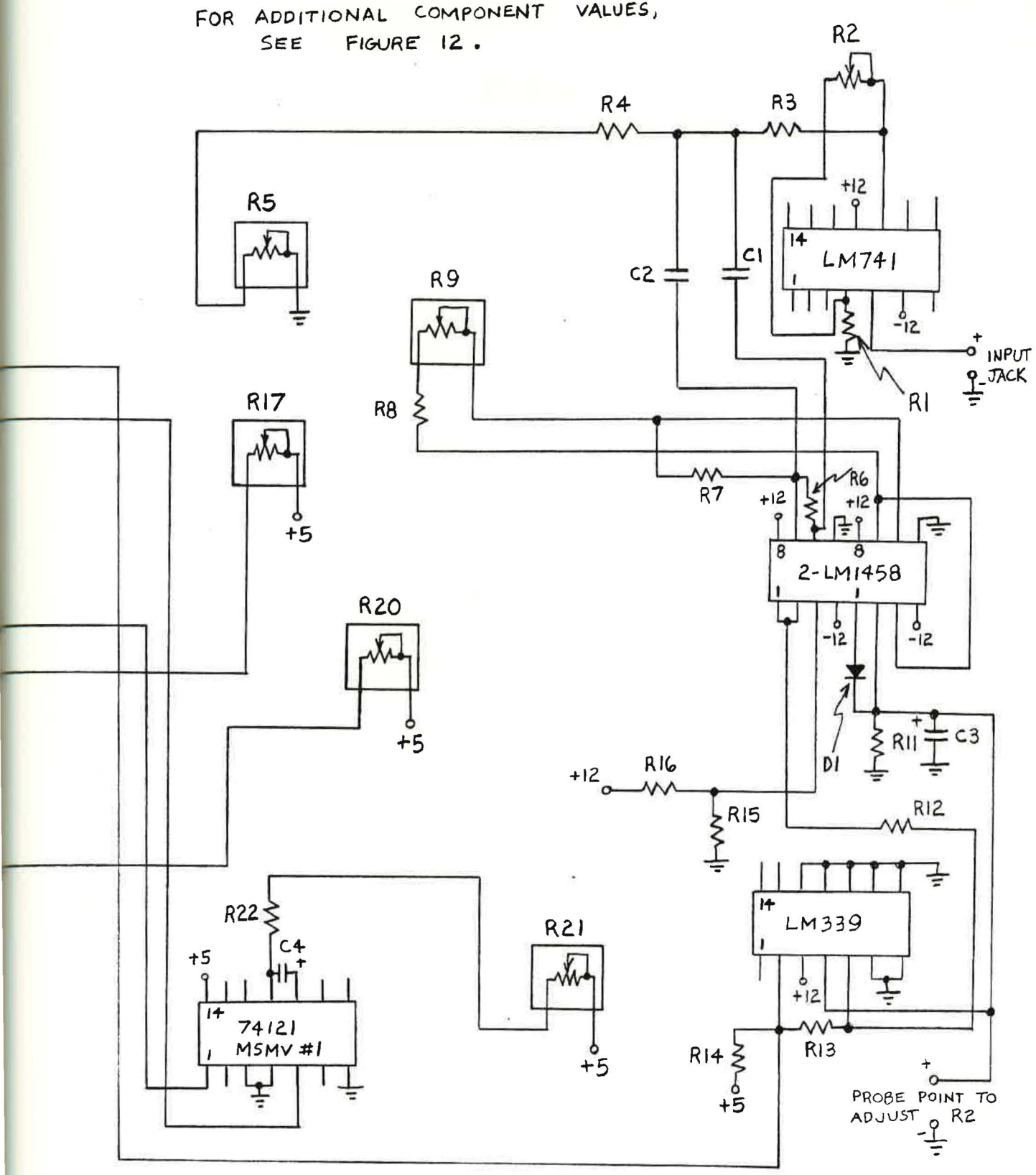
Board Layout - WWV Decoder

R17 - 5K POT	R22 - 30K	C4 - 15 µF	C8 - 22 µF
R19 - 49.7 K	R23 - 27K	C5 - 25 µF	C9 - 4.7 µF
R20 - 5K POT	R24 - 27K	C6 - 15 µF	*C10 - 47 µF
R21 - 5K POT	R25 - 30K	C7 - 15 µF	

* - BACK OF BOARD



Pin Diagram - WWV Decoder

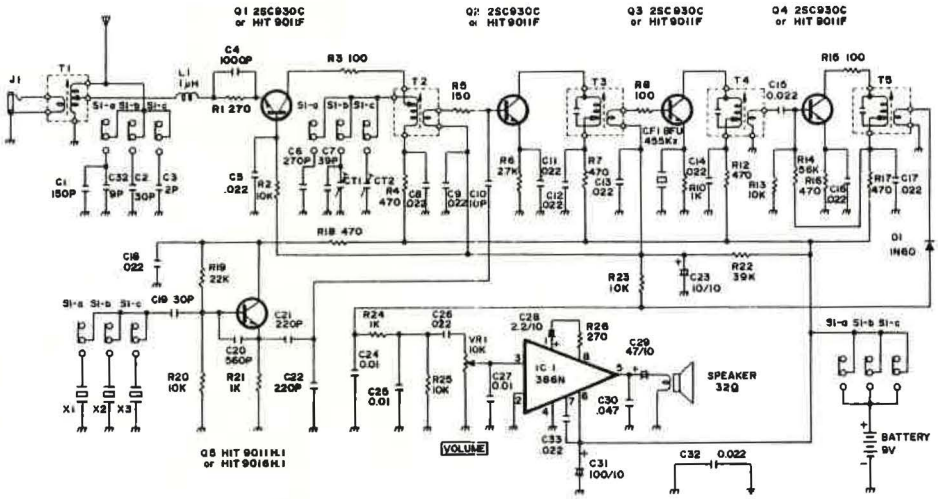


Pin Diagram - WWV Decoder

APPENDIX V

WWV RECEIVER AND POWER SUPPLY SCHEMATICS

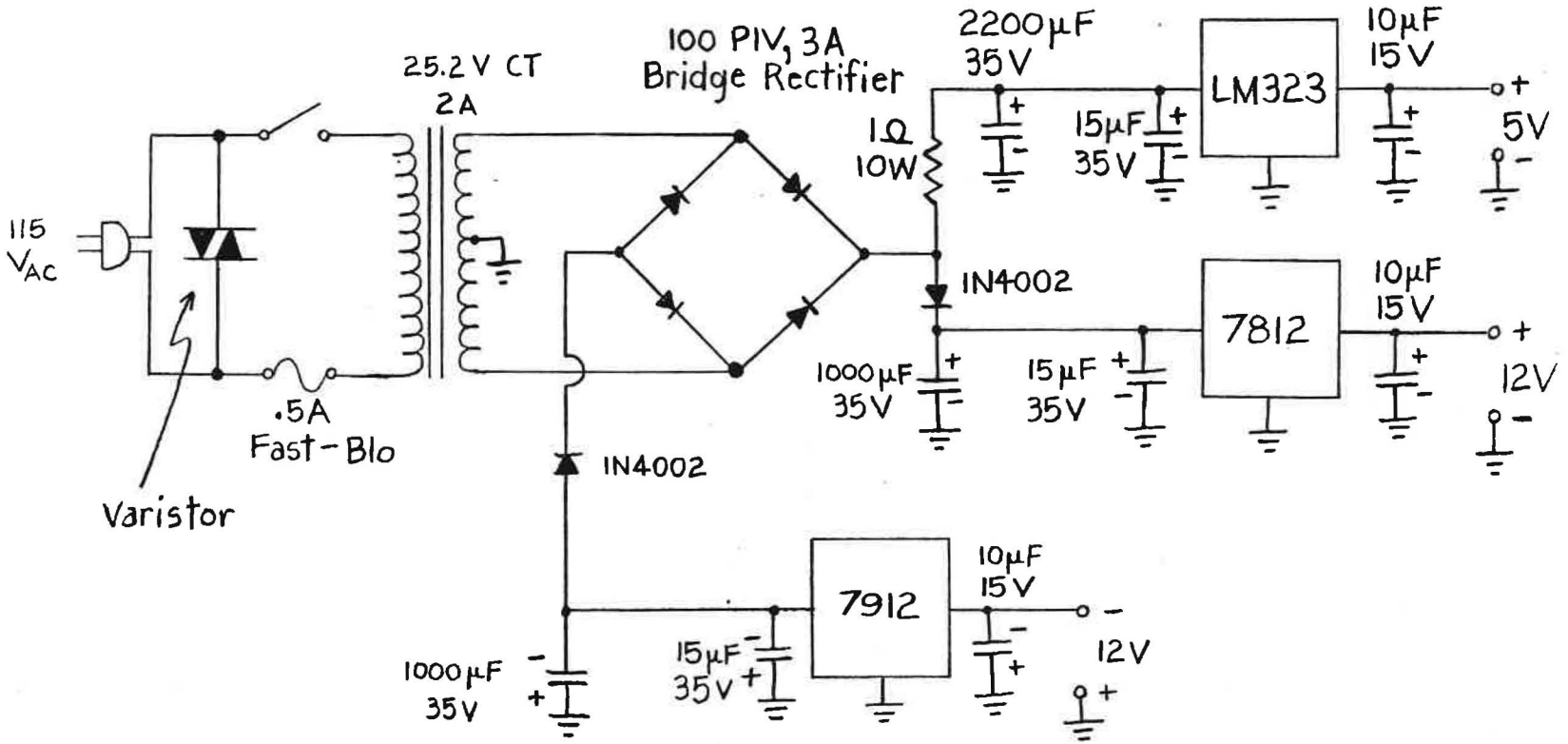
SCHEMATIC DIAGRAM



NOTE (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" (K=10³ OHM)
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10⁶ μF)

Radio Shack WWV Receiver Cat. No. 12-159A

Source : Owner's Manual



Power Supply Schematic

APPENDIX VI

MASTER CLOCK, WWV DECODER, AND POWER SUPPLY ITEMIZED COSTS

TABLE II

MASTER CLOCK PRICE LIST

QUANTITY	DESCRIPTION	UNIT PRICE	AMOUNT
1	MC6802 Microprocessor	$7.95	$ 7.95
1	MC6821 PIA	$4.95	$ 4.95
1	2716 EPROM	$5.95	$ 5.95
1	MM58167 Clock	$8.95	$ 8.95
1	74LS154 TTL IC	$ .99	$ .99
1	SCS11C3 Optoisolator	$1.19	$ 1.19
1	M0C3010 Optoisolator	$1.25	$ 1.25
3	LM555 Timer	$ .39	$ 1.17
1	2.0 MHz Crystal	$5.95	$ 5.95
1	32.768 KHz Crystal	$3.95	$ 3.95
5	74LS125 TTL IC	$ .49	$ 2.45
4	7446 TTL IC	$ .79	$ 3.16
2	74LS32 TTL IC	$ .35	$ .70
1	74LS08 TTL IC	$ .29	$ .29
1	74LS04 TTL IC	$ .29	$ .29
1	LM339 Comparator	$ .69	$ .69
4	TIL 321 Display	$ .99	$ 3.96
1	DIP Jumper	$1.65	$ 1.65
2	40 Pin Socket	$ .63	$ 1.26
5	24 Pin Socket	$ .38	$ 1.90
7	16 Pin Socket	$ .30	$ 2.10
10	14 Pin Socket	$ .27	$ 2.70
4	14 Pin Header	$ .72	$ 2.88
1	Triac	$1.49	$ 1.49
1	SCR	$ .99	$ .99
1	Perfboard	$5.14	$ 5.14
20	.1μF Capacitor	$ .12	$ 2.40
1	Project Box	$9.95	$ 9.95
1	Terminal Strip	$1.89	$ 1.89
	Miscellaneous		$10.00
		TOTAL	$98.39

TABLE III

WWV DECODER PRICE LIST

QUANTITY	DESCRIPTION	UNIT PRICE	AMOUNT
3	74121 TTL IC	$ .39	$ 1.17
3	74LS164 TTL IC	$ .45	$ 1.35
2	74LS74 TTL IC	$ .45	$ .90
1	74LS123 TTL IC	$1.25	$ 1.25
1	7420 TTL IC	$ .25	$ .25
1	74LS90 TTL IC	$ .69	$ .69
1	74LS04 TTL IC	$ .29	$ .29
1	74LS00 TTL IC	$ .19	$ .19
1	LM741 Op Amp	$ .35	$ .35
2	LM1458 Op Amp	$ .59	$ 1.08
1	LM339 Comparator	$ .69	$ .69
1	Project Box	$2.99	$ 2.99
2	16 Pin Socket	$ .30	$ .60
15	14 Pin Socket	$ .27	$ 4.05
	Miscellaneous		$ 5.00
		TOTAL	$20.85

TABLE IV

POWER SUPPLY PRICE LIST

QUANTITY	DESCRIPTION	UNIT PRICE	AMOUNT
1	Transformer	$ 6.29	$ 6.29
2	1000μF Capacitor	$ 1.59	$ 3.18
1	2200μF Capacitor	$ 2.49	$ 2.49
1	Switch	$ 1.89	$ 1.89
1	Rectifier	$ 1.59	$ 1.59
1	LM323 Regulator	$ 5.95	$ 5.95
1	7912 Regulator	$ 1.59	$ 1.59
1	7812 Regulator	$ 1.59	$ 1.59
1	Neon Lamp	$ .99	$ .99
1	Battery Holder	$ .89	$ .89
1	Fuse Holder	$ .89	$ .89
5	Binding Post	$ .40	$ 2.00
1	Project Box	$10.95	$10.95
	Miscellaneous		$ 8.00
		TOTAL	$48.29

APPENDIX VII

TROUBLESHOOTING GUIDE

Master Clock

There are no adjustments required on the master clock and, theoretically, it should never require servicing. If something should go wrong, the most likely cause is a "glitch" that has caused the microprocessor in the master clock to get "lost". As a first step, the system should be turned off and the first power-up procedure (see APPENDIX I) should be followed. If the problem persists, a component in the master clock is probably defective (assuming the power supply voltages are correct) and will have to be replaced. Using the materials provided in the APPENDICES of this thesis and the master clock description in the main text, a good technician should be able to isolate the problem.

WWV Decoder

The real-time clock inside the master clock will lose about four seconds per day if it is not updated with WWV time information. At this rate, it would take about two weeks for the school clocks to lose one minute. Ordinarily, the real-time clock will be updated with WWV time information at least once a day. This means that if the school clock time differs from WWV time by more than one minute, something associated with the decoder is either malfunctioning or incorrectly adjusted.

To see if the WWV decoder is interrupting the microprocessor in the master clock, pin 7 on the DIP jumper from the decoder to the master clock should be probed with a logic probe. At one second after the beginning of the

minute, a 0.1 second high pulse should appear on pin 7. If this is not the case over a period of several minutes, the decoder is not transferring any information to the master clock. The most likely reason for this is an incorrectly adjusted "gain control" knob on the decoder (see APPENDIX I), a detuned receiver, or an inadequate signal from WWV due to unfavorable atmospheric conditions. If a clear, non-fading signal is heard at the speaker (remember that the volume control on the receiver can be turned without affecting the decoder) and the "gain control" knob is properly adjusted, but no interrupt occurs, then something in the decoder is either incorrectly adjusted or defective. As with the master clock, the APPENDIX materials and the description of decoder operation in the main text should allow a good technician to isolate the problem.

VITA

John E. Pfeifer, Jr., was born on May 29, 1959, in Louisville, Kentucky to John E., Sr., and Mary Margaret Pfeifer. He graduated from Saint Xavier High School in May 1977, and entered the University of Louisville in the fall of 1977. He received the Bachelor of Science degree from the Speed Scientific School, University of Louisville, in December, 1980. He received the Master of Engineering degree with Specialization in Electrical Engineering, from the Speed Scientific School, University of Louisville, in May, 1983.