A Generic Theory for Design of Efficient Three-stage Doherty Power Amplifiers

A Generic Theory for Design of Efficient Three-stage Doherty Power Amplifiers

Han Zhou, *Student Member, IEEE*, Jose-Ramon Perez-Cisneros, *Member, IEEE*, Sara Hesami, *Member, IEEE*, Koen Buisman, *Senior Member, IEEE*, Christian Fager, *Senior Member, IEEE*

***Abstract*—An analytical load—pull-based design methodology for three-stage Doherty power amplifiers (PAs) is presented and demonstrated. A compact output combiner network, together with the input phase delays, is derived directly from transistor load—pull data and the design requirements. The technique opens up a new design space for three-stage Doherty PAs with reconfigurable high-efficiency power back-off levels. The method is designed to enable high transistor power utilization by maintaining full voltage and current swings of the main and auxiliary amplifier cells. Therefore, a wide efficiency enhancement range can be achieved also with symmetrical devices. As a proof of concept, a 2.14-GHz 30-W three-stage Doherty PA with identical gallium nitride (GaN) HEMT active devices is designed, fabricated, and characterized. The prototype PA is able to linearly reproduce 20-MHz long-term evolution signals with 8.5- and 11.5-dB peak-to-average power-ratio (PAPR), providing average efficiencies of 56.6% and 46.8% at an average output power level of 36.8 and 33.8 dBm, respectively. Moreover, an average efficiency as high as 54.5% and an average output power of 36.3 dBm have been measured at an adjacent power leakage ratio of 45.7 dBc for a 100-MHz signal with 8.5 dB of PAPR, after applying digital predistortion linearization.**

***Index Terms*—Combiner synthesis, Doherty power amplifiers (PAs), energy efficiency, gallium nitride (GaN), high peak-to-average power ratio (PAPR), three-stage symmetrical devices.**

I. Introduction

MODERN wireless communication systems require spectrally efficient modulation schemes to obtain high data throughput. This results in signals with large peak-to-average power ratio (PAPR) values, typically in the order of 8-12 dB. Therefore, several power amplifier (PA) architectures have been proposed to improve the PA efficiency at significantly reduced output power (power back-off), including Doherty PA [1], outphasing PA [2], dynamic load modulation [3] and envelope tracking [4]. Among them, the Doherty PA is the most widely used architecture in cellular base stations, thanks to its low complexity, moderate linearity and bandwidth performance.

This research has been carried out in GigaHertz Centre in a joint project financed by the Swedish Government Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, Ericsson, Gotmic, Infineon Technologies Austria, Qamcom, RISE, and SAAB.

H. Zhou, J.-R. Perez-Cisneros, K. Buisman and C. Fager are with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96, Gothenburg, Sweden (e-mail: han.zhou@chalmers.se; jospere@chalmers.se; koen.buisman@chalmers.se; christian.fager@chalmers.se). Koen Buisman is also with the Advanced Technology Institute, University of Surrey, Guildford, UK.

S. Hesami is with Ericsson AB, 164 83, Stockholm, Sweden (e-mail: sara.hesami@ericsson.com)

The Doherty PA provides high efficiency at both maximum and back-off power levels by means of mutual load modulation between two amplifier cells. The standard Doherty PA was initially proposed to enhance the efficiency up to 6-dB output power back-off [5]–[7]. However, the high-efficiency output power back-off range needs to be further extended in order to cope with the modern communication standards with larger PAPR values. Therefore, asymmetrical two-way [8]–[11] and N-way [12] Doherty PAs have been proposed. Nonetheless, the efficiency of these Doherty architectures drops considerably between its high-efficiency back-off and maximum power levels when back-off ranges exceed 6 dB, and thus degrades average efficiency for modern communication signals. Consequently, the three-stage Doherty PA was proposed in [13] to enhance the efficiency at two different output power back-off levels, denoted by γ_{B1} and γ_{B2} henceforth. Fig. 1 shows a comparison of the efficiency versus output power performance of asymmetrical two-way, N-way and three-stage Doherty PAs.

Essentially, two different types of three-stage Doherty PA architectures can be found in the literature [14]. One is referred as the conventional three-stage Doherty PA [15]–[20], which requires amplifier cells with different fundamental current components, i.e., unequal device peripheries. The main drawbacks of this PA architecture are the deep saturation of the main amplifier cell, and the added complexity due to the different device peripheries of all the three amplifier cells. The second type is referred as the modified three-stage Doherty PA. It utilizes a modified output combiner to enhance the efficiency at two fixed output power back-off levels, i.e., at 6-dB and 9.54-dB [21]–[24]. This architecture exhibits two main advantages over the conventional one. First, its main amplifier cell is operating linearly throughout the complete output power range. Second, the fundamental current components for all three amplifier cells are the same at maximum power.

In two-way Doherty PAs, it is well known that the auxiliary amplifier cells, which operate in class-C mode, have a smaller fundamental current component compared to the class-B biased main amplifier cells. This requires larger input power to the auxiliary amplifier cells. Consequently, the use of the same amplifier cells, together with a fixed output combiner network would result in degraded overall power gain and power added efficiency (PAE) performance. For the three-stage Doherty PA, the degradation of the gain and PAE is more significant since its auxiliary amplifiers are biased at even deeper class-C mode to ensure high efficiency at larger power back-off levels. Hence, even for the modified three-stage Doherty PA, its PAE performance is severely affected by the two auxiliary cells

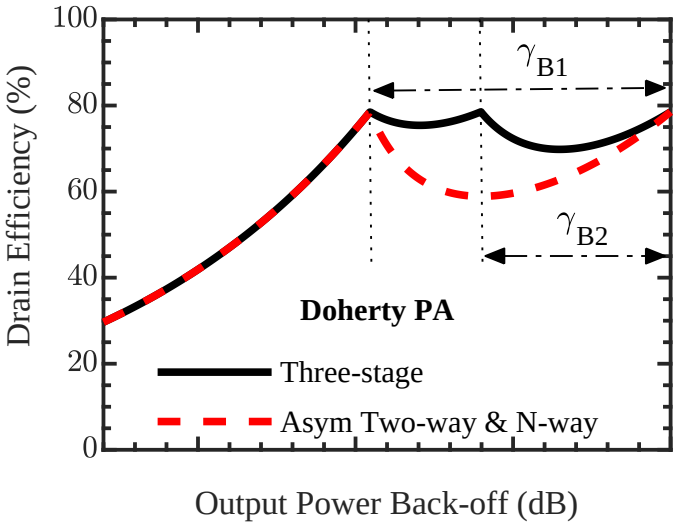

Fig. 1. Drain efficiency versus output power back-off profiles of different Doherty PA architectures: Asymmetrical two-way, N-way and three-stage Doherty PA.

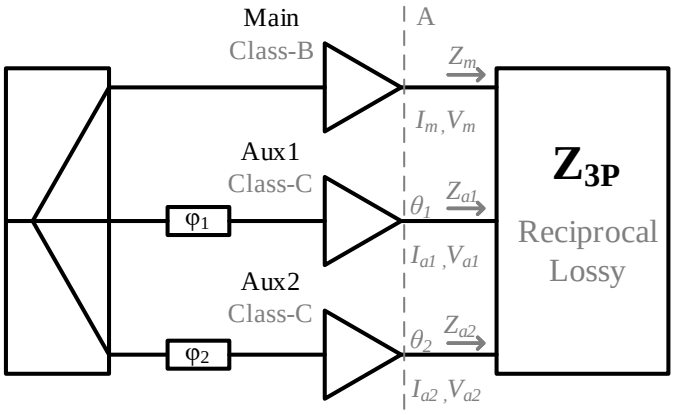

Fig. 2. Generalized reciprocal and lossy three-port combiner used for the analysis of the three-stage Doherty PA. The load is terminated inside. Z_m, Z_{a1} and Z_{a2} denote, the impedances seen by the Main, Aux1 and Aux2 cells, respectively. Plane A represents the output plane of the amplifier cells.

operating in deep class-C mode. In addition, the use of large class-C auxiliary cells demands for non-even input splitter and, therefore, the circuit complexity increases. Moreover, the load modulation networks of the conventional and modified three-stage Doherty PAs use quarter-wavelength ($\lambda/4$) transmission lines (T-lines) as the impedance inverters, which inevitably restricts the design space.

In this paper, we extend the theory from [25], [26] and propose a generic analytical load-pull based design methodology for three-stage Doherty PAs. The theory is applied to maintain high efficiency at two reconfigurable output power back-off levels. The analytical approach solves for the network parameters of the output combiner and the output phase delays in terms of predefined boundary conditions, which comprise transistor loading conditions for high efficiency from large-signal load-pull characterizations. Therefore, the design methodology opens up a new design space, which enables a high power utilization factor and thus enhanced efficiency in three-stage Doherty PAs. In particular, it allows highly efficient three-stage Doherty PAs with identical transistors to be designed and realized. The complete analytical synthesis approach, from load-pull data to the realization of the output combiner, is presented. In order to validate the proposed methodology, a 2.14-GHz gallium nitride (GaN) symmetrical three-stage Doherty PA prototype is designed, implemented and characterized using continuous-wave and modulated signals. The state-of-the-art performance and compact output combiner further indicate its potential in future wireless applications.

The paper is organized as follows. In Section II, the proposed generic analysis of the three-stage Doherty PA is introduced. Furthermore, the analysis and derivation of the output combiner network with ideal current sources are presented. In Section III, the behavior of the symmetrical three-stage Doherty PAs under varies current drive profiles is studied. Section IV describes an analytical approach to directly synthesize the output combiner network from load-pull data of real microwave transistors. Section V covers the generalization and simplification for the circuit realization of the obtained output combiner network. Section VI addresses the practical design procedure by using the proposed design methodology, which is applied on GaN HEMT transistors. For experimental validation, the measurement results of GaN HEMT symmetrical three-stage Doherty PA prototype are given in Section VII. Finally, the main conclusions from this work are presented in Section VIII.

II. Generic Analysis for Three-Stage Doherty PAs

In this section, the operational principles of a generic three-stage Doherty PA are presented. Following the same approach as in [25], the analysis assumes a representation where the load is merged with the combiner into a lossy and reciprocal three-port combiner network, as shown in Fig. 2. The realization of the actual combiner network, for the case of a three-stage Doherty PA, involves a conversion from the lossy three-port network with the load inside, into a lossless four-port combiner network terminated with a purely resistive load.

A. Assumptions and boundary conditions

For simplicity, the following assumptions are adopted in the subsequent theoretical analysis:

1) The transistors are modeled as ideal piece-wise voltage-controlled linear current sources with zero knee voltage.
2) Only the fundamental component is considered, when analyzing the efficiency. All higher harmonic components are short circuited, corresponding to ideal class-B operation.
3) The same drain bias is used for the main and auxiliary cells, and they exhibit same upper drain voltage limit.
4) The input current phase delay between the main (Main) and first auxiliary cell (Aux1) is θ_1 (plane A in Fig. 2). The input current phase delay between the main and second auxiliary cell (Aux2) is θ_2. Meanwhile, the input current phase delay between Main and Aux1 and Aux2 is φ_1 and φ_2, respectively.

Furthermore, the following boundary conditions are used in the derivation to ensure high efficiency at two back-off power levels and that all transistors are fully utilized at maximum output power:

1) Optimal load impedance (the available voltage swing is fully utilized) is presented to the class-B biased Main amplifier cell at the maximum power and the two desired back-off power levels.
2) Optimal load impedance is presented to the class-C biased Aux1 amplifier cell at maximum power and at the second desired back-off power level.
3) Optimal load impedance is presented to the class-C biased Aux2 amplifier cell at the maximum power levels.

B. Three-port combiner network parameters

The assumptions and boundary conditions presented above, together with the ideal voltage-controlled current source models of the transistors will now be used to derive the impedance parameters of the combiner.

The impedance parameters of the lossy and reciprocal three-port output combiner, $\mathbf{Z_{3P}}$, are derived using the ideal current source models. Later, in section IV, the combiner parameters will be obtained by load-pull data from real microwave transistors. The voltages and currents shown in Fig. 2 are related through $\mathbf{Z_{3P}}$,

$$\begin{bmatrix} V_m \\ V_{a1} \\ V_{a2} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{12} & Z_{22} & Z_{23} \\ Z_{13} & Z_{23} & Z_{33} \end{bmatrix} \begin{bmatrix} I_m \\ I_{a1} \\ I_{a2} \end{bmatrix}. \tag{1}$$

where that $Z_{12} = Z_{21}$, $Z_{13} = Z_{31}$ and $Z_{23} = Z_{32}$ since the network is assumed to be reciprocal. The impedance parameters of the lossy and reciprocal three-port combiner from (1) can be derived from the the output optimal impedance and the current ratios (α) of main and two auxiliary cells at maximum and two back-off levels. Note that the output current phase relationship between the Main and Aux1 and Aux2 is θ_1 and θ_2, respectively.

At maximum drive level (subscript M):

$$Z_{m,M} = Z_{11} + Z_{12}\alpha_{1,M} + Z_{13}\alpha_{2,M} \tag{2a}$$
$$Z_{a1,M} = Z_{12}/\alpha_{1,M} + Z_{22} + Z_{23}\alpha_{2,M}/\alpha_{1,M} \tag{2b}$$
$$Z_{a2,M} = Z_{13}/\alpha_{2,M} + Z_{23}\alpha_{1,M}/\alpha_{2,M} + Z_{33} \tag{2c}$$

At the second back-off drive level (subscript $B2$):

$$Z_{m,B2} = Z_{11} + Z_{12}\alpha_{1,B2} + Z_{13}\alpha_{2,B2} \tag{3a}$$
$$Z_{a1,B2} = Z_{12}/\alpha_{1,B2} + Z_{22} + Z_{23}\alpha_{2,B2}/\alpha_{1,B2} \tag{3b}$$
$$Z_{a2,B2} = Z_{13}/\alpha_{2,B2} + Z_{23}\alpha_{1,B2}/\alpha_{2,B2} + Z_{33} \tag{3c}$$

At the first back-off drive level (subscript $B1$):

$$Z_{m,B1} = Z_{11} + Z_{12}\alpha_{1,B1} + Z_{13}\alpha_{2,B1} \tag{4a}$$
$$Z_{a1,B1} = Z_{12}/\alpha_{1,B1} + Z_{22} + Z_{23}\alpha_{2,B1}/\alpha_{1,B1} \tag{4b}$$
$$Z_{a2,B1} = Z_{13}/\alpha_{2,B1} + Z_{23}\alpha_{1,B1}/\alpha_{2,B1} + Z_{33} \tag{4c}$$

where

$$\alpha_{1,B2} = \frac{i_{a1,B2}}{i_{m,B2}} \cdot e^{-j\theta_1}$$
$$\alpha_{1,M} = \frac{i_{a1,M}}{i_{m,M}} \cdot e^{-j\theta_1}$$
$$\alpha_{2,M} = \frac{i_{a2,M}}{i_{m,M}} \cdot e^{-j\theta_2}$$

where the first subscript index of the optimal impedances (Z) and current ratios (α), m, $a1$ and $a2$, corresponds to Main, Aux1, and Aux2 cells, respectively. Similarly, the second subscript index, M, $B1$, and $B2$, represents the maximum, first and second back-off drive levels, respectively.

It should be stressed that at the first back-off level, the output impedances of the Aux1 and Aux2 cells are open-circuit for the ideal current source operation. Similarly, at the second back-off level, Aux2 cell is off. Therefore, only six of the above complex equations, (2), (3a), (3b) and (4a), are valid. As there are six unknown parameters in the impedance matrix, $\mathbf{Z_{3P}}$ can be solved uniquely. Moreover, the value of the current ratios at the first back-off level ($\alpha_{1,B1}$ and $\alpha_{2,B1}$) and the current ratio at the second back-off level ($\alpha_{2,B2}$) is assumed to be zero, because the Aux1 and Aux2 cells are turned off there. This helps to reduce the complexity of the system of equations presented above. The solution set is thus given by

$$\begin{cases} Z_{11} = Z_{m,B1} \\ Z_{12} = \dfrac{Z_{m,B2} - Z_{m,B1}}{\alpha_{1,B2}} \\ Z_{22} = \dfrac{Z_{a1,B2}\alpha_{1,B2}{}^2 - (Z_{m,B2} - Z_{m,B1})}{\alpha_{1,B2}{}^2} \\ Z_{13} = \dfrac{(Z_{m,M} - Z_{m,B1})\,\alpha_{1,B2} - (Z_{m,B2} - Z_{m,B1})\,\alpha_{1,M}}{\alpha_{2,M}\alpha_{1,B2}} \\ Z_{23} = \dfrac{(Z_{m,B1} - Z_{m,B2})\,(\alpha_{1,B2} - \alpha_{1,M})}{\alpha_{2,M}\alpha_{1,B2}{}^2} \\ \qquad + \dfrac{\alpha_{1,M}\,(Z_{a1,M} - Z_{a1,B2})}{\alpha_{2,M}} \\ Z_{33} = \dfrac{(Z_{a1,B2} - Z_{a1,M})\,\alpha_{1,M}{}^2 - Z_{m,M} + Z_{m,B1}}{\alpha_{2,M}{}^2} \\ \qquad + \dfrac{\left(\alpha_{1,M}{}^2 - 2\,\alpha_{1,M}\alpha_{1,B2}\right)(Z_{m,B1} - Z_{m,B2})}{\alpha_{2,M}{}^2\alpha_{1,B2}{}^2} \\ \qquad + Z_{a2,M}. \end{cases} \tag{5}$$

The solution obtained above shows that the impedance parameters from the lossy three-port combiner are based on the current ratios and optimal impedances of Main, Aux1, and Aux2 transistors. More specifically, the derived impedance parameters depend on $|\alpha_{1,M}|$, $|\alpha_{1,B2}|$ and $|\alpha_{2,M}|$. They also depend on the output current phase delays (θ_1 and θ_2), which will be determined in the following section.

C. Conversion conditions

Now that the lossy three-port impedance parameters, $\mathbf{Z_{3P}}$ are derived, it should be verified that it can be realized with a lossless four-port combiner having one of the ports terminated

with a resistive load. It can be shown that, in order to make this conversion possible, the following conditions are necessary and sufficient [27]:

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\} \tag{6}$$

$$\Re\{Z_{13}\}^2 = \Re\{Z_{11}\}\Re\{Z_{33}\} \tag{7}$$

$$\Re\{Z_{23}\}^2 = \Re\{Z_{22}\}\Re\{Z_{33}\}. \tag{8}$$

Note that the derived impedance parameters from (5) depend on the three current ratios ($|\alpha_{1,M}|$, $|\alpha_{1,B2}|$ and $|\alpha_{2,M}|$), the two output current phase delays (θ_1 and θ_2) and optimal impedances at desired maximum and back-off power levels. As a result, there are five unknown parameters. Combined with the three boundary conditions (6)-(8) above, the system is under-determined. Two of the unknown parameters can therefore be selected freely.

III. Symmetrical three-stage Doherty PA

The generic theory presented in the previous section, will now be used to study the behavior of the modified three-stage Doherty PA with different current ratios (α_1 and α_2), when enhancing the efficiency at different back-off power levels (γ_{B1} and γ_{B2}). Note that the modified three-stage Doherty PA with different current ratios, using equally sized cells, will be referred as symmetrical three-stage Doherty PA in the subsequent context.

A. Drive profiles and power relations

For simplicity and without affecting the conclusions, the auxiliary cells operating in class-C mode are approximated by ideal voltage-controlled current sources with a piece-wise linear characteristic. The Aux1 and Aux2 amplifiers are turned on when the normalized input voltage drive level (β) exceeds β_{B1} and β_{B2}, respectively.

As shown in Fig. 3, the Main cell fundamental current is defined as

$$I_m = \beta i_{m,M} \tag{9}$$

where $i_{m,M}$ is the maximum current of the main cell.

The fundamental current flowing through the class-C biased Aux1 cell is defined as

$$I_{a1} = \begin{cases} 0, & 0 \le \beta \le \beta_{B1} \\ \left(\dfrac{\beta - \beta_{B1}}{\beta_{B2} - \beta_{B1}}\right) i_{a1,B2} \cdot e^{-j\theta_1}, & \beta_{B1} \le \beta \le \beta_{B2} \\ \left(\dfrac{i_{a1,M} - i_{a1,B2}}{1 - \beta_{B2}}\right) \cdot e^{-j\theta_1}, & \beta_{B2} \le \beta \le 1 \end{cases} \tag{10}$$

where $i_{a1,B2}$ and $i_{a1,M}$ are the magnitude of the current from the Aux1 cell at the second back-off (β_{B2}) and the maximum drive level, respectively. Note that the value of $i_{a1,B2}$ and $i_{a1,M}$ may affect the transconductance of the Aux1 cell.

The fundamental current flowing through the Aux2 cell is expressed as

$$I_{a2} = \begin{cases} 0, & 0 \le \beta \le \beta_{B2} \\ \left(\dfrac{\beta - \beta_{B2}}{1 - \beta_{B2}}\right) i_{a2,M} \cdot e^{-j\theta_2}, & \beta_{B2} \le \beta \le 1 \end{cases} \tag{11}$$

where $i_{a2,M}$ is the magnitude of the current from the Aux2 cell at maximum drive level.

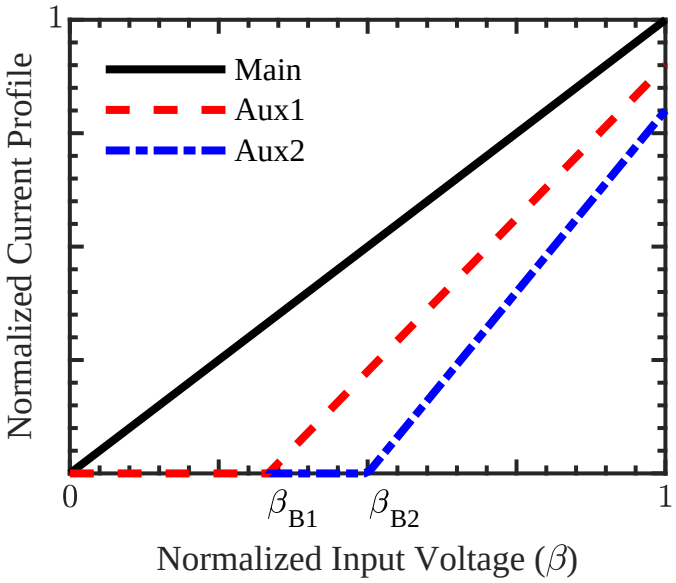

Fig. 3. Current profiles for the Main, Aux1, and Aux2 cells in a symmetrical three-stage Doherty PA. The current profiles are normalized to the peak magnitude of the Main cell current.

In addition, to maximize the overall efficiency of the PA, the voltage of the Main, Aux1 and Aux2 cells at both back-off levels should be equal to the maximum saturated voltage.

Furthermore, it should be noted that when selecting the design parameters γ_{B1} and γ_{B2}, the total output power from the Main, Aux1 and Aux2 cells should be related by

$$\begin{aligned} P_{tot} &= 10^{\frac{\gamma_{B1}}{10}} P_m|_{\beta=\beta_{B1}} \\ &= 10^{\frac{\gamma_{B2}}{10}} (P_m|_{\beta=\beta_{B1}} + P_{a1}|_{\beta=\beta_{B2}}) \end{aligned} \tag{12}$$

where

$$P_{tot} = P_m|_{\beta=1} + P_{a1}|_{\beta=1} + P_{a2}|_{\beta=1}.$$

B. Efficiency reconfigurability

To better demonstrate that the efficiency versus output power profile of the symmetrical three-stage Doherty PA can be reconfigured, three different cases are studied and presented. It is important to mention that the current ratios should be related by (12), to satisfy the law of power conservation, i.e.:

$$\begin{aligned} 1 + |\alpha_{1,M}| + |\alpha_{2,M}| &= 10^{\frac{\gamma_{B1}}{10}} (\beta_{B1}) \\ &= 10^{\frac{\gamma_{B2}}{10}} (\beta_{B2} + |\alpha_{1,B2}|). \end{aligned} \tag{13}$$

Therefore, β_{B1} and β_{B2} can be solved in terms of $|\alpha_{1,B2}|$, once γ_{B1}, γ_{B2}, $|\alpha_{1,M}|$ and $|\alpha_{2,M}|$ are determined. Thus, the three remaining unknowns $|\alpha_{1,B2}|$, θ_1 and θ_2 can be obtained using (6)-(8). Note that it is challenging to derive an analytical solution, but a numerical solution can be obtained using standard optimization techniques.

Table I shows the obtained parameters of three different cases for varying back-off power (γ_B) and current ratios (α). By using the current profiles together with obtained impedance

TABLE I
DIFFERENT THREE-STAGE DOHERTY PA DESIGN CASES

Three-stage Doherty PA	Case 1 Modified	Case 2 Symmetrical	Case 3
γ_{B1} (dB)	9.54	10.5	11
γ_{B2} (dB)	6	5.5	5
$\lvert\alpha_{1,M}\rvert$	1	0.85	0.85
$\lvert\alpha_{2,M}\rvert$	1	0.7	0.7
$\lvert\alpha_{1,B2}\rvert$	0.25	0.31	0.38
θ_1 (deg)	-90	-76.56	-67.61
θ_2 (deg)	0	25.86	31.42

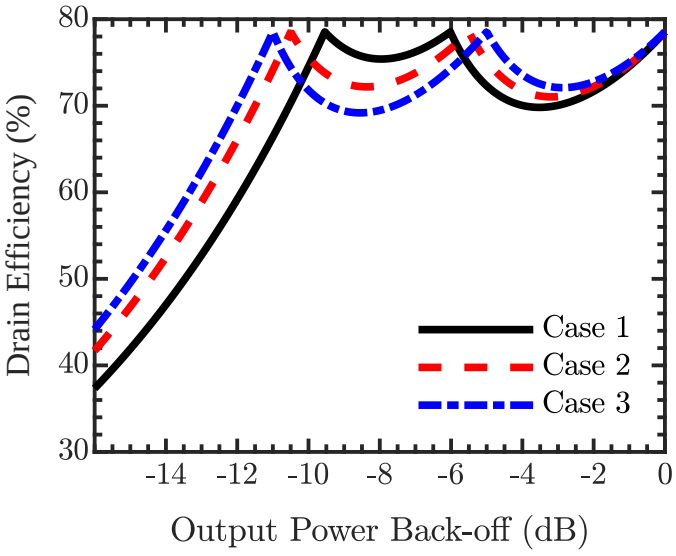

Fig. 4. Efficiency versus output power back-off profiles of the generalized symmetrical three-stage Doherty PA. Three cases with different power back-off levels and current ratios are defined according to Table I.

parameters, the RF output power, DC supply power and efficiency of each amplifier cell can be calculated. Assuming both main and auxiliary amplifier cells with ideal class-B efficiency, the ideal efficiency of the Doherty PA can therefore be obtained [28]. The corresponding efficiency versus output power back-off profiles are presented in Fig. 4.

Case 1 is the modified three-stage Doherty PA, where the design parameters γ_{B1} and γ_{B2} are selected to be 9.54 dB and 6 dB, respectively. The current ratios $\alpha_{1,M}$ and $\alpha_{2,M}$ are assumed to be 1. This case reveals that the modified three-stage Doherty PA is one special case of the proposed theory.

For Case 2 and Case 3, γ_{B1} and γ_{B2} are chosen arbitrarily to demonstrate the back-off efficiency reconfigurability that the theory offers. The current ratios $\alpha_{1,M}$ and $\alpha_{2,M}$ are assumed to be 0.85 and 0.7 to mimic a symmetrical transistor scenario, where smaller fundamental current is presented by equally sized amplifier cells biased in class-C [29].

These results indicate that, based on the proposed method, it is possible to utilize the current ratios ($|\alpha_{1,M}|$ and $|\alpha_{2,M}|$), together with the output current phase delays (θ_1 and θ_2) to design three-stage Doherty PAs with high efficiency at different back-off power levels (γ_{B1} and γ_{B2}). It should be stressed that there is only a finite range of current ratios that gives a physical realization of the phase delays for each power back-off level selection. Since an analytical solution is not available, one has to rely on numerical trials to determine the limitations for a given current ratio.

IV. COMBINER NETWORK PARAMETERS FROM TRANSISTOR LOAD-PULL DATA

The analysis in the previous section assumes ideal current sources. However, in reality, especially at microwave frequencies, the parasitic and non-linear effects of real transistors are significant and their operation deviates greatly from that of ideal current sources. Therefore, to synthesize the combiner network and fully utilize the transistor capabilities, a design approach based on the transistor load-pull data is desired [25].

Similar to the mathematical derivation procedure with ideal current sources, the lossy three-port impedance matrix $\mathbf{Z_{3P}}$ can be derived using the optimal impedances and the current ratios. It should be noted that the fundamental current component can be easily derived, directly from the optimal impedances and output power obtained from the load-pull characterization [30]. The current ratios $\alpha_{1,B2}$, $\alpha_{1,M}$ and $\alpha_{2,M}$ needed in (2)-(4) can then be expressed as

$$\alpha_{1,B2} = \frac{i_{a1,B2}}{i_{m,B2}} e^{-j\theta_1} = \sqrt{\frac{P_{a1,B2}\Re\{Z_{m,B2}\}}{P_{m,B2}\Re\{Z_{a1,B2}\}}} e^{-j\theta_1} \tag{14}$$

$$\alpha_{1,M} = \frac{i_{a1,M}}{i_{m,M}} e^{-j\theta_1} = \sqrt{\frac{P_{a1,M}\Re\{Z_{m,M}\}}{P_{m,M}\Re\{Z_{a1,M}\}}} e^{-j\theta_1} \tag{15}$$

$$\alpha_{2,M} = \frac{i_{a2,M}}{i_{m,M}} e^{-j\theta_2} = \sqrt{\frac{P_{a2,M}\Re\{Z_{m,M}\}}{P_{m,M}\Re\{Z_{a2,M}\}}} e^{-j\theta_2} \tag{16}$$

where the output current phase delay θ_1 is added to $\alpha_{1,M}$ and $\alpha_{1,B2}$, while θ_2 is added to $\alpha_{2,M}$.

The off-state impedances of the Aux1 and Aux2 cells at the back-off power levels, i.e, $Z_{a2,B2}$, $Z_{a1,B1}$ and $Z_{a2,B1}$, are finite for real microwave transistors. The mathematical derivation will therefore be slightly different compared to the ideal operation case introduced previously, where the off-impedance is assumed to be infinite. Therefore, equation (3c), (4b) and (4c) should be employed when introducing the three new variables to the system. First, $\alpha_{1,B1}$ and $\alpha_{2,B1}$ can be derived by (4b) and (4c)

$$\alpha_{1,B1} = \frac{(Z_{a2,B1} - Z_{33})\, Z_{12} + Z_{13}Z_{23}}{(Z_{a2,B1} - Z_{33})\,(Z_{a1,B1} - Z_{22}) - Z_{23}^2} \tag{17}$$

$$\alpha_{2,B1} = \frac{(Z_{a1B1} - Z_{22})\, Z_{13} + Z_{12}Z_{23}}{(Z_{a2B1} - Z_{33})\,(Z_{a1,B1} - Z_{22}) - Z_{23}^2}. \tag{18}$$

Then, from equation (3c), $\alpha_{2,B2}$ can be expressed as

$$\alpha_{2,B2} = \frac{Z_{23}\alpha_{1,B2} + Z_{13}}{Z_{a2,B2} - Z_{33}}. \tag{19}$$

Thus, $\alpha_{1,B1}$, $\alpha_{2,B1}$ and $\alpha_{2,B2}$ can be obtained in terms of the lossy three-port impedance parameters, the three off-state impedances, and $\alpha_{1,B2}$. The lossy three-port impedance parameters can thereafter be solved symbolically, using equations (2), (3a), (3b) and (4a), together with (17)-(19). Consequently, the impedance parameters of the lossy three-port combiner can be expressed in terms of the optimal impedances at maximum

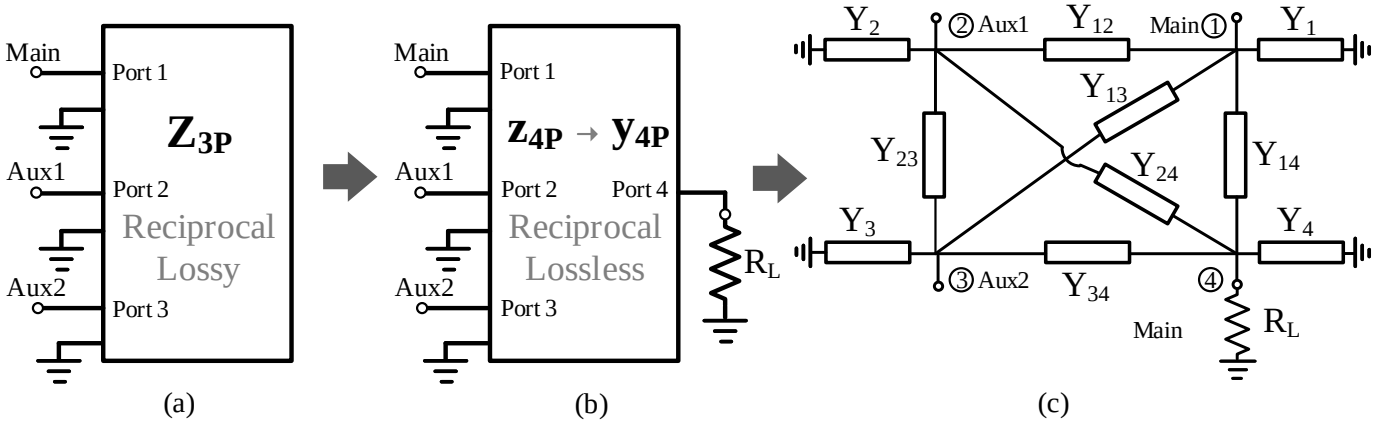

Fig. 5. Step-by-step conversion of the generalized output combiner into a realizable network. First, the lossy and reciprocal three-port output combiner in (a) is converted to a lossless and reciprocal four-port output combiner terminated with a purely resistive load R_L in (b). Then, the obtained four-port impedance parameters are transferred to the four-port admittance parameters, which can be converted into an equivalent network topology in (c).

and two back-off power levels, the off-state impedances, the three current ratios $|\alpha_{1,M}|$, $|\alpha_{2,M}|$ and $|\alpha_{1,B2}|$, as well as the Aux1 and Aux2 output current phase delays θ_1 and θ_2. Finally, the lossy three-port impedance parameters can be determined by solving the three boundary conditions (6)-(8). As discussed previously, a numerical solution technique has been used to determine the phase delays that satisfy the boundary conditions.

Moreover, it should be stressed that the parasitic and nonlinear effects shift the current phase from the input to the output current in realistic transistors. This phase shift depends on bias, transistor size, harmonic termination and matching networks. The physical input phase delays φ_1 and φ_2 should therefore be adjusted to compensate for these effects and to ensure that the desired output phase delays θ_1 and θ_2 are achieved at the interface to the output combiner:

$$\varphi_1 = \theta_1 - \varphi_{a1,B2} + \varphi_{m,B2} \tag{20}$$

$$\varphi_2 = \theta_2 - \varphi_{a2,M} + \varphi_{m,M}. \tag{21}$$

where φ_m, φ_{a1} and φ_{a2} represent the input-to-output phase shifts introduced by the Main, Aux1 and Aux2 transistors, respectively.

V. Realization of Lossless Four-port Combiner

Now that the lossy and reciprocal three-port impedance parameters are determined, the next step is to convert it to the lossless and reciprocal four-port network ($\mathbf{z_{4P}}$), terminated with a purely resistive load R_L. Assuming that the output port 4, is terminated with load R_L, the four-port impedance parameters (denoted by z_{ij}) can be derived in terms of the three-port impedance parameters (denoted by Z_{ij}) [27]:

$$\begin{aligned} z_{14} &= \pm j\sqrt{\Re(Z_{11})/C} \\ z_{24} &= \pm j\sqrt{\Re(Z_{22})/C} \\ z_{34} &= \pm j\sqrt{\Re(Z_{33})/C} \end{aligned} \tag{22}$$

$$\begin{aligned} z_{11} &= Z_{11} + \frac{z_{14}^2}{z_{44}+R_L} & z_{12} &= Z_{12} + \frac{z_{14}z_{24}}{z_{44}+R_L} \\ z_{22} &= Z_{22} + \frac{z_{24}^2}{z_{44}+R_L} & z_{13} &= Z_{13} + \frac{z_{24}z_{34}}{z_{44}+R_L} \\ z_{33} &= Z_{33} + \frac{z_{34}^2}{z_{44}+R_L} & z_{23} &= Z_{23} + \frac{z_{24}z_{34}}{z_{44}+R_L} \end{aligned} \tag{23}$$

where

$$C = \frac{z_L}{R_L^2 + |z_{44}|^2}.$$

Note that all the impedance elements from $\mathbf{z_{4P}}$ should be imaginary, which is used to determine the proper signs in (22). It is worth mentioning that z_{44} and R_L offer two degrees of freedom. It is then straightforward to convert the lossless and reciprocal four-port impedance parameters to four-port admittance parameters ($\mathbf{y_{4P}}$). From them, it is always possible to synthesize a lumped-element combiner network [31], as shown in Fig. 5. The value of each element in the combiner network can be calculated from the four-port admittance parameters:

$$Y_k = y_{kk} + \sum_{j=1, j\neq k}^{n} y_{kj} \tag{24}$$

with cross elements:

$$Y_{kj} = -y_{kj} \tag{25}$$

where Y_k and Y_{kj} denote the admittance in the combiner network, while y_{kk} and y_{kj} stand for the parameters in the four-port admittance matrix.

The combiner network presented in Fig. 5 may be difficult to realize in a real design. However, as presented previously, there are two degrees of freedom when converting the lossy three-port combiner network to the lossless four-port combiner network, i.e, z_{44} and R_L. R_L can, for instance, be set to $50\ \Omega$ to let the combiner directly interface the $50\ \Omega$ load termination. Moreover, the lumped-element components Y_{12} and Y_{13} both can be approximately nullified by tuning the

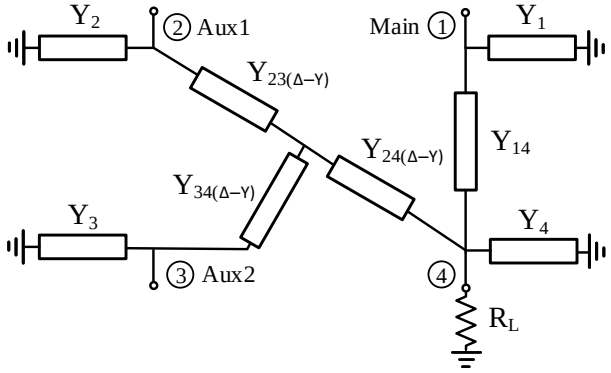

Fig. 6. Simplified combiner network after tuning of z_{44} and $\Delta - Y$ circuit transformation.

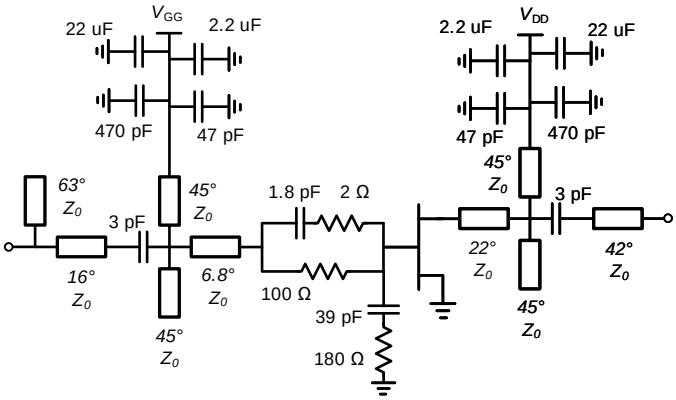

Fig. 7. Schematic of the single PA design, which is used for the Main, Aux1, and Aux2 cells.

value of z_{44}, without any influence on the combiner operation. This simplifies the physical realization of the combiner network significantly. The layout of the combiner network can be even more compact and easier to be fabricated, if $\Delta - Y$ circuit transformation is applied. Fig. 6 illustrates the resulting simplified output combiner network, which can be transformed to a transmission-line based network, if desired.

Therefore, it is possible to realize a compact output combiner network with the presented load-pull based analytical synthesis approach. In the next section, the practical application of the complete procedure is illustrated through the design of a symmetrical three-stage Doherty PA at 2.14 GHz.

VI. Prototype Design Demonstration

In this section, a prototype PA which follows the proposed approach is designed to illustrate the complete design procedure. A commercially available 10-W packaged GaN HEMT transistor from Wolfspeed (CGH40010F) has been selected to act as the active device in all three stages. Fig. 7 shows the schematic of the employed PA cell, which includes stabilization, fundamental source matching, second harmonic source and load terminations, as well as bias and supply feeds. The same PA cell is used for Main, Aux1 and Aux2 cells, except for the choice of gate biasing and fundamental load. The fundamental output matching network is omitted as the output combiner network, which is obtained directly from load-pull data, merges matching and combining operation into a single compact and low loss network. The drain bias voltage is set to $V_{\mathrm{DD}} = 28$ V for all three amplifier cells.

Fig. 8 shows a step-by-step flowchart of the design methodology used. Details of each step are presented below.

Step 1: The PA efficiency is designed to have peaks at $\gamma_{B1} = 10$ dB and $\gamma_{B2} = 6$ dB, respectively. Note that the selection of the gate bias for the Main cell should be made taking into account the trade-offs between gain and efficiency performance. For example, a Main cell biased at towards Class-AB mode helps to improve the overall gain performance of the PA, meanwhile its efficiency performance is degraded. In this specific design, the gate bias for the main cell is determined to be $V_{\mathrm{GG-m}} = -3.1$ V.

Step 2: Select the gate bias for the Aux1 and Aux2 cells. The selection of the gate bias may require several iterations to find the bias for the Aux1 and Aux2 cells to turn them on at the desired back-off power levels. The gate bias for Aux1 and Aux2 cells are, in this design, selected to be $V_{\mathrm{GG-a1}} = 5.2$ V and $V_{\mathrm{GG-a2}} = -7.8$ V, respectively.

Step 3: Perform load-pull characterization of the Main, Aux1 and Aux2 cells at maximum and two selected back-off power levels. The load pull is performed with the selected bias points for the Main, Aux1 and Aux2 cells in the previous steps. The load-pull simulation data obtained for this prototype, is presented in Table II. The off-state impedances of the Aux1 and Aux2 cells at the two back-off power levels, are $(0.74 - j11.8)\ \Omega$ and $(0.73 - j12.0)\ \Omega$, respectively.

Step 4: Numerically solve the two output current phase delays θ_1 and θ_2, using (6)-(8). For this design example, their values are calculated to be $45°$ and $53°$, respectively. Therefore, using the theory presented in Section IV, the lossy three-port impedance matrix $\mathbf{Z_{3P}}$ can be determined as

$$\mathbf{Z_{3P}} = \begin{bmatrix} 11.4 + j7.5 & 5.9 - j4.3 & 4.1 - j1.6 \\ 5.9 - j4.3 & 3.1 - j1.5 & 1.9 - j6.8 \\ 4.1 - j1.6 & 1.9 - j6.8 & 1.5 - j0.75 \end{bmatrix}. \quad (26)$$

Step 5: Convert lossy three-port impedance matrix $\mathbf{Z_{3P}}$ to a lossless four-port impedance matrix $\mathbf{z_{4P}}$, using (22) and (23), which is then converted into admittance matrix form $\mathbf{y_{4P}}$.

Step 6: Realize an initial lumped-element combiner network from the obtained four-port admittance matrix $\mathbf{y_{4P}}$, using (24) and (25). The lumped-element combiner network is then further simplified by fine tuning the value of z_{44}, to eliminate the cross connections in the admittance matrix. The following $\mathbf{y_{4P}}$ is obtained:

$$\mathbf{y_{4P}} = \frac{j}{1000} \begin{bmatrix} -71 & 0 & 0 & -42 \\ 0 & 3 & 183 & 31 \\ 0 & 183 & 108 & 76 \\ -42 & 31 & 76 & 13 \end{bmatrix}. \quad (27)$$

Step 7: Apply $\Delta - Y$ circuit transformation to make the combiner more compact and easier to fabricate. The resulting lumped-element output combiner network is finally converted to a transmission-line based network [25]. The resulting transmission-line combiner is presented in Fig. 9.

TABLE II
SELECTED LOAD-PULL SIMULATION DATA AT 2.14 GHZ

	Main			Aux1			Aux2		
	$Z_{opt}(\Omega)$	P_{out} (dBm)	PAE (%)	$Z_{opt}(\Omega)$	P_{out} (dBm)	PAE (%)	Z_{opt} (Ω)	P_{out} (dBm)	PAE (%)
Peak power	$14.2 - j5.9$	42.1	66.1	$10.4 - j5.2$	41.8	65.3	$7.0 - j4.7$	41.0	56.6
6 dB back-off (γ_{B2})	$10.6 + j1.7$	40.0	63.8	$7.0 + j4.7$	37.8	71.7	–	–	–
10 dB back-off (γ_{B1})	$6.8 + j7.8$	37.0	68.6	–	–	–	–	–	–

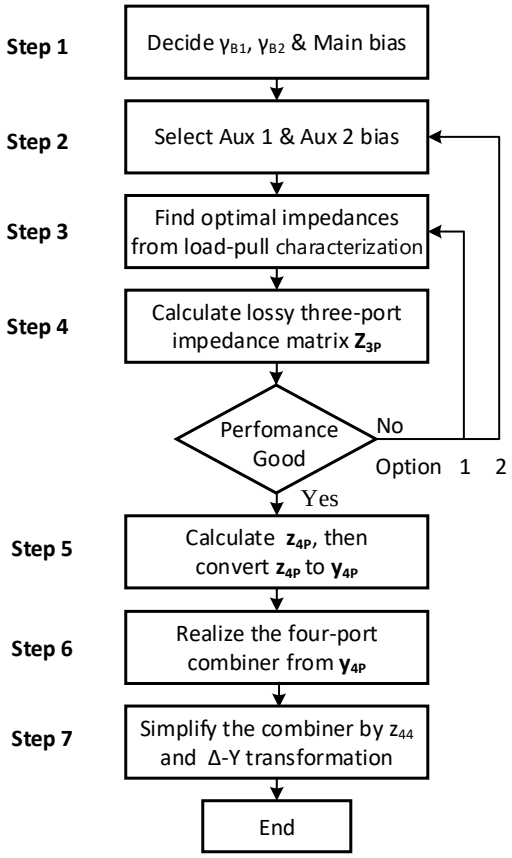

Fig. 8. Design methodology enabling high power back-off efficiency enhancement using load-pull data from simulation or measurement.

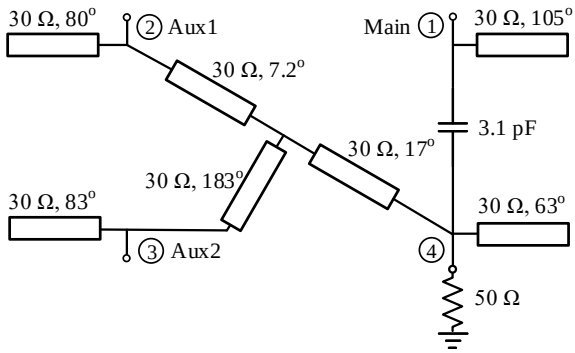

Fig. 9. Final output combiner network realization derived from the simulated load-pull data using the proposed design methodology.

A three-way equal-split power divider is used at the input of the prototype circuit. It should be stressed that, in order to use the symmetrical power splitter, the input power level of the Main, Aux1 and Aux2 amplifier cells should be identical, when performing load-pull characterization during the design process. Single-stub impedance-matching networks are used at the inputs of the Main, Aux1 and Aux2 amplifier cells. Furthermore, 50-Ω transmission lines are added to the inputs of the Aux1 and Aux2 cells to provide proper phase delays.

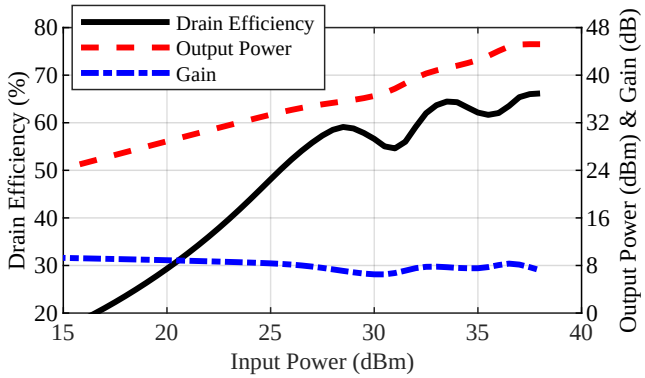

Fig. 10. Simulated drain efficiency, output power and gain versus input power of the prototype three-stage Doherty PA at 2.14 GHz.

The output power, efficiency and gain simulation results using transistor models provided by the vendor are shown in Fig. 10. The simulated efficiency and power profiles show a clear three-stage Doherty PA behavior. Moreover, comparing the load-pull data from Table II with the final simulated results, it is evident that the analytical load-pull based design approach enables the highest possible efficiency performance from the device at peak and back-off power levels.

VII. MEASUREMENT RESULTS

The output combiner and test circuits derived in the previous section has been implemented on a 20-mil Rogers 4350B substrate. All transmission lines are EM simulated using Keysight Momentum and models provided by Modelithics are employed for all the lumped elements to guarantee good agreement between measurements and simulations. Fig. 11 shows a photograph of the fabricated 2.14 GHz prototype circuit with three 10-W GaN HEMT devices (CGH40010F) from Wolfspeed. The design assumes equal power split. The input power is therefore divided using a surface mount three-way SCN-3-28 power splitter from Mini-Circuits. The input transmission lines are designed to provide proper input phase delays to the Aux1 and Aux2 cells.

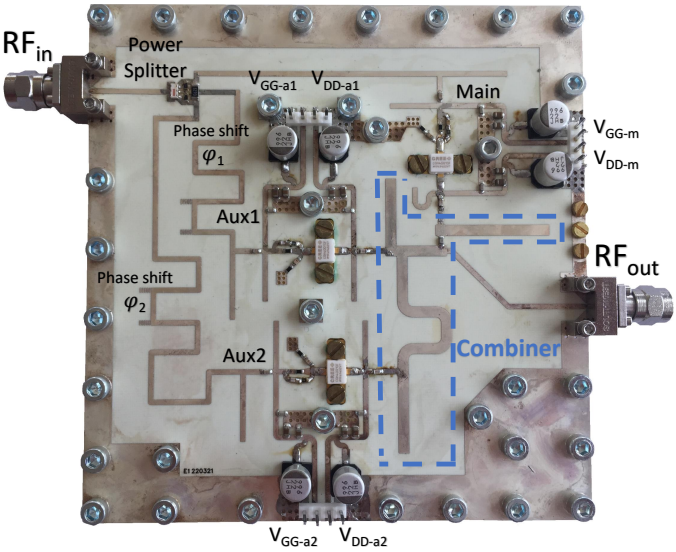

Fig. 11. Photograph of the fabricated three-stage Doherty PA prototype. The dimensions are 11.0 cm $\times$ 11.4 cm.

To evaluate the performance of the fabricated symmetrical three-stage Doherty PA, measurement results for continuous-wave (CW) and digitally modulated signals are presented below. The measurement results are compared with representative state-of-the-art load modulated PAs at the end of the section.

A. *Continuous-wave measurements*

The measurement results using CW signals at 2.14 GHz are presented and compared with harmonic balance (HB) simulations. A drain bias voltage of $V_{\mathrm{DD}} = 28$ V is used for all PA cells. The Main cell is biased for a quiescent drain current of 26 mA, corresponding to a gate voltage of $V_{\mathrm{GG-m}} = -3.1$ V. The gate voltages for Aux1 and Aux2 cells are selected to be $V_{\mathrm{GG-a1}} = -5.2$ V and $V_{\mathrm{GG-a2}} = -7.8$ V, respectively. During measurements, the gate bias of Aux1 and Aux2 were slightly modified to $V_{\mathrm{GG-a1}} = -5.5$ V and $V_{\mathrm{GG-a2}} = -8$ V for better agreement with simulations.

The measured and simulated drain efficiency versus output power profiles at 2.14 GHz are presented in Fig. 12. The maximum measured output power is 45.3 dBm whilst the measured drain efficiency values at 6-dB and 10-dB power back-off levels are 68% and 56%, respectively. As shown in the figure, the measured drain efficiency profile agrees very well with the circuit simulations. Moreover, a distinct three-stage Doherty PA efficiency profile is achieved, which confirms the effectiveness of the proposed design methodology.

The measured and simulated PAE and power gain at 2.14 GHz are presented in Fig. 13 and 14, respectively. The measured PAE at 6-dB and 10-dB output power back-offs is 56% and 45%, respectively. The agreement between measurements and simulations is in general very good, although the measured PAE and power gain shows a small degradation compared to simulations in the lower output power region.

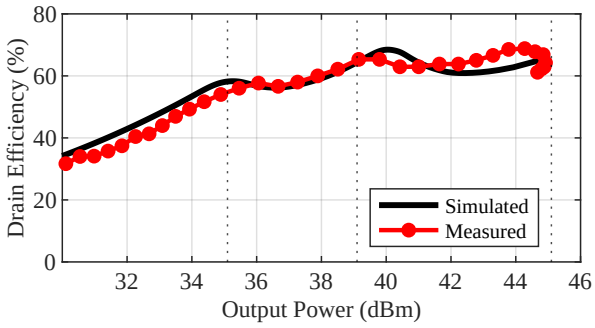

Fig. 12. Measured and simulated drain efficiency versus output power.

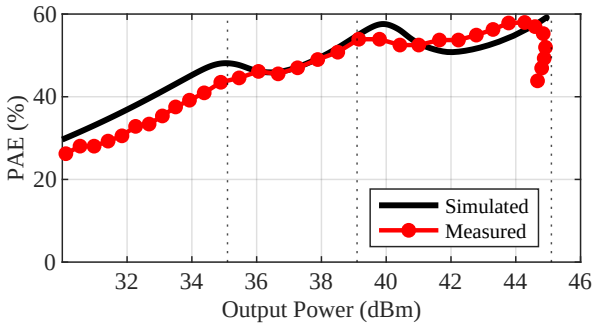

Fig. 13. Measured and simulated PAE versus output power.

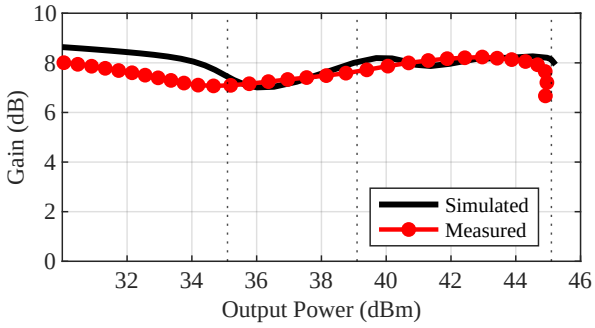

Fig. 14. Measured and simulated gain versus output power.

In Fig. 15 and 16, the measured efficiency performance is presented versus frequency for different output power back-off levels. As seen from the figures, the prototype circuit exhibits a drain efficiency of higher than 58% and 48% and a PAE of higher than 44% and 39% at 6-dB and 10-dB power back-off levels, respectively, across 2.08 – 2.20 GHz.

The measured output power and gain results are presented in Fig. 17. Across the 2.08 – 2.20 GHz frequency band, the output power and the gain are above 44.5 dBm and 7.5 dB, respectively. There are several reasons to explain the relatively narrowband nature of the presented design. First, the employed PA unit cell design in Fig. 7 is designed for single-frequency operation at 2.14 GHz. The overall design procedure is also based on load-pull characterization at a single frequency only. Although it goes beyond the scope of the current work, a more wideband design could be obtained by incorporating load-pull data from different frequencies in the design procedure.

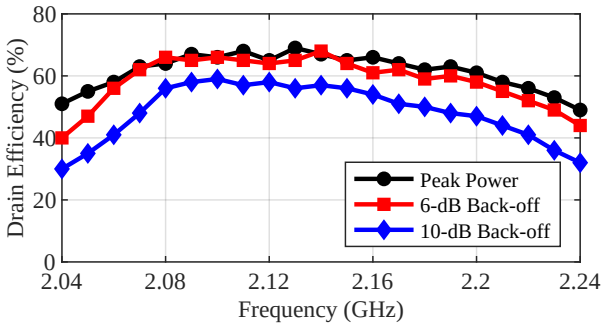

Fig. 15. Measured drain efficiency versus frequencies at peak, 6-dB, and 10-dB back-off power levels.

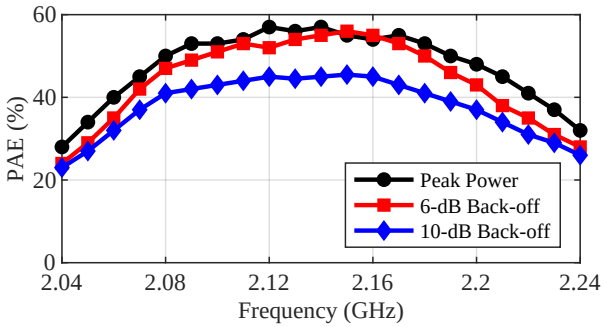

Fig. 16. Measured PAE versus frequencies at peak, 6-dB, and 10-dB back-off power levels.

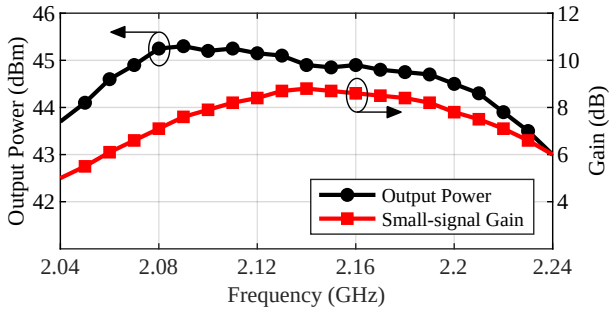

Fig. 17. Measured output power and small-signal gain versus frequencies.

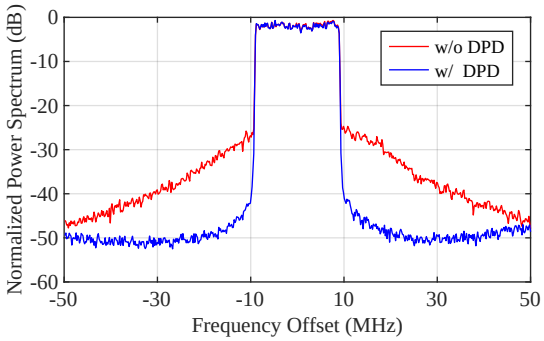

Fig. 18. Measured normalized power spectral density for a 20-MHz 8.5-dB PAPR LTE signal at 2.14 GHz, with and without DPD.

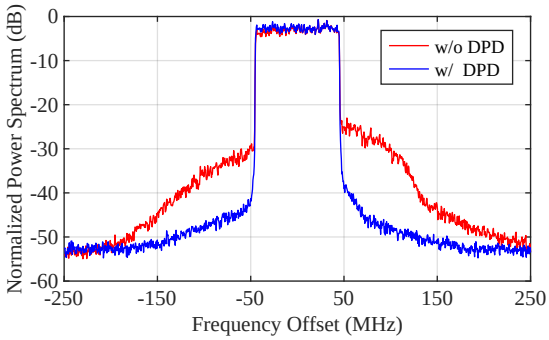

Fig. 19. Measured normalized power spectral density for a 100-MHz 8.5-dB PAPR LTE signal at 2.14 GHz, with and without DPD.

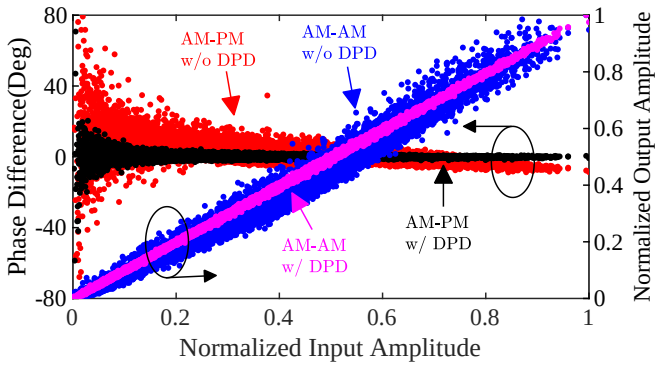

Fig. 20. Measured AM-AM and AM-PM characteristics when using a 100-MHz 8.5-dB PAPR LTE signal at 2.14 GHz, with and without DPD.

B. Modulated-signal Measurements

The performance of the three-stage Doherty PA prototype is characterized at 2.14 GHz using Long Term Revolution (LTE)-like signals of varying PAPR and bandwidth. Results are presented both with and without the use of digital predistortion linearization (DPD) with the generalized memory polynomial model [32]. The initial tests are made with a 8.5-dB PAPR 20-MHz LTE signal at 2.14 GHz. Without any linearization, the PA prototype circuit provides an average drain efficiency of 56.6% and an adjacent channel leakage ratio (ACLR) of below −28.6 dBc at an average output power of 36.8 dBm. After applying DPD, the ACLR of the prototype is improved to −49.4 dBc at an average output power of 36.7 dBm. Fig. 18 shows the output spectrum, before and after applying DPD.

When increasing the PAPR of the 20-MHz LTE-like signal to 11.5-dB, which is the case if no crest-factor reduction technique is applied, an average output power of 33.7 dBm and an average efficiency of 46.8% is observed. For this signal, the ACLR values, before and after applying DPD are better than −29.2 dBc and −49.4 dBc, respectively.

Finally, the bandwidth of the 8.5-dB PAPR LTE signal has been scaled up to 100 MHz to test the PA performance under wideband signal excitation. Fig. 19 shows the measured output spectrum with and without applying DPD. The corresponding AM/AM and AM/PM characteristics are presented in Fig. 20. The measured average drain efficiency is reduced to 54.5%

TABLE III
COMPARISON WITH STATE-OF-THE-ART LOAD MODULATED PAS.

Reference	Architecture	f_0 (GHz)	P_{max} (dBm)	Continuous-wave measurement $\eta_{\text{-10 dB/-6 dB/-0 dB}}$ (%)	Continuous-wave measurement $PAE_{\text{-10 dB/-6 dB/-0 dB}}$ (%)	Modulated-signal measurement BW (MHz)	PAPR (dB)	η_{avg} (%)	ACLR (dBc)
[33]	Outphasing	2.14	50.2	42/60/51	N/A	3.84	9.15	54.5	$-34.2^{w/o}$
[27]	LMBA	2.4	45.6	-/54/67	34/50/61	10	7.5	47	$-27^{w/o}$
[34]	CLMA	2.09	43.1	48/73/72	N/A		N/A		
[25]	Doherty 2-way	1.95	44	52/62/68	44/57/60	20	9	55	$-49^{w/}$
[35]	Doherty 2-way	2	42.9	50/60/70	47/60/68	20	9.55	53.3	$-47.1^{w/}$
[18]	Doherty 3-stage	0.75	46	58/60/74	-/-/72	15	10.6	51.7	$-46.3^{w/}$
[22]	Doherty 3-stage	2.65	50.5	46/56/55	40/46/49	10	7.8	55	$-40^{w/}$
[19]	Doherty 3-stage	2.1	45.7	46/61/59	N/A	40	8.5	50	$-50^{w/}$
This work	Doherty 3-stage	2.14	45.3	55/68/69	45/56/57	20	8.5	56.6	$-49.8^{w/}$
						20	11.5	46.8	$-49.4^{w/}$
						100	8.5	54.5	$-45.7^{w/}$

whilst providing an average output power of 36.2 dBm. The ACLR is improved from -26.3 to -45.7 dBc after DPD.

C. Performance Comparison

Table III presents a summary of the static and dynamic measurement results and compares them with representative state-of-the-art load modulated PAs that target high efficiency at deep power back-off. The performance of the symmetrical three-stage Doherty PA in this work stands out in terms of high efficiency at deep back-off at comparable frequencies. The presented PA also shows very good linearity performance with competitive average efficiency and output power values with modulated signals, while meeting the requirements of modern wireless communication standards.

VIII. CONCLUSION

A generic methodology for systematic design of highly efficient three-stage Doherty PAs has been proposed. The methodology is tailored to maximize the PA efficiency at two reconfigurable output power back-off levels, therefore enhancing the average efficiency for signals with high PAPR values. The method is based on an analytical design approach where the combiner network, and its physical realization, is derived directly from the conditions and transistor load-pull data that guarantee maximum performance in three-stage Doherty PAs. The obtained four-port combiner integrates the output matching and load modulation circuits in one compact network. It therefore results in a combiner network with very low loss. The proposed method has been experimentally verified through the design of a 2.14 GHz GaN prototype PA presenting excellent efficiency performance when amplifying modern communication signals with large bandwidth and high peak-to-average power ratio.

The main advantage of the proposed design method, compared to traditional three-stage Doherty PAs, is the possibility to realize the design for varying back-off efficiency peaks while maintaining full transistor utilization even with identical transistors. With symmetrical transistors, the input power splitting is simplified, the gain is improved, and the overall efficiency is maximized. Thus, the symmetrical three-stage Doherty PA fabricated using the load-pull based analytical method can be a strong candidate for future wireless transmitters where high power back-off efficiency and compact size are required. Furthermore, it is possible to use the proposed generic theory to understand fundamental limits of three-stage Doherty PAs, and for exploration of new multiple-input architectures.

ACKNOWLEDGMENT

The authors would like to thank Modelithics, Inc., Tampa, FL, USA, for the use of Modelithics models utilized under the University License Program. The authors also acknowledge Dr. L. Peterson, Chalmers University of Technology, for fruitful discussions.

REFERENCES

[1] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng.*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.
[2] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
[3] F. H. Raab, "High-efficiency linear amplification by dynamic load modulation," in *IEEE MTT-S Int. Microw. Symp. Dig*, vol. 3, pp. 1717–1720, Jun. 2003.
[4] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," in *IEEE MTT-S Int. Microw. Symp. Dig*, vol. 2, pp. 873–876, Jun. 2000.
[5] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microwave Mag.*, vol. 7, no. 5, pp. 42–50, Nov. 2006.
[6] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.
[7] J. Xia, M. Yang, Y. Guo, and A. Zhu, "A broadband high-efficiency Doherty power amplifier with integrated compensating reactance," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2014–2024, Jul. 2016.
[8] M. Iwamoto, A. Williams, Pin-Fan Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.
[9] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 425–434, Feb. 2011.
[10] H. Jang, P. Roblin, C. Quindroit, Y. Lin, and R. D. Pond, "Asymmetric Doherty power amplifier designed using model-based nonlinear embedding," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3436–3451, Dec. 2014.

[11] D. Gustafsson, C. M. Andersson, and C. Fager, "A modified Doherty power amplifier with extended bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 533–542, Jan. 2013.
[12] Youngoo Yang, Jeonghyeon Cha, Bumjae Shin, and Bumman Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 986–993, Apr. 2003.
[13] F. H. Raab, "Efficiency of Doherty RF power-amplifier systems," *IEEE Trans. Broadcast.*, vol. BC-33, no. 3, pp. 77–83, Sep. 1987.
[14] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The Doherty power amplifier," *Advanced Microwave Circuits and Systems*, pp. 108–132, 2010.
[15] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 852–860, Mar. 2005.
[16] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 866–879, May. 2007.
[17] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.
[18] A. Barthwal, K. Rawat, and S. K. Koul, "A design strategy for bandwidth enhancement in three-stage Doherty power amplifier with extended dynamic range," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1024–1033, Feb. 2018.
[19] J. Xia, W. Chen, F. Meng, C. Yu, and X. Zhu, "Improved three-stage Doherty amplifier design with impedance compensation in load combiner for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 2, pp. 778–786, Feb. 2019.
[20] A. Barthwal, K. Rawat, and S. K. Koul, "Dual input digitally controlled broadband three-stage Doherty power amplifier with back-off reconfigurability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1421–1431, Mar. 2021.
[21] W. Neo, M. Pelk, L. de Vreede, Y. Zhao, and R. Gajadharsing, "3-way Doherty amplifier with minimum output network," 2009, NXP B.V. - Eindhoven; WO 2009/081341; H03F.
[22] I. Kim, J. Moon, S. Jee, and B. Kim, "Optimized design of a highly efficient three-stage Doherty PA using gate adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2562–2574, Aug. 2010.
[23] H. Golestaneh, F. A. Malekzadeh, and S. Boumaiza, "An extended-bandwidth three-way Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3318–3328, Aug. 2013.
[24] A. Barthwal, K. Rawat, and S. Koul, "Bandwidth enhancement of three-stage Doherty power amplifier using symmetric devices," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2399–2410, Aug. 2015.
[25] M. Özen, K. Andersson, and C. Fager, "Symmetrical Doherty power amplifier with extended efficiency range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1273–1284, Apr. 2016.
[26] W. Hallberg, M. Özen, D. Gustafsson, K. Buisman, and C. Fager, "A Doherty power amplifier design method for improved efficiency and linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4491–4504, Dec. 2016.
[27] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of a Doherty-like RF-input load modulated balanced amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5322–5335, Dec. 2018.
[28] S. C. Cripps, *RF Power Amplifiers for Wireless Communications, 2nd ed.* Artech house Norwood, MA, 2006.
[29] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty power amplifier. Part I: Theory," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 19, no. 3, pp. 293–306, Nov. 2009.
[30] A. Grebennikov, *Radio Frequency and Microwave Power Amplifiers, Volume 2 - Efficiency and Linearity Enhancement Techniques*. Institution of Engineering and Technology, ch. 5, 2019.
[31] P. Linnér, *Unified Electronic Circuit Simulation: Theory and Design*. Chalmers University of Technology, 2010.
[32] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *IEEE Trans. Signal Process.*, vol. 54, no. 10, pp. 3852–3860, Sep. 2006.
[33] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-way lossless outphasing system based on an all-transmission-line combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1313–1326, Apr. 2016.
[34] H. Zhou, J.-R. Perez-Cisneros, and C. Fager, "Circulator load modulated amplifier: A non-reciprocal wideband and efficient PA architecture," in *IEEE MTT-S Int. Microw. Symp. Dig*, Jun. 2021.
[35] C. Liang, P. Roblin, and Y. Hahn, "Accelerated design methodology for dual-input Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 10, pp. 3983–3995, Oct. 2019.

Han Zhou received the B.Sc. degree in aerospace engineering from Harbin Institute of Technology, Harbin, China, in 2016. He received the M.Sc. degree in electrical engineering from the Chalmers University of Technology in 2018, where he is currently pursuing the Ph.D. degree.

His research interests include highly efficient, wideband and linear power amplifier architectures for future wireless transmitters and design of mm-wave CMOS/III-V front-ends.

Jose-Ramon Perez-Cisneros received his Ph.D. degree (*cum laude*) from University of Zaragoza, Spain, in 2017. He currently holds a post-doc position at the Microwave Electronics Laboratory from Chalmers University of Technology, Sweden. From 2017 to 2019 he worked as researcher at the RF and Microwave Group from University of Cantabria, Spain. From 2013 to 2017 he was with the Institute of Engineering Research in Aragón (I3A) of the University of Zaragoza, being part of the Mobile Communications Group.

He has authored or coauthored more than 20 publications in international journals and conferences. His main research interests include wireless communications systems, with emphasis on high-efficiency wireless transmitters, tunable matching networks and RF/microwave topologies such as power amplifiers, rectifiers and DC/DC converters.

Sara Hesami received the M.Sc. degree from KTH Royal Institute of Technology, Stockholm, Sweden in 2012, and the Ph.D. degree from the Maynooth University, Maynooth, Ireland, in 2020. From 2020 to 2021, she was a Post-Doctoral Researcher with the Chalmers University of Technology, Gothenburg, Sweden. Since 2021, she has been a researcher at Ericsson AB, Kista, Sweden.

Her current research interests include RF measurements and signal processing for RF impairment mitigation, over-the-air measurements and system identifications for power amplifier modeling and linearization.

Koen Buisman (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2004 and 2011, respectively.

From 2004 to 2014, he was with the Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology. In 2014, he joined the Chalmers University of Technology, Gothenburg, Sweden, where he is currently an Affiliated Associate Professor with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience. In addition, in 2020, he joined the University of Surrey, Guildford, U.K., where he is currently a Reader in microwave and mm-wave electronics. He is also the Director of the Nonlinear Microwave Measurement and Modeling Laboratories, a joint University of Surrey/National Physical Laboratory, Teddington, U.K.

He has authored or coauthored over 85 refereed journal and conference papers. He holds one patent. His current research interests include nonlinear device characterization, technology optimization, and design of linear transceivers for wireless systems.

Christian Fager (Senior Member, IEEE) received his Ph.D. degree from Chalmers University of Technology, Sweden, in 2003. He became Full Professor at the same university in 2019 and is currently Head of the Microwave Electronics Laboratory. He has authored or co-authored more than 200 publications in international journals and conferences, where he has made significant contributions to the area of linear and energy efficient power amplifiers and transmitters for wireless communications.

Dr. Fager serves as Associate Editor of IEEE Microwave Magazine and IEEE Microwave and Wireless Components Letters. He is representative for Sweden, Norway and Iceland in the European Microwave Association (EuMA) and member of the IEEE MTT-S Technical Committee on Wireless Communications. He served as chair of the 2021 IEEE Topical Conference on RF/microwave Power Amplifiers and TPC co-chair for the 2020 European Microwave Integrated Circuits Conference. Dr. Fager received Chalmers Supervisor of the Year Award in 2018 and the IEEE International Microwave Symposium Best Student Paper Award in 2002.