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MODULAR MULTILEVEL CONVERTERS WITH MODULE-LEVEL ENERGY STORAGE FOR MEDIUM VOLTAGE APPLICATIONS

by

Bora Novakovic

A Dissertation Submitted in
Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
in Engineering

at

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ABSTRACT

MODULAR MULTILEVEL CONVERTERS WITH MODULE-LEVEL ENERGY STORAGE FOR MEDIUM VOLTAGE APPLICATIONS

by

Bora Novakovic

The University of Wisconsin-Milwaukee, 2021
Under the Supervision of Professor Adel Nasiri

This dissertation is on Modular Multilevel Converter (MMC) converter design and analysis and its integration with energy storage at the low voltage module-level. The developed converter concept and topology can be used in various applications especially for the support of intermittent renewable energy resources. The general converter structure is analyzed and extended to include integrated energy storage suitable but not limited to medium voltage applications. The behavior of the idealized structure is analyzed to obtain equations that govern general converter behavior and identify possible control loops. Detail mathematical switching model is developed for the MMC converter with generalized module structure. The switching model is averaged to obtain a large signal model and then reduced to obtain lower order models suitable for sizing and optimization. Open and compensated closed loop current control is proposed and extended to include feedback loops needed for full control of integrated energy storage. General sizing procedure with the optimization aspects is then proposed and used on the example system to obtain the converter structure parameters. The example system models are then used to fine tune the control and structure parameters and investigate the converter behavior.

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GLOSSARY

M^2LC Modular MultiLevel Converter.

CHB Cascaded H-Bridge.

DAB Dual Active Bridge.

FACTS Flexible AC Transmission Systems.

FERC Federal Energy Regulatory Commission.

HVDC High Voltage Direct Current.

IGBT Insulated Gate Bipolar Transistor.

KVL Kirchhoff's Voltage Law.

LVRT Low Voltage Ride Through.

MMC Modular Multilevel Converter.

MMCC Modular Multilevel Cascaded Converter.

MVDC Medium Voltage Direct Current.

PFR Primary Frequency Response.

PLL Phase Locked Loop.

PV Photovoltaic.

PWM Pulse Width Modulation.

SCADA Supervisory Control and Data Acquisition.

STATCOM Static Synchronous Compensator.

THD Total Harmonic Distortion.

WECSS Wind Energy Conversion and Storage System.

1 Introduction

1.1 Problem Statement

The trend for power electronics systems is to move to higher power voltages and control utility grid power and energy. Various power converter topologies have been proposed and developed for medium voltage and high power systems. One major issue is that energy storage systems are typically developed and operated at low voltage and an efficient means for integration with medium voltage systems is required. The focus of this research is the analysis of Modular Multilevel Converter (MMC) converter topology and integration of energy storage to create power and energy flexibility. The main purpose of this analysis is to investigate the modifications to the MMC topology and necessary control that will facilitate the possibility of energy storage integration. This will make the converter suitable for the high power medium voltage systems that require higher level of decoupling between the input and output power flows. The decoupling between the input and output power flows is commonly associated with modern renewable energy systems grid tie converters, especially for wind and solar. While it is not limited to the renewable energy systems applications, this converter topology aims to solve the same set of challenges commonly associated with converters used in modern wind turbines and large solar fields. To put the problem in more practical framework the challenges and the solutions will be treated from a wind energy system standpoint. The energy storage and the converter will therefore be designed to assist with the power by the new grid connection codes for renewable energy.

1.2 Motivation

There is a need for integration of energy storage systems at various levels of power conversion systems to improve reliability, flexibility, and stability. MMC topology enables medium voltage power conversion using widely available low-voltage power switching devices. In the same manner, low-voltage energy storage systems can be conceptually integrated with MMC converter to offer energy storage and energy conversion in a single converter. MMC topology is a complex converter in regard to hardware and control. Adding energy storage adds flexibility to converter but increases complexity. This dissertation performs detail analysis, formulation, control, and simulation of the new concept. The developed converter can help with better control of energy from renewable resources and ultimately increase their penetration.

1.2.1 Large Wind Energy Systems

The percentage of renewable energy systems in the total world power generation is constantly increasing [7], [8]. With the increase in number of large offshore wind farms, the size of the individual wind turbine is increasing as well. At the end of 2016 the average power rating of a single wind turbine was about 2MW [8]. Individual offshore wind turbines of 8MW are available and power levels of 10MW-20MW are being researched [9], [10], [11]. The increase in the power conversion system size introduces new technical challenges into electrical, mechanical and control subsystems design. For wind energy systems these challenges can be summarized in several groups:

1. Intermittent and unpredictable nature of the wind energy can affect the power system

stability in a negative manner on many levels. Large power production fluctuations can change the grid frequency, voltage or even destabilize the entire power system. This is especially true in cases when wind accounts for a large percentage of the power production in a utility grid. Such utility grids usually do not have enough conventional generators that would provide a sufficient amount of inertia and counteract sudden changes in power delivery from the wind. Problem of intermittency and unpredictability is common for wind and solar power systems. As a consequence, utility companies with high percentage of renewables impose strict power quality codes for such systems [12], [13].

2. Fault ride through capabilities are required by the new grid connection codes for all renewable energy systems. Fault ride through requirements dictate the behavior of a grid connected power converter during the short term grid faults. Fault ride through behavior is an important aspect of any grid connected system, specially the power generating systems. To maintain power grid stability and to prevent the sudden loss of large amount of power production, it is important to keep the power generating system on line during short faults and low voltage conditions [5]. The fulfillment of these requirements can be challenging for the systems that rely on sensitive power electronic converters like modern wind turbines and Photovoltaic (PV) systems.
3. Ancillary support requirements for reactive power and grid frequency are also included in the most new grid connection codes for renewable energy systems [5]. Implementation of these requirements requires that the system always has power and energy reserve in order to be able to support the grid in cases of low voltage or low frequency

conditions. This requirement conflicts the intermittent nature of wind and PV systems.

4. Steady increases in wind turbine size and power created a number of design challenges for the electrical subsystem. These challenges are mostly related to high current ratings and the efficiency of the power conversion system. For wind turbines this is additionally complicated due to the limited space in the nacelle. High power wind turbines nowadays have full back-to-back conversion systems in excess of 5 MW but they still operate on 690V in most cases. To achieve power levels so high, power converters have to be paralleled. Paralleling and high current ratings negatively affect efficiency, size and economical aspects of the system [14].
5. The power conversion system of wind turbine is usually in the nacelle, high off the ground. Furthermore, offshore wind farms are usually far from the shore and are not easily accessible for repair. Difficult access to the system in conjunction with projected lifetime of a common the wind turbine, which is about 20 years, makes the reliability and fault tolerance specially important issue for the wind energy systems.

1.2.2 Renewable Energy and Storage Systems

If properly integrated with the power converter, energy storage system can provide a level of power decoupling between the power exported to the grid and the power coming from the renewable energy resource. This power decoupling can be helpful for solving the problems associated with fault ride through, ancillary support requirements and intermittency. As a consequence, wind and solar energy systems and energy storage systems complement each other very well [13], [15], [16].

Fault ride through challenges are easier to solve if the energy storage system is integrated into a renewable energy system. This is specially true for the wind energy. Power decoupling provided by the integrated energy storage can be used to isolate and protect the mechanical system of the wind turbine from the grid faults [17].

Energy storage can be used to provide extra power needed to emulate inertia or support the grid frequency [18]. Without the energy storage, renewable energy systems have to be moved off their optimal operating points to maintain power production margin needed for ancillary services. This is known as power curtailing in the available literature.

Power curtailment is also used when for some reason energy coming from the renewable resource cannot be exported to the grid. This condition can be encountered in cases of low power demand or lack of transmission capacity.

As it forces the system off its optimal point, power curtailment decreases the overall efficiency and the affordability of renewable energy. With the use of energy storage, the power flow from the renewable resource to the grid become decoupled, which can reduce or completely mitigate the need for power curtailment [19], [20]. Furthermore, with the properly designed energy storage the excess energy can be stored and used when needed.

When talking about wind turbines and energy storage systems one can notice two parallel trends, the size and the investment into individual wind turbines is continuously going up while the price of energy storage technologies goes down. Furthermore, energy storage systems are becoming more reliable, more affordable and more widespread. As a consequence, joining the wind energy systems and energy storage systems in various ways became more attractive research area [17], [21].

Integrated wind energy system and energy storage system is known as Wind Energy

Conversion and Storage System (WECSS) in the available literature [22]. While somewhat covered in the literature, integrated wind energy and energy storage systems are still not common in industry. However, one can argue that the technology will eventually come to a point when the benefits from the integration of the energy storage within a wind turbine will overcome the drawbacks of the increased price and complexity of the system.

1.2.3 Medium Voltage Wind Energy Systems

While the individual wind turbines power rating have increased steadily over the years, the majority of generators and power converters inside individual wind turbine remains at low-voltage levels, below $1kV$. For the systems above 0.75MW low-voltage power converters are usually paralleled to achieve the appropriate current rating as shown in Figure 1 [14].

Parallel arrangement of low-voltage power converters is used in many commercial high power wind turbines as most commercially effective solution. However, for the wind turbines above 3MW this arrangement is affecting efficiency and reliability of the power conversion system. As an example, a 3MW wind turbine requires a number of converters connected in parallel to handle 2500A of the output current per phase. High current levels dissipate relatively high amount of heat in the converter semiconductors and conductors of the generator and the step-up transformer. This creates a cooling problem in the narrow space of the wind turbine nacelle. One way to solve the dissipation problem is to move to medium voltage levels to reduce the current ratings of the conversion system.

Although medium voltage technology is mature for motor drives, it is still not common for wind energy systems [14]. As a result, some manufacturers are trying to migrate their wind energy systems to medium voltage levels of up to several kV. The use of medium

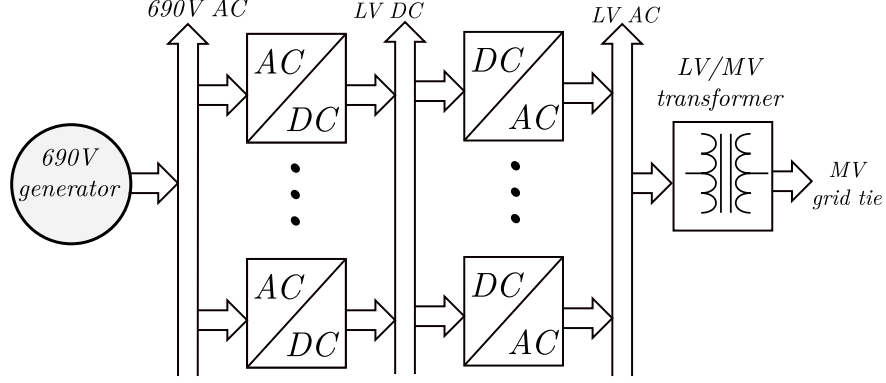


Figure 1: Power conversion system arrangement inside the common low-voltage high-power wind turbine. To achieve desired power level, the power electronics converters are usually paralleled.

voltage generators and power converters improves the system efficiency as it allows the use of a single power converter and eliminates the need for low-voltage converter paralleling but it also introduces new design issues.

One of the major problems with medium voltage converters is silicon semiconductor device breakdown voltage. To overcome this issue multilevel converter topologies are used for medium voltage power electronics systems. For these topologies, the voltage stress on the semiconductor device usually reduces proportionally to the number of levels. As a result, each semiconductor device switches only a fraction of the total DC bus voltage. Multilevel converter topology solves the semiconductor breakdown problem but increases the complexity of the system and sometimes reduces the reliability with the larger number of active components that can fail.

In general, medium voltage power conversion systems are more challenging to design because of the more severe requirements for the insulation system and higher voltage stress on the active components. Increase of the insulation system complexity and voltage stress on the components affects all parts of the conversion system from the generator to the

control system. Protection circuits, data-acquisition circuits, gate-driving circuits, DC bus capacitor banks and power supplies are harder to implement for medium voltage than for the low-voltage converters. It should be noted however, that all additional engineering and design efforts become more justified as the power level increases due to the increase in the system cost and size.

It seems that the wind industry has reached the power levels where the use of medium voltage conversion systems becomes justified and more commercially viable [14], [23].

1.2.4 Multilevel Converters and MMC

For traditional two-level power converters the maximum DC bus and maximum input voltage are limited by the breakdown voltage limitation of the semiconductor switching devices. For conventional two level typologies each switch has to withstand the full DC bus voltage. To overcome the breakdown limitations of the semiconductor switching devices and to increase the output waveform quality, most medium voltage power electronic converters use some sort of multilevel topology. For multilevel topologies the DC bus voltage is evenly spread among the switches that generate the individual voltage levels, the more the levels the higher the total DC bus voltage can go with the same semiconductor switches. The trade-off is of course the use of additional switching and accompanying components.

Most traditional multilevel topologies have quadratic dependence between the number of levels and the component count (i.e. number of diodes in the diode clamped multilevel converters or capacitors in capacitor clamped multilevel converters is proportional to the square of the number of levels) [24]. High component count increases cost and complexity and decreases the converter efficiency. This makes conventional multilevel converter topologies

with number of levels greater than five somewhat unattractive in the industry unless they are necessary.

One of the converter families that allow linear increase of converter complexity with the increase of levels is MMC. One of the most important properties of the MMC family of converters is their modular nature. The number of converter levels is increased by simply adding identical modules, which are completely identical and interchangeable. As a result, this converter topology has become very interesting for medium and high voltage systems that require higher number of levels [25], [26].

If used in high-power wind-energy systems, the desired power level is achieved by increasing the number of modules connected in series as illustrated in Figure 2. This may be viewed as dual approach to the parallel connection of converters given in Figure 1. In this way the operating voltage of the system is increased while keeping the current at relatively low levels, which in some cases increases the efficiency of the system. If the system is operated at medium voltage levels that are high enough, the same voltage can be used for the power transmission and the grid connection transformer from Figure 1 can also be avoided. This makes the overall system lighter and potentially more efficient.

Due to its modular nature the MMC topology can be varied and augmented in many ways. For this study the modification of interest changes the structure of the basic module of the converter to include an energy storage system. Although the MMC topology has been mentioned in the literature for the use with the energy storage systems and wind energy systems separately, as will be shown later in the text, it has not been investigated for the use in Wind Energy Conversion and Storage Systems (WECSS).

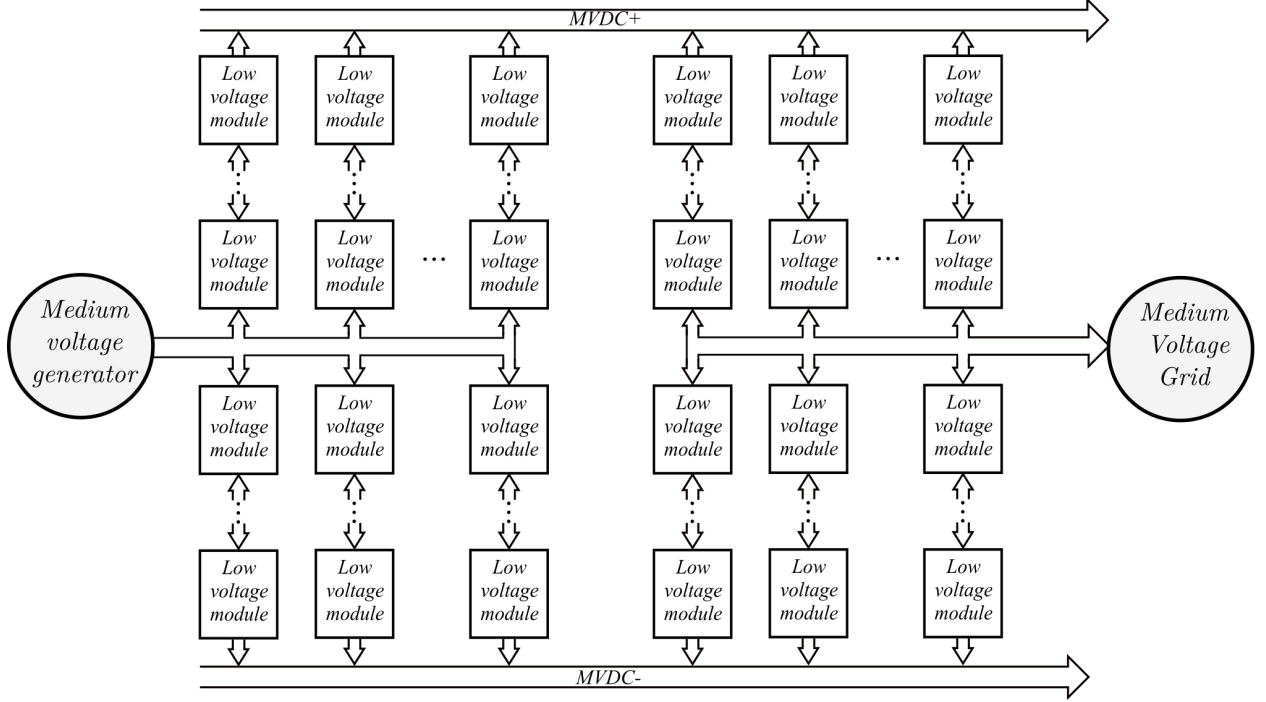


Figure 2: Power conversion system arrangement inside the proposed medium voltage high power wind turbine. To achieve desired power and voltage levels, MMC converter modules are connected in series.

2 Literature background

This section will focus on the research publications related to the MMC converter topology or rather a family of converters that are usually referred under the name MMC. In order to provide the base for the proposed topology modification, an attempt will be made to outline the main branches of this family of converters and show their distinct characteristic and most suitable application.

Attention will also be given to the renewable energy systems, energy storage uses and the applicable grid codes in order to provide the background for the proposed topology modification and its potential usefulness and feasibility.

2.1 MMC Background

Growing demand for high and medium voltage grid tied power electronic conversion systems and medium voltage motor drives in the 1990's and early 2000's inspired an entire family of very similar multilevel converter topologies. The main characteristic of these converter topologies is their modular nature, which allows expanded voltage and power range and overcomes the limitations imposed by the semiconductor switching element breakdown voltage. The modularity in this case refers to the series connection of identical cells or modules that create multiple converter levels. Converters that belong to this family of topologies can be easily recognized in the literature as they usually have label "modular", "stacked" or "cascaded" together with "multilevel" in their names. Although the term MMC appeared later, some researchers classify all these similar modular converter topologies and their variations under this name [27].

The main advantage of the modular multilevel converters compared to the non-modular multilevel topologies like diode or capacitor clamped voltage source converters, is slower increase of power carrying components per additional converter level. Modular topologies usually have linear increase in the component count per level compared to the quadratic increase for non-modular topologies. Besides the number of power components per level, for large number of levels, modular topologies tend to be less complicated and in some cases more efficient.

Although modular topologies have definitive advantages for multilevel converters with high number of levels, they have a disadvantage for the applications that can be implemented with simpler multilevel topologies with low number of levels. For the low level count, modular

topologies tend to require more components per level than non modular. As a result, these topologies are still rarely considered for the applications that operate at low voltage and lower range of medium voltage.

The point where the component count advantage tilts to the modular topologies is usually when the number of levels reach seven or more. This point depends on the particular type and implementation of the stacked or modular multilevel converter and can be significantly higher for some variants. As a result, they are suitable for systems that operate at high voltage and upper range of medium voltage levels where the maximum reverse blocking voltage of available semiconductor devices dictates the requirement for relatively high number of levels.

One of the first modular multilevel converter structures was proposed by Hammond in 1995 [1], [28], [29]. This topology finds its inspiration in medium voltage drives and is commonly referred to as Cascaded H-Bridge (CHB) topology. The proposed multilevel voltage source converter was aimed to be cheaper and better performing than the current source topologies commonly used in medium voltage drives at that time. The topology uses isolated outputs of a multiple winding transformer to supply individual converter cells. A cell of the converter is implemented as low voltage full-bridge inverter supplied by a 3-phase diode bridge rectifier. The full-bridge cell outputs are connected in series to form multilevel phase legs. Phase legs are then Y-connected to supply the motor as shown in Figure 3.

Using this approach, medium voltage drive can be implemented using standard, low voltage semiconductors making the entire power switch and gate driver circuit cheaper. In fact, the drive described in the original publications uses low voltage 480V rated 3-phase supplied full-bridge converters as cells and then uses three cells in series to generate 2.3kV voltage supply for the medium voltage motor [1].

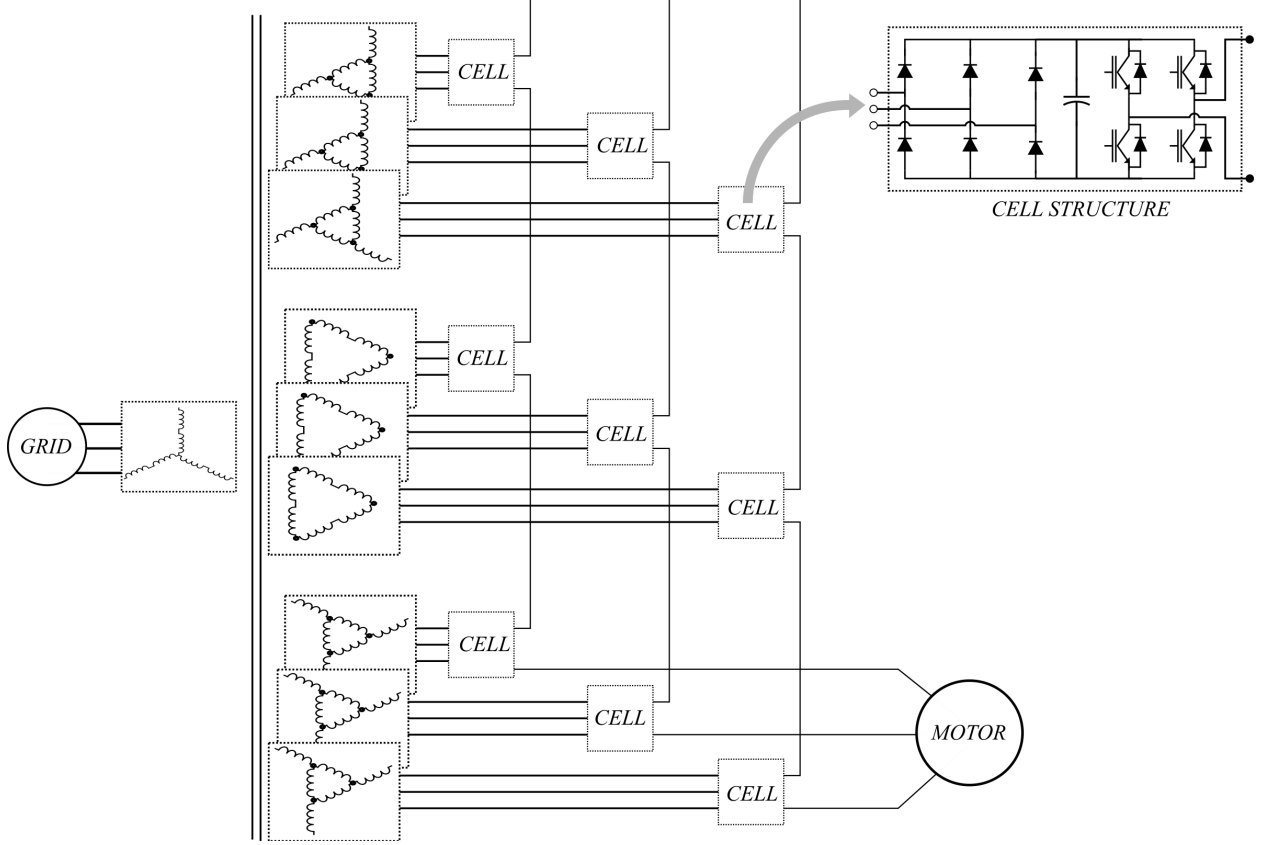


Figure 3: Multilevel structure proposed by Hammond for the use in medium voltage drives [1]. In this case proposed output voltage is 2400V and the cells operate at standard 480V.

The main drawback of the Cascaded H-Bridge converter is the expensive and rather complicated multiple output 3-phase transformer. The system implemented using this topology also cannot operate in all four quadrants, i.e. if the motor enters a generating mode, the active power cannot be delivered to the grid.

One can also argue that this topology is not completely modular in nature. Adding more levels requires not just adding more identical modules in series but also requires modification of the multiple winding transformer, which is an integral part of the converter. For this reason the cells were not marked as modules in Figure 3.

The idea of the modular multilevel topology was pushed a bit further with the "Multilevel Cascade Inverter" proposed in 1995 by Peng *et al.* for Flexible AC Transmission Systems

(FACTS) applications, specifically for the VAr generation [30]. This topology is composed of completely identical modules and the number of levels can be extended by just adding more modules in series. The topology uses stacked full-bridge converters as modules and needs one full-bridge converter for additional level. As a result, N-level inverter can be implemented using $4N$ diodes and $4N$ semiconductor switches. In the original paper the inverter was proposed in two different configurations: Y-connected configuration shown in Figure 4 - (b) and Δ -connected shown in Figure 4 - (c).

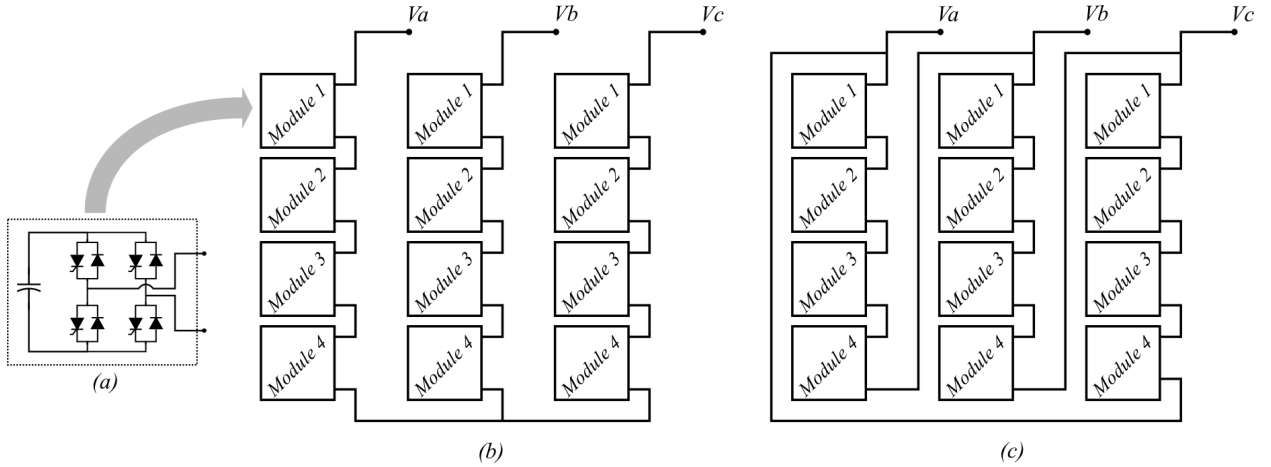


Figure 4: Cascade multilevel structure first proposed by Peng et al. (a) - Module structure. (b) - Y-connected converter configuration. (c) - Δ -connected converter configuration.

Although this inverter seems very attractive for the medium voltage applications that could benefit from a large number of levels and high quality output waveform, the topology has one interesting drawback - it does not have a DC bus in the classical sense. Instead, the DC bus is divided among converter modules. Furthermore, each module DC bus has to be isolated from the rest of the modules. As a result, inverter supply implementation is somewhat challenging. In fact, if we use multiple winding transformer to supply the modules of the Y-connected configuration shown in Figure 4 - (a) we will end up with the converter

topology very similar to the one proposed by Hammond.

In a number of follow-up papers related to the Cascade Multilevel Converter Topology authors argue that the topology can be used for the applications:

- Where individual DC bus voltage can be maintained through the full-bridge output.

These applications include phase shifting, reactive power support - Static Var Generators (SVG) and harmonic filtering [31], [32].

- Where the isolation between DC sources naturally exists. Examples of such systems are PV and fuel cell grid tie converters [30], [33].

The idea that finally introduced a truly modular multilevel AC to DC and DC to AC converter topology was proposed in 2002 by Marquardt *et al.* and is illustrated in Figure 5 [34]. The topology was proposed in an effort to create network inter-tie system suitable for FACTS applications and high power, high or medium voltage power transmission and distribution systems. An obvious trend up to this point was to reduce the module complexity and increase modularity of the topology by utilizing symmetries available in the standard three-phase grid supply. The arrangement in Figure 5 seems to have reached the optimum in this regard. The members of the MMC family of converters that were proposed after usually represent a combination, rearrangement or the adaptation to a new application of the previous three ideas. Although usually considered as the origin for most of the multilevel converters that belong to MMC family, topology in Figure 5 can also be seen as the successor of the previously mentioned topologies illustrated in Figure 3 and Figure 4.

As with the previous converters the main benefit of the M^2LC topology is its modular nature and the linear increase in the component count with the increase in the number

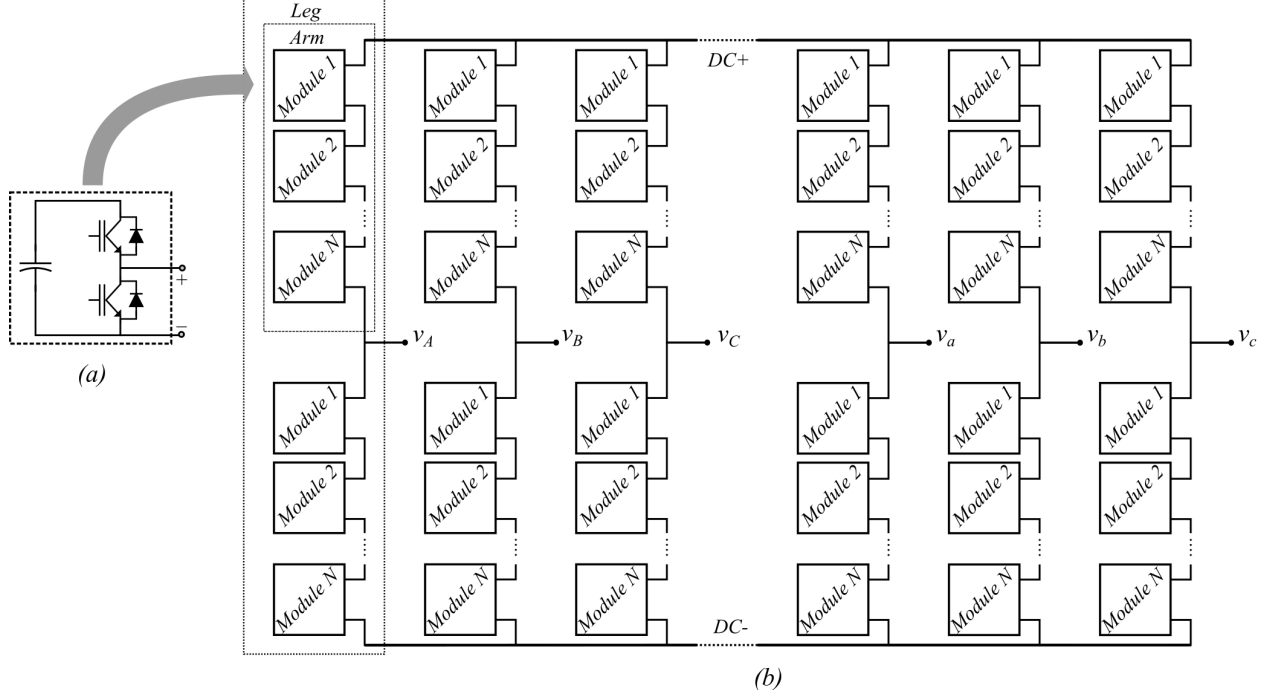


Figure 5: Back-to-back structure implemented with MMC converters with the DC bus proposed by Marquardt et al. and named Modular MultiLevel Converter (M^2LC) by the authors. (a) - Half bridge module (cell) structure. (b) - MMC back to back structure showing the substructures commonly called "converter arm" and "converter leg" in MMC terminology.

of levels. Although the idea seems very similar to the previously mentioned Cascaded H-Bridge converter and Multilevel Cascade Inverter given in figures 3 and 4, it has a number of important differences:

- M^2LC topology allows the simplest module topology (half-bridge + capacitor)
- M^2LC topology has single, common high-voltage DC bus.
- M^2LC topology uses half bridge modules instead of H-bridge modules common for most stacked or cascaded converters.
- M^2LC does not have a DC bus supply for individual modules, but can be supplied through the high voltage DC bus.

- M^2LC topology was the first modular topology of its kind to be suitable for high and medium voltage back to back conversion systems and operation in all four PQ quadrants without the use of transformer of any kind.

Since the early 2000s acronym MMC has become the common term in the literature for many variations of the modular multilevel topology including M^2LC and cascade modular multilevel converter mentioned above [27], [35]. It may be argued that there is a level of confusion regarding the topology names and naming conventions in the literature dealing with this topic. Different topologies sometimes share the same name and same or very similar configurations have been referred under different names. For example, same or very similar configurations can be found in the literature under different names like: M^2LC , double star MMC configuration, M2C, MMC configuration with a DC bus, Chainlink, etc. [25], [27], [36], [37].

The line between MMC and CHB seems to be particularly vague as well. For example, many authors consider converter from Figure 4 and similar structures a part of MMC family if they do not have external supplies to the DC bus of the modules. If every module DC bus has external power supply, it is usually considered to be a CHB converter. The converter from Figure 5 is considered MMC even if the modules have independent external supplies. Classification and naming convention attempt was given in a publication by Akagi [38]. In this publication the author classified most of the mentioned topologies under the name - Modular Multilevel Cascaded Converter (MMCC).

Over the years the topic known as MMC has become very broad and includes dozens of various multilevel topologies with different practical importance and field of application.

Furthermore, the converter itself has become integrated with the higher level system to such extent that it cannot be treated or analyzed on its own. Excellent example of this can be found in wind and solar applications of the MMC topology. The following sections will attempt to outline at least some of the directions the above mentioned converters have evolved to.

2.2 MMC Applications and Modifications

MMC topology and its variations have been investigated in the literature for many applications mostly for high power, medium and high voltage systems. Applications can be divided into several groups where each group introduces a distinctive characteristic and some modification to the MMC topology. MMC applications can therefore be classified as:

- Grid support applications including various Static Synchronous Compensator (STATCOM) systems
- Grid inter-tie applications
- HVDC applications
- Medium voltage motor drive applications
- DC/DC conversion systems
- Converters solar PV systems
- Converters for wind energy systems
- Energy storage applications

- Other applications

2.2.1 Grid Support Applications

The idea of using the MMC topology for grid support device and STATCOM applications has been extensively analyzed in the available literature. One of the earliest modular topologies was proposed by Peng *et al.* for the use in a medium voltage static VAr generation system as mentioned in previous section [30]. Akagy *et al.* pointed out early on that the MMC topology allows design of medium and high voltage STATCOMs without the use of a step-up transformers. This makes high power medium voltage systems of this kind lighter, smaller, cheaper and more efficient in most cases [39]. Ota *et al.* further extended the research of the STATCOM applied MMCs with the control system analysis, different modulation techniques and balancing algorithms that allow improved current Total Harmonic Distortion (THD), current control and capacitor voltage balancing [40], [41].

The application of the MMC converter topology for grid support inverters, STATCOMs and similar applications usually does not require an external supply, but only internal storage. As a consequence, most of these systems do not have DC bus and have similar structure as the converters shown in Figure 4.

2.2.2 Grid Inter-tie Applications

The flexibility of the MMC structure allowed AC to AC conversion systems and grid inter-tie converters to evolve in a couple of directions. One line of converters uses back-to-back MMC structure with the common DC bus and the other uses AC to AC MMC arrangement converter without the DC bus.

The original converter structure with the DC bus, introduced by Marquardt *et al.* and shown in Figure 5, was proposed for a three-phase to three-phase grid inter-tie system [34]. Similar system with more levels was later analyzed by Lesnicar and Marquardt for a three-phase to single-phase grid inter-tie [25]. This configuration with the DC bus can easily be extended to link two multi-phase systems with arbitrary number of phases.

Glinka and Marquardt also showed that the same MMC structure (or M^2LC as these authors call it) can be used for the AC to AC power conversion if the DC terminals are connected to the AC supply eliminating the DC bus in the system as shown in Figure 6 [26].

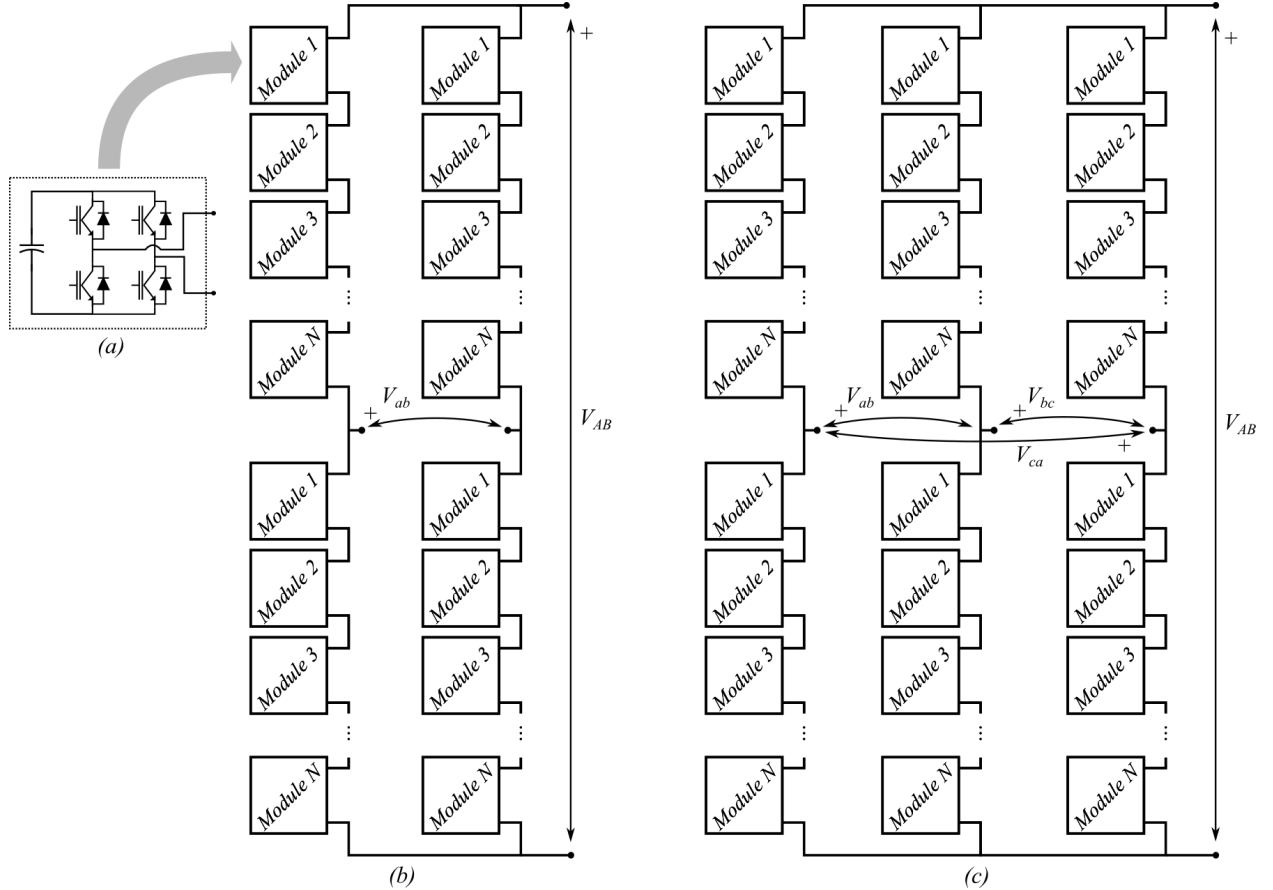


Figure 6: Structure of the AC to AC MMC topology without the DC bus proposed by Glinka and Marquardt. (a) - Module (cell) structure. (b) - Single phase AC to AC converter. (c) - MMC 3-phase AC to AC structure.

MMC converters without the DC bus proposed by Glinka and Marquardt shown in Figure 6 allows connections between single-phase and multi-phase systems but not between two multi-phase systems. Compared to the structure in Figure 5 for the same application they have significantly less modules but are more difficult to analyze and control. Furthermore, this AC to AC topology requires full-bridge switching arrangement in each module which could make the total semiconductor switch count equal or even higher for the same number of levels.

Structure that allows connection between two three-phase systems is shown in Figure 7 and was introduced much later in 2011 by Baruschka and Mertens as a "Hexverter" topology [2]. This converter has half of the module count compared to the three-phase back-to-back structure illustrated in Figure 5 with the same number of levels. While the capacitor and module count is half of the converter in Figure 5, Hexverter still requires full bridge modules making the equivalent semiconductor count equal.

2.2.3 HVDC Applications

Modular nature and series connection of modules makes the MMC topology suitable for high voltage power conversion systems commonly found in High Voltage Direct Current (HVDC) transmission applications. Besides bulk power transmission over long distances for conventional power grid and power production, HVDC systems also found their application in modern renewable energy power production system like large off-shore wind farms and remote solar fields.

First commercial HVDC transmission systems appeared in 1950s as a result of advancements in power electronics and increasing demand for electric power and long distance trans-

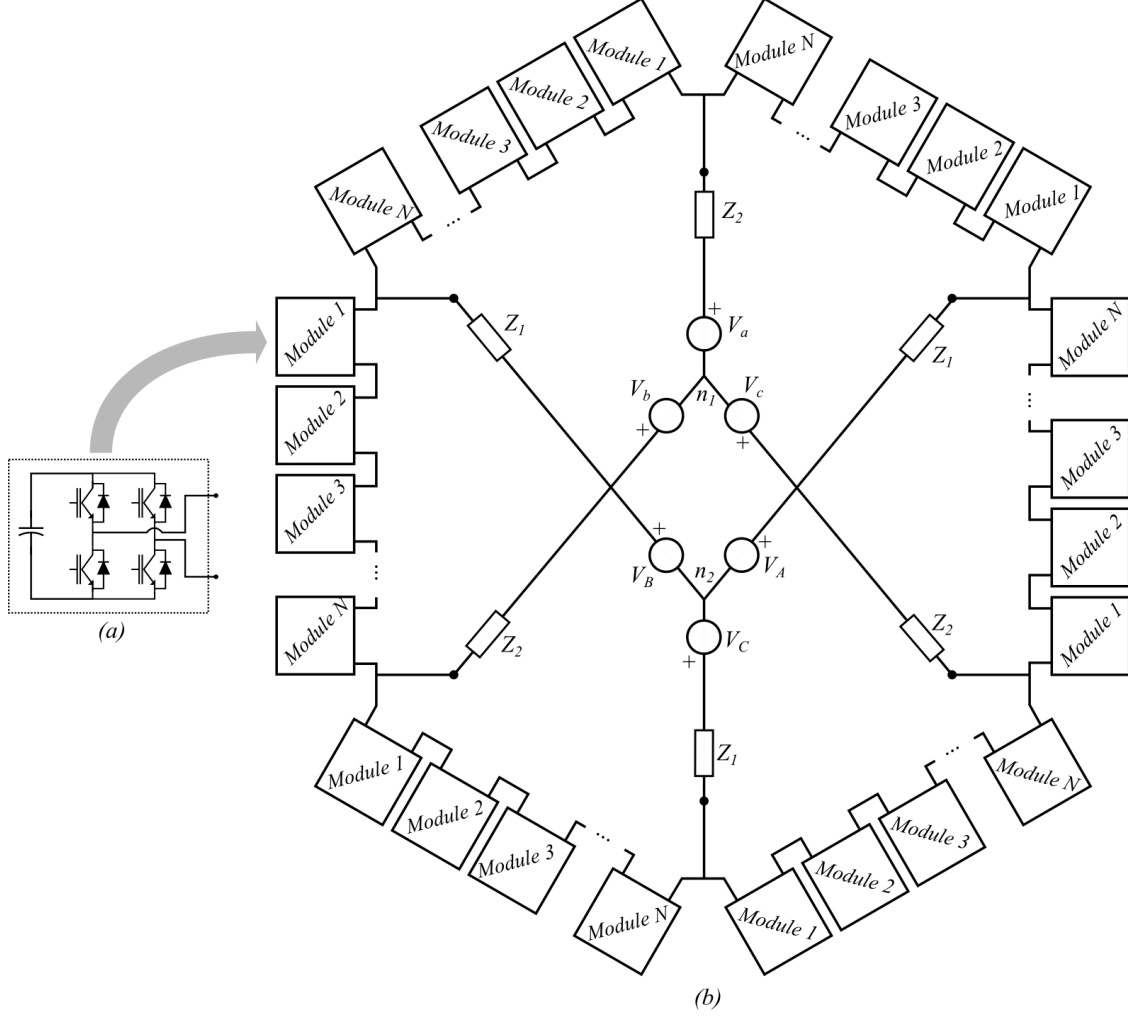


Figure 7: MMC based 3-phase AC to AC converter structure known as Hexverter [2].

mission systems. These early HVDC systems were supplied by high power high voltage two level converters implemented with mercury-arc vacuum tubes. To achieve the voltage rating mercury-arc tubes were usually connected in series to create HVDC switches, or valves as they were called at the time that could operate at voltages of hundreds of kilo-Volts. With the introduction of semiconductor switches and the invention of thyristors in 1970s, mercury-arc tubes in the HVDC converter valves were replaced by a rather complicated series-parallel connection of large number of thyristors [42]. To facilitate proper high voltage operation of the entire switching structure thyristors had to be protected and balanced by the special

snubber circuits [43], [44]. Finally in 2010 HVDC valves were replaced by MMC converter arms, implemented with Insulated Gate Bipolar Transistor (IGBT) semiconductor switches. In this way the two-level converter topology was replaced with the multilevel MMC structure shown in Figure 5 [45].

MMC topology offers better power quality and higher HVDC conversion efficiency than conventional two level converters as demonstrated in a paper by Allebrod *et al.* [46]. Furthermore, high number of switches in a two level HVDC converters makes the MMC approach comparable in complexity and cost. As a result, relatively expensive and complicated MMC topology found its first commercial implementation in the area of HVDC power transmission systems. The first large commercial MMC system and the first MMC based HVDC transmission systems was commissioned in the Bay of San Francisco, between San Francisco and Pittsburgh CA in 2010. The system is rated at 400MVA with $216 + 16$ modules (cells) per arm and DC transmission voltage of $\pm 200\text{kV}$ [27], [47], [45].

HVDC transmission systems usually carry significant power to or from the local power systems. As a result, outages can have serious negative effects on economy and grid stability. In general, when it comes to large power transmission systems besides efficiency and power quality, reliability is among the most important aspects of the system. Fault management and fault ride through is therefore a highly important topic in the field of MMC based HVDC transmission systems and has inspired a great number of publications and MMC topology modifications.

MMC topology with the DC bus given of Figure 5-(b) is vulnerable to the DC faults if used with the modules shown in Figure 5-(a). In case of the DC fault, series connection of the anti-parallel diodes will rectify the AC input and will feed the DC fault arc until

the entire converter is disconnected from the AC side supply or until the diodes fail. To avoid over sizing of the anti-parallel diodes, high current rating bypass thyristor shown as $S3$ in Figure 8-(a) is usually added to each module. This high current thyristor protects the converter from damage until the AC side circuit breakers act and disconnects the entire system from the supply [48]. If the system has to be disconnected from the grid and powered down, each fault can cause a significant downtime. As a result, this kind of MMC converters systems are not suitable for overhead DC transmission systems where faults may be frequent and intermittent.

A solution that makes the MMC converters more suitable for overhead transmission was proposed by Li *et al.* [3]. The authors proposed a minimal modification to the module topology shown in Figure 8-(b) that allows quick recovery from non-permanent DC faults. Added thyristors $S3$ and $S4$ protect the converter switches from high fault currents, shunt the DC bus and allow the fault arc to extinguish. If the fault persists, the converter and the system still need to be disconnected from the AC grid supply.

Another solution that makes the MMC converter shown in Figure 5-(b) and the HVDC transmission system completely fault tolerant and fault ride through capable is analyzed by Kontos *et al.* [49]. In this case authors used full-bridge modules as shown in Figure 9-(a) instead of half bridge modules given in Figure 5-(a). full-bridge module facilitates the control over AC and DC side currents and makes the MMC converter AC and DC fault tolerant. The price is highly reduced efficiency as the current path contains twice as many semiconductor switches.

To mitigate the problem of decreased efficiency a number of module variations were proposed over the last decade. The guiding idea behind most of these modifications was to

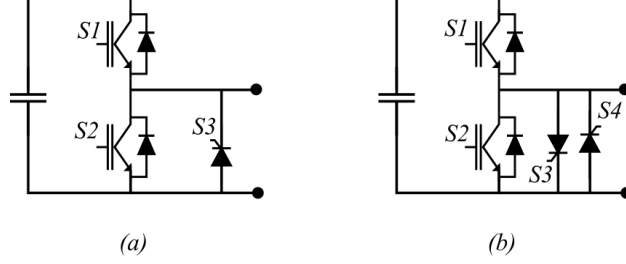


Figure 8: Simple fault capable modules. (a) - Half bridge module with the fault bypass thyristor. (b) - Fast fault recovery module modification proposed by Li et al. [3]

combine multiple modules into one and eliminate the redundant switches while maintaining the fault tolerant capability. This reduces the losses caused by the increased number of switches in the current path and effectively creates fault tolerant multilevel modules for the MMC topology.

One of the first such modules was proposed by Marquardt and was named clamp-double module. This module combines two half bridge modules into one. Compared to the equivalent connection of half-bridge modules, the losses are increased by one additional switch per two modules shown as $S5$ in Figure 9-(b) [50]. Switch $S5$ is normally ON and is turned OFF only during the fault handling situations. When the $S5$ is OFF, the current path is not symmetric during the positive and negative half cycle of the current, which means that the blocking voltages is not symmetric during fault handling. The module can block full DC bus amplitude for negative half cycle of the input current and only half for the positive [51].

Module topology in Figure 9-(c) was proposed by Li *et al.* and can block full DC voltage for positive and negative current half cycle. The module has one additional switch $S6$ and higher losses than clamp-double module. Switches $S5$ and $S6$ are always ON in normal operation [52].

Topology in Figure 9-(d) was proposed by Zhang and Zhao and can also block the full

DC bus voltage on the input but requires switch $S5$ and diode $D1$ with doubled voltage ratings [53]. For this module, switch $S5$ is always ON in normal operation.

Module in Figure 9-(e) was named T-Type and was proposed by Zhao *et al.* as an efficiency improvement to the clamp-double module topology given in Figure 9-(b) [54]. As can be seen from figures 9-(b) and 9-(e), T-Type module topology has one diode less than the clamp-double module but suffers from the same asymmetric blocking voltage for positive and negative half cycle.

A number of other arrangements were also proposed that were based on combining a number of full bridge and half bridge modules into one. These modules are sometimes called mixed modules. The simplest one is shown in Figure 9-(f) and covered in a publication by Adam *et al.* [55].

Other more complicated module topologies are also possible and were proposed in the available literature but they usually do not bring any significant advantage compared to using full bridge modules for the MMC converter structure shown in Figure 5-(b). A survey of some of the fault tolerant MMC module topologies that were proposed up to 2015 can be found in a publication by Nami *et al.* [56].

2.2.4 Medium Voltage Drives

One of the predecessors of the MMC topology, mentioned in Section 2.1 and shown in Figure 3, was proposed by Hammond for medium voltage drives [1]. For this converter each individual module has its own supply, which is the main feature that separates this converter from the MMC family of converters. Without a supply for each module, DC bus voltage must be maintained by the module internal capacitance. As the current flowing through the

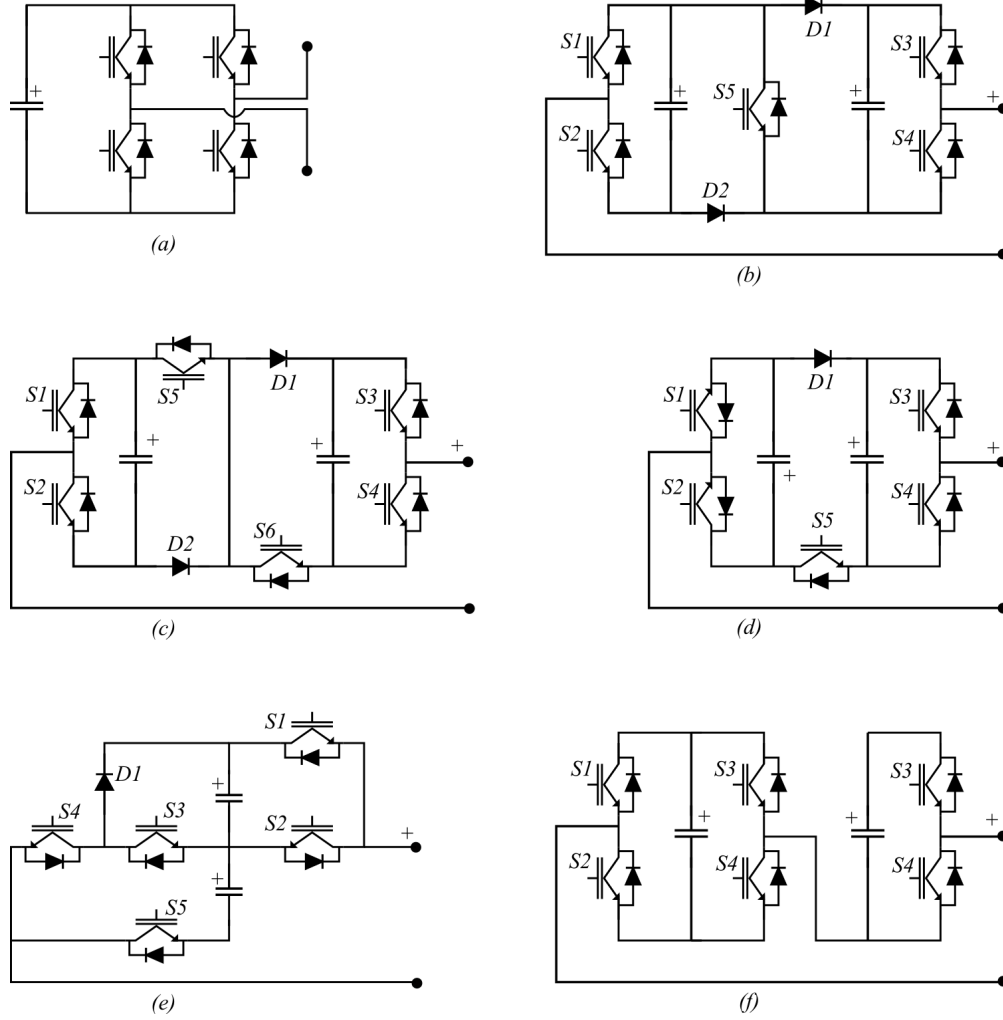


Figure 9: Some of the fault tolerant module topologies: (a) - Full-bridge module. (b) - Clamp-double module. (c) - Three-level module. (d) - Series connected double module. (e) - T-Type module. (f) - Mixed module.

module capacitors have strong first and second harmonics for the MMC converter topologies, maintaining DC bus voltage relatively constant at lower operating frequencies requires higher capacitance in each module.

Frequency dependent capacitance requirement for module DC bus creates a number of challenges for the application of MMC converters in variable speed drives. Capacitor voltage stability at low speed and standstill operation and consequently the stability of the entire converter operation is a serious issue that was initially described by Antonopoulos *et al.* back

in 2009 [57]. Year later in a publication by Hagiwara *et al.* it was pointed out that stable operation of the MMC drive requires capacitor sizing for the worst case of the particular application and torque limiting control at lower operating frequencies in order to avoid module overvoltage problems, especially during the machine startup [58].

One of the first control system based solutions that allows stable operation of the MMC drive through the entire range of frequencies was proposed by Antonopoulos *et al.* in 2010 [59]. The proposed control algorithm adjusts output reference voltages for the converter arms in order to control the total energy stored in the converter leg and to balance the energy between upper and lower arm. As a consequence, DC bus voltage in each module is maintained within limits. The trade-off of this approach is the introduction of, so called, circulating currents in order to move the power between arms of the converter leg. Circulating currents flowing between converter leg and the DC bus or between two converter legs are unwanted in normal operation as they introduce additional losses and do not contribute to the converter output. In fact, a significant number of publications are dedicated to the suppression controllers for circulating currents in HVDC and grid connected MMC converters [60], [61], [62]. The circulating current control for MMC based drives helps with capacitor voltage imbalances but it reduces the output power capability of the drive and torque production at start-up and low frequencies. As a consequence, instead of capacitor banks the semiconductors have to be over-sized.

Circulating current control has been covered extensively in the literature. For example, the circulating current control has been extended for the $\alpha\beta 0$ frame of reference and described in more detail by Kolb *et al.* [63]. The same concept was used by Baruschka *et al.* to help balance the module voltages for the drives application of the MMC based AC to AC Hexverter

topology mentioned in previous section and illustrated in Figure 7 [64]. The application of the circulating current control in conjunction with space vector modulation for the MMC based drive was described by Brando *et al.* [65].

Another interesting approach that does not require any modifications to the basic MMC topology illustrated in Figure 5 but modifies the approach to the structure control in order to allow stable low frequency operation was proposed by Mertens and Kucka in 2016 [66]. This approach treats the MMC structure as a two level converter. The arms of the converter are treated as high voltage switches and the output voltage is formed by effective two level modulation. In this mode of operation modules and module DC bus capacitor banks serve only during the switching transition and have a much higher base switching frequency than what is observed by the effective two level output. Therefore, for the most of the waveform period the current flows only through the semiconductors completely bypassing the module DC bus capacitors. This approach does, however, require fairly stiff high voltage DC bus. In cases where a back-to-back MMC structure is used, the DC bus is maintained again by the totality of arm module capacitances in the circuit at each particular instance.

Most of the publications that deal with MMC applications to electric drives focus on the control system investigations for the already proposed MMC topology variations. Although not as nearly as abundant in new ideas, another line of solutions to the problem of low frequency operation is the modification of the MMC converter structure. One example of such approach is given by Du *et al.* In this approach the authors introduced a bypass arm in each leg of the MMC converter that will help in balancing the capacitor energies within the converter [67].

2.2.5 DC to DC Conversion Systems

Several MMC topology applications and modifications have been inspired by the medium and high voltage DC to DC power converters. These converters are mostly investigated for the application in Medium Voltage Direct Current (MVDC) transmission systems which are gaining in research interest and popularity with the development of diversified power sources and power conversion systems.

While HVDC transmission systems have been in utilization for a while, MVDC transmission is not yet that common. However, it has been shown in the literature that MVDC transmission and distribution systems may have a number of benefits for the applications where the source naturally has a DC output, for smaller isolated power systems with highly diversified sources and loads requiring a number of power conversion stages and for the systems that have large number of interconnected power electronic converters. These applications include renewable energy systems, some microgrid applications, industrial power supply systems, naval power systems, electric trains, and others [68], [69], [70].

Dual Active Bridge (DAB) arrangement is the most straightforward way to implement a structure like MMC in a DC to DC converter. A number of researchers covered this topic over the last decade. In one of the earlier publications, Kenzelmann *et al.* investigated isolated DC to DC converter that uses DAB equivalent topology with H-bridge switching structure implemented with MMC converter legs as shown in Figure 10. The converter can be optimized for high voltage and high frequencies, which can significantly reduce the size of the MMC capacitor banks and the isolation transformer $T1$. Authors investigated this converter structure for fault handling in HVDC systems. Besides galvanic isolation

this converter offers a level of protection from the faults on the secondary DC side of the structure. In case of a fault the DAB converter can be turned off, which completely blocks the power flow and collapses the DC voltage quickly until the fault is cleared [71].

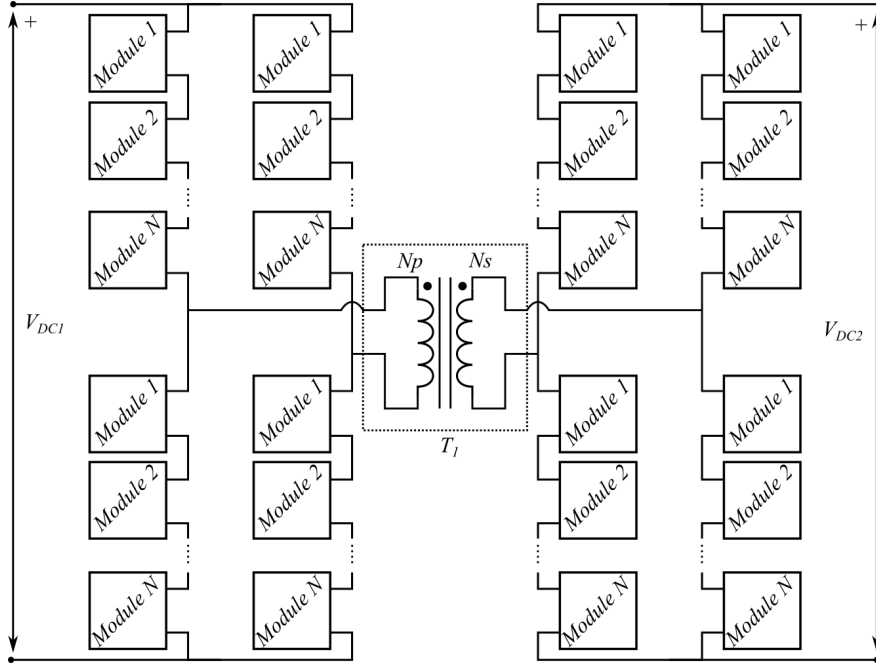


Figure 10: Isolated dual active bridge DC to DC converter implemented with MMC structures.

Depending on the system size, the approach of turning the converter off may cause long restart times. This may be unwanted for the systems that need strict fault ride through requirements. To solve this problem, Jovicic and Zhang investigated the control system for the MMC based 3-phase dual active bridge converter. The authors analyzed the behavior of the system under fault conditions and proposed a control system that will allow fast recovery of the power converter and active control of the fault current limits in case of DC faults [72].

Besides the isolated dual active bridge DC to DC converter, non-isolated versions have been proposed in the literature as well. Dual active bridge linked with LCL filter element has been proposed by Wang *et al.* [73]. Other topologies that use MMC structures have also been

investigated. In most cases these topologies were derived from Buck, Boost, Flyback or other standard topologies. The semiconductor switches for the standard topologies can be replaced by the MMC leg that serves as a high voltage multilevel switching structure [74], [75].

2.2.6 Applications Solar PV Systems

Application of MMC for solar PV converters has two main directions proposed in the available literature. First and the most straightforward approach is to use the MMC as a regular grid connected inverter with a solar field connected to the converter DC bus [76], [77]. Applicable standards limit the maximum DC bus voltage of the solar converters to $1.5kV$. This seriously limits the benefits obtainable by using the MMC converter topology and makes other simpler topologies more attractive.

Second approach uses MMC based grid tie converters for solar PV systems that integrate solar panels directly in the DC bus of the MMC modules as shown in Figure 11-(a). This approach was analyzed by Stringfellow *et al.* [78]. Although very similar in structure, the configuration from Figure 11-(b) is considered to be a CHB converter [79].

Integration of PV panels in the MMC modules offers some advantages but also has several serious drawbacks. The main advantage of this approach, advocated throughout literature, lies in finer maximum power point tracking capability. The converter interfaces with a solar panel strings or even individual panels as opposed to the interface with the entire solar field. This enables finer operating point control for each solar panel and alleviates efficiency problems related with partial shading and temperature differences across the PV field [80], [80].

The approach of connecting PV panels directly to the MMC modules has a number of

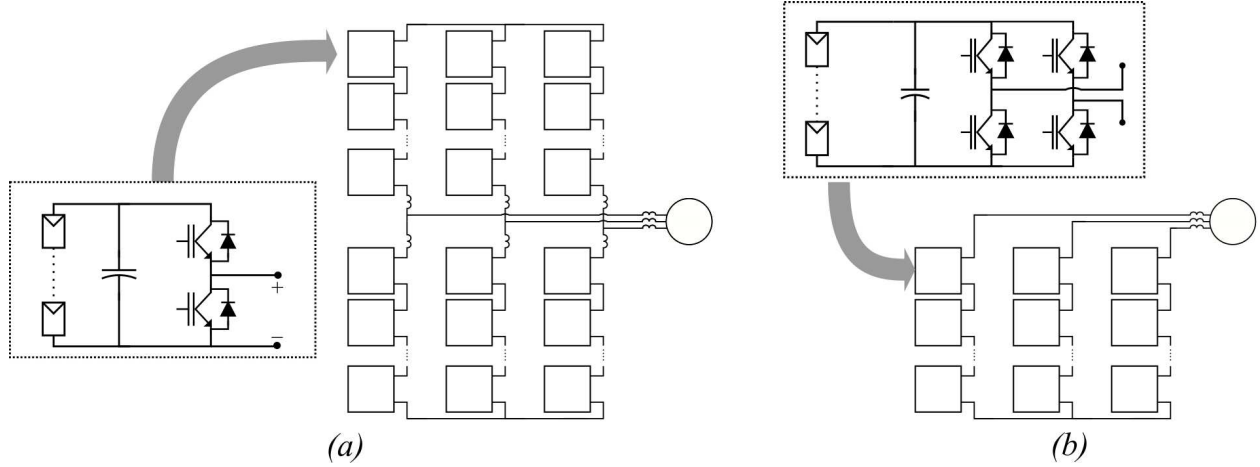


Figure 11: (a) - Integration of solar panels directly in the DC bus of the MMC module. (b) - Integration of the solar panels into the modules of CHB converter.

drawbacks and limitations that are directly linked to the nature of the MMC topology:

- The maximum system voltage is usually lower than 1.5kV for solar PV systems to accommodate for the panel isolation ratings and applicable standards. The fact that the converter cannot be implemented for medium or high voltage defeats the purpose of using the MMC topology to some extent. The use of parallel modular topologies seems much more appropriate for this application.
- Panel to ground voltage is alternating in this arrangement, which can cause undesired ground leakage currents. To solve this problem an isolation transformer is necessary. The isolation transformer can be on the grid connection, or in an isolated DC to DC converter integrated in every module of the MMC converter as proposed by Perez *et al.* [81].
- Low maximum system voltage limits the number of levels and/or the MMC module DC voltage, which in turn may increase losses and reduce the system efficiency compared to the more conventional grid tie converters.

- The current flowing through the module DC bus of the MMC converter has a dominant AC current component. If left unfiltered, this may additionally heat the PV panels, which reduces the efficiency and may cause damage.

2.2.7 Converters for Wind Energy Systems

The first interests for the MMC topology application in wind energy systems appeared after the MMC has been recognized as an ideal solution for HVDC transmission systems. Remote offshore wind farms require long distance transmission systems to the main land electric grid and it may be beneficial to move to HVDC transmission in some cases. The same reasoning can be applied in cases when the onshore wind farms are far from the points of power consumption.

The practical limits for the High Voltage Alternating Current (HVAC) power transmission from a remote wind farms and the point when it may be more beneficial to use HVDC transmission for offshore wind farms was analyzed by Sharma *et al.* [82]. The authors compared the losses in the system and analyzed the impact of the cable and its length on the conventional HVAC and the MMC based HVDC transmission system used for long distance power transmission from an offshore wind farm. The conclusion was that the MMC based HVDC systems becomes more efficient for the exemplified 180MW wind farm if the transmission line length exceeds 100km.

Nanhui project in China is one of the first large scale implementations of MMC converter topology for wind energy systems. In this case the MMC converter was used for the HVDC transmission link between the on shore wind farm and the rest of the power system. The system consists of 11 wind turbines connected to the electric grid through an AC transmission

line and 8km long HVDC cable powered by the MMC converters. Description of the system can be found in the publication by Jie *et al.* [83]. The authors analyzed the operation of the system and described its features including reactive power support and fault handling.

Besides in the point to point HVDC transmission systems the MMC converter has also been proposed for the multi-terminal DC networks for the power transmission and interconnection of wind turbines in a wind park. A system of this type was analyzed by Wenig *et al.* [84].

Another interesting application of the MMC topology for wind energy systems was proposed by Zhang *et al.* In this case wind turbines are integrated into individual MMC modules making the entire wind park one large and fairly complicated power converter. The potential issues related to the practical implementation of the system as large as this one were not mentioned in the paper [85].

Application of the MMC back to back structure similar to the one shown in Figure 5-(b) was also considered for the application in wind energy systems. Wang *et al.* used this structure to connect a wind turbine to the medium voltage AC grid [86]. The authors also proposed a solution for low speed operation and low voltage ride through. For low speed operation they used circulating current injection, which is a widely accepted solution for this problem. For low voltage ride through they used braking choppers distributed throughout modules.

2.2.8 Energy storage applications

The MMC topology can be suitable for bringing energy storage to medium and high voltage systems. This seems particularly true for battery, supercapacitors and ultracapacitors storage

technologies. DC outputs from these storage systems are hard to protect from faults once the total voltage of the stacked storage elements exceeds 1000V due to the lack of convenient fusing elements above this voltage level. If the MMC topology is properly modified, energy storage systems can be distributed throughout the converter modules. In this way the maximum voltage level for the energy storage systems remains at the maximum voltage of the individual module DC bus, which can be designed to be well below 1000V. This means that the storage system can still be protected using common low voltage fusing systems or conventional DC circuit breakers while achieving medium or high voltage levels of the entire energy storage/power converter system. The fault protection and fault handling capabilities on the high voltage terminal points can be designed into the converter topology itself, which is not overly complicated for the MMC family of converters, as shown in Section 2.2.3.

Modular multilevel systems with energy storage system integrated into individual modules have appeared in the literature in the last decade and have been proposed for various applications. For example, Kawakami *et al.* used a form of cascaded H-bridge multilevel topology which they referred to as MMCC to integrate battery energy storage system into an inverter structure [4]. Simplified block diagram of the proposed system topology is shown in Figure 12. The investigation of this energy storage/inverter structure was the result of an effort to solve the power quality problems caused by the intermittency of the solar PV energy resources. Large energy storage system that can be implemented using this form of power converter can be tied to the medium or high voltage network and used for power smoothing, load shifting, frequency support and other ancillary services in order to improve stability of the power grid.

As can be seen from Figure 12, battery energy storage system is integrated directly into

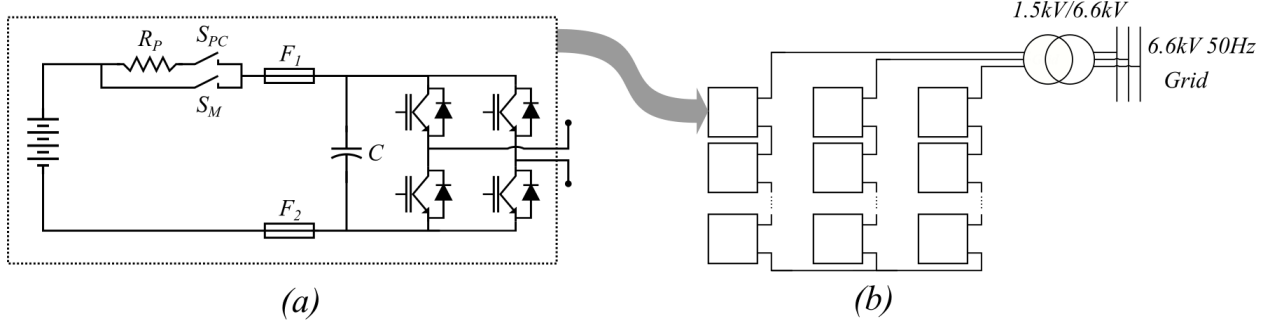


Figure 12: CHB based energy storage system proposed by Kawakami *et al.* [4]. (a) - Integration of battery energy storage directly in the DC bus of the MMC module. R_p , S_{PC} and S_M make the module DC bus precharge circuit. F_1 and F_2 are standard low voltage DC fuses. (b) - Overall system topology named MMCC by the authors.

the DC bus of each MMCC module through a precharge and fusing circuitry. The storage system peak DC voltage can be below 400V, allowing the use of conventional DC fuses while the AC output voltage of the system can easily exceed 1.5kV. The precharge circuit allows the converter to have a quick black start. Module DC buses can be precharged at once from the storage and the complicated sequential precharge for each module can be avoided.

MMC structure with DC bus, also known as M^2LC , has also been investigated for the energy storage systems. For this converter topology the modules are usually connected through half bridge switching structures. Therefore, the current flowing through the module DC bus and energy storage elements has higher AC component. For this reason, authors usually chose to connect the energy storage system to the module DC bus through a DC to DC converter as shown in Figure 13. In most cases the DC to DC converter topology of choice is buck-boost. For example, Vasiladiotis and Rufer have investigate the balancing algorithm for this form of distributed energy storage system [87]. Similar system has been proposed by Trintis *et al.* for the use as an UPS system for future HVDC meshed grids [88]. The authors proposed Buck-Boost converter for the non-isolated system and DAB converter

in the case when the batteries need to be isolated from the rest of the system.

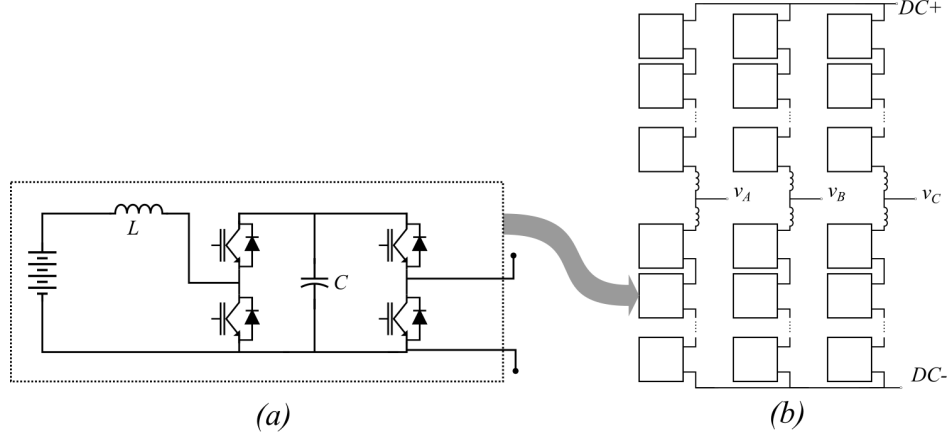


Figure 13: M^2LC based energy storage system with the energy storage integrated into the module CD bus through a DC to DC converter. (a) - Integration of battery energy storage in the DC bus of the converter module. (b) - Overall system topology (3-phase case).

Although the topology shown in Figure 13 is more common, authors also considered using the direct connection of energy storage system into the module DC bus for the M^2LC converter structure as shown in Figure 14. Zhang *et al.* have proposed such system for the power smoothing application in the wind energy system and investigated the optimal energy storage operation modes for this application [89].

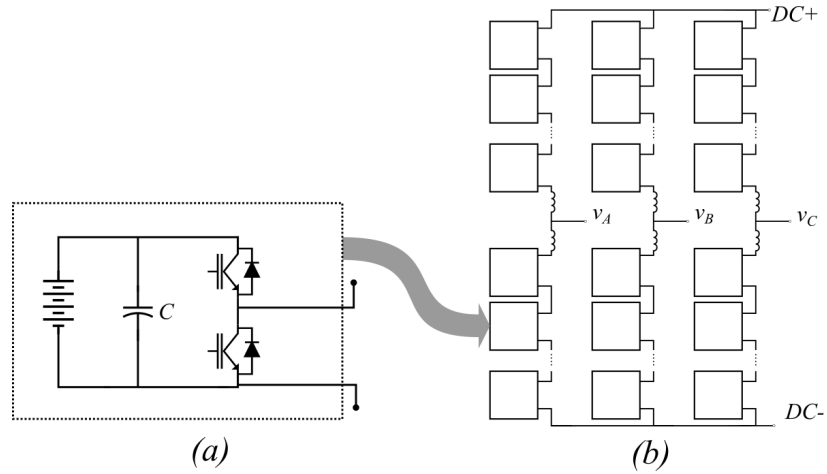


Figure 14: M^2LC based energy storage system with the energy storage integrated directly into the module DC bus. (a) - Integration of battery energy storage in the DC bus of the converter module. (b) - Overall system topology (3-phase case).

Another way of integrating energy storage into the M^2LC structure is through a passive filter network. Wersland *et al.* concluded that the use of fairly complicated passive resonant filter for this purpose may be attractive in cases when high reliability of the system is required [90].

A large part of the current text will also deal with the passive filtering design and component sizing for the energy storage application of the MMC converter. Summarized investigation of the filter and energy storage sizing from the current text can also be found in [91].

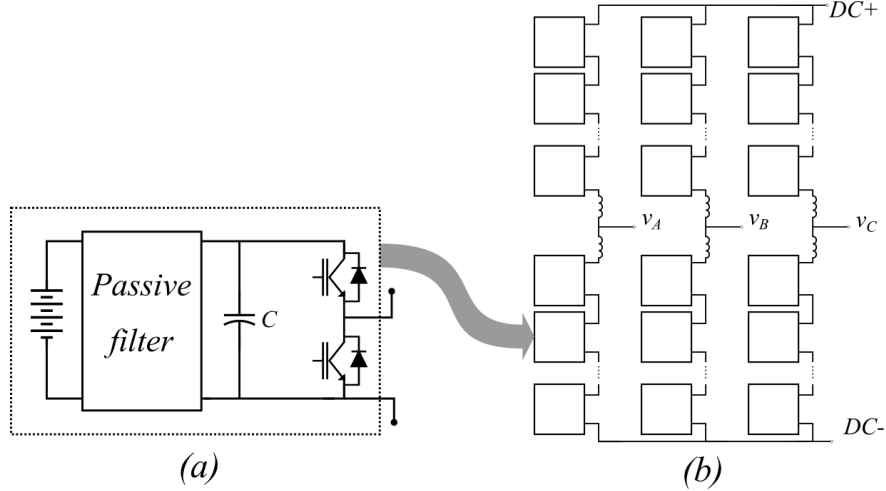


Figure 15: M^2LC based energy storage system with the energy storage integrated into the module DC bus through a passive filter. (a) - Integration of battery energy storage in the DC bus of the converter module. (b) - Overall system topology (3-phase case).

MMC topology has been investigated in other arrangements for the energy storage systems. Interesting example of the MMC topology application for the energy storage systems was proposed by Hagiwara and Akagi. The authors used MMC based isolated push pull converter to connect a battery string to the power grid [92]. Another interesting application of the MMC-like topology for electric vehicles storage systems was proposed by Zheng *et al.* The authors placed one battery cell in each converter module and used the converter

structure to improve balancing, control the charging of the batteries and even provide a single phase AC output to drive the electric motor [93].

2.3 Renewable Energy, Energy Storage and Grid Tie Codes

Previous sections outline evolution of the MMC topology through applications and research publications. As can be seen from the limited sample of literature publications presented in the previous sections MMC topology has highly diverse application base and is convenient when topology modifications are necessary to adjust the structure of the converter for a specific application.

The following section will outline the evolution of grid connection codes that are the reason for the increased interest for the integration of wind energy systems and energy storage. Furthermore, from the text below it may be inferred that integrating energy storage to any renewable energy generator or large grid connected system might be of interest in the future.

2.3.1 Renewable Energy and Grid Connection Code

Renewable energy resources like wind and solar PV have a significant and uncontrollable variability over time. Although long time variability can be forecasted to some extent, short time variations are usually completely random and cannot be predicted. Unpredictable and variable energy availability creates difficulties for the utility grid energy dispatching and can, under extreme conditions, lead to grid instabilities.

Control systems used for the energy harvesting from wind and solar radiation in most cases aim to extract maximum amount of energy available at any given time. As a result,

the power production can swing fairly quickly from zero to full rated power. In the past these swings were treated by the utility companies as if they were caused by the changes in virtual loads. Depending on the relative size of the renewable energy source, these sudden variations can have different levels of negative effects on the utility grid. The effect can go from minimal voltage or frequency variations to large changes in frequency and voltage that can cause entire power plants to lose grid connection. Once this happens it can cause chain of generator disconnections that can affect large zones of a power grid and cause serious power outages [94] [95].

Increase in the percentage of power generated by variable power renewable energy systems like wind and solar PV inspired the evolution of more strict generator interconnection standards and requirements. Federal Energy Regulatory Commission (FERC) orders related to renewable energy or variable energy sources can serve as a source of information about rather complicated interaction between free energy market, incentives for alternative (renewable energy sources) and the evolution of grid connection requirements for renewable energy sources.

A number of FERC orders for generator interconnection procedures play a particularly interesting role in the development of the renewable energy in the United States. These orders were issued to promote open market for renewable energy systems and to make the power grid and network operators more welcoming to the renewable energy power plants and their distinctive properties, most of all their variable and unpredictable power output. At the same time the requirements for the renewable systems themselves evolved from almost no regulation regarding the power quality to the requirements for the Low Voltage Ride Through (LVRT), reactive power and frequency support.

Since FERC orders 888 & 889, renewable energy power plants were allowed to use transmission networks and sell the energy on the open market. The same order allowed the transmission providers to charge transmission penalty fees to the power plants that deviate more than 1.5% from their scheduled power production. This penalty was almost unavoidable for renewable energy power plants and forced them to sell power to the market that could tolerate the deviations. FERC order 2000 mandated real time balancing that allowed minute to minute power dispatch and enabled higher penetration of renewables. FERC order 2003 finally made no distinction between renewable energy and conventional power generators. This caused large increase in renewable energy generators and prompted a revision for the interconnection procedures in FERC order 661, which required grid utility companies to provide standard requirements for the connection of large wind generator units. The order addressed LVRT and Supervisory Control and Data Acquisition (SCADA) requirements for wind energy systems as well. Finally, in 2016 FERC order 827 withdraw the exemption of the wind generators to provide reactive power support they had since 2003 [96].

A number of FERC orders give special treatment and incentives to the systems that can provide ancillary services and support grid stability. For example, FERC order 755 promotes fast response for the frequency regulation services and encourages "pay for performance" approach for the service providers [97]. Order 819 allowed the sale of Primary Frequency Response (PFR) on the market-based rates. This served as an incentive for the systems that will support the grid stability and allow higher penetration of variable power renewable energy power plants [98].

2.3.2 Energy Storage and Grid Connection Codes

Energy storage systems received special treatment in 2013 with FERC order 784. This order focuses on ancillary service providers and the way the ancillary services can be procured. The order promotes precision and speed of the resource providing the service and regulates energy storage systems as premium service providers. With this order renewable generators are allowed to provide ancillary services as well [99].

Adding energy storage to the renewable energy power plants can improve the power quality from the renewable energy generators. If the energy storage is large enough it can even make the renewable energy power plant dispatch-able [100]. As a result, from the new grid connection codes mentioned above, integrating energy storage into the renewable energy power plant can make the entire system more profitable. Besides using the energy storage to improve the output power quality and satisfy the grid connection requirements, it can be used to provide ancillary services as well. As a result, if designed properly, future renewable energy systems can serve as grid stabilizers rather than grid stability risk factors.

The benefits from integrating energy storage into renewable energy system can be observed from two sides. From the renewable generator standpoint, integrated energy storage provides a number of capabilities to the integrated system, including power smoothing, ancillary support services and possibly even dispatch-ability. These capabilities can greatly improve the usability of the integrated renewable generation/storage system, the quality and market value of the energy it delivers.

From the energy storage standpoint, appropriate integration with modern renewable energy generators can provide shared high performance grid connection inverter, controls

and protection devices that can lower the overall cost of the storage system deployment and usage.

2.4 Wind Energy Systems and Energy Storage

Short outline of the existing approaches for the integration of wind energy systems and energy storage systems will be provided in this section.

The first mention of the integration of wind energy and storage systems go way back. In a paper from 1968 Bruckner *et al.* investigated the economic advantages of integrated energy storage and energy conversion systems. The analysis was done from the economic standpoint and the energy storage was proposed as a mean to meet peak demand, allowing the smaller and more economical conversion system in general. The authors concluded that the energy storage could be of great help in cases when the available power production does not meet the peak demand, which is especially pronounced and can happen very often with the renewable energy systems like wind and solar. In this publication the authors were proposing hydrogen from water electrolysis as the energy storage system and acknowledged that the energy storage technologies were not developed sufficiently at the time for large power production systems [101].

The idea of integrating energy storage systems with wind power evolved further in 1980s when combined wind turbine and diesel generator systems became a convenient way to power remote areas that do not have easy access to the utility grid. In the series of articles from 1989 Davies *et al.* proposed the use of a flywheel energy storage system in order to balance demand and supply in a small Fair Isle community powered by wind and diesel

generators [102], [103].

For a period of time in the early late 1980s and 1990s a combined wind-diesel systems were a fairly live research area. Many publications from that time were investigating the problems related to the integration of wind energy with the diesel generator systems. Majority of these publications were proposing the integration of energy storage with wind and diesel generators for "power buffering" [104], [105]. Interesting overview of the battery energy storage systems of that time and the possibilities for their application in wind-diesel systems was given by Manwell and McGowan [106].

In the same period, fair number of research papers were published about integrated systems of smaller wind, solar PV and diesel generators with battery storage. These systems were investigated mostly for the supplies of smaller remote loads like communication repeater stations. The combination of these resources provides reliable source of energy while at the same time maintains good battery lifetime making the system if this kind ideal for the supply of hard to reach loads that require low maintenance and high reliability [107], [108].

Most of the combined systems mentioned above are tightly coupled and usually have a common control system that regulates the voltage, regulates the frequency and dispatches generators or storage system as required. From the standpoint of integration, the combination of renewable generating and storage systems evolved in two ways from this point.

In one direction we have loosely coupled systems of more independently controlled generation systems of various kinds and energy storage devices working together in order to achieve highly efficient, independent and reliable system. These systems have evolved under the concepts of microgrids and distributed generation systems that appeared in 2000s [109] [110]. To achieve high level of grid independence and fuel supply independence, modern microgrids

always have a significant portion of renewable generation that usually includes at least one wind generator and some form of energy storage system [111], [112].

The other direction goes for more integrated renewable energy generators and storage systems. These systems usually have single renewable generator like solar PV array, solar field, wind generator or wind farm and some form of storage. For these systems energy storage is usually included in order to compensate for the variability and intermittency of the renewable generators and to help the system meet the new renewable energy grid codes. For the wind energy and energy storage systems of this kind there is also two levels of integration. In the first level the energy storage is integrated as a part of the wind farm and in the second level the energy storage system is integrated in a single wind turbine.

For systems that integrate energy storage at the wind farm level, the problems are usually linked to the energy storage sizing, dispatching and optimal operation of the wind farm and storage system as a whole. In most cases these systems have independent grid tie converters with low level controllers while the entire systems has a higher level control that allows dispatching of storage and wind generators. The optimal energy storage size can be hard to determine as the wind generator behavior depends on the season of the year, time of the day and even the landscape and terrain where it is located. High level control strategy can also be quite challenging to formulate as it is influenced by many factors including standards, economical aspects of operation, current energy and service prices and of course fairly unpredictable wind behavior.

An example of the control system formulation and the description of challenges involved can be found in a couple of papers by Teleke *et al.* The authors have analyzed the behavior, storage requirements and control strategies for a wind farm with integrated energy storage

from a fairly high level power dispatching perspective [113], [114].

Systems that integrate energy storage on the level of a single wind turbine usually have different challenges. Although the dispatching, power smoothing and optimal operation of energy storage are still very important, high level of conversion and control system integration introduces a new set of challenges. The coupling between wind and energy storage systems is in most cases done on the DC bus of the back to back converter. This allows sharing of common grid tie converter and may increase system efficiency and lower the system cost, but it also complicates the control system.

The controller has to deal with mechanical aspects of the wind turbine, electric generator, energy storage and grid tie converter. The minimum requirement for the electric generator control is to have appropriate torque/speed control algorithm, which takes the reference from the higher level maximum power point tracking controller for the wind turbine. Maximum power point wind turbine control algorithm needs to adjust the pitch and yaw angles to maintain the optimal wind energy extraction. Energy storage controller needs to maintain appropriate state of charge for the storage system and adjust the power flow from the wind generator to the grid and storage in order to satisfy the control objectives. The formulation of these control objectives is an entirely separate topic as mentioned above. The grid tie converter has to export commanded power to the grid and take care that the grid conditions and faults impact the rest of the system as little as possible. Wind turbine - storage system of this kind was analyzed from the controls perspective by Strachan and Jovicic in a couple of papers. The authors described the controllers for each mentioned subsystems, modeled the entire system and analyzed its performance [115], [22].

2.5 Conclusion of Background

It can be concluded from previous chapters that medium voltage conversion system may be necessary for the largest wind turbines in the near future due to the constant increase in their size and power. Research publications and grid codes also suggest that renewable energy systems like wind turbines and the grid they are connected to can benefit from energy storage integration. On the other hand, it has been shown that the MMC converter topology is suitable for medium-voltage and high-voltage levels. Modifications that integrate energy storage into the MMC structure have also been proposed in many variations. The natural conclusion is to bring energy storage, MMC structure and medium-voltage wind energy systems together, which is the main motivation for this dissertation.

3 Terminology

Before the start of the converter analysis, complicated and modular nature of the MMC converter structure requires the formulation of some conventions in the sub-structure naming and variable marking. This is even more pronounced by the desire to introduce additional level of complexity by integrating energy storage into the converter at the module level, which is the main focus of this dissertation. The following passages will attempt to outline a set of naming and marking rules that will be used throughout the text in equations and drawings.

Basic building blocks for the MMC topology, legs, arms, and modules (sometimes called cells in the available literature) are marked in Figure 16 in the basic three phase converter arrangement with the DC bus. The converter structures without DC bus usually have one

arm per leg while the converter structures with DC bus have two: top (upper) and bottom (lower) arm. The MMC converter legs are arranged in appropriate manner in order to create multi-phase converters. The output node of the converter leg is between two arms, as shown in Figure 16. Arm impedances Z_{ax} , Z_{ay} etc. model filter inductors or filter inductors with lumped up parasitic inductances and resistances of the converter arm power structure.

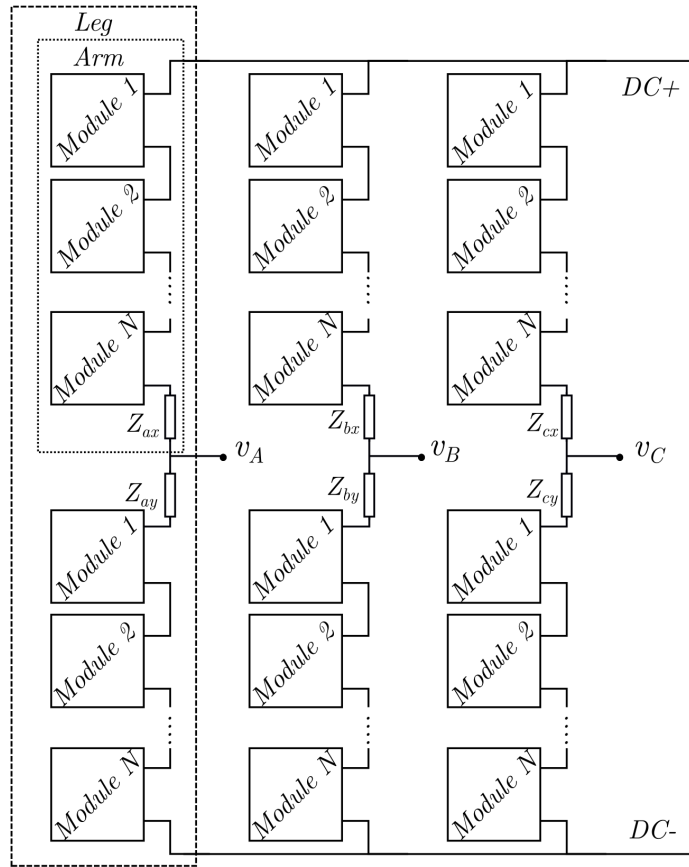


Figure 16: High level representation of the three phase MMC structure with DC bus showing the main building blocks of the converter: legs, arms and modules

Each converter arm contains two or more modules. Modules are the basic building blocks for the MMC converter. Generalized structure of the MMC module is shown in Figure 17. The structure of the module can be divided in switching, filter and storage sections.

Switching section contains commutation structure - a number of switches responsible for

redirection of the current flow and generation of module output voltage. The current can flow through the module filter and storage section or can be bypassed through the module. On average, module output voltage can be pulse-width modulated to any voltage between 0V to the full voltage of the module DC bus v_{Cf} .

The role of the filter section is to filter out the DC current I_s for storage section. Analysis of MMC converters in the available literature do not treat energy storage independent from the filter section. Storage/filter devices in the basic MMC topology are usually implemented as fairly simple electrolytic capacitor banks that do not require filtering of the AC current components. For the modules that aim to integrate battery storage systems current filtering may be necessary and consequently separate storage and filter sections might be necessary.

3.1 Naming Rules

For the MMC topology the number of modules and the number of levels can be very high. Furthermore, the number of levels becomes a variable in the topology analysis, which becomes a bit different and more complicated from the analysis of conventional multilevel topologies with fixed number of levels and number of components. As a consequence, in the graphic representations of the converter some elements and components will be indexed and will not

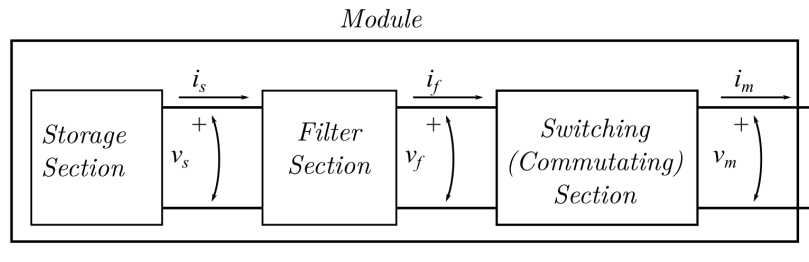


Figure 17: Generalized structure of the MMC module and its building blocks: switching section, filter section and optional storage section.

be shown directly in the schematic diagrams. However, it will be assumed that they exist in the circuit.

To simplify the schematic diagrams the markings of the components within the identical modules will show only module level (simplified) names. To identify individual components or variables within the topology in the equations, the module level names will be appended with converter level descriptors. This makes naming and indexing of the objects important and it is worthwhile to set indexing and variable naming rules. The rules that will be followed in the rest of the text are outlined in the following paragraphs.

Variables and measurements are identified using lower or upper case letters v , i , q , e , p and s for voltages, currents, charge, energy, power and switch states respectively. Lower case will denote time domain instantaneous values while the uppercase will be used for s domain or frequency domain values. If needed other letters for the specific values and additional explanation will be added in the accompanying text. Measurements and variable are further identified by the component they refer to or by the schematic marking. Depending on the position of the measurement, schematic marking will at least contain identifier mentioned above and module and/or converter level descriptor.

Component name is the string of letters and numbers used to identify an object within the converter structure. Objects are identified using upper case letters L , R , C , Z , X , and Q for inductor, resistors, capacitors, impedance, reactance and switch objects respectively. If needed additional component will be described in the accompanying text. Objects are further identified by the module level and converter level descriptors.

- Module level - Module descriptor determines the position of the object inside the

module structure. It consists of a letter and a number. The letters s , f or c are used to denote storage, filter and commutation section of the module for the generalized module structure shown in Figure 17. Numerical index is used to further describe the object within the section of the module. For example, filter section capacitor 3 will be marked as C_{f3} . If an object is within a module it will have both object level and converter level descriptors in the equations and the accompanying text but the converter level descriptor may be omitted in the diagrams.

- Converter level - converter level descriptor determines the position of module or an object within the converter structure. This descriptor has a letter-letter structure as follows:

- First letter identifies phase leg using letters (a,b,c, A, B, C...)
- Second letter identifies arm using letters x for upper and y for lower arm
- Ending number identifies the module number within converter arm

For example the filter section capacitor 3 in the 6th module of the top arm in the phase a leg will be referred to using C_{f3ax6} in the equations. Voltage across this capacitor will be referred to using V_{Cf3ax6} . If an object is unique for the converter arm leg or the entire structure it will have converter level descriptor only.

An example of the schematic markings with abbreviated names and full names that will be used in the text and equations to identify each component and variable within the MMC converter is given in Figure 18.

Variables for circuit currents will be associated with a reference positive direction that

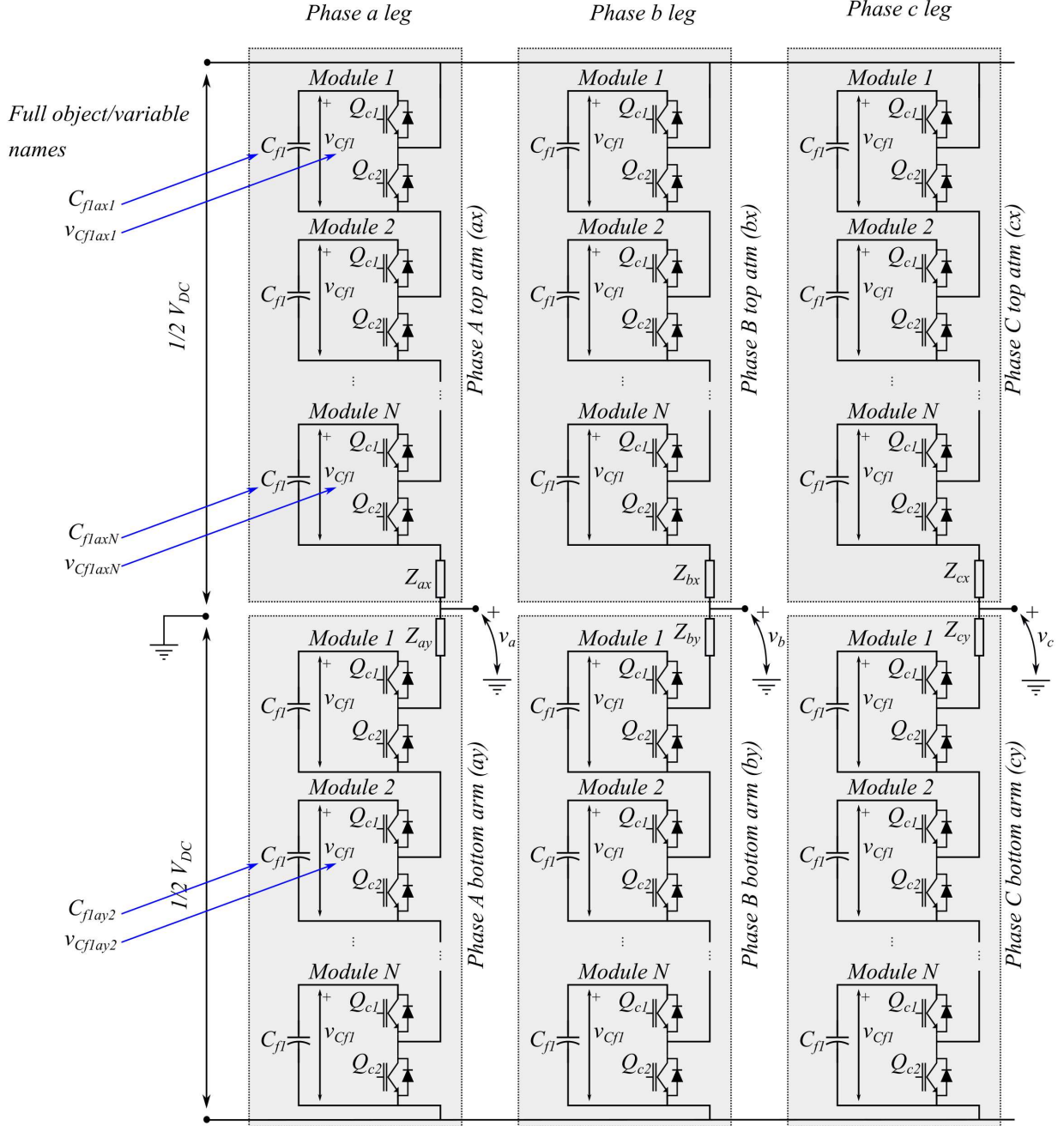


Figure 18: Schematic diagram of the conventional three-phase MMC converter with examples of the abbreviated and full names used for the components and variables in equations.

will be marked in the schematic and will be same for each module unless otherwise noted.

Voltage variables will always associated with markings on the schematic designating reference positive and negative node that will be same for each module unless otherwise noted.

If indexing is used in the equations, the index variable will be placed in brackets. For example, the state variable of the n^{th} commutation switch in the k^{th} module of the top (upper) arm of the phase a leg will be named as $s_{Qc[n]ax[k]}$.

4 Basic Equations for MMC Converter Leg

This section will outline basic MMC equations. Structure from Figure 19 will serve as a starting point for the analysis. In order to simplify the structure from Figure 19, following assumptions will be used for this section unless otherwise noted.

1. Switches and interconnections within the converter are ideal. This means that all parasitic inductances, resistances and capacitances are neglected or lumped up into arm impedances. IGBT commutation is instant and without delay. Diodes are ideal.
2. The DC bus feeding the converter is behaving as ideal voltage source maintained by another converter or power source. This assumption holds for single-phase and multi-phase systems.
3. All module filter (and storage) capacitors C_{f1} are charged to equal initial voltage. The initial DC bus capacitor voltage of the modules is such that appropriate switch arrangements can produce voltage in the range from zero to V_{DC} across each of the converter arms.
4. Pulse Width Modulation (PWM) frequency is high compared to the important harmonic components of arm and output currents.
5. Module DC bus capacitors have infinite capacitance.

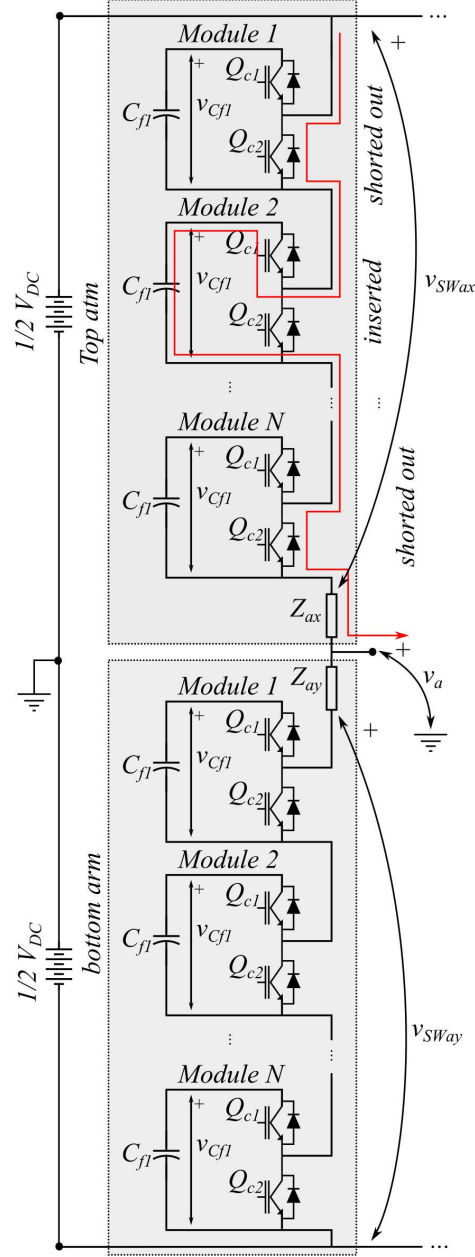


Figure 19: Single phase leg of the MMC converter connected to the infinite DC bus.

Assumption 1 allows the replacement of IGBT transistors and anti-parallel diodes from Figure 19 with ideal switches. Capacitor banks are treated as ideal capacitors and conductors as ideal electrical connections.

Assumption 2 eliminates the interaction between the legs of the converter. As a consequence, the modeling can be limited to a single phase for the investigation of the internal dynamics of a converter leg. This allows transition from the structure shown in Figure 18 to the structure from Figure 19. In general, for MMC the total DC bus of the modules or the voltage reach of the converter arm is:

$$\begin{aligned} V_{DCaxm}(t) &= \sum_{i=1}^n V_{Cf1x[i]}(t) \\ V_{DCaym}(t) &= \sum_{i=1}^n V_{Cf1y[i]}(t) \end{aligned} \tag{1}$$

If the system is symmetric 1 can be rewritten as:

$$V_{DCaxm}(t) = V_{DCaym}(t) = V_{DCm} \geq V_{DC} \tag{2}$$

Assumption 3 about the charge of the module DC bus capacitors ensures that the output voltage can swing from rail to rail of the input DC bus supply ($-V_{DC}/2$ to $+V_{DC}/2$). Equation (2) gives the relationship between DC bus voltage and initial module DC bus capacitor voltages for phase leg of the converter that meets this requirement. Note that the voltage of the module DC bus should be equal or greater than the external DC bus voltage in order to fully control the currents within the converter leg. For this approximation the DC bus is

equal among modules and the total arm module DC bus is just above the external DC bus:

$$\begin{aligned} V_{Cf1x[i]}(t) &= \frac{V_{DCm}}{N} \\ V_{Cf1y[i]}(t) &= \frac{V_{DCm}}{N} \end{aligned} \tag{3}$$

Assumption 5 allows the operation of the converter in the open loop, without monitoring and balancing controls for the module DC bus capacitors. This assumption hides some of the important converter dynamics and will be used only to draw a number of conclusions about the basic converter operation.

Infinite capacitance capacitors can be replaced by voltage sources having the voltage equal to the initial capacitor voltage given in Equation (3). The string of modules in the converter arm in Figure 19 now consist of only ideal voltage sources and ideal switches. As the current path through the modules always exist (through ideal IGBT switch or ideal anti parallel diode). The entire string of arm modules from Figure 19 can be replaced with the ideal controlled voltage sources as shown in Figure 20. This is one of the simplest models of the MMC commonly used in available literature [35], [60].

The total sum of DC voltages of the inserted modules from Figure 19 will determine the converter arm voltage in Figure 20. General relation for the arm voltages of the converter leg shown in Figure 19 can be expressed with equations (4) and (5).

$$v_{SWax}(t) = \sum_{i=1}^N v_{Cf1ax[i]}(t) s_{ax[i]}(t), \quad s_{ax[i]} \in \{0, 1\} \tag{4}$$

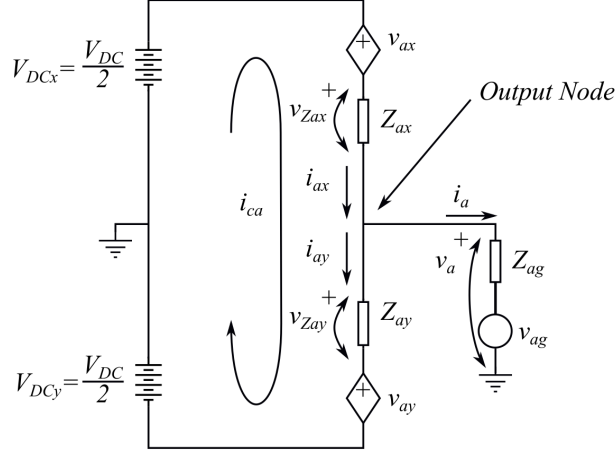


Figure 20: Simplified model of the idealized phase leg of the MMC converter.

$$v_{SWay}(t) = \sum_{i=1}^N v_{Cf1ay[i]}(t) s_{ay[i]}(t), \quad s_{ay[i]} \in \{0, 1\} \quad (5)$$

$s_{ax[i]}$ and $s_{ay[i]}$ are the module commutation section states for the modules of the upper and lower arms of the converter leg respectively. The commutation section state is 1 when the module is inserted into the string of arm modules generating the output voltage and 0 when it is shorted out. It can be noted that commutation section state formulated in this way does not depend on the implementation and the number of switches in the module but can be derived (expressed) from module switch states or even module switch gating states and current polarities.

4.1 Modulation Index Definition

In order to link the modulation index of the module PWM outputs with the total arm voltages v_{ax} and v_{ay} it may be good to observe sums in equations (4) and (5) using the reasoning given below:

- The modulation index is defined as a normalized output averaged over one switching period. Normalized in this case means the ratio between actual output and maximum achievable output obtainable by the allowed switching states.
- In case of the MMC converter the maximum voltage is achieved when the switching state is "inserted" for the entire switching period (e.g. $s_{ax[i]}(t) = 1$ for $t = kT_s \dots (k + 1)T_s$).
- Consequently, it can be concluded that the duty ratio of the insertion switching state (or duty of the state $s_{a..} = 1$ as defined above) of the MMC module during the switching period is equal to the modulation index at the time of sampling for that module. This is expressed in (6) and (7).

$$m_{ax[i]}(nT_s) = \frac{T_{ONax[i]}(t)}{T_s} \quad \text{for } t \in [nT_s, (n+1)T_s) \quad (6)$$

$$m_{ay[i]}(nT_s) = \frac{T_{ONay[i]}(t)}{T_s} \quad \text{for } t \in [nT_s, (n+1)T_s) \quad (7)$$

- Duty of the insertion switch of the MMC module can be obtained from switch state using equations (8) and (9)

$$m_{ax[i]}(nT_s) = \frac{T_{ONax[i]}(t)}{T_s} = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ax[i]}(t) dt \quad (8)$$

$$m_{ay[i]}(nT_s) = \frac{T_{ONay[i]}(t)}{T_s} = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ay[i]}(t) dt \quad (9)$$

- As the entire converter structure acts as a low pass filter, in this approximation it can be assumed that the higher harmonics in (4) - (5) are not of interest and that the arm voltages can be approximated by their filtered versions. A moving average filter as shown in (10) and (11) is convenient for this propose.

$$v_{ax}(t) = \sum_{i=1}^N \left(\frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} v_{Cf1ax[i]}(t) s_{ax[i]}(\tau) d\tau \right) \quad (10)$$

$$v_{ay}(t) = \sum_{i=1}^N \left(\frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} v_{Cf1ay[i]}(t) s_{ay[i]}(\tau) d\tau \right) \quad (11)$$

- For a well-designed MMC structure the output of the filtering section of the module can be approximated as constant during one switching period. The ripple on the output of the module DC bus (or filter section) should be small in any case compared to the total DC bus voltage and the ripple in case of the MMC is mostly at Grid frequency fundamental. Furthermore, for the current approximation, under Assumption 2 the module DC bus is constant. As a result, $v_{Cf1ax[i]}(t)$ and $v_{Cf1ay[i]}(t)$ can be taken out of the integrals in (10) and (11).

$$v_{ax}(t) = \sum_{i=1}^N \left(v_{Cf1ax[i]}(t) \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} s_{ax[i]}(\tau) d\tau \right) \quad (12)$$

$$v_{ay}(t) = \sum_{i=1}^N \left(v_{Cf1ay[i]}(t) \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} s_{ay[i]}(\tau) d\tau \right) \quad (13)$$

- By comparing (8) - (9) and (10) - (11) it is possible to link the arm voltages and

modulation references as given in (14) and (15).

$$v_{ax}(t) = \sum_{i=1}^N v_{Cf1ax[i]}(t) m_{ax[i]}(t) \quad (14)$$

$$v_{ay}(t) = \sum_{i=1}^N v_{Cf1ay[i]}(t) m_{ay[i]}(t) \quad (15)$$

Note that voltages are now expressed using normalized continuous (modulation) references $m_{ax[i]}(t)$ and $m_{ay[i]}(t)$. For each module the PWM references can be expressed as a sum of average references and the disturbances as given in (16) and (17). Average references $\bar{m}_{ax}(t)$ and $\bar{m}_{ay}(t)$ are common for all modules in the same arm and are the consequence of a common control strategy that generates the output voltage. Individual, module specific modulation reference disturbances $m_{\Delta ax}(t)$ and $m_{\Delta ay}(t)$ are the consequence of the finite switching frequency, asymmetry in the structure, the switching strategy, module voltage balancing and other factors.

$$\begin{aligned} v_{ax}(t) &= \sum_{i=1}^N v_{Cf1ax[i]}(t) (\bar{m}_{ax}(t) + m_{\Delta ax[i]}(t)) = \\ &= \sum_{i=1}^N v_{Cf1ax[i]}(t) \bar{m}_{ax}(t) + \sum_{i=1}^N v_{Cf1ax[i]}(t) m_{\Delta ax[i]}(t) \end{aligned} \quad (16)$$

$$\begin{aligned} v_{ay}(t) &= \sum_{i=1}^N v_{Cf1ay[i]}(t) (\bar{m}_{ay}(t) + m_{\Delta ay[i]}(t)) = \\ &= \sum_{i=1}^N v_{Cf1ay[i]}(t) \bar{m}_{ay}(t) + \sum_{i=1}^N v_{Cf1ay[i]}(t) m_{\Delta ay[i]}(t) \end{aligned} \quad (17)$$

The average modulation index is the same for all modules within one arm and can be taken out of the sums as shown in (18) and (19)

$$\begin{aligned}
v_{ax}(t) &= \bar{m}_{ax}(t) \sum_{i=1}^N v_{Cf1ax[i]}(t) + \sum_{i=1}^N v_{Cf1ax[i]}(t) m_{\Delta ax[i]}(t) = \\
&= \bar{m}_{ax}(t) V_{DCaxm} + \sum_{i=1}^N v_{Cf1ax[i]}(t) m_{\Delta ax[i]}(t)
\end{aligned} \tag{18}$$

$$\begin{aligned}
v_{ay}(t) &= \bar{m}_{ay}(t) \sum_{i=1}^N v_{Cf1ay[i]}(t) + \sum_{i=1}^N v_{Cf1ay[i]}(t) m_{\Delta ay[i]}(t) = \\
&= \bar{m}_{ay}(t) V_{DCaym} + \sum_{i=1}^N v_{Cf1ay[i]}(t) m_{\Delta ay[i]}(t)
\end{aligned} \tag{19}$$

If the converter output follows the control strategy well enough it can be argued that the disturbances in the PWM references cancel each other in the string of modules making the converter arm and that the sums $\sum_{i=1}^N v_{Cf1ax[i]}(t) m_{\Delta ax[i]}(t)$ and $\sum_{i=1}^N m_{v_{Cf1ay[i]}(t) \Delta ay[i]}(t)$ can be neglected. If that is the case, equations (16) and (17) can be rewritten as shown in (20) and (21).

$$v_{ax}(t) \approx \bar{m}_{ax}(t) V_{DCaxm} \tag{20}$$

$$v_{ay}(t) \approx \bar{m}_{ay}(t) V_{DCaym} \tag{21}$$

Under the assumptions 3 and 5 given above equations (20) and (21) can be rewritten as shown in (22) and (23).

$$v_{ax}(t) \approx V_{DC}\bar{m}_{ax}(t) \quad (22)$$

$$v_{ay}(t) \approx V_{DC}\bar{m}_{ay}(t) \quad (23)$$

4.2 Circuit Equations

Analysis of the circuit from Figure 20 will be performed in s domain at this point. Fairly simple Equation (24) can be used to describe the dependency between the output voltage v_a and output current i_a . Capital letters are used to denote the complex domain values equations below and they correspond to the lowercase letters denoting time domain variables used in the schematic given in Figure 20.

$$V_a(s) = Z_{ag}(s) \cdot I_a(s) + V_{ag}(s) \quad (24)$$

Relation that links output and arm currents for the circuit shown in Figure 20 is given in Equation (25). Besides the components making the output current upper and lower arm currents contain components of the circulating current. In this analysis, circulating current is assumed to be the current closing through both arms of the converter leg. This current contains useful input DC current necessary for the power conversion and a number of harmonic components.

$$I_a(s) = I_{ax}(s) - I_{ay}(s) \quad (25)$$

For the analysis of the converter operation, it is useful to express the arm currents in terms of circulating and output current components of the converter leg. To make the relations as general as possible and to account for the fact that arms belonging to a leg of a MMC converter do not have to share the output current equally a new variable can be introduced. This variable can be named Sharing Factor (k_s) and can be seen as the fraction of the output current carried by the upper arm of the converter relative to the total output current. Note that the sharing factor is a real and not a complex number. The interpretation can be seen in Figure 21 where k_s is used to scale vector I_a in order to obtain arm currents I_{ax} and I_{ay} with selected circulating current I_{ca} . Note that besides the fundamental represented with the vectors given in Figure 21 there will also be other harmonic content in the arm and output currents as well as DC component in the circulating current.

Equations that express arm currents in terms of sharing factor, output and circulating currents are given in (26) and (27).

$$I_{ax}(s) = I_{ca}(s) + k_s I_a(s), \quad k_s \leq 1 \quad (26)$$

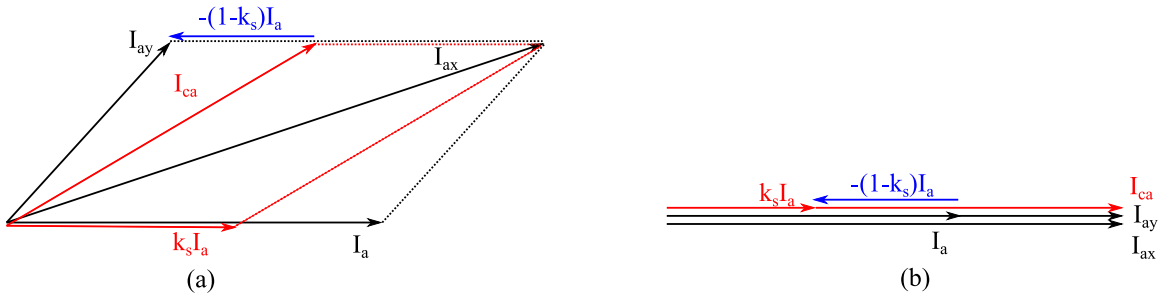


Figure 21: Phasor diagrams for the leg currents and its output and circulating current representations for the fundamental frequency. (a) - For the circulating current with arbitrary phase. (b) - For the circulating current in phase with output current.

$$I_{ay}(s) = I_{ca}(s) - (1 - k_s)I_a(s), \quad k_s \leq 1 \quad (27)$$

Circulating current can be expressed in terms of upper and lower arm currents by rearranging equations (25), (26) and (27). The result is given in Equation (28). The same result can be obtained from 21-(a) by applying triangle similarity to scaled vectors along I_{ax} and I_{ay} adding up to I_{ca} .

$$I_{ca}(s) = (1 - k_s)I_{ax}(s) + k_s I_{ay}(s) \quad (28)$$

Arm currents are the consequence of the voltage applied across the arm impedance as expressed in equations (29) and (30).

$$I_{ax}(s) = \frac{V_{Zax}(s)}{Z_{ax}(s)} \quad (29)$$

$$I_{ay}(s) = \frac{V_{Zay}(s)}{Z_{ay}(s)} \quad (30)$$

With the help of Kirchhoff's Voltage Law (KVL) and Figure 20 the relations that link controlled voltage sources and arm impedance voltages can be written as:

$$V_{DCx}(s) - V_{ax}(s) - V_{Zax}(s) - V_{Zag}(s) - V_{ag}(s) = 0 \quad (31)$$

$$-V_{DCy}(s) + V_{ay}(s) + V_{Zay}(s) - V_{Zag}(s) - V_{ag}(s) = 0 \quad (32)$$

$$V_{DCx}(s) + V_{DCy}(s) = V_{DC}(s) \quad (33)$$

$$V_{DCx}(s) - V_{DCy}(s) = \Delta V_{DC}(s)$$

Equations (33) emphasize that the DC BUs imbalance may exist and that DC supply in general does not have to be balanced around ground. However, for the most of the analysis it will assumed that V_{DCx} is equal to V_{DCy} and that $\Delta V_{DC}(s)$ is 0. By combining equations (31) - (33) with (29), (30) and (24) the following relations are obtained:

$$\begin{aligned} V_{ax}(s) - V_{ay}(s) = & -2V_{ag}(s) + \Delta V_{DC}(s) + I_{ca}(s)(Z_{ay}(s) - Z_{ax}(s)) \\ & - I_a(s)(k_s Z_{ax}(s) + (1 - k_s)Z_{ay}(s) + 2Z_{ag}(s)) \end{aligned} \quad (34)$$

$$\begin{aligned} V_{ax}(s) + V_{ay}(s) = & V_{DC}(s) - I_{ca}(s)(Z_{ay}(s) + Z_{ax}(s)) \\ & - I_a(s)(k_s Z_{ax}(s) - (1 - k_s)Z_{ay}(s)) \end{aligned} \quad (35)$$

Several important conclusions can be drawn from equations (34) and (35):

- If the leg impedances are equal $Z_{ax}(s) = Z_{ay}(s) = Z_a$, the output current depends only on the output node voltage, the difference between the controlled voltages $V_{ax}(s)$ and $V_{ay}(s)$ and DC bus imbalance as illustrated in Equation (36). As the DC bus imbalance is usually small, this suggests that the output current can be controlled by controlling the difference of the arm voltages.

$$V_{ax}(s) - V_{ay}(s) = -2V_{ag}(s) + \Delta V_{DC}(s) - I_a(s)(Z_a(s) + 2Z_{ag}(s)) \quad (36)$$

- If the sharing factor is $k_s = 0.5$, which means that the output current is equally shared between the upper and the lower arm of the converter leg, the circulating current depends only on the DC bus voltage and the sum of the converter arm voltages. This can be easily proved from Equation (37) which is derived from (35) with the assumption that $Z_{ax}(s) = Z_{ay}(s) = Z_a$.

$$V_{ax}(s) + V_{ay}(s) = V_{DC}(s) - 2Z_a(s)I_{ca}(s) - 2(k_s - 0.5)I_a(s)Z_a(s) \quad (37)$$

- The influence of the circulating current and sum of the arm voltages on the output current increases as the sharing factor goes away from $k_s = 0.5$. In other words, the coupling between circulating and output current increases if the sharing of the output current is unequal between the arms of the MMC converter leg and the control of the converter becomes a bit more challenging.
- Equations (36) and (37) can be used to derive no load conditions for the converter and control references. No load condition when $I_a = 0$ and $I_{ca} = 0$ require the following conditions to be true:

$$V_{ax}(s) - V_{ay}(s) = -2V_{ag}(s) + \Delta V_{DC}(s) \quad (38)$$

$$V_{ax}(s) + V_{ay}(s) = V_{DC}(s) \quad (39)$$

- Observing equations (36) to (39) leads to the conclusion that the feedback controller for this converter in its simplest form will have to be able to control at least DC components and the components at the frequency of the grid voltage generator v_{ag} .

Presence of AC and DC components within converter legs that have to be controlled using a same set of inputs complicates the controller design to some extent. For now, references for the voltage sources v_{ax} and v_{ay} will be derived and used for the analysis of power flow between converter legs and converter modules.

4.3 Arm Voltage References

Equations (31) and (32) can be used to derive control references for the arm voltages V_{ax} and V_{ay} for the steady state, zero circulating current and zero output current (no load conditions). In this case there are no voltage drops across impedances Z_{ax} , Z_{ay} and Z_{ag} . Solving for V_{ax} and V_{ay} results in equations (40) and (41).

$$V_{ax}(s) \Big|_{I_a=0, I_{ca}=0} = V_{DCx}(s) - V_{ag}(s) \quad (40)$$

$$V_{ay}(s) \Big|_{I_a=0, I_{ca}=0} = V_{DCy}(s) + V_{ag}(s) \quad (41)$$

Terms in equations (40) and (41) should be actual measurements of V_{DCx} , V_{DCy} and V_{ag} . Note that V_{ag} is AC voltage, usually 60Hz and V_{DCx} , V_{DCy} are DC in the ideal case and are

equal to $V_{DC}/2$.

Deviations in the reference values from the no load values given in (40) and (41) cause output and circulating current to be greater than zero. In the ideal case the amplitude of these deviations is significantly smaller than the amplitude of the signals given in (40) and (41). It can be assumed that these disturbances take the form of factors $V_{a\Sigma}$ and $V_{a\Delta}$ as shown in (42) and (43).

$$V_{ax}(s) = V_{DCx}(s) - V_{ag}(s) + \frac{1}{2}V_{a\Sigma}(s) - \frac{1}{2}V_{a\Delta}(s) \quad (42)$$

$$V_{ay}(s) = V_{DCy}(s) + V_{ag}(s) + \frac{1}{2}V_{a\Sigma}(s) + \frac{1}{2}V_{a\Delta}(s) \quad (43)$$

Substituting (42) and (43) in (34) and (35) and solving for $V_{a\Sigma}$ and $V_{a\Delta}$ results in equations (44) and (45) that link disturbances $V_{a\Sigma}$ and $V_{a\Delta}$ with circulating and output currents.

$$V_{a\Delta}(s) = -I_{ca}(s)(Z_{ay}(s) - Z_{ax}(s)) + I_a(s)(k_s Z_{ax}(s) + (1 - k_s)Z_{ay}(s) + 2Z_{ag}(s)) \quad (44)$$

$$V_{a\Sigma}(s) = -I_{ca}(s)(Z_{ay}(s) + Z_{ax}(s)) - I_a(s)(k_s Z_{ax}(s) - (1 - k_s)Z_{ay}(s)) \quad (45)$$

If arm impedances are equal $Z_{ax} = Z_{ay} = Z_a$ and sharing factor $k_s = 0.5$, equations (44) and (45) can be simplified into equations (46) and (47).

$$V_{a\Delta}(s) = I_a(s)(Z_a(s) + 2Z_{ag}(s)) \quad (46)$$

$$V_{a\Sigma}(s) = -I_{ca}(s)(2Z_a(s)) \quad (47)$$

Equations (46) and (47) indicate that in the that circulating current can be controlled with the factor $V_{a\Sigma}(s)$ and that output current can be controlled with the factor $V_{a\Delta}$.

Equations (42), (43), (44) and (45) can be used to obtain references for the arm voltage voltage sources V_{ax} and V_{ay} from Figure 20 for the desired circulating and output currents and known voltages V_{ag} and V_{DC} .

4.4 Power Flow

4.4.1 General Equations

From the previous section it can be seen that the simplest model of a single leg of the MMC converter still contains at least five power sources (four if DC bus is counted as a single source). In order to have the output current as factor in the analysis, in the previous sections, currents were transformed from a natural set of coordinates corresponding to arm current to another set of coordinates corresponding to the output and circulating current. Furthermore, arm voltage sources will have AC and DC components both in voltage and current waveforms. As a result, the power flow within the structure can get quite complicated.

Starting from a structure given in Figure 20 and using equations for arm voltage control references (42) and (43) from the previous section and assuming that $V_{DCx} = V_{DCy} = V_{DC}/2$ it is possible to evaluate the power delivered by all supplies in the circuit of one MMC converter leg.

Note that the power is instantaneous and signals are in time domain in the following

equations. For consistency of notation all supplies will be observed as power producers and all impedances as power consumers. The sign of the power will determine the direction of actual power flow.

Power delivered from the output supply is given in (48).

$$p_{ag}(t) = -v_{ag}(t)i_a(t) \quad (48)$$

The power delivered from the DC supplies V_{DCx} and V_{DCy} is given in Equation (49).

$$p_{DC}(t) = p_{V_{DCx}}(t) + p_{V_{DCy}}(t) = V_{DC}(t)i_{ca}(t) + \left(k_s - \frac{1}{2}\right) V_{DC}(t)i_a(t) \quad (49)$$

Expressions for the power delivered by the top and bottom arm of the converter are given in (50) and (51). The equations are derived with the help of (26), (27) and (42), (43).

$$\begin{aligned} p_{v_{ax}}(t) = -v_{ax}(t)i_{ax}(t) = & -\frac{1}{2}V_{DC}(t)i_{ca}(t) \\ & -\frac{1}{2}V_{DC}(t)k_s i_a(t) \\ & + v_{ag}(t)i_{ca}(t) \\ & + v_{ag}(t)k_s i_a(t) \\ & -\frac{1}{2}v_{a\Sigma}(t)(i_{ca}(t) + k_s i_a(t)) \\ & +\frac{1}{2}v_{a\Delta}(t)(i_{ca}(t) + k_s i_a(t)) \end{aligned} \quad (50)$$

$$\begin{aligned}
p_{v_{ay}}(t) = & -v_{ay}(t)i_{ay}(t) = -\frac{1}{2}V_{DC}(t)i_{ca}(t) \\
& +\frac{1}{2}V_{DC}(t)(1-k_s)i_a(t) \\
& -v_{ag}(t)i_{ca}(t) \\
& +v_{ag}(t)(1-k_s)i_a(t) \\
& -\frac{1}{2}v_{a\Sigma}(t)(i_{ca}(t)-(1-k_s)i_a(t)) \\
& -\frac{1}{2}v_{a\Delta}(t)(i_{ca}(t)-(1-k_s)i_a(t))
\end{aligned} \tag{51}$$

Note that the terms for DC bus voltage $V_{DC}(t)$ and grid voltage $v_{ag}(t)$ in (50) and (51) are references generated by the arm voltage control based on the measurement of these voltages. The references are fed to the arm voltage sources and it is assumed that the voltage of the arm source follows the references ideally. For the sake of simplicity measurements and references are not distinct here.

The following conclusions can be drawn from equations (48) - (51):

- From (48) and (49) can be concluded that the input and output power can be decoupled if the arms share the output current equally ($k_s = 0.5$). In this case DC bus power does not depend on the output current, at least not directly. Output power is completely supplied by the converter arms and their internal energy storage. If the sharing is not ideal the output current will have direct influence on the input DC bus power.
- Instantaneous DC bus power from Equation (49) and first two terms in (50) and (51) add up to zero. It can be concluded that these terms describe the instantaneous power transfer from DC bus sources to the arms of the converter.

- Second term in (49) and second terms in (50) and (51) add up to zero as well. When $k_s = 0.5$ second term in (49) disappears but the second terms in equations (50) and (51) remain. This suggests that in addition to the power exchange between DC bus and arms, second term in equations (50) and (51) also describes power exchange between arms carried by the output current. To evaluate the amount of this power exchange second terms in equations (50) and (51) can be rewritten as shown in (52) and (53). If expressed in this way, the sign of the terms indicate which term describes power transfer between converter arms and DC bus and between converter arms themselves. The arms should receive power from the DC bus and this is indicated by the minus sign. The terms that describe exchange between arms will have alternate signs.

$$-\frac{1}{2}V_{DC}(t)k_s i_a(t) = -\frac{1}{2}\left(k_s - \frac{1}{2}\right)V_{DC}(t)i_a(t) - \frac{1}{4}V_{DC}(t)i_a(t) \quad (52)$$

$$+\frac{1}{2}V_{DC}(t)(1 - k_s)i_a(t) = -\frac{1}{2}\left(k_s - \frac{1}{2}\right)V_{DC}(t)i_a(t) + \frac{1}{4}V_{DC}(t)i_a(t) \quad (53)$$

- Third term in (50) and (51) also describe the power exchange between converter arms but this portion is carried by the circulating current.

The physical explanation of the power exchange between arms can be found in the referent directions of the arm voltages and currents. From Figure 20 it is obvious that arm supplies v_{ax} and v_{ay} cannot contribute to the output power with the same sign. Depending on the output current direction and the output voltage one arm will deliver and another will receive a portion of power carried by the output current. The size

of this portion will depend on the output voltage as well as that will dictate the arm voltage source values. The fact that one arm is delivering and another receiving a portion of the power carried by the output current can be viewed as power exchange between converter arms. This logic is in part dictated by the choice to analyze the converter in terms of circulating and output currents and not in terms of upper and lower arm currents.

- Equation (48) and fourth term in (50) and (51) add up to zero. These terms describe the transfer of power from the arms to the output.
- By adding equations (48), (49), (50) and (51) all terms except last two in equations (50) and (51) add up to zero. As a result of the power conservation law, it can be concluded that these two terms represent the power delivered to the arm impedances Z_{ax} and Z_{ay} in Figure 20 as the only remaining option. Another way of looking at this is that this is the power for the control effort. The arm sources act on the arm impedance voltages to maintain the desired arm currents.

It is convenient to assign a variable to each of the power components in the arm instantaneous power from (50) and (51) as shown in equations (54) and (55). Terms used in equations (54) and (55) can be found in (48), (49) and (56)-(58). Besides DC bus power p_{DC} and output power p_{ag} , terms p_{ae} , $p_{Z_{ax}}$ and $p_{Z_{ay}}$ describe the power exchanged between the converter arms, control power delivered to the upper arm and lower arm impedances respectively.

$$p_{v_{ax}}(t) = -\frac{1}{2}p_{DC}(t) + p_{ae}(t) - k_s p_{ag}(t) + p_{Z_{ax}}(t) \quad (54)$$

$$p_{v_{ay}}(t) = -\frac{1}{2}p_{DC}(t) - p_{ae}(t) - (1 - k_s)p_{ag}(t) + p_{Z_{ay}}(t) \quad (55)$$

$$p_{ae}(t) = +v_{ag}(t)i_{ca}(t) - \frac{1}{4}V_{DC}(t)i_a(t) \quad (56)$$

$$\begin{aligned} p_{Z_{ax}}(t) = & -\frac{1}{2}v_{a\Sigma}(t)(i_{ca}(t) + k_s i_a(t)) \\ & + \frac{1}{2}v_{a\Delta}(t)(i_{ca}(t) + k_s i_a(t)) \end{aligned} \quad (57)$$

$$\begin{aligned} p_{Z_{ay}}(t) = & -\frac{1}{2}v_{a\Sigma}(t)(i_{ca}(t) - (1 - k_s)i_a(t)) \\ & - \frac{1}{2}v_{a\Delta}(t)(i_{ca}(t) - (1 - k_s)i_a(t)) \end{aligned} \quad (58)$$

4.4.2 Converter Arm Power Balance

Analysis above applies to instantaneous power flow within the converter. To evaluate the power balance additional assumptions are necessary. As the converter is analyzed in a grid tie structure, it can be assumed that:

- Grid voltage will have pure sinusoidal waveform. It is assumed that the grid voltage term $v_{ag}(t)$ in the references creating arm voltages in (48) - (58) is harmonic free. In case there are harmonics in the actual grid voltage, they will cause harmonics in the output current.
- Grid current will have a dominant fundamental with higher harmonic content.
- Circulating current will have DC component and a number of harmonics.
- DC bus is constant.

The assumptions mentioned above about the power carrying waveforms are summarized in Table 1.

Table 1: Power carrying waveforms

Waveform approximation	Description
$v_{ag}(t) = V_{ag1}\cos(\omega_g t)$	Grid supply voltage
$i_a(t) = I_{a1}\cos(\omega_g t - \theta_{a1}) + \sum_{h=2}^H I_{ah}\cos(h\omega_g t - \theta_{ah})$	Grid current
$V_{DC}(t) = V_{DC}$	DC bus voltage
$i_{ca}(t) = I_{ca0} + \sum_{h=1}^H I_{cah}\cos(h\omega_g t - \theta_{cah})$	Circulating current

Higher current harmonics in Table 1 are given with respect to the grid voltage (fundamental) frequency. Harmonic limit H is chosen as a range of interest and can be somewhere between grid fundamental and switching frequency. The assumption about harmonic content here is made only to investigate the effects these might have on active (DC) and reactive (AC) power components within the converter.

Applying the waveforms from Table 1 to the output power Equation (48) results in (59). All terms in Equation (59) except for the first represent reactive power components. First term in (59) is a active power component that describes the transfer of power from arm sources to the output. Second term describes the transfer of reactive power from the converter arms to the output. Last two terms can be seen as harmonic power components describing the harmonic power exchange between the converter arms and the output.

$$\begin{aligned}
p_{ag}(t) = & -v_{ag}(t)i_a(t) = \\
& + \frac{1}{2}V_{ag1}I_{a1}\cos(\theta_{a1}) \\
& + \frac{1}{2}V_{ag1}I_{a1}\cos(2\omega_g t - \theta_{a1}) \\
& + \sum_{h=2}^H \frac{1}{2}V_{ag1}I_{ah}\cos((h+1)\omega_g t - \theta_{a1}) \\
& + \sum_{h=2}^H \frac{1}{2}V_{ag1}I_{ah}\cos((h-1)\omega_g t - \theta_{a1})
\end{aligned} \tag{59}$$

Applying the waveforms from Table 1 to the DC bus power Equation (49) results in (61).

$$\begin{aligned}
p_{DC}(t) = & +V_{DC}(t)i_{ca}(t) + \left(k_s - \frac{1}{2}\right)V_{DC}(t)i_a(t) = \\
& + V_{DC}I_{ca0} \\
& + \sum_{h=1}^H V_{DC}I_{cah}\cos(h\omega_g t - \theta_{cah}) \\
& + (k_s - \frac{1}{2})V_{DC}I_{a1}\cos(\omega_g t - \theta_{a1}) \\
& + (k_s - \frac{1}{2})\sum_{h=2}^H V_{DC}I_{ah}\cos(h\omega_g t - \theta_{ah})
\end{aligned} \tag{60}$$

The first term in (60) active power transfer from DC source to the converter arms. The remaining terms describe reactive power flows that move energy between arms and the DC source. In case of ideal sharing ($k_s \rightarrow 0.5$) last two terms tend to zero.

Applying the waveforms from Table 1 to the arm exchange power Equation (56) results in (61).

$$\begin{aligned}
p_{ae}(t) = & + v_{ag}(t)i_{ca}(t) - \frac{1}{4}V_{DC}(t)i_a(t) = \\
& + V_{ag1}I_{ca0}\cos(\omega_g t) \\
& - \frac{1}{4}V_{DC}I_{a1}\cos(\omega_g t - \theta_{a1}) \\
& - \sum_{h=2}^H \frac{1}{4}V_{DC}I_{ah}\cos(h\omega_g t - \theta_{ah}) \\
& + \sum_{h=1}^H \frac{1}{2}V_{ag1}I_{cah}\cos((h+1)\omega_g t - \theta_{cah}) \\
& + \sum_{h=1}^H \frac{1}{2}V_{ag1}I_{cah}\cos((h-1)\omega_g t - \theta_{cah})
\end{aligned} \tag{61}$$

There are couple of rather important takeaways from Equation (61):

- First two terms in (61) are always there and are the consequence of the converter operation. These cannot be avoided and the energy storage within arms should be sized to handle them.
- Third term in (61) is the consequence of output current harmonics and can be limited by the converter design.
- Last two terms in (61) are the consequence of the circulating current harmonic components which can be controlled and can be avoided or at least limited by the converter design.
- Last term in Equation (61) suggests possible active power exchange between converter arms when the converter is operating. This can be done by injecting an AC component in the circulating current at the frequency of the output fundamental as indicated in

Equation (62).

$$\begin{aligned} \sum_{h=1}^H \frac{1}{2} V_{ag1} I_{cah} \cos((h-1)\omega_g t - \theta_{cah}) = & + \frac{1}{2} V_{ag1} I_{ca1} \cos(-\theta_{ca1}) \\ & + \sum_{h=2}^H \frac{1}{2} V_{ag1} I_{cah} \cos((h-1)\omega_g t - \theta_{cah}) \end{aligned} \quad (62)$$

The direction of the power flow can be controlled by the angle θ_{ca1} between the first harmonic of the circulating current and the output voltage fundamental.

Components $p_{Z_{ax}}$ and $p_{Z_{ay}}$ are a bit harder to analyze in this manner. These components represent the instantaneous power delivered by the arm supplies in order to force the desired current through impedances Z_{ax} , Z_{ay} and Z_{ag} . All power components related to these impedances will be frequency dependent, including the ones in the "active power" category. For the purpose of power balance investigation, the total active power delivered by the converter arms to the impedances Z_{ax} , Z_{ay} and Z_{ag} will be marked as $p_{R_{ax}}$ and $p_{R_{ay}}$. It can be assumed that this power component will be small compared to the rest.

As can be seen from the previous analysis MMC converter arms act as energy hubs that receive power from the DC bus and deliver it to the arm impedances and the output. The energy storage in the arms is usually very limited so the proper balance of power flow between DC bus, converter arms and output must be maintained at all times to ensure system stability. Special care must be taken when dealing with harmonic components that can carry DC (active) power components. By collecting all non-alternating terms from equations (54) and (55) it is possible to write the equations (63) and (64) for the active power balance

within the converter.

$$\overline{p_{v_{ax}}(t)} = -\frac{1}{2}V_{DC}I_{ca0} + \frac{1}{2}V_{ag1}I_{ca1}\cos(-\theta_{ca1}) - k_s\frac{1}{2}V_{ag1}I_{a1}\cos(\theta_{a1}) + p_{R_{ax}}(t) = 0 \quad (63)$$

$$\overline{p_{v_{ay}}(t)} = -\frac{1}{2}V_{DC}I_{ca0} - \frac{1}{2}V_{ag1}I_{ca1}\cos(-\theta_{ca1}) - (1 - k_s)\frac{1}{2}V_{ag1}I_{a1}\cos(\theta_{a1}) + p_{R_{ay}}(t) = 0 \quad (64)$$

$\overline{p_{v_{ax}}(t)}$ and $\overline{p_{v_{ay}}(t)}$ in equations (63) and (64) stand for average values. First and third term describe active power transfer from the DC bus to the output. Last term represents losses in the leg impedances and the second term describes power transfer between arms. Second term can be controlled and unless the power transfer is desired should be 0 either by forcing the amplitude of the fundamental of the circulating current to 0 or the phase angle to $\pi/2$.

If the converter control is designed to maintain the balance expressed in (63) and (64) then the storage in the converter arms only needs to deal with the reactive and harmonic power components. The size of energy storage needed for reactive component will determine the minimum amount of DC bus capacitance in each module of the converter arms.

Although the reactive power requirements will determine the minimum amount of energy storage the relationship is not simple. The energy storage has to be large enough such that the nonlinear loop (arm reactive power) \rightarrow (energy storage voltage variation) \rightarrow (circulating and output current harmonics) \rightarrow (arm reactive power) within the converter does not have

unstable modes. To attempt to model this loop, more detailed model of the module and arm is needed.

Equations (63) and (64) can also be used to complete the control reference equations in (44) and (45). Equations (63) and (64) link the output and circulating current. Using Equation (65), in cases when $k_s = 0.5$. it is possible to calculate the needed circulating current for desired output current in order to maintain power balance.

$$I_{ca0} = \frac{1}{2} \frac{V_{ag1}}{V_{DC}} I_{a1} \cos(\theta_{a1}) + \frac{p_{R_{ax}} + p_{R_{ay}}}{V_{DC}} \quad (65)$$

In the equation above $\cos(\theta_{a1})$ is the power factor of the converter output. It is obvious that the second terms in (63) and (64) should be zero.

In case when $k_s \neq 0.5$ second terms in (63) and (64) cannot be zero and the fundamental of the circulating current can be used to achieve power balance. If (63) and (64) are rewritten as (66) and (67) the value of the fundamental of the circulating current can be linked with output current as given in (68). Note that even in this case (65) still stands.

$$\begin{aligned} & -\frac{1}{2} V_{DC} I_{ca0} + \frac{1}{2} V_{ag1} I_{ca1} \cos(-\theta_{a1}) \\ & -\frac{1}{2} \frac{1}{2} V_{ag1} I_{a1} \cos(\theta_{a1}) + \left(\frac{1}{2} - k_s\right) \frac{1}{2} V_{ag1} I_{a1} \cos(\theta_{a1}) \\ & + p_{R_{ax}}(t) = 0 \end{aligned} \quad (66)$$

$$\begin{aligned}
& -\frac{1}{2}V_{DC}I_{ca0} - \frac{1}{2}V_{ag1}I_{ca1}\cos(-\theta_{a1}) \\
& -\frac{1}{2}\frac{1}{2}V_{ag1}I_{a1}\cos(\theta_{a1}) - (\frac{1}{2} - k_s)\frac{1}{2}V_{ag1}I_{a1}\cos(\theta_{a1}) \\
& + p_{R_{ay}}(t) = 0
\end{aligned} \tag{67}$$

$$I_{ca1}\cos(-\theta_{ca1}) = -(\frac{1}{2} - k_s)I_{a1}\cos(\theta_{a1}) \tag{68}$$

4.5 Low Switching Frequency Considerations

For the analysis of the MMC given above the assumption is that the modules are balanced through switching actions either by modifying the duty (insertion time) or the order of insertion of the modules. In both cases it is important to facilitate frequent exchange of states on each module so that the energy exchange can be controlled properly.

In cases when the switching and balancing action frequency is comparable to the fundamental or the first harmonic of the converter, the power flow within the converter cannot be observed as shown above. In this case the amount of energy absorbed by the module will highly depend on the phase between the modulation carrier and the arm current (the point where the module gets inserted in the string relative to the peaks of the current sine wave).

In this case it is possible to encounter a situation where one module will constantly be inserted near the peak of the sine wave and have large energy exchange while and other modules may be always inserted near zero crossing have almost no energy exchange. The situation will change with each change of the current phase angle (power command) which is highly unpredictable. The balancing in this case becomes highly involved task.

The modules will receive or deliver a relatively large and unpredictable quantum of energy that has to be absorbed by the module internal capacitors. Sorting balancing algorithms work well in this case but the internal capacitance of the module will have to be based on the largest quantum of energy that the module can ever exchange. This quantum of energy will depend on maximum duty of the module or balancing period and absolute peak of the current. The converter behavior becomes extremely nonlinear during transients when stability is of importance and hard to analyze.

While it is still possible to create fine sinusoidal waveforms with large number of levels and low switching frequency, the control and analysis of the converter will be fairly different and will be left for future study. The modulation index for each module will not follow the average modulation index in the same way as presented in Chapter 4.1. Due to the unpredictability mentioned above, tight control of values within the converter module by the means of modulation index will be very hard and the internal storage will be very hard to balance.

It will be assumed here that the switching frequency is at least ten times higher than the fundamental of the output current.

5 Converter Model

Previous section outlined the equations that describe the fundamental behavior and defined the operating point for the MMC converter. As in the previous section this section will deal only with one leg of the converter. Assuming that the controller is capable of full control over circulating and output current, analysis done on one leg and the single phase system

can easily be extended to any kind of multi-phase arrangement. The MMC converter leg structure that will be analyzed in this section is fairly general and is given in Figure 22.

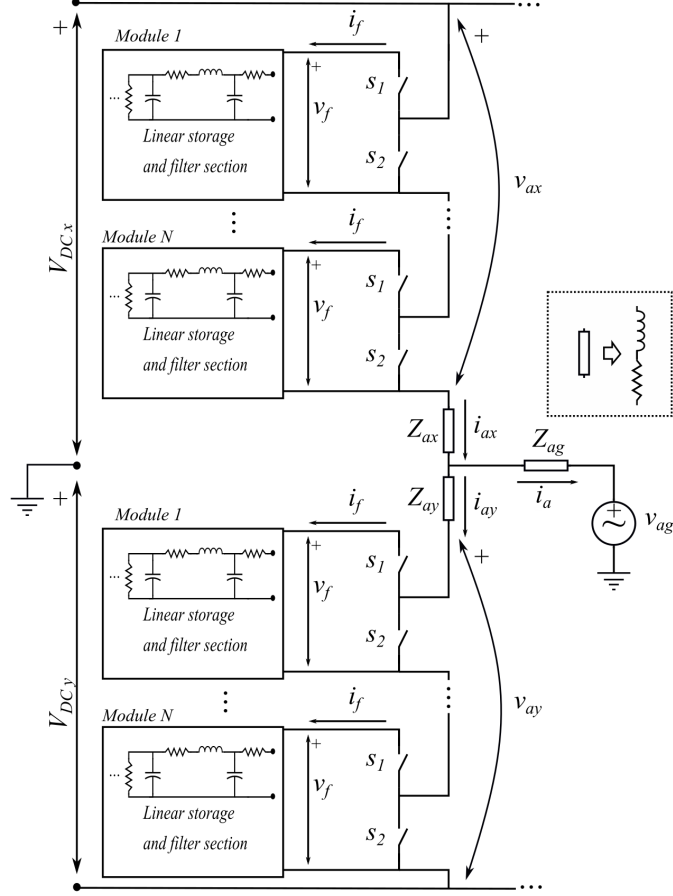


Figure 22: General structure of the MMC converter leg. Module structure is arbitrary as long as it gives well filtered filter section output v_f .

The approach here will be to go from general module equations and then incorporate them into arm and leg equations. The equations for three structures that are of interest: conventional module, module with battery energy storage and module with ultracapacitor energy storage will be derived in the next section.

5.1 Converter Module Equations

In most of the available literature, switching section is defined as a part of the module as illustrated in Figure 17 and previous sections of the current text. This is true when observing the MMC converter as a mechanical structure as switching section of each module also belongs to the mechanical assembly of the module. To make the module equations more straightforward, the switching section will not be modeled as a part of the module but as a part of the converter arms in the next section.

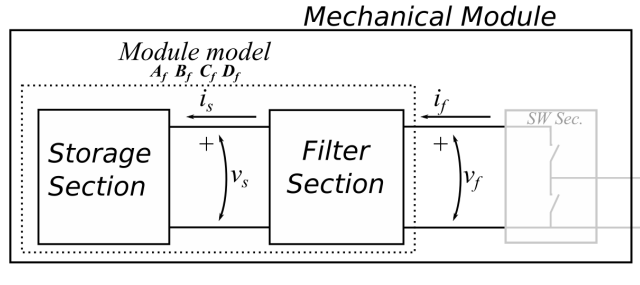


Figure 23: General structure of the MMC converter module. The switching section is modeled within the converter arm equations, as a result, the module is illustrated with switching section grayed out.

To obtain the equations that link module currents and module voltages it will be useful to assume that:

- Module storage and filter section are linear or that they can be linearized around the operating point defined by the state of charge.
- All modules have identical internal structure.

In case above mentioned is true, general module equations can be represented with the system of differential equations in general matrix form given in (69).

$$\begin{aligned}
\frac{d}{dt}\mathbf{x}_f(t) &= \mathbf{A}_f\mathbf{x}_f(t) + \mathbf{B}_fi_f(t) + \mathbf{E}_f\mathbf{u}_f(t) \\
v_f(t) &= \mathbf{C}_f\mathbf{x}_f(t) + D_fi_f(t) + \mathbf{F}_f\mathbf{u}_f(t)
\end{aligned} \tag{69}$$

Matrices \mathbf{A}_f , \mathbf{B}_f , \mathbf{C}_f , D_f , \mathbf{E}_f and \mathbf{F}_f are common for all modules. However, each module has its own set of states \mathbf{x}_f , current input i_f , voltage output v_f , and a set of other inputs $\mathbf{u}_f(\mathbf{t})$ if needed. These matrices will depend on the module implementation. Models for the few module implementations of interest will be given in the following text.

5.1.1 Implementation #1 Module Equations

Circuit diagram used to derive the equations for the generic MMC module without the switching section is given in Figure 24. In this case the module equations need to model only the module capacitor bank and module internal losses. It will be assumed that the module buswork inductances can be neglected. Capacitor C_{f1} in Figure 24 models capacitance of the DC bus capacitor bank. Resistance R_{f1} models internal resistance of the capacitor bank and any other input current dependent losses in the system. Resistance R_{f2} can be used to model the leakage commonly associated with Al electrolytic capacitors or internal loads on the module DC bus.

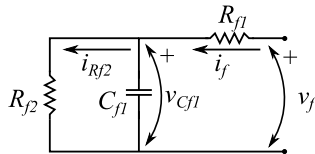


Figure 24: Circuit diagram of a generic MMC module. Resistance model internal resistance of the capacitor bank and leakage/balancing circuit.

The set of equations that describes the circuit from Figure 24 is given in (70).

$$\begin{aligned}\frac{d}{dt}v_{Cf1} &= -\frac{1}{R_{f2}C_{f1}}v_{Cf1} + \frac{1}{C_{f1}}i_f \\ v_f &= v_{Cf1} + R_{f1}i_f\end{aligned}\tag{70}$$

After examining (69) and (70) it is possible to define matrices \mathbf{A}_f , \mathbf{B}_f , \mathbf{C}_f and D_f for the system from Figure 24 as shown in (71). In this case the model has only one state and the matrices are actually scalars represented as 1x1 matrices. Additional inputs $\mathbf{u}_f(\mathbf{t})$ do not exist in this case. As a consequence, matrices \mathbf{E}_f and \mathbf{F}_f are also empty and are not listed in (71).

$$\mathbf{A}_f = \left[-\frac{1}{R_{f2}C_{f1}} \right] \quad \mathbf{B}_f = \left[\frac{1}{C_{f1}} \right] \quad \mathbf{C}_f = \left[1 \right] \quad D_f = R_{f1}\tag{71}$$

5.1.2 Implementation #2 Module Equations

Circuit diagram of the structure that will be used to model the module with integrated battery energy storage is given in Figure 25. The battery model incorporated in Figure 25 represents the one time constant dynamic model usually associated with Li-ion and other batteries. It is assumed that one time constant model is good enough for the purpose of this study [116], [117].

The differential equations that describe the circuit from Figure 25 are given in (72).

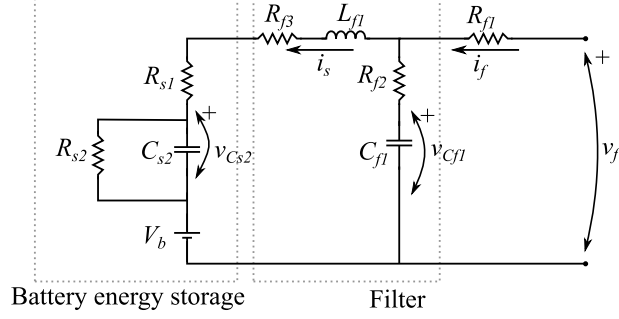


Figure 25: Circuit diagram of the module with integrated battery energy storage. Battery energy storage is modeled.

$$\begin{aligned}
\frac{d}{dt}v_{Cf1} &= -\frac{1}{C_{f1}}i_s + \frac{1}{C_{f1}}i_f \\
\frac{d}{dt}v_{Cs1} &= -\frac{1}{R_{s2}C_{f1}}v_{Cs1} + \frac{1}{C_{s1}}i_s \\
\frac{d}{dt}i_s &= \frac{1}{L_{f1}}v_{Cf1} - \frac{1}{L_{f1}}v_{Cs1} - \frac{R_{s1} + R_{f3} + R_{f2}}{L_{f1}}i_s + \frac{R_{f2}}{L_{f1}}i_f - \frac{1}{L_{f1}}v_b
\end{aligned} \tag{72}$$

After examining Equations from (69) and (72) it is possible to define matrices \mathbf{A}_f , \mathbf{B}_f , \mathbf{C}_f , \mathbf{E}_f , \mathbf{F}_f and D_f for the system from Figure 25. The matrices are given in (73). Input $\mathbf{u}_f(\mathbf{t})$ is in this case a scalar representing the battery voltage. Matrices \mathbf{E}_f and \mathbf{F}_f are also scalars but are represented as single element matrices in (73).

$$\begin{aligned}
\mathbf{A}_f &= \begin{bmatrix} 0 & 0 & -\frac{1}{C_{f1}} \\ 0 & -\frac{1}{R_{s2}C_{s2}} & \frac{1}{C_{s1}} \\ \frac{1}{L_{f1}} & -\frac{1}{L_{f1}} & -\frac{R_{s1}+R_{f3}+R_{f2}}{L_{f1}} \end{bmatrix} & \mathbf{B}_f &= \begin{bmatrix} \frac{1}{C_{f1}} \\ 0 \\ \frac{R_{f2}}{L_{f1}} \end{bmatrix} & \mathbf{E}_f &= \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_{f1}} \end{bmatrix} \\
\mathbf{C}_f &= \begin{bmatrix} 1 & 0 & -R_{f2} \end{bmatrix} & D_f &= R_{f1} + R_{f1} & \mathbf{F}_f &= \begin{bmatrix} 0 \end{bmatrix}
\end{aligned} \tag{73}$$

5.1.3 Implementation #3 Module Equations

Circuit diagram of the structure used to model the module with integrated ultra-capacitor energy storage is given in Figure 26. It is assumed that the acceptable ultra-capacitor modeled includes capacitance C_{s1} with internal resistance R_{s1} and leakage or internal load discharge resistance R_{s2} . In most cases R_{s2} will be a very small load making this resistance very high.

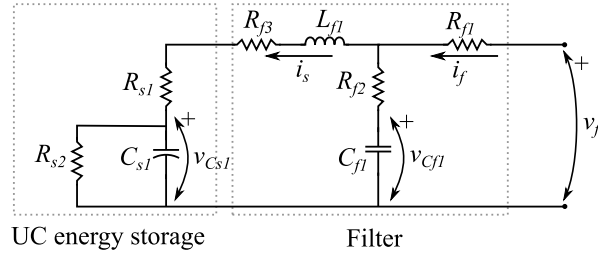


Figure 26: Circuit diagram of the module with integrated ultra-capacitor energy storage.

The differential equations that describe the circuit from Figure 26 are given in (74).

$$\begin{aligned}
 \frac{d}{dt}v_{Cf1} &= -\frac{1}{C_{f1}}i_s + \frac{1}{C_{f1}}i_f \\
 \frac{d}{dt}v_{Cs1} &= -\frac{1}{R_{s2}C_{f1}}v_{Cs1} + \frac{1}{C_{s1}}i_s \\
 \frac{d}{dt}i_s &= \frac{1}{L_{f1}}v_{Cf1} - \frac{1}{L_{f1}}v_{Cs1} - \frac{R_{s1} + R_{f3} + R_{f2}}{L_{f1}}i_s + \frac{R_{f2}}{L_{f1}}i_f
 \end{aligned} \tag{74}$$

After examining Equations from (69) and (74) it is possible to define matrices \mathbf{A}_f , \mathbf{B}_f , \mathbf{C}_f and \mathbf{D}_f for the system from Figure 26. The matrices are given in (75). Input $\mathbf{u}_f(\mathbf{t})$ does not exist in this case. As a consequence, matrices \mathbf{E}_f and \mathbf{F}_f are also empty and are not listed in (75).

$$\begin{aligned}
\mathbf{A}_f &= \begin{bmatrix} 0 & 0 & -\frac{1}{C_{f1}} \\ 0 & -\frac{1}{R_{s2}C_{f1}} & \frac{1}{C_{s1}} \\ \frac{1}{L_{f1}} & -\frac{1}{L_{f1}} & -\frac{R_{s1}+R_{f3}+R_{f2}}{L_{f1}} \end{bmatrix} & \mathbf{B}_f &= \begin{bmatrix} \frac{1}{C_{f1}} \\ 0 \\ \frac{R_{f2}}{L_{f1}} \end{bmatrix} \\
\mathbf{C}_f &= \begin{bmatrix} 1 & 0 & -R_{f2} \end{bmatrix} & D_f &= R_{f1} + R_{f2}
\end{aligned} \tag{75}$$

5.2 Converter Arm Equations

The next step is to describe arm voltages V_{ax} and V_{ay} and their dependence on the arm currents i_{ax} and i_{ay} . To do this it is necessary to define the operation of the switching section. For the converter implementation given in Figure 22 switching states $s_{ax[i]}$ and $s_{ay[i]}$ have the same meaning as in Chapter 4 and are defined as:

- $s_{ax[i]}, s_{ay[i]}$ is equal to 0 if the module i is shorted out in the string of modules making the converter arm.
- $s_{ax[i]}, s_{ay[i]}$ is equal to 1 if the module i is inserted in the string of modules making the converter arm.

With the switching states defined as above, the switching section always inserts the module in the same way and that it cannot invert the polarity of the filter section with respect to the module terminals.

If the switching states of the switching section are defined in terms of module arrangement in the converter arm (inserted, shorted out, inverted...) and the switches are assumed to be ideal the model does not depend on the switching section implementation and the number

of switches. For the switching section types that have Full Bridge or some more complicated implementations switching state definitions can be extended to include negative numbers or even fractions.

Having in mind the definitions of the switching states given above and the module equations given in (69), arm voltages for the structure shown in Figure 22 can be expressed with Equation (76). Note that (69) and equations describing modules given in previous sections refer to one module of interest only. To denote all modules within the converter, marking system described in Section 3.1 is used in the following equations.

$$\begin{aligned} v_{ax}(t) &= \sum_{i=1}^N v_{fax[i]}(t) s_{ax[i]}(t), \quad s_{ax[i]} \in \{0, 1\} \\ v_{ay}(t) &= \sum_{i=1}^N v_{fay[i]}(t) s_{ay[i]}(t), \quad s_{ay[i]} \in \{0, 1\} \end{aligned} \tag{76}$$

Similarly, currents $i_{fax[i]}$ and $i_{fay[i]}$ can be expressed as in (77):

$$\begin{aligned} i_{fax[i]}(t) &= i_{ax}(t) s_{ax[i]}(t), \quad s_{ax[i]} \in \{0, 1\} \\ i_{fay[i]}(t) &= i_{ay}(t) s_{ay[i]}(t), \quad s_{ay[i]} \in \{0, 1\} \end{aligned} \tag{77}$$

Assuming that the variables from equations (76) and (77) are given in a vector forms as shown in (78) - (80) arm voltage expressions can be converted to (81) and arm current expression to (82).

$$\mathbf{s}_{\mathbf{ax}}(t) = \begin{bmatrix} s_{ax[1]}(t) \\ s_{ax[2]}(t) \\ \vdots \\ s_{ax[N]}(t) \end{bmatrix} \quad \mathbf{s}_{\mathbf{ay}}(t) = \begin{bmatrix} s_{ay[1]}(t) \\ s_{ay[2]}(t) \\ \vdots \\ s_{ay[N]}(t) \end{bmatrix} \quad (78)$$

$$\mathbf{v}_{\mathbf{fax}}(t) = \begin{bmatrix} v_{fax[1]}(t) \\ v_{fax[2]}(t) \\ \vdots \\ v_{fax[N]}(t) \end{bmatrix} \quad \mathbf{v}_{\mathbf{fay}}(t) = \begin{bmatrix} v_{fay[1]}(t) \\ v_{fay[2]}(t) \\ \vdots \\ v_{fay[N]}(t) \end{bmatrix} \quad (79)$$

$$\mathbf{i}_{\mathbf{fax}}(t) = \begin{bmatrix} i_{fax[1]}(t) \\ i_{fax[2]}(t) \\ \vdots \\ i_{fax[N]}(t) \end{bmatrix} \quad \mathbf{i}_{\mathbf{fay}}(t) = \begin{bmatrix} i_{fay[1]}(t) \\ i_{fay[2]}(t) \\ \vdots \\ i_{fay[N]}(t) \end{bmatrix} \quad (80)$$

$$\begin{aligned} v_{ax}(t) &= \mathbf{s}_{\mathbf{ax}}^T(t) \mathbf{v}_{\mathbf{fax}}(t) \\ v_{ay}(t) &= \mathbf{s}_{\mathbf{ay}}^T(t) \mathbf{v}_{\mathbf{fay}}(t) \end{aligned} \quad (81)$$

$$\mathbf{i}_{\text{fax}}(t) = \mathbf{s}_{\text{ax}}(t)i_{ax}(t) \quad (82)$$

$$\mathbf{i}_{\text{fay}}(t) = \mathbf{s}_{\text{ay}}(t)i_{ay}(t)$$

To link equations describing modules it is necessary to extend (69) to include all modules within the arm. This can be done with the help of the marking system described in Section 3.1. The system of equations describing one converter arm now becomes:

$$\begin{aligned} \frac{d}{dt}\mathbf{x}_{\text{fax}}(t) &= \mathbf{A}_{\text{fax}}\mathbf{x}_{\text{fax}}(t) + \mathbf{B}_{\text{fax}}\mathbf{s}_{\text{ax}}(t)i_{ax}(t) + \mathbf{E}_{\text{fax}}\mathbf{u}_{\text{fax}}(t) \\ \frac{d}{dt}\mathbf{x}_{\text{fay}}(t) &= \mathbf{A}_{\text{fay}}\mathbf{x}_{\text{fay}}(t) + \mathbf{B}_{\text{fay}}\mathbf{s}_{\text{ay}}(t)i_{ay}(t) + \mathbf{E}_{\text{fay}}\mathbf{u}_{\text{fay}}(t) \end{aligned} \quad (83)$$

$$\begin{aligned} v_{ax}(t) &= \mathbf{s}_{\text{ax}}(t)^T \mathbf{C}_{\text{fax}}\mathbf{x}_{\text{fax}}(t) + \mathbf{s}_{\text{ax}}(t)^T \mathbf{D}_{\text{fax}}\mathbf{s}_{\text{ax}}(t)i_{ax}(t) + \mathbf{s}_{\text{ax}}(t)^T \mathbf{F}_{\text{fax}}\mathbf{u}_{\text{fax}}(t) \\ v_{ay}(t) &= \mathbf{s}_{\text{ay}}(t)^T \mathbf{C}_{\text{fay}}\mathbf{x}_{\text{fay}}(t) + \mathbf{s}_{\text{ay}}(t)^T \mathbf{D}_{\text{fay}}\mathbf{s}_{\text{ay}}(t)i_{ay}(t) + \mathbf{s}_{\text{ay}}(t)^T \mathbf{F}_{\text{fay}}\mathbf{u}_{\text{fay}}(t) \end{aligned} \quad (84)$$

Vectors \mathbf{x}_{fax} and \mathbf{x}_{fay} are aggregate state vectors for all modules within an arm and are consisting of concatenated state vectors given in (69) for each module within an arm. Similarly, vectors \mathbf{u}_{fax} and \mathbf{u}_{fay} are aggregate optional input vectors for all modules within an arm. The structure of both vectors is given in (85). Assuming that the vectors in (69) are m-dimensional, vectors \mathbf{x}_{fax} and \mathbf{x}_{fay}

$$\mathbf{x}_{\text{fax}} = \begin{bmatrix} \mathbf{x}_{\text{fax}[1]} \\ \mathbf{x}_{\text{fax}[2]} \\ \vdots \\ \mathbf{x}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{x}_{\text{fay}} = \begin{bmatrix} \mathbf{x}_{\text{fay}[1]} \\ \mathbf{x}_{\text{fay}[2]} \\ \vdots \\ \mathbf{x}_{\text{fay}[N]} \end{bmatrix} \quad \mathbf{u}_{\text{fax}} = \begin{bmatrix} \mathbf{u}_{\text{fax}[1]} \\ \mathbf{u}_{\text{fax}[2]} \\ \vdots \\ \mathbf{u}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{u}_{\text{fay}} = \begin{bmatrix} \mathbf{u}_{\text{fay}[1]} \\ \mathbf{u}_{\text{fay}[2]} \\ \vdots \\ \mathbf{u}_{\text{fay}[N]} \end{bmatrix} \quad (85)$$

Matrices \mathbf{A}_{fax} and \mathbf{A}_{fay} are block diagonal matrices consisting of identical blocks given in (69) and specified for different module implementations in (70)-(82). Their structure is shown in (86). If the module state vector x_f is m -dimensional and there are N modules within a leg these matrices dimensions are $mN \times mN$.

$$\mathbf{A}_{\text{fax}} = \begin{bmatrix} \mathbf{A}_{\text{fax}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{\text{fax}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{A}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{A}_{\text{fay}} = \begin{bmatrix} \mathbf{A}_{\text{fay}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{\text{fay}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{A}_{\text{fay}[N]} \end{bmatrix} \quad (86)$$

Matrices \mathbf{B}_{fax} and \mathbf{B}_{fay} are given in (87). If the module state vector x_f is m -dimensional and there are N modules within a leg these matrices are $mN \times N$ dimensional.

$$\mathbf{B}_{\text{fax}} = \begin{bmatrix} \mathbf{B}_{\text{fax}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_{\text{fax}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{B}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{B}_{\text{fay}} = \begin{bmatrix} \mathbf{B}_{\text{fay}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_{\text{fay}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{B}_{\text{fay}[N]} \end{bmatrix} \quad (87)$$

Matrices \mathbf{C}_{fax} and \mathbf{C}_{fay} are given in (88). These matrices are used in the equations for the output voltages of the filter outputs of each module. If the module state vector x_f is m -dimensional and there are N modules within a leg these matrices are $N \times mN$ dimensional.

$$\mathbf{C}_{\text{fax}} = \begin{bmatrix} \mathbf{C}_{\text{fax}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_{\text{fax}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{C}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{C}_{\text{fay}} = \begin{bmatrix} \mathbf{C}_{\text{fay}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_{\text{fay}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{C}_{\text{fay}[N]} \end{bmatrix} \quad (88)$$

Matrices \mathbf{D}_{fax} and \mathbf{D}_{fay} are given in (89). These matrices are used in the equations for the output voltages of the filter outputs of each module. If the module state vector x_f is m -dimensional and there are N modules within a leg these matrices are $N \times N$ dimensional.

$$\mathbf{D}_{\text{fax}} = \begin{bmatrix} D_{fax[1]} & 0 & \dots & 0 \\ 0 & D_{fax[2]} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & D_{fax[N]} \end{bmatrix} \quad \mathbf{D}_{\text{fay}} = \begin{bmatrix} D_{fay[1]} & 0 & \dots & 0 \\ 0 & D_{fay[2]} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \mathbf{0} & \dots & D_{fay[N]} \end{bmatrix} \quad (89)$$

Matrices \mathbf{E}_{fax} and \mathbf{E}_{fay} are given in (90). These matrices are used in the equations in case there are "auxiliary" inputs to the module filter equations besides the module current. If the module state vector x_f is m -dimensional, there are k auxiliary inputs and there are N modules within a leg these matrices are $Nm \times Nk$ dimensional.

$$\mathbf{E}_{\text{fax}} = \begin{bmatrix} \mathbf{E}_{\text{fax}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{E}_{\text{fax}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{E}_{\text{fax}[N]} \end{bmatrix} \quad \mathbf{E}_{\text{fay}} = \begin{bmatrix} \mathbf{E}_{\text{fay}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{E}_{\text{fay}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{E}_{\text{fay}[N]} \end{bmatrix} \quad (90)$$

Matrices \mathbf{F}_{fax} and \mathbf{F}_{fay} are given in (91). These matrices are used in the equations in case there are "auxiliary" inputs to the module filter equations besides the module current. If there are k auxiliary inputs and there are N modules within a leg these matrices are $N \times Nk$ dimensional.

$$\mathbf{F}_{\text{fax}} = \begin{bmatrix} \mathbf{F}_{\text{fax}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{F}_{\text{fax}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{F}_{\text{fax}[\text{N}]} \end{bmatrix} \quad \mathbf{F}_{\text{fay}} = \begin{bmatrix} \mathbf{F}_{\text{fay}[1]} & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{0} & \mathbf{F}_{\text{fay}[2]} & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \dots & \mathbf{F}_{\text{fay}[\text{N}]} \end{bmatrix} \quad (91)$$

5.3 Integrated Switching Model

Next step is to integrate the module and arm equations into differential equations modeling the converter leg. To simplify the derivation of the differential equations for the structure from Figure 22 and for the sake of continuity it is convenient to start from (34) and (35) derived in Section 4.2 for the simplified version of the converter leg. The system of equations from (34) and (35) is rewritten in (92).

$$\begin{aligned} V_{ax}(s) - V_{ay}(s) &= -2V_{ag}(s) + \Delta V_{DC}(s) + I_{ca}(s)(Z_{ay}(s) - Z_{ax}(s)) \\ &\quad - I_a(s)(k_s Z_{ax}(s) + (1 - k_s)Z_{ay}(s) + 2Z_{ag}(s)) \\ V_{ax}(s) + V_{ay}(s) &= V_{DC}(s) - I_{ca}(s)(Z_{ay}(s) + Z_{ax}(s)) \\ &\quad - I_a(s)(k_s Z_{ax}(s) - (1 - k_s)Z_{ay}(s)) \end{aligned} \quad (92)$$

Expressions from (92) can be relatively easy converted to a set of linear differential equations if it is assumed that the impedances Z_{ax} , Z_{ay} and Z_{ag} consist of resistive and inductive parts only as shown in (93).

$$\begin{aligned}
V_{ax}(s) - V_{ay}(s) = & -2V_{ag}(s) + \Delta V_{DC}(s) \\
& + I_{ca}(s)((R_{ay} + sL_{ay}) - (R_{ax} + sL_{ax})) \\
& - I_a(s)(k_s(R_{ax} + sL_{ax}) + (1 - k_s)(R_{ay} + sL_{ay})) \\
& - I_a(s)(2(R_{ag} + sL_{ag}))
\end{aligned} \tag{93}$$

$$\begin{aligned}
V_{ax}(s) + V_{ay}(s) = & +V_{DC}(s) \\
& - I_{ca}(s)((R_{ay} + sL_{ay}) + (R_{ax} + sL_{ax})) \\
& - I_a(s)(k_s(R_{ax} + sL_{ax}) - (1 - k_s)(R_{ay} + sL_{ay}))
\end{aligned}$$

$$\begin{aligned}
V_{DCx}(s) + V_{DCy}(s) &= V_{DC}(s) \\
V_{DCx}(s) - V_{DCy}(s) &= \Delta V_{DC}(s)
\end{aligned} \tag{94}$$

After the conversion into time-domain and into a matrix form, system from (93) can be expressed as shown in (95) - (97).

$$\frac{d}{dt}\mathbf{i}_{aco} = -\mathbf{L}_{aco}^{-1}\mathbf{R}_{aco}\mathbf{i}_{aco} - \mathbf{L}_{aco}^{-1}\mathbf{K}_{Vxyco}\mathbf{V}_{axy} - \mathbf{L}_{aco}^{-1}\mathbf{K}_{Vainco}\mathbf{V}_{ain} \tag{95}$$

$$\begin{aligned}
\mathbf{v}_{\text{axy}}(t) &= \begin{bmatrix} v_{ax}(t) \\ v_{ay}(t) \end{bmatrix} & \mathbf{v}_{\text{ain}}(t) &= \begin{bmatrix} v_{DCx}(t) \\ v_{DCy}(t) \\ v_{ag}(t) \end{bmatrix} & \mathbf{i}_{\text{aco}}(t) &= \begin{bmatrix} i_{ca}(t) \\ i_a(t) \end{bmatrix} \\
\mathbf{K}_{\mathbf{V}_{\text{xyco}}} &= \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} & \mathbf{K}_{\mathbf{V}_{\text{inco}}} &= \begin{bmatrix} -1 & 1 & 2 \\ -1 & -1 & 0 \end{bmatrix}
\end{aligned} \tag{96}$$

$$\begin{aligned}
\mathbf{R}_{\text{aco}} &= \begin{bmatrix} R_{ax} - R_{ay} & k_s R_{ax} + (1 - k_s) R_{ay} + 2R_{ag} \\ R_{ax} + R_{ay} & k_s R_{ax} - (1 - k_s) R_{ay} \end{bmatrix} \\
\mathbf{L}_{\text{aco}} &= \begin{bmatrix} L_{ax} - L_{ay} & k_s L_{ax} + (1 - k_s) L_{ay} + 2L_{ag} \\ L_{ax} + L_{ay} & k_s L_{ax} - (1 - k_s) L_{ay} \end{bmatrix}
\end{aligned} \tag{97}$$

Equations (95)-(97) are written in terms of output and circulating current, which was convenient for the power flow investigation in the previous section. However, for this section it may be more convenient to work with arm currents. The equations in terms of arm currents can be obtained from the circuit directly or by applying coordinate transformation to equations (95)-(97). The transformation between circulating and output current and arm currents is outlined in Equation (98).

$$\mathbf{T}_{\text{ixy}} = \begin{bmatrix} 1 & k_s \\ 1 & -(1 - k_s) \end{bmatrix}; \begin{bmatrix} i_{ax} \\ i_{ay} \end{bmatrix} = \mathbf{T}_{\text{ixy}} \begin{bmatrix} i_{ca} \\ i_a \end{bmatrix}; \begin{bmatrix} i_{ca} \\ i_a \end{bmatrix} = \mathbf{T}_{\text{ixy}}^{-1} \begin{bmatrix} i_{ax} \\ i_{ay} \end{bmatrix} \tag{98}$$

Multiplying with $\mathbf{K}_{\mathbf{V}_{\text{xyco}}}^{-1}$ and applying (98) to (95)-(97) results in equations (99)-(101).

$$\frac{d}{dt}\mathbf{i}_{\text{axy}} = -\mathbf{L}_{\text{axy}}^{-1}\mathbf{R}_{\text{axy}}\mathbf{i}_{\text{axy}} - \mathbf{L}_{\text{axy}}^{-1}\mathbf{v}_{\text{axy}} - \mathbf{L}_{\text{axy}}^{-1}\mathbf{K}_{\text{Vinxy}}\mathbf{v}_{\text{ain}} \quad (99)$$

$$\mathbf{i}_{\text{axy}}(t) = \begin{bmatrix} i_{ax}(t) \\ i_{ay}(t) \end{bmatrix} \quad \mathbf{K}_{\text{Vinxy}} = \begin{bmatrix} -1 & 0 & 1 \\ 0 & -1 & -1 \end{bmatrix} \quad (100)$$

$$\begin{aligned} \mathbf{R}_{\text{axy}} &= \begin{bmatrix} R_{ax} + R_{ag} & -R_{ag} \\ -R_{ag} & R_{ay} + R_{ag} \end{bmatrix} \\ \mathbf{L}_{\text{axy}} &= \begin{bmatrix} L_{ax} + L_{ag} & -L_{ag} \\ -L_{ag} & L_{ay} + L_{ag} \end{bmatrix} \end{aligned} \quad (101)$$

Equations (99)-(101) can now be linked with arm and module equations given in (83) and (84). The result is shown in equations (102)-(105). Note that the matrices are aggregated one step further. In the indices of terms used in the equations, $_{fa}$ denotes that the matrices belong to the equations for the filter/storage section of the a -phase modules. Terms with indices $_x$ or $_y$ alone denote only upper or lower arm while term indexed with $_{xy}$ denotes matrices aggregated for the whole converter leg.

$$\begin{aligned}
\frac{d}{dt}\mathbf{i}_{\text{axy}} = & - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^{\text{T}}(t) \mathbf{D}_{\text{faxy}} \mathbf{s}_{\text{axy}}(t) \right) \mathbf{i}_{\text{axy}}(t) \\
& - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^{\text{T}}(t) \mathbf{C}_{\text{faxy}} \right) \mathbf{x}_{\text{faxy}}(t) \\
& - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^{\text{T}}(t) \mathbf{F}_{\text{faxy}} \right) \mathbf{u}_{\text{faxy}}(t) \\
& - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{vinxy}} \right) \mathbf{v}_{\text{ain}}(t)
\end{aligned} \tag{102}$$

$$\frac{d}{dt}\mathbf{x}_{\text{faxy}}(t) = \mathbf{A}_{\text{faxy}}\mathbf{x}_{\text{faxy}}(t) + \mathbf{B}_{\text{faxy}}\mathbf{s}_{\text{axy}}(t)\mathbf{i}_{\text{axy}}(t) + \mathbf{E}_{\text{faxy}}\mathbf{u}_{\text{faxy}}(t) \tag{103}$$

$$\begin{aligned}
\mathbf{A}_{\text{faxy}} &= \begin{bmatrix} \mathbf{A}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{\text{fay}} \end{bmatrix} & \mathbf{B}_{\text{faxy}} &= \begin{bmatrix} \mathbf{B}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_{\text{fay}} \end{bmatrix} & \mathbf{E}_{\text{faxy}} &= \begin{bmatrix} \mathbf{E}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{E}_{\text{fay}} \end{bmatrix} \\
\mathbf{C}_{\text{faxy}} &= \begin{bmatrix} \mathbf{C}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_{\text{fay}} \end{bmatrix} & \mathbf{D}_{\text{faxy}} &= \begin{bmatrix} \mathbf{D}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{D}_{\text{fay}} \end{bmatrix} & \mathbf{F}_{\text{faxy}} &= \begin{bmatrix} \mathbf{F}_{\text{fax}} & \mathbf{0} \\ \mathbf{0} & \mathbf{F}_{\text{fay}} \end{bmatrix}
\end{aligned} \tag{104}$$

$$\begin{aligned}
\mathbf{x}_{\text{faxy}}(t) &= \begin{bmatrix} \mathbf{x}_{\text{fax}}(t) \\ \mathbf{x}_{\text{fay}}(t) \end{bmatrix} & \mathbf{u}_{\text{faxy}}(t) &= \begin{bmatrix} \mathbf{u}_{\text{fax}}(t) \\ \mathbf{u}_{\text{fay}}(t) \end{bmatrix} & \mathbf{s}_{\text{axy}}(t) &= \begin{bmatrix} \mathbf{s}_{\text{ax}}(t) & \mathbf{0} \\ \mathbf{0} & \mathbf{s}_{\text{ay}}(t) \end{bmatrix}
\end{aligned} \tag{105}$$

Based on (102) and (103) it is possible to assemble a non-linear switching State-Space model of the MMC converter leg:

$$\begin{aligned}
\frac{d}{dt} \begin{bmatrix} \mathbf{i}_{\text{axy}} \\ \mathbf{x}_{\text{faxy}} \end{bmatrix} = & \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^T(\mathbf{t}) \mathbf{D}_{\text{faxy}} \mathbf{s}_{\text{axy}}(\mathbf{t})) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^T(\mathbf{t}) \mathbf{C}_{\text{faxy}}) \\ \mathbf{B}_{\text{faxy}} \mathbf{s}_{\text{axy}}(\mathbf{t}) & \mathbf{A}_{\text{faxy}} \end{bmatrix} \begin{bmatrix} \mathbf{i}_{\text{axy}} \\ \mathbf{x}_{\text{faxy}} \end{bmatrix} \\
& + \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{vinxy}}) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}^T(\mathbf{t}) \mathbf{F}_{\text{faxy}}) \\ \mathbf{0} & \mathbf{E}_{\text{faxy}} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{\text{ain}} \\ \mathbf{u}_{\text{faxy}} \end{bmatrix}
\end{aligned} \tag{106}$$

5.4 Large Signal Model

The state matrices of switching model given in (106) are time variant, input dependent and only piece-wise continuous and for these reasons not really suitable for any other analysis except for time domain transient simulations. To continue the analysis of the converter, the first step is to get rid of the switching states and create a continuous model, usually referred to as large signal model.

The large signal model can be extracted from (106) using the procedure similar to the one described by Erickson *et al.* in [118]. Erickson *et al.* used linear ripple approximation to factor out switching states and express the equations in terms of duty ratio which is the control variable for the circuitry investigated in their work.

Similarly, for the analysis in this text the behavior of the converter will be approximated by the piece-wise linear solution. For the simpler notation, the system from (106) can be rewritten in more compact form as in (107).

$$\dot{\mathbf{X}}_{\mathbf{a}}(t) = \mathbf{A}_{\mathbf{a}}(t)\mathbf{X}_{\mathbf{a}}(t) + \mathbf{B}_{\mathbf{a}}(t)\mathbf{U}_{\mathbf{a}}(t) \quad (107)$$

The procedure described by Erickson *et al.* in [118] applies to a DC/DC converter with only two switching states. MMC converter in contrast can have very large number of states. As a result the linear ripple approximation outlined in [118] will not be directly applicable to MMC and the procedure will have to be generalized to some extent. Modulation plays important part in the modeling shown in [118]. As a result, before the model can be formulated PWM specific to the MMC must be investigated.

5.4.1 MMC Modulation Aspects

In the case of DC/DC converter analyzed [118] linearizing solution and factoring out switching states from the model is straightforward as the converter has only few possible switching states and a rigid structure. The linearization could be done across one switching interval. This allowed the authors to model the converter in terms of duty ratio instead of the switching states. In the case of the MMC converter the procedure will be different due to the following considerations:

- The number of levels in the MMC converter and consequent different switching states can be very high. Conceptually the number of levels can be infinite and so can be the number of switching states.
- In contrast to DC/DC converter where the large signal model can be expressed using

the duty ratio, the MMC converter model will have to be formulated in terms of modulation index.

- Modulation index and its relation to the switching states will depend on the modulation type and the balancing algorithm. In order to "extract" modulation index from switching states, proper observation period has to be identified. For MMC converters one can distinguish between effective switching period (T_{sw}) and component or module switching period (T_s) as illustrated in Figure 27 and Figure 28. Effective and module switching periods can be described in the following manner:

- The effective switching period is visible from the output terminals and is the effect that determines the output ripple.
- The module or component switching period (or just switching period) is the switching sequence period seen from the standpoint of one module and in case of simple module implementations from the standpoint of the switching component.
- Effective and module switching periods are not the same for most implementations of MMC converter and the relation of the two will depend on PWM type.
- In the case of the phase-shifted carrier PWM illustrated in Figure 27, the module switching period is the period of the carrier. If the carrier phase shifts are uniform and the number of modules in the converter arm is N , the effective switching period is easily identified as T_s/N . The effective switching period can also be easily identified as a width of the lowermost triangles from the carrier waveform illustrated in Figure 27. Balancing is in this case linear and will not influence

switching pattern but will be reflected in the modulation index extracted from the switching states.

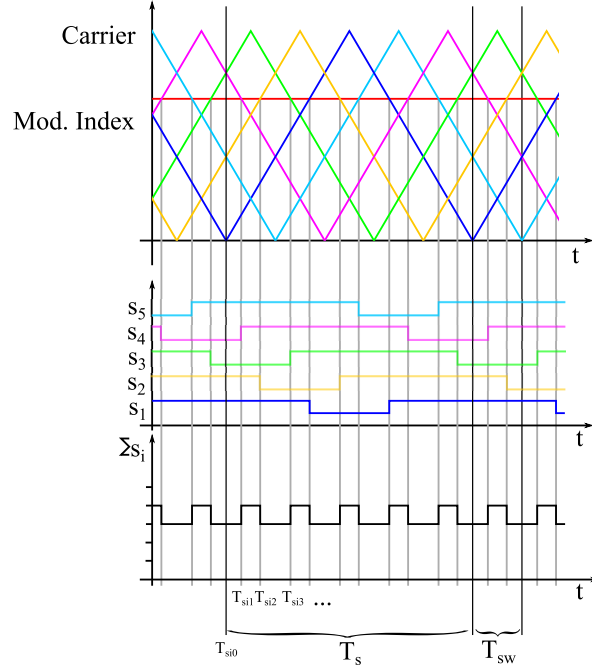


Figure 27: Ideal phase-shifted PWM. The graphs illustrate: carrier, approximately constant modulation index, individual module PWM and aggregate output PWM for 5 level modulator. The color of the signals show correlation between carrier and module PWM.

- For the level-shifted carrier PWM shown in Figure 28 the effective switching period can be easily identified. The effective switching period T_{sw} is equal to the period of the carrier. The module switching period, on the other hand, cannot be easily determined without the effects of the balancing algorithm. If the balancing algorithm is excluded, the module switching period will not be consistent for all modules or across time and will depend on the modulation index value as illustrated in Figure 28-(a). The balancing algorithm must be included in the analysis to make the module periods consistent and switching states relatable to the modulation index. The balancing algorithm will sort the modules according to

their DC bus state of charge or voltage and assign them different "level" carriers in order to spread the energy equally across the modules. Eventually all modules will cycle through the same "level" of the carrier as shown in Figure 28-(b). In the ideal case, if the number of modules in the converter arm is N and the balancing algorithm operates once per switching period T_{sw} , it will take NT_{sw} to cycle through all modules which will in this case determine the module switching period.

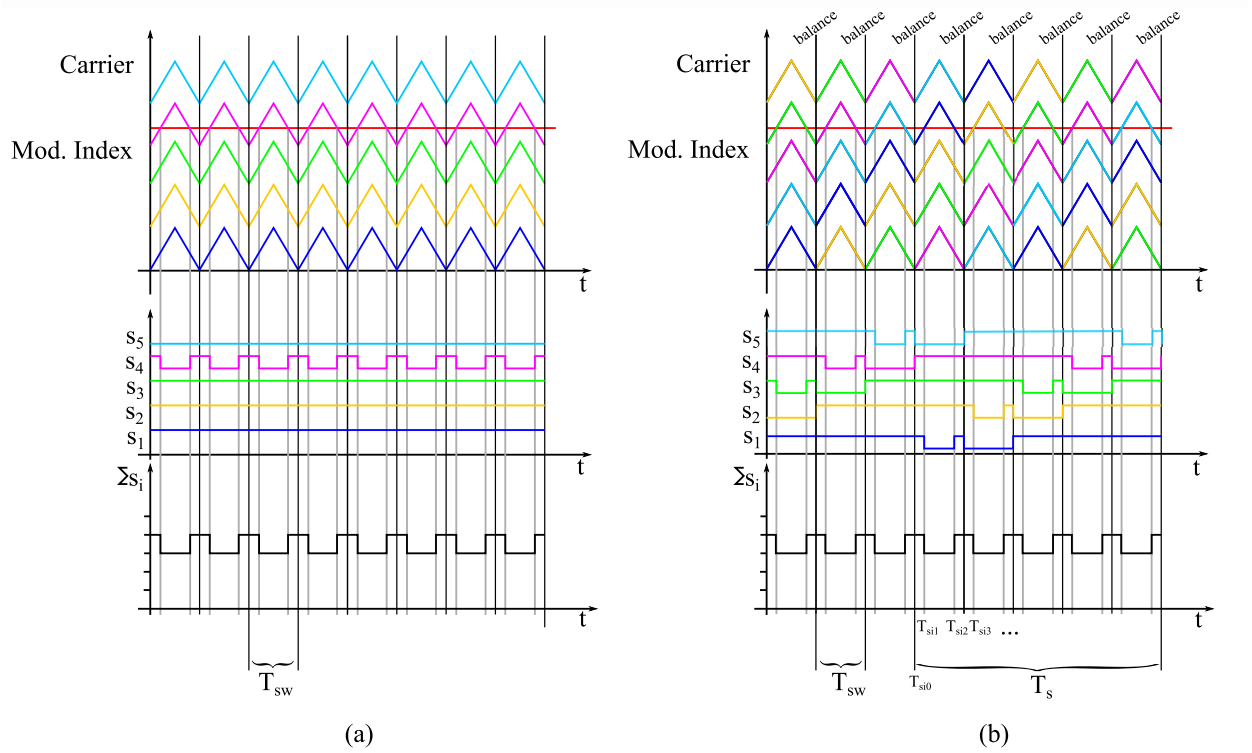


Figure 28: (a) - Ideal level-shifted carrier PWM. The modulation does not show the effects of balancing algorithm. (b) - Level-shifted carrier modulation. The color of the signals show correlation between carrier and module PWM. Modulation index is shown constant which is approximately true for high switching frequencies.

- To summarize, the effective switching period is the minimum, ripple generating period and the effective switching period can be loosely defined as the period of the repeating sequence of the switching states for a single module switching

section.

- To extract the modulation index from the switching states it is necessary to observe the longer interval, which is in both PWM cases module switching period.
- This means that contrast to DC/DC converters with only two switching states, the MMC will have much higher numbers of switching states per observed interval.

5.4.2 Linear Ripple Approximation Generalization

The first step in obtaining the large signal model is to represent the solution of the differential equation given in (107) around switching instance T_{si0} illustrated in Figure 27 and Figure 28 using Taylor expansion as shown in Equation (108).

$$\mathbf{X}_{\mathbf{a}}(t) = \mathbf{X}_{\mathbf{a}}(T_{si0}) + \frac{\frac{d}{dt}\mathbf{X}_{\mathbf{a}}(T_{si0})}{1!}(t - T_{si0}) + \underbrace{\frac{\frac{d^2}{dt^2}\mathbf{X}_{\mathbf{a}}(T_{si0})}{2!}(t - T_{si0})^2 + \dots}_{\text{H.O.T.}} \quad (108)$$

Similar to the procedure in [118] the solution expressed in (108) can be linearized between successive switching instances marked as T_{si0} and T_{si1} in Figure 27 and Figure 28 by neglecting the higher order terms marked as H.O.T. in (108). The linear version of the model state is shown in (109). The simplification here is only that the ripple (change in the solution between two switching instances) is linear.

$$\mathbf{X}_{\mathbf{a}}(t) = \mathbf{X}_{\mathbf{a}}(T_{si0}) + \frac{\frac{d}{dt}\mathbf{X}_{\mathbf{a}}(T_{si0})}{1!}(t - T_{si0}) \quad (109)$$

for $T_{si0} \leq t < T_{si1}$

The derivative $\frac{d}{dt}\mathbf{X}_a(T_{si0})$ can be replaced with (107) as shown in (110).

$$\begin{aligned}\mathbf{X}_a(t) &= \mathbf{X}_a(T_{si0}) + [\mathbf{A}_a(T_{si0})\mathbf{X}_a(T_{si0}) + \mathbf{B}_a(T_{si0})\mathbf{U}_a(T_{si0})](t - T_{si0}) \\ &\text{for } T_{si0} \leq t < T_{si1}\end{aligned}\tag{110}$$

It is assumed that the $\mathbf{X}_a(T_{si0})$ are initial conditions for the first switching interval, which are known. At the end of the first switching interval the solution can be expressed with Equation (111), which is rewritten in more convenient form in (112).

$$\begin{aligned}\mathbf{X}_a(T_{si1}) &= \mathbf{X}_a(T_{si0}) + \left[\mathbf{A}_a(T_{si0})\mathbf{X}_a(T_{si0}) + \mathbf{B}_a(T_{si0})\mathbf{U}_a(T_{si0}) \right] \Delta t_0 \\ \Delta t_0 &= T_{si1} - T_{si0}\end{aligned}\tag{111}$$

$$\mathbf{X}_a(T_{si1}) = \left[\mathbf{I} + \mathbf{A}_a(T_{si0})\Delta t_0 \right] \mathbf{X}_a(T_{si0}) + \mathbf{B}_a(T_{si0})\mathbf{U}_a(T_{si0})\Delta t_0\tag{112}$$

The next switching interval between T_{si1} and T_{si2} can be described in the same manner as shown in (113).

$$\begin{aligned}\mathbf{X}_a(t) &= \mathbf{X}_a(T_{si1}) + \left[\mathbf{A}_a(T_{si1})\mathbf{X}_a(T_{si1}) + \mathbf{B}_a(T_{si1})\mathbf{U}_a(T_{si1}) \right] (t - T_{si1}) \\ &\text{for } T_{si1} \leq t < T_{si2}\end{aligned}\tag{113}$$

Substituting (112) in (113) and expressing the solution at the end of the interval, at the point T_{si2} , results in (114).

$$\begin{aligned}
\mathbf{X}_{\mathbf{a}}(T_{si2}) = & \left[\mathbf{I} + \mathbf{A}_{\mathbf{a}}(T_{si0})\Delta t_0 + \mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1 \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\
& + \mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0})\Delta t_0 \\
& + \mathbf{B}_{\mathbf{a}}(T_{si1})\mathbf{U}_{\mathbf{a}}(T_{si1})\Delta t_1 \\
& + \mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{A}_{\mathbf{a}}(T_{si0})\mathbf{X}_{\mathbf{a}}(T_{si0})\Delta t_0\Delta t_1 \\
& + \mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0})\Delta t_0\Delta t_1
\end{aligned} \tag{114}$$

$$\Delta t_1 = T_{si2} - T_{si1}$$

In the same way as in [118] the quadratic terms in (114) can be neglected. The justification for this step can be summarized as follows:

- The last two terms from (114) have quadratic factors like $\Delta t_0\Delta t_1$, $\mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{A}_{\mathbf{a}}$ and $\mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{B}_{\mathbf{a}}(T_{si0})$. These two terms can be rewritten as in (115)

$$\begin{aligned}
& \mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{A}_{\mathbf{a}}(T_{si0})\mathbf{X}_{\mathbf{a}}(T_{si0})\Delta t_0\Delta t_1 + \mathbf{A}_{\mathbf{a}}(T_{si1})\mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0})\Delta t_0\Delta t_1 \\
& = \mathbf{A}_{\mathbf{a}}(T_{si1}) \left[\left(\mathbf{A}_{\mathbf{a}}(T_{si0})\mathbf{X}_{\mathbf{a}}(T_{si0}) + \mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0}) \right) \Delta t_0 \right] \Delta t_1
\end{aligned} \tag{115}$$

- Substituting (111) in (115) results in (116).

$$\begin{aligned}
& \mathbf{A}_{\mathbf{a}}(T_{si1}) \left[\left(\mathbf{A}_{\mathbf{a}}(T_{si0}) \mathbf{X}_{\mathbf{a}}(T_{si0}) + \mathbf{B}_{\mathbf{a}}(T_{si0}) \mathbf{U}_{\mathbf{a}}(T_{si0}) \right) \Delta t_0 \right] \Delta t_1 \\
&= \mathbf{A}_{\mathbf{a}}(T_{si1}) \left[\mathbf{X}_{\mathbf{a}}(T_{si1}) - \mathbf{X}_{\mathbf{a}}(T_{si0}) \right] \Delta t_1 \\
&= \mathbf{A}_{\mathbf{a}}(T_{si1}) \Delta t_1 \Delta \mathbf{X}_{\mathbf{a}}(T_{si1})
\end{aligned} \tag{116}$$

- Term $\Delta \mathbf{X}_{\mathbf{a}}(T_{si1})$ represents the change in the state values during one switching interval, which is in case of the MMC converter much shorter than the module (component) switching interval. States $\mathbf{X}_{\mathbf{a}}(t)$ in (106) are MMC arm currents and module states. Module states are capacitor and storage voltages as well as storage currents. All these signals are filtered by design and will have slow rate of change making the change of these signals during of one switching period (or ripple) much smaller than the average values of the states.
- Comparing (116) and (114) it is evident that the quadratic terms are smaller than the rest of the terms in (114), this is true even in an absence of input signals as expressed in Equation (117). Smaller in this case means that the norm is smaller. $\|\cdot\|$ in (117) denotes vector 2-norm and its induced matrix norm.

$$\left\{ \begin{aligned} &\|\Delta \mathbf{X}_{\mathbf{a}}(T_{si1})\| \ll \|\mathbf{X}_{\mathbf{a}}(T_{si0})\|; \\ &\|\mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1\| < \|\mathbf{I} + \mathbf{A}_{\mathbf{a}}(T_{si0})\Delta t_0 + \mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1\| \end{aligned} \right\} \quad (117)$$

\Rightarrow

$$\|\mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1\Delta \mathbf{X}_{\mathbf{a}}(T_{si1})\| \ll \left\| \left[\mathbf{I} + \mathbf{A}_{\mathbf{a}}(T_{si0})\Delta t_0 + \mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1 \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \right\|$$

After neglecting the quadratic terms in (111), the resulting equation is given in (118).

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}(T_{si2}) = & \left[\mathbf{I} + \mathbf{A}_{\mathbf{a}}(T_{si0})\Delta t_0 + \mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1 \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\ & + \mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0})\Delta t_0 \\ & + \mathbf{B}_{\mathbf{a}}(T_{si1})\mathbf{U}_{\mathbf{a}}(T_{si1})\Delta t_1 \end{aligned} \quad (118)$$

In the same manner the reasoning can be extended to the third switching interval as shown in (119)

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}(T_{si3}) = & \left[\mathbf{I} + \mathbf{A}_{\mathbf{a}}(T_{si0})\Delta t_0 + \mathbf{A}_{\mathbf{a}}(T_{si1})\Delta t_1 + \mathbf{A}_{\mathbf{a}}(T_{si2})\Delta t_2 \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\ & + \mathbf{B}_{\mathbf{a}}(T_{si0})\mathbf{U}_{\mathbf{a}}(T_{si0})\Delta t_0 \\ & + \mathbf{B}_{\mathbf{a}}(T_{si1})\mathbf{U}_{\mathbf{a}}(T_{si1})\Delta t_1 \\ & + \mathbf{B}_{\mathbf{a}}(T_{si2})\mathbf{U}_{\mathbf{a}}(T_{si2})\Delta t_2 \end{aligned} \quad (119)$$

If the procedure is continued for the remaining switching intervals within one module

switching period, (119) can be rewritten as (120). The reason for the choice of module switching period, which is longer switching period as described above will be evident later in the text.

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}(T_{si\nu}) = \mathbf{X}_{\mathbf{a}}(T_{si0}) &+ \left[\sum_{n=0}^{\nu-1} \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\ &+ \sum_{n=0}^{\nu-1} \left[\mathbf{B}_{\mathbf{a}}(T_{si[n]}) \mathbf{U}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \end{aligned} \quad (120)$$

For generality purposes, it can be assumed that the number of switching intervals is ν during the current module switching period. This is also shown in Equation (121). Note that triangle carrier PWM as illustrated in Figure 27 and Figure 28 will create up to three switching intervals per one effective switching period as opposed to saw-tooth carrier PWM that can create up to two switching intervals per one effective switching period, depending on how the modulation index waveform intersects with carrier waveforms. There will be N effective switching periods per one module switching period for the MMC converter leg with N modules per arm. This means that the number of intervals can be fairly high and is not constant.

$$\sum_{i=0}^{\nu-1} \Delta t_i = T_s \quad (121)$$

If the number of switching intervals per module switching period is ν , based on the reasoning above the following can be stated:

- The beginning of the module switching period will be at T_{si0}
- The last interval of the switching period will begin at $T_{si(\nu-1)}$
- The beginning of the next switching interval will be $T_{si\nu}$

The link between two module switching periods can in this case be expressed as in (122).

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}(T_{si\nu}) = \mathbf{X}_{\mathbf{a}}(T_{si0}) &+ \left[\sum_{n=0}^{\nu-1} \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\ &+ \sum_{n=0}^{\nu-1} \left[\mathbf{B}_{\mathbf{a}}(T_{si[n]}) \mathbf{U}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \end{aligned} \quad (122)$$

As will be shown below it is convenient to assume that the converter input signal is sampled once per module switching period, at the beginning of the module switching interval. This is not far from the truth for digital controllers where the signals are sampled once per switching period, which is usually the control loop period. In this case Equation (122) can be rewritten as (123).

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}(T_{si\nu}) = \mathbf{X}_{\mathbf{a}}(T_{si0}) &+ \left[\sum_{n=0}^{\nu-1} \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\ &+ \left[\sum_{n=0}^{\nu-1} \mathbf{B}_{\mathbf{a}}(T_{si[n]}) \Delta t_n \right] \mathbf{U}_{\mathbf{a}}(T_{si0}) \end{aligned} \quad (123)$$

Matrices $\mathbf{A}_{\mathbf{a}}$ and $\mathbf{B}_{\mathbf{a}}$ change only at the switching instances and are constant between switching instance, which is evident from the structure of these matrices as given in (107), (106) and earlier in the text. The matrices are constant during each switching interval n bounded by $[T_{si[n]}, T_{si[n+1]})$. The boundaries are illustrated in Figure 27 and Figure 28. As a

consequence, sums in (123) can be replaced with integrals. The reasoning for this is outlined in (124).

$$\begin{aligned}
\mathbf{A}_{\mathbf{a}}(t) &= \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \text{ for } t \in [T_{si[n]}, T_{si[n+1]}) \\
&\Rightarrow \\
\int_{T_{si0}}^{T_{si\nu}} \mathbf{A}_{\mathbf{a}}(t) dt &= \\
&= \sum_{n=0}^{\nu-1} \left[\int_{T_{si(n)}}^{T_{si(n+1)}} \mathbf{A}_{\mathbf{a}}(t) dt \right] \\
&= \sum_{n=0}^{\nu-1} \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \left[\int_{T_{si[n]}}^{T_{si(n+1)}} dt \right] \\
&= \sum_{n=0}^{\nu-1} \mathbf{A}_{\mathbf{a}}(T_{si[n]}) \Delta t_n
\end{aligned} \tag{124}$$

The sums from (123) can be replaced with integrals as shown in (125).

$$\begin{aligned}
\mathbf{X}_{\mathbf{a}}(T_{si\nu}) &= \mathbf{X}_{\mathbf{a}}(T_{si0}) + \left[\int_{T_{si0}}^{T_{si\nu}} \mathbf{A}_{\mathbf{a}}(t) dt \right] \mathbf{X}_{\mathbf{a}}(T_{si0}) \\
&\quad + \left[\int_{T_{si0}}^{T_{si\nu}} \mathbf{B}_{\mathbf{a}}(t) dt \right] \mathbf{U}_{\mathbf{a}}(T_{si0})
\end{aligned} \tag{125}$$

Time instance T_{si0} denotes the start of a module switching interval and time instance $T_{si\nu}$ denotes the start of the next switching interval. As long as the states at the start of the module switching interval T_{si0} are known, the state at the start of the next module switching

interval $T_{si\nu}$ can be found.

In contrast to the equations (109)-(112) that describe the system between two (effective) switching intervals which can be of different length, Equation (125) describes the system at the constant module switching period. As a consequence, system can be expressed in the form of difference equations as in (126).

$$\begin{aligned} \mathbf{X}_{\mathbf{a}}((n+1)T_s) = \mathbf{X}_{\mathbf{a}}(nT_s) &+ \left[\int_{nT_s}^{(n+1)T_s} \mathbf{A}_{\mathbf{a}}(t)dt \right] \mathbf{X}_{\mathbf{a}}(nT_s) \\ &+ \left[\int_{nT_s}^{(n+1)T_s} \mathbf{B}_{\mathbf{a}}(t)dt \right] \mathbf{U}_{\mathbf{a}}(nT_s) \end{aligned} \quad (126)$$

5.4.3 Large Signal System Model Matrices

To obtain state matrices of the system, the integrals in (126) have to be evaluated. Fortunately, the only time dependent term is the switching state matrix $s_{axy}(t)$.

Matrix $\mathbf{A}_{\mathbf{a}}(nT_s)$ and the structure of corresponding integral is given in (127).

$$\begin{aligned} \mathbf{A}_{\mathbf{a}}(nT_s) = \int_{nT_s}^{(n+1)T_s} \mathbf{A}_{\mathbf{a}}(t)dt = \\ \int_{nT_s}^{(n+1)T_s} \left[\begin{array}{cc} -(\mathbf{L}_{\mathbf{axy}}^{-1}\mathbf{R}_{\mathbf{axy}} + \mathbf{L}_{\mathbf{axy}}^{-1}\mathbf{s}_{\mathbf{axy}}^T(\mathbf{t})\mathbf{D}_{\mathbf{faxy}}\mathbf{s}_{\mathbf{axy}}(\mathbf{t})) & -(\mathbf{L}_{\mathbf{axy}}^{-1}\mathbf{s}_{\mathbf{axy}}(\mathbf{t})^T\mathbf{C}_{\mathbf{faxy}}) \\ \mathbf{B}_{\mathbf{faxy}}\mathbf{s}_{\mathbf{axy}}(\mathbf{t}) & \mathbf{A}_{\mathbf{faxy}} \end{array} \right] dt \end{aligned} \quad (127)$$

Integral for each element of the matrix given in (127) will be evaluated individually below.

Integral of the element at (1,1) has two terms which will be evaluated individually.

First term is straightforward to evaluate and the solution of the integral is given in (128).

$$\int_{nT_s}^{(n+1)T_s} \mathbf{L}_{\mathbf{axy}}^{-1} \mathbf{R}_{\mathbf{axy}} dt = \mathbf{L}_{\mathbf{axy}}^{-1} \mathbf{R}_{\mathbf{axy}} T_s \quad (128)$$

Second term, at (1,1) in Matrix shown in Equation (127) is a bit more complicated and the structure of the corresponding integral is given in (129).

$$\int_{nT_s}^{(n+1)T_s} \mathbf{L}_{\mathbf{axy}}^{-1} \mathbf{s}_{\mathbf{axy}}(\mathbf{t})^T \mathbf{D}_{\mathbf{faxy}} \mathbf{s}_{\mathbf{axy}}(\mathbf{t}) dt \quad (129)$$

Matrix $\mathbf{D}_{\mathbf{faxy}}$ is diagonal. As a result, term $\mathbf{s}_{\mathbf{axy}}(\mathbf{t})^T \mathbf{D}_{\mathbf{faxy}} \mathbf{s}_{\mathbf{axy}}(\mathbf{t})$ can be rewritten as shown in (130).

$$\begin{aligned} \mathbf{s}_{\mathbf{axy}}(\mathbf{t})^T \mathbf{D}_{\mathbf{faxy}} \mathbf{s}_{\mathbf{axy}}(\mathbf{t}) = \\ \begin{bmatrix} \sum_{i=1}^N s_{ax[i]}(t) D_{fax[i]} s_{ax[i]}(t) & 0 \\ 0 & \sum_{i=1}^N s_{ay[i]}(t) D_{fay[i]} s_{ay[i]}(t) \end{bmatrix} \end{aligned} \quad (130)$$

Terms $D_{fax[i]}$ are given in Chapter 5.1 and can be only scalars. As a consequence, the multiplication in the sums is commutative. Also, matrix $\mathbf{L}_{\mathbf{axy}}^{-1}$ is constant. As a result, integral in (130) can be rewritten as (131)

$$\begin{aligned}
& \int_{nT_s}^{(n+1)T_s} \mathbf{L}_{\mathbf{axy}}^{-1} \mathbf{s}_{\mathbf{axy}}^T(\mathbf{t}) \mathbf{D}_{\mathbf{faxy}} \mathbf{s}_{\mathbf{axy}}(\mathbf{t}) dt = \\
& \mathbf{L}_{\mathbf{axy}}^{-1} \begin{bmatrix} \sum_{i=1}^N \left(D_{fax[i]} \int_{nT_s}^{(n+1)T_s} s_{ax[i]}^2(t) dt \right) & 0 \\ 0 & \sum_{i=1}^N \left(D_{fay[i]} \int_{nT_s}^{(n+1)T_s} s_{ay[i]}^2(t) dt \right) \end{bmatrix} \quad (131)
\end{aligned}$$

As defined earlier in the text, the switching states take only the values of 1 and 0 so they are invariant to the power operator: $s_{ax[i]}^2(t) = s_{ax[i]}(t)$ and $s_{ay[i]}^2(t) = s_{ay[i]}(t)$. It was also shown in Chapter 4 that the modulation index can be extracted from switching states. The equations were given in (8) and (9). Following from (8) and (9), modulation indexes can be expressed as shown in (132).

$$\begin{aligned}
& s_{ax[i]}, s_{ay[i]} \in \{0, 1\} \Rightarrow \\
& m_{ax[i]}(nT_s) = \frac{T_{ONax[i]}(t)}{T_s} = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ax[i]}(t) dt = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ax[i]}^2(t) dt \\
& m_{ay[i]}(nT_s) = \frac{T_{ONay[i]}(t)}{T_s} = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ay[i]}(t) dt = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} s_{ay[i]}^2(t) dt \quad (132)
\end{aligned}$$

Comparing (131) and (132) it is possible to rewrite the integrals from (131) as:

$$\begin{aligned}
& \int_{nT_s}^{(n+1)T_s} \mathbf{L}_{\mathbf{axy}}^{-1} \mathbf{s}_{\mathbf{axy}}^T(\mathbf{t}) \mathbf{D}_{\mathbf{faxy}} \mathbf{s}_{\mathbf{axy}}(\mathbf{t}) dt = \\
& T_s \mathbf{L}_{\mathbf{axy}}^{-1} \begin{bmatrix} \sum_{i=1}^N (D_{fax[i]} m_{ax[i]}(nT_s)) & 0 \\ 0 & \sum_{i=1}^N (D_{fay[i]} m_{ay[i]}(nT_s)) \end{bmatrix} \quad (133)
\end{aligned}$$

To put (133) back into matrix form it is convenient to introduce new matrices given in (134) and (135). Matrix \mathbf{S}_a has constant elements and can be seen as structural matrix reflecting the arrangement of the module switching elements in the higher (arm and leg) structures. It can be obtained by setting all switching states at 1 in the switching state matrix $\mathbf{s}_{\mathbf{axy}}(t)$ as defined in (105). Matrix $\mathbf{m}_{\mathbf{ax}}(\mathbf{t})$ can be seen as modulation matrix.

$$\begin{aligned}
\mathbf{m}_{\mathbf{ax}}(\mathbf{t}) &= \begin{bmatrix} m_{ax[1]}(t) & 0 & \dots & 0 \\ 0 & m_{ax[2]}(t) & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & m_{ax[N]}(t) \end{bmatrix} \\
\mathbf{m}_{\mathbf{ay}}(\mathbf{t}) &= \begin{bmatrix} m_{ay[1]}(t) & 0 & \dots & 0 \\ 0 & m_{ay[2]}(t) & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & m_{ay[N]}(t) \end{bmatrix} \quad (134)
\end{aligned}$$

$$\mathbf{m}_{\text{axy}}(\mathbf{t}) = \begin{bmatrix} \mathbf{m}_{\text{ax}}(\mathbf{t}) & \mathbf{0} \\ \mathbf{0} & \mathbf{m}_{\text{ay}}(\mathbf{t}) \end{bmatrix} \quad \mathbf{S}_{\mathbf{a}} = \begin{bmatrix} \mathbf{1}_{N \times 1} & \mathbf{0}_{N \times 1} \\ \mathbf{0}_{N \times 1} & \mathbf{1}_{N \times 1} \end{bmatrix} \quad (135)$$

Integral in (133) can be rewritten now as shown in (136).

$$\int_{nT_s}^{(n+1)T_s} \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{axy}}^T(\mathbf{t}) \mathbf{D}_{\text{faxy}} \mathbf{S}_{\text{axy}}(\mathbf{t}) d\mathbf{t} = \quad (136)$$

$$T_s \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{D}_{\text{fax}} \mathbf{m}_{\text{axy}}(nT_s) \mathbf{S}_{\mathbf{a}}$$

Element 1,1 integral can now be rewritten as:

$$\int_{nT_s}^{(n+1)T_s} - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{axy}}^T(\mathbf{t}) \mathbf{D}_{\text{faxy}} \mathbf{S}_{\text{axy}}(\mathbf{t}) \right) d\mathbf{t} = \quad (137)$$

$$- T_s \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{D}_{\text{faxy}} \mathbf{m}_{\text{axy}}(nT_s) \mathbf{S}_{\mathbf{a}} \right)$$

Integral of the element at (1,2) can be expressed in terms of modulation index as shown in (138). The reasoning is the same as for the integral of the element at (1,1).

$$\int_{nT_s}^{(n+1)T_s} - \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{axy}}(\mathbf{t})^T \mathbf{C}_{\text{faxy}} \right) d\mathbf{t} = -T_s \left(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{m}_{\text{axy}}(nT_s) \mathbf{C}_{\text{faxy}} \right) \quad (138)$$

Integral of the element at (2,1) can be obtained in the same manner and is given in (139).

$$\int_{nT_s}^{(n+1)T_s} \mathbf{B}_{\text{faxy}} \mathbf{s}_{\text{axy}}(\mathbf{t}) dt = T_s \mathbf{B}_{\text{faxy}} \mathbf{m}_{\text{axy}}(\mathbf{nT}_s) \mathbf{S}_{\mathbf{a}} \quad (139)$$

Integral of the element at (2,2) integral is straightforward is given in (140).

$$\int_{nT_s}^{(n+1)T_s} \mathbf{A}_{\text{faxy}} dt = T_s \mathbf{A}_{\text{faxy}} \quad (140)$$

Matrix $\mathbf{A}_{\mathbf{a}}(nT_s)$ can now be expressed as:

$$\mathbf{A}_{\mathbf{a}}(nT_s) = T_s \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{D}_{\text{faxy}} \mathbf{m}_{\text{axy}}(\mathbf{nT}_s) \mathbf{S}_{\mathbf{a}}) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{m}_{\text{axy}}(\mathbf{nT}_s) \mathbf{C}_{\text{faxy}}) \\ \mathbf{B}_{\text{faxy}} \mathbf{m}_{\text{axy}}(\mathbf{nT}_s) \mathbf{S}_{\mathbf{a}} & \mathbf{A}_{\text{faxy}} \end{bmatrix} \quad (141)$$

Matrix $\mathbf{B}_{\mathbf{a}}(nT_s)$ and the structure of corresponding integral is given in (142).

$$\mathbf{B}_{\mathbf{a}}(nT_s) = \int_{nT_s}^{(n+1)T_s} \mathbf{B}_{\mathbf{a}}(t) dt = \int_{nT_s}^{(n+1)T_s} \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{Vinxy}}) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{axy}}^T(\mathbf{t}) \mathbf{F}_{\text{faxy}}) \\ \mathbf{0} & \mathbf{E}_{\text{faxy}} \end{bmatrix} dt \quad (142)$$

Each element of the matrix integral from (142) are evaluated below.

Integral of the element at (1,1) is straightforward to evaluate and is given in (143).

$$\int_{nT_s}^{(n+1)T_s} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{vinxy}}) dt = -T_s (\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{vinxy}}) \quad (143)$$

Integral of the element at (1,2) is similar to the integral of the element at (1,2) of matrix $A_a(nT_s)$ and can be evaluated using the similar reasoning. The result is given in (144).

$$\int_{nT_s}^{(n+1)T_s} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{s}_{\text{axy}}(\mathbf{t})^T \mathbf{F}_{\text{faxy}}) dt = -T_s (\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\mathbf{a}}^T \mathbf{m}_{\text{axy}}(\mathbf{nT}_s) \mathbf{F}_{\text{faxy}}) \quad (144)$$

Integral of the element at (2,2) and (2,1) are straightforward to evaluate as well. Matrix \mathbf{E}_{faxy} is constant, the corresponding integral is given in (145). The element at (2,1) is constant 0-matrix making the integral solution the same 0-matrix.

$$\int_{nT_s}^{(n+1)T_s} \mathbf{E}_{\text{faxy}} dt = -T_s \mathbf{E}_{\text{faxy}} \quad (145)$$

Matrix $\mathbf{B}_{\mathbf{a}}(nT_s)$ can now be expressed as:

$$\mathbf{B}_a(nT_s) = T_s \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{Viny}}) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_a^T \mathbf{m}_{\text{axy}}(nT_s) \mathbf{F}_{\text{faxy}}) \\ \mathbf{0} & \mathbf{E}_{\text{faxy}} \end{bmatrix} \quad (146)$$

5.4.4 Large Signal State Space Equation

Difference equation with sampling time T_s can now be expressed as shown in (147).

$$\begin{aligned} \mathbf{X}_a((n+1)T_s) &= \mathbf{X}_a(nT_s) \\ &+ T_s \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_a^T \mathbf{D}_{\text{faxy}} \mathbf{m}_{\text{axy}}(nT_s) \mathbf{S}_a) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_a^T \mathbf{m}_{\text{axy}}(nT_s) \mathbf{C}_{\text{faxy}}) \\ \mathbf{B}_{\text{faxy}} \mathbf{m}_{\text{axy}}(nT_s) \mathbf{S}_a & \mathbf{A}_{\text{faxy}} \end{bmatrix} \mathbf{X}_a(nT_s) \\ &+ T_s \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{K}_{\text{Viny}}) & -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_a^T \mathbf{m}_{\text{axy}}(nT_s) \mathbf{F}_{\text{faxy}}) \\ \mathbf{0} & \mathbf{E}_{\text{faxy}} \end{bmatrix} \mathbf{U}_a(nT_s) \end{aligned} \quad (147)$$

To obtain the continuous time system, forward difference approximation for the derivative given in (148) can be used.

$$\frac{d}{dt} \mathbf{X}_a(\mathbf{t}) \approx \frac{\mathbf{X}_a(\mathbf{t} + \mathbf{T}_s) - \mathbf{X}_a(\mathbf{t})}{T_s} \quad (148)$$

Comparing (147) and (148) and nT_s with t and $(n+1)T_s$ with $t + Ts$, the continuous time model can be obtained as shown in (149).

$$\begin{aligned}
\frac{d}{dt} \mathbf{X}_a(t) = & \begin{bmatrix} -(\mathbf{L}_{axy}^{-1} \mathbf{R}_{axy} + \mathbf{L}_{axy}^{-1} \mathbf{S}_a^T \mathbf{D}_{faxy} \mathbf{m}_{axy}(t) \mathbf{S}_a) & -(\mathbf{L}_{axy}^{-1} \mathbf{S}_a^T \mathbf{m}_{axy}(t) \mathbf{C}_{faxy}) \\ \mathbf{B}_{faxy} \mathbf{m}_{axy}(t) \mathbf{S}_a & \mathbf{A}_{faxy} \end{bmatrix} \mathbf{X}_a(t) \\
+ & \begin{bmatrix} -(\mathbf{L}_{axy}^{-1} \mathbf{K}_{Vinyx}) & -(\mathbf{L}_{axy}^{-1} \mathbf{S}_a^T \mathbf{m}_{axy}(t) \mathbf{F}_{faxy}) \\ \mathbf{0} & \mathbf{E}_{faxy} \end{bmatrix} \mathbf{U}_a(t)
\end{aligned} \tag{149}$$

The averaged model from Equation (149) can be represented as a circuit model. This the circuit diagram of the averaged model is given in Figure 29.

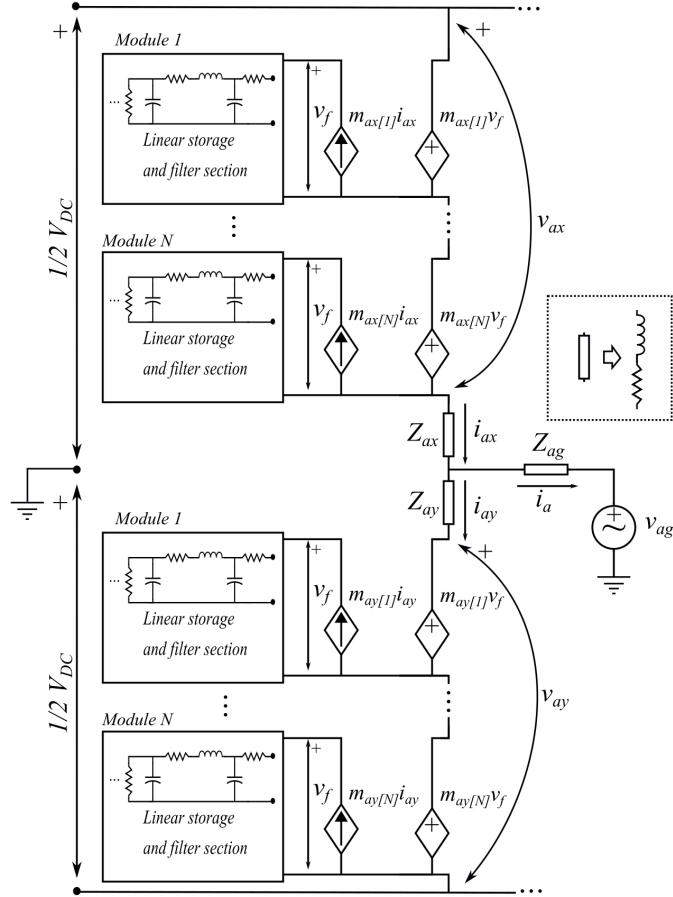


Figure 29: The circuit diagram for the averaged MMC model given in Equation 149.

Model from (149) has modulation index matrices incorporated in state matrices of the model making the system fairly uncomfortable to handle. With some matrix manipulations the system can be expressed as shown in (150).

$$\begin{aligned}
\frac{d}{dt}\mathbf{X}_a(t) = & \left(\begin{bmatrix} -\mathbf{L}_{\text{axy}}^{-1}\mathbf{R}_{\text{axy}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{\text{faxy}} \end{bmatrix} + \right. \\
& \left. \begin{bmatrix} -\mathbf{L}_{\text{axy}}^{-1}\mathbf{S}_a^T\mathbf{D}_{\text{faxy}} & -\mathbf{L}_{\text{axy}}^{-1}\mathbf{S}_a^T \\ \mathbf{B}_{\text{faxy}} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{m}_{\text{axy}}(t) & \mathbf{0} \\ \mathbf{0} & \mathbf{m}_{\text{axy}}(t) \end{bmatrix} \begin{bmatrix} \mathbf{S}_a & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_{\text{faxy}} \end{bmatrix} \right) \mathbf{X}_a(t) + \\
& \left(\begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1}\mathbf{K}_{\text{Viny}}) & \mathbf{0} \\ \mathbf{0} & \mathbf{E}_{\text{faxy}} \end{bmatrix} + \right. \\
& \left. \begin{bmatrix} \mathbf{0} & -(\mathbf{L}_{\text{axy}}^{-1}\mathbf{S}_a^T) \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{m}_{\text{axy}}(t) & \mathbf{0} \\ \mathbf{0} & \mathbf{m}_{\text{axy}}(t) \end{bmatrix} \begin{bmatrix} \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{F}_{\text{faxy}} \end{bmatrix} \right) \mathbf{U}_a(t)
\end{aligned} \tag{150}$$

Equation (150) can be rewritten as shown in (151) where the system is expressed in terms of constant matrices and time varying modulation matrix.

$$\frac{d}{dt}\mathbf{X}_a(t) = (\mathbf{A}_{1a} + \mathbf{A}_{2a}\mathbf{M}_a(t)\mathbf{A}_{3a}) \mathbf{X}_a(t) + (\mathbf{B}_{1a} + \mathbf{B}_{2a}\mathbf{M}_a(t)\mathbf{B}_{3a}) \mathbf{U}_a(t) \tag{151}$$

5.4.5 Modulation Index Average

Model in (151) has $2N$ modulation indexes. Although each module will have different modulation index, the indexes belonging to the same converter arm are very similar. All modules belonging to the same converter follow the common control strategy that will force the desired output and DC current. The differences between individual module modulation indexes within the same arm will result from small inequalities among module bus voltages, imperfections in the control system transients and other effects that will eventually cause unequal state of charge in the module storage elements. These differences will be introduced in the modulation indexes by the balancing algorithm that will try to equalize the state of charge in each module.

This has already been discussed about in Chapter 4.1 and the takeaway is that the modulation index can be written as a sum of averaged modulation index and perturbations as shown in (152).

$$\begin{aligned} m_{ax[i]}(t) &= \bar{m}_{ax}(t) + m_{\Delta ax[i]}(t) \\ m_{ay[i]}(t) &= \bar{m}_{ay}(t) + m_{\Delta ay[i]}(t) \end{aligned} \tag{152}$$

Following the reasoning in Chapter 4.1 equations below can be written about the average and differential parts of the modulation indexes:

$$\begin{aligned}
\bar{m}_{ax}(t) &= \frac{1}{N} \sum_{i=1}^N m_{ax[i]}(t) = \frac{v_{ax}^r(t)}{V_{DCaxm}^m} \\
\bar{m}_{ay}(t) &= \frac{1}{N} \sum_{i=1}^N m_{ay[i]}(t) = \frac{v_{ay}^r(t)}{V_{DCaym}^m}
\end{aligned} \tag{153}$$

$$\begin{aligned}
\sum_{i=1}^N m_{\Delta ax[i]}(t) &\approx 0 \\
\sum_{i=1}^N m_{\Delta ay[i]}(t) &\approx 0
\end{aligned} \tag{154}$$

Expressions in (153) were already derived in Chapter 4.1 and given in (20) and (21) in a slightly different form. Desired arm voltage amplitude (or arm reference voltages) are marked as $v_{ax}^r(t)$ and $v_{ay}^r(t)$ in (153). Maximum peak of the carrier is, in the case of MMC, equal to the sum of the actual DC bus voltages of all modules within one arm, previously defined as voltage reach of converter the arm and marked as measured value $V_{DCaxm}^m(t)$ and $V_{DCaym}^m(t)$ in (153).

Note that although individual converter leg in general can be capable of having the output above the rails of the DC bus, the implementation of the switching section and the structure given in Figure 22 will prevents this. There are implementations that may allow this mode of operation, but they will not be evaluated here and are left for future studies. For the structures analyzed here the output can still swing only from -bus to +bus. The additional voltage in the voltage reach of the converter arms can be used to boost the stored energy or account for the ripple on the leg filter elements and other.

Going back to Equations (134) and (135) it is possible to rewrite the modulation matrices as shown in (155). Matrix \mathbf{I} is unity matrix and $\mathbf{m}_{\Delta ax}(t)$, $\mathbf{m}_{\Delta ay}(t)$ and $\mathbf{m}_{\Delta axy}(t)$ have same structure as matrices in (134).

$$\begin{aligned}
\mathbf{m}_{axy}(t) &= \begin{bmatrix} \bar{\mathbf{m}}_{ax}(t) + \mathbf{m}_{\Delta ax}(t) & \mathbf{0} \\ \mathbf{0} & \bar{\mathbf{m}}_{ay}(t) + \mathbf{m}_{\Delta ay}(t) \end{bmatrix} \\
&= \begin{bmatrix} \bar{m}_{ax}(t)\mathbf{I} & \mathbf{0} \\ \mathbf{0} & \bar{m}_{ay}(t)\mathbf{I} \end{bmatrix} + \begin{bmatrix} \mathbf{m}_{\Delta ax}(t) & \mathbf{0} \\ \mathbf{0} & \mathbf{m}_{\Delta ay}(t) \end{bmatrix} \\
&= \bar{\mathbf{m}}_{axy}(t) + \mathbf{m}_{\Delta axy}
\end{aligned} \tag{155}$$

5.5 Reduced Average Model

Assuming that each arm has N identical modules, that the converter operates in steady state and that the balancing is ideal, terms in Equation (149) can be simplified using the expanded form of the modulation index given in (155) and in the light of (153), (154), and (155).

Term 1,1 in matrix "A_a" of the model shown in (149) can be simplified using the reasoning given in (156). All terms involving $m_{\Delta ax[i]}(t)$ and $m_{\Delta ay[i]}(t)$ can be canceled using (154). Note that the D_f is the module output matrix, actually a scalar for any implementation of the module model given in Section 5.1.

$$\begin{aligned}
& \mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{a}}^T \mathbf{D}_{\text{faxy}} \mathbf{m}_{\text{axy}}(\mathbf{t}) \mathbf{S}_{\text{a}} = \\
& \mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + \mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} \sum_{i=1}^N D_{fax[i]} m_{ax[i]} & 0 \\ 0 & \sum_{i=1}^N D_{fay[i]} m_{ay[i]} \end{bmatrix} = \\
& \mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + N \mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} D_f & 0 \\ 0 & D_f \end{bmatrix} \begin{bmatrix} \bar{m}_{ax}(t) & 0 \\ 0 & \bar{m}_{ay}(t) \end{bmatrix} \\
& + \mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} D_f & 0 \\ 0 & D_f \end{bmatrix} \begin{bmatrix} \sum_{i=1}^N m_{\Delta ax[i]}(t) & 0 \\ 0 & \sum_{i=1}^N m_{\Delta ay[i]}(t) \end{bmatrix} \approx \\
& \mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + N \mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} D_f & 0 \\ 0 & D_f \end{bmatrix} \begin{bmatrix} \bar{m}_{ax}(t) & 0 \\ 0 & \bar{m}_{ay}(t) \end{bmatrix} = \\
& \mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + N \mathbf{L}_{\text{axy}}^{-1} \mathbf{D}_{\text{axy}}^s \bar{\mathbf{m}}_{\text{axy}}^s
\end{aligned} \tag{156}$$

$$\mathbf{D}_{\text{faxy}}^s = \begin{bmatrix} D_f & 0 \\ 0 & D_f \end{bmatrix}; \quad \bar{\mathbf{m}}_{\text{axy}}^s = \begin{bmatrix} \bar{m}_{ax}(t) & 0 \\ 0 & \bar{m}_{ay}(t) \end{bmatrix} \tag{157}$$

Term 1,2 in matrix "A_a" of the model shown in (149) can be simplified only if the multiplication with the state vector is observed as given in (158). State vector can be found in Equation (106). This step will outline the justification for the model reduction. The idea is to eliminate all of the converter modules and keep one that will be used as representative for the behavior, ideally one per arm.

$$\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_{\text{a}}^T \mathbf{m}_{\text{axy}}(\mathbf{t}) \mathbf{C}_{\text{faxy}} \mathbf{x}_{\text{faxy}} =$$

$$\mathbf{L}_{\text{axy}}^{-1} \left(\begin{bmatrix} \sum_{i=1}^N \bar{m}_{ax}(t) \mathbf{C}_{\text{fax}[i]} \mathbf{x}_{\text{fax}[i]}(\mathbf{t}) \\ \sum_{i=1}^N \bar{m}_{ay}(t) \mathbf{C}_{\text{fay}[i]} \mathbf{x}_{\text{fay}[i]}(\mathbf{t}) \end{bmatrix} + \begin{bmatrix} \sum_{i=1}^N m_{\Delta ax[i]}(t) \mathbf{C}_{\text{fax}[i]} \mathbf{x}_{\text{fax}[i]}(\mathbf{t}) \\ \sum_{i=1}^N m_{\Delta ay[i]}(t) \mathbf{C}_{\text{fay}[i]} \mathbf{x}_{\text{fay}[i]}(\mathbf{t}) \end{bmatrix} \right) \quad (158)$$

If the modules are identical with the same initial conditions and the converter is in the steady state, it can be assumed that the sates are identical or that they are close enough to be represented by their average as shown in (159) and (160). This time the averaging is not done across time interval but across a number of modules and their states. Matrix $\mathbf{C}_{\mathbf{f}}$ is the output matrix from the module model given in Section 5.1. The aggregate arm module state vector \mathbf{x}_{fax} is now reduced to a single representative state vector marked as $\mathbf{x}_{\text{fax}[0]}$. Similarly \mathbf{x}_{fay} is reduced to a single representative state vector marked as $\mathbf{x}_{\text{fay}[0]}$.

$$\mathbf{C}_{\text{fax}[i]} \mathbf{x}_{\text{fax}[i]} \approx \mathbf{C}_{\mathbf{f}} \mathbf{x}_{\text{fax}[0]}(\mathbf{t}), \quad i = 1..N$$

$$\sum_{i=1}^N \bar{m}_{ax}(t) \mathbf{C}_{\text{fax}[i]} \mathbf{x}_{\text{fax}[i]}(\mathbf{t}) \approx \bar{m}_{ax}(t) N \mathbf{C}_{\mathbf{f}} \mathbf{x}_{\text{fax}[0]}(\mathbf{t}) \quad (159)$$

$$\sum_{i=1}^N m_{\Delta ax[i]}(t) \mathbf{C}_{\text{fax}[i]} \mathbf{x}_{\text{fax}[i]}(\mathbf{t}) \approx \mathbf{C}_{\mathbf{f}} \mathbf{x}_{\text{fax}[0]}(\mathbf{t}) \sum_{i=1}^N m_{\Delta ax[i]}(t) \approx 0$$

$$\begin{aligned}
\mathbf{C}_{\text{fay}[i]} \mathbf{x}_{\text{fay}[i]} &\approx \mathbf{C}_f \mathbf{x}_{\text{fay}[0]}(\mathbf{t}), \quad i = 1..N \\
\sum_{i=1}^N \bar{m}_{ay}(t) \mathbf{C}_{\text{fay}[i]} \mathbf{x}_{\text{fay}[i]}(\mathbf{t}) &\approx \bar{m}_{ay}(t) N \mathbf{C}_f \mathbf{x}_{\text{fay}[0]}(\mathbf{t}) \\
\sum_{i=1}^N m_{\Delta ay[i]}(t) \mathbf{C}_{\text{fay}[i]} \mathbf{x}_{\text{fay}[i]}(\mathbf{t}) &\approx \mathbf{C}_f \mathbf{x}_{\text{fay}[0]}(\mathbf{t}) \sum_{i=1}^N m_{\Delta ay[i]}(t) \approx 0
\end{aligned} \tag{160}$$

Taking into account (159) and (160), Equation (158) can be rewritten as (161).

$$\begin{aligned}
&\mathbf{L}_{\text{axy}}^{-1} \mathbf{S}_a^T \mathbf{m}_{\text{axy}}(\mathbf{t}) \mathbf{C}_{\text{faxy}} \mathbf{x}_{\text{faxy}} \approx \\
&\mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} \bar{m}_{ax}(t) N \mathbf{C}_f \mathbf{x}_{\text{fax}[0]}(\mathbf{t}) \\ \bar{m}_{ay}(t) N \mathbf{C}_f \mathbf{x}_{\text{fay}[0]}(\mathbf{t}) \end{bmatrix} = \\
&N \mathbf{L}_{\text{axy}}^{-1} \begin{bmatrix} \bar{m}_{ax}(t) & 0 \\ 0 & \bar{m}_{ay}(t) \end{bmatrix} \begin{bmatrix} \mathbf{C}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_f \end{bmatrix} \begin{bmatrix} \mathbf{x}_{\text{fax}[0]} \\ \mathbf{x}_{\text{fay}[0]} \end{bmatrix} = \\
&N \mathbf{L}_{\text{axy}}^{-1} \bar{\mathbf{m}}_{\text{axy}}^s \mathbf{C}_{\text{faxy}}^s \mathbf{x}_{\text{faxy}}^s
\end{aligned} \tag{161}$$

$$\mathbf{C}_{\text{faxy}}^s = \begin{bmatrix} \mathbf{C}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{C}_f \end{bmatrix}; \quad \mathbf{x}_{\text{faxy}}^s = \begin{bmatrix} \mathbf{x}_{\text{fax}[0]} \\ \mathbf{x}_{\text{fay}[0]} \end{bmatrix} \tag{162}$$

Term 2,1 in matrix "A_a" of the model shown in (149) can be rewritten as shown in (163). As this portion of the model describes the module behavior there is no strictly mathematical justification for the new expression in (163). The justification for the model reduction is given for the simplifications in the first row of matrix "A_a". The second row elements model the module behavior. As a result, instead of N repetitions of the module

states and module matrices there will be only 2 as given in (163).

$$\mathbf{B}_{\text{faxy}} \mathbf{m}_{\text{axy}}(t) \mathbf{S}_{\mathbf{a}} \rightarrow \begin{bmatrix} \mathbf{B}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_f \end{bmatrix} \begin{bmatrix} \bar{m}_{ay}(t) & \mathbf{0} \\ \mathbf{0} & \bar{m}_{ay}(t) \end{bmatrix} = \mathbf{B}_{\text{faxy}}^s \bar{\mathbf{m}}_{\text{axy}}^s \quad (163)$$

$$\mathbf{B}_{\text{faxy}}^s = \begin{bmatrix} \mathbf{B}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_f \end{bmatrix} \quad (164)$$

Term 2,2 in matrix "A_a" of the model shown in (149) can be rewritten as shown in (165). The justification is similar as for the Term 2,1 in matrix "A_a".

$$\mathbf{A}_{\text{faxy}} \rightarrow \mathbf{A}_{\text{faxy}}^s = \begin{bmatrix} \mathbf{A}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_f \end{bmatrix} \quad (165)$$

Reduced matrix "A_a^s" can be summarized as shown in equations (166).

$$\mathbf{A}_{\mathbf{a}}^s = \begin{bmatrix} -(\mathbf{L}_{\text{axy}}^{-1} \mathbf{R}_{\text{axy}} + N \mathbf{L}_{\text{axy}}^{-1} \mathbf{D}_{\text{faxy}}^s \bar{\mathbf{m}}_{\text{axy}}^s) & -(N \mathbf{L}_{\text{axy}}^{-1} \bar{\mathbf{m}}_{\text{axy}}^s \mathbf{C}_{\text{faxy}}^s) \\ \mathbf{B}_{\text{faxy}}^s \bar{\mathbf{m}}_{\text{axy}}^s & \mathbf{A}_{\text{faxy}}^s \end{bmatrix} \quad (166)$$

Reduced matrix "B_a^s" can be summarized as shown in equations (167). The matrices $\mathbf{F}_{\text{faxy}}^s$ and $\mathbf{E}_{\text{faxy}}^s$ are given in (168). They can be obtained using the same reasoning outlined in the sections above.

$$\mathbf{B}_a^s = \begin{bmatrix} -(\mathbf{L}_{axy}^{-1} \mathbf{K}_{Viny}) & -N(\mathbf{L}_{axy}^{-1} \bar{\mathbf{m}}_{axy}^s(\mathbf{t}) \mathbf{F}_{faxy}^s) \\ \mathbf{0} & \mathbf{E}_{faxy}^s \end{bmatrix} \quad (167)$$

$$\mathbf{F}_{faxy}^s = \begin{bmatrix} \mathbf{F}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{F}_f \end{bmatrix}; \quad \mathbf{E}_{faxy}^s = \begin{bmatrix} \mathbf{E}_f & \mathbf{0} \\ \mathbf{0} & \mathbf{E}_f \end{bmatrix} \quad (168)$$

The reduced averaged model can be summarized as shown in Equation (169). The state and input vectors also have to be reduced and are given in Equation (170). The rest of the reduced model matrices are given in the text above in: (168), (165), (162) and (157).

$$\frac{d}{dt} \mathbf{X}_a^s(\mathbf{t}) = \mathbf{A}_a^s(\mathbf{t}) \mathbf{X}_a^s(\mathbf{t}) + \mathbf{B}_a^s(\mathbf{t}) \mathbf{U}_a^s(\mathbf{t}) \quad (169)$$

$$\mathbf{X}_a^s(\mathbf{t}) = \begin{bmatrix} \mathbf{i}_{axy} \\ \mathbf{x}_{faxy}^s \end{bmatrix}; \quad \mathbf{U}_a^s = \begin{bmatrix} \mathbf{v}_{ain} \\ u_{fax[0]} \\ u_{fay[0]} \end{bmatrix} \quad (170)$$

Model from Equation (169) can be represented with the circuit diagram given in Figure 30.

Note that the model as represented in Figure 30 is not conservative. The voltage/current

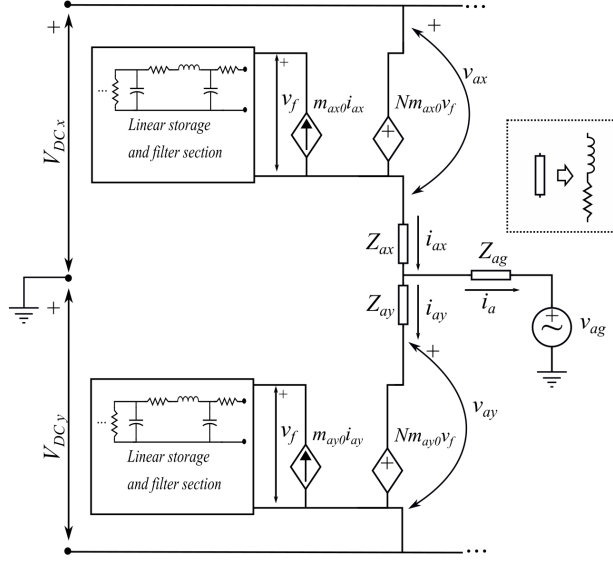


Figure 30: Circuit representation of the reduced linearized model given in Equation (169).

source pairs act as a power amplifiers. The arm side controlled source voltage is N times higher than the module side source voltage. This is the consequence of using one module as representative for N actual modules within the arm. To make the model power conservative the model of the module can be modified as shown in paper by Wang *et al.* [35]. The problem with this approach is that it obscures the behavior of the module. If it is necessary to make the model power conservative and maintain the structure of the module the model shown in Figure 30 can be used.

6 Control

The expected behavior of the converter modeled in the previous section is that it produces sinusoidal output voltages and currents at the same frequency and constant phase shift with respect to the grid voltage and ideally DC input current. This limits the averaged modulation indexes to a fairly specific set of waveforms. Modulation index will depend on the external

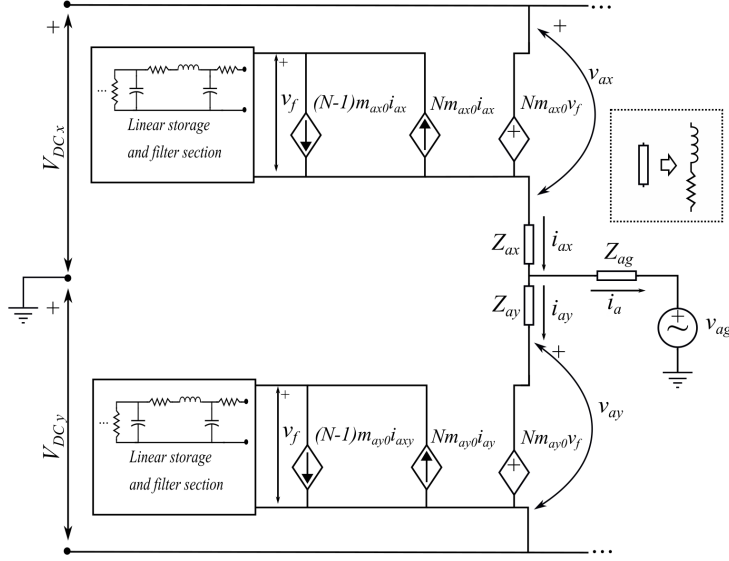


Figure 31: Alternate circuit representation of the reduced linearized model given in Equation (169). The extra current source models the remaining $N-1$ modules. All modules behave the same.

DC bus voltage, grid voltage and desired input and output currents. If designed well the averaged modulation index will not depend on the individual module states and there will be only two distinct averaged modulation index waveforms per MMC converter leg. These modulation indexes will come from the controller which will be the main focus of the sections below.

6.1 Control Model Equations

To obtain the averaged modulation indexes, the references for the steady state operating point of the converter will be defined first. Fundamentals for this were done in Chapter 4.3 and a good starting point would be equations (42) - (45), which represent the simplest MMC plant model as shown in Figure 20. These equations are given again in (171)-(174) and are written in the form that calculates the references for the arm voltages for the desired circulating and output currents. Note that equations (171)-(174) fall under the set of

assumptions given in Chapter 4 and they do not include the dynamics of the modules. As a consequence, the module dynamics will be the disturbances for the controller derived from equations (171)-(174).

$$V_{ax}(s) = V_{DCx}^m(s) - V_{ag}(s) + \frac{1}{2}V_{a\Sigma}(s) - \frac{1}{2}V_{a\Delta}(s) \quad (171)$$

$$V_{ay}(s) = V_{DCy}(s) + V_{ag}(s) + \frac{1}{2}V_{a\Sigma}(s) + \frac{1}{2}V_{a\Delta}(s) \quad (172)$$

$$V_{a\Delta}(s) = -i_{ca}(s)(Z_{ay}(s) - Z_{ax}(s)) + i_a(s)(k_s Z_{ax}(s) + (1 - k_s)Z_{ay}(s) + 2Z_{ag}(s)) \quad (173)$$

$$V_{a\Sigma}(s) = -i_{ca}(s)(Z_{ay}(s) + Z_{ax}(s)) - i_a(s)(k_s Z_{ax}(s) - (1 - k_s)Z_{ay}(s)) \quad (174)$$

Models in the previous sections were derived in time domain, as a result it is convenient to translate (171)-(174) in time domain as well. With the help of circuit analysis, it is simple to rewrite the equations in time domain as shown in equations (175)-(178). It is assumed that the arm impedance is well represented with RL circuit.

$$v_{ax}(t) = V_{DCx}(t) - v_{ag}(t) + \frac{1}{2}v_{a\Sigma}(t) - \frac{1}{2}v_{a\Delta}(t) \quad (175)$$

$$v_{ay}(t) = V_{DCy}(t) + v_{ag}(t) + \frac{1}{2}v_{a\Sigma}(t) + \frac{1}{2}v_{a\Delta}(t) \quad (176)$$

$$\begin{aligned}
v_{a\Delta}(t) = & -i_{ca}(t)(R_{ay} - R_{ax}) + i_a(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
& - \frac{d}{dt}i_{ca}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i_a(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
\end{aligned} \tag{177}$$

$$\begin{aligned}
v_{a\Sigma}(t) = & -i_{ca}(t)(R_{ay} + R_{ax}) - i_a(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i_{ca}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i_a(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned} \tag{178}$$

Equations (175) to (178) will be the plant model which will be used for the control design in the following chapters.

6.2 dq Frame of Reference and Transformations

For the control of active and reactive power within any AC system it is necessary to know the amplitude of currents and voltages and their relative angles. For poly-phase systems the control of current and voltage pairs can be quite complicated. However, it has been shown in the literature that symmetric multi-phase systems can be reduced to two phase equivalent no matter how many phases there are in the system. One example of this approach is well known Clarke transformation that reduces 3 phase system to the equivalent 2 phase $\alpha\beta$ representation [119]. All the controls and calculations can then be reduced to the investigation of a pair of currents and voltages.

The problem with $\alpha\beta$ representation is that the instantaneous values of currents and voltages still change rapidly over time making the amplitude and relative angle difficult to

control. Resonant controllers are required in this case and they are usually more difficult to analyze and implement. However, the amplitudes and relative angles do not change over time in the same manner as voltages and currents do. As a result, convenient coordinate transformation can be used to change the representation of the system to the one that will favor amplitude and phase angle instead of the instantaneous value. One convenient coordinate transformation that is commonly used in the available literature for this purpose is called Park transformation [119]. This transformation rotates the vectors of voltages and currents from the $\alpha\beta$ coordinate system in time such that they become stationary in the new coordinate system. The resulting coordinate system is usually called stationary dq frame of reference. It preserves amplitudes and angles between current and voltage vectors which are now stationary and relatively easy to evaluate and control.

For single phase system shown here the voltage measurement is a single AC value coordinate, the " β coordinate" is missing. The relative angle and amplitude of the measurement are still important but the vector representation in the 2-D plane that will make the amplitude and relative angle easy to evaluate cannot be obtained in the same way as for the multi-phase systems. Due to the missing coordinate the application of the rotation transformation cannot be simply done. As a result, the equations must be augmented with auxiliary 90 degree offset coordinate usually called quadrature component. The quadrature component can be obtained from the measurements by 90 degree phase shift.

The analogy that can be used to justify the approach chosen here is the phasor representation from the circuit analysis [120]. Any AC circuit variable can be represented in a complex plane by rotating phasors. This technique is commonly used in circuit analysis and is somewhat analogous to the rotating vectors. The phasors are represented in the 2-d com-

plex plane as stationary and is usually said that the instantaneous value of each vector can be obtained by projection of the rotating vector on the stationary phase axis. The phase axis is usually aligned with the real axis of the complex plane in the phasor drawings and would be analogous to the α coordinate axis. The β coordinate axis would be the projection of the vector onto the axis that is 90 degree shifted from the α and would align with imaginary axis of the complex plane as illustrated in Figure 32.

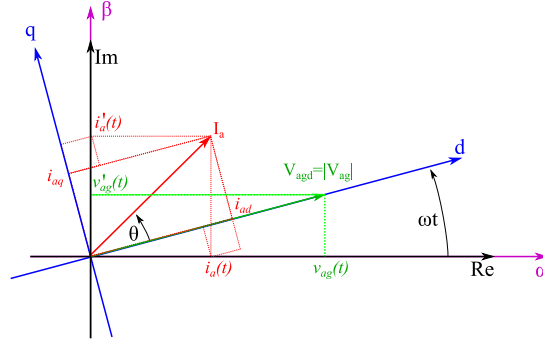


Figure 32: dq frame of reference and its relation to the voltage and current phasor. Similar triangles used to obtain the transformation matrix in (181) are outlined as well.

The α coordinates for $i_a(t)$ and $v_{ag}(t)$ in Figure 32 are actual measurements of the current and voltage. The β (imaginary or quadrature component) coordinates for $i'_g(t)$ and $v'_g(t)$ can be generated from the measurements using a 90 degree phase shifter. Assuming sinusoidal waveforms at grid frequency ω_g , the 90 degree phase shift can be obtained using all pass filter as stated in (179). Another solution may be to use appropriately attenuated differentiator. Although the differentiator with appropriate attenuation at grid frequency may work fine for relatively pure AC grid voltage, for the current that is saturated in harmonic content it may be complicated to implement appropriate linear attenuation that will keep the high frequency components at appropriate levels.

$$\begin{aligned}
i'_a(s) &= -\frac{s - \omega_g}{s + \omega_g} i_a(s) \\
v'_{ag}(s) &= -\frac{s - \omega_g}{s + \omega_g} v_{ag}(s)
\end{aligned} \tag{179}$$

$$H_{qc}(s) = -\frac{s - \omega_g}{s + \omega_g} \tag{180}$$

The dq coordinates can be obtained by applying the clockwise rotation transformation to the counterclockwise rotating phasor coordinates as illustrated in Figure 32. The dq and inverse transformation matrices are given in (181) and exemplified using current i_a . The rotation angle $\omega_g t$ can be extracted from the grid voltage measurement using some form of Phase Locked Loop (PLL) which will not be investigated here.

$$\begin{aligned}
\mathbf{T}_{\mathbf{dq2}} &= \begin{bmatrix} \cos(\omega_g t) & \sin(\omega_g t) \\ -\sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix}; \quad \begin{bmatrix} i_{ad} \\ i_{aq} \end{bmatrix} = \mathbf{T}_{\mathbf{dq2}} \begin{bmatrix} i_a \\ i'_a \end{bmatrix} \\
\mathbf{T}_{\alpha\beta2} = \mathbf{T}_{\mathbf{dq2}}^{-1} &= \begin{bmatrix} \cos(\omega_g t) & -\sin(\omega_g t) \\ \sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix}; \quad \begin{bmatrix} i_a \\ i'_a \end{bmatrix} = \mathbf{T}_{\alpha\beta2} \begin{bmatrix} i_{ad} \\ i_{aq} \end{bmatrix}
\end{aligned} \tag{181}$$

Differentials in dq

The expressions for the arm voltage references in (175)-(175) contain differentials. The time differentials of the transformation matrices are given in (182) and (183). As can be seen the differential of the rotation matrix can be represented as a product of constant and

rotation matrix. The fact that the differentials can be avoided in some sense is another benefit of using dq frame of reference for control.

$$\begin{aligned} \frac{d}{dt} \mathbf{T}_{\mathbf{dq2}} &= \begin{bmatrix} -\omega_g \sin(\omega_g t) & \omega_g \cos(\omega_g t) \\ -\omega_g \cos(\omega_g t) & -\omega_g \sin(\omega_g t) \end{bmatrix} = \\ &= \begin{bmatrix} 0 & \omega_g \\ -\omega_g & 0 \end{bmatrix} \begin{bmatrix} \cos(\omega_g t) & \sin(\omega_g t) \\ -\sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix} = \\ &\mathbf{\Omega}_{\mathbf{g2}} \mathbf{T}_{\mathbf{dq2}} \end{aligned} \quad (182)$$

$$\begin{aligned} \frac{d}{dt} \mathbf{T}_{\alpha\beta\mathbf{2}} &= \begin{bmatrix} -\omega_g \sin(\omega_g t) & -\omega_g \cos(\omega_g t) \\ \omega_g \cos(\omega_g t) & -\omega_g \sin(\omega_g t) \end{bmatrix} = \\ &= \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix} \begin{bmatrix} \cos(\omega_g t) & -\sin(\omega_g t) \\ \sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix} = \\ &\mathbf{\Omega}_{\mathbf{g2}}^T \mathbf{T}_{\alpha\beta\mathbf{2}} \end{aligned} \quad (183)$$

Note that matrix the $\mathbf{\Omega}_{g2}$ is usually referred to as cross coupling between d and q coordinates in the systems with reactive components that are modeled or controlled in dq frame of reference. Common dq frame of reference controllers usually have some form of control structure to account for effect, e.g feed forward decoupling [121].

6.3 Control Model Equations in DQ frame

From Section 4.4 it can be concluded that for the successful control of the power flow within the MMC converter leg, the controller should include at least the references for active and reactive output current and DC component of the circulating current. To control the individual arm state of charge it may be necessary to include the references for the d and q components (active and reactive components) of the circulating current at the fundamental frequency.

To derive the open loop dq equations, the arm voltage reference equations given in (175) - (178) must be augmented with appropriate quadrature components. However, as outlined above the circulating current will have DC component besides component at the grid fundamental. Before augmenting the circulating current with the quadrature component it should be split into AC and DC components. Having this in mind, the equations given in (177) and (178) can be rewritten as shown in (184) - (187). The output current should not have the DC component, however for the completeness of the equations it will be included here.

$$\begin{aligned}
 v_{a\Delta 0}(t) = & -i_{ca0}(t)(R_{ay} - R_{ax}) + i_{a0}(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
 & - \frac{d}{dt}i_{ca0}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i_{a0}(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
 \end{aligned} \tag{184}$$

$$\begin{aligned}
 v_{a\Delta 1}(t) = & -i_{ca1}(t)(R_{ay} - R_{ax}) + i_{a1}(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
 & - \frac{d}{dt}i_{ca1}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i_{a1}(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
 \end{aligned} \tag{185}$$

$$\begin{aligned}
v_{a\Sigma 0}(t) = & -i_{ca0}(t)(R_{ay} + R_{ax}) - i_{a0}(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i_{ca0}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i_{a0}(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned} \tag{186}$$

$$\begin{aligned}
v_{a\Sigma 1}(t) = & -i_{ca1}(t)(R_{ay} + R_{ax}) - i_{a1}(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i_{ca1}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i_{a1}(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned} \tag{187}$$

Equations (185) and (187) can be augmented to include quadrature components, marked prime (') as shown in (188) - (191). Note that DC variables do not have the β (quadrature) components.

$$\begin{aligned}
v_{a\Delta 0}(t) = & -i_{ca0}(t)(R_{ay} - R_{ax}) + i_{a0}(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
& - \frac{d}{dt}i_{ca0}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i_{a0}(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
\end{aligned} \tag{188}$$

$$\begin{aligned}
v_{a\Sigma 0}(t) = & -i_{ca0}(t)(R_{ay} + R_{ax}) - i_{a0}(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i_{ca0}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i_{a0}(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned} \tag{189}$$

$$\begin{aligned}
v_{a\Delta 1}(t) = & -i_{ca1}(t)(R_{ay} - R_{ax}) + i_a(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
& - \frac{d}{dt}i_{ca1}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i_a(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
\end{aligned} \tag{190}$$

$$\begin{aligned}
v'_{a\Delta 1}(t) = & -i'_{ca1}(t)(R_{ay} - R_{ax}) + i'_a(t)(k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) \\
& - \frac{d}{dt}i'^{r'}_{ca1}(t)(L_{ay} - L_{ax}) + \frac{d}{dt}i'^{r'}_a(t)(k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})
\end{aligned}$$

$$\begin{aligned}
v_{a\Sigma 1}(t) = & -i_{ca1}(t)(R_{ay} + R_{ax}) - i_a(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i_{ca1}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i_a(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned} \tag{191}$$

$$\begin{aligned}
v'_{a\Sigma 1}(t) = & -i'_{ca1}(t)(R_{ay} + R_{ax}) - i'_a(t)(k_s R_{ax} - (1 - k_s)R_{ay}) \\
& - \frac{d}{dt}i'^{r'}_{ca1}(t)(L_{ay} + L_{ax}) - \frac{d}{dt}i'^{r'}_a(t)(k_s L_{ax} - (1 - k_s)L_{ay})
\end{aligned}$$

The AC components in Equations (190) and (191) can be rewritten in matrix form as:

$$\begin{aligned}
\begin{bmatrix} v_{a\Delta 1}(t) \\ v'_{a\Delta 1}(t) \end{bmatrix} &= - \begin{bmatrix} (R_{ay} - R_{ax}) & 0 \\ 0 & (R_{ay} - R_{ax}) \end{bmatrix} \begin{bmatrix} i_{ca1}(t) \\ i'_{ca1}(t) \end{bmatrix} \\
&+ \begin{bmatrix} (k_s R_{ax} + (1 - k_s) R_{ay} + 2R_{ag}) & 0 \\ 0 & (k_s R_{ax} + (1 - k_s) R_{ay} + 2R_{ag}) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i'_a(t) \end{bmatrix} \\
&- \begin{bmatrix} (L_{ay} - L_{ax}) & 0 \\ 0 & (L_{ay} - L_{ax}) \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ca1}(t) \\ i'_{ca1}(t) \end{bmatrix} \\
&+ \begin{bmatrix} (k_s L_{ax} + (1 - k_s) L_{ay} + 2L_{ag}) & 0 \\ 0 & (k_s L_{ax} + (1 - k_s) L_{ay} + 2L_{ag}) \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a(t) \\ i'_a(t) \end{bmatrix}
\end{aligned} \tag{192}$$

$$\begin{aligned}
\begin{bmatrix} v_{a\Sigma 1}(t) \\ v'_{a\Sigma 1}(t) \end{bmatrix} &= - \begin{bmatrix} (R_{ay} + R_{ax}) & 0 \\ 0 & (R_{ay} + R_{ax}) \end{bmatrix} \begin{bmatrix} i_{ca0}(t) \\ i'_{ca0}(t) \end{bmatrix} \\
&- \begin{bmatrix} (k_s R_{ax} - (1 - k_s) R_{ay}) & 0 \\ 0 & (k_s R_{ax} - (1 - k_s) R_{ay}) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i'_a(t) \end{bmatrix} \\
&- \begin{bmatrix} (L_{ay} + L_{ax}) & 0 \\ 0 & (L_{ay} + L_{ax}) \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ca1}(t) \\ i'_{ca1}(t) \end{bmatrix} \\
&- \begin{bmatrix} (k_s L_{ax} - (1 - k_s) L_{ay}) & 0 \\ 0 & (k_s L_{ax} - (1 - k_s) L_{ay}) \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a(t) \\ i'_a(t) \end{bmatrix}
\end{aligned} \tag{193}$$

Equations (192) and (193) can be written in more concise form as shown in:

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\alpha\beta}}(\mathbf{t}) = & - (R_{ay} - R_{ax})\mathbf{I}_{2\times 2}\mathbf{i}_{\mathbf{ca1}_{\alpha\beta}}(\mathbf{t}) \\
& + (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{I}_{2\times 2}\mathbf{i}_{\mathbf{a1}_{\alpha\beta}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\mathbf{I}_{2\times 2}\frac{d}{dt}\mathbf{i}_{\mathbf{ca1}_{\alpha\beta}}(\mathbf{t}) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{I}_{2\times 2}\frac{d}{dt}\mathbf{i}_{\mathbf{a1}_{\alpha\beta}}(\mathbf{t})
\end{aligned} \tag{194}$$

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\alpha\beta}}(\mathbf{t}) = & - (R_{ay} + R_{ax})\mathbf{I}_{2\times 2}\mathbf{i}_{\mathbf{ca1}_{\alpha\beta}}(\mathbf{t}) \\
& - (k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{I}_{2\times 2}\mathbf{i}_{\mathbf{a1}_{\alpha\beta}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\mathbf{I}_{2\times 2}\frac{d}{dt}\mathbf{i}_{\mathbf{ca1}_{\alpha\beta}}(\mathbf{t}) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{I}_{2\times 2}\frac{d}{dt}\mathbf{i}_{\mathbf{a1}_{\alpha\beta}}(\mathbf{t})
\end{aligned} \tag{195}$$

The vectors from the equations (194) and (195) can be easily related to equations (192) and (193) showing their structure and will not be noted individually again. Note that $\mathbf{I}_{2\times 2}$ represents identity matrix with dimensions 2x2. It is now easy to rewrite the equations (194) and (195) in the dq frame of reference by incorporating the transformations to dq frame of reference and back given in (181) as shown in (196) and (197) .

$$\begin{aligned}
\mathbf{T}_{\alpha\beta\mathbf{2}}\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & - (R_{ay} - R_{ax})\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t}) \\
& + (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\mathbf{I}_{\mathbf{2x2}}\frac{d}{dt}(\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t})) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{I}_{\mathbf{2x2}}\frac{d}{dt}(\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}))
\end{aligned} \tag{196}$$

$$\begin{aligned}
\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & - (R_{ay} + R_{ax})\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\mathbf{I}_{\mathbf{2x2}}\frac{d}{dt}(\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t})) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{I}_{\mathbf{2x2}}\frac{d}{dt}(\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}))
\end{aligned} \tag{197}$$

After multiplying the left and the right side with $\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})$ and applying product rule to the differentials the equations (196) and (197) become:

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & - (R_{ay} - R_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t}) \\
& + (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}\mathbf{I}_{\mathbf{2x2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}\mathbf{I}_{\mathbf{2x2}}\left(\frac{d}{dt}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t}) + \mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\frac{d}{dt}\mathbf{i}_{\mathbf{ca1}_{\mathbf{dq}}}(\mathbf{t})\right) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{I}_{\mathbf{2x2}}\left(\frac{d}{dt}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t}) + \mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\frac{d}{dt}\mathbf{i}_{\mathbf{a1}_{\mathbf{dq}}}(\mathbf{t})\right)
\end{aligned} \tag{198}$$

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & \\
& - (R_{ay} + R_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{I}_{\mathbf{2}\times\mathbf{2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{I}_{\mathbf{2}\times\mathbf{2}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{I}_{\mathbf{2}\times\mathbf{2}}\left(\frac{d}{dt}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) + \mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})\right) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{I}_{\mathbf{2}\times\mathbf{2}}\left(\frac{d}{dt}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) + \mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})\right)
\end{aligned} \tag{199}$$

To simplify the equation above the following notes will be of help:

- In dq frame of reference, in the steady state, the coordinates are constant. This means that the terms $\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})$ and $\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})$ are zero.
- Matrix $\mathbf{I}_{\mathbf{2}\times\mathbf{2}}$ is identity matrix and is commutative with the $\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})$
- Differential from terms $\frac{d}{dt}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})$ can be eliminated using Equation (183).

As a result equations (198) and (199) can be rewritten as:

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & - (R_{ay} - R_{ax})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& + (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})
\end{aligned} \tag{200}$$

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) = & - (R_{ay} + R_{ax})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t}) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\mathbf{dq}}}(\mathbf{t})
\end{aligned} \tag{201}$$

The time dependent terms in the form of $\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t})$ appear in couple of places in the equations above. These terms can be simplified as well as shown in (202).

$$\begin{aligned}
\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}(\mathbf{t})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{T}_{\alpha\beta\mathbf{2}}(\mathbf{t}) = & \begin{bmatrix} \cos(\omega_g t) & \sin(\omega_g t) \\ -\sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix} \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix} \begin{bmatrix} \cos(\omega_g t) & -\sin(\omega_g t) \\ \sin(\omega_g t) & \cos(\omega_g t) \end{bmatrix} = \\
& \begin{bmatrix} 0 & -\omega_g (\sin^2(\omega_g t) + \cos^2(\omega_g t)) \\ \omega_g (\sin^2(\omega_g t) + \cos^2(\omega_g t)) & 0 \end{bmatrix} = \\
& \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix} = \mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}
\end{aligned} \tag{202}$$

Using the result from (202), equations (200) and (201) can be rewritten as (203) and (204):

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\text{dq}}}(\mathbf{t}) = & -(R_{ay} - R_{ax})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& + (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (L_{ay} - L_{ax})\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& + (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t})
\end{aligned} \tag{203}$$

$$\begin{aligned}
\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\text{dq}}}(\mathbf{t}) = & -(R_{ay} + R_{ax})\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{\Omega}_{\mathbf{g}\mathbf{2}}^{\mathbf{T}}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (L_{ay} + L_{ax})\frac{d}{dt}\mathbf{i}_{\mathbf{ca}\mathbf{1}_{\text{dq}}}(\mathbf{t}) \\
& - (k_s L_{ax} - (1 - k_s)L_{ay})\frac{d}{dt}\mathbf{i}_{\mathbf{a}\mathbf{1}_{\text{dq}}}(\mathbf{t})
\end{aligned} \tag{204}$$

All components of the $\mathbf{v}_{\mathbf{a}\Sigma\mathbf{d}\mathbf{q}}(\mathbf{t})$ and $\mathbf{v}_{\mathbf{a}\Delta\mathbf{d}\mathbf{q}}(\mathbf{t})$ can be summarized in matrix form as :

$$\mathbf{v}_{\Sigma\Delta\mathbf{d}\mathbf{q}}(\mathbf{t}) = \mathbf{R}_{\Sigma\Delta\mathbf{d}\mathbf{q}}\mathbf{i}_{\text{aco}\mathbf{d}\mathbf{q}}(\mathbf{t}) + \mathbf{X}_{\Sigma\Delta\mathbf{d}\mathbf{q}}\mathbf{i}_{\text{aco}\mathbf{d}\mathbf{q}}(\mathbf{t}) + \mathbf{L}_{\Sigma\Delta\mathbf{d}\mathbf{q}}\frac{d}{dt}\mathbf{i}_{\text{aco}\mathbf{d}\mathbf{q}}(\mathbf{t}) \tag{205}$$

The terms from (205) are shown expanded in equations (206)-(209).

$$\mathbf{v}_{\Sigma\Delta_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{a\Delta 0}(t) \\ \mathbf{v}_{a\Delta 1_{dq}}(\mathbf{t}) \\ v_{a\Sigma 0}(t) \\ \mathbf{v}_{a\Sigma 1_{dq}}(\mathbf{t}) \end{bmatrix}; \quad \mathbf{i}_{aco_{dq}}(\mathbf{t}) = \begin{bmatrix} i_{ca0}(t) \\ \mathbf{i}_{ca1_{dq}}(\mathbf{t}) \\ i_{a0}(t) \\ \mathbf{i}_{a1_{dq}}(\mathbf{t}) \end{bmatrix} \quad (206)$$

$$\mathbf{R}_{\Sigma\Delta_{dq}} = \begin{bmatrix} -(R_{ay} - R_{ax}) & \mathbf{0}_{1 \times 2} & (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(R_{ay} - R_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{I}_{2 \times 2} \\ -(R_{ay} + R_{ax}) & \mathbf{0}_{1 \times 2} & -(k_s R_{ax} - (1 - k_s)R_{ay}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(R_{ay} + R_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{1 \times 2} & -(k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{I}_{2 \times 2} \end{bmatrix} \quad (207)$$

$$\mathbf{X}_{\Sigma\Delta_{dq}} = \begin{bmatrix} 0 & \mathbf{0}_{1 \times 2} & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} - L_{ax})\mathbf{\Omega}_{\mathbf{g}2}^T & \mathbf{0}_{1 \times 2} & (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{\Omega}_{\mathbf{g}2}^T \\ 0 & \mathbf{0}_{1 \times 2} & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} + L_{ax})\mathbf{\Omega}_{\mathbf{g}2}^T & \mathbf{0}_{1 \times 2} & -(k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{\Omega}_{\mathbf{g}2}^T \end{bmatrix} \quad (208)$$

$$\mathbf{L}_{\Sigma\Delta_{dq}} = \begin{bmatrix} -(L_{ay} - L_{ax}) & \mathbf{0}_{1 \times 2} & (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} - L_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{I}_{2 \times 2} \\ -(L_{ay} + L_{ax}) & \mathbf{0}_{1 \times 2} & -(k_s L_{ax} - (1 - k_s)L_{ay}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} + L_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & -(k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{I}_{2 \times 2} \end{bmatrix} \quad (209)$$

Note that the $\mathbf{I}_{2 \times 2}$ is identity matrix and that the matrices above actually have dimension 6x6. The currents used as inputs in Equation (205) are references that can be obtained from the higher level power controller. Equation above can be rewritten in a more concise form given in (210):

6.4 Open Loop Control

Since these are the steady state references it can be assumed that the differentials are zero $\frac{d}{dt}\mathbf{i}_{\text{aco}_{dq}}(\mathbf{t}) = \mathbf{0}$. Therefore, Equation (205) can be rewritten as (210) for the purpose of the open loop control.

$$\mathbf{v}_{\Sigma\Delta_{dq}}(\mathbf{t}) = \mathbf{R}_{\Sigma\Delta_{dq}}\mathbf{i}_{\text{aco}_{dq}}(\mathbf{t}) + \mathbf{X}_{\Sigma\Delta_{dq}}\mathbf{i}_{\text{aco}_{dq}}(\mathbf{t}) \quad (210)$$

Note that the term "dq0" is avoided on purpose in this investigation. Zero vector component in 3-phase dq0 converter control and DC components marked with 0 and used in the equations above do not have the same meaning. The zero component in 3-phase dq0 frame of reference is perpendicular to the plane of rotation and does not go through the rotational transformation but is still AC in most cases. It actually represents the line to ground components that are not observable in the line to line measurements of the common 3-wire 3-phase system. One common example is 3^{rd} harmonic that is usually injected in 3-phase converter control to extend its DC bus utilization. The 3^{rd} harmonic adds alternating 0 component to the dq0 frame measurements.

In the previous equation, terms for $v_{a\Sigma}(t)$ and $v_{a\Delta}(t)$ from (176) and (177) have been split in DC and fundamental AC. The AC components are then expressed in dq coordinate system.

To obtain the arm voltage references, Equation (210) will have to be incorporated into equations (175) and (176). In order to do this, (175) and (176) will have to be represented in dq frame as well and in appropriate matrix form.

Equations (175) and (176) contain grid voltage measurement ($v_{ag}(t)$) and DC bus mea-

surement ($V_{DCx}(t)$ and $V_{DCy}(t)$) besides $v_{a\Sigma}(t)$ and $v_{a\Delta}(t)$. For the purpose of the open loop control, it can be assumed that the grid voltage is pure sine wave at the fundamental frequency of ω_g and that the external DC bus measurement is constant. As a consequence, the grid voltage measurement $v_{ag}(t)$ will have be augmented with quadrature (β) component and then represented as a vector in $\alpha\beta$ and dq frame of reference and DC bus measurements can remain what they are. Equations (175) and (176) will have to be separated into DC and AC equations. AC equations should be augmented with the quadrature components as shown in (211) - (214) so that the appropriate dq transformation can be applied.

$$v_{ax0}(t) = V_{DCx}(t) + \frac{1}{2}v_{a\Sigma0}(t) - \frac{1}{2}v_{a\Delta0}(t) \quad (211)$$

$$\begin{aligned} v_{ax1}(t) &= -v_{ag1}(t) + \frac{1}{2}v_{a\Sigma1}(t) - \frac{1}{2}v_{a\Delta1}(t) \\ v_{ax1}^{r'}(t) &= -v_{ag1}^{m'}(t) + \frac{1}{2}v_{a\Sigma1}'(t) - \frac{1}{2}v_{a\Delta1}'(t) \end{aligned} \quad (212)$$

$$v_{ay0}(t) = V_{DCy}(t) + \frac{1}{2}v_{a\Sigma0}(t) + \frac{1}{2}v_{a\Delta0}(t) \quad (213)$$

$$\begin{aligned} v_{ay1}(t) &= +v_{ag1}(t) + \frac{1}{2}v_{a\Sigma1}(t) + \frac{1}{2}v_{a\Delta1}(t) \\ v_{ay1}^{r'}(t) &= +v_{ag1}^{m'}(t) + \frac{1}{2}v_{a\Sigma1}'(t) + \frac{1}{2}v_{a\Delta1}'(t) \end{aligned} \quad (214)$$

Equations (212) and (214) can be rewritten in matrix form as:

$$\begin{bmatrix} v_{ax1}(t) \\ v_{ax1}^{r'}(t) \end{bmatrix} = - \begin{bmatrix} v_{ag1}(t) \\ v_{ag1}^{m'}(t) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} v_{a\Sigma1}(t) \\ v_{a\Sigma1}'(t) \end{bmatrix} - \frac{1}{2} \begin{bmatrix} v_{a\Delta1}(t) \\ v_{a\Delta1}'(t) \end{bmatrix} \quad (215)$$

$$\mathbf{v}_{\mathbf{ax}\mathbf{1}_{\alpha\beta}}(\mathbf{t}) = -\mathbf{v}_{\mathbf{ag}\mathbf{1}_{\alpha\beta}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\alpha\beta}}(\mathbf{t}) - \frac{1}{2}\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\alpha\beta}}(\mathbf{t})$$

$$\begin{bmatrix} v_{ay1}(t) \\ v_{ay1}^{r'}(t) \end{bmatrix} = \begin{bmatrix} v_{ag1}(t) \\ v_{ag1}^{m'}(t) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} v_{a\Sigma1}(t) \\ v_{a\Sigma1}'(t) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} v_{a\Delta1}(t) \\ v_{a\Delta1}'(t) \end{bmatrix} \quad (216)$$

$$\mathbf{v}_{\mathbf{ay}\mathbf{1}_{\alpha\beta}}(\mathbf{t}) = \mathbf{v}_{\mathbf{ag}\mathbf{1}_{\alpha\beta}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\alpha\beta}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\alpha\beta}}(\mathbf{t})$$

Applying the dq transformation $\mathbf{T}_{\alpha\beta\mathbf{2}}$ from (181) to (215) and (216), and then multiplying both sides with $\mathbf{T}_{\alpha\beta\mathbf{2}}^{-1}$ results in (217) and (218).

$$\mathbf{v}_{\mathbf{ax}\mathbf{1}_{\text{dq}}}(\mathbf{t}) = -\mathbf{v}_{\mathbf{ag}\mathbf{1}_{\text{dq}}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\text{dq}}}(\mathbf{t}) - \frac{1}{2}\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\text{dq}}}(\mathbf{t}) \quad (217)$$

$$\mathbf{v}_{\mathbf{ay}\mathbf{1}_{\text{dq}}}(\mathbf{t}) = \mathbf{v}_{\mathbf{ag}\mathbf{1}_{\text{dq}}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Sigma\mathbf{1}_{\text{dq}}}(\mathbf{t}) + \frac{1}{2}\mathbf{v}_{\mathbf{a}\Delta\mathbf{1}_{\text{dq}}}(\mathbf{t}) \quad (218)$$

Arranging (211), (213), (217) and (218) in a convenient matrix form results in:

$$\begin{bmatrix} v_{ax0}(t) \\ \mathbf{v}_{ax1dq}(\mathbf{t}) \\ v_{ay0}(t) \\ \mathbf{v}_{ay1dq}(\mathbf{t}) \end{bmatrix} = \begin{bmatrix} 1 & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & -\mathbf{I}_{2 \times 2} \\ 0 & 1 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & \mathbf{I}_{2 \times 2} \end{bmatrix} \begin{bmatrix} V_{DCx}(t) \\ V_{DCy}(t) \\ \mathbf{v}_{ag1dq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{2} & \mathbf{0}_{1 \times 2} & \frac{1}{2} & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -\frac{1}{2}\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} \\ \frac{1}{2} & \mathbf{0}_{1 \times 2} & \frac{1}{2} & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} \end{bmatrix} \begin{bmatrix} v_{a\Delta 0}(t) \\ \mathbf{v}_{a\Delta 1dq}(\mathbf{t}) \\ v_{a\Sigma 0}(t) \\ \mathbf{v}_{a\Sigma 1dq}(\mathbf{t}) \end{bmatrix} \quad (219)$$

More concise form of (219) is given in (220).

$$\mathbf{v}_{axydq}(\mathbf{t}) = \mathbf{K}_{aindq} \mathbf{v}_{aindq}(\mathbf{t}) + \mathbf{K}_{\Sigma\Delta dq} \mathbf{v}_{\Sigma\Delta dq}(\mathbf{t}) \quad (220)$$

Equation (210) can now be substituted in (220) as shown in (221).

$$\mathbf{v}_{axydq}(\mathbf{t}) = \mathbf{K}_{aindq} \mathbf{v}_{aindq}^m(\mathbf{t}) + \mathbf{K}_{\Sigma\Delta dq} (\mathbf{R}_{\Sigma\Delta dq} + \mathbf{X}_{\Sigma\Delta dq}) \mathbf{i}_{aco dq}^r(\mathbf{t}) \quad (221)$$

Equation (221) represents the open loop current control for arm voltages of the MMC converter in dq frame arranged as a vector $\mathbf{v}_{axydq}(\mathbf{t})$. Outputs from the equation are arm voltage references in dq frame and input are the desired output and circulating current components in dq frame given as vector $\mathbf{i}_{aco dq}^r$ and measured voltages of the grid and DC bus given as vector $\mathbf{v}_{aindq}^m(\mathbf{t})$. The vectors and matrices from (221) are listed for convenience below in (222) - (228).

$$\mathbf{v}_{\mathbf{axy}_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{ax0}(t) \\ \mathbf{v}_{\mathbf{ax}1_{dq}}(\mathbf{t}) \\ v_{ay0}(t) \\ \mathbf{v}_{\mathbf{ay}1_{dq}}(\mathbf{t}) \end{bmatrix} \quad \mathbf{v}_{\Sigma\Delta_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{a\Delta 0}(t) \\ \mathbf{v}_{\mathbf{a}\Delta 1_{dq}}(\mathbf{t}) \\ v_{a\Sigma 0}(t) \\ \mathbf{v}_{\mathbf{a}\Sigma 1_{dq}}(\mathbf{t}) \end{bmatrix} \quad \mathbf{i}_{\mathbf{aco}_{dq}}^r(\mathbf{t}) = \begin{bmatrix} i_{ca0}^r(t) \\ \mathbf{i}_{\mathbf{ca}1_{dq}}^r(\mathbf{t}) \\ i_{a0}^r(t) \\ \mathbf{i}_{\mathbf{a}1_{dq}}^r(\mathbf{t}) \end{bmatrix}; \quad (222)$$

$$\mathbf{v}_{\mathbf{ax}1_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{ax1_d}(t) \\ v_{ax1_q}(t) \end{bmatrix}; \quad \mathbf{v}_{\mathbf{ay}1_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{ay1_d}(t) \\ v_{ay1_q}(t) \end{bmatrix}; \quad \mathbf{v}_{\mathbf{a}\Delta 1_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{a\Delta 1_d}(t) \\ v_{a\Delta 1_q}(t) \end{bmatrix}; \quad (223)$$

$$\mathbf{v}_{\mathbf{a}\Sigma 1_{dq}}(\mathbf{t}) = \begin{bmatrix} v_{a\Sigma 1_d}(t) \\ v_{a\Sigma 1_q}(t) \end{bmatrix}; \quad \mathbf{i}_{\mathbf{ca}1_{dq}}(\mathbf{t}) = \begin{bmatrix} i_{ca1_d}(t) \\ i_{ca1_q}(t) \end{bmatrix}; \quad \mathbf{i}_{\mathbf{a}1_{dq}}(\mathbf{t}) = \begin{bmatrix} i_{a1_d}(t) \\ i_{a1_q}(t) \end{bmatrix}; \quad (224)$$

$$\mathbf{v}_{\mathbf{ain}_{dq}}^m(\mathbf{t}) = \begin{bmatrix} V_{DCx}^m(t) \\ V_{DCy}^m(t) \\ v_{ag1_d}^m(t) \\ v_{ag1_q}^m(t) \end{bmatrix}; \quad \mathbf{\Omega}_{\mathbf{g}2} = \begin{bmatrix} 0 & \omega_g \\ -\omega_g & 0 \end{bmatrix} \quad (225)$$

$$\mathbf{K}_{\text{aindq}} = \begin{bmatrix} 1 & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & -\mathbf{I}_{2 \times 2} \\ 0 & 1 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & \mathbf{I}_{2 \times 2} \end{bmatrix}; \quad \mathbf{K}_{\Sigma\Delta\text{dq}} = \begin{bmatrix} -\frac{1}{2} & \mathbf{0}_{1 \times 2} & \frac{1}{2} & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -\frac{1}{2}\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} \\ \frac{1}{2} & \mathbf{0}_{1 \times 2} & \frac{1}{2} & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & \frac{1}{2}\mathbf{I}_{2 \times 2} \end{bmatrix}; \quad (226)$$

$$\mathbf{R}_{\Sigma\Delta\text{dq}} = \begin{bmatrix} -(R_{ay} - R_{ax}) & \mathbf{0}_{1 \times 2} & (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(R_{ay} - R_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{2 \times 1} & (k_s R_{ax} + (1 - k_s)R_{ay} + 2R_{ag})\mathbf{I}_{2 \times 2} \\ -(R_{ay} + R_{ax}) & \mathbf{0}_{1 \times 2} & -(k_s R_{ax} - (1 - k_s)R_{ay}) & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(R_{ay} + R_{ax})\mathbf{I}_{2 \times 2} & \mathbf{0}_{1 \times 2} & -(k_s R_{ax} - (1 - k_s)R_{ay})\mathbf{I}_{2 \times 2} \end{bmatrix} \quad (227)$$

$$\mathbf{X}_{\Sigma\Delta\text{dq}} = \begin{bmatrix} 0 & \mathbf{0}_{1 \times 2} & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} - L_{ax})\mathbf{\Omega}_{\mathbf{g}2}^T & \mathbf{0}_{1 \times 2} & (k_s L_{ax} + (1 - k_s)L_{ay} + 2L_{ag})\mathbf{\Omega}_{\mathbf{g}2}^T \\ 0 & \mathbf{0}_{1 \times 2} & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & -(L_{ay} + L_{ax})\mathbf{\Omega}_{\mathbf{g}2}^T & \mathbf{0}_{1 \times 2} & -(k_s L_{ax} - (1 - k_s)L_{ay})\mathbf{\Omega}_{\mathbf{g}2}^T \end{bmatrix} \quad (228)$$

The next step is to transform the vectors back to $\alpha\beta$ domain and then use *alpha* and DC components to obtain the actual references for the converter arm voltages. This can be done by applying the transformation matrix given in (229). The first matrix applied transforms the dq coordinates into $\alpha\beta$ and the second aggregates the AC and DC components into a final reference signal. The matrix and vector terms from (229) are given in (230) and (231).

$$\mathbf{v}_{\text{axy}}(\mathbf{t}) = \mathbf{K}_{\text{vxyab}} \mathbf{T}_{\text{vabdq}}(\mathbf{t}) \mathbf{v}_{\text{axydq}}(\mathbf{t}) \quad (229)$$

$$\mathbf{v}_{axy}(\mathbf{t}) = \begin{bmatrix} v_{ax}(t) \\ v_{ay}(t) \end{bmatrix}; \quad \mathbf{K}_{\mathbf{v}_{xyab}} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix}; \quad (230)$$

$$\mathbf{T}_{\mathbf{v}_{abdq}}(\mathbf{t}) = \begin{bmatrix} 1 & \mathbf{0}_{1 \times 2} & 0 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{T}_{\alpha\beta 2} & \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 2} \\ 0 & \mathbf{0}_{1 \times 2} & 1 & \mathbf{0}_{1 \times 2} \\ \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 2} & \mathbf{0}_{2 \times 1} & \mathbf{T}_{\alpha\beta 2} \end{bmatrix} \quad (231)$$

The open loop current control from (229)-(231) can be represented in a form of a control diagram shown in Figure 33. White blocks in Figure 33 represent matrix multiplications and grey blocks represent the subsystems or transfer functions. The controller uses the measurements of voltages and transformations to the dq frame of reference described in text above. Matrix T_{dq2} is given in (181). Transfer function for the 90 degree phase sifter is given in (179). The block marked as PLL is a standard PLL extracting the angle from the sinusoidal signal. PLL will not be investigated here as this topic is extensively covered in the literature. Review of some of the common PLL systems used in power electronics systems can be found in [122].

Now that the simplest controller has been defined it can be verified in a simulation. Since the size of the module components are not defined yet at this point, the simplest model shown in Figure 20 is used for this verification. The v_{axy} from the output of Figure 33 is fed to the inputs of controlled voltage generators in Figure 20.

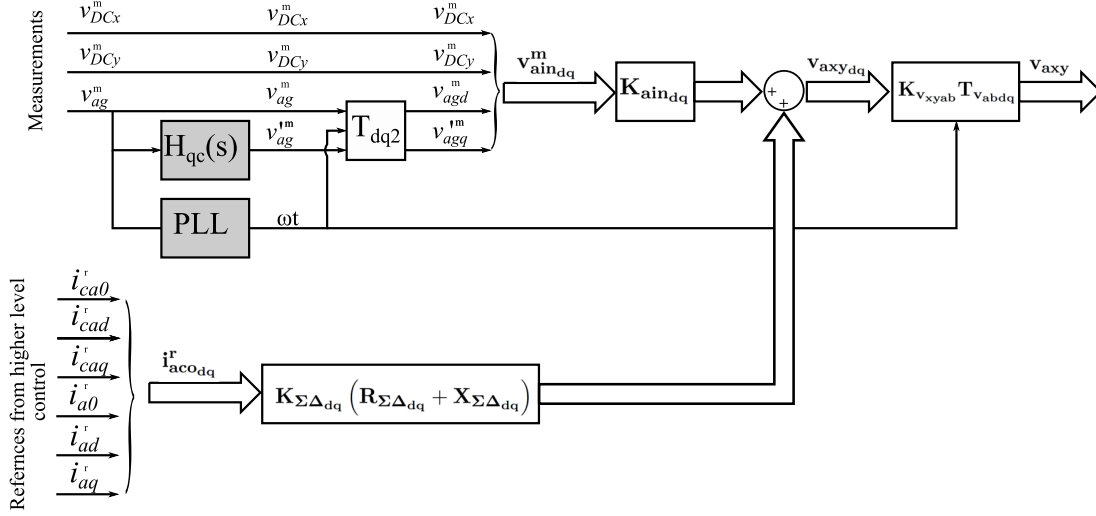


Figure 33: Open loop current controller for the MMC converter leg described in equations (229) and (221). White blocks are matrix multiplications and grey blocks are subsystems. Wide connection strips represent vectors and line represent scalars.

Table 2: Base System Parameters

Description	Symbol	Value
Base Active Power	P_{nw}	5MW
Base Power	S_n	6.25MVA
Base Voltage	V_n	13.8kV
Base current	I_n	262A
Base Impedance	Z_n	30Ω
Base Frequency	f_0	60Hz
DC Bus Voltage min.	V_{DC}	23kV

It is assumed that the converter operated in medium voltage system with parameters given in Table 2. The arm and output connection (grid) inductors are 1% and 0.1% respectively. The time constant L/R for the inductors is assumed to be 100ms which means that they are quite poorly damped for 60Hz system and that the losses are fairly low. The simulation is done in Matlab - Simulink. The model is shown in Figure 34 and the results are given further below.

Figure 35 shows the references forwarded the open loop controller. These are the coordinates of the vector $\mathbf{i}_{aco dq}(\mathbf{t})$ in the same order as in given in Equation (222) but skipping

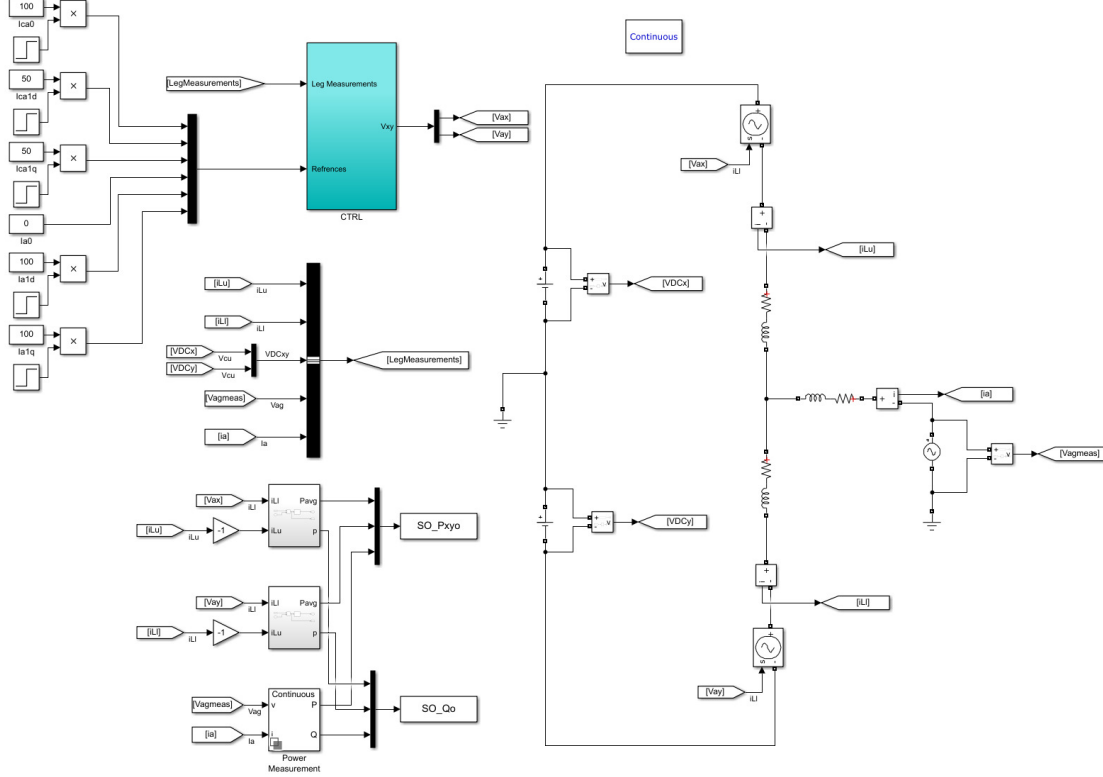


Figure 34: Simulink model of the simplified converter leg. The controller CTRL structure is shown in Figure 33.

$i_{a0}(t)$ which is always zero. The model uses ideal voltage sources for the arms so it is not important to maintain power balance within converter as described in Chapter 4.4.2. The idea at this point is to verify the control behavior with the same model it was used as a source for the circuit equations for the controller design. At $t=0.1s$ the DC component of the circulating current is set to 100A providing 2.3mW of DC power to the converter arm, half to each arm. At $T=0.5s$ d component of the output current is set to 100A, making the output current amplitude 100A all active and providing about 560kW of power to the grid. At $T=1s$ q component of the output current is set to 100A inductive (q positive), making the output current amplitude approximately 141A, providing about 560kW of active and consuming 560VAR of reactive power from the grid. At time $t=1.5s$ the q component of

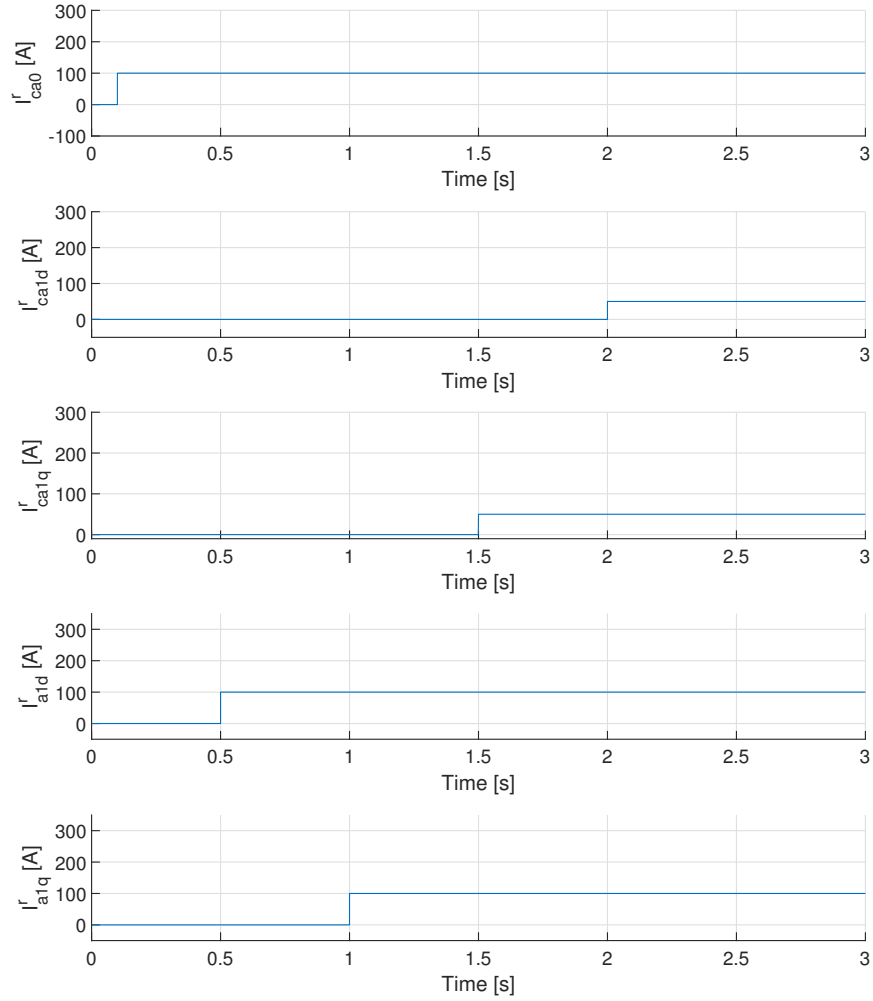


Figure 35: References given to the open loop controller. From top to bottom plot the references are: circulating current DC component, circulating current fundamental d component, circulating current fundamental q component, output current fundamental d component, output current fundamental q component. Note that the v_{ag0} is omitted in this and all other figures to save space. It is set to be constant zero in in reference and feedback vectors.

the circulating current fundamental is set to 50A changing the distribution alternate component of instantaneous power handled by the converter arms. At $t=2s$ the d component of the circulating current fundamental is set to 50A changing the distribution of average instantaneous power handled by the converter arms.

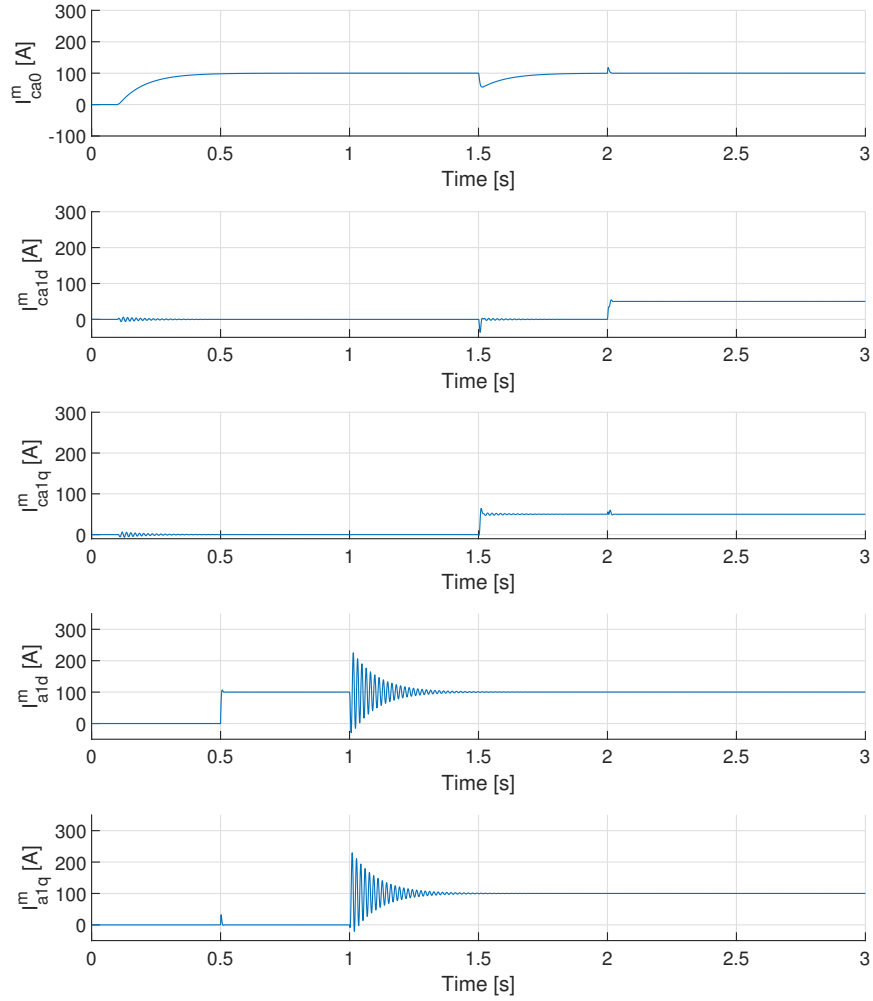


Figure 36: Measured outputs of the converter model in dq frame of reference. From top to bottom the measurements are: circulating current DC component, circulating current fundamental d component, circulating current fundamental q component, output current fundamental d component, output current fundamental q component.

Figure 36 shows the model response for the controlled variables set in the Figure 35 in the same order. As can be seen all variables settle to the correct steady state values.

The measurements shown in Figure 35 reveal few problems that will be encountered if the converter is used with the open loop control:

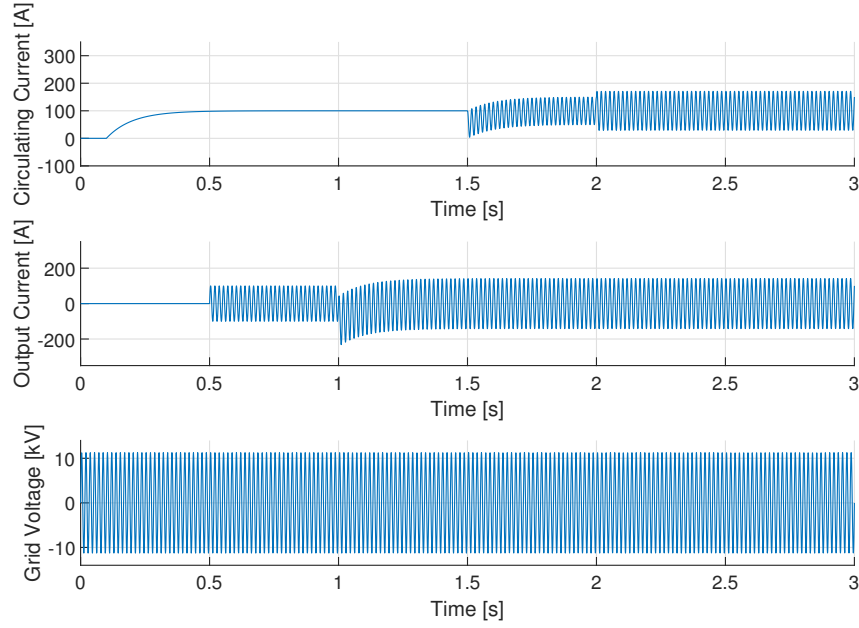


Figure 37: Measured outputs of the converter model. First plot is the circulating current, second is output current and third is the grid emf.

- The DC current time constant is much lower than the AC current. This means that the output can step up the power delivery much faster than the DC bus. As a consequence, arm modules and their internal storage elements may over-discharge if not designed and maintained with this in mind.
- Reactive q component of the output current is poorly damped and causes large swing in the current. This can be observed even in the actual current measurements in Figure 37.

Figure 38 is used to illustrate the behavior if the arm generators (which are in the actual converter arm module strings) and show the effects of various current components. Initially as the DC bus current rises, the converter arms absorb all the power from the DC bus. When the output current starts to flow at $t=0.5s$ the power absorbed by the arms drops.

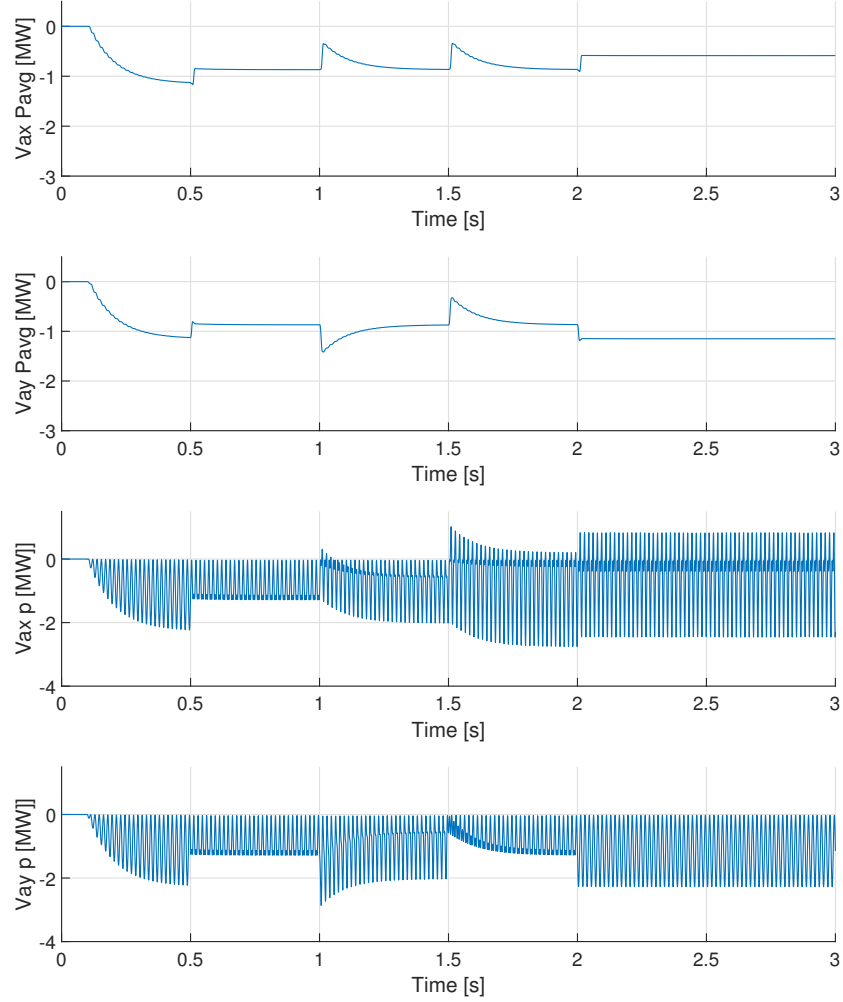


Figure 38: Output power of the arm generators. From top to bottom the plots are: average power of the upper arm generator v_{ax} , average power of the lower arm generator v_{ay} , instantaneous power of the upper arm generator v_{ax} , instantaneous power of the lower arm generator v_{ay} .

When the reactive power starts to flow at $t=1s$ the average power remains the same in the steady state but the oscillations of the instantaneous power rise significantly. During the previous intervals the arm equally shared the power. However, when the q component of the circulating current starts to flow at $t=1.5s$ the share of the instantaneous power is

not the same anymore and upper arm absorbs more of the power oscillations. The sign of the q component of the circulating current will control which leg will be more exposed to the power oscillations. When the d component of the circulating current starts to flow the average power share is not equal anymore. the upper arm now delivers more power and the preferred arm is again controlled by the sign of the current component.

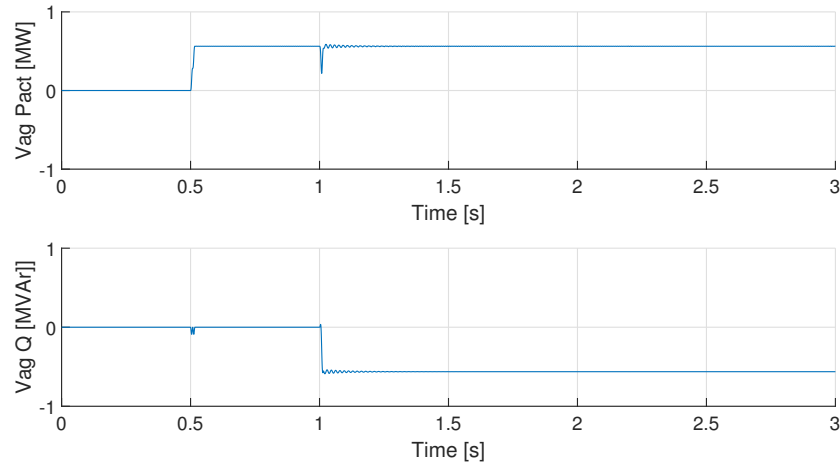


Figure 39: Active and reactive power flowing from the converter to the grid.

Figure 39 shows the active and reactive power at the output of the converter. The converter delivers power to the grid and acts as an inductive load (absorbs the reactive power from the grid).

To check that there are no unreasonable converter arm voltage references, V_{ax} and V_{ay} are shown in Figure 40. The voltage references are clearly within the expected range from 0 to the DC bus voltage.

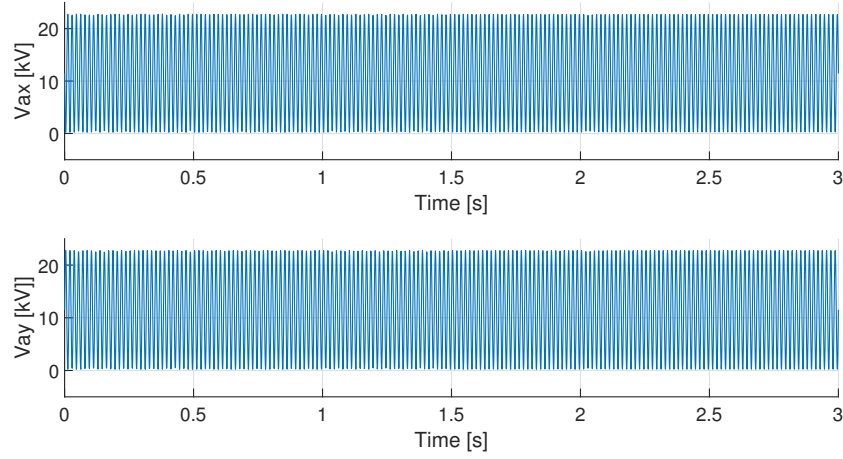


Figure 40: Upper and lower arm voltage references in $\alpha\beta$ time domain.

6.5 Closed Loop Control

As shown above the open loop controller may not work optimally and may require over sizing of the energy storage capacity of the converter arms and consequently modules. In order to improve this, the converter requires feedback compensator for the current control.

To compensate the dynamics from the previous chapter the starting point can be Equation (232), which is obtained by substituting (205) in (220) and rearranging the terms. This time the currents are not the references but they approximate the measurements (or states) and the voltages are the inputs. The same idealized model is used for the analysis.

$$\begin{aligned}
 \frac{d}{dt} \mathbf{i}_{\text{aco dq}}(\mathbf{t}) = & -\mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} (\mathbf{R}_{\Sigma \Delta \text{dq}} + \mathbf{X}_{\Sigma \Delta \text{dq}}) \mathbf{i}_{\text{aco dq}}(\mathbf{t}) \\
 & + \mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{K}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{v}_{\text{axy dq}}(\mathbf{t}) \\
 & - \mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{K}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{K}_{\text{ain dq}} \mathbf{v}_{\text{ain dq}}(\mathbf{t})
 \end{aligned} \tag{232}$$

Equation 232 can easily be transformed into a state space form suitable for feedback

analysis given in (233). Note that only $\mathbf{v}_{\text{axydq}}(\mathbf{t})$ are controlled inputs for this reason the *Bfb* matrix does not include terms with $v_{\text{aindq}}(t)$.

$$\begin{aligned} \frac{d}{dt} \mathbf{i}_{\text{aco dq}}(\mathbf{t}) = & -\mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} (\mathbf{R}_{\Sigma \Delta \text{dq}} + \mathbf{X}_{\Sigma \Delta \text{dq}}) \mathbf{i}_{\text{aco dq}}(\mathbf{t}) \\ & + \mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{K}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{v}_{\text{axydq}}(\mathbf{t}) \end{aligned} \quad (233)$$

State and input matrices can be easily obtained from (233) and are given in (234).

$$\begin{aligned} \mathbf{A}_{\text{fb}} &= -\mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} (\mathbf{R}_{\Sigma \Delta \text{dq}} + \mathbf{X}_{\Sigma \Delta \text{dq}}) \\ \mathbf{B}_{\text{fb}} &= \mathbf{L}_{\Sigma \Delta \text{dq}}^{-1} \mathbf{K}_{\Sigma \Delta \text{dq}}^{-1} \\ \mathbf{C}_{\text{fb}} &= \mathbf{I}_{6 \times 6} \\ \mathbf{D}_{\text{fb}} &= \mathbf{0}_{6 \times 6} \end{aligned} \quad (234)$$

For the system from Table 2 and Figure 35, Equation (234) reveals two complex pairs of complex conjugate poles at $(-10 \pm j37)\text{Hz}$ and two poles are at -10Hz .

It can be assumed that the desired behavior is to have no complex conjugate poles to avoid oscillations and that the settling time of the transients should be within 1-2 fundamental cycles. To achieve this all poles can be placed at 4 times the fundamental frequency of the output.

Feedback matrix \mathbf{K}_{fb} can be obtained by using Matlab command *Kfb=place(Afb, Bfb, Pfb)*. This command returns the feedback matrix for the specified systems matrices *Afb* and *Bfb* and desired set of poles *Pfb*. The command actually finds coefficients of the matrix \mathbf{K}_{fb}

such that the poles of the system with state matrix $\mathbf{A}_{fb} - \mathbf{B}_{fb}\mathbf{K}_{fb}$ match the desired set of poles given in vector \mathbf{P}_{fb} [123].

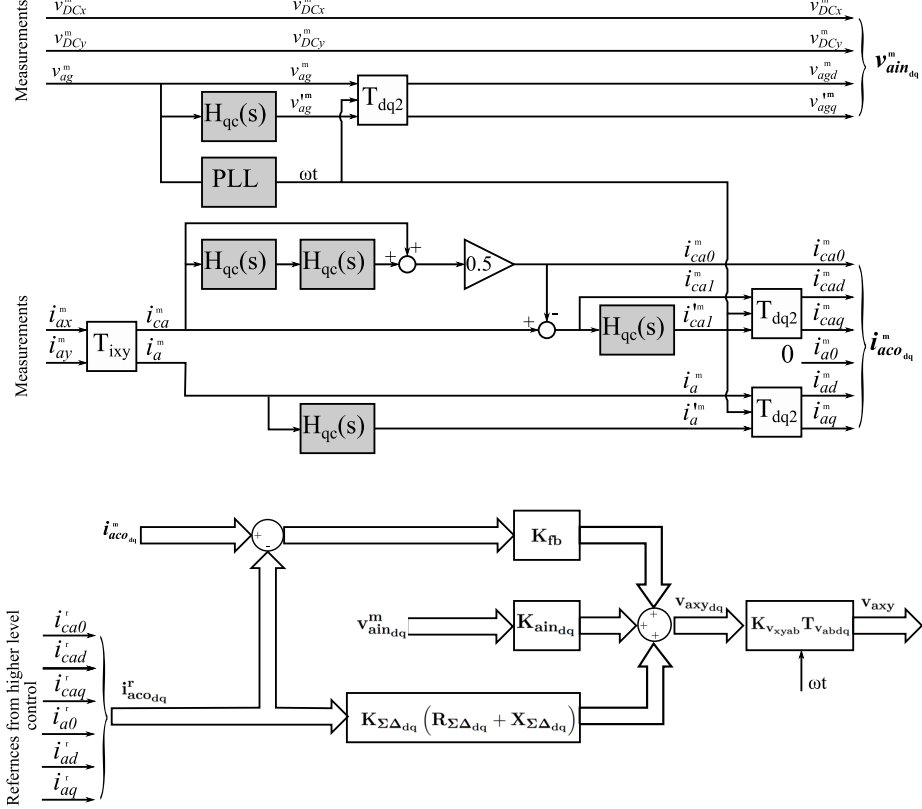


Figure 41: Block diagram for the closed loop controller. The controller includes feed forward control and closed loop feedback compensator K_{fb} for appropriate pole placement.

In order to check the behavior of the closed loop control another simulation is performed. The simulation model used this verification is the same as given in Figure 34 above. The closed loop controller with the feedback matrix k_{fb} will have the structure shown in Figure 41. The only difference between model Figure 34 and Model in Figure 41 is in the controller block (shaded block). The new implementation of this block in Simulink is given in Figure 42. Open loop control just uses zero matrix for the feedback.

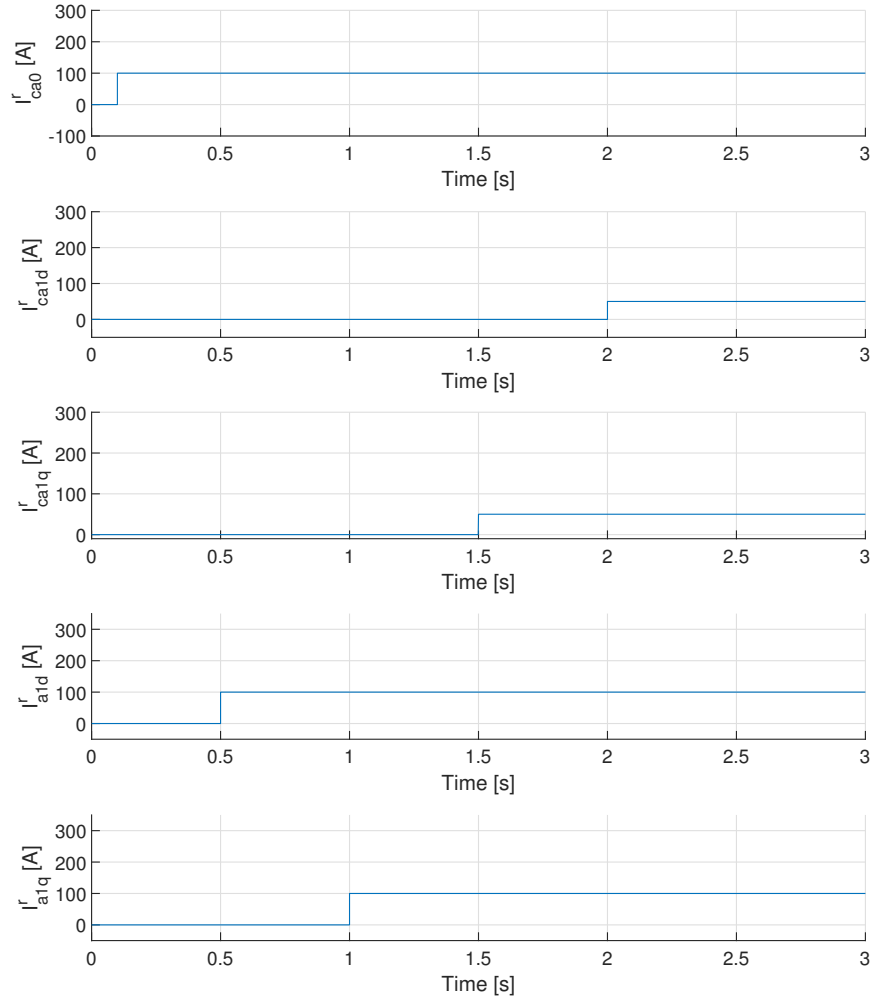


Figure 43: Current reference vector components on dq frame of reference for the close loop control simulation. For more information look at the corresponding open loop control references given in Figure 35.

The responses of the plant in dq frame of reference is shown in Figure 44. Comparing the behavior of the closed loop system with open loop in Figure 36 it can be concluded that the system behaves much more consistent across the controlled values than before. The oscillations in the grid current are also gone, which is consistent with the new placement of the poles at real axis.

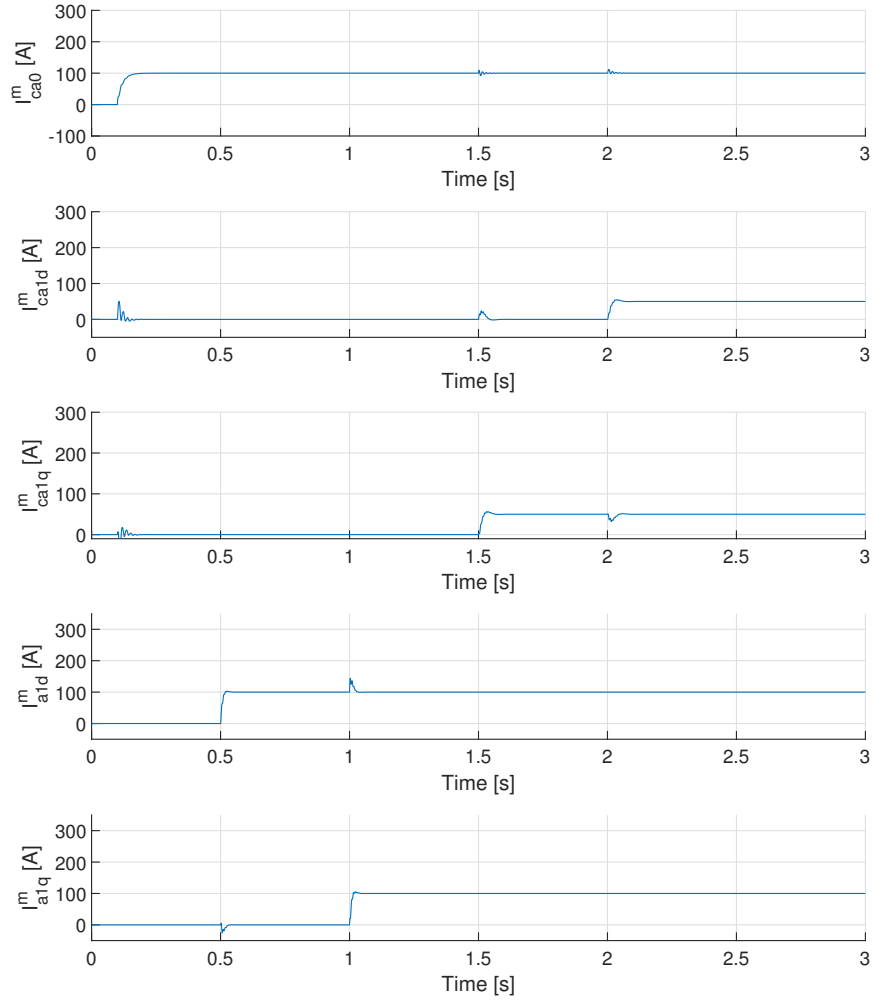


Figure 44: Current measurement vector components in dq frame of reference. For more information and comparison look at the corresponding open loop current measurements given in Figure 36.

The natural measurements of the output current, calculating current and grid voltage are given in Figure 45.

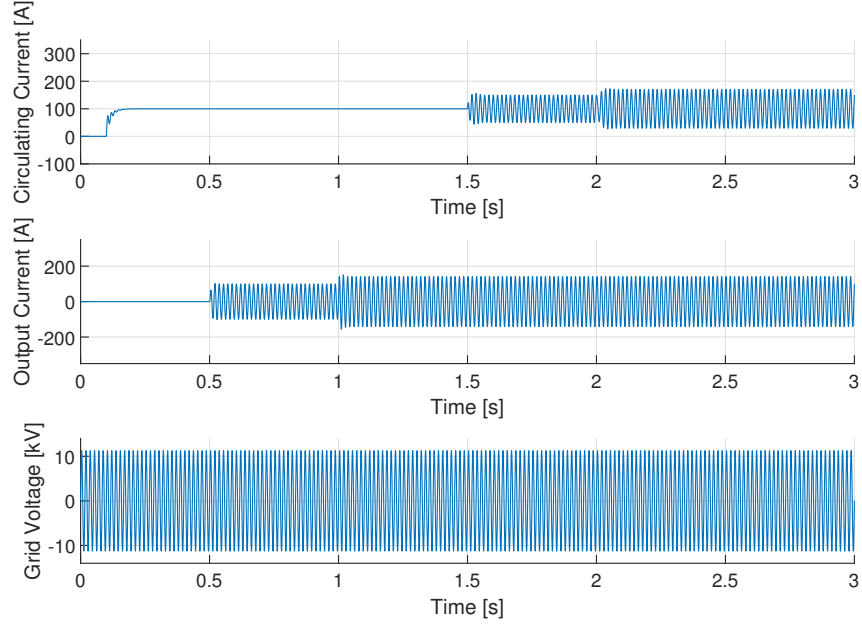


Figure 45: Circulating current, output current and grid voltage measurements in natural $\alpha\beta$ frame of reference. For more information and comparison look at the corresponding open loop measurements given in Figure 37.

The output powers of the converter arms are given in Figure 46. The closed loop controller provides much faster control over the power levels coming from the converter arms. This reduces the risks related with the size of the internal energy storage elements. Since the poles can be tuned to have the same frequency the energy difference between input DC and output AC power will be minimal during transients, assuming the same amount of power is commanded on both AC and DC sides of the converter.

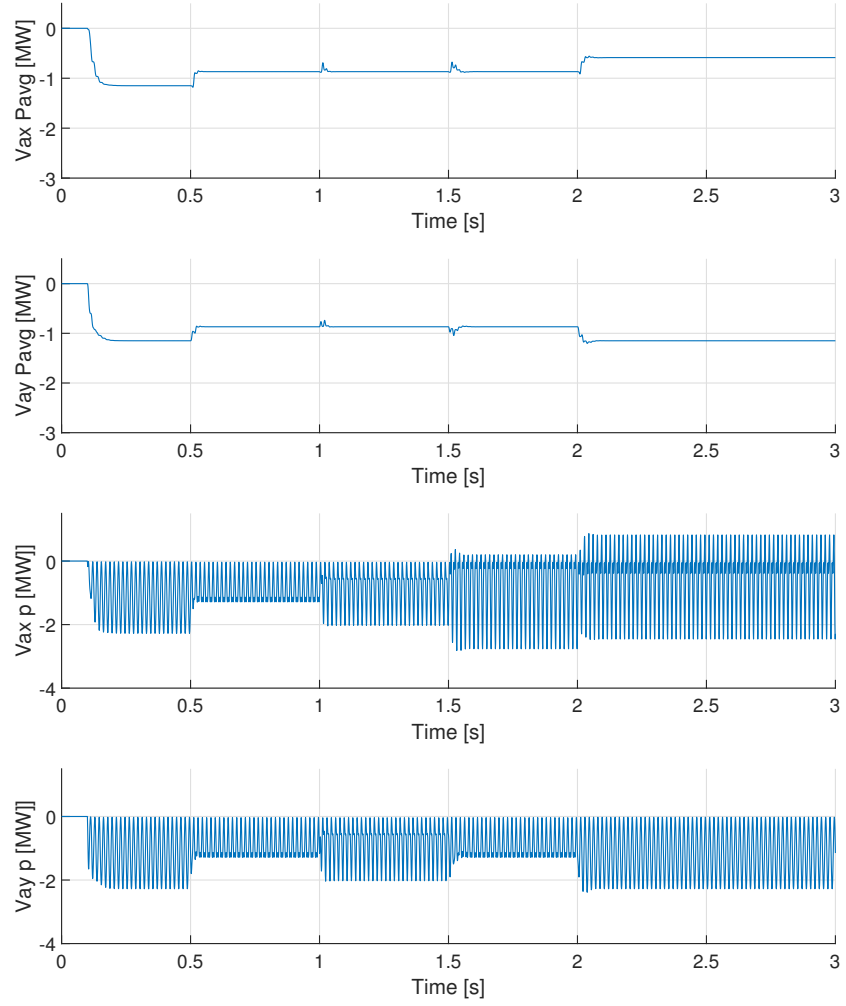


Figure 46: Output power of the arm generators. For more information and comparison look at the corresponding open loop measurements given in Figure 38.

Active and reactive power measurements at the grid source are given in Figure 47.

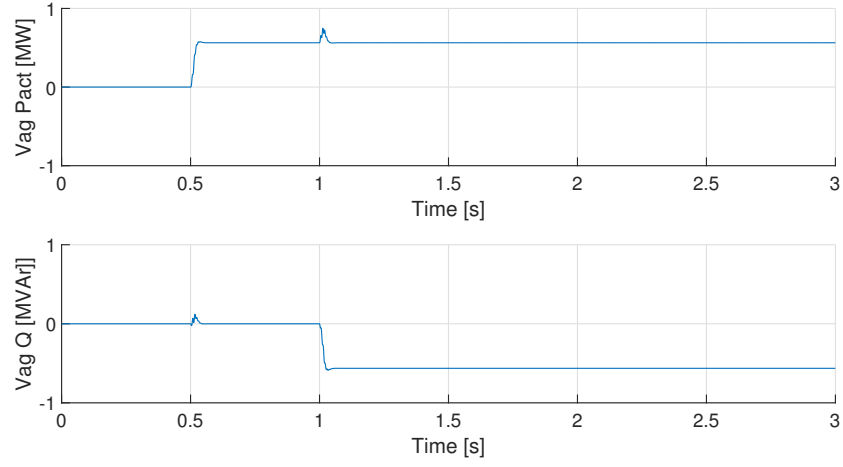


Figure 47: Active and reactive power flowing from the converter to the grid. For comparison with open loop behavior look at Figure 39.

To verify the validity of the control references for the closed loop controller, they are given in Figure 48. The references have the proper range, between 0 and DC bus voltage, and should be fully reachable by the modular converter arms.

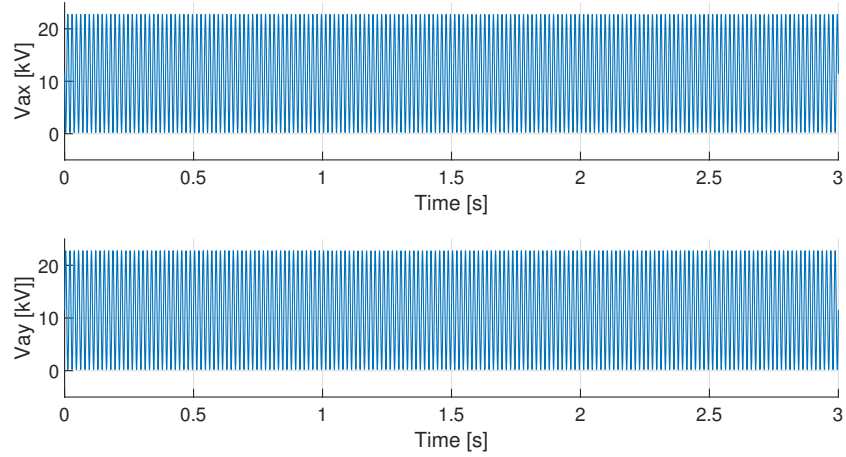


Figure 48: Upper and lower arm voltage references in $\alpha\beta$ time domain. For comparison with open loop behavior look at Figure 40.

6.6 Modulation Index References

The references produced by the controllers described above generate values that are not scaled in any way. In this particular case the range goes from 0V to about 23000V as can be seen from Figure 47. In order to relate these references with the modulation indexes which should be in the range from 0 to 1 they must be normalized. For this purpose, expression (153) given in Section 5.4.5 can be used. Equations (153) actually state that the reference voltage should be normalized with the sum of the DC bus voltages of all modules within the arm. In Equation (1) from Chapter 4, this normalizing voltages were defined as voltage reach of the converter arms V_{DCaxm} and V_{DCaym} . Consequently, the average modulation indexes can be obtained as shown in (235).

$$\begin{bmatrix} \bar{m}_{ax} \\ \bar{m}_{ay} \end{bmatrix} = \begin{bmatrix} V_{DCaxm}(t) & 0 \\ 0 & V_{DCaym}(t) \end{bmatrix}^{-1} \mathbf{v}_{axy} \quad (235)$$

6.7 Balancing

Open loop and closed loop controllers described in the previous sections will output average modulation indexes for given set of references and measurements in order to control the output and circulating currents. Individual module DC bus voltage (or state of charge) balancing is not included in these average control references nor the balancing between state of charge between arms.

6.7.1 Module Balancing

There are two main ways of balancing the module state of charge or capacitor voltages as briefly outlined in Chapter 5.4.1. For level shifted modulation and specially for simplest staircase modulation it is more convenient to use sorting balancing algorithms. These will not be covered here but are described in detail in the available literature [124]. For the phase shifted carrier modulation that is used in this investigation it is more convenient to use linear balancing algorithm. One form of the linear balancing is described in the paper by Li *et al.* [125]. Similar approach for module balancing will be outlined here as well.

The easiest way to include the balancing algorithm is to do it on the modulation index level. The individual modulation references can be modified to provide negative feedback to the deviation of the state of charge from the arm average. This can be done by applying individual module balancing control contributions to the average modulation indexes given in (235). In order to maintain precise current control, it is important to maintain the modulation index average. From the current controller standpoint, the deviations can be arbitrary as long as they sum up to zero across all modules of one converter arm as stated in Chapter 5.4.5.

Before formulating the balancing strategy, it is good to investigate the effects of modulation index modifications.

- For the structure of module shown in Figure 23 the increase in the modulation index increases the insertion time of the module and its energy exchange.
- For the structure and reference directions of currents and voltage from Figure 22 the negative sign of the arm currents i_{ax} and i_{ay} discharges and the positive charges the

module for both upper and lower arms.

- If the module deviates from the average positively (overcharge imbalance) the balancing should support discharging the module meaning increase of the modulation index during the negative current half cycle and decrease over positive half cycle of the arm current.
- If the module deviates from the average negatively (over-discharge imbalance) the balancing should support charging the module meaning increase the modulation index during the positive current half cycle and decrease during negative half cycle of the arm current.

Following the reasoning above the average modulation index decrease should be proportional to the product of deviation of the state of charge from the desired level and the arm current or just the sign of the arm current. To ensure that the effects of the balancing will not influence the current controller described in the previous chapter the desired level can be the average of the state of charge of all modules of the converter arm.

The balancing controller can now be formulated by the few equations below. Equation (236) gives the arm average module voltage based on the measured output voltages of the filter section of the module. This will be the base value for the balancing.

$$\begin{aligned}\overline{v_{fax}} &= \frac{1}{N} \sum_{i=1}^N v_{fax}[i] \\ \overline{v_{fay}} &= \frac{1}{N} \sum_{i=1}^N v_{fay}[i]\end{aligned}\tag{236}$$

The deviation from the average value can be obtained and normalized. These deviations fulfill the condition of zero sum and can be multiplied with the arm current or just the sign of arm current to obtain the modulation index deviations as shown in (237).

$$\begin{aligned}\mathbf{m}_{\Delta\mathbf{ax}} &= K_{bal} \left(\frac{1}{v_{fax}} \mathbf{v}_{\mathbf{fax}} - 1 \right) \text{sign}(i_{ax}^m) \\ \mathbf{m}_{\Delta\mathbf{ay}} &= K_{bal} \left(\frac{1}{v_{fay}} \mathbf{v}_{\mathbf{fay}} - 1 \right) \text{sign}(i_{ay}^m)\end{aligned}\tag{237}$$

The modulation index for each module can be obtained now by adding averaged modulation indexes from (235) to the deviations in (238).

$$\begin{aligned}\mathbf{m}_{\mathbf{ax}} &= \bar{m}_{ax} + \Delta\mathbf{m}_{\mathbf{ax}} \\ \mathbf{m}_{\mathbf{ay}} &= \bar{m}_{ay} + \Delta\mathbf{m}_{\mathbf{ay}}\end{aligned}\tag{238}$$

The balancing algorithm and the generation of module modulation indexes are represented in the block diagram given in Figure 49. Gain K_{bal} tunes the negative feedback effect for the balancing and will have to be obtained experimentally or estimated using the switching model described in Chapter 5.3. In general, the imbalances will develop relatively slowly for higher switching frequencies and a well-controlled converter. Besides the effects that are easy to simulate, like transients the imbalances will develop due to the differences in parasitic elements within the modules. Practical implementation and the actual assembly structure of the converter (losses in wires, active and passive components) will influence it. As a result, the precise tuning will have to be done only on the actual implementation of the

converter.

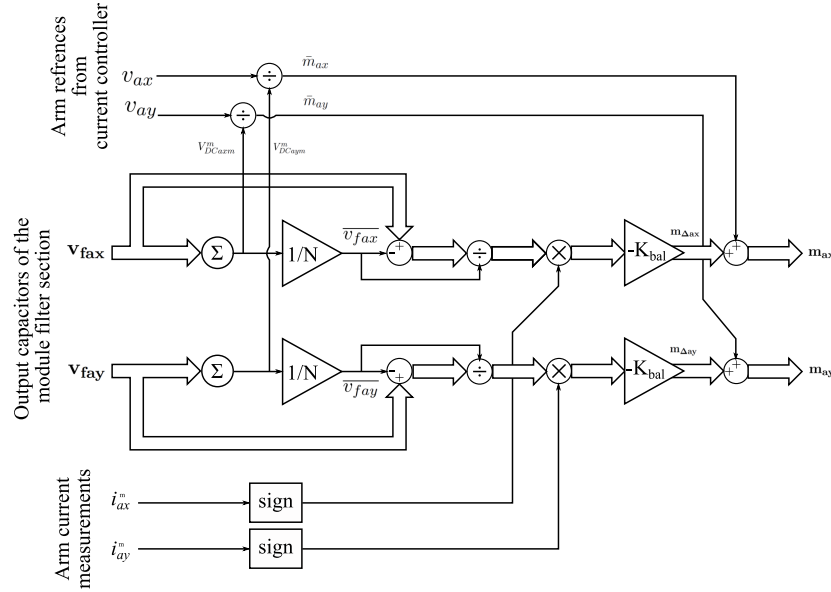


Figure 49: Block diagram for module state of charge balancing and generation of normalized modulation indexes. Wide lines represent vectors of width N and thin lines are scalars.

The balancing algorithm described in this section is based on the measurement of the output voltage of the filter section which is acceptable when modules contain capacitor energy storage only. In cases when modules contain batteries or other types of energy storage, the balancing can be based on the state of charge of the module energy storage system. It can be directly measured if possible or can be obtained from the dedicated energy storage monitoring system. In this case the balancing algorithm will have the state of charge and the output voltage of the filter section as well. Output voltage of the filter section is necessary to obtain the averaged modulation index.

6.7.2 Arm Balancing

The MMC converter arrangement investigated in this work has two arms per each leg. As a result, the balancing between state of charge has to be maintained between the converter

arms of the same leg as well. The arm balancing can be achieved by changing the power flow withing the converter. It was suggested in 4.4.2 and showed in the simulations above that this can be done with the fundamental component of the circulating current.

The arm balancing controller can be implemented as a higher level controller for the current controller described in Chapter 6.5. The block diagram for the proposed controller is shown in Figure 50.

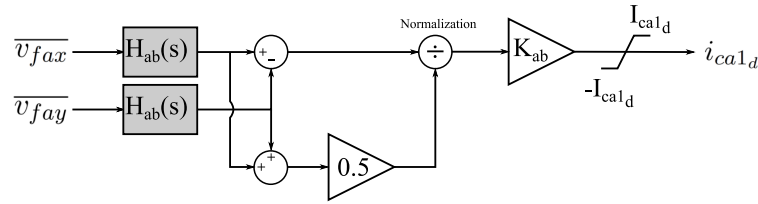


Figure 50: Block diagram for the balancing of arm state of charges within one leg of the converter.

Two filters $H_{ab}(s)$ in Figure 50 are low pass filters that will eliminate the fundamental and the first harmonic components from the voltage measurements. The imbalance between legs accumulates slowly, same as the imbalance between modules of one arm. As a result the low pass filter pole can be placed a decade below grid frequency. The gain K_{ab} will again have to be determined experimentally for the same reasons mentioned above for the module balancing gain K_{bal} .

6.8 Poly-phase System Considerations

The controller described above has currents source properties on AC and DC side as well. The controller assumes that a stiff DC source is present on the DC side of the converter. Furthermore, due to the nature of MMC topology the DC side source is above "rectified"

AC side voltage. Otherwise, the anti-parallel diodes in the converter modules will conduct, which may destabilize the control.

As a result, for the poly-phase systems with all identical MMC legs where the DC side source is not maintained externally, one leg has to act as a bus regulator and maintain the DC bus levels. Since this leg will have to act as a bus regulator, the current control loop on the DC side has to be eliminated from the controller described above. As the arm and module balancing depend on the DC side current control this bus controller converter arm will have to maintain its internal balance by influencing controllers for other arms in the structure.

There is another rather simpler but potentially more expensive way to maintain the DC bus. Since all converter legs have full DC side current control, a bus controller can be designed to maintain the bus across externally added passive impedance like a string of capacitors or another auxiliary energy storage string. This impedance can be sized based on the expected AC components of the circulating currents and dominant time constants of the bus controller. For balanced multi-phase system, AC components flowing through this externally added impedance should be relatively small compared to other values within the converter. The bus controller objective will then be simple, to regulate the DC components of all converter legs in the structure and maintain fairly regulated DC voltage across the externally added impedance.

Both of these solutions require a fairly complicated system level control analysis, which falls out of the scope of this study and will be left for future research.

7 Converter Sizing

The capacitor sizing in the case of the simplest module implementation #1 from Chapter 5.1 is well covered in the literature [126], [127], [128] and will not be further analyzed here. However, the sizing process for the MMC converter with integrated energy storage outlined below is more general and can be used to design the converter with a simpler structure. The study outlined below will extend and generalize the procedure outlined in [91] which was focused on more particular example.

As with any complicated structure, the solution that meets the same set of requirements does not have to be unique in case of MMC converter. Depending on how the requirements of the design are formulated there may be few variables that will be left loosely constrained. As a result, there may be a range of solutions that will satisfy the requirements. In order to settle for a particular solution two design approaches can be identified: One is the approach based on good engineering estimations that will guide the design to a particular solution. The other approach is optimization based. Optimization approach settles for the solution that minimizes some predefined cost function.

7.1 General System Parameters

The system requirements and operating conditions for the MMC converter sizing are listed below. It will be assumed that these parameters are design inputs and are defined prior to the converter parameters sizing. Input parameters are listed and explained below:

- System nominal AC voltage V_n is the voltage of the AC system the converter is connected to (i.e. voltage of the medium voltage grid connection).

- System nominal DC voltage V_{DC} is the voltage of the DC system the converter is connected to (i.e. voltage of the DC bus of the back to back conversion system or DC transmission system voltage).
- Number of system phases n_{ph} . In most case this will be 3 but for generality it may be more or less. Since the converter analysis is done on per leg basis, the number of phases will not affect anything stated before.
- The tolerance of the system AC voltage Δ_{V_n} . This parameter represents maximum deviation of the system AC voltage with respect to the nominal value, normalized (per unitized) by nominal value.
- Nominal system frequency f_n . For the MMC this should be the lowest system frequency the converter is expected to operate at full current. In general, the lower frequencies introduce more ripple in the MMC structure and could cause problems in the system stability.
- The converter nominal active power P_n is the maximum active power converter is expected to output.
- The converter nominal apparent power S_n or nominal reactive power capability Q_n are can be used to complete the nominal power definition of the converter. The reactive and apparent power are linked with active power as shown in Equation (239).

$$S_n^2 = P_n^2 + Q_n^2 \quad (239)$$

- Maximum output THD.
- Minimum output connection impedance in percents of the rated system impedance.
This is the external impedance of the converter connection point (i.e. grid impedance).
- Storage requirement defined by the rated energy E_{es} of the integrated energy storage.
- Maximum module voltage V_{fmax} . This parameter is based on the selection of the semiconductor technology. For example, if 1200V semiconductors are used they may allow maximum DC bus voltage of 800V accommodating 400V for switching transients. The current rating of the semiconductors is somewhat determined by the voltages on the AC and DC side of the converter leg and the power rating. Furthermore, IGBT module selection or paralleling can be used to achieve most current ratings of interest here. As a result, the current rating of the semiconductor is will not be considered as a limiting factor.

The parameters above outline the system requirements and the conditions the converter will operate in. Beside these parameters some initial assumptions on the energy storage technology will be made as well. It will be assumed that the energy storage will be made of a number of basic cells (e.g. battery, super-capacitor or ultra-capacitor cells). The technology of the cell will dictate some of its basic properties as:

- Energy storage cell maximum voltage V_{scmax} is the maximum voltage of the storage cell the storage system within each module will be built from. It can be basic Li-ION battery cell, ultra-capacitor cell or some other type of energy storage element convenient for the application.

- Energy storage cell energy rating E_{scmax} is the storage rating of the basic energy storage cell.
- Energy storage cell maximum current I_{scmax} is the maximum RMS current of the energy storage cell. This included useful DC component and loss causing harmonic components.
- Energy storage cell discharge characteristic $V_{sc}(\delta_{sc})$ will be used here links the Depth of Discharge δ_{sc} with the storage cell voltage V_{sc} . The discharge characteristic showing the voltage as a function of discharge capacity is usually given for the batteries and can be easily converted to the voltage by depth of discharge by normalizing the discharge capacity axis. Discharge characteristic is usually given graphically in datasheets, for the analysis in this text it would either have to be expressed analytically or taken as an interpolated lookup table.

For the super-capacitor and similar energy storage systems the link between the voltage and depth of discharge can be easily expressed analytically as shown in Equation (240). As a result, instead of the discharge characteristic, rated energy and capacitance will be sufficient for ultra-capacitors and super-capacitors.

$$V_{sc}(\delta_{sc}) = \sqrt{\frac{2(1 - \delta_{sc})E_{scmax}}{C_{sc}}} \quad (240)$$

Depth of discharge δ_{sc} is defined as a normalized fraction of the total storage capacity that has been discharged from the storage as shown in (241).

$$\delta_{sc} = \frac{E_{sc_{max}} - E_{sc}}{E_{sc_{max}}} \quad (241)$$

The rough cell size selection can be done based on the total power and energy of the system and the DC bus voltage rating. Equations (242) and (243) will allow a rough estimation of the storage cell energy and current for a single string per module case. For batteries $\delta_{sc_{est}}$ can be assumed to be 100%. For capacitive storage cells the entire stored energy may not be available as the voltage may drop too low, for the purpose of this estimation 20% should be reasonable assumption. A cell with the closest current and energy rating can be chosen as a starting point for the application. In case of a significant mismatch between available ratings and the estimations, the energy and current estimation can be divided by an integer number of the parallel strings until the closes match presents itself for a particular storage technology.

$$E_{sc_{est}} = \frac{E_{es}}{\delta_{sc_{est}} 2n_{ph} \frac{V_{DCn}}{V_{sc_{max}}}} \quad (242)$$

$$I_{sc_{est}} = \frac{P_n}{2n_{ph} V_{DCn}} \quad (243)$$

7.2 Example System Parameters

The items listed in Section 7.1 are given in Table 3 for one particular system. Table 3 lists the requirements for the example system: the converter operating as a grid tie converter in a wind energy system with fault ride through capability. One example of the fault ride

through profile is shown in Figure 51.

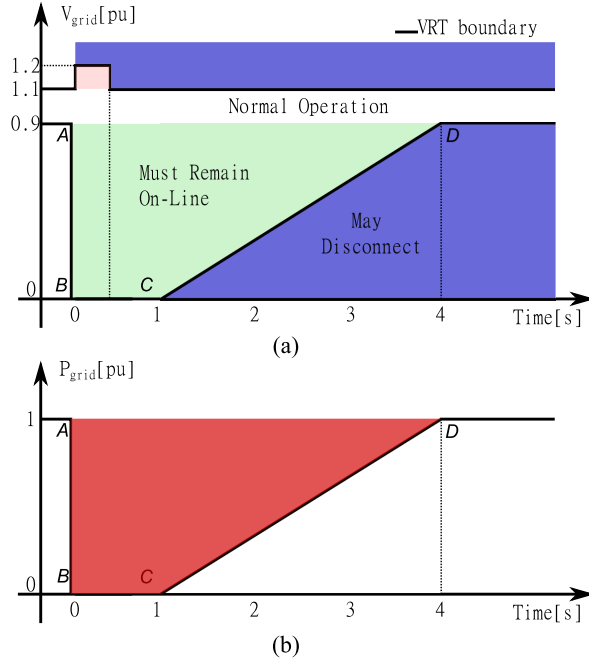


Figure 51: (a) - Fault Ride Through requirements for large wind energy system meeting all the requirements listed in [5]. (b) - Assumed power delivery profile. Energy storage rating can be obtained by calculating the red shaded surface area.

The worst case for the energy storage is when the wind is at full power and the fault follows the profile from Figure 51-(a). In this case the requirement for the stored energy can be obtained by calculating the area of the red shaded surface in Figure 51-(b). The energy requirement for the system from Table 3 sums up to 3.47kWh, which can be rounded up to 5kWh to accommodate for storage system tolerances.

The basic parameters of the energy storage are given in Table 4. Note that the assumption is that the storage system in each module will consist of n_{scs} parallel strings of n_{sc} identical energy storage cells connected in series. The system described above requires short term high power energy storage technology which correlates well with the high power / moderate energy density of ultra-capacitor or super-capacitors [129]. Using equations (242) and (243)

Table 3: Sizing requirements and operating conditions

Description	Symbol	Value
Nominal System Voltage	V_n	13.8kV
Nominal System DC Bus level	V_{DCn}	23kV
Number of phases	n_{ph}	3
Input voltage Tolerance	ΔV_n	0.1
Nominal system frequency	f_n	60Hz
Nominal Active Power	P_n	5MW
Nominal Apparent Power	S_n	6.25MVA
Maximum Output THD	THD	5%
Storage Requirement	E_{es}	5kWh
Grid Impedance	Z_g	0.1% Inductive
Maximum module voltage	V_{fmax}	800V

for 3V rated cells the current rating of the cell should be in the 40A range and the energy in the range of 0.5Wh. The parameters for one commercially available ultra-capacitor storage cell that will meet the requirements well are given in Table 4.

Table 4: Energy Storage Cell Parameters [6]

Description	Symbol	Value
Full Charge (maximum) Voltage	V_{scmax}	2.7V
Storage Rating	E_{scmax}	0.66Wh
Capacitance	C_{es}	650F
Maximum RMS Current	I_{scmax}	54A
Ekv. Series Resistance (ESR)	R_{scesr}	0.8mΩ

7.3 Design constraints

The general system requirements listed in the previous section should be linked with the design variables by imposing proper design constraints. Design constraints will be given in the following section as a system of inequalities.

7.3.1 Voltage Reach of the Converter Arm

For the structure from Figure 22, three sources are connected to the converter leg. One is on the AC side and two on the DC. For the sizing analysis the DC bus voltage will be the sum of the two sources on the DC side and it will be assumed that the mid point is exactly half of the full DC voltage.

For the proper operation of converter as described in the previous chapters, the total sum of all module filter section output voltages (module DC bus voltages) within each converter arm must be above the minimum level that allows full control of the output and circulating current. This was defined as a voltage reach of the converter arms and is given in Equation (2) as V_{DCm} . For the proper control of output and circulating currents the voltage reach of the converter arm must be above the externally applied DC bus source.

For the structure where the mid point of the DC bus is grounded as shown in Figure 22 operating in the balanced 3 phase system, the minimum external DC bus source voltage cannot be below the limit given in (244). For ungrounded system, the minimum DC bus level is given in (245). To achieve levels from (245) for ungrounded systems third harmonic injection is required and should be added to the control algorithms described in Chapter 6. Note that these levels do not take into account the voltage drops across arm and output impedances. Also note that operating in the over-modulation region should be avoided as it stops the PWM and with it the proper balancing and control of circulating currents.

$$V_{DCm_{min}} = \sqrt{\frac{2}{3}}(1 + \Delta_{V_n})V_n \quad (244)$$

$$V_{DCm_{min}} = \sqrt{2}(1 + \Delta_{V_n})V_n \quad (245)$$

In case when the leg is setting the DC bus voltage (acting as a bus controller), Equations (244) and (245) define absolute minimums of the bus. In the case when the bus voltage V_{DCn} is applied externally the limit for the voltage reach of the arm becomes the externally applied bus voltage.

$$V_{DCm_{min}} = V_{DCn} \quad (246)$$

The voltage reach of the converter arm is maintained by the string of modules connected in series. The module DC bus voltage average is maintained by string(s) of storage cells connected in series. At the maximum depth of discharge and worst case ripple, the voltage reach of the converter arm must be above the minimum that allows proper control of the output and circulating current. This value will depend on the implementation and will either be the externally applied DC bus from (246) or the value given in (244) or (245). This condition is summarized in (247).

$$Nn_{sc}V_{sc}(\delta_{sc}) - N\Delta_{V_f} \geq V_{DCm_{min}} \quad (247)$$

The design variables that can be identified in the (247) are: the number of modules per arm N , the number of storage cells in one storage string of the spanning across module DC bus n_{sc} , the maximum allowed voltage ripple in the output of the filter section of the module Δ_{V_f} and depth of discharge δ_{sc} .

The discharge characteristic of the storage is given in Equation (240) for capacitive storage cells. For more complicated discharge characteristics curves, (e.g. battery) interpolated lookup table can be used.

7.3.2 Module DC Voltage

The output of the filter module cannot exceed the maximum voltage level given as V_{fmax} in Table 3, which is based on the semiconductor voltage ratings. To keep the filter output voltage below the maximum, a margin for the ripple should be added on top of the average voltage kept by the storage section of the module, as shown in (248).

$$n_{sc}V_{scmax} + \Delta V_f \leq V_{fmax} \quad (248)$$

7.3.3 Storage Power Rating

All cells within the converter will have to be able to absorb or deliver the full power of the converter in the worst case. The worst case would be the charging of the fully discharged storage when the cell voltage is lowest with the full active power of the converter.

It can be assumed that the power is equally spread among all storage cells within the module and within all modules of an arm and between arms of the converter leg and between all phase legs of the converter. As a result, the power rating of the storage cells must meet the requirement given in (249).

$$2Nn_{ph}n_{sc}n_{scs}I_{sc}V_{sc}(\delta_{sc}) \geq P_n \quad (249)$$

Design variables here are the average storage current I_{sc} , the number of parallel storage strings across the module DC bus n_{scs} , and the depth of discharge of the energy storage cell δ_{sc} .

7.3.4 Storage Energy Rating

The sum of all available energy stored within all storage cells within all modules of all arms and legs of the converter must meet the requirement from Table 3 while not exceeding the maximum depth of discharge. This condition can be expressed as shown in Equation (250).

$$2Nn_{ph}n_{sc}n_{scs}\delta_{sc}E_{sc} \geq E_{es} \quad (250)$$

7.3.5 Energy Storage Current

The average (or DC component) of the storage current is the design variable and must meet constraints given in (249). Besides the average value, the energy storage current will contain harmonic components (or ripple) $\Delta_{I_{sc}}$ as well. Ripple in the storage current is unavoidable in this case and will be determined by the module filter section design. As a result, ripple (or harmonic) storage current will be the design parameter as well. The RMS value of the average component and ripple component of the storage current must be below the RMS rating of the energy storage cell as expressed in Equation (251).

$$\sqrt{I_{sc}^2 + \Delta_{I_{sc}}^2} \leq I_{scmax} \quad (251)$$

The Storage cell current ripple RMS will be a design variable in the same manner the

filter section output voltage ripple used in Section 7.3.1.

7.3.6 THD and Ripple

Ripple on the storage current and filter output voltage are design variables for the converter sizing that will be used as parameters for filter section design of the module. The filter design will be done after the converter sizing and may require several iterations to reach satisfactory performance.

The arm inductors will be sized later as well. The inductance will be influenced by the THD requirement from Table 3 and the maximum voltage of the structure and number of modules per arm which will be determined by the converter sizing in this section. The output current THD will depend on many parameters of the converter including the control and may require few iterations to reach satisfactory results as well.

Note that the converter arm inductor is supposed to filter out the components at the effective switching frequency range while the module filters will have to handle frequencies at the range of the fundamental and 1st harmonic of the output current. However, both inductors will influence the output current THD.

7.3.7 Constrain and Variable Summary

Based on the sections above, design variables and constraints can be summarized as shown in Table 5.

Table 5: Sizing Variables and Affected Constraints

Variable Description	Symbol	Constraint Equations
Number of modules per arm	N	(247), (249), (250)
Number of cells per storage string	n_{sc}	(247), (248), (249), (250)
Number storage strings	n_{scs}	(249), (250)
Depth of discharge	δ_{sc}	(247), (249), (250)
Storage cell current	I_{sc}	(249), (251)
Storage cell current ripple RMS	ΔI_{sc}	(251)
Module filter voltage ripple	ΔV_f	(247), (248)

7.4 Converter Sizing - Approximation Approach

Based on the constraints above the sizing based on the engineering approximations can be summarized as follows:

1. Allocate the margin for the module output filter ripple ΔV_f as the percentage of the maximum module voltage V_{max} .
2. Calculate the number of storage cells per module storage string using constraint given in Equation (248) by finding the minimum integer n_{sc} that meets the constraint.

3. Set the value of the depth of discharge that will make good use of the energy storage.

For batteries this can be fairly high e.g. 95%. For capacitive storage cells the higher the depth of discharge goes the lower the minimum voltage is. A number above 50% may be a good choice to keep the minimum module voltage relatively high and keep the number of modules in the reasonable range.

4. Calculate the number of modules using Equation (247) by finding the minimum integer N that meets the constraint. The minimum voltage reach of the arm may have to be determined first using (246).
5. Calculate the number of storage strings using Equation (250) by finding the minimum integer n_{scs} that meets the constraint.
6. Calculate the storage cell current using (249) by assuming the corner case when the left and right side of the equation are equal.
7. Calculate the available storage cell ripple margin using (251) by assuming the corner case when the left and right side of the equation are equal.
8. Readjust the storage cell selection if needed and repeat all steps.

Note that the procedure outlined above gives one corner case solution that may not be optimal in terms of module number, cost or storage utilization. However, this solution will give a reasonable starting point for the further optimization algorithms.

7.4.1 Example System Results

Following the procedure outlined in Section 7.4, the design solution for the system example from Table 3 and Table 4 can be obtained. The results are summarized in Table 6.

7.5 Converter Sizing - Optimization

As stated before, the design solution for the MMC converter leg described in Section 7.4 is not unique. To achieve more flexibility in the design process it may be of interest to

Table 6: Design Solution Parameters - Arm parameters, estimate

Variable Description	Symbol	Constraint Equations
Module filter voltage ripple amplitude	$\Delta_{V_{f0}}$	80V
Depth of discharge	δ_{sc0}	0.5
Number of cells per storage string	n_{sc0}	267
Number of modules per arm	N_0	54
Number storage strings	n_{scs0}	1
Storage cell current	I_{sc0}	30.2A
Storage cell current ripple RMS	$\Delta_{I_{sc0}}$	44.8A

formulate the design procedure as a optimization problem.

It can be shown that the number of modules is a trade off to the utilization of energy storage system, especially when the ultra-capacitors are used. As the utilization of the storage goes up the depth of discharge goes up and the lowest module voltage goes down. As a result, the number of modules to achieve the minimum voltage reach of the converter arm increases. To achieve a balanced design, it may be of interest to formulate optimization cost function (or objective function in terms of number of modules, depth of discharge and number of storage cells per module. One possible cost function that can be used is given in (252). The number of modules, deviation from preset depth of discharge and number of storage cells per module are normalized to make the achieve easier weighting.

$$cost = k_{c1} \left(\frac{N}{N_0} \right) + k_{c2} \left(\frac{|\delta_{sc} - \delta_{sc0}|}{\delta_{sc0}} \right) + k_{c3} \left(\frac{n_{sc} n_{scs}}{n_{sc0} n_{scs0}} \right) \quad (252)$$

k_{c1} , k_{c2} and k_{c3} are the weight coefficients that allow the adjustment of the impact of the number of modules, number of storage cells per module and deviation from δ_{sc0} depth of discharge. N_0 is the number of modules and δ_{sc0} is the depth of discharge n_{sc0} and n_{scs0} are the numbers of storage cells in a string and number of strings per module given obtained

from the engineering solution.

Cost function given in (252) with the design constraints expressed in (247), (248), (249), (250) and (251) can be used to formulate the constrained optimization problem. Solvers available in Matlab can be used to find the solution. One implementation of the optimization Matlab code is given in Listing 1.

The requirements of the system and engineering solution from Section 7.4 results are stored in "*ConverterParameters.mat*" for easier manipulation into the work-space. The design constraints are expressed in variables C1-C6. Power and energy constraints are entered as strict equality constraints to match the requirements as close as possible. Constraint C7 ensures at least one whole string per module. It should be noted that the algorithm and solver given in Listing 1 output real numbers that must be rounded to obtain the actual number of modules, cells and strings. This may cause some deviation from the minimums. If the deviation cannot be tolerated the constraints of the optimization can be adjusted until the desired ratings are met or the error is acceptable.

7.5.1 Example System Results

The optimization results for the example system are summarized in Table 7. The results are obtained by running the optimization algorithm from Listing 1 on the example system data given in Table 3, Table 4 and Table 6. For this example the weight coefficients k_{c1} , k_{c2} and k_{c3} were set to one giving the same significance to the number of modules, number of storage cells and utilization of energy storage.

Note that the optimization resulted in significantly smaller system regarding the number of modules. Based on these results it can be concluded that the flaw with the "engineering

Listing 1: Arm parameter optimization code in Matlab

```

1 load('ConverterParameters.mat');
2 x0=[N0, nsc0, nscs0, dsc0, Isc0];
3 options=optimoptions('fmincon','Algorithm','interior-point',...
4 'MaxIterations',10000,'MaxFunctionEvaluations',10000);
5 [x,fval,exitflag,output]=fmincon(@CostFcn,x0,[],[],[],[],...
6 [],[],@CondFcn,options);
7
8 function cost=CostFcn(x)
9     load('ConverterParameters.mat');
10    N=x(1); nsc=x(2); nscs=x(3); dsc=x(4); Isc=x(5);
11    cost=1*N/N0+1*(abs(0.5-dsc)/dsc0)+1*nsc*nscs/(nsc0*nscs0);
12 end
13 function [c,ceq]=CondFcn(x)
14     load('ConverterParameters.mat');
15    N=x(1); nsc=x(2); nscs=x(3); dsc=x(4); Isc=x(5);
16    Vdcm_min = max(23e3,sqrt(2/3)*(1+DVn)*Vn);
17    C1 = Vdcm_min-N*nsc*StorageChar_Fsc(dsc, Escmax, Csc)+N*(Dvf);
18    C2 = nsc*Vscmax+Dvf-Vfmax;
19    C3 = dsc-dscmax;
20    C4 = Isc-Iscmax;
21    C5 = Ees-(2*N*nph*nsc*nscs*dsc*Escmax);
22    C6 = Pn-(2*N*nph*nsc*nscs*Isc*StorageChar_Fsc(dsc, Escmax, Csc));
23    C7 = 1-nscs; %Ensures that there is at least one string
24    c=[C1, C2, C3, C4, C7];
25    ceq=[C5, C6];
26 end
27 function v=StorageChar_Fsc(dsc, Escmax, Csc)
28    v=sqrt(2*(1-dsc)*Escmax/Csc);
29 end

```

Table 7: Design Solution Parameters - Arm parameters, optimal

Variable Description	Symbol	Constraint Equations
Module filter voltage ripple amplitude	ΔV_{f1}	87V
Depth of discharge	δ_{sc1}	0.12
Number of cells per storage string	n_{sc1}	264
Number of modules per arm	N_1	40
Number storage strings	n_{scs1}	1
Storage cell current	I_{sc1}	30.3A
Storage cell current ripple RMS	ΔI_{sc1}	44.7A

assumption" solution from Section 7.4.1 was too high depth of discharge assumption, which drove the number of modules up and cased an oversized design. The solution in Table 7 has energy rating of 4.87kWh, which is slightly below the requirement in Table 3. However, the solution is acceptable as the actual need was 3.47kWh for the application, the margin allocated for design tolerances will be slightly smaller.

7.6 Module Filter - Approximation Design

The parameters that determine the structure of the MMC converter leg were defined in the previous few chapters. The properties of module filter section will be defined next. The filter section as defined in Chapter 5.1 and Figure 23 can be characterized by 4 variables: two currents i_f and i_s and two voltages v_f and v_s .

The current of the module switching section i_f is determined by the state of the switching section and all other modules within the converter leg. The single module will not have much influence on it. As a result, i_f can be modeled as an ideal current source and can be seen as an input to the system as illustrated in Figure 52. The outputs of interest will then be the storage current i_s and filter output voltage v_f .

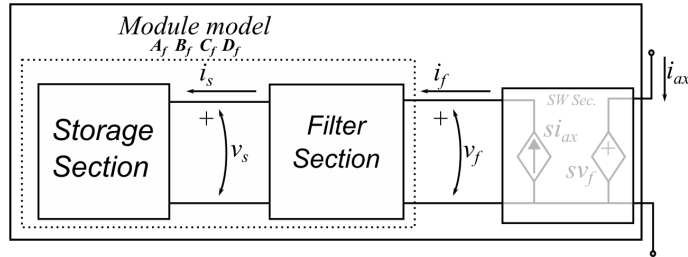


Figure 52: Module filter section inputs and outputs.

The transfer functions from i_f and v_s to i_s and v_f can be obtained from the module models given in Chapter 5.1. The transfer functions should behave as low pass filters, this is obvious from previous analysis. The attenuation of filter can be obtained from the maximum amplitude of the filter output voltage Δ_{v_f} and maximum RMS current of the storage section $\Delta_{I_{sc0}}$ determined in tea analysis above and the maximum harmonic content expected on in the input current i_f .

The harmonic content of the filter input current may be difficult to estimate exactly as

it will depend on the mode of operation and the implementation of the converter. This is indirectly evident from figures 38 and 46. As before two approaches for the filter module design will be given below. The first approach is based on engineering assumptions and the second on the model given in Chapter 5.5.

Assuming that the module filter voltage v_f is pure DC and that the sharing of power between modules is ideal, the harmonic content of the filter input current is same as the harmonic content of the arm instantaneous power.

The arm instantaneous power can be estimated based on equations (50) and (51) from Chapter 4.4. As stated in Chapter 4.4, only first four terms are significant and the last two account for the losses in the arm filter inductors due to the control effort and should be small by design. Assuming that all is symmetric, that the DC bus is constant and nominal and that the power is shared equally between modules and arms, the module power estimate can be obtained by dividing the arm power from (50) and (51) by the number of modules per arm as shown in equations (253) and (254) for upper and lower arm modules respectively.

$$p_{fax}(t) = -\frac{1}{2N}V_{DCn}(t)i_{ca}(t) - \frac{1}{4N}V_{DCn}i_a(t) + \frac{1}{N}v_{ag}(t)i_{ca}(t) + \frac{1}{2N}v_{ag}(t)i_a(t) \quad (253)$$

$$p_{fay}(t) = -\frac{1}{2N}V_{DCn}(t)i_{ca}(t) + \frac{1}{4N}V_{DCn}i_a(t) - \frac{1}{N}v_{ag}(t)i_{ca}(t) + \frac{1}{2N}v_{ag}(t)i_a(t) \quad (254)$$

Finally, the module filter current can be estimated by dividing module power by the

module filter voltage. For the purpose of estimating filter current, it can be assumed that the filter voltage is constant and that the voltage reach of the arm is equally spread by the modules. The worst case is when the voltage reach of the arm is at the minimum value (at the external DC bus value). Module voltage will then be $\frac{V_{DCn}}{N}$ and the filter current estimations become:

$$i_{fax}(t) = -\frac{1}{2}i_{ca}(t) - \frac{1}{4}i_a(t) + \frac{v_{ag}(t)}{V_{DCn}}i_{ca}(t) + \frac{1}{2}\frac{v_{ag}(t)}{V_{DCn}}i_a(t) \quad (255)$$

$$i_{fay}(t) = -\frac{1}{2}i_{ca}(t) + \frac{1}{4}i_a(t) - \frac{v_{ag}(t)}{V_{DCn}}i_{ca}(t) + \frac{1}{2}\frac{v_{ag}(t)}{V_{DCn}}i_a(t) \quad (256)$$

Considering only the DC component and fundamental of the circulating current and fundamental of the output current (controlled variables) and the AC side voltage, equations (255) and (256) can be rewritten as (257) and (258).

$$\begin{aligned} i_{fax}(t) = & -\frac{1}{2}I_{ca0} - \frac{1}{2}I_{ca1}\cos(\omega_n t - \theta_{ca1}) \\ & - \frac{1}{4}I_{a1}\cos(\omega_n t - \theta_{a1}) \\ & + \frac{V_{ag1}}{V_{DCn}}I_{ca0}\cos(\omega_n t) + \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(2\omega_n t - \theta_{ca1}) + \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(\theta_{ca1}) \\ & + \frac{V_{ag1}}{2V_{DCn}}I_{a1}\cos(2\omega_n t - \theta_{a1}) + \frac{V_{ag1}}{2V_{DCn}}I_{a1}\cos(\theta_{a1}) \end{aligned} \quad (257)$$

$$\begin{aligned}
i_{f_{ay}}(t) = & -\frac{1}{2}I_{ca0} - \frac{1}{2}I_{ca1}\cos(\omega_n t - \theta_{ca1}) \\
& + \frac{1}{4}I_{a1}\cos(\omega_n t - \theta_{a1}) \\
& - \frac{V_{ag1}}{V_{DCn}}I_{ca0}\cos(\omega_n t) - \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(2\omega_n t - \theta_{ca1}) - \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(\theta_{ca1}) \\
& + \frac{1}{2}\frac{V_{ag1}}{V_{DCn}}I_{a1}\cos(2\omega_n t - \theta_{a1}) + \frac{1}{2}\frac{V_{ag1}}{V_{DCn}}I_{a1}\cos(\theta_{a1})
\end{aligned} \tag{258}$$

I_{ca0} , I_{ca1} , I_{a1} and V_{a1} are DC component of the circulating current, amplitude of the fundamental of the circulating current, amplitude of the fundamental of the output current and amplitude of the fundamental of the output voltage respectively.

Harmonic components from (257) and (258) are given in (259) and (260).

$$\begin{aligned}
i_{f_{axh}}(t) = & -\frac{1}{2}I_{ca1}\cos(\omega_n t - \theta_{ca1}) \\
& - \frac{1}{4}I_{a1}\cos(\omega_n t - \theta_{a1}) \\
& + \frac{V_{ag1}}{V_{DCn}}I_{ca0}\cos(\omega_n t) + \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(2\omega_n t - \theta_{ca1}) \\
& + \frac{V_{ag1}}{2V_{DCn}}I_{a1}\cos(2\omega_n t - \theta_{a1})
\end{aligned} \tag{259}$$

$$\begin{aligned}
i_{f_{ayh}}(t) = & -\frac{1}{2}I_{ca1}\cos(\omega_n t - \theta_{ca1}) \\
& + \frac{1}{4}I_{a1}\cos(\omega_n t - \theta_{a1}) \\
& - \frac{V_{ag1}}{V_{DCn}}I_{ca0}\cos(\omega_n t) - \frac{V_{ag1}}{V_{DCn}}I_{ca1}\cos(2\omega_n t - \theta_{ca1}) \\
& + \frac{1}{2}\frac{V_{ag1}}{V_{DCn}}I_{a1}\cos(2\omega_n t - \theta_{a1})
\end{aligned} \tag{260}$$

In order to estimate the amplitude of the fundamental and the first harmonic of the filter input current, all factors from (259) and (260) should be expressed in terms from Table 3 as shown in (261).

$$\begin{aligned}
I_{fh_{11}} &= \frac{1}{2} I_{ca_1} = \frac{1}{2} I_{ca_{1d}} \\
I_{fh_{12}} &= \frac{1}{4} I_{a1} = \frac{1}{4} \sqrt{\frac{2}{3}} \frac{S_n}{V_n} \\
I_{fh_{13}} &= \frac{V_{ag1}}{V_{DCn}} I_{ca_0} = \frac{\sqrt{2} V_n}{\sqrt{3} V_{DCn}} \frac{P_n}{3 V_{DCn}} \\
I_{fh_{21}} &= \frac{V_{ag1}}{V_{DCn}} I_{ca_1} = \frac{\sqrt{2} V_n}{\sqrt{3} V_{DCn}} I_{ca_{1d}} \\
I_{fh_{22}} &= \frac{1}{2} \frac{V_{ag1}}{V_{DCn}} I_{a1} = \frac{1}{2} \frac{\sqrt{2} V_n}{\sqrt{3} V_{DCn}} \sqrt{\frac{2}{3}} \frac{S_n}{V_n}
\end{aligned} \tag{261}$$

The following assumptions are made before (261):

- The converter is outputting the full power from the DC to AC side.
- The storage is fully discharged.
- The converter outputs full active and reactive power making the power factor phase angle $\theta_{a1} = \arccos\left(\frac{P_n}{S_n}\right)$.
- The fundamental component in the circulating current I_{ca_1} will not exceed $I_{ca_{1d}}$. This can be achieved by limiting the output of the controller in Figure 50. Note that the fundamental of the circulating current has only d component, meaning it is in phase with the output (grid) voltage $\theta_{ca_1} = 0$.

Equations (259) and (260) can be rewritten as:

$$\begin{aligned}
i_{f_{axh}}(t) = & + (I_{fh_{13}} - I_{fh_{11}})\cos(\omega_n t) \\
& - I_{fh_{12}}\cos(\omega_n t - \theta_{a_1}) \\
& + I_{fh_{21}}\cos(2\omega_n t) \\
& + I_{fh_{22}}\cos(2\omega_n t - \theta_{a_1})
\end{aligned} \tag{262}$$

$$\begin{aligned}
i_{f_{ayh}}(t) = & - (I_{fh_{11}} + I_{fh_{13}})\cos(\omega_n t) \\
& + I_{fh_{12}}\cos(\omega_n t - \theta_{a_1}) \\
& - I_{fh_{21}}\cos(2\omega_n t) \\
& + I_{fh_{22}}\cos(2\omega_n t - \theta_{a_1})
\end{aligned} \tag{263}$$

The amplitude of each harmonic component can be found with the help of phasor representations shown in Figure 53 and Cosine theorem as shown in (264)-(266).

$$\begin{aligned}
i_{f_{axh}}(t) = & I_{f_{axh_1}}\cos(\omega_n t - \theta_{f_{axh_1}}) + I_{f_{axh_2}}\cos(2\omega_n t - \theta_{f_{axh_2}}) \\
i_{f_{ayh}}(t) = & I_{f_{ayh_1}}\cos(\omega_n t - \theta_{f_{ayh_1}}) + I_{f_{ayh_2}}\cos(2\omega_n t - \theta_{f_{ayh_2}})
\end{aligned} \tag{264}$$

$$\begin{aligned}
I_{faxh1} &= \sqrt{(I_{fh13} - I_{fh11})^2 + I_{fh12}^2 - 2(I_{fh13} + I_{fh11})I_{fh12}\cos(\theta_{a1})} \\
I_{faxh2} &= \sqrt{I_{fh21}^2 + I_{fh22}^2 - 2I_{fh21}I_{fh22}\cos(\theta_{a1})} \\
I_{fayh1} &= \sqrt{(I_{fh13} + I_{fh11})^2 + I_{fh12}^2 - 2(I_{fh13} + I_{fh11})I_{fh12}\cos(\theta_{a1})} \\
I_{fayh2} &= \sqrt{I_{fh21}^2 + I_{fh22}^2 - 2I_{fh21}I_{fh22}\cos(\pi + \theta_{a1})}
\end{aligned} \tag{265}$$

$$\begin{aligned}
\theta_{faxh1} &= \pi + \arccos\left(\frac{I_{fh12}\cos(\theta_{a1}) - (I_{fh13} - I_{fh11})}{I_{faxh1}}\right) \\
\theta_{fayh1} &= \arccos\left(\frac{I_{fh12}\cos(\theta_{a1}) - (I_{fh13} + I_{fh11})}{I_{fayh1}}\right) \\
\theta_{faxh2} &= \arccos\left(\frac{I_{fh22}\cos(\theta_{a1}) + I_{fh21}}{I_{faxh2}}\right) \\
\theta_{fayh2} &= \arccos\left(\frac{I_{fh22}\cos(\theta_{a1}) - I_{fh21}}{I_{fayh2}}\right)
\end{aligned} \tag{266}$$

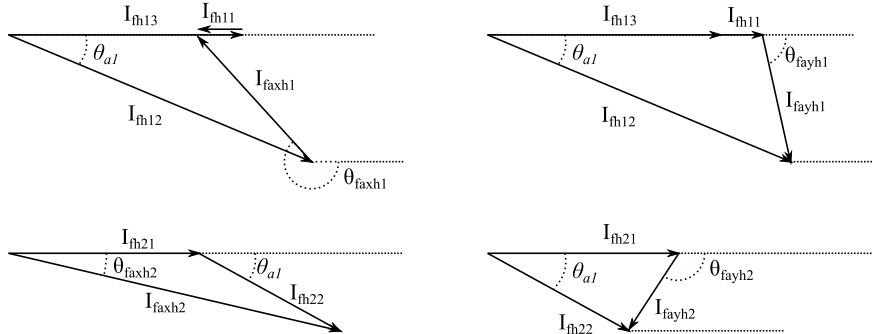


Figure 53: Phasor diagrams for fundamental and first harmonic components of the filter input current i_f .

The filter parameters can be roughly estimated using the calculated harmonics of the filter input current and the transfer function of the filter from input current to output voltage and storage current. The transfer function and exact analysis will highly depend on

the filter implementation. However, in case of simple LC filter it may be possible to perform the rough estimate of the filter parameters based on the estimated "parallel capacitance" and "series inductance". Parallel and series would roughly be with respect to the output voltage and storage current. For example for the filter structure from Figure 54, the "parallel capacitance" would be C_{f1} and "series inductance" would be L_{f1} . Once the starting rough estimates are determined the rest of the analysis can be done numerically or graphically as shown in [91].

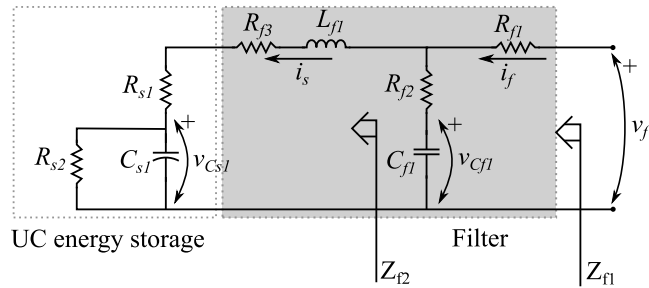


Figure 54: Module model for the Example System from Table 3 and Table 7. The filter section is shaded.

Equation (267) can be written for the output voltage. The amplitude of the output voltage is approximated by the sum of amplitudes of harmonics.

$$\Delta V_f \geq \frac{I_{f ax h_1}}{\omega_n C_{f1}} + \frac{I_{f ax h_2}}{2\omega_n C_{f1}} \quad (267)$$

Based on (267), the capacitance can be estimated as shown in (268). It is assumed here that the module contains only the parallel capacitance. The equation is also extended to both arms of the converter leg.

$$C_{f1} \geq \max \left(\frac{I_{f ax h_1}}{\omega_n \Delta_{V_f}} + \frac{I_{f ax h_2}}{\omega_n \Delta_{V_f}}, \frac{I_{f ay h_1}}{\omega_n \Delta_{V_f}} + \frac{I_{f ay h_2}}{2\omega_n \Delta_{V_f}} \right) \quad (268)$$

Next the series inductance can be added to the estimation and Equation (269) can be written for the maximum RMS of the storage current.

$$\Delta_{I_{sc}} \geq \sqrt{\left(\frac{I_{f ax h_1}}{\omega_n^2 L_{f1} C_{f1}} \right)^2 + \left(\frac{I_{f ax h_2}}{4\omega_n^2 L_{f1} C_{f1}} \right)^2} \quad (269)$$

The inductance can be estimated as shown in (270).

$$L_{f1} \geq \max \left(\sqrt{\left(\frac{I_{f ax h_1}}{\omega_n^2 \Delta_{I_{sc}} C_{f1}} \right)^2 + \left(\frac{I_{f ax h_2}}{4\omega_n^2 \Delta_{I_{sc}} C_{f1}} \right)^2}, \sqrt{\left(\frac{I_{f ay h_1}}{\omega_n^2 \Delta_{I_{sc}} C_{f1}} \right)^2 + \left(\frac{I_{f ay h_2}}{4\omega_n^2 \Delta_{I_{sc}} C_{f1}} \right)^2} \right) \quad (270)$$

7.6.1 Example System Approximation Results

For the system from Table 3 and Table 7 the filter section has the structure from module implementation #3 given in Chapter 5.1. The structure is shown again in Figure 54.

Table 8: Estimated Module Filter Parameters

Symbol	Value	Symbol	Value
R_{f1}	10 $m\Omega$	R_{f2}	10 $m\Omega$
R_{f2}	50 $m\Omega$	R_{s1}	211 $m\Omega$
R_{s2}	1 $M\Omega$	C_{s1}	2.46 F
C_{f1}	4.8 mF	L_{f1}	2.3 mH

The switching section in Figure 54 is not shown and is modeled with the switch resistance R_{f1} . R_{f2} is the equivalent series resistance of the DC module DC bus capacitors. Capacitance of the module capacitors is C_{f1} . R_{f3} models the losses in the filter inductor L_{f1} . The ultra-capacitor energy storage model is marked as "UC Energy Storage". R_{s1} models equivalent series resistance of all storage cells within the module. R_{s2} is used to model internal discharge or internal module loads and C_{s1} is the total energy storage capacitance. The values of the parameters are given in Table 8. Filter inductance and capacitance are estimated using (268) and (270).

7.7 Module Filter - Model Based Optimization Design

The module filter design can be formulated in the form of optimization and reduced order model given in (169) can be used for this purpose. The model is simple enough to execute fast. The operating conditions of the converter during the optimization will be constant for the purpose of this study. The converter will be simulated at the expected worst case for the filter currents and voltages. The expected worst case is when the converter is discharging the storage at full active and reactive current. If the simulation is set for constant operating conditions, the evaluation of the parameters needed for the cost function will be fairly straightforward.

In contrast to the engineering approach given above for a fixed LC filter structure, for the optimization approach given in this section the complexity of the filter section can be arbitrary. The optimization algorithm can be adjusted to minimize properly formulated cost function based on any number of filter component parameters.

Besides the module filter parameters, arm inductances (marked as arm impedances Z_{ax} and Z_{ay} in Figure 22) are unknowns as well. The arm inductors should have only negligible filtering effects at the lower frequencies where the module filter pass band starts. Furthermore, the averaged and simplified model simulated frequency range ends before the effects of the arm inductors become significant. As a result, the arm inductors L_{ax} and L_{ay} will not be included at the design process at this stage and they will be set to an arbitrary low value. One percent of the rated impedance of the converter can be used in this case to complete the model parameters. Lower values are also possible but may extend simulation time. The actual value of arm inductors needed to suppress the switching harmonics will be evaluated in the following chapters.

One possible cost function can be defined as shown in Equation (271). This cost function will drive the filter voltage variation and storage current RMS to match the design values given in Table 7. Note that the storage current will in this case include the DC component, for this reason the target is set to $I_{sc_{max}}$ and not ΔI_{sc} . The current RMS and voltage amplitude values will be obtained from optimization model simulation results.

$$cost = |\Delta V_f - \Delta V_{f1}| + |I_{sc} - I_{sc_{max}}| \quad (271)$$

The optimization model is described in (169) and is implemented in Simulink as shown in Figure 55. Note that the matrix calculations are used for Simulink modeling instead of the circuit modeling with Simscape components. Simulink part of the model will in this case be independent on the module implementation and parameters as the model is fully defined

by the matrices from Chapter 5.5.

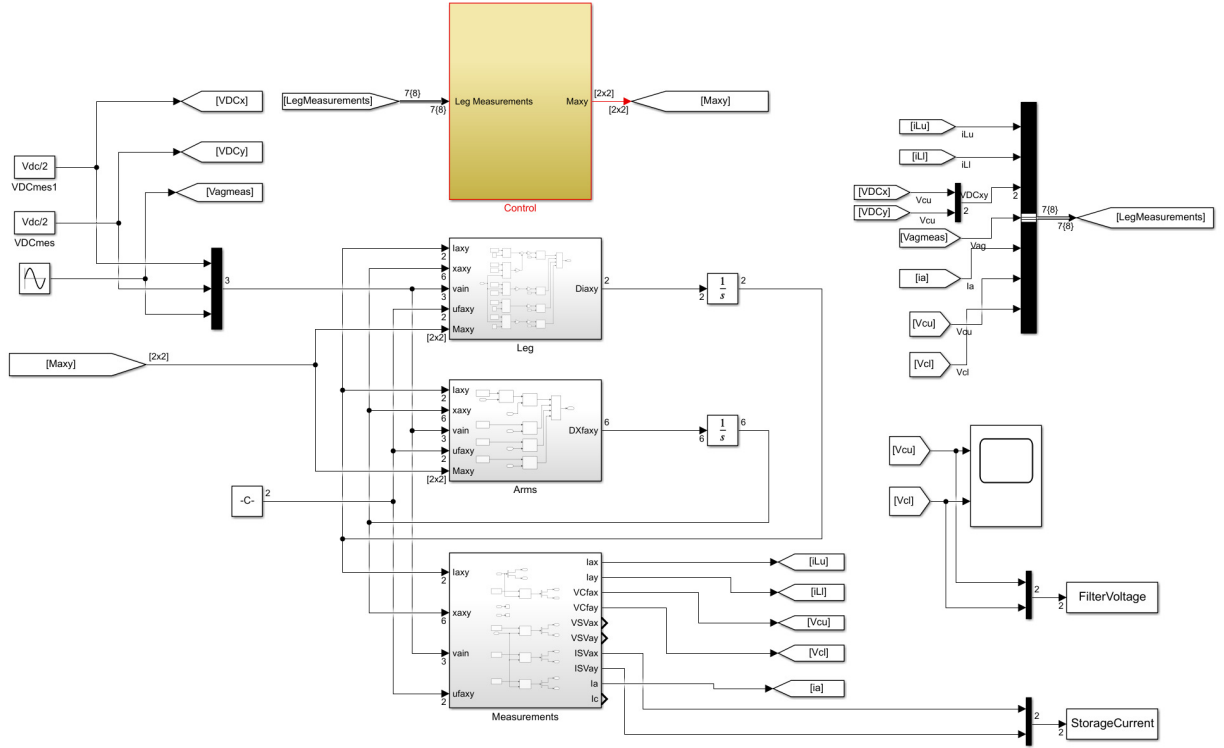


Figure 55: Reduced order model top level.

The Leg block calculates the first row from matrices given in (166) and (167). These equations actually model the converter leg as described in Chapter 5. The block structure is given in Figure 56 - (a). The Arm block calculates the second row from the same set of matrices modeling the cells of the converter arm, in this case only two representative cells. The implementation of the Arm block is given in Figure 56 - (b)

Control block structure is given in Figure 57. The block named CTRL is the closed loop current controller described in Chapter 6.5 and its structure is shown in Figure 41 and implementation in Figure 42.

The section marked as Arm balancing is explained in Chapter 6.7.2.

The section marked as DC Power control is expressing the DC current in terms of the

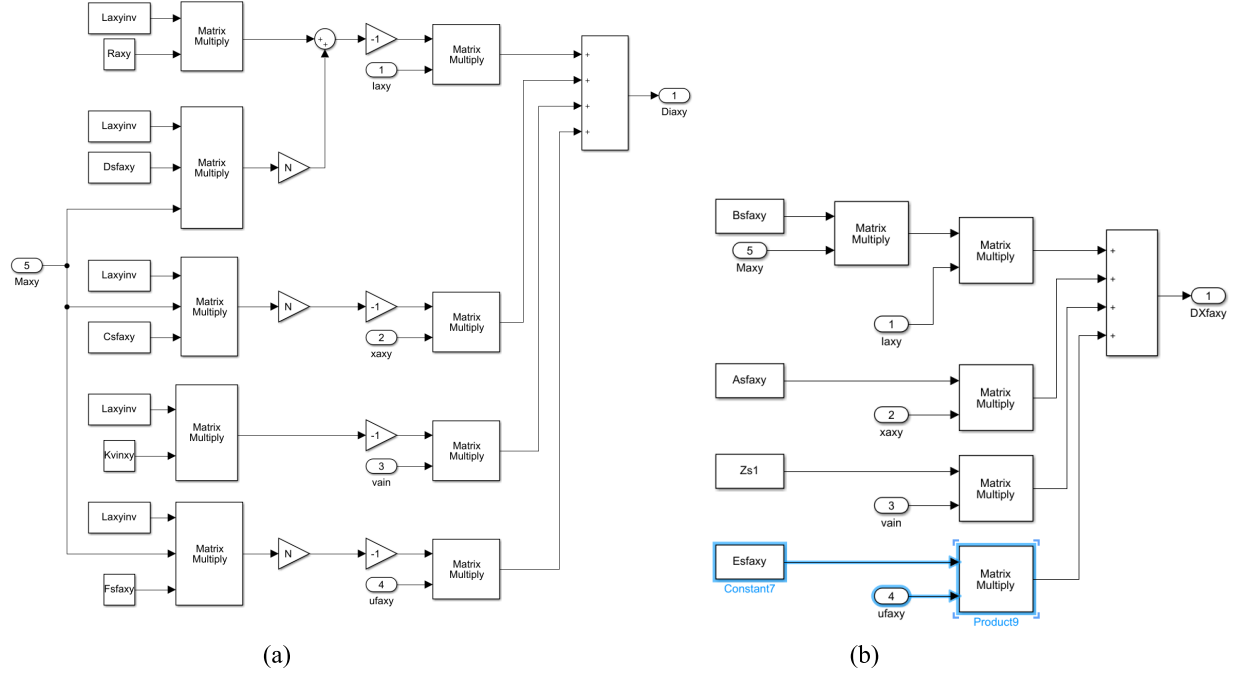


Figure 56: (a) - Structure of the Leg block. (b) - Structure of the Arm block.

rated AC current making it easier to balance the AC and DC power. For the optimization, the DC component of the circulating current reference is set to 0 forcing the storage to charge or discharge while the AC is at full active and reactive power. This should create the worst case conditions for the filter and storage RMS current. If AC component of the storage current ΔI_{sc} is figuring in the optimization cost function the reference for the AC/DC Power balance control should be the same as the active output current I_{a1d} .

Block named Measurements is just rearranging states into convenient vectors of measurements (e.g. module storage current vector, module DC bus vector...). The structure of the block measurements is given in Figure 58.

Matlab off-the-shelf optimization solver can be used to minimize the cost function. In this case "fminsearch()" is appropriate solver as the design problem is nonlinear and unconstrained. The optimization code is fairly simple and is given in Listing 2. For the example

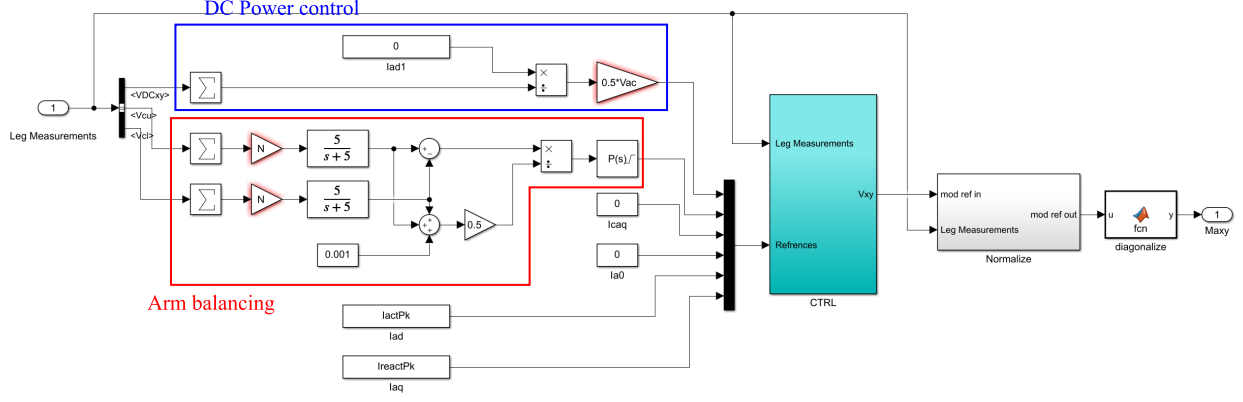


Figure 57: Control block structure.

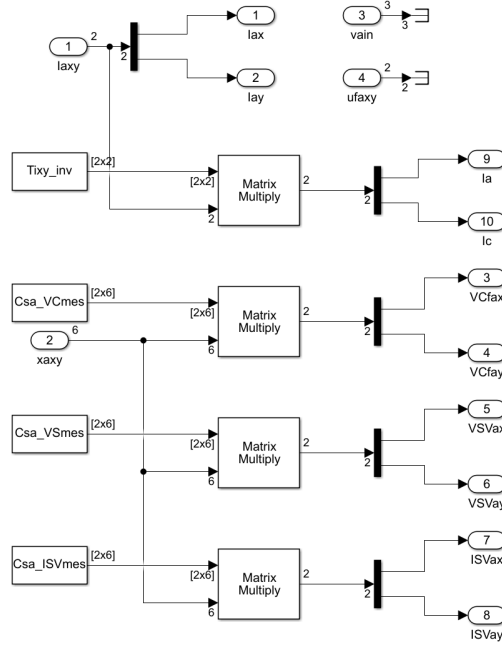


Figure 58: Measurement block structure.

system from Table 3, the model file-name is "MMCMModel" and the starting point for the optimization can be the result of the engineering approximate approach given before. The matrices and constants are pre-calculated and loaded into the work space from the Model-Properties.mat file.

Listing 2: Filter design optimization code in Matlab

```

1 options = optimset('Display','iter','PlotFcns',@optimplotfval);
2 x0=[2.3e-3, 4.8e-3];
3 x = fminsearch(@CostCalculator, x0, options)
4
5 function cost=CostCalculator(x);
6     load('ModelProperties.mat');
7     Lb=x(1);
8     Cc=x(2);
9     LegModelMat;
10    mdl='MMCMModel';
11    SimOut=sim(mdl, 'SrcWorkspace','current');
12    DIsc=max(rms(SimOut.StorageCurrent.signals.values));
13    DIsc=max(rms(SimOut.StorageCurrent.signals.values));
14    DVs=max(max(SimOut.FilterVoltage.signals.values(SimOut.FilterVoltage.time ...
15    > (SimOut.FilterVoltage.time(end)-5/60)))...
16    -min(SimOut.FilterVoltage.signals.values(SimOut.FilterVoltage.time ...
17    > (SimOut.FilterVoltage.time(end)-5/60))));
18    cost=abs(DVf-DVf1)+abs(DIsc-DIsc1)
19 end

```

7.7.1 Example System Optimization Approach Results

The optimization process converges relatively fast and drops below 1 in 12 iterations and stops after 137 iterations at the error below 0.01. Even for the error of 1, voltage and current are within the volt and ampere of the target. The resulting filter parameters obtained using the optimization code from Listing 2 for the system from Table 3 are given in Table 9.

Table 9: Estimated Module Filter Parameters - Model Based Design

Symbol	Value	Symbol	Value
R_{f1}	10 $m\Omega$	R_{f2}	10 $m\Omega$
R_{f2}	50 $m\Omega$	R_{s1}	211 $m\Omega$
R_{s2}	1 $M\Omega$	C_{s1}	2.46 F
C_{f1}	4.5 mF	L_{f1}	3.4 mH

Since the optimization is based on a single operating point, the same model used for the optimization process can be used to check the behavior of the module under different operating conditions. Instead of constant, the references are modified to cycle through all of the expected combinations. For the current analysis, the set of references are cycled through the conditions shown in Figure 59.

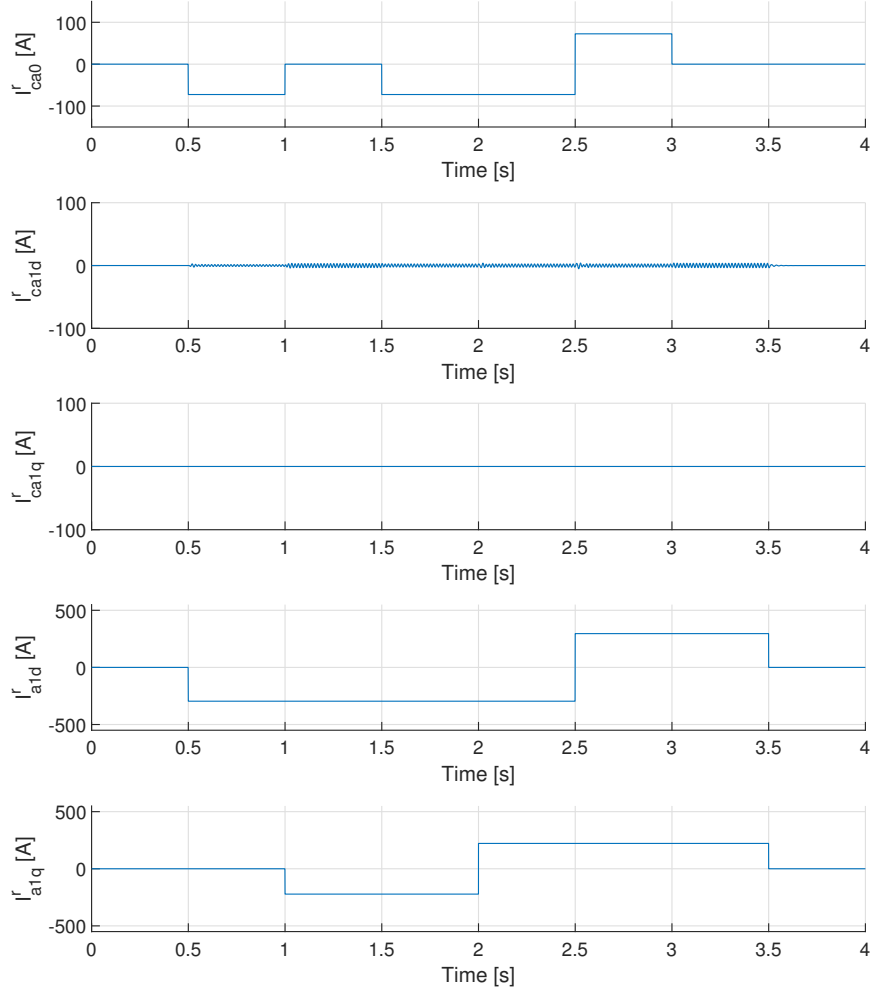


Figure 59: Simplified model simulation results - Control references.

The references from Figure 59 are forwarded to the current controller block marked as CTRL in Figure 56 and described in detail in Chapter 6.5. The active current is sequenced from full consumption to full delivery as shown in I^r_{a1d} plot in Figure 59. The reactive power has similar sequence from full reactive consumption to full delivery as shown in I^r_{a1q} plot in Figure 59. The fundamental of the circulating current is used for arm balancing efforts and has an outer loop control described in Chapter 6.7.2 added to the model. This outer

loop control causes the oscillations observable in I_{ca1d}^r plot in Figure 59 due to the imperfect single pole filters used for this implementation.

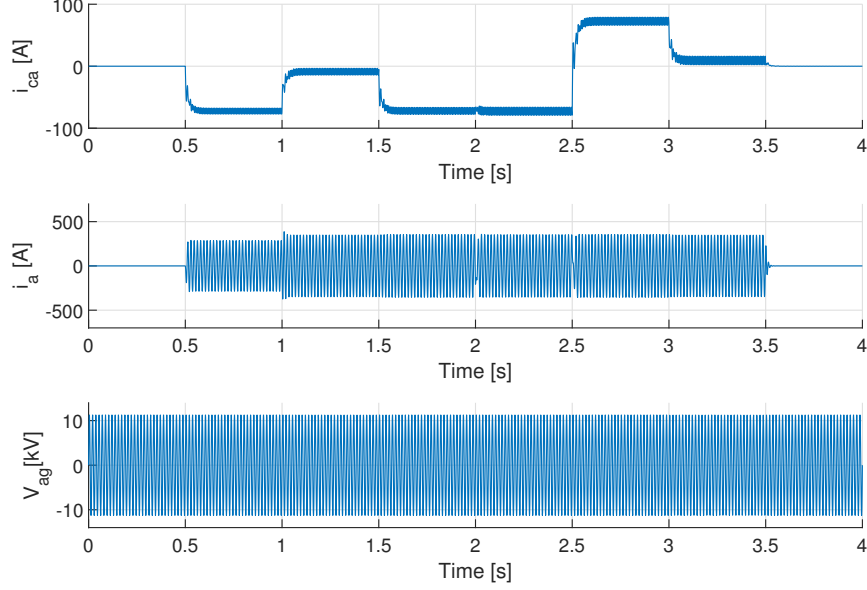


Figure 60: Simplified model simulation results - Output currents and grid voltage.

Figure 60 shows circulating current, output current and grid voltage. The circulating current i_{ca} has DC component following the reference and small AC component superimposed as a result of arm balancing controller. The output current i_a follows the reference as well. The grid voltage v_{ag} is given for reference only and is modeled as shown in Figure 22.

Figure 61 shows the voltages for the filter capacitors (V_{Cf1ax} and V_{Cf1ay}) and storage system model voltage (V_{sax} and V_{say}). The converter cycles through all states, charge, storage maintaining state and discharge. As mentioned before the power balance control that maintains the storage at steady state is open loop and does not take into account the losses in the converter, which explains the slope during the period $t=[1.5s, 3s]$ when the balance should be maintained between ac and dc side of the converter. The maximum filter

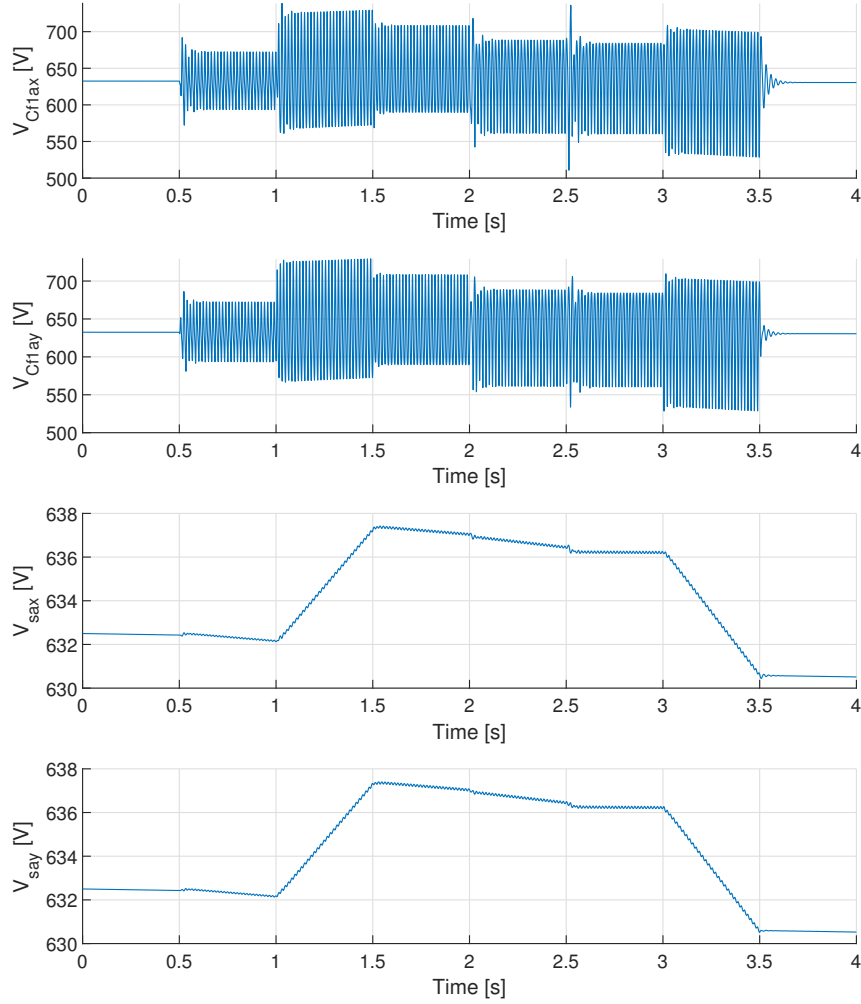


Figure 61: Voltage of the module filter section for upper and lower arm and module module storage systems of upper and lower arm.

output voltage swing is about 85V which meets the 87V limit.

Figure 62 shows the RMS measurements and actual waveforms of the storage current. The Current RMS is about 53A max which is within one ampere of 54A limit. If needed, the process can be repeated with adjusted limits to meet the maximums. For the purpose of this study the value will be left as is which will make it possible to evaluate the design error

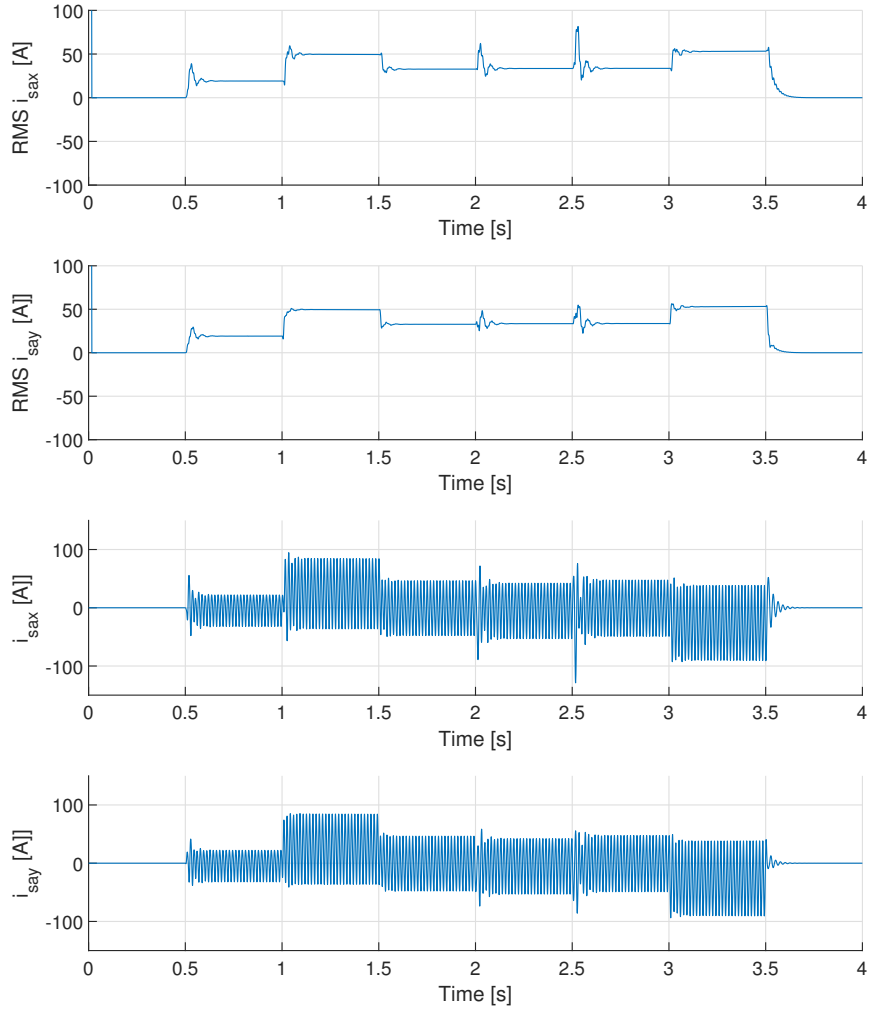


Figure 62: RMS currents for the storage system current for upper and lower arm and waveforms of the storage system currents for upper and lower arms.

once the switching model has been fully defined and evaluated.

7.8 Arm Inductors

The final part in the design procedure is the design of the arm inductors. The main purpose of the arm inductors is to limit the switching harmonics and facilitate the DC current control.

One approximate way to estimate the arm inductors is presented in [91]. However, the case presented in [91] assumes that the voltage reach of the arm is exactly equal to the DC bus ($vV_{f_{max}} = V_{DCn}/N$), which does not have to be the case.

It will be assumed that the grid inductance is set by the grid connection and that no inductors are added. The converter can be designed for the worst case which can be defined by the grid connection short circuit limit the converter designed for.

In general, there are two considerations for the ripple in the inductor current. One is the THD of the output current and the other is ripple and current harmonics in the circulating current. The current ripple is a good indicator for the THD and harmonics in signals with dominant sinusoidal fundamental characteristic for the converters and motor drives.

The direct mathematical link between the current ripple and converter parameters is not straightforward nor is the link between ripple and THD or harmonics. As a result for accurate analysis, it may be easier to use switching model and harmonic analysis tools to estimate and tune the values than to attempt to derive expression for the inductance values analytically.

Current section will just estimate for the arm inductances based on the ripple amplitude. The values obtained from the analysis in this section can be used as the starting point and the switching model derived in Chapter 5.3 can be used to verify the acceptability of the behavior and perform fine tuning of the inductance.

The Arm inductance is tightly coupled with switching frequency. Due to the issues outlined in Chapter 4.5 for low switching frequencies, it will be assumed that the (module or device) switching frequency is at or above ten times the current fundamental frequency $f_s \geq 10 \times f_{n_{max}}$. In contrast to the f_n meaning minimum, the effective switching frequency

seen by the arm and grid inductances will be the product of the number of modules per arm N and the switching frequency $f_{sw} = N \times f_s$.

7.8.1 Ripple Based Approximation Limits

The arm inductance can be estimated based on the output ripple current using the following reasoning:

- Assume that the arms string have enough capacitance to act as ideal voltage sources.
- Assume that each arm contributes equally to the output current and ripple.
- Effective switching frequency is:

$$f_{sw} = N f_s \quad (272)$$

- The amplitude of the ripple Δi_{ax} for the worst case when the converter output alternates around grid voltage as illustrated in Figure (63) is linked with the module voltage and effective switching period as shown in (273).

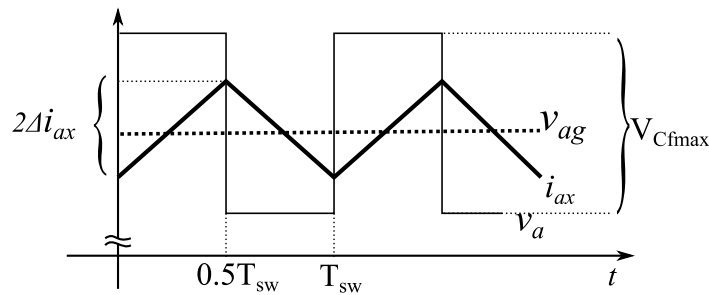


Figure 63: Arm current ripple illustration.

Note that the worst case for the ripple is when the module voltage is at maximum value.

$$2\Delta i_{ax} \approx \frac{v_{ag} - v_a}{L_{ax} + L_{ag}} \frac{T_{sw}}{2} = \frac{V_{fmax}}{2(L_{ax} + L_{ag})} \frac{T_{sw}}{2} = \frac{V_{fmax}}{4(L_{ax} + L_{ag})Nf_s} \quad (273)$$

- To keep the output current ripple below predefined value of Δi_{ax} the ripple of lower and upper arm currents will have to be below $\Delta i_{ax} = \Delta i_{ay} = \frac{1}{2}\Delta i_a$. The arm inductance will have to satisfy the condition given in (274).

$$L_{axg} = L_{ayg} \geq \frac{V_{fmax}}{4\Delta i_a N f_s} - L_{ag} \quad (274)$$

Equation (274) gives the condition for the output current ripple. Since the controller and the overall design of the converter requires the full control of output and circulating current the ripple in the circulating current should be evaluated as well. The amplitude of the circulating current ripple can be evaluated as follows:

- In contrast to the output current, which is controlled by the difference in the arm voltages as illustrated in Equation (38) the circulating current is controlled by the sum of the arm voltages as illustrated in (39).
- The voltage across arm both inductors in the worst case is then at least two module voltages.
- The worst case is again when the duty of the switching is 50%.
- Following the assumptions above, the ripple in the circulating current should satisfy Equation (275).

$$2\Delta i_{ca} \approx \frac{V_{DC} - (v_{ax} + v_{ay})}{L_{ax} + L_{ag}} \frac{T_{sw}}{2} = \frac{V_{fmax}}{2L_{ax}} \frac{T_{sw}}{2} = \frac{V_{fmax}}{4L_{ax}L_{ag}Nf_s} \quad (275)$$

- The arm inductance then has to satisfy Equation (276).

$$L_{ax_{DC}} = L_{ay_{DC}} \geq \frac{V_{fmax}}{8\Delta i_{ca}Nf_s} \quad (276)$$

Finally, the arm inductance will be larger of the two requirements: the requirement for the output current ripple given in (274) and the requirement for the maximum DC current ripple given in (276). This is expressed in Equation (277).

$$L_{ax} = L_{ay} \geq \max\{L_{ax_{DC}}, L_{ay_{DC}}, L_{ax_g}, L_{ay_g}\} \quad (277)$$

7.8.2 Example System Arm Inductance

The limits for the ripple current can be determined based on the rated DC component of the circulating and the amplitude of the output current. The parameters are calculated for the example system from Table 3 and Table 7 and are given in Table 10 with the estimated value of the arm inductance.

Note that the limiting factor for the system from Table 3 and Table 7 is the DC current ripple. The conditions are in general harsher for the DC current ripple as the calculation is based on voltage reach of the arm and not the external DC bus. Furthermore, for the same rated power of the converter DC side current is lower.

If the current ripple is expressed as a percentage of the amplitude of the AC current and

Table 10: Estimated arm inductance and related parameters.

Symbol	Value	Comment
R_r	30Ω	Rated impedance of the converter
L_{ag}	$80\mu H$	Grid tie inductance (about 0.1%)
R_{ag}	$30m\Omega$	Grid tie resistance (about 0.1%)
I_r	$372A$	Rated AC current amplitude of the converter leg
I_{ca0r}	$52A$	Rated DC current amplitude of the converter leg
Δi_a	$18.5A$	Output current ripple (5% of the rated amplitude)
Δi_{ca0}	$5.2A$	DC current ripple (10% of the rated amplitude)
L_{axDC}/L_{ayDC}	$800\mu H$	Arm inductance (DC current limit)
L_{axg}/L_{ayg}	$370\mu H$	Arm inductance, actual (AC current limit)
L_{ax}/L_{ay}	$800\mu H$	Arm inductance (turns out to be about 1%)
R_{ax}/R_{ay}	$300m\Omega$	Arm inductance resistance (about 1%)

DC current and if the percentage is the same, the operation and control of the converter will be more sensitive to the output current ripple. In the worst case the arm current ripple can be estimated using the link between arm currents and output and circulating currents given in Equations (26) and (27). If the output current is higher so will be its ripple content in the arm currents.

8 Simulation Results and Related Considerations

The previous sections completely defines the structure of one leg of the MMC converter. As the leg is fully controlled it can be used in larger poly-phase structure as a module, provided that the proper DC and AC side sources are present, thus maintaining the modular spirit of the entire converter design.

Simulation results obtained from the models derived in Chapter 5 will be presented in this section. The controller described in Chapter 6 will be used to control the converter currents. The structure of the converter is given Chapter 7 and the parameters of the converter are

listed in Tables 3, 5, 7, 9 and 10.

8.1 Arm Balance Verification and Tuning

As the module parameters are fully defined now, the simplified model used for the optimization process for the filter design in Chapter can be used to verify and tune that the arm balancing algorithm given in Chapter 6.7.2 operates. The block diagram of the arm balance controller from Figure 50 has the controller gain K_{ab} and saturation limits that should be determined based on the desired behavior. It can be assumed that the time constant for balancing between arms can be in the range of several seconds. Also, the limit for the d component of the fundamental of the circulating current can be assumed to be 50% or the rated current of the converter. The higher the limit is the faster the imbalance can be corrected. Constant K_{ab} gain is set to 5000 to keep the voltage tightly balanced. Simulation results for the upper and lower arm module storage voltages and filter are shown in Figure 64.

The simulation in Figure 64 starts with 7% imbalance and 100% output current while maintaining power balance. At $t=1s$ the balancing algorithm is activated. As can be seen the storage systems of both arms are balanced after approximately 7s. Note that the balancing algorithm should be on-line at all times. If that is the case the converter arm will be kept in balance at all times and large imbalances as shown here should not be expected except maybe during the converter start-up.

Currents of the module storage system are shown in Figure 65. It is evident from the current waveforms that the lower arm is discharging and upper is charging during the balancing sequence.

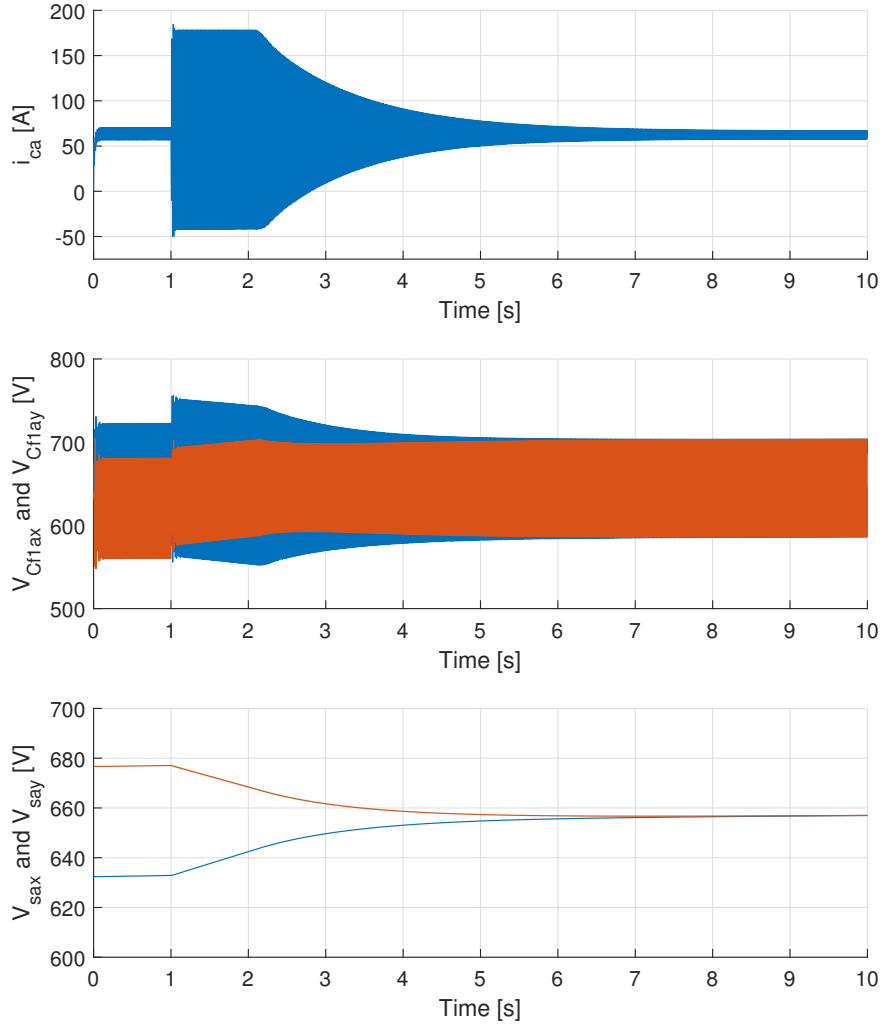


Figure 64: From top to bottom: circulating current and upper and lower arm module filter voltages and upper and lower arm storage voltages. AC/DC power balance is maintained.

Figures 66 and 67 show the balancing transients while the AC output is at full active and reactive power and charging the energy storage. In other words, the power balance is not maintained between AC and DC side.

If the storage is being charged/discharged at full power and the output is at full active and reactive power during the balancing event the storage RMS current can be significantly

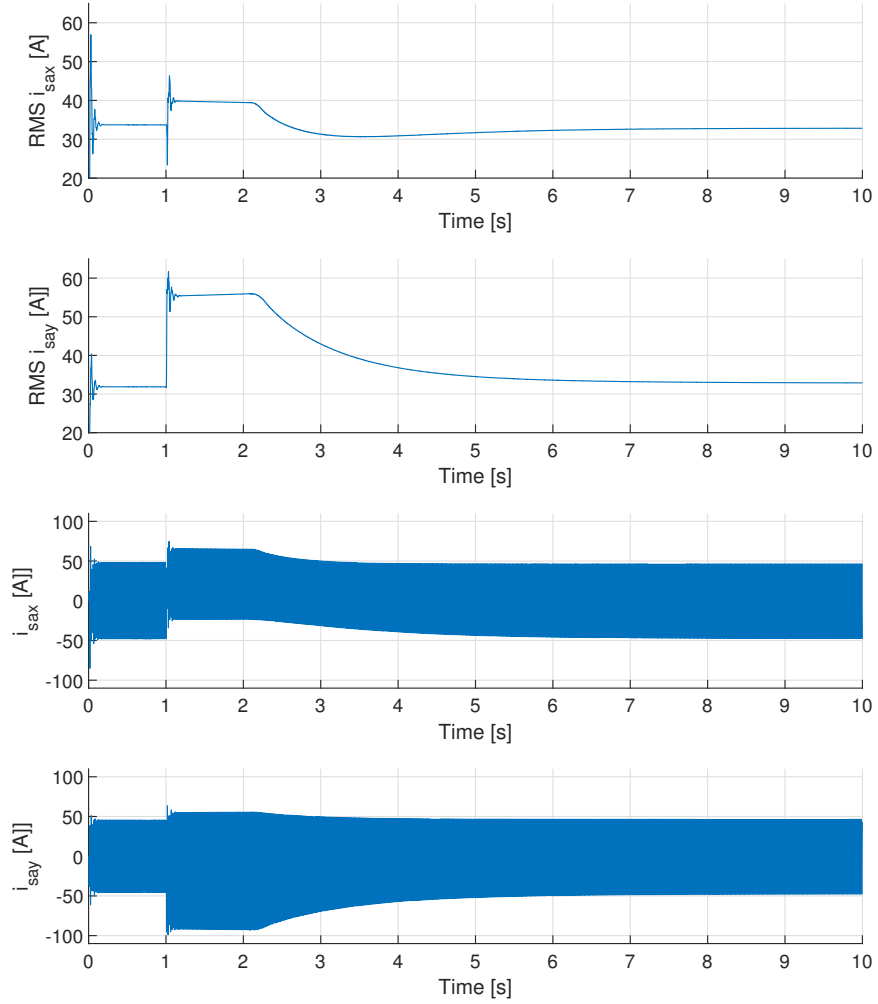


Figure 65: Storage current RMS are shown in upper two plots and waveforms on the lower two plots. AC/DC power balance is maintained.

exceeded as shown in Figure 67.

If it is expected that the converter will operate with large imbalances and intermittent balancing, modules should be designed to include the balancing currents in the storage and filter currents/voltages budget. If the balancing algorithm is normally on-line, large imbalances can be encountered only during irregularities. In this case, during balancing

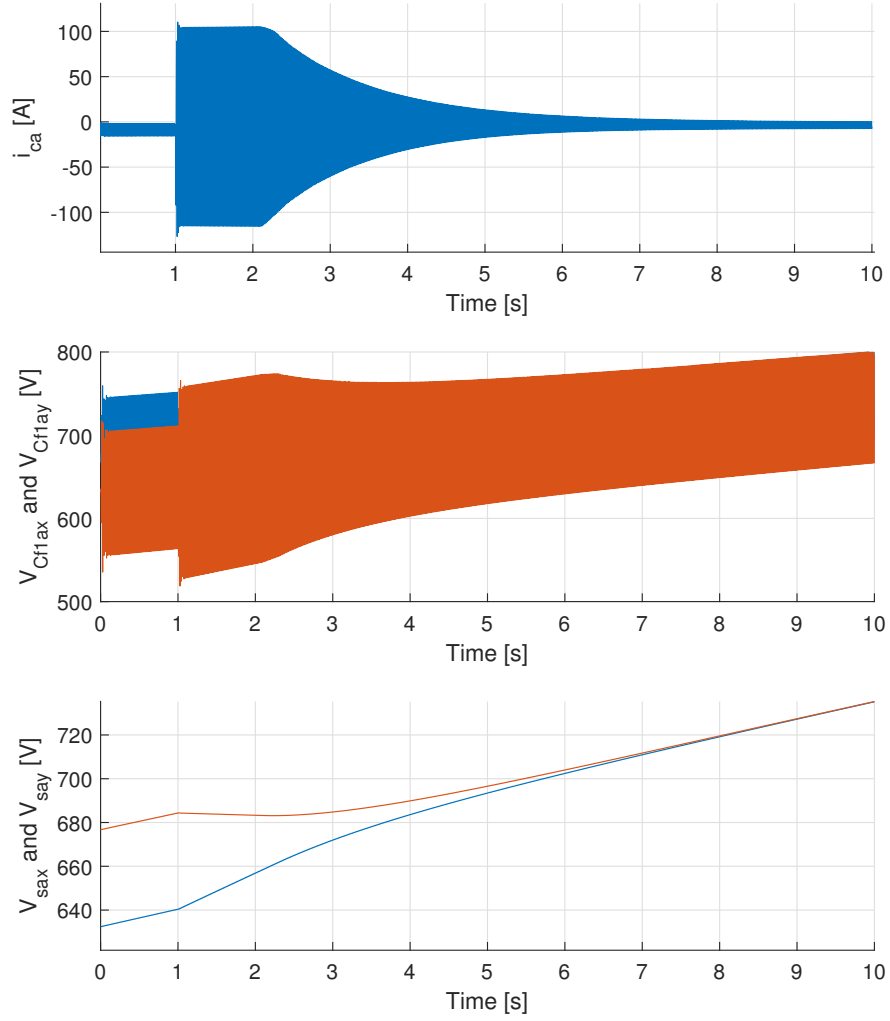


Figure 66: From top to bottom: circulating current and upper and lower arm module filter voltages and upper and lower arm storage voltages. The power balance is not maintained. Storage is being charged.

transients the power balance should always be maintained (storage should not be charged or discharged) or reactive current should be limited to keep the currents and voltages below the design limits.

The balancing current closes through the external DC bus and is AC at the fundamental frequency of the output. Consequently, the components in the external DC bus should be

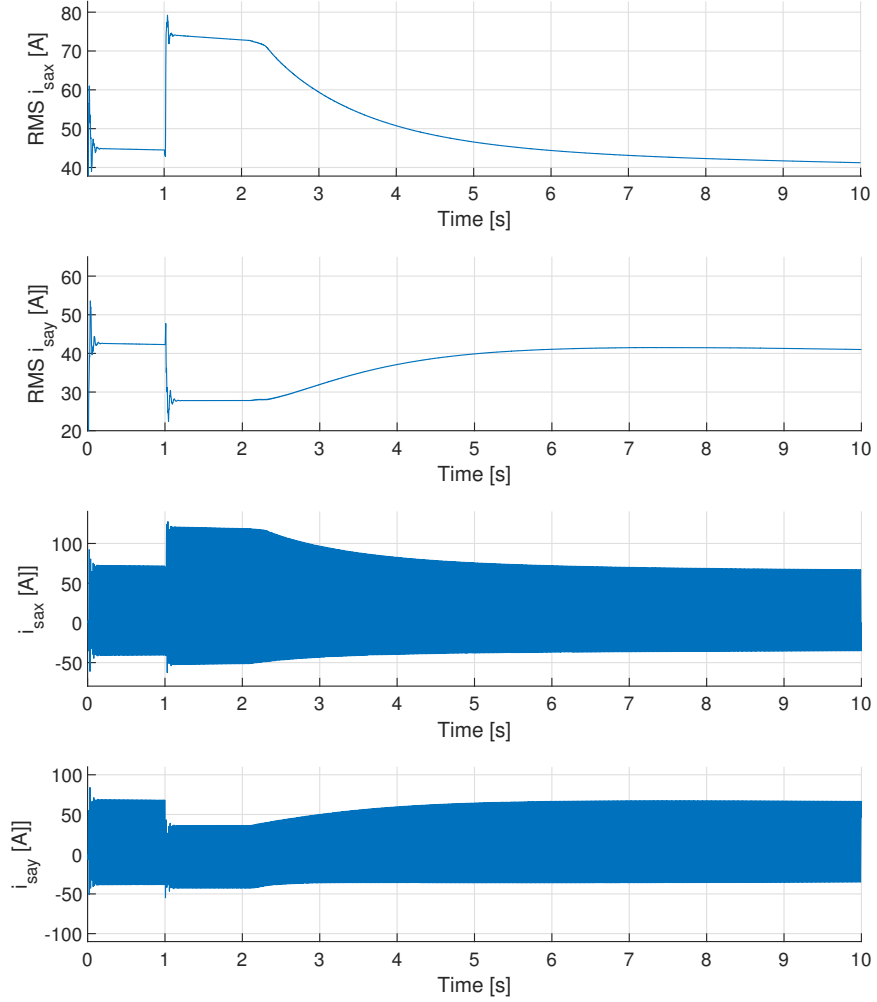


Figure 67: Storage current RMS are shown in upper two plots and waveforms on the lower two plots. The power balance is not maintained. Storage is being charged.

sized with the balancing currents in mind.

8.2 Module Balance Verification and Tuning

Balancing algorithm is derived in Chapter 6.7.1 and shown in Figure 49. Averaged model derived in Chapter 5.4 and given in Equation (149) is convenient for investigation and tuning

of the module balancing algorithm. The model is fully symmetric meaning that the imbalances will not appear on their own and will have to be introduced artificially. The balancing algorithm will not be influenced by the switching effects if the averaged model is used and will be easy to tune. Another advantage of the averaged model is that it is executing faster than the switching model.

The main difficulty with the module balancing algorithm tuning results from considerable amount of storage within each module. Furthermore, a relatively small energy storage voltage difference will translate into relative high amount of energy imbalance due to the quadratic dependence between energy and voltage for the ultra-capacitors used in the example system. As a result, the storage will be reduced to only 1% of the design value to investigate the behavior of the balancing algorithm and its influence in the converter. This will reduce the simulation time and exaggerate the effects of the balancing algorithm.

The converter model is implemented in Simulink using matrix multiplications and has the similar structure as the model from Chapter 7.7 shown in figures 55, 56, 57 and 58. The only differences are in the control block, the size of the vectors and the additional multiplication of the modulation index matrix with constant S_a matrix as shown in Equation (149).

The Simulink implementation of the control block is shown in Figure 68. The control is only slightly different. For the large signal averaged model, the control outputs $2N$ individual module modulation indexes instead of just 2 averaged ones.

The control block structure in Figure 68 is different from the control block structure given previously in Figure 57 only in the implementation of the Balancing and Normalization block, which was previously normalization block only. The structure of Balancing and Normalization block is described in Chapter 6.7.1 and shown in Figure 49. The actual

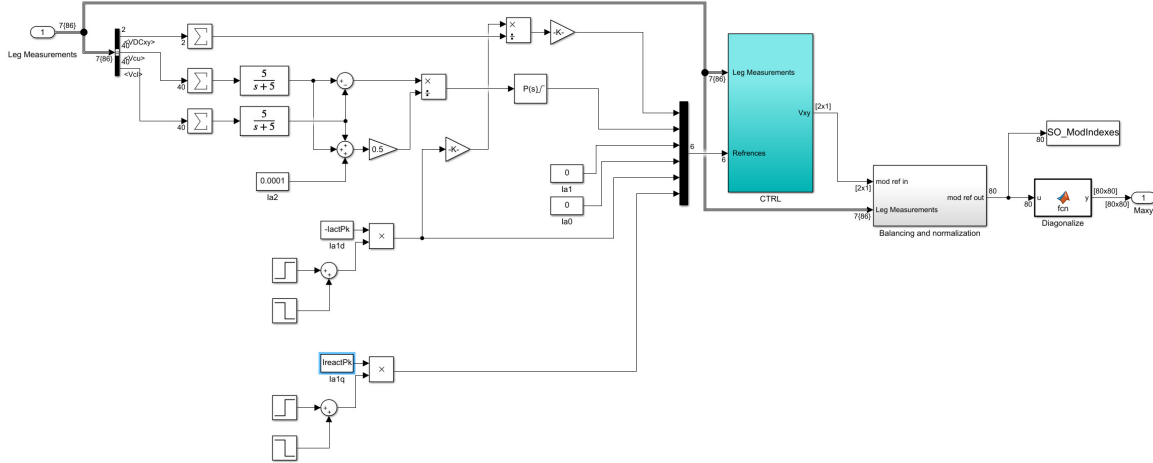


Figure 68: Control section for the averaged converter model (shaded Control block structure from Figure 68).

Simulink implementation of the Balancing and normalization block is shown in Figure 69.

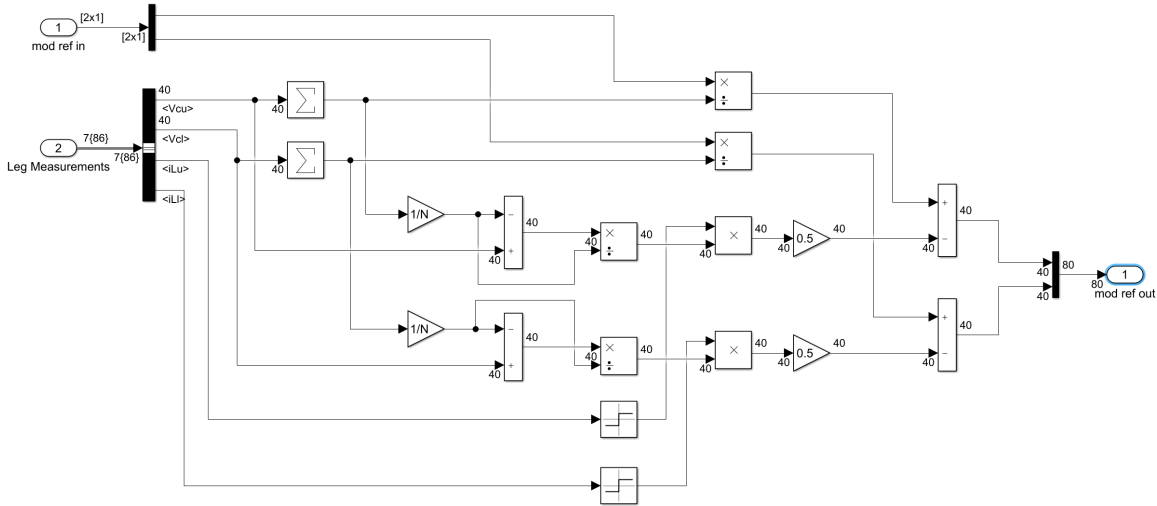


Figure 69: Balancing and normalization block structure implementation in Simulink.

The module balancing controller shown in Figure 49 has balancing coefficient K_{bal} that needs to be determined. The model that has storage system reduced to 1% of the design value for the example system with all other parameters the same. The system was simulated for the balancing algorithm gain set to $K_{bal} = 0.5$. The storage systems of the modules are initialized with imbalances that sums up to about one average voltage of the module across

all modules of an arm. This is considered to be the 100% imbalance.

The model is set to start delivering full reactive power and draw full active power at $t=0.05s$. The output current is set to zero at $t=1.5s$. The DC side is tuned to maintain the power balance between AC and DC side. The effects of the open loop inaccuracy due to the losses within the converter are more exaggerated for reduced storage capability. As a result, the DC side delivery was manually tuned until approximate power balance is achieved. This revealed that the approximate efficiency with the modeled losses is about 93%. Balancing algorithm is activated at $t=0.2s$.

Figure 70 shows output and circulating currents. The output current slightly jumps when the balancing is activated. This transient effect is due to the relatively large imbalance and step initialization of the balancing algorithm and should not be present if the balancing is constantly on-line.

The measurements for the module filter voltages are given in Figure 71. The module filter voltage is measured at the capacitor C_{f1} shown in Figure 67. At the beginning, the imbalance is clearly seen. At the end of the simulation interval, when the output current is zero the voltages of all modules are clearly balanced.

Figure 72 shows the voltage of the storage strings within the module. The ripple is exaggerated as the storage capacity is reduced to only 1%. The results show that the storage system is well balanced at the end of the simulation run compared with the clear imbalance that can be seen in the beginning.

In order to evaluate the time constant and overall system behavior, it is important to quantize the imbalance in some way. One way to approach the imbalance measurement is to treat the total imbalance as the sum of absolute deviations from the module average value as

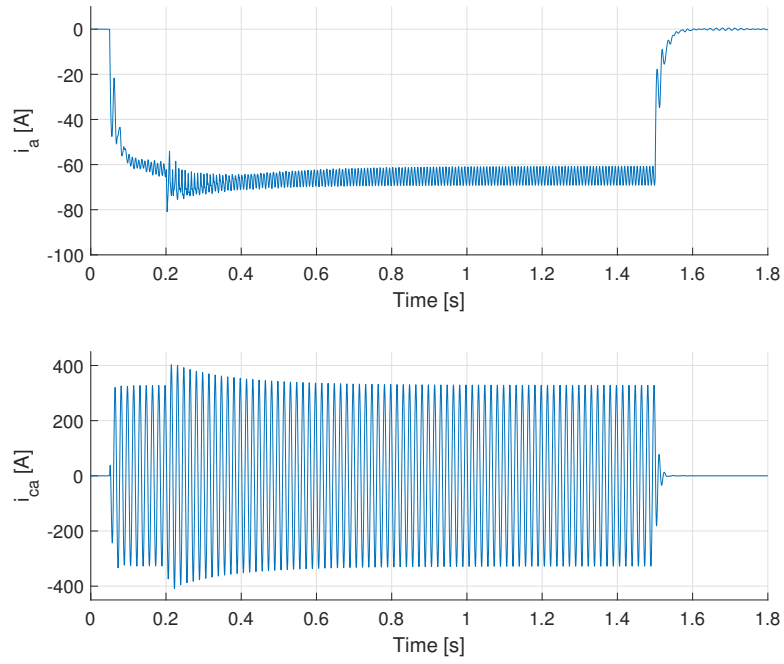


Figure 70: Circulating current during the module balancing sequence in the upper plot and the output current in the lower plot.

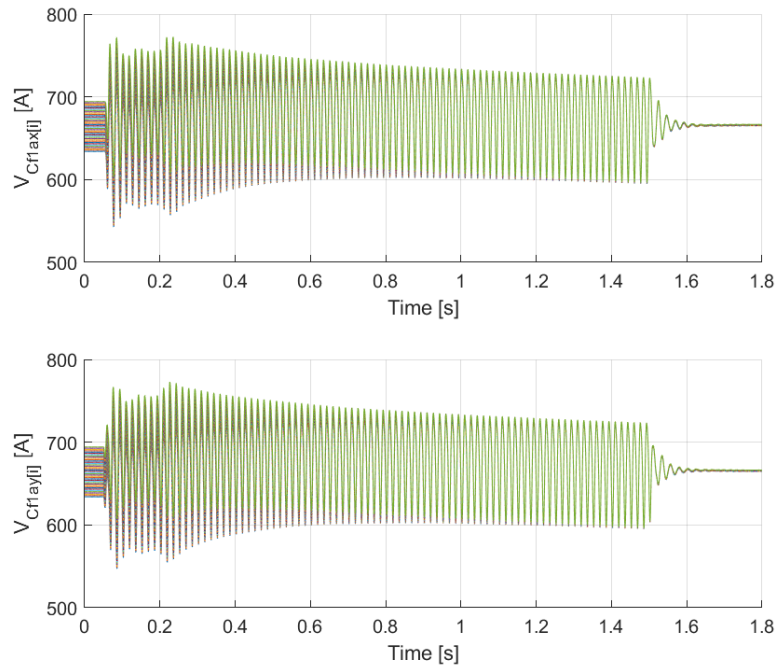


Figure 71: Module filter output voltage during the balancing simulation sequence.

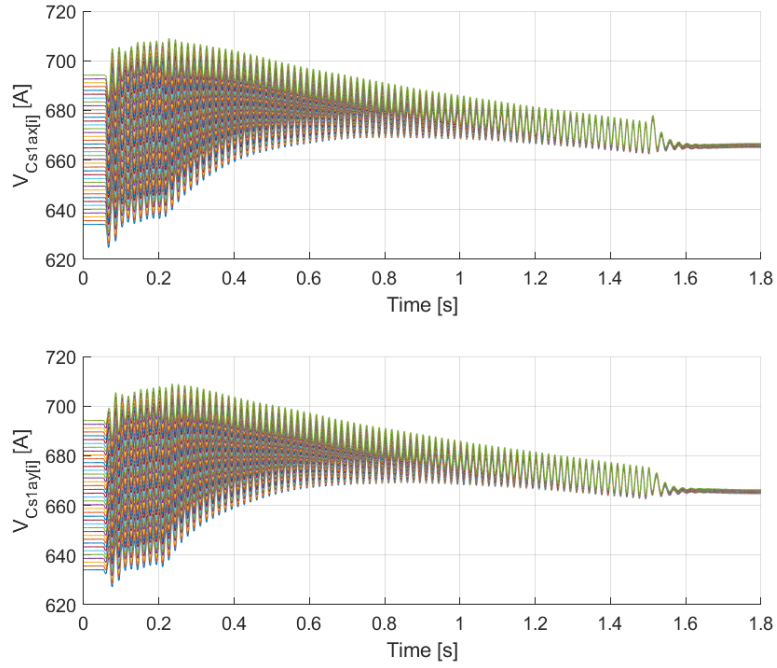


Figure 72: Circulating current during the module balancing sequence in the upper plot and the output current in the lower plot.

shown in Equation (278). Figure 73 shows simulation results during the balancing sequence for the converter leg imbalance measurement implemented in this way .

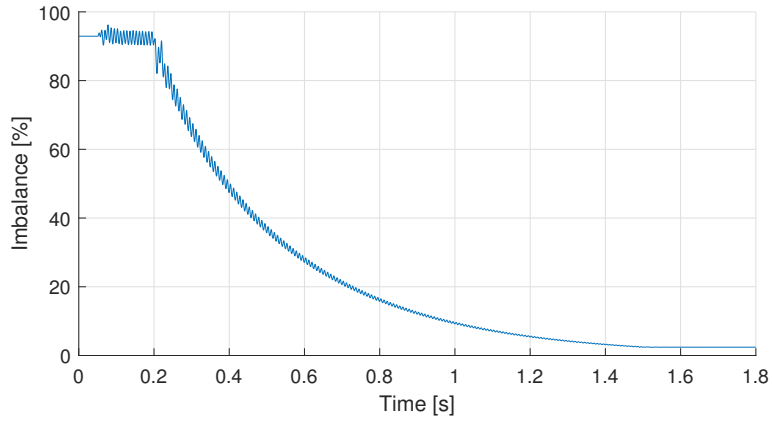


Figure 73: Imbalance measurements as defined in (278) during the balancing sequence simulation run.

$$\begin{aligned}
imbalance = \frac{1}{2} \left(\frac{\sum_{i=1}^N (V_{C_{f1ax}[i]} - \overline{V_{C_{f1ax}}})}{\overline{V_{C_{f1ax}}}} + \frac{\sum_{i=1}^N (V_{C_{f1ay}[i]} - \overline{V_{C_{f1ay}}})}{\overline{V_{C_{f1ay}}}} \right) \\
\overline{V_{C_{f1ax}}} = \frac{1}{N} \sum_{i=1}^N V_{C_{f1ax}[i]} \quad \overline{V_{C_{f1ay}}} = \frac{1}{N} \sum_{i=1}^N V_{C_{f1ay}[i]}
\end{aligned} \tag{278}$$

8.3 Switching Model Simulation Results

All parameters of the converter are determined now and the controller is tuned at this point. However, only the averaged and simplified models have been used to test its behavior. The next step is to verify the behavior of the converter with the switching model. The model given in Chapter 5.3 and Equation (106) will be used for this purpose. As mentioned in the previous chapters, the goal for the switching model simulations is to determine if the THD is met for the output current and to evaluate if the converter behaves as expected.

The model is implemented in Simulink in the same way the models in previous chapters have been implemented, using the matrices from Chapter 5.3. This way the number of modules and converter parameters can be varied without the change of Simulink the model structure. The structure of the model in Simulink is very similar to the structure of the models used in Chapter 7.7, shown in Figure 68 and is given in Figure (74).

The arm and leg block structures are very similar to the structure of Arms and Leg block implementations for averaged and simplified models and are given in Figure 75. Measurement block rearranges the states in the form more suitable for feedback and plots and will not be elaborated in more detail as it does not contain any note worthy calculations.

"Gate to state" block converts gating signals from the control block modulator into switching states matrix S_{axy} suitable for the model described in Chapter 5.3. As mentioned

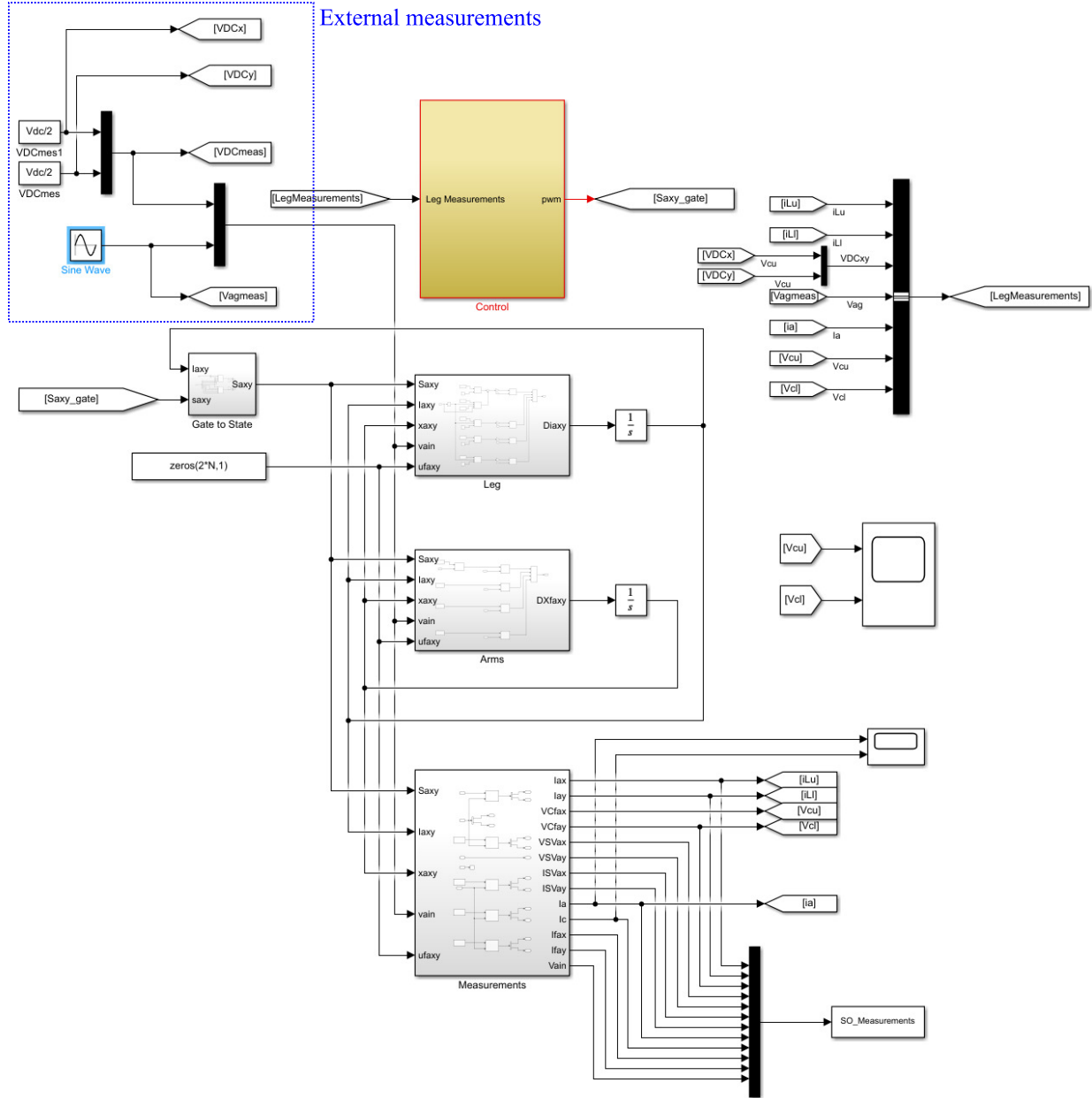


Figure 74: Switching model structure.

earlier in Chapter 5.2 and Chapter 4 the switching states depend on the current direction and the gating signals for semiconductors in the switching section of the module due to the presence of anti-parallel diodes. The block is implemented as a lookup table. The inputs for the lookup table are the switch gates and arm current sign and outputs are the switching states. The lookup table rules are given in Table 11 for the half bridge switching section

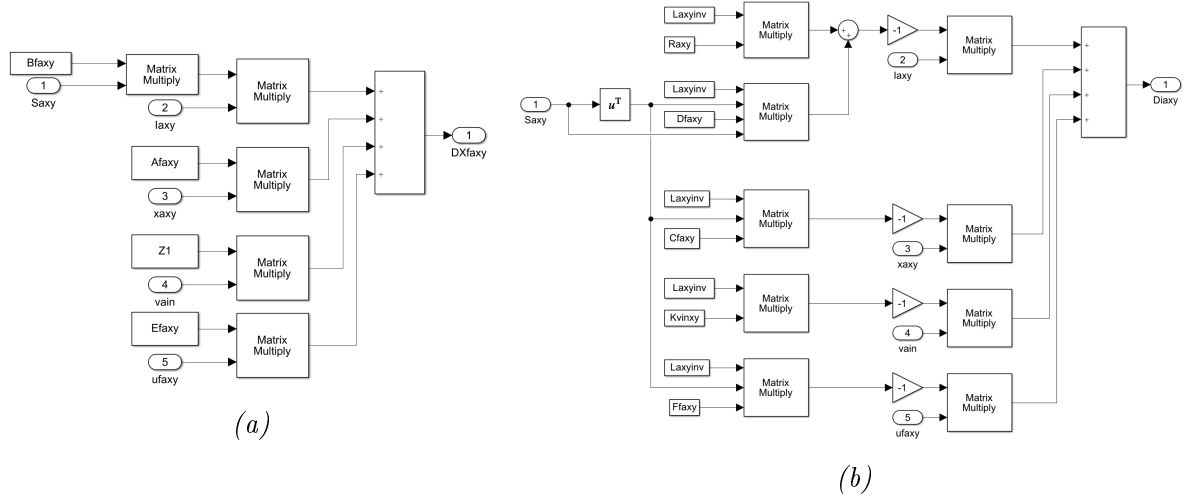


Figure 75: (a) - Arms block structure and (b) - Leg block structure for switching model.

used for this model and illustrated in Figure 19.

Table 11: Gates to switching states conversion table.

$S_{Q2[i]}$	$S_{Q1[i]}$	Arm Current > 0	$S_{[i]}$
0	0	0	0
0	0	1	1
0	1	1	0
0	1	1	0
1	0	0	1
1	0	0	1
1	1	0	illegal
1	1	1	illegal

The switching model control block also has the structure very similar to the the control block used for the averaged and simplified models. The difference is that the outputs are now module switching section gate states instead of the modulation indexes. The structure of the Simulink implementation of the switching model control block is given in Figure 76.

The CTRL block is the closed loop current controller described in Chapter 6.5 and its structure is shown in Figure 41 and implementation in Figure 42. The controller is re-tuned to the converter parameters determined in the previous chapters.

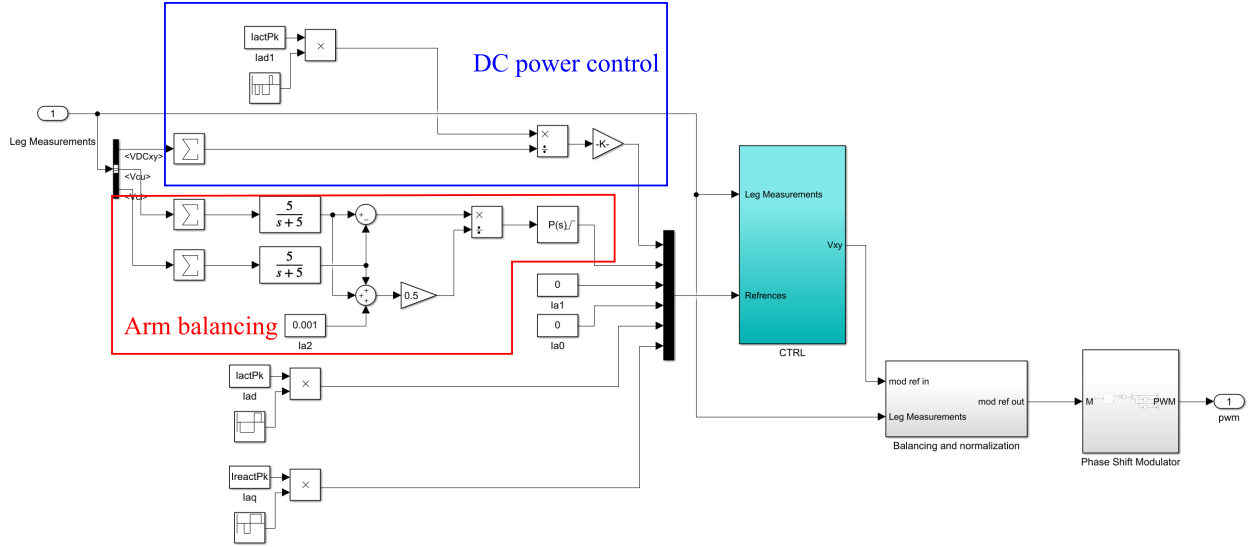


Figure 76: Switching model Control block structure.

The section marked as DC power control sets the DC current reference based on the AC reference set point. The section marked as Arm balancing is the implementation of arm balancing algorithm described in Chapter 6.7.2.

Balancing and normalization block is described in Chapter 6.7.1 and shown in Figure 49. The functionality of this control subsystem was investigated in Chapter 8.2 on an averaged converter model.

Phase shift modulator performs standard phase shift modulation for N levels of half bridge multilevel power structure. The illustration of the modulator operation is shown in Figure 27. The modulator generates the N triangle carriers phase shifted by $\frac{2\pi}{N}$ and compares them to the modulation indexes in order to generate the gating signals. When the modulation index value is greater than the carrier for the respective module the upper (insertion) switch gate is on, otherwise the lower (short out) switch is on. Since the converter has only half bridge switching section, the triangle wave and modulation indexes range from 0-1.

The model is simulated for a sequence of changes in the current controller references.

The controller references are cycled through the similar set of states used for the simulations given in Chapter 7.7.1. The references for the circulating currents in dq frame are given in Figure 77. The first plot is the command for the DC component of the circulating current, which controls the power at the DC side of the converter. The second plot is the reference for the fundamental harmonic of the of the circulating current used for arm balancing and is the output of the Arms balancing controller. As said before, the oscillations are the result of imperfect filtering in the implementation of the arm balancing controller described in Section 6.7.2.

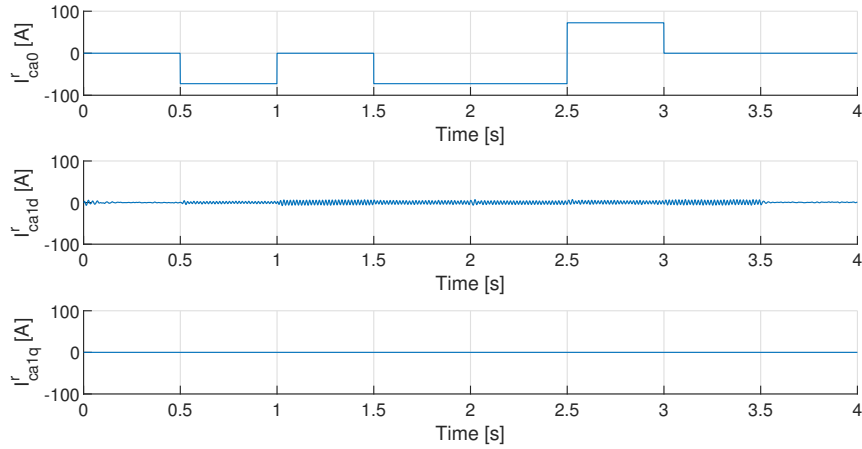


Figure 77: References for the circulating current for the switching model simulation.

The output current references in dq frame are given in Figure 78. The d current component controls active power and q reactive power. The d and q component references correspond to the amplitude of active and reactive current components. The rated amplitude of the active and reactive current component for the example system are 296A and 222A respectively.

Until $t=0.5s$ the references are at zero, meaning that the control forces AC and DC side currents to zero. At $t=0.5s$ the full active power is drawn from the AC side and delivered

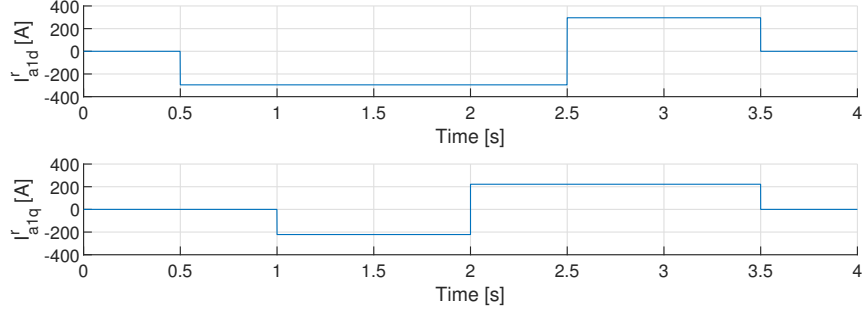


Figure 78: References for the output current for the switching model simulation.

to the DC. At $t=1s$ the DC side power is set to 0 making the converter charge its internal storage. At the same time full reactive power is drawn from the grid. At $t=1.5s$ DC side current is set to deliver full active power. The converter now maintains the state of charge of its internal storage. At $t=2s$ the reference for the reactive power is set to deliver the full reactive power. At $t=2.5s$ the reference for active current is set to deliver full active power from the AC side and DC side is set to draw full power from the external DC bus. At $t=3s$ DC current is set to zero. This means that the converter will discharge storage to the AC side at full power. At $t=3.5s$ all references are set to zero. This forces AC and DC side currents to 0.

The simulation results for the output and circulating currents are given in Figure 79. The waveforms from Figure 79 are zoomed at $t=0.5$ and shown in Figure 80 to illustrate the transient behavior of the converter. As can be seen, the transients last less than a fundamental cycle.

The waveforms from Figure 80 are zoomed even further the illustration of current ripple waveforms as shown in Figure 81. The normalized spectrum for the output current is given in Figure 82. As can be sen the harmonic content is low, all harmonics are below 1% except for the second harmonic.

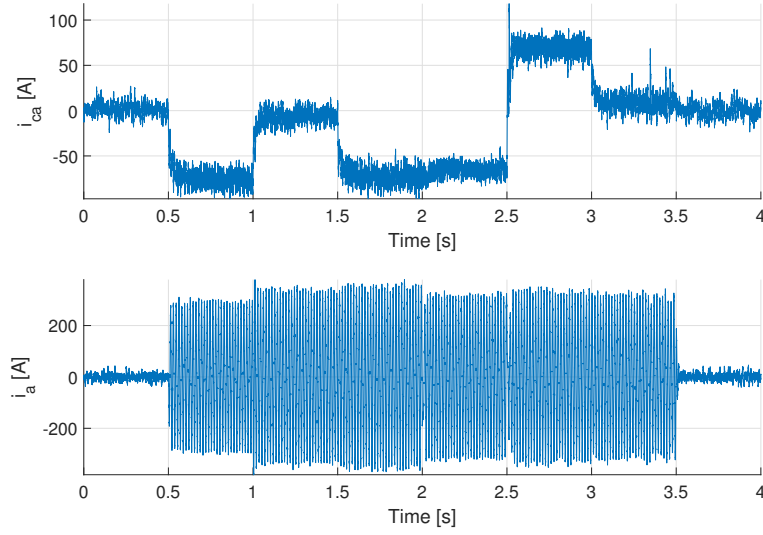


Figure 79: Circulating current and output current simulation results for the switching model.

The output current THD is about 6.7% based on all spectral components (not only harmonics) at full active and reactive current. It turns out that the arm inductance can be increased from $800\mu H$ to $1mH$ to reduce THD below 5%.

Note that the switching frequency is set to 600Hz for this simulation. The switching frequency is chosen to be ten times the fundamental to facilitate good balancing as mentioned in Chapter 4.5. With 40 modules per leg the effective switching frequency is 24kHz making the ripple in the output current is very low.

To speed the simulation up, the triangle carriers for the modulator are implemented digitally using counters with equivalent resolution of 9 bits. Consequently, the harmonics observed in the output are coming in part from the low resolution of the modulator combined with very low leg and grid inductances. It should be noted that most hardware implementation have 16 bit or better PWM blocks.

The module filter output voltages for both arms of the converter are shown in Figure 83.

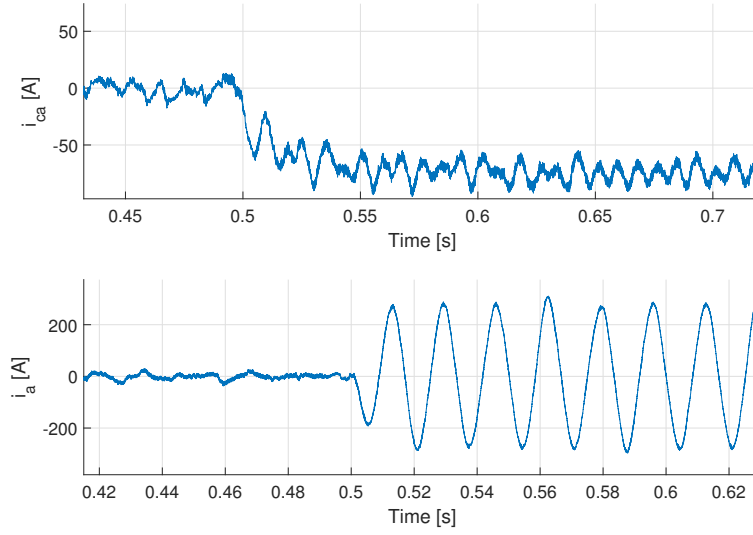


Figure 80: Circulating current and output current transient at $t=0.5$ s from Figure 79.

The amplitude of the module filter output voltages depends on the mode of operation of the converter. The amplitude is lowest when the converter is operating with active power only.

Figure 84 shows zoomed sections of the module filter voltages to illustrate the actual waveforms during the transitions at $t=1$ s. As can be seen besides the amplitude, the waveform shape also depends on the mode of operation. The difference comes from the difference in the angle between fundamental and first harmonic in the module input current caused by interaction between modulation and arm currents.

The module filter voltage waveforms from Figure 84 are further zoomed in Figure 85 to illustrate the waveforms in more detail and balancing action between 40 modules within each arm.

The example converter is designed to have fairly high voltage ripple on the output of the filter, 87V for the example system per Table 7. The total change in the storage system voltage from full charge to full discharge depends on the designed depth of discharge and is

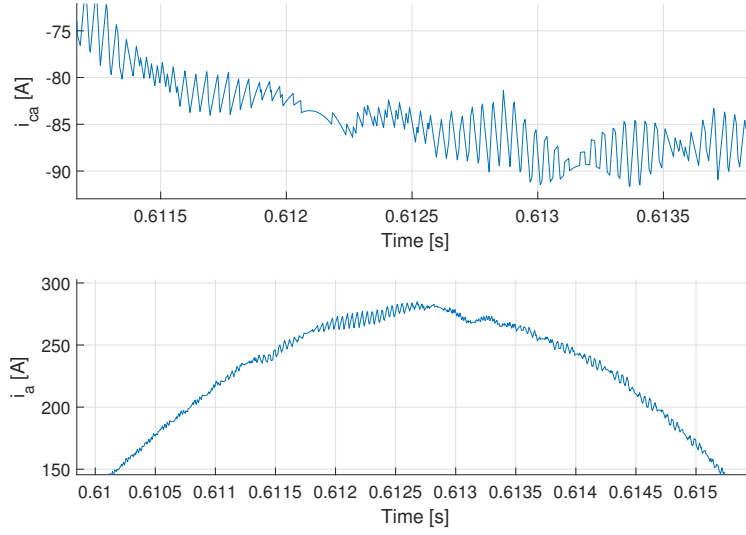


Figure 81: Output and circulating current ripple.

about 45V for the example system design given in Table 7. As a result, the average voltage change is difficult to notice in Figure 85. The State of charge can be observed by looking at the storage capacitor voltage given in Figure 86. As can be seen, the storage clearly charges and discharges as commanded and maintains balance well during the charge and discharge cycles.

The storage current for the upper and lower arm are shown in Figure 87. The storage current is well filtered, it has DC component with strong fundamental AC component superimposed but very low in other harmonic content. This is illustrated in zoomed waveforms of the storage current given in Figure 88.

The filter input current for all modules together is shown in Figure 89. The current has DC current with superimposed AC component. The modules share the converter arm current by chopping the waveform. This is illustrated in Figure 90.

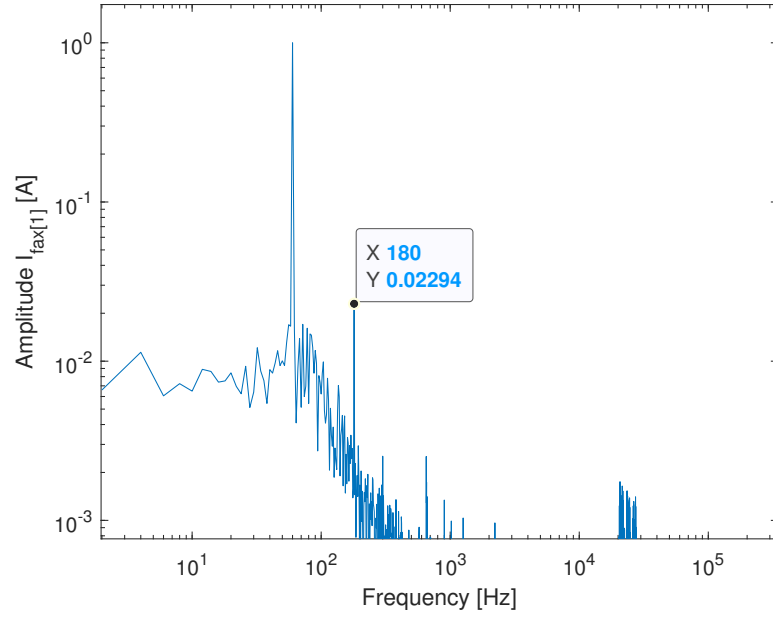


Figure 82: Normalized output current spectrum.

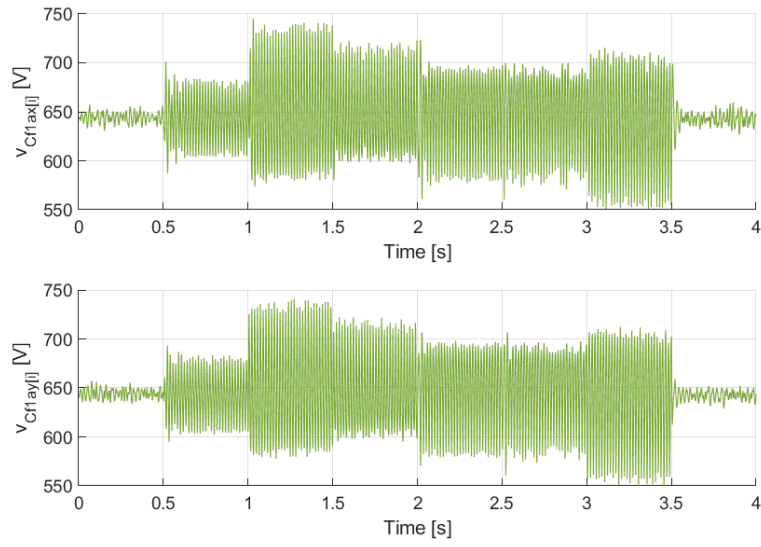


Figure 83: Module filter output voltages for top and bottom arms.

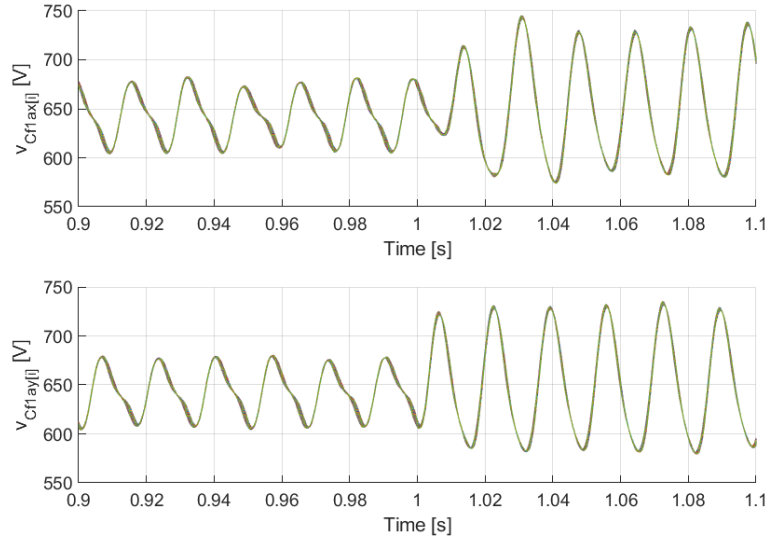


Figure 84: Module filter output voltages for top and bottom arms. Zoomed during transient at $t=1$ s to illustrate waveform shapes for different operating conditions.

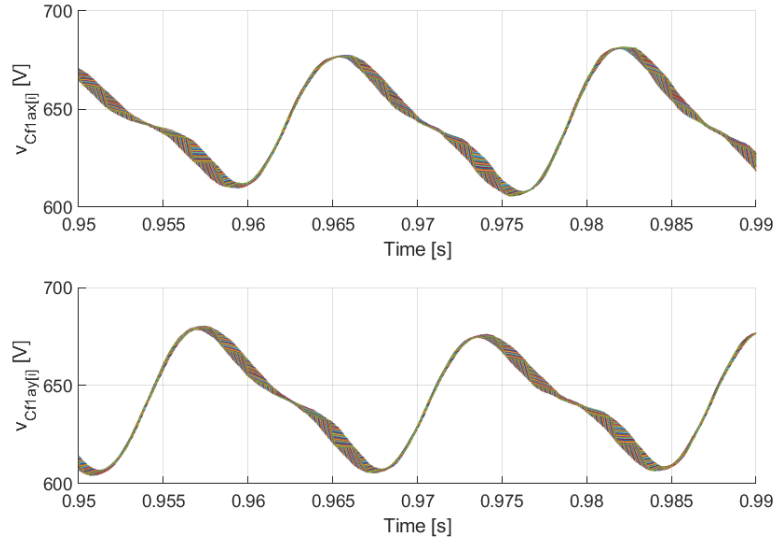


Figure 85: Module filter output voltages for top and bottom arms. Zoomed section during transient at $t=1$ s.

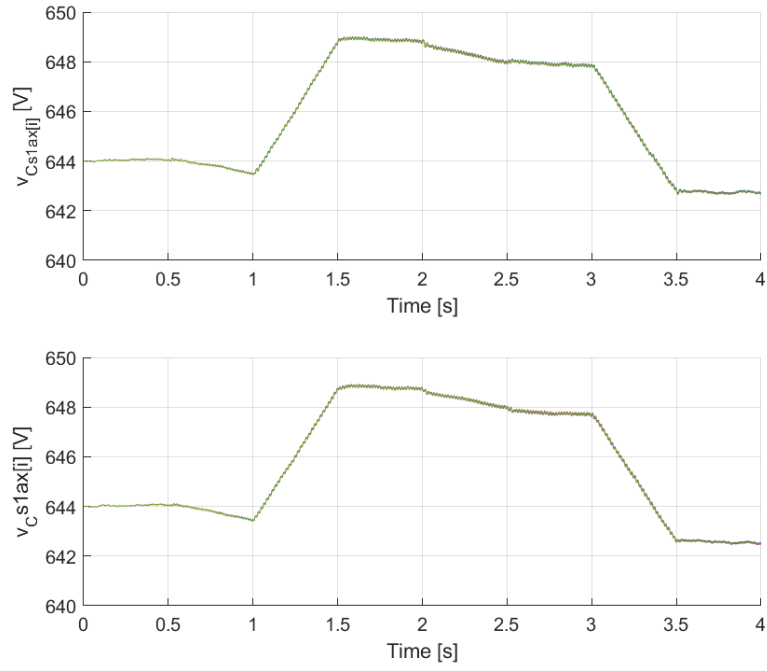


Figure 86: Module storage system voltage for top and bottom arms.

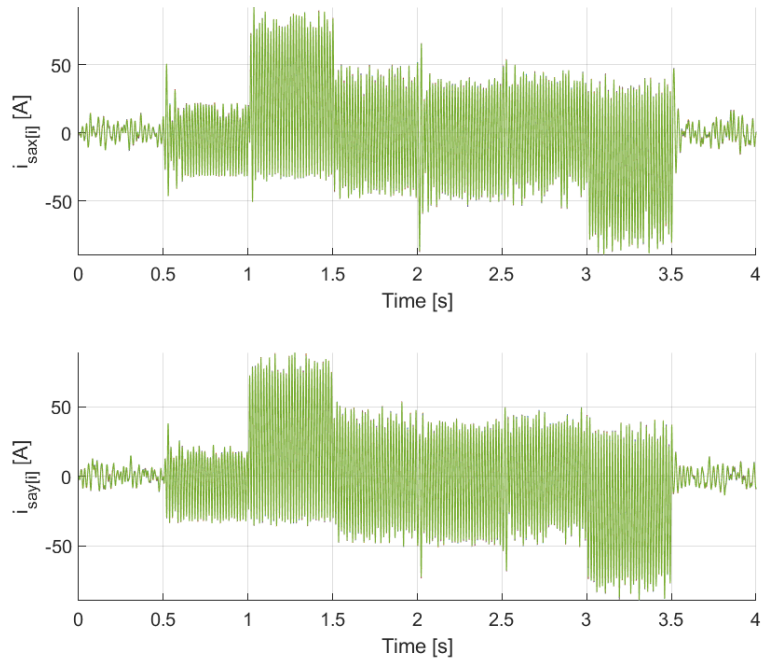


Figure 87: Module storage currents.

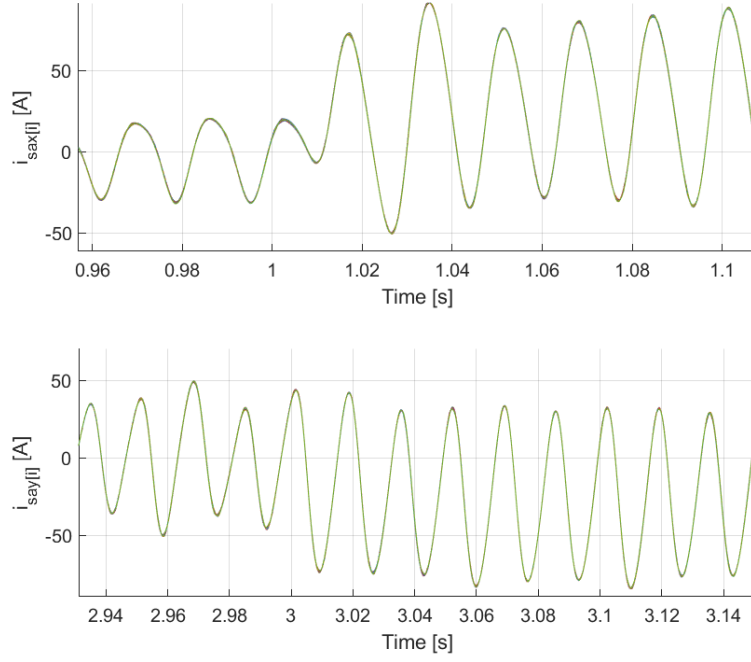


Figure 88: Module storage current waveforms. for two different points near the start and near the end of the simulation run.

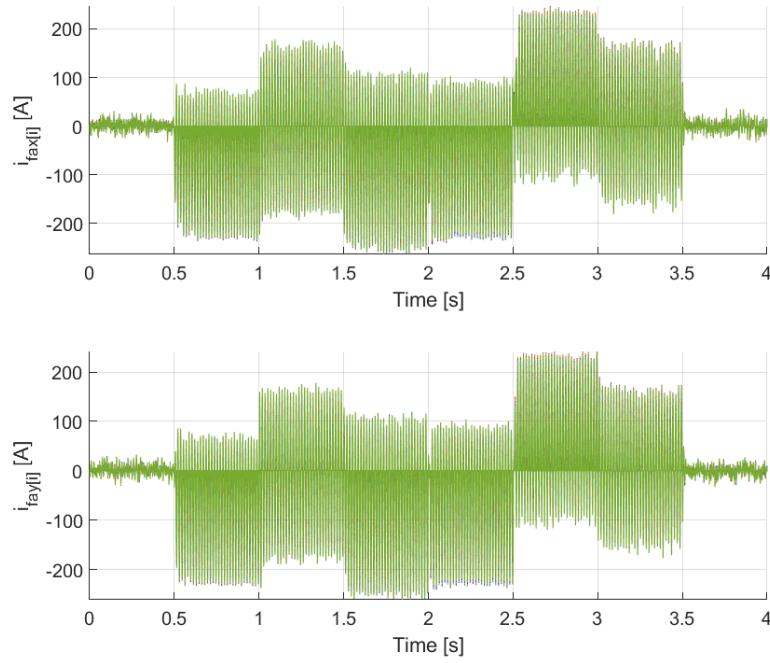


Figure 89: Filter input currents for upper and lower arm modules.

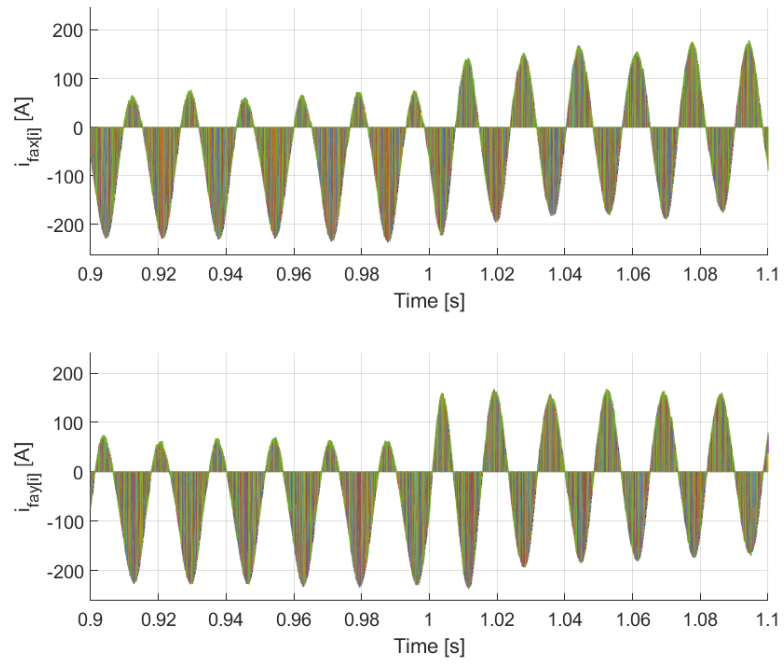


Figure 90: Zoomed section of filter input currents for upper and lower arm modules.

8.4 Module Stability Considerations

The approximate design approach for the module filter given in Chapter 7.6 assumes uniformly decaying magnitude characteristic. Even the model based design from Chapter 7.7 does not take into account most of the input current spectral components since the model is averaged and reduced. As the module illustrated in Figure 54 has fairly complicated structure, current resonance that can be excited in the C-L-C structure of the modules should be evaluated. The resonance peak in the magnitude characteristic may cause currents and voltages to exceed the design requirements. The easiest way to quickly evaluate possible resonance issues is to evaluate the frequency response of the module filter transfer functions from input current to the output voltage and storage current. The resonance peaks on the Bode plots can be compared to the locations of the harmonic components filter input currents to evaluate for potential issues.

Bode magnitude plots can be obtained from the model derived in Chapter 5.1.3 and given in Equation (75). For input current to output voltage Bode plot, the model from can be used directly. For the input current to storage current Bode plot the output matrices will have to be modified and are given in (279).

$$\mathbf{C}_f = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}; \quad D_f = 0 \quad (279)$$

The bode plots should be evaluated for the significant spectral components of the filter input current. The typical waveform of the filter input current for the single module can

be obtained by extracting one trace from the aggregate plot in Figure 90 and is given in Figure 91.

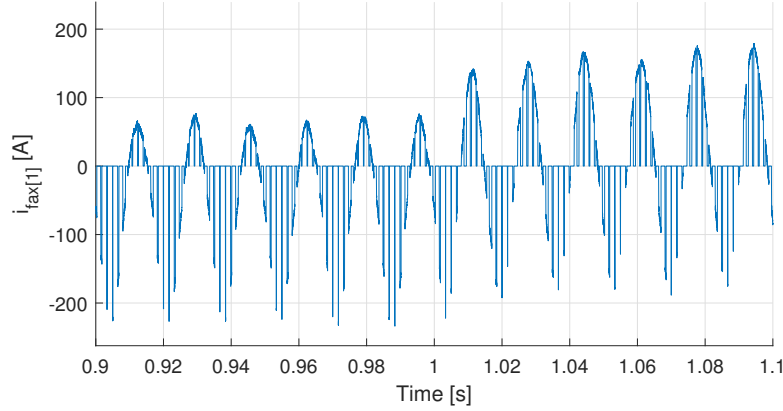


Figure 91: Zoomed section of filter input currents for one first module in the upper arm.

As mentioned earlier the main function of the module filter is to limit the oscillations at fundamental and first harmonic frequencies. However, the current coming from the switching section of the module is chopped as shown in Figure 91, therefore, the filter will also see high harmonic content at module switching frequency. Note that the module switching frequency is much lower than effective switching frequency seen by the arm inductors.

The magnitude plots for the gains from input current i_f to storage current i_s for the module from Figure 54 with parameters from Table 8 are given in Figure 92 together with the normalized spectrum of the input current i_f . The input current spectrum was calculated based on the current for the first module of the upper arm from $t=0.5$ s to $t=1$ s for the simulation run presented in Chapter 8.3. During this time the storage state of charge is maintained and the converter draws full active AC power.

The Bode plots show a resonance near 40Hz. This resonance peak will not cause problems as long as the converter is working as a grid tie at 60Hz or higher. In cases when the converter

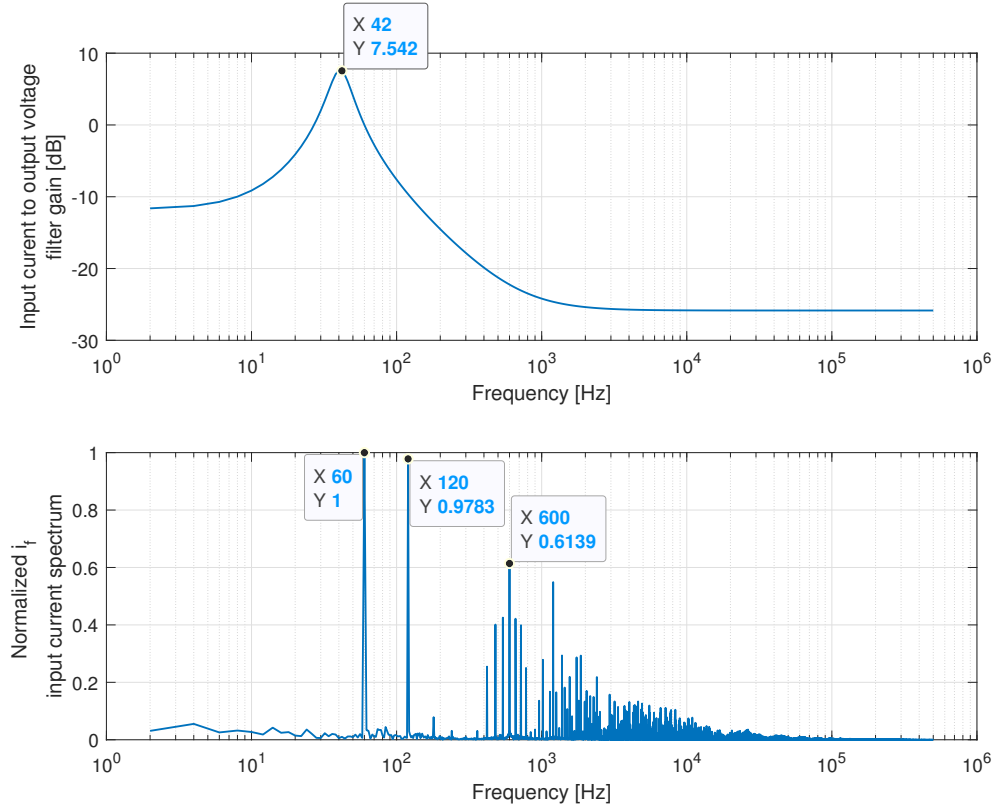


Figure 92: Magnitude Bode plot of the transfer function from the input current to the filter output voltage and normalized spectrum of the input current.

needs to operate at lower fundamental frequency the converter output should be de-rated to take into account the amplitude increase due to the resonance peaks. Another path would be to redesign the converter with resonances in mind.

The de-rating values can be roughly estimated from the relative gains for 40Hz/60Hz. From Figures 92 and 92 it can be expected that the storage current ripple RMS may increase by 55% if the fundamental goes down to 40Hz while the output voltage ripple will increase by about 12%.

To maintain the thermal rating of the storage system several options are available: the rated operating temperature can be decreased, cooling can be improved or higher current rating storage cells can be used. The semiconductors should be able to withstand extra 13%

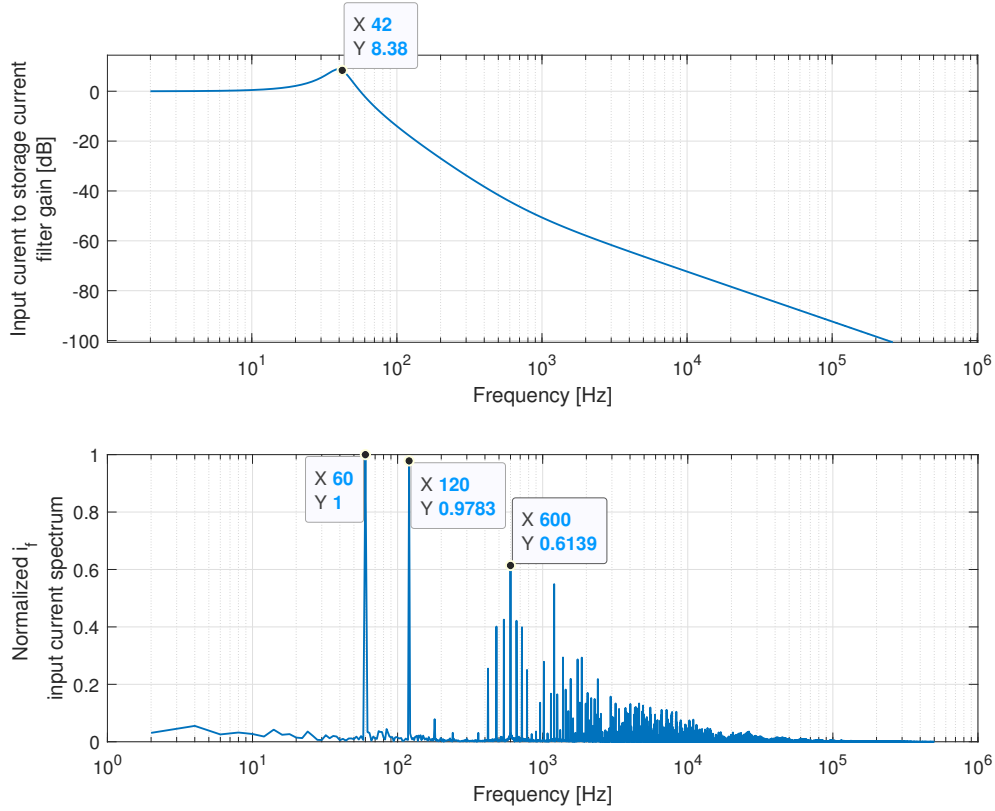


Figure 93: Magnitude Bode plot of the transfer function from the input current to the storage current and normalized spectrum of the input current.

of the ripple voltage (approximately 10V on average) and will not require change.

The current control should not be affected by the increase in the filter output voltage. The filter output voltage is measured and compensated for in the controller as described in Chapter 6. However, the depth of discharge must be reduced to maintain the minimum voltage reach of the arm and maintain controllability of the circulating current as explained in Chapter 7.3.1. This may reduce the storage capacity significantly (approximately 25% for the example system).

8.5 Low Voltage Ride Through and Reactive Power Support

To investigate the behavior of the system for the wind energy conversion applications, the converter leg is simulated during the LVRT event. The assumption is that the converter leg operates in a 3 phase grid tie for high power wind turbine as illustrated in Figure 94. The parameters of the system are given in Table 3 and the parameters of the grid tie converter with integrated energy storage were determined in Chapter 7.

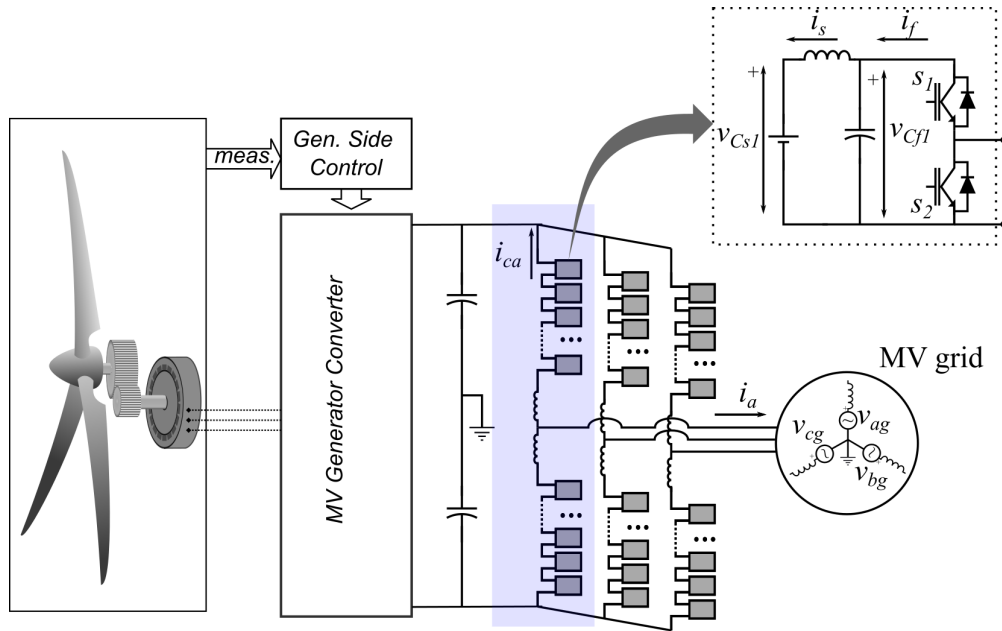


Figure 94: Application of the MMC converter within wind energy system with the representative leg highlighted.

It will be assumed that the converter must follow LVRT requirements from E-ON standard or similar [5]. The requirements are illustrated in Figure 95. According to E-ON standard standard, the converter must output rated reactive current during the low voltage sequence to support the grid voltage restoration. The active current will be dropped to zero during the short event and it will ramp up together with grid voltage as much as the reactive support allows. It will be assumed that the reactive current 1pu is the maximum

converter current corresponding to 6.25MVA from Table 3. The DC side current will remain unchanged to facilitate normal operation of the wind turbine system.

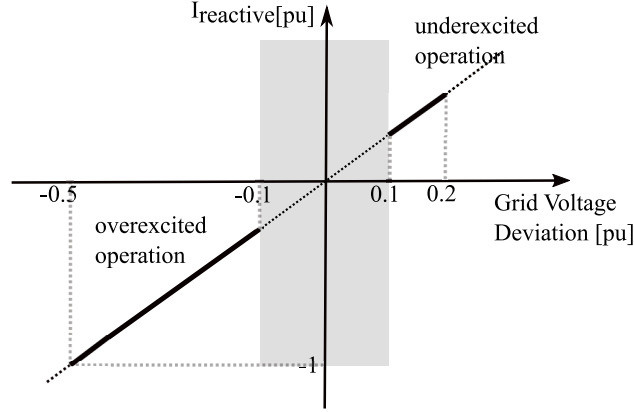


Figure 95: Reactive support requirement according to E-ON standard [5].

The simulated LVRT event profile follows the worst case curve which is the “may disconnect” borderline (A,B,C,D) from Figure 51. Accordingly, the simulated grid voltage waveform is shown in Figure 96. The LVRT event starts at $t=0.5$ s. Up to this point the converter delivers full power received from the wind energy conversion system to the grid. It is assumed that the wind energy conversion system delivers full rated power for the entire duration of the LVRT event as this should be the worst case for the storage system integrated into the grid tie converter.

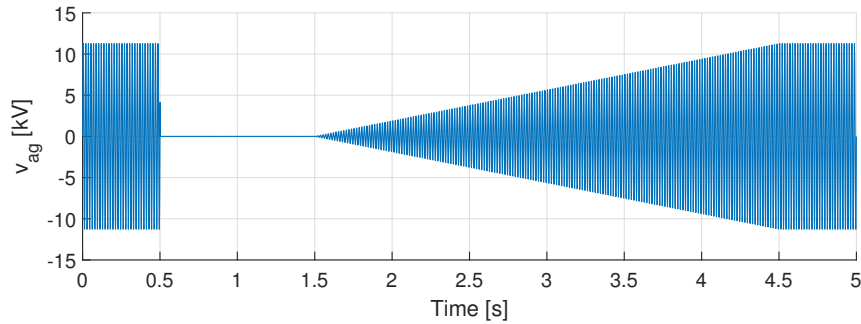


Figure 96: Grid voltage for the LVRT simulation run.

The circulating current fundamental and DC current component references and measurements in dq frame are shown in Figure 97. The DC current remains constant to protect wind energy conversion system from the fault and disturbances in the grid. A short transient at the beginning of the simulation can be observed in the references and measurements as the simulation is started from zero initial conditions. The fundamental of the circulating current is used for the arm storage balancing only. As can be seen, there are no significant imbalances or balancing control reference changes due to the LVRT event.

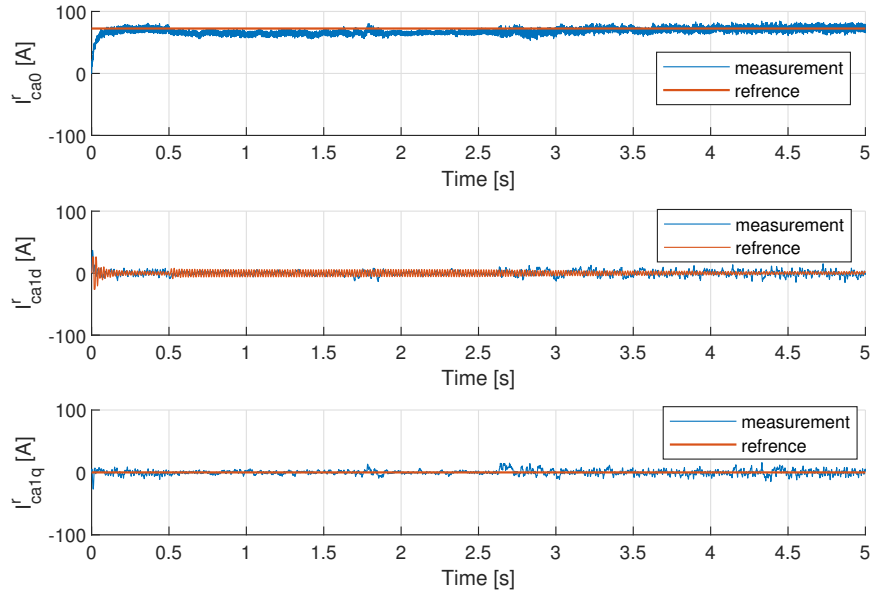


Figure 97: DC and circulating current fundamental references in dq frame during the LVRT event.

The references and measurements for the grid side output current are shown in Figure 98. As soon as the LVRT sequence starts, the active power reference controlled by the d current component changes to 0. In the same time, the reactive current reference controlled by the q component of the output current changes to full rated converter current leading (overexcited). As the grid voltage starts to recover, the reactive current command is decreased in accordance

with E-ON requirements given in Figure 95. The remaining converter current capacity is used to ramp up the active power delivery to the grid.

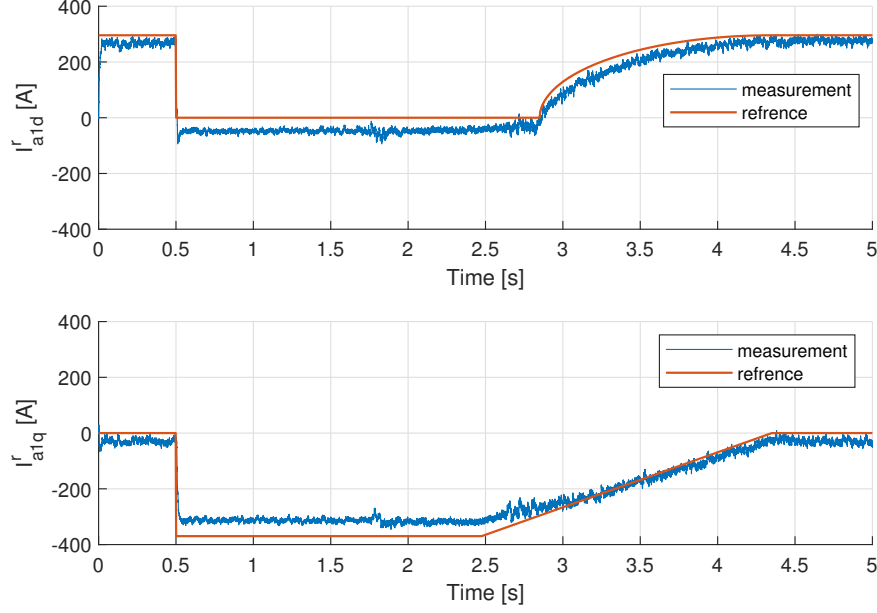


Figure 98: AC output current references and measurements in dq frame during the LVRT event.

As can be seen from simulation results, the measurements follow the references with some steady state error but respond to the command fairly well. Keep in mind that the current controller compensator is only proportional for pole placement, consequently the steady state error is expected. The steady state error can be corrected by introducing integral compensators for the outer loop PQ converter controllers or directly in the dq current control and will be left for future study. For this investigation, the current references are based on the grid voltage profile and are commanded in the open loop directly to the current controller.

The circulating (DC side) and grid currents for the entire duration of the LVRT event are shown in Figure 99. As can be seen, DC current remains fairly stable. As a result there is no need for the changes in power delivery on the wind turbine side. Effectively, this will

isolate the wind turbine mechanical system from the LVRT disturbance on the grid.

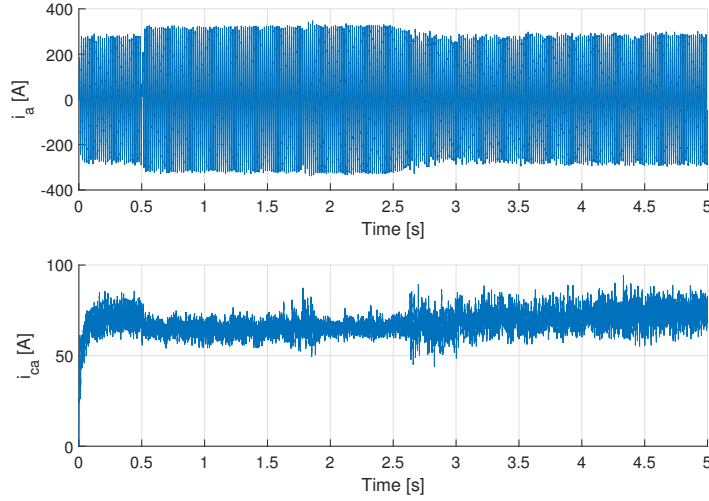


Figure 99: DC and AC side current waveforms of the converter leg during the LVRT event.

The grid current and voltage in per unit are shown together in Figure 100 to illustrate the control performance and the reactive current support. At the short circuit instant when the grid voltage drops to 0 the current shifts from active power delivery to reactive power support. The current phase changes from being in-phase with the voltage to 90 degree leading as required by the standard to assist in the grid voltage restoration. The entire transient in the current waveform is over in less than half of the fundamental cycle.

During the LVRT event, the rated wind power cannot be delivered to the grid due to the low grid voltage and reactive current support requirements. During the event, the power imbalance between AC and DC side is stored in the energy storage system integrated into the converter leg. The simulation results in Figure 101 show the storage system voltage for the modules in the upper and lower arm of the converter leg and the voltage rise as a consequence of the energy storage storage charging. Note that the storage is well balanced making the individual module storage system voltages almost indistinguishable.

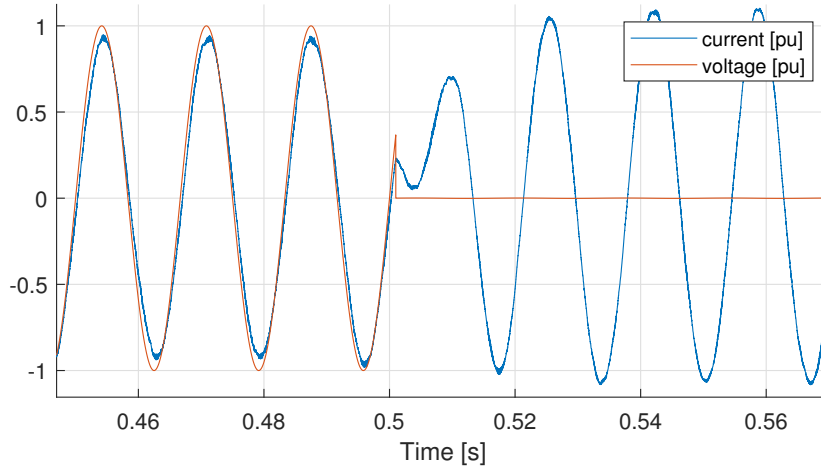


Figure 100: Active power, reactive current support and control performance illustration during the LVRT event.

To illustrate that the LVRT event does not cause any unpredictable effects inside the module, the filter capacitor voltages are given in Figure 102. As expected the ripple voltage increases during the increase in the reactive current delivery and the average slowly rises but there are no undesirable effects.

Output voltage of the converter leg together with the zoomed section of the converter output and grid voltage is shown in Figure 103. The number of levels of the converter is quite high, 40 in this case, as a result the actual PWM is barely noticeable. The large number of modules and levels enables easy control for low voltage conditions. For example, during the short circuit the effective output voltage is equivalent to only one module voltage. As the grid voltage recovers, more and more levels contribute to the output.

The simulation results show that the converter leg is capable of operating under the conditions expected during the LVRT events. The DC side current does not show any significant disturbances during the short circuit and grid recovery and remains well controlled during the entire event. The AC side current is also well controlled and stable during the entire

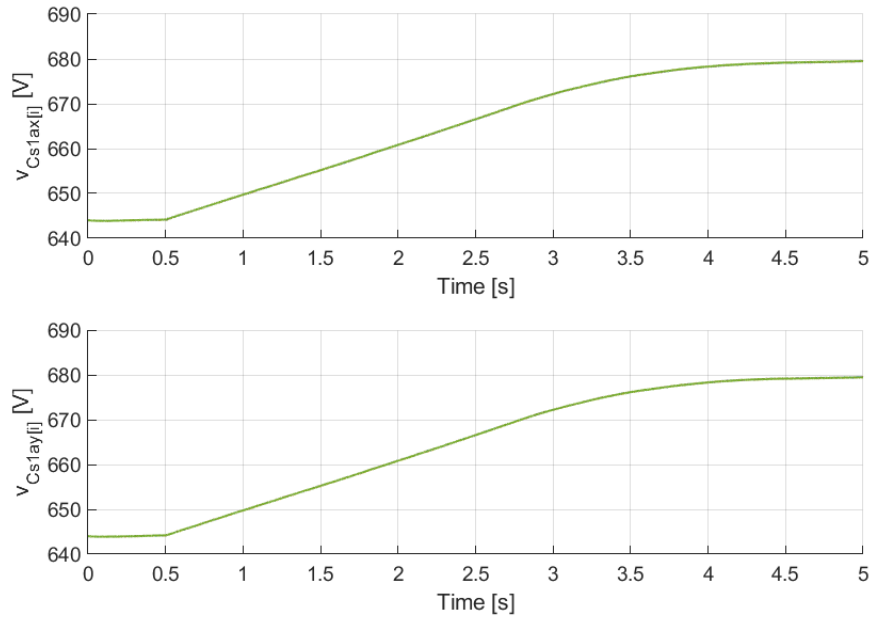


Figure 101: Storage system voltage within the modules of upper and lower arm of the converter leg during the LVRT event.

LVRT event. It should be noted again, that the steady state error is expected due to the proportional closed loop compensator chosen for the current control.

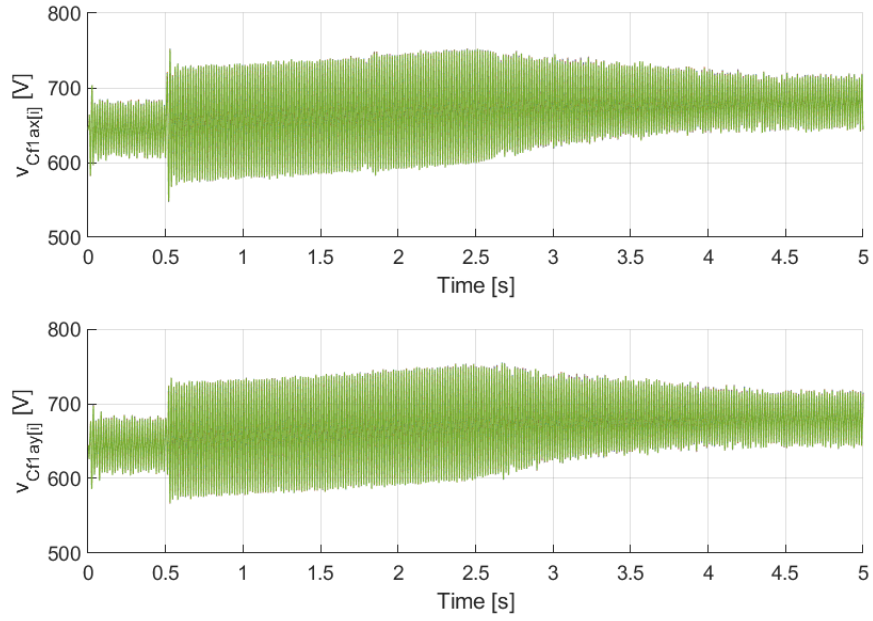


Figure 102: Filter voltages of modules within upper and lower arm of the converter leg during the LVRT event.

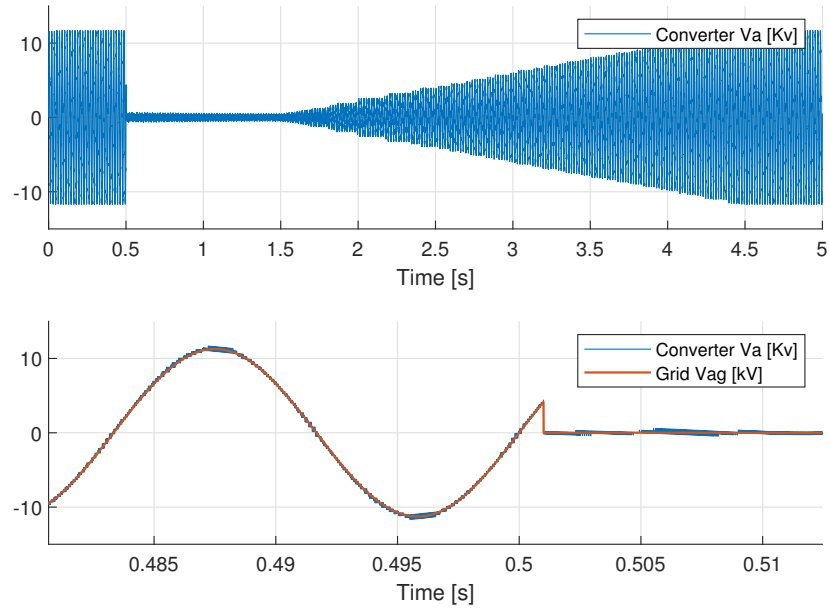


Figure 103: Converter output voltage and zoomed section of the converter output voltage compared to the grid back emf voltage just at the start of the LVRT sequence.

9 Conclusion

The analysis of the MMC converter topology will be concluded here for the purpose of this study. Although the actual components have not been selected yet, the converter structure has been fully analyzed and defined. Using the information outlined in this dissertation, it is possible to determine all the parameters needed for the component selection. For example, the input filter currents will directly correlate with the requirements for the semiconductor switches. Filter and storage currents can be used to determine RMS currents for the DC bus capacitors for each module, RMS and peak currents for the filter inductors and so on. This will further allow losses estimation, thermal analysis and actual mechanical design with specific component selection.

Thermal and mechanical design should be fairly generic and comparable to other medium voltage converter topologies. Since the losses analysis, thermal and mechanical design and hardware component selection must be tightly focused on a specific implementation of the converter they fall out of the scope of this study aimed at the general design and converter sizing analysis.

The contributions covered in this text include:

- Analysis of the idealized MMC structure in Chapter 4.
- Analysis of the power flow within the converter from the standpoint of circulating and output currents and their harmonics in Chapter 4.4.
- Detailed mathematical modeling of the generalized converter structure including:
 - Generalized module structure models including integrated storage variants in

Chapter 5.1.

- Generalized switching model in state space from in Chapter 5.3.
 - Generalization of the linear ripple approximation approach and model averaging in Chapter 5.4.
 - Model order reduction and simplification in Chapter 5.5.
- Control system analysis including:
 - Five axis open loop controller for full converter leg control and the control of integrated energy storage in Chapter 6.4.
 - Closed loop compensator design with pole placement in Chapter 6.5.
 - Module balancing controller in Chapter 6.7.1.
 - Arm balancing controller in Chapter 6.7.2
 - Detailed structure sizing procedure with optimization elements in Chapter 7.
 - Fine tuning guidelines and general structure simulation verification in Chapter 8.

Future study directions may include: Analysis of the multi-phase system controller and stability using the structures described in the current text. Extension of the analysis for low switching frequencies and "staircase" modulation and investigation of the necessary conditions for the integrated storage control in this case. Since the MMC power structure is fairly broad topic, other future study opportunities have been identified and pointed out throughout the current text.

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