AN ALL-DIGITAL CHARGE TO DIGITAL CONVERTER

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DECLARATION

I hereby declare that this thesis is my own work and effort and that it has not been submitted anywhere for any award. Where other sources of information have been used, they have been acknowledged.

Newcastle upon Tyne September 2018

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CERTIFICATE OF APPROVAL

I confirm that, to the best of my knowledge, this thesis is from the student's own work and effort, and all other sources of information used have been acknowledged. This thesis has been submitted with my approval.

ALEX YAKOVLEV

To the soul of my wonderful Wife, and my lovely family.

— Yuqing

ACKNOWLEDGEMENTS

I would like to express my deep gratitude to my supervisors Prof. Alex Yakovlev, Dr. Delong Shang and Dr. Fei Xia for their support and guidance through my PhD journey. They have always been a source of motivation and my inspirational model as a researcher.

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ABSTRACT

During the last two decades, the topic of the Internet of Things (IoT) has become very popular. It provides an idea that everything in the real world should be connected with the internet in the future. Integrating sensors into small wireless networked nodes is a huge challenge due to the low power/energy budget in wireless sensor systems. An integrated sensor normally consumes significant power and has complex design which increases the cost. The core part of the sensor is the sensor interface which consumes major power especially for a capacitor-based sensor.

Capacitive sensors and voltage sensors are two frequently used sensor types in the wireless sensor family. Capacitive sensors, that transform capacitance values into digital outputs, can be used in areas such as biomedical, environmental, and mobile applications. Voltage sensors are also widely used in many modern areas such as Energy Harvesting (EH) systems. Both of these sensors may make use of sensor interfaces to transform a measured analogue signal into a frequency output or a digital code for use in a digital system. Existing sensor interfaces normally use complex analog-to-digital converter (ADC) techniques that consume high power and suffers from slow sensing response.

This thesis proposes a smart all-digital dual-use capacitor-based sensor interface called charge to digital converter (QDC). This QDC is capable of not only sensing capacitance but also sensing voltages by using fully digital solutions based on iterative delay chain discharge. Unlike the conventional methods

that only treats the sensed capacitance only as the input signal, this thesis proposes a method that can directly use the stored energy from the sensed capacitance as well to power parts of the circuit, which simplifies the design and saves power. By playing with the capacitance and input voltage, it can be used as a capacitance-to-digital converter (CDC) to sense capacitance under fixed input voltage and it also can be used as a capacitor-based voltage sensor interface to measure voltage level under fixed capacitance. The new method achieves the same accuracy with less than half the circuit size, and 25% and 33% savings on power and energy consumption compared with the state of art benchmark. The method has been validated by experimenting with a chip fabricated in 350nm process, in addition to extensive simulation analysis.

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ACRONYMS

QDC charge-to-digital converter

CDC capacitance-to-digital converter

ADC analog-to-digital converter

PCB printed circuit board

CVC capacitance-to-voltage converter

SAR successive approximation

CDAC capacitive digital-to-analog converter

TDC time-to-digital converter

TDCs time-to-digital converters

RO ring oscillator

VPwC voltage-to-pulse width converter

EH energy harvesting

VCO voltage controlled oscillators

PMOS p-type metal-oxide-semiconductor

NMOS n-type metal-oxide-semiconductor

MUTEX mutual exclusion

LVS Layout verse schematic

DRC Design Rule Check

PGA pin grid array

PCB printed circuit board

MUTEX mutual exclusion

IoT Internet of Things

WSN wireless sensor network

Part I

Thesis Chapters

1

INTRODUCTION

1.1 MOTIVATION

The term Internet of Things (IoT) was initially proposed by Kevin Ashton in 1999 [5]. The basic concept of IoT is that every object in the real world can be connected together with the internet [72]. Many people believe that building a smart world is the goal for the near future, where the world itself will be covered by sensing and actuation [70]. During the last two decades, the research on IoT has been developed tremendously [80, 31, 56]. The dream of a smart world is becoming closer. Nowadays, for instance, home automation develops fast to provides a more convenient life style for people than before [26]; Many buildings have sensors to save power [11, 83, 70]; Mobile phones with sensors help people achieve things that was not possible before [14]; Wearable devices in healthcare monitor people's body conditions in real time [45, 44]. However, all of these are still at early stages of development and are not qualified enough to build a smart world [70]. One important issue is the degree of the density of sensing coverage. In the world of IoT, the density of sensing coverage should be way higher than today [70].

The wireless sensor network (WSN) is one of the foundational technology for IoT [80]. The wireless sensor plays a vital role as a bridge connecting the physical world and the information world [72]. The increasing density of sensing for IoT means more power

consumption and cost on WSN in total. Integrating sensors into small wireless networked nodes thus becomes a huge challenge due to the low power/energy budget in wireless sensor systems [32]. The integrated sensor normally consumes significant power and has complex design which increases the cost.

Sensors, as a key part of the WSN, are hot topics in industrial and research fields [36, 3, 41, 13]. A sensor is a device which can detect a physical parameter (e.g., humidity, temperature, pressure, voltage, etc.) from a target and then output a digital or other desired signal corresponding to and representing this parameter to fulfil requirements such as data transmission, processing, storage, recording and controlling [6].

The capacitive sensor is one of the widely used types in the sensor family [17, 75]. Capacitive sensors are a solution of sensing and measuring many different types of quantities [6] because a large number of physical quantities can be made to charge a capacitor so that this charge reflects the value of the parameter [81]. Unlike other sensors, capacitive sensors can detect both conductive and non-conductive materials [58, 74]. Moreover, capacitive sensors tend to consume lower power compared to others so the battery life for small portable products may last for a very long time [6].

The voltage sensor is also a very important type of sensors in many applications [84, 76, 68]. A voltage sensor can detect and/or measure voltages and transform them into efficient output signals in order to monitor or control the voltage of an equipment or a system. For example, in Energy Harvesting systems, voltage levels are monitored during energy accumulation. Based on the different voltage levels, different tuning mecha-

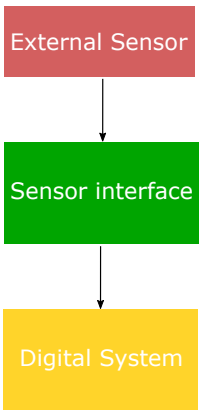


Figure 1.1: Basic sensing system

nism are used to achieve greater energy accumulation efficiency [81].

Both of the above types of sensors may need sensor interfaces [39, 46]. Fig. 1.1 shows a simple basic sensing system. A sensor interface is used to transform a measured analogue signal (e.g., capacitance, voltage level) from an external sensor into a frequency output or a digital code [85] for use in a digital system e.g., a microcontroller. Typically, sensor interface requires complex analogue circuits, e.g., amplifiers and analog-to-digital converter (ADC), which increase design complexities and often require additional power consumption [32, 81]. An all-digital converter will significantly reduce the power consumption comparing with the conventional converters. The development of the digital converter will be shown in the literature review below.

The sensor interface in a capacitive sensor is typically realized with a capacitance-to-digital converter (CDC) , which converts a sensed capacitance value to a digital code. A CDC can be implemented with a charge-to-digital converter (QDC), which converts the amount of charge on a capacitor to a digital code. On the other hand, a QDC can also be used in other sensing applications unrelated to capacitance sensing where it does not

serve as a CDC , and a CDC can also be implemented with other non-QDC methods. The distinction between CDC and QDC is an important concept throughout this thesis.

1.2 THESIS CONTRIBUTION

The aim of this thesis is to present a power efficient QDC that can be used in both capacitive sensing and voltage sensing systems. The following contributions are made as a result of this research work.

- An all-digital capacitor-based QDC is proposed. This QDC is capable of not only sensing capacitance but also sensing voltages by using fully digital solutions based on iterative delay chain discharge. Unlike the conventional methods that only treats the sensed capacitance only as the input signal, this thesis proposes a method that can also directly use the stored energy from the sensed capacitance to power parts of the circuit, which simplifies the design and saves power. By playing with the capacitance and input voltage, it can be used as a CDC to sense capacitance under fixed input voltage and also can be used as a capacitor-based voltage sensor to measure voltage level under fixed capacitance. The all-digital design results in low power, low energy consumption, fast response time, high resolution and low system complexity compared to other CDCs and QDCs.

- A test chip consisting of the all-digital QDC was fabricated and used in experimental tests for validation purposes, in addition to extensive simulation analysis.

1.3 PUBLICATIONS

The published paper can be seen as following:

1. Y. Xu, D. Shang, F. Xia and A. Yakovlev, *A smart all-digital charge to digital converter*, 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, 2016, pp. 668-671. doi: 10.1109/ICECS.2016.7841290

2. D. Shang, Y. Xu, K. Gao, F. Xia and A. Yakovlev, *Low power voltage sensing through capacitance to digital conversion*, 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Kosice, 2016, pp. 1-6. doi: 10.1109/DDECS.2016.7482476

3. K. Gao, Y. Xu, D. Shang, F. Xia and A. Yakovlev, *Wideband dynamic voltage sensing mechanism for EH systems*, 2015 25th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Salvador, 2015, pp. 185-192. doi: 10.1109/PATMOS.2015.7347605

4. D. Shang, O. Benafa, F. Xia, Y. Xu and A. Yakovlev, *An elastic timer for wide dynamic working range*, 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS), Grenoble, 2015, pp. 1-4. doi: 10.1109/NEWCAS.2015.7182004

1.4 ORGANIZATION OF THESIS

This thesis is organized into six chapters, as shown in Fig. 1.2. Their contents are described as followed:

Chapter 1 "Introduction": introduce the motivations, contributions,publications and organization of this thesis.

Chapter 2 "Background and Literature Review": This chapter provides a background knowledge of capacitive sensors and their applications. subsequently, it presents a coherent overview of existing approaches for sensor interfaces including ADC-based CDC, and Frequency/time-based CDC. Moreover, it shows the existing voltage sensing technologies. It also studies the operation of capacitor discharging through a ring oscillator. In addition, the characteristic of metastability and its solution is introduced. In the end, it discusses the existing QDC with their advantages and disadvantages.

Chapter 3 "General theory of Digital Discharge QDC": This chapter presents the design process from a simple RC discharging circuit to an iterative delay chain discharge method which can form the foundation for QDC. The mechanism and algorithm behind these methodologies are explained. It also studies the capacitance to digital discharge progress.The mathematical theory shows that the proposed design can not only sense capacitance under fixed input voltage but also can sense voltage under fixed input capacitor.

Chapter 4 "Design and Implementation": In this chapter, a detailed QDC design which contains six blocks is provided. Firstly, it presents the asynchronous implementation of the design. Then the functions of each block are explained with the circuit designs and timing diagrams in detail.

Chapter 5 "Experimental Results and Validations": This chapter firstly presents the simulation results in terms of power consumption, total energy, response time, output codes. A summary of the measured results of the QDC will be presented in a table and compared to the state of art benchmark. Then the

fabricated chip and its test platform is showed. Finally, the chip performance is discussed based on the tested results.

Chapter 6 "Conclusions and Future Work": This chapter summarizes the contributions of the thesis and includes a critical review of this research as well as the prospective future work.

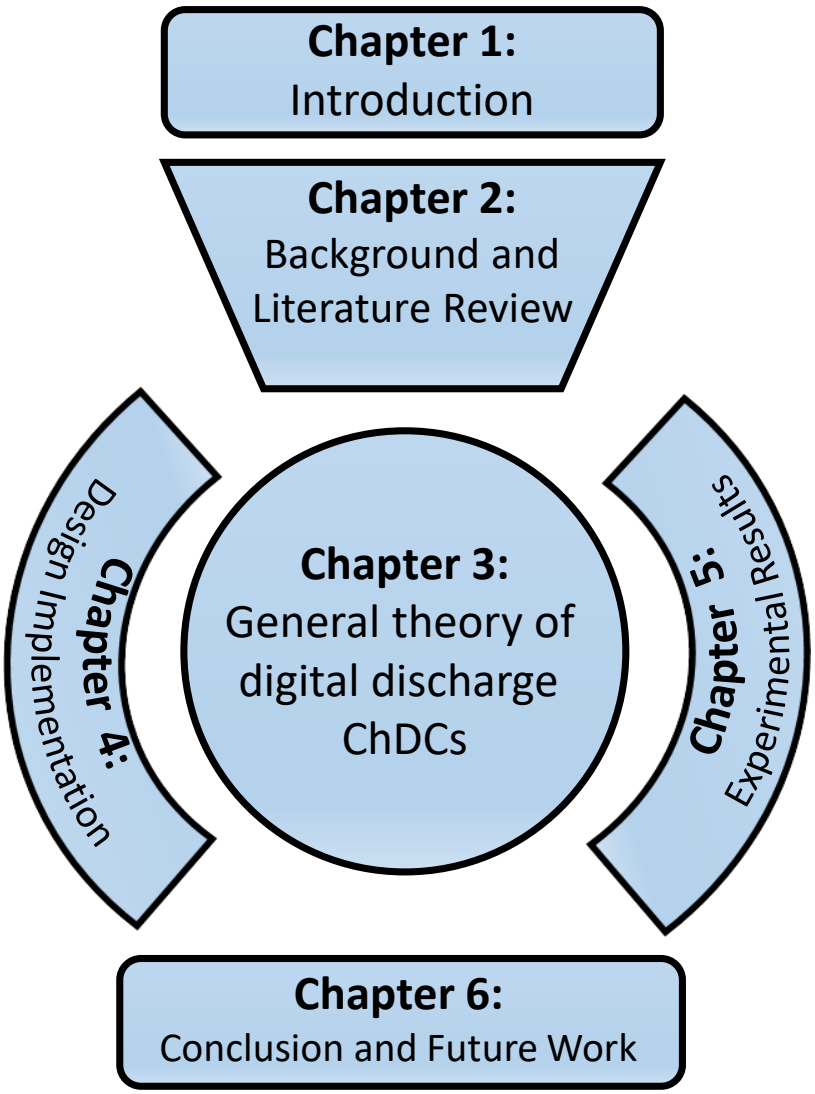


Figure 1.2: Thesis orginization.

2

BACKGROUND AND LITERATURE REVIEW

2.1 INTRODUCTION

Section 2.2 will show an overview of capacitive sensing including the characteristics of capacitors and applications of capacitive sensors. The capacitance-to-digital converter (CDC) will thereafter be presented in section 2.3. This section will start by introducing how a CDC is used in a capacitive sensing system as well as the main types of the CDC. After that, the detailed methodologies of modern CDCs will be presented with their advantages and disadvantages discussed. In section 2.4, the principle of voltage sensing will be presented by giving some examples of the existing voltage sensing techniques. Section 2.5 will introduce the principles of the charge-to-digital conversion system. In section 2.6, the principle of capacitor discharging through a ring oscillator will be presented. The final section of this chapter, section 2.7 will explore the definition of metastability and the mutual exclusion (MUTEX) element.

2.2 CAPACITIVE SENSING

2.2.1 *Capacitors*

The capacitance of a capacitor can be calculated as [74, 10]:

$$C = \varepsilon_r \frac{\varepsilon_0 A}{d} \tag{2.1}$$

where,

C is the capacitance in farads (F),

ε_r is a dielectric constant of the material between the two plates,

ε_0 is permittivity of free space and is equal to 8.85×10^{12} F/m,

A is the area of each plate in m^2 and

d is the distance between two plates.

According to the Eq. 2.1, except ε_0 which is a constant, the rest three parameters: ε_r, A and d become the factors that change the characteristics of a capacitor. In other word, the functions of different capacitive sensors are determined by varying any of these three parameters.

2.2.2 *Capacitive Sensors*

A large number of capacitive sensors with different functions have been developed [4, 18, 16, 34, 55]. Some typical applications of capacitive sensors are shown below:

Proximity Sensor: A capacitive proximity sensor is a type of sensors that can provide non-contact detection of nearby ob-

jects. Unlike inductive proximity sensors which can only detect metal objectives, capacitive proximity sensors can detect not only electrically conductive, but also non-conductive objects such as glass, plastics, paper and so on [58, 74]. The key parts of a typical capacitive proximity sensor is a capacitive probe, an oscillator and a controller unit. When a target gets near the capacitive probe, the electric field around the capacitor changes. This results in a change of the oscillator frequency. It is then detected and sent to controller unit [58, 74]. Because there is no direct contact between a capacitive proximity sensor and a sensed object, it is very reliable and has long functional life [74].

Humidity Sensor: Humidity plays an important role in many areas such as manufacture industry, agriculture, comfortability of daily life and so on [71]. For a capacitive humidity sensor, the dielectric constant of material ε_r, in this case, air, is influenced by humidity. According to Eq. 2.1, the value of a capacitance is in direct proportion of ε_r[74]. Basically, when temperature goes higher, the air holds more moisture. The dielectric between two plates in the capacitor then collects more moisture, which causes the change of ε_r and results in the change of capacitance [85].

Liquid level sensor: Liquid level sensors are widely used to monitor the liquid volume in industry and medical field [27]. In a capacitance, the dielectric constant changes when the device occupies different levels of liquid because the relative permittivity of liquid and air are different. When the plates start to fill with liquid, more and more space, in other words, the dielectric, between the two plates will be filled by liquid as well. The capacitance will then increase because liquid has more ability to hold electric charge than air [74, 20].

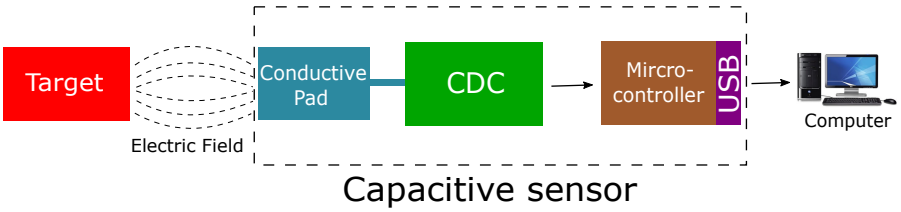


Figure 2.1: CDC-based Capacitive sensing system

Table 2.1 shows a case study of how capacitive sensors are used in our daily life in terms of its working environment, description and sensor type, and receptively.

2.3 CAPACITANCE TO DIGITAL CONVERTER

In the modern capacitive sensor interface technologies, standardized and easy to read output are two main goals leading the research direction [50]. In capacitive sensor design, a CDC is commonly used as a sensor interface.

Fig. 2.1 shows a typical CDC-based capacitive sensing system. Mainly, it includes three different sections. These are a conductive pad, a CDC section and a data transmission section. The conductive pad normally can be either a simple piece of metal, or a conductive trace on a printed circuit board (PCB). The CDC section includes a capacitance to digital converter. The data transmission section contains an interface such as a USB and is managed by a microcontroller.

Let us take a proximity sensor as an example. When the object is at a detectable distance from the conductive pad, it produces a capacitance and refers to CDC. The CDC then converts the capacitance to digital output. Then the output signal from CDC transmits to microcontroller to process the digital data. At last, these data are sent to computer through USB. When the target moves towards or away from the capacitive pad within an

Table 2.1: Applications of capacitive sensors.

Sensor type	Scenarios	Description	Reference
Proximity sensor	In most smart phones usage	To detect whether the user is listening to the call with or without the loudspeaker. When a user answers a call without the loudspeaker and his/her ear is near the phone, the sensor implemented in the mobile phone detects this and turns off the screen light to save battery.	[64]
Humidity Sensor	In production of noodles	Humidity sensors are widely used in noodle production such as flour moisture control, noodle drying, swear stage humidity monitoring and so on.	[57]
Liquid level sensor	Rain gauge	Liquid level sensors are often used as rain gauges to monitor the level of rainfall, which is an important parameter for weather station to analyse the climate.	[27]
Displacement sensor	Thickness Measurement	Measuring if the thickness of rolled steel sheets is uniform, if the thickness of laminated glass achieves the standard, etc.	[33]
Tilt sensor	Anti-theft system in car	Prevent a vehicle from being stolen. When the vehicle is being lifted by a car jack, the tilt sensor will detect the attempt of removing the wheels.	[77]

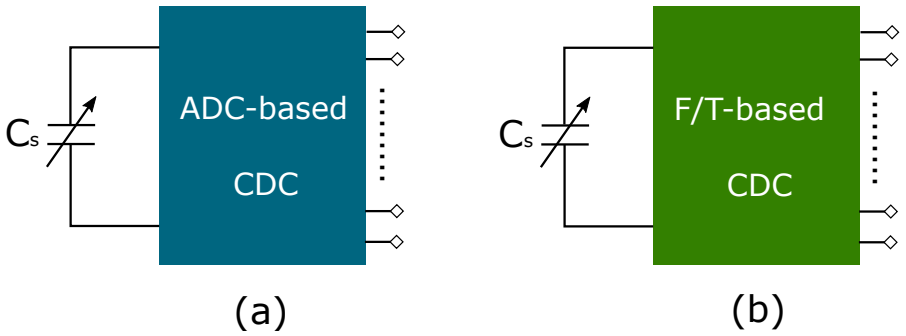


Figure 2.2: Two different types of CDCs (a) CDC based on ADC modulation; (b) CDC based on frequency/time modulation

effective range, the capacitance changes because electric fields between the target and conductive pad changes. Then the capacitive sensor repeats the above steps and generates new output data.

Fig. 2.2 shows two general types of CDCs based on different modulations. Conventional CDCs are based on an analog-to-digital converter (ADC), which contains ADC-related techniques, as shown in Fig. 2.2(a). They convert capacitance to electrical signals and measured with ADCs. The other type of CDCs uses Frequence/Time modulations, as shown in Fig. 2.2(b). They transform capacitance into frequencies or periods and often measure with time-to-digital converters (TDCs).

2.3.1 *ADC-related CDC*

The ADC-baesd CDC technique is unrelated to the proposed design in this thesis. Hence, only a short review are presented.

Fig. 2.3(a) shows a ADC-based CDC that transform the sensor capacitance C_s into a output analog voltage V_o by using a capacitance-to-voltage converter (CVC). V_o then is digitized via an ADC [23, 79].

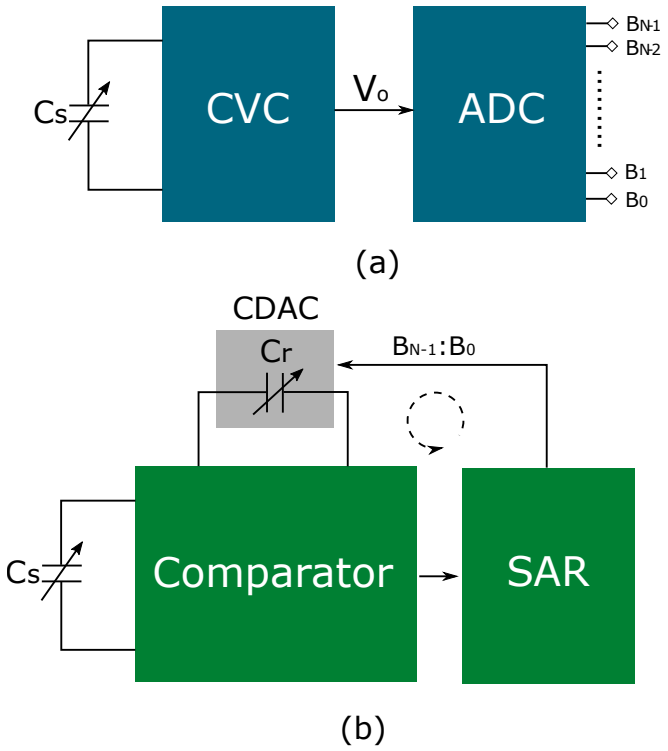


Figure 2.3: ADC-based CDC

Another ADC-related CDC is called a successive-approximation CDC [54, 30], which is shown in Fig. 2.3(b). C_s represents sensor capacitance. C_r is a reference capacitance implemented in a capacitive digital-to-analog converter (CDAC). The comparator compares the capacitance values C_s and C_r. A successive approximation (SAR) is a commonly used technique in an ADC, which can also implements in an CDC. According to the results of the comparison, the SAR keeps sending different digital outputs to CDAC to get different C_r until the values of C_s and C_r matches with each other.

There are some advantages of ADC-based CDCs. ADC techniques are very mature with several modulations such as Discrete-Time $\Delta\Sigma$ modulation [52], Continuous-Time $\Delta\Sigma$ modulation [48], SAR modulation [54], etc. It is very convenient to design CDCs with these existing modulations. However, the ADC

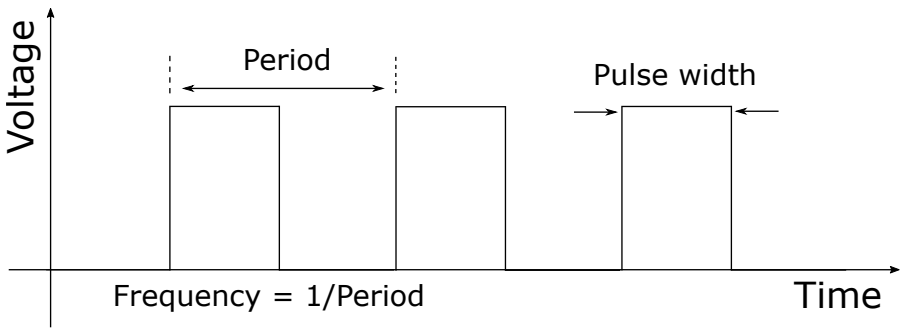


Figure 2.4: Digital waveform

consumes external power and increases the complexity which may lead to high power consumption, slow response time.

2.3.2 *Frequency/Time-based CDC*

This section introduces some examples of frequency/time based CDCs. Fig. 2.4 shows some basic definition in a digital waveform which is related to the work below. The period refers to the duration time taken to complete one cycle in a repeating event. The frequency is the number of repeating cycles in a unit of time, which can be expressed as 1/period. The pulse width is the duration time for a pulse to maintain it's maximum amplitude [9]. The CDCs shown in this section are all based on the theory that the sensed capacitors are in a relation of these factors.

2.3.2.1 *Period Modulation-based CDC*

Fig. 2.5 shows a typical period modulation based CDC. It uses relaxation oscillators [78] that converts the sensed capacitance to a period time. First, φ_1 sets to on and φ_2 sets to off, , as is shown in Fig 2.5(a). The sensed capacitance C_x is charged because it is connected between V_{dd} and a mid-supply common-mode reference V_{cm}. Then φ_1 sets to off and φ_2 sets to on, ,as is shown

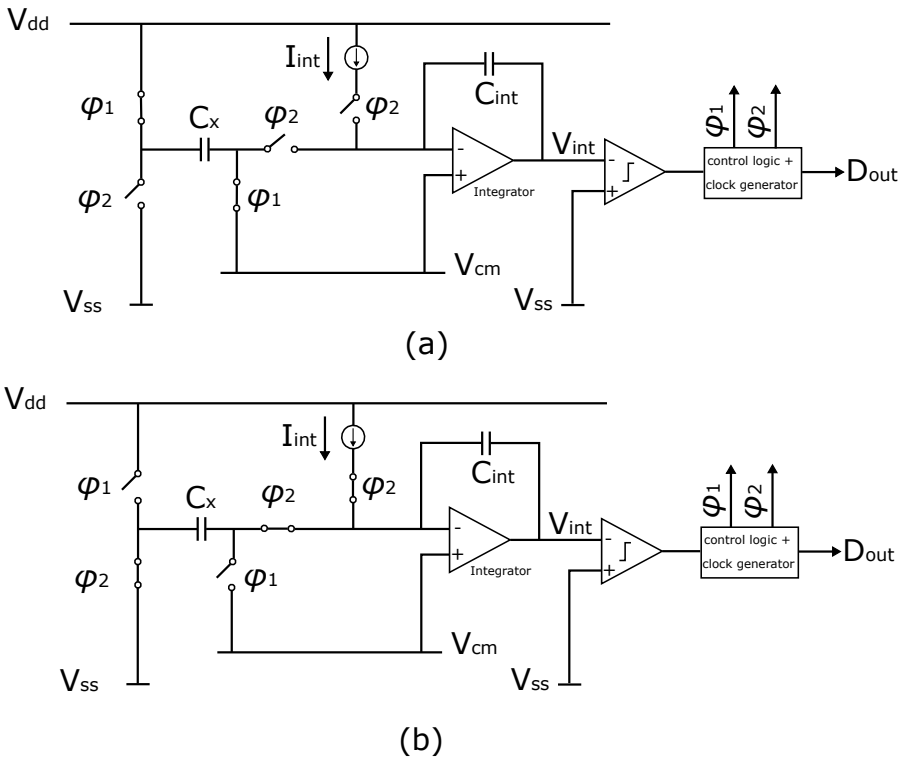


Figure 2.5: Period modulation:(a) φ_1 on,φ_2 off; (b) φ_2 on,φ_1 off [73]

in Fig 2.5(b). C_x is connected between V_{ss} and the virtual ground of an active integrator. The charge from C_x, which is $C_x \times V_{dd}$, is then transferred to an integrated capacitor C_{int}. This causes a step up for the output of the integrator V_{int}. The charge from C_{int} is then removed by a constant integration current I_{int} until V_{int} returns to its original level. This is detected by a comparator at the output of the integrator. The time interval T_{msm} in Fig 2.6, which is the time difference from the start of phase φ_2 until V_{int} crosses the threshold of the comparator, is then proportional to C_x [73, 28]:

$$T_{msm} = \frac{V_{dd}}{I_{int}} C_x \tag{2.2}$$

This means T_{msm} can be used to measure C_x. And by counting the number of cycles of a faster reference clock during this

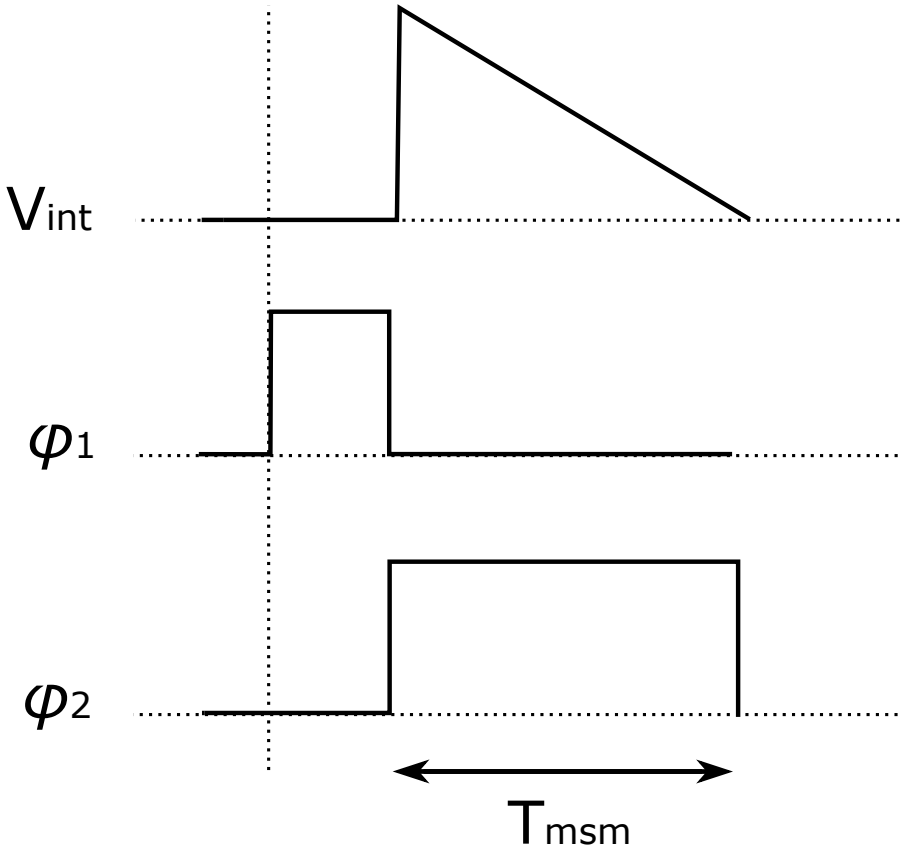


Figure 2.6: Period modulation associated waveforms

period by a digital counter or microcontroller, an output code is then obtained [73, 28].

The advantage of this design is that it is operated asynchronously which means it does not need a clock signal. The input capacitance range can also be very large with high resolution [73]. However, it needs a high quality amplifier to act as an integrator and the constant current source design is a very costly approach which makes the design more complicated.

2.3.2.2 *Pulse width Modulation-based CDC*

Fig. 2.7 shows the block diagram of a pulse width modulation [86, 67] based CDC. As can be seen from Fig. 2.7(a), it includes two CVCs and one voltage-to-pulse width converter (VPwC). The sensed capacitors C_1 and C_2 are from a differential capacitive

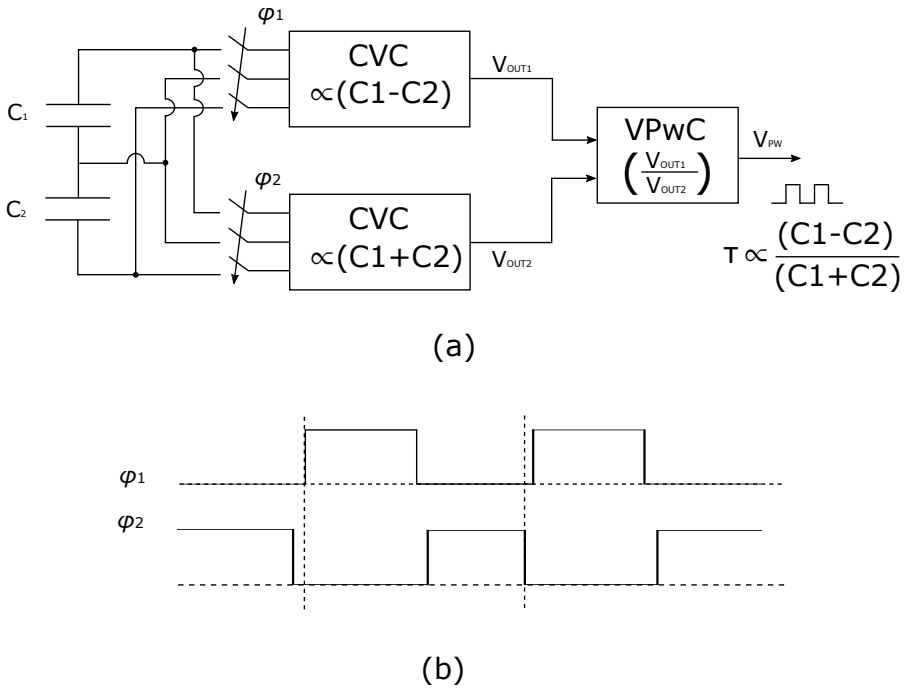


Figure 2.7: Structure of PW [2]

microsensor. φ_1 and φ_2 in Fig. 2.7(b) are two non-overlapping clock phases which act as switches of the corresponding CVCs. The top CVC generates an output voltage V_{OUT1} which is proportional to the difference between C_1 and C_2 (i.e. C_1-C_2), while the bottom CVC generates an output voltage V_{OUT2} which is proportional to the sum of C_1 and C_2 (i.e. C_1+C_2). The VPwC provides a pulse width which is proportional to the ratio of V_{OUT1} and V_{OUT2} (i.e. V_{OUT1}/V_{OUT2}). This means by replacing the value of V_{OUT1} and V_{OUT2} with C_1 and C_2, the output pulse width is proportional to the ratio of the difference to the sum of C_1 and C_2, which is shown below [2]:

$$\tau \propto \frac{C_1 - C_2}{C_1 + C_2} \tag{2.3}$$

The pulse width based CDC may minimize the sensitivity to parasitic capacitances [12, 49, 2] with low power consumptions.

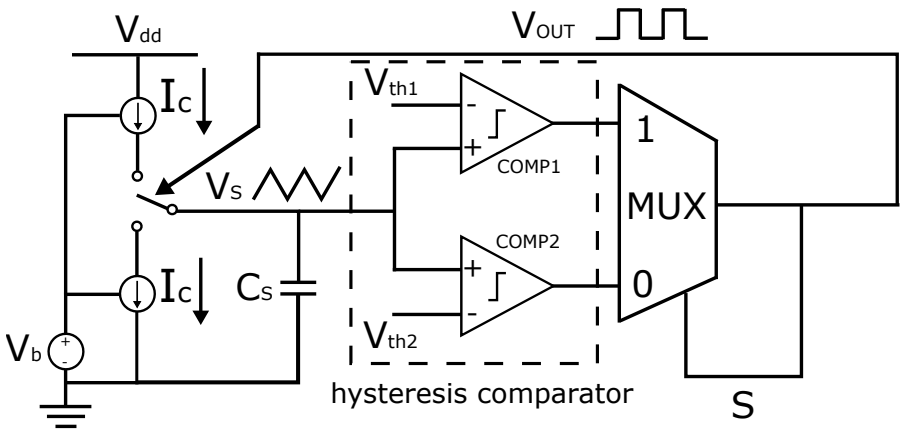


Figure 2.8: Frequency based CDC [22]

However, the performance is affected by the stability of clock signals which may affect the linearity.

2.3.2.3 *Frequency modulation-based CDC*

Fig. 2.8 shows a block digram of capacitance-to-frequency based [8] CDC. The sensed capacitance C_s is charged and discharged with two constant current sources I_c. The output voltage V_{OUT} decides the action of the switch. The hysteresis comparator is designed with two comparators COMP1 and COMP2 with different threshold voltages V_{tr+} and V_{tr-}, which transform the triangle voltage V_s on C_s into a square wave. The outputs of COMP1 and COMP2 are then sent to a multiplexer MUX [43], which has two inputs and a one output fed back to the strobe terminal. Table 2.2 shows the truth table of the multiplexer. If S=0, the output voltage V_{OUT} only depends on the state of input voltage V_{COMP2} and if S=1, the output voltage V_{OUT} only depends on the state of the input voltage V_{COMP1}. In other words, for V_s increasing, the output of the multiplexer is decided by V_{COMP2} and for V_s decreasing, it is decided by V_{COMP1} [22].

The constant current sources are controlled by a bias voltage V_b. C_s is charging when V_{OUT} is low. On the other hand, it

Table 2.2: Truth table of Multiplexer [43]

S	COMP1	COMP2	V_{OUT}
0	X	0	0(COMP2)
0	X	1	1(COMP2)
1	0	X	0(COMP1)
1	1	X	1(COMP1)

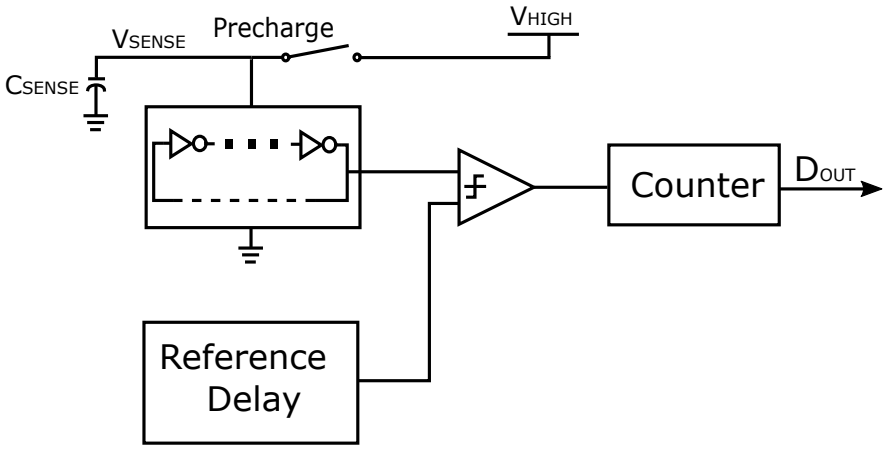


Figure 2.9: Structure of Iterative Delay-Chain Discharge based CDC [32]

is discharging when which charges when V_{OUT} is high. As a result, the frequency of V_{OUT} is a function of C_s. The output frequency can be converted by digital codes with a time-to-digital converter (TDC) and thus can be used as a CDC [22].

This design is suitable for low-voltage low-power capacitance sensor application. However, it suffers from the stability of the oscillator signal [1] and the design of constant current source complicates the design.

2.3.2.4 *Iterative Delay-Chain Discharge based CDC*

Fig. 2.9 shows a basic structure of iterative Delay-Chain Discharge based CDC that uses ring oscillators to transform sensor capacitance into digital outputs. It is based on the theory that when a ring oscillator (RO) [42] uses a charged capacitance as a power supply, the number of RO cycles required to discharge the

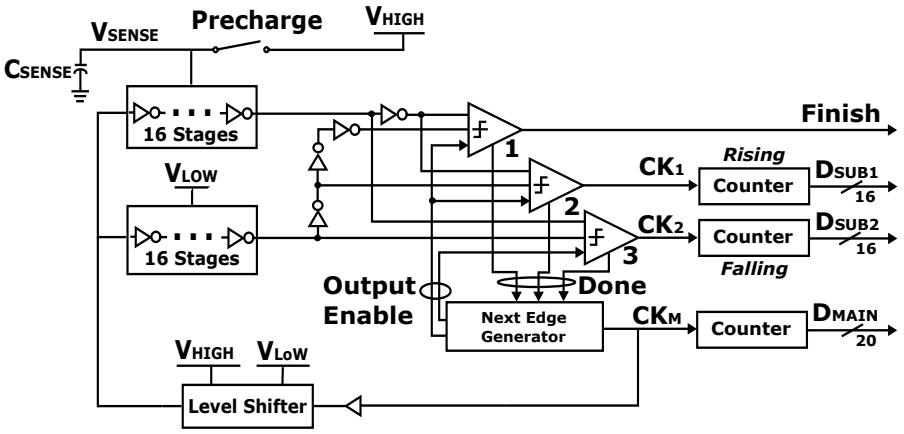


Figure 2.10: Iterative Delay-Chain Discharge based CDC [32]

capacitance to a fixed voltage varies linearly with the capacitance value. This structure basically consists five parts: a capacitance charging/discharging block, a ring oscillator, a reference delay block, a delay comparator and a counter. The sensed capacitor C_{SENSE} is charged to V_{HIGH} by turning the *Precharge* switch on. After C_{SENSE} is fully charged, the *Precharge* switch turns off. The ring oscillator powered by V_{SENSE} then starts oscillating. During the oscillation, the RO draws some charge from C_{SENSE} and gradually lowering V_{SENSE}. As a result, the propagation delay of RO increases gradually. The comparator compares its delay with the reference delay. The counter counts the pulse number of the RO until the propagation delay of RO become longer than the reference delay and outputs the code D_{OUT} [32].

Fig. 2.10 shows the detailed architecture of this CDC. The CDC is built by two 16-stage inverter chains, three comparators, a clock generator, a level shifter and three counters. The circuit is powered by V_{LOW} to save power, except the upper inverter chain. In the first step, the precharge switch is on, V_{HIGH} charges the capacitor. After C_{SENSE} is fully charged, the precharge switch turns off and the second step starts. The two inverter chains which are supplied by V_{SENSE} and V_{LOW} respectively compare their

propagation delay in three comparators. The middle comparator compares their rising edges and the bottom comparator compares their falling edges. After each comparison, the next edge generator triggers the next discharge and delay comparison. The level shifter converts V_{LOW} to V_{HIGH} [32].

As the upper inverter chain is powered by V_{SENSE} from a charged capacitor, which is not an unlimited power source, V_{SENSE} keeps decreasing because the oscillation in the upper inverter chain drains the charge from C_{SENSE}. The top comparator, which takes a slightly delayed version of the reference delay, decides when to pulse a *Finish* signal to stop the overall conversion. The conversion stops when V_{SENSE} becomes lower than V_{LOW} by some margin. The middle and bottom comparators output pulses once only when the propagation delay of the top inverter chain is longer than the bottom inverter chain. The top two counters counts the number of pulses from comparators and output digital codes D_{SUB1} and D_{SUB2}. The bottom counter counts the main oscillation triggering signal and output digital codes D_{main} [32].

Fig. 2.11 shows the waveform of this design. After the capacitance precharge finishes, the *Sense* signal goes high to trigger the oscillation. Before V_{SENSE} falls some margin below the level of V_{LOW} , the next edge generator keeps outputting pulses CK_M. The clock signals CK_1 and CK_2 from the bottom two comparators pulse sporadically, due to noise, and more frequently as V_{SENSE} goes across V_{LOW}. After the *Finish* from the top com-

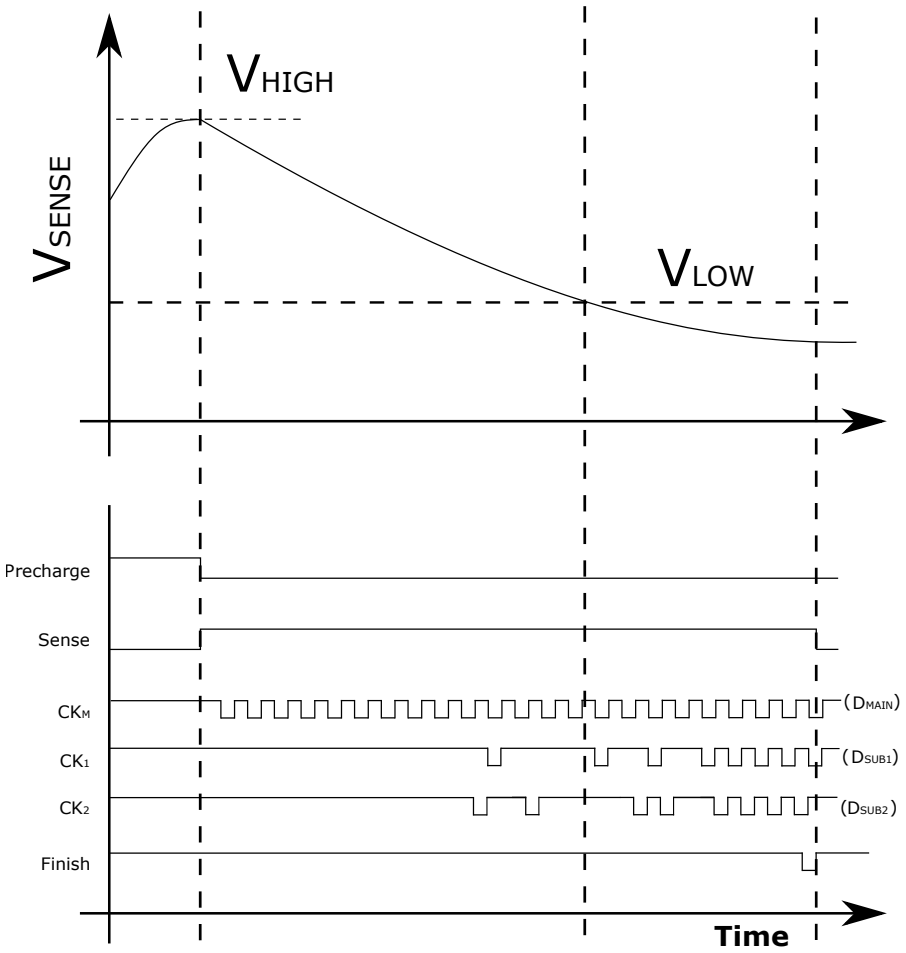


Figure 2.11: Waveform of Iterative Delay-Chain Discharge based CDC [32]

parator pulses, the oscillation stops. The final output code of comparator outputs D_{OUT} is then calculated as [32]:

$$D_{OUT} = 2 \times D_{MAIN} - (D_{SUB1} + D_{SUB2}) \tag{2.4}$$

The reason for using three comparators is to increase the accuracy by averaging noise over many comparisons when V_{SENSE} is closed to V_{LOW}. The number of comparisons is doubled by comparing both rising and falling edges. By extending the oscillation to where V_{SENSE} is lower than V_{LOW} by some margin, comparisons are performed through the whole noise region

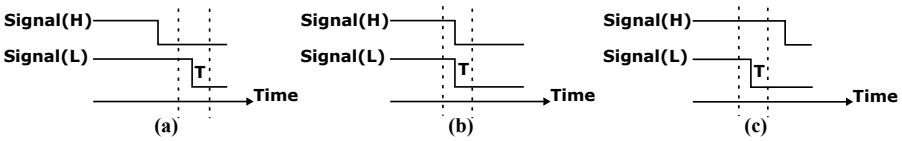


Figure 2.12: Three scenarios [66]

around V_{LOW}. Hence, the false "V_{SENSE}<V_{LOW}" decisions above V_{LOW} and false "V_{SENSE}>V_{LOW} " decisions below V_{LOW} are compensated stochastically. By using the calculation method in Eq. 2.4, the output code D_{OUT} becomes centred at the number of exact counts from V_{HIGH} to V_{LOW}. Thus, the performance of linearity is improved [32].

This design is fully digital, and transforms the sensed capacitance directly into digital codes, which means it does not need complex circuits, such as amplifiers and ADCs. Comparing to conventional CDCs, it consumes less power. As the RO draws sensor capacitance directly from C_{SENSE} without a CVC, the input capacitance range is only limited by the counter size. However, there are still some disadvantages existed as following [66]:

Problem 1: Extra power/Energy for correction. There are three comparators implemented in this design to improve the linearity performance of output code corresponding to the sensor capacitance by using Eq. 2.4 for correction. This results in extra computation and more power/Energy consumption [66].

Problem 2: Accuracy. The errors may happen in the final results. In theory, only one comparator and one counter are needed for detecting the propagation delay when V_{SENSE} goes from V_{High} down to V_{LOW} and count the number of discharging iterations. However, instead of stopping comparison immediately the moment V_{SENSE} becomes lower than V_{LOW}, it uses a complicated method to introduce extra delays to let the comparison stop after V_{SENSE} becomes lower than V_{LOW} by some margin to min-

imize the error. One reason for this design is because of the three scenarios shown in Fig. 2.12 when V_{SENSE} discharges to and close to V_{LOW}. Signal(H) is the output signal of the top inverter chain and Signal(L) is the output signal of the bottom inverter chain in Fig. 2.10. Fig. 2.12(a) represents the state when Signal(H) comes earlier than Signal(L); Fig. 2.12(b) represents the state when Signal(H) and Signal(L) comes very closely; Fig. 2.12(c) represents the state when Signal(H) comes later than Signal(L) [66].

However, even with three comparators and counters, and the correction equation in Eq. 2.4, the signal in the comparator may not be triggered if metastability (This will be explained in section 2.7) happens in the scenario Fig. 2.12(b), which could causes the missing of counts and affects the accuracy of the final result [66].

2.3.3 *Summary of existing CDC techniques*

The above section discussed some existing CDC techniques. Each technique has its own advantages and disadvantages in terms of the trade-off among power consumption, resolution, capacitance range, etc. Table. 2.3 concludes an overview of different CDC techniques in terms of power consumption, capacitance range, resolution, etc. based on other researchers' review on the existing CDC techniques.

2.4 VOLTAGE SENSING

Voltage sensing is also a very important technique for many applications [59, 24]. It transforms a sensed analog dc voltage

Table 2.3: Overview of different CDC techniques

Type	Advantages	Disadvantages
CVC+ADC	Relatively high resolution	Mostly power hungry [23]; Require complex signal conditioning circuits [23]; Require large die area [23]
SAR	Relatively low power consumption [38]; Excellent energy efficiency [53].	Limited capacitance range [40]. Medium resolution [62].
ΔΣ modulation	Very high resolution by virtue of oversampling and noise shaping [53].	Power hungry [40]; Limited in dynamic range due to the fast oversampling clock frequency used [23]
Dual-slope	Simplicity [62].	Low energy efficient [62].
Period /Pulse width modulation	High resolution [48]; Large input capacitance range [73];	Large measurement time[48]; High-resolution time reference decreases the energy efficiency[48]; Time-to-digital converter circuits (TDCs) are required which dissipate significant power [23].
Iterative Delay-Chain Discharge	High capacitor range; Relatively low power consumption [62].	Need extra correction limited resolution [66]; Not suitable for sensing small capacitors despite its wide sensing range [62].

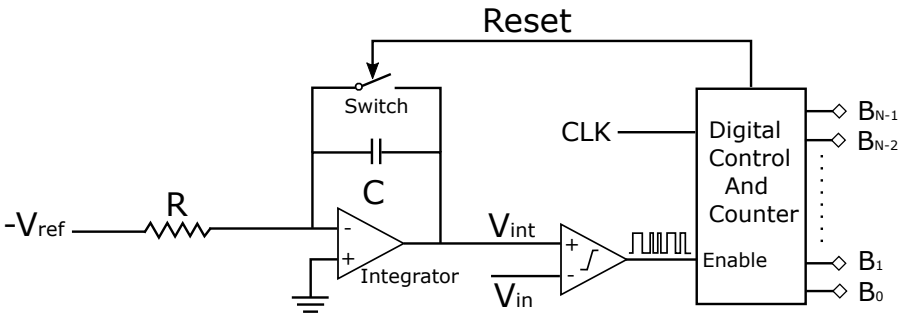


Figure 2.13: Single slope ADC [51]

into digital signals. This section introduces two techniques for the voltage sensing.

2.4.1 *Reference-based Voltage Sensing*

The most commonly used voltage sensing technique is the ADC. The ADC compares the input voltage V_{in} with a known reference voltage V_{ref} and generates a digital code corresponding to the V_{in} [37, 19, 51, 24].

Fig. 2.13 shows a typical single slope ADC also known as an integrating ADC. The integration starts when V_{ref} inputs to the integrator and outputs the integrated voltage V_{int}. V_{int} is then compared against V_{in} by the comparator until V_{int} equals to V_{in}. The time it takes during the comparison is then encoded. The time encoded pulse then inputs to the counter as an enable signal which triggers the counter to count to a digital value which representing the time information. A digital control block controls the operation of the ADC. It resets the integrator after a set number of clock cycles elapse to make sure that there is enough conversion time for the counter to count the highest value which representing the full-scaled input voltage [51].

The disadvantage of the single slope ADC is that the accuracy is dependant on the integrator. The accuracy of the integrator is

also affected by the value of C and R. Even a slightly change of these parameters will completely affect the results [51].

2.4.2 *Reference-free Voltage Sensing*

In the energy harvesting (EH) system, the harvested energy may provide a low and unstable power supply. The introduced dynamic voltage sensing mechanism can sense the unstable voltage without a reference voltage [24].

Fig. 2.14 shows the block diagram of the wideband dynamic voltage sensing mechanism. The voltage controlled oscillators (VCO) transform the input voltage V_{in} into the time domain, which is the frequency T_c. The top delay block generates a delayed frequency T_{up} to compare against T_c with the top time comparator to detect the voltage rising and generate an up event when the voltage increases by a sensing resolution Δv. If sensing starts at V_0, the voltage in the i^{th} step of an up event can be calculated as $V_0 + i\Delta v$, if there is no down events happened [24],

The same thing happens in the bottom delay block and time comparator. The only deference is that it detects the voltage falling by comparing the delayed frequency T_{down} against T_c and generates the down events [24].

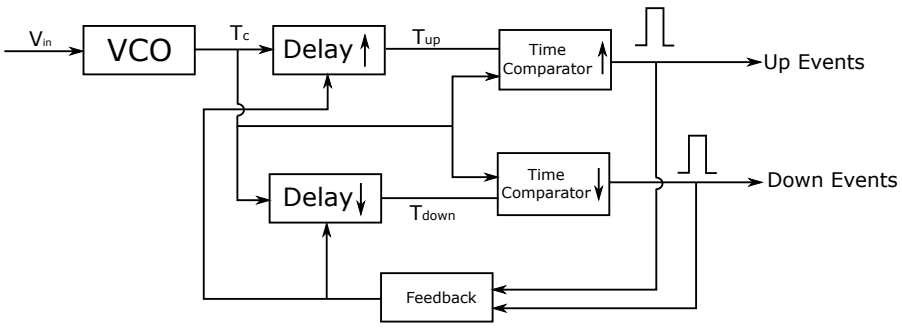


Figure 2.14: Reference-free voltage sensing mechanism [24]

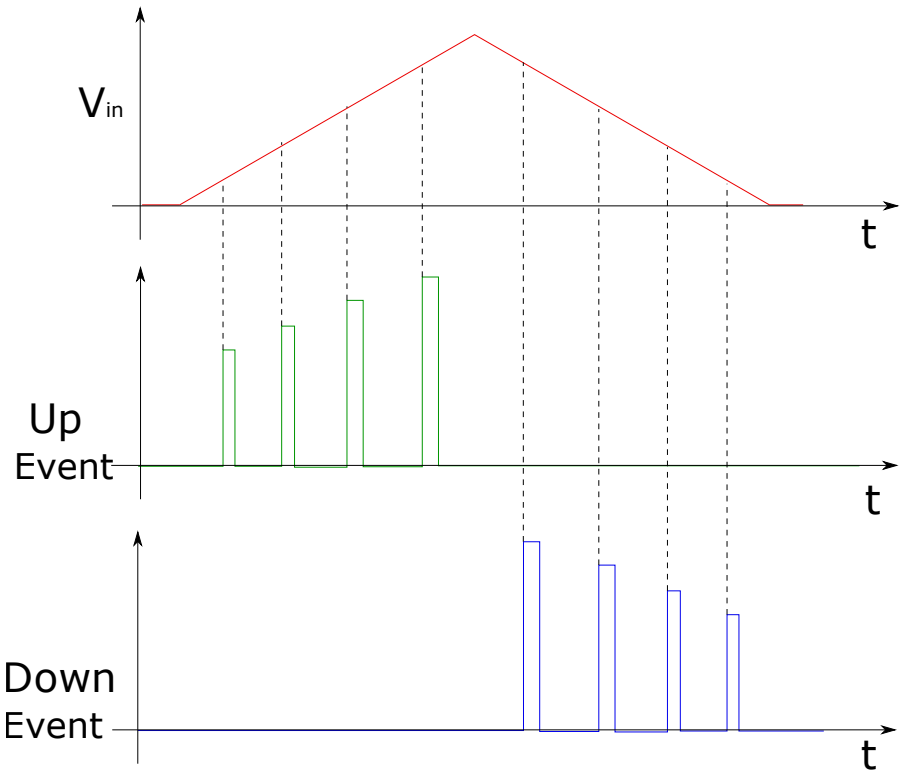


Figure 2.15: Voltage tracking [24]

Either an up event or a down event triggers the next round of sensing by the feedback block until the system powers off, which can be seen in Fig. 2.15. The input voltage V_{in} thus can be calculated by counting the number of the events [24].

This voltage sensing technique can track or sense unstable voltage without a reference voltage. However, there is a trade-off between the resolution and power consumption. The resolution depends on the value of Δv. For higher resolution, a smaller Δv is needed, which increases the number of events. This means more comparison are required and it consumes more power in a result. If you want to decrease the power consumption, then the resolution are sacrificed.

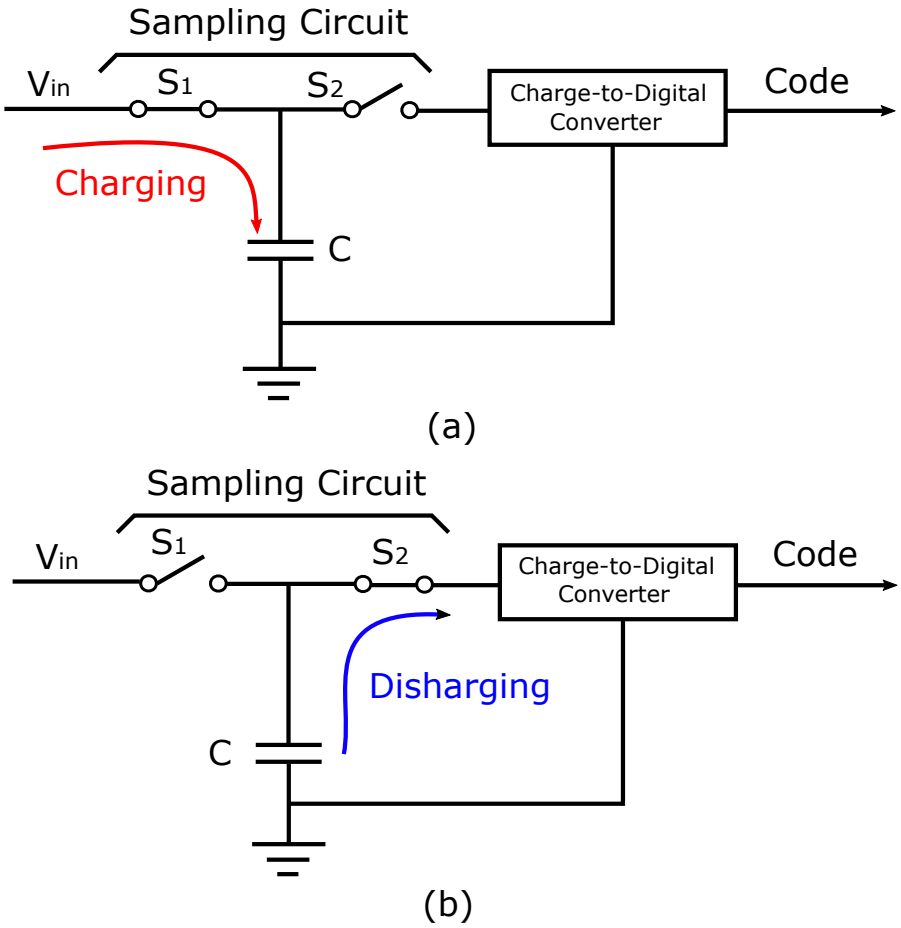


Figure 2.16: Charge-to-Digital Conversion: (a) Charging process; (b) Discharging process[60]

2.4.3 *Summary of existing voltage sensing techniques*

The above section introduced the reference-based/reference-free voltage sensing techniques. Table. 2.4 concludes an overview of different voltage sensing techniques in terms of power consumption, voltage range, etc. based on other researchers' review on the existing voltage sensing techniques.

Table 2.4: Overview of different voltage sensing techniques

Type	Advantages	Disadvantages
ADC	Most widely used to convert voltage to digital outputs	Requires a stable reference voltage which consumes more energy; Relatively high power consumption [51].
Power-on set	May not need a stable reference voltage but can be created from inherent properties of CMOS technologies which results in low power consumption [24, 65].	inherent references highly rely on circuit structures [24].
Charging and discharging a sampling capacitor	Fully digital; Low power consumption [24].	relatively long response time [24].
SRAM+inverter chain	Reference free; Detect huge range of supply voltage [35]; High accuracy [24]; Fast response time [24].	the circuit area is relatively large which may increase power consumption [24].

2.5 CHARGE TO DIGITAL CONVERTER

A charge-to-digital converter (QDC) is used to convert the amount of charge stored in a capacitor to a binary output code. Fig. 2.16 shows a system overview of a charge-to-digital conversion. A capacitor is used to transform an input voltage V_{in} into a certain amount of energy contained in the form of a charge stored on this capacitor. A QDC provides reliable conversion of the stored energy to a binary code on the output [60]. This is realized in two steps. Fig. 2.16(a) shows a first step, which is the capacitor charging process. The sampling circuit turns the switch S_1 on and switch S_2 off. The capacitor will then be charged to V_{in}. In the second step shown in 2.16(b), after the capacitor is fully charged, the switch S_1 turns off and switch S_1 turns on. This results in a capacitor discharging process. The energy stored in the capacitor will then be converted to a binary code by a QDC [60].

The code number depends on the charge stored in the capacitance. As can be seen in Eq. 2.5 below [74, 10], different values of C and V affect the amount of charge Q, in other words, changes the output code. Hence a QDC can either be used as a CDC to sense capacitance under a fixed input voltage, or be used as a voltage sensor to sense voltage under a fixed input capacitance. The detailed explanation will be found in chapter 3.1.

$$Q = C \times V \tag{2.5}$$

Where,

Q is the stored charge in coulomb(C),

C is the capacitance in farads(F),

V is the voltage cross the capacitor in volts(V).

Unlike a conventional CDC which needs an external power supply to sense the capacitance, in a QDC system, the stored energy from the capacitance is not wasted and can be used to power the circuit, which simplifies the design and saves power.

2.6 RING OSCILLATOR

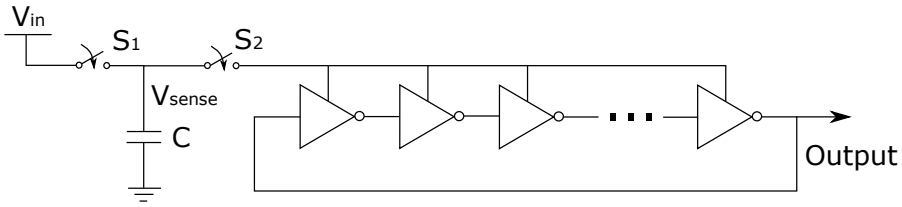


Figure 2.17: Ring oscillator powered by capacitor[59]

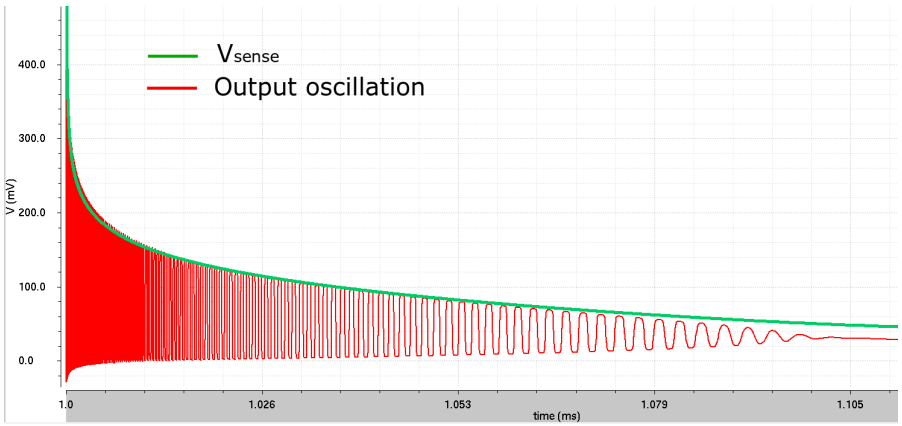


Figure 2.18: Ring oscillator discharging

Fig .2.17 shows a capacitor discharging through a ring oscillator. The ring oscillator is made of an odd number of inverters to produce the oscillation [42]. In step one, the switch S_1 is on and S_2 is off. The capacitor C is then be charged to the input voltage V_{in}. After the capacitor is fully charged, the second step

begins. The switch S_1 turns off and S_2 turns on. The voltage V_{sense} on the capacitance starts to power the ring oscillator. The ring oscillator powered by higher voltage produces higher oscillation frequency. Thus, the oscillation frequency is high in the beginning when V_{sense} is high. Then, every step of oscillation draws some energy from the capacitor. As a result, V_{sense} becomes lower. Thus, oscillation frequency becomes lower. The simulation results of the output oscillation is shown in Fig. 2.18. It clearly shows that the oscillation draws the energy from the capacitance, which decreases V_{sense}. In return, V_{sense} keeps decreasing and slowing the oscillation. In the end, the energy runs out and the oscillation stops [59].

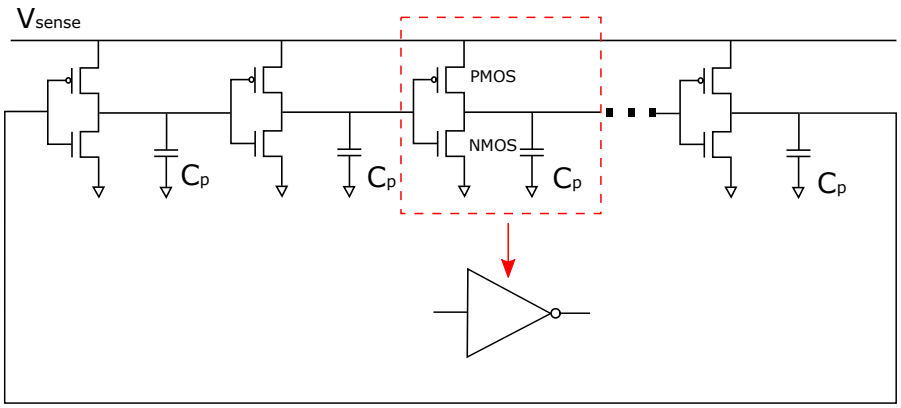


Figure 2.19: Schematic of inverters

Fig. 2.19 shows the schematic of inverters in the ring oscillator. An inverter includes a p-type metal-oxide-semiconductor (PMOS) transistor, a n-type metal-oxide-semiconductor (NMOS) transistor and a parasitic capacitor C_p. Fig. 2.20 shows the simplification of charging and discharging process in an inverter. When the input is low (i.e. logic '0'), the PMOS is on and NMOS is off. The output becomes high (i.e. logic '1') and V_{sense} charges C_p through PMOS. In contrast, when the input is high (i.e. logic '0'), the PMOS turns

off and NMOS turns on. The output becomes low (i.e. logic '0') and C_p is discharged through NMOS [59].

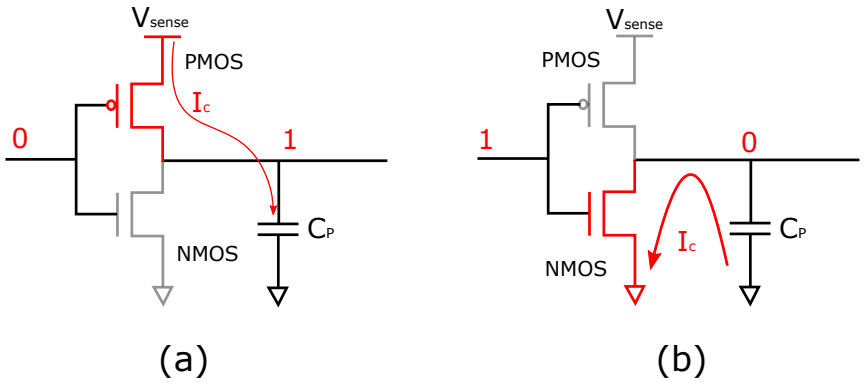


Figure 2.20: Transistor switching

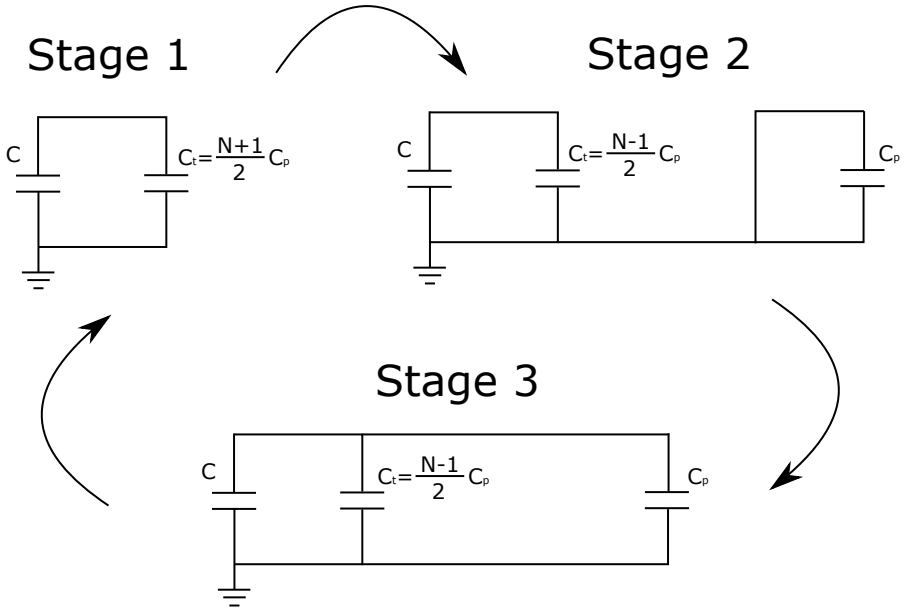


Figure 2.21: The operation of the ring oscillator[82]

The operation of the ring oscillator with N inverters can be explained in three stages shown in Fig.2.21. Stage 1 represents the situation when C is just connected to the ring oscillator. In this state, no switching action has been fired. In other words, no charging or discharging action takes place. In this initial state, the output of each odd numbered inverter is at logic '1', which means (N+1)/2 of C_p are charged to the voltage level equal to

that of C. The output of rest inverters is at logic '0' and their corresponding C_p are empty. Stage 2 represents the state that a switching occurs. The output of one of the odd numbered inverter is supposed to switch from 1 to 0. Its corresponding C_p is gradually discharged. The state of the remaining inverters stays the same as in stage 1. No energy transfers from C in this stage. In stage 3, the discharged C_p associated with the next inverter which is supposed to switch from 0 to 1 begins to receive charge from C. This is the only state that draws energy from C [59]. These three stages keep repeating until the energy in C is empty.

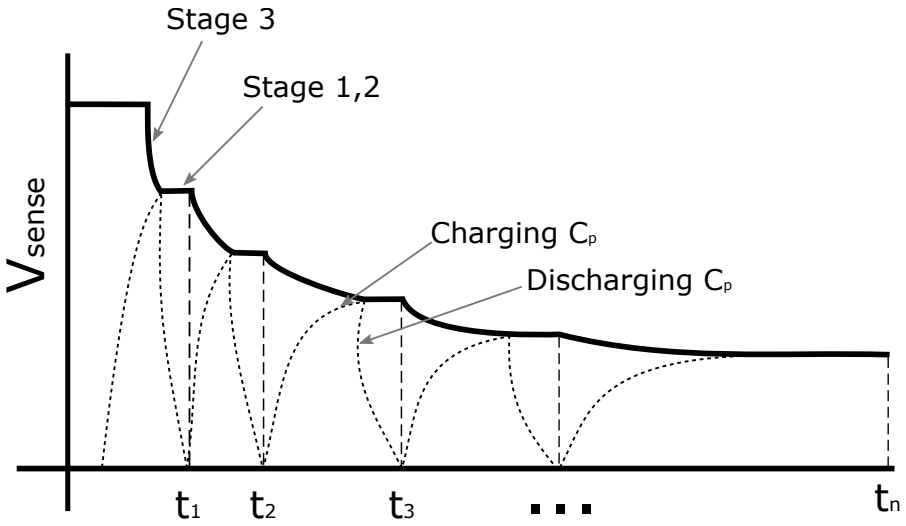


Figure 2.22: V_{sense} drop over time [59]

Fig. 2.22 shows the process of V_{sense} dropping over time. V_{sense} represents the voltage across C. Hence, as explained before, V_{sense} drops only in stage 3 and t_n is a function of V_{sense}.

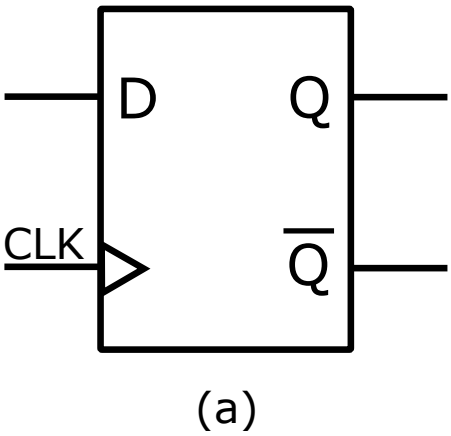
2.7 METASTABILITY FILTER

2.7.1 *Definition of Metastability*

In a digital circuit system, the digital signals should be either logic '0' or '1' within certain voltage to operate the circuit correctly. In certain situations, it is possible for a signal to have an equilibrium point with a voltage which is somewhere in between those corresponding to logic '0' and logic '1'. For instance, if logic '0' corresponds to 0V and logic '1' corresponds to 1V, a circuit may have an equilibrium at around 0.5V. The state of a signal being in such an equilibrium point is known as metastability because such equilibriums are not stable. The metastability may cause loss of data. In the worst case scenario, if a metastable output is continuously interpreted as random '0' or '1' by different subsequent logic stages, it may cause system failure [47, 69, 15].

The metastability mostly happens in a flip flop or latch. When the active edge of the clock and the transition of data signal arrive at the same time (or sufficiently close) [7], the time difference between them becomes smaller than the clock setup time t_{su} or hold time t_h of the signal. [15, 69]. The latching circuit may fall into a non-logic '0' and non-logic '1' equilibrium, which although unstable, would persist for an non-determinant amount of time.

Take the operation of a D flip-flop as an example. Fig. 2.23 shows the symbol of a D flip-flop and the corresponding truth table. The D flip-flop has two inputs which are signal 'D' and the clock 'CLK'. If the rising edge of 'CLK' is not triggered, the



CLK	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

(b)

Figure 2.23: D flip-flop and the truth table

output Q remains its previous state; If 'CLK' becomes logic '1', then 'Q' becomes the same logic as input 'D' [8].

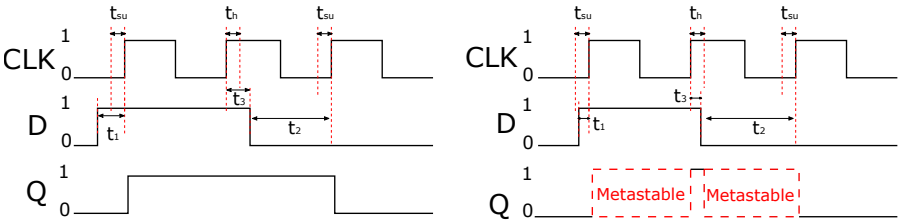


Figure 2.24: Timing diagram of D flip-flop (a) Normal state; (b) Metastable state

Fig. 2.24(a) shows the time diagram of a D flip-flop in a normal state. Before the 'CLK' rises, a certain time is needed that the input 'D' can not change. That time is called setup time, t_{su}. The same, after 'CLK' rises, another certain time is needed during which the input 'D' need to be stable as well. That time is called hold time, t_h. In this case, $t_{su} < t_1$ and t_2 ; $t_h < t_3$. This makes sure that the D flip-flop can operate correctly and outputs a stable 'Q'. However, Fig. 2.24(b) shows a metastable state. In this scenario, sometimes the two inputs 'CLK' and 'D' are triggered almost at the same time, where $t_{su} > t_1$ and $t_h > t_3$. The metastable state then may happen during transition. The consequence is that the D flip-flop does not have enough

time to stabilize the signal. The output 'Q' becomes unstable, which means random '0' and '1' will be triggered.

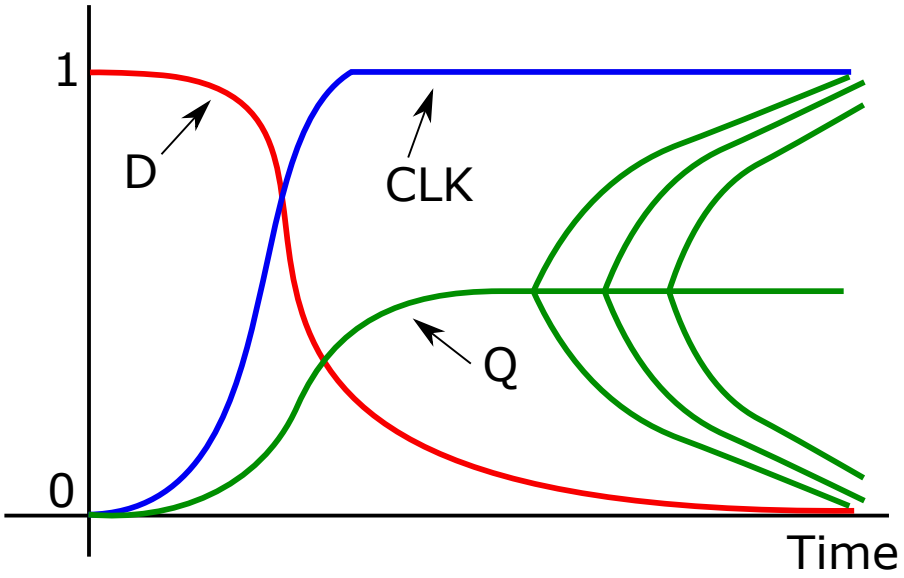


Figure 2.25: Detailed timing diagram of metastable state [47]

Fig. 2.25 shows the metastable state happened in 2.24(b) in detail. Assuming that 'Q' is set to logic '0' initially and 'D' just becomes logic '1'. When 'CLK' is triggered and at the same time, 'D' is becoming '0' again. 'Q' should start rising but may get stuck in the middle of logic levels because it detects the falling of 'D'. Should 'Q' keep rising to '1' or falling to '0'? In fact, either decision is correct. However, in this case, the D flip-flop becomes unstable. During this time, 'Q' may persist in the metastable equilibrium of '0.5' for an non-determinant amount of time before settling randomly either to '0' or '1'. The time it takes 'Q' to become a valid logic value is theoretically unbounded. In this metastable state, 'Q' inputs to the different subsequent logic stages and may be interpreted as random '0' or '1'. This could cause operation errors of the circuit and eventually cause system failure [47].

2.7.2 *Mutual Exclusion*

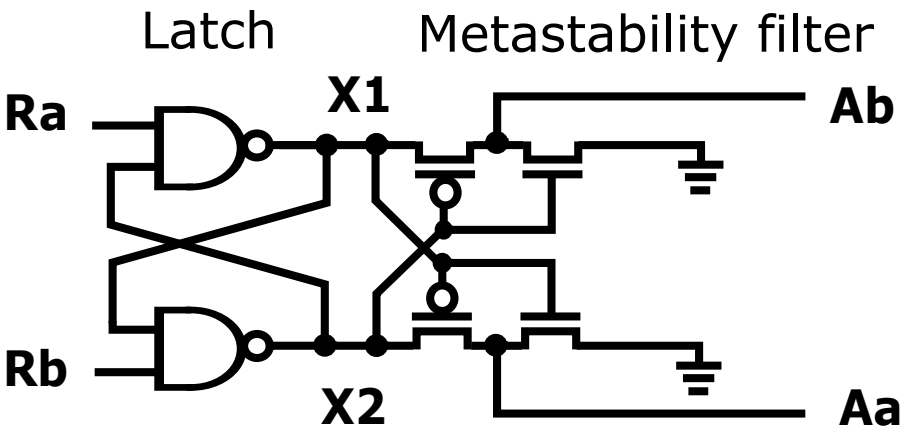


Figure 2.26: The mutual exclusion element [69]

Metastability is an obvious problem with MUTEX elements because these are designed for arbitrating asynchronously arriving signals, for which 'conflicting signals arriving at the same time' is a standard operation state. A MUTEX element therefore must contain methods of resolving metastability. One way of doing this is to add a metastability resolver or filter to a standard SR latch, in the scheme shown in Fig. 2.26. 'Ra' and Rb' are input signals with independent timing. 'Aa' and 'Ab' are the outputs of the MUTEX. The NAND gate latch enables one input to block the other. The task of the MUTEX is to pass 'Ra' and Rb' to their corresponding outputs 'Aa' and 'Ab' in such a way that at most one output is active at any given time. If one input arrives well earlier than the other, the corresponding output is then granted and the latter input signal is blocked until the first arrived signal is de-asserted. When the two inputs arrive at the same time, the circuit may fail to immediately resolve which one comes first, leading to metastability. In this scenario, both 'X1' and 'X2' have voltages about half way between those of V_{dd} and ground. The metastability filter prevents these undefined values to propagate

to the outputs. 'Aa' and 'Ab' are both kept low until 'X1' and 'X2' differ by more than a transistor threshold voltage in the metastability filter [69]. Hence, the metastable state does not propagate outside the MUTEX when it is happening and the output only moves after metastability has settled.

2.8 SUMMARY

This chapter provides a background and literature review of capacitive and voltage sensing techniques. Capacitive sensors are widely used in modern life. In a capacitive sensing system, the CDCs are commonly used in capacitive sensing systems as sensor interfaces. The ADC-based CDCs are reviewed briefly. These CDCs require complex analogue circuits which increase design complexities and power consumption. Several Frequency/Time-based CDCs based on different methods including period modulation, pulse width modulation, frequency modulation and iterative delay-chain discharge method are then summarized. These CDCs are semi-digital or fully digital, which often consume less power but the measurement time usually needs to be improved. Moreover, the voltage sensing systems with/without reference voltages are presented. The principles of the charge-to-digital conversion system is summarized as well. The QDC does not need external power supply and can be implemented as either a capacitive sensor interface or a voltage sensor interface. In addition, the operation of capacitor discharging through a ring oscillator are explained. The process is in fact charging and discharging the parasitic capacitors in the oscillator. Finally, the issue of metastability is discussed. The metastability mostly happens in a flip flop or latch and may cause system failure. A

MUTEX element within a metastability filter inside makes sure the metastable state does not propagate outside the MUTEX and the output only moves after metastability has settled.

3

GENERAL THEORY AND ALGORITHM

3.1 MATHEMATICAL THEORY

This section shows the steps of improvement and simplification from a RC discharging circuit to a fully digital QDC.

3.1.1 *RC discharging circuit*

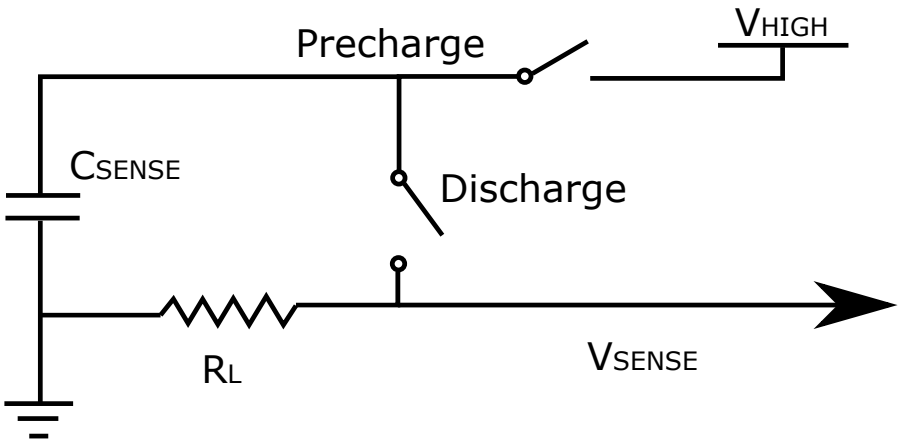


Figure 3.1: A simple RC discharging circuit

Fig. 3.1 shows a simple RC discharging circuit. It contains a power source V_{HIGH}, a sensed capacitor C_{SENSE}, a load resistor R_L and two switches which control the charging and discharging of C_{SENSE}. First, the switch 'Precharge' turns on while the switch 'Discharge' is off. C_{SENSE} is then charged gradually to the level of V_{HIGH}. Once it is fully charged, the switch 'Precharge' turns off and the switch 'Discharge' turns on. C_{SENSE} is then discharged

gradually through R_L. The discharging equation is shown below according to [9, 21]:

Firstly, we have:

$$I = -\frac{dQ}{dt} \tag{3.1}$$

As we know:

$$V = IR, Q = CV \tag{3.2}$$

By replacing I and Q in Eq. 3.1, we can have:

$$\frac{V}{R} = -C\frac{dV}{dt} \tag{3.3}$$

After rearranging, we can get:

$$\frac{dV}{V} = -\frac{1}{RC}dt \tag{3.4}$$

By integrating Eq. 3.4, we have:

$$\int \frac{dV}{V} = -\int \frac{1}{RC}dt \tag{3.5}$$

Then:

$$\ln V = -\frac{t}{RC} + A \tag{3.6}$$

$$V = e^{-\frac{t}{RC}+A} \tag{3.7}$$

$$V = e^{-\frac{t}{RC}} \cdot e^{A} \tag{3.8}$$

$$V = V_0 \cdot e^{-\frac{t}{RC}} \tag{3.9}$$

Where V is the voltage across the capacitor and V_0 is the initial voltage.

Hence, in this specific case, we can have:

$$V_{SENSE} = V_{HIGH} \times e^{-\frac{t}{RC}} \tag{3.10}$$

where,

v_{sense} is the voltage across C_{SENSE} (V),

v_{high} is the supply voltage (V),

e is Euler's number equal to 2.718281828459,

t is the elapsed time since the removal of the supply voltage,

RC RC is the time constant of the RC discharging circuit.

Then we can have,

$$\frac{V_{SENSE}}{V_{HIGH}} = e^{-\frac{t}{RC}} \tag{3.11}$$

Then,

$$\ln \frac{V_{SENSE}}{V_{HIGH}} = -\frac{t}{RC} \tag{3.12}$$

Finally, we can get,

$$\frac{t}{C} = -R \times \ln \frac{V_{SENSE}}{V_{HIGH}} \tag{3.13}$$

When C discharges from V_{HIGH} to a fixed low voltage V_{LOW}, then,

$$\frac{t}{C} = -R \times const. \tag{3.14}$$

Then we can see that for a capacitance discharging from a fixed V_{HIGH} to a fixed V_{LOW}, the time it requires 't' is linear to the value of C. As is shown in Fig. 3.2, after fully charge to V_{HIGH}, the larger C is, the longer time it takes to discharge to V_{LOW}.

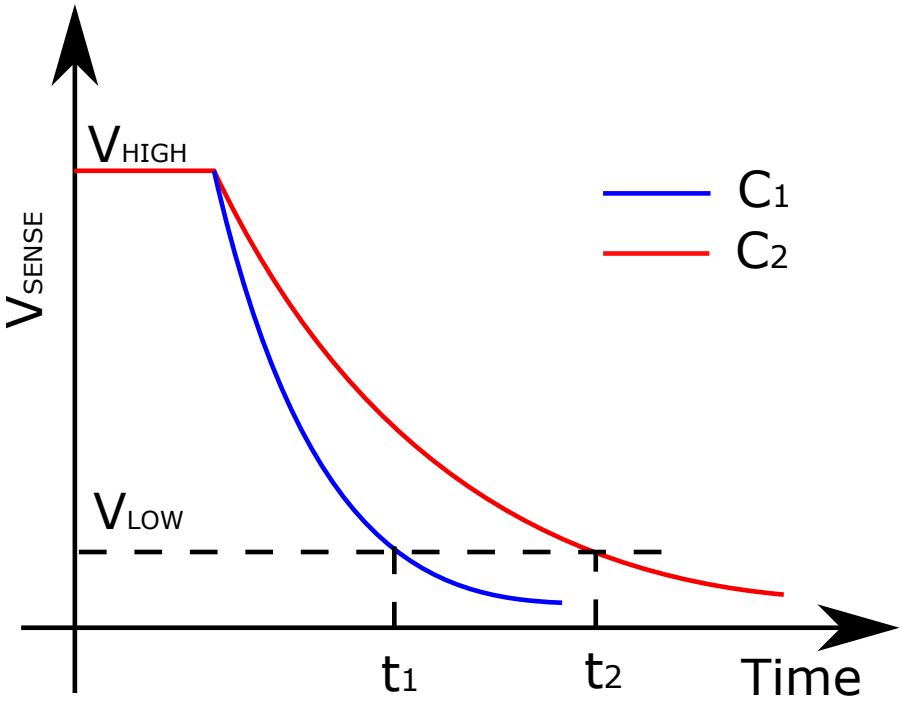


Figure 3.2: RC discharging time

3.1.2 *RC load CDC*

Fig. 3.3 shows a simple RC load based CDC. It contains an RC discharging circuit, a comparator and a counter. The sensed

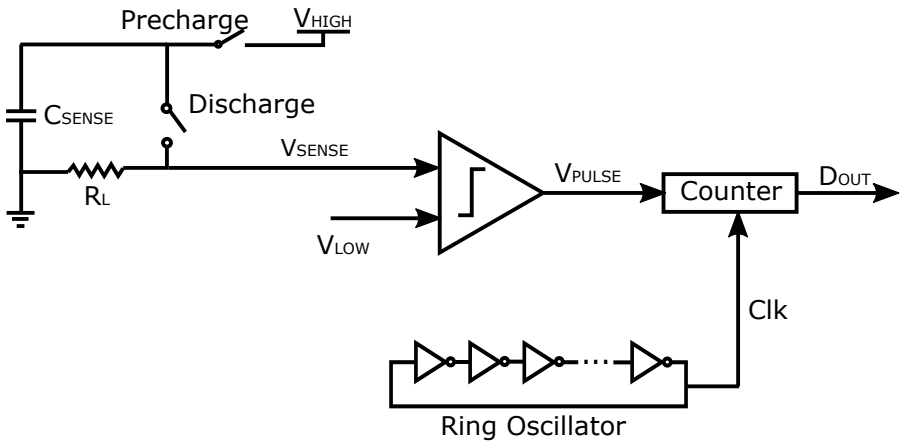


Figure 3.3: RC load QDC

capacitor C_{SENSE} is charged by the power supply V_{HIGH} when the switch 'Precharge' is on and switch 'Discharge' is off. After C_{SENSE} is fully charged, the switch 'Precharge' turns off and switch 'Discharge' turns on. C_{SENSE} starts to discharged through the load resistor R_L. V_{SENSE} is the voltage across C_{SENSE} while the discharge process. During C_{SENSE} discharging, V_{SENSE} is compared with the reference voltage V_{LOW} by a comparator and the counter with a ring oscillator keeps generating a clock signal. When V_{SENSE} drops to the same level as V_{LOW}, the comparator pulses a signal V_{PLUSE}. By counting the cycles of the clock signal from the beginning to the time when V_{PLUSE} triggers, we can get a digital code D_{OUT}. Fig. 3.4 shows the signal performance during the discharging process. Thus, D_{OUT} represents the value of C_{SENSE}. This is based on the fact that T_{PULSE}, which is the time taking for V_{SENSE} to drop to V_{LOW}, is proportional to the value of C_{SENSE}, which is shown below [32]:

As we know,

$$I_{SENSE} = C_{SENSE}\frac{dV_{SENSE}}{dt} \tag{3.15}$$

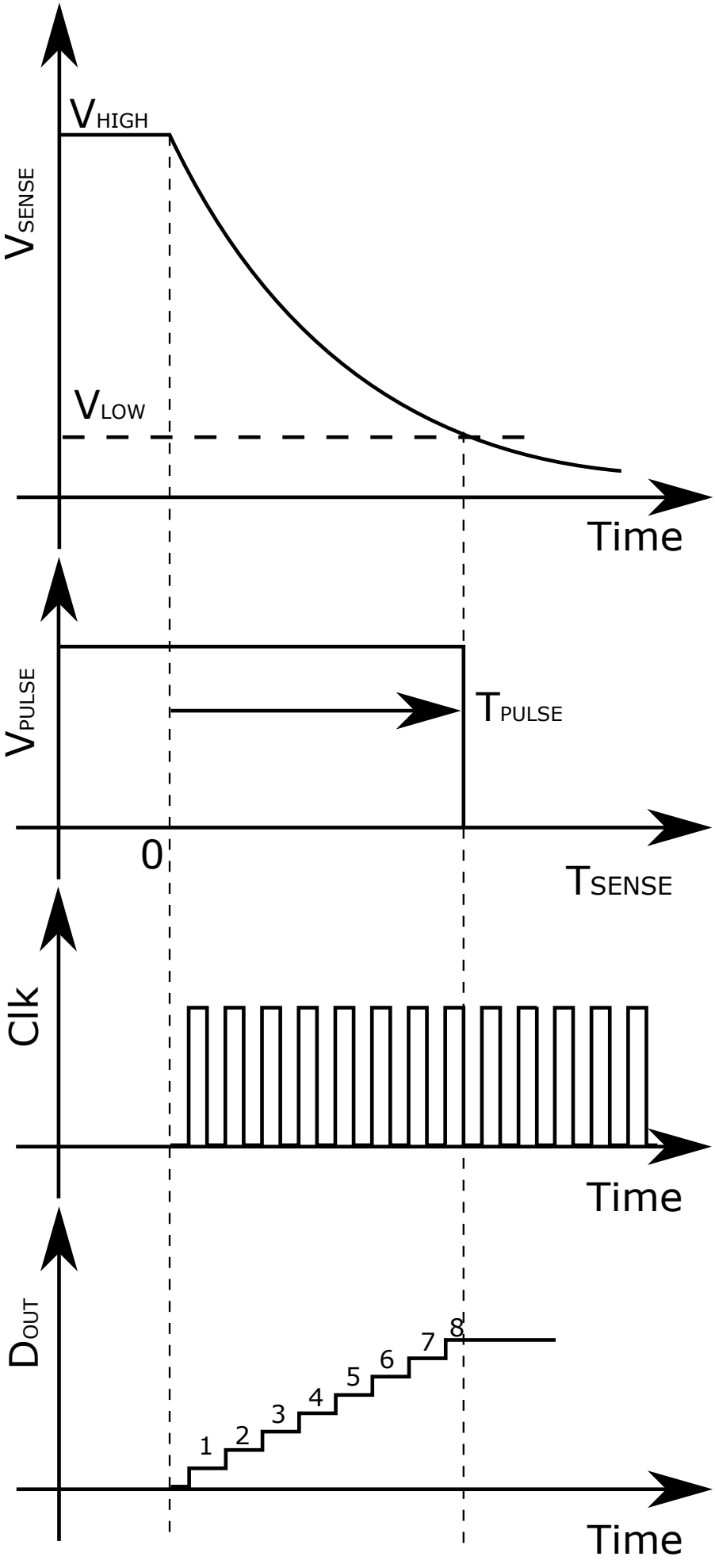


Figure 3.4: Signal performance during the discharging process [32]

Then we can have

$$\frac{dV_{SENSE}}{dt} = \frac{I_{SENSE}}{C_{SENSE}} \tag{3.16}$$

Then

$$dt = \frac{C_{SENSE}}{I_{SENSE}} dV_{SENSE} \tag{3.17}$$

According to Fig. 3.4

$$T_{PULSE} = \int_0^{T_{SENSE}} dt = \int_{V_{HIGH}}^{V_{LOW}} \frac{C_{SENSE}}{I_{SENSE}} dV_{SENSE} \tag{3.18}$$

Then we have

$$T_{PULSE} = C_{SENSE} \times \int_{V_{HIGH}}^{V_{LOW}} \frac{1}{I_{SENSE}} dV_{SENSE} \tag{3.19}$$

According to Eq. 3.19, we can say that T_{PULSE} is proportional to C_{SENSE}. Hence, a larger C_{SENSE} refers to a longer T_{PULSE}, as is shown in Fig. 3.5, where C_1 and C_2 are two sensed capacitors and $C_1 < C_2$. C_1 and C_2 are both charged to V_{HIGH} first and discharges to V_{LOW}. Thus, $T_{PULSE1} < T_{PULSE2}$. This means D_{out} of C_1 is smaller than it of C_2.

3.1.3 *Ring oscillator load QDC*

In Fig. 3.3, a ring oscillator is used to provide a clock signal to the counter. In fact, this ring oscillator can also act as a discharge

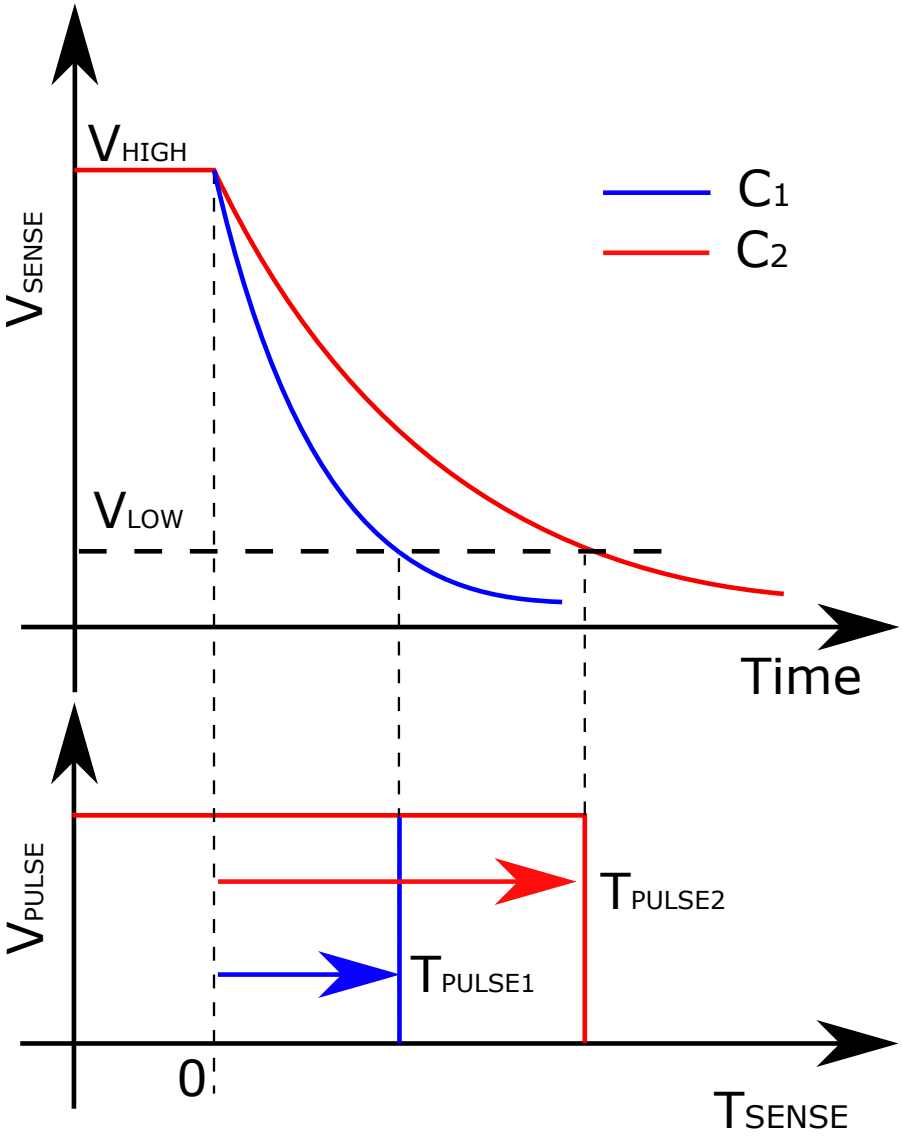


Figure 3.5: Signal performance during the discharging process [32]

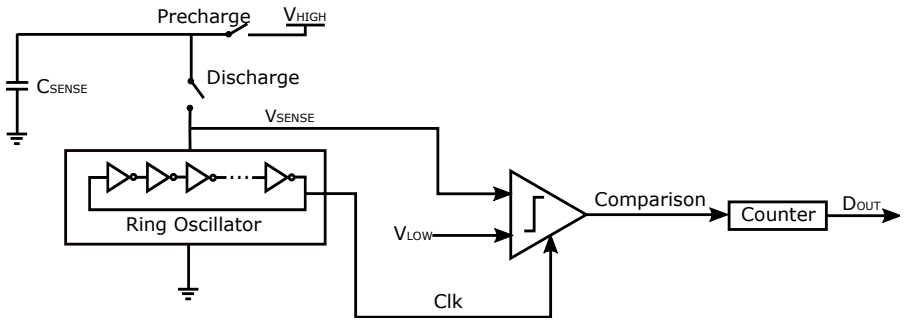


Figure 3.6: RC load replaced by ring oscillator [32]

circuit and thus can replace the load resistor. When using a resistor as a load, V_{SENSE} is only considering as a signal while the energy in C_{SENSE} is not used by the conversion circuit. By replacing the load resistor with the ring oscillator, V_{SENSE} can act not only as a signal, but also as a voltage source of the ring oscillator, and the energy in C_{SENSE} is used by the conversion process. In this way, it reduces the circuit complexity as well as the power consumption. Fig. 3.6 shows the simplified circuit. As can be seen, the load resister is removed and the ring oscillator takes its place. The clock signal is generated by the ring oscillator as an input to the comparator. The counter counts the output of comparator instead of Clk. In the discharging process, The output of each signal is shown in Fig. 3.7. As can be seen, V_{SENSE} drops step by step instead of a smooth dropping curve shown in Fig. 3.4. This is because the parasitic capacitance is charging and discharging in the inverters of the ring oscillator, which is described in section 2.6 in the background chapter. The output of the comparator keeps oscillating until V_{SENSE} drops to V_{LOW}. By counting how many cycles there are, we can generate D_{OUT} by the counter.

3.1.3.1 *Sensing Capacitance*

Fig. 3.8 shows the capacitance to digital discharge process. At step i, Q_i will be $C_{SENSE} \times V_i$, and at step i+1, Q_{i+1} will be $C_{SENSE} \times V_{i+1} + C_p \times V_{i+1}$ where C_p is the parasitic capacitance of the circuit (i.e. the inverter chain) onto which the charge on C_{SENSE} is discharged.

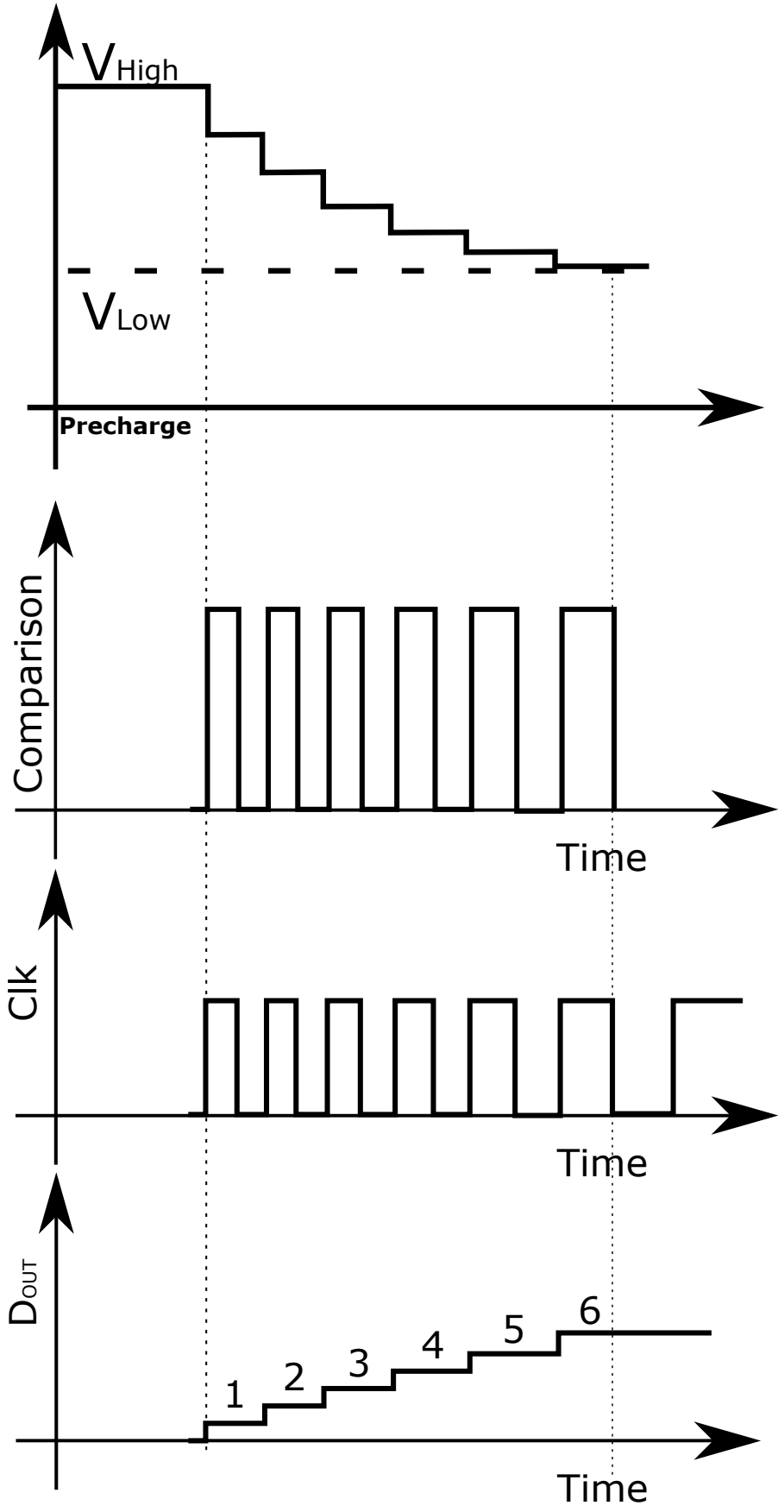


Figure 3.7: Signal performance during the discharging process [32]

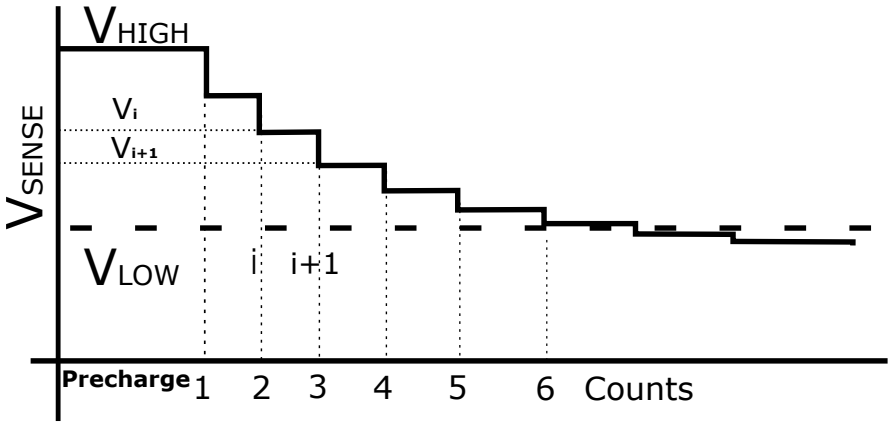


Figure 3.8: Discharge process

As Q_i=Q_{i+1}, $C_{SENSE} \times V_i = (C_{SENSE} + C_p) \times V_{i+1}$, we can derive the following formula:

$$\frac{V_{i+1}}{V_i} = \frac{C_{SENSE}}{C_{SENSE} + C_p} \tag{3.20}$$

and assuming V_{i+1}=V_i(1-k), then

$$k = \frac{C_p}{C_{SENSE} + C_p} \tag{3.21}$$

We can then model the discharge process by using the equation:

$$V_{LOW} = V_{HIGH}(1 - k)^n \tag{3.22}$$

where n is the number of steps taken to discharge C_{SENSE} from the voltage V_{HIGH} to V_{LOW}.

Based on the Taylor series,

$$(1-k)^n = 1-nk+\frac{n(n-1)k^2}{2!}-\frac{n(n-1)(n-2)k^3}{3!}+... \quad (3.23)$$

and, if nk«1, the above formula can be approximated as:

$$(1-k)^n = 1-nk \quad (3.24)$$

From Eq. 3.22, if we have V_{HIGH} and V_{LOW} fixed (i.e. const) by the measurement method, we must have $(1-k)^n$=*const*. Thus, under nk«1, we have 1-nk=*const* and thus nk=*const*, and hence

$$n\frac{C_p}{C_{SENSE}+C_p} = const \quad (3.25)$$

So, if C_{SENSE}»C_p, then C_{SENSE}+C_p≈C_{SENSE}. We will have

$$n\frac{C_p}{C_{SENSE}} = const \quad (3.26)$$

and thus *n* must be linearly proportional to C_{SENSE} with fixed V_{HIGH} and V_{LOW}. This means that with fixed V_{HIGH} and V_{LOW}, the value of *n* can be used to derive the value of tested capacitor C_{SENSE}.

3.1.3.2 *Sensing Voltage*

Similarly, we can measure V_{HIGH} under a known capacitance value and reference voltage V_{LOW}. Therefore, according to Eq. 3.22, we will have:

$$V_{LOW} = V_{HIGH} K^n \tag{3.27}$$

Where n is the number of steps taken to discharge C_{SENSE}, $K = \frac{C_{SENSE}}{C_{SENSE}+C_p}$, and here K=1-k.

With constant V_{HIGH} and V_{LOW}, the discharge process determines the value of C_{SENSE}. Similarly, if C_{SENSE} is fixed, it can be used to determine V_{HIGH}. After n steps, V_{HIGH} is discharged to V_{LOW}, then based on Eq. 3.27, we finally have,

$$n = \log_K(\frac{V_{LOW}}{V_{HIGH}}) = -\log_K(\frac{V_{HIGH}}{V_{LOW}}) \tag{3.28}$$

As a result, n is logarithmic with the sensed voltage (V_{HIGH}). This means that with a fixed capacitor and a fixed V_{LOW}, n can be used to derive V_{HIGH} to form a voltage sensor.

3.1.4 *Replacing V_{LOW} in QDC*

The next step is to simplify V_{LOW}. [25] shows a solution by using a time reference to create a delayed version of the clock 'Clk2' from the ring oscillator (i.e VCO) and compares it with the original clock 'Clk1' from the oscillator, as is shown in Fig. 3.9. As is explained before, in a ring oscillator powered by a voltage source, lower voltage generates slower frequency (i.e

larger period). Hence when the time distance compared in the time comparator between two 'Clk1' and 'Clk2' has reached a certain value, a finish signal is triggered and stops the oscillation. By counting the number of oscillation in the VCO , the counter generates a N-bits code. This design compares the frequencies instead of voltages because a time reference is easier to design than a voltage reference. However, the time reference is designed by using an RC circuit, which consumes more power and has relatively limited resolution.

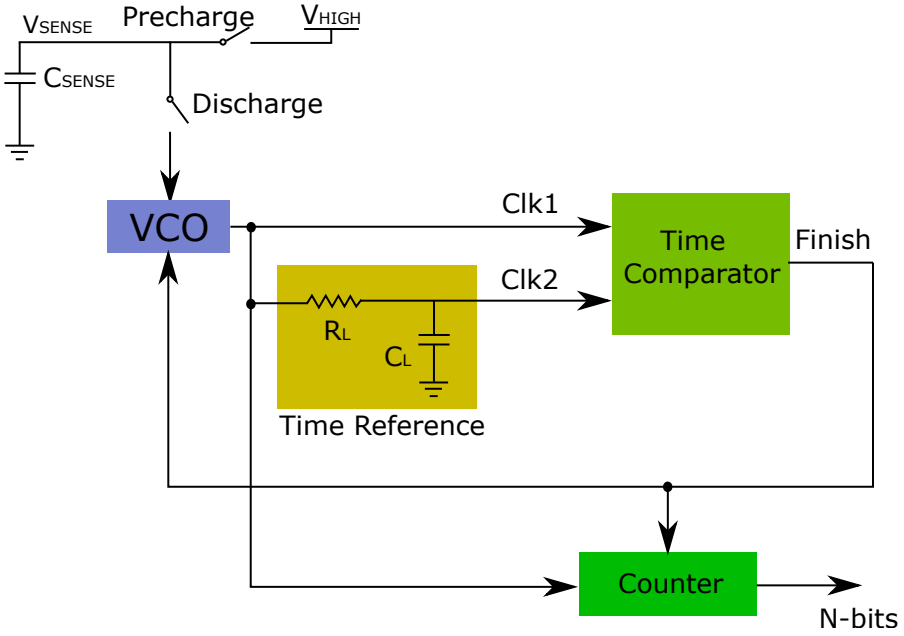


Figure 3.9: Fast capacitance-to-digital converter with internal reference [25]

A better solution is using an identical ring oscillator powered by V_{LOW} as a time reference, as shown in Fig. 3.10. A Clk_{SENSE} signal is generated from the upper ring oscillator during discharging process, while a Clk_{LOW} signal is generated from the bottom ring oscillator. Instead of comparing V_{SENSE} with V_{LOW} in a voltage comparator, the delay comparator compares the delay of Clk_{SENSE} with Clk_{LOW}. When V_{SENSE} is higher than V_{LOW}, Clk_{SENSE} is faster than Clk_{LOW}, which means it provides

a smaller propagation delay. When V_{SENSE} drops to V_{LOW}, the delays of Clk_{SENSE} and Clk_{LOW} become the same. The delay comparator detects this and stops the the 'comparison' signal. By counting the number of cycles of 'comparison' in the counter, we can get a digital code D_{OUT}. This circuit is now fully digital. However, the two ring oscillators need to start oscillation at the same time to make sure the delay comparator compares the same edge of the two clocks. However, it may be hard to synchronize them as they are powered independently usually under different voltages.

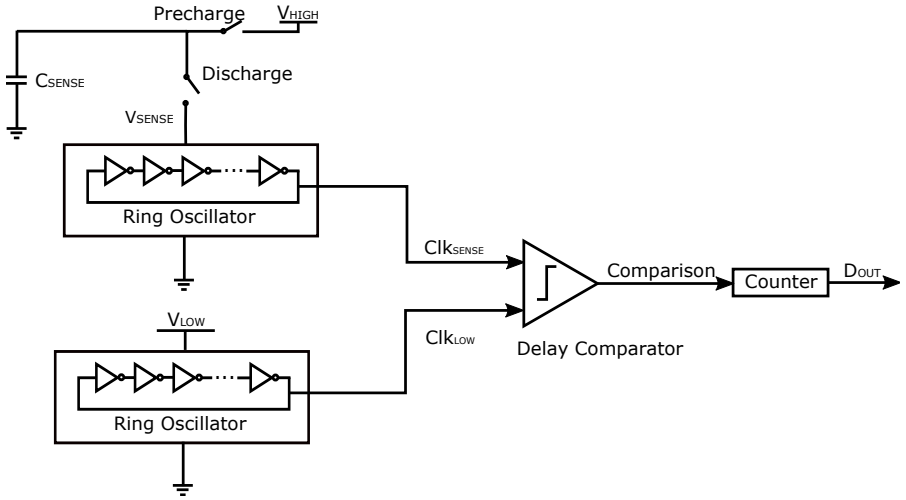


Figure 3.10: Time reference using inverter chain

3.1.5 *The proposed design*

The final version solves the problem in the last section by introducing a signal generator. As is shown in Fig. 3.11. A signal generator is added between the delay comparator and the counter. This signal generator can provide a self-generated clock triggered by a 'Start' signal when the discharging process starts. The two ring oscillators are replaced by two identical inverter chains. The whole circuit is powered by V_{LOW} to save power except the

top inverter chain which is powered by V_{SENSE}. Hence, a level shifter is needed to convert the amplitude of 'Clk' signal to the level of V_{SENSE} to drive the top inverter chain. The 'Level-up Clk' signal goes to both of the inverter chains and generates the Signal(H) and Signal(L) respectively. These two signals are compared by the delay comparator and triggers the signal generator to generate an other pulse for the next event until their delays become the same. The counter counts the number of oscillation of Clk and ouputs a digital code D_{out}.

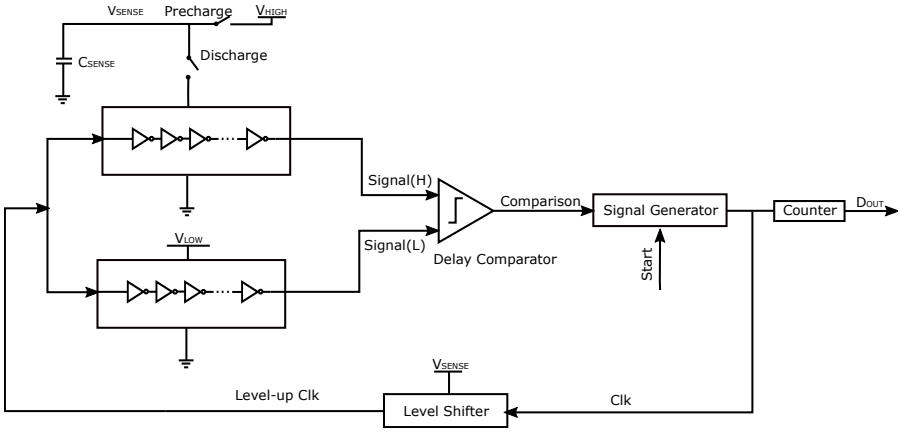


Figure 3.11: The proposed QDC

3.2 SUMMARY

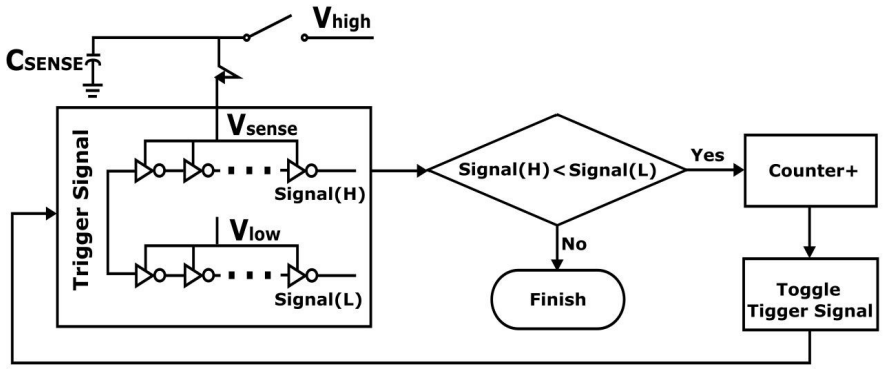


Figure 3.12: Iterative delay chain discharge method

This section shows the steps of how the system is designed from a simple RC discharging circuit to the proposed QDC. In conclusion, the key method is comparing the delay of two inverter chains powered by two different voltage sources. One voltage source is set to a fixed low value as a reference, and the other one is powered by a fully-charged capacitor with a higher voltage initially.

The summarized iterative delay chain discharge method is illustrated in fig. 3.12. Conceptually, a capacitor C_{SENSE}, whose charge is related to the physical parameter being measured, is discharged to a pre-set reference voltage. And the number of iterations of discharging is related to the initial charge.

Initially, the voltage across C_{SENSE}, V_{SENSE}, is charged to V_{HIGH} by the physical parameter. In each iteration, C_{SENSE} is discharged through an inverter chain powered by V_{SENSE}, in which a trigger signal passes through. At the same time, the trigger signal also passes through another inverter chain powered by a reference voltage (V_{LOW}) with the same number of inverters. Signal(H) and Signal(L) are the outputs of the two inverter chains respectively. The delays of the inverter chains are related to their V_{dd}s. The higher the V_{dd}, the smaller the delay. The two delays can be compared to detect whether V_{SENSE} has been discharged to V_{LOW}. If Signal(H) comes earlier than Signal(L), V_{SENSE} has not been discharged to V_{LOW}. As a result, more discharging is required. So, the counter is incremented by 1, the trigger signal is toggled, and another iteration of discharge will be performed. Otherwise, the voltage of C_{SENSE} has been discharged to V_{LOW}. The iterations stop, and the value of the counter is used to represent the value of V_{HIGH} and hence the physical parameter being measured.

When sensing the capacitance with fixed V_{HIGH}, the number of steps taken to discharge C_{SENSE} from the voltage V_{HIGH} to V_{LOW} is linearly proportional to C_{SENSE}. When sensing the voltage with fixed C_{SENSE}, the number of steps taken to discharge C_{SENSE} from the sensed voltage V_{HIGH} to V_{LOW} is logarithmic with the V_{HIGH}.

4

DESIGN AND IMPLEMENTATION

4.1 PROPOSED SOLUTION

This chapter describes the asynchronous implementation including the architecture of the proposed design with 6 blocks. Then the detailed design of the QDC-based capacitance/voltage sensor interface introduced in the previous chapter is shown respectively including charging/discharging circuit, signal generator, event generator, event comparator, level shifter and event counting mechanism. At last, the physical implementation is introduced to show the chip schematic and layout of the proposed QDC.

4.1.1 *Asynchronous Implementation*

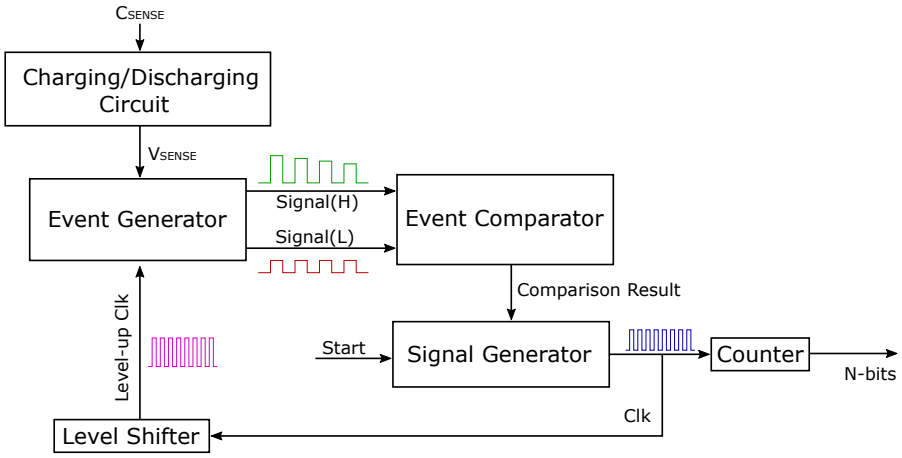


Figure 4.1: Asynchronous Implementation

Fig. 4.1 shows the architecture of the proposed design to achieve the sensing functions. The implementation includes 6 blocks: Charging/Discharging circuit, signal generator, event generator, event comparator, level shifter and event counting mechanism. In principle, a start signal triggers the signal generator to generate a *Clk* signal from the sensed quantity. The level shifter converters the amplitude of *Clk* signal to a high voltage. That converted *Clk* signal will be the input of the event generator as a trigger to produce two events. Those two generated ev ents are compared in terms of occurrence orders, and based on the comparison result, either the event counting is triggered or the conversion is finished. Along with the C_{sense} discharging in charging/discharging circuit, V_{SENSE} keeps dropping. The above process will be repeated until the finish condition is approached. Eventually, the event counter outputs the number of transitions of the *Clk* signal. The number of transitions, or the output code, is related to the capacitance of the sensed capacitor under fixed voltage level or the sensed voltage level under a fixed capacitance.

4.2 DETAILED DESIGN OF EACH BLOCK

4.2.1 *Charging/Discharging Circuit*

This charging/discharging circuit shown in 4.2 contains a power source V_{HIGH}, a sensed capacitor C_{SENSE} and two switches for charge and discharge C_{SENSE}. Firstly, the switch 'Precharge' is on. C_{sense} is then being charged by V_{HIGH}. The switch 'Discharge' keeps off during the charging process to make sure no voltage and current go across to the next section. After C_{sense} is

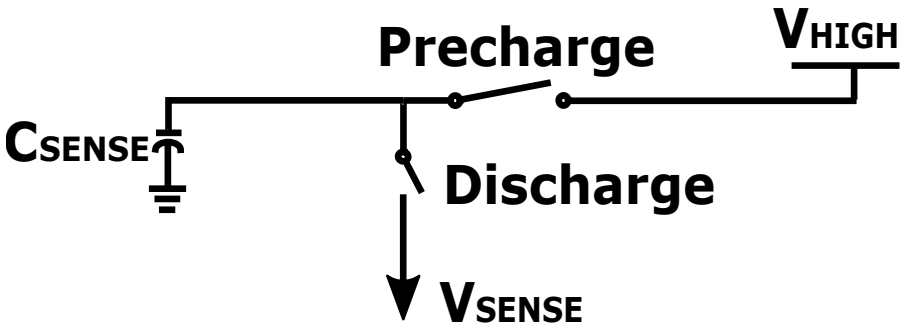


Figure 4.2: Charging/Discharging Circuit

fully charged, the switch 'Precharge' turns off, and the switch 'Discharge' turns on. Then the sensing mechanism is started. V_{SENSE} means the voltage across C_{sense} while discharging.

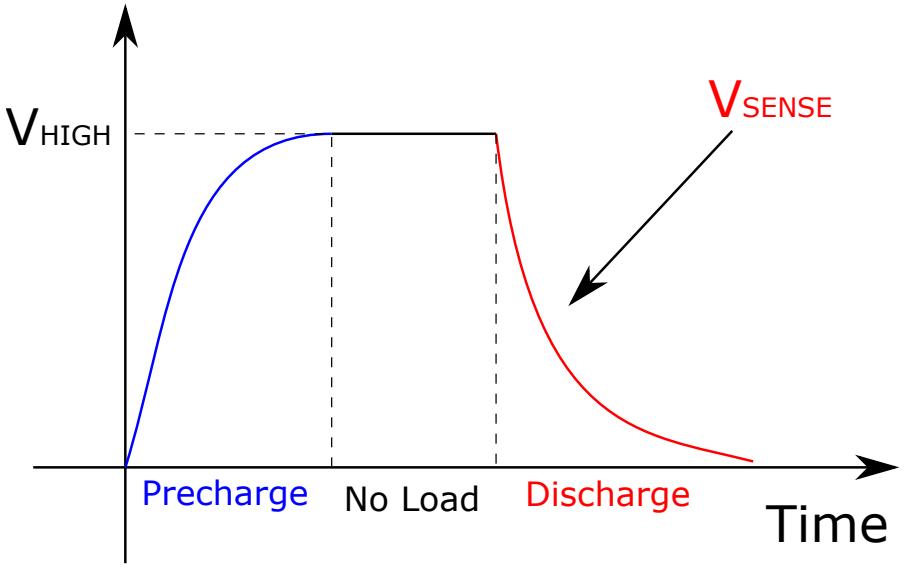


Figure 4.3: Operation of capacitor charging and discharging

Fig. 4.3 shows the operation of charging and discharging C_{sense}. The blue line is the charging process. After C_{sense} is fully charged to V_{HIGH}, if the 'Start' signal in the signal generator is not triggered, it then assumes that sensing is not yet to start. Hence, C_{sense} keeps on the level of V_{HIGH}. Once the 'Start' signal triggered, the inverter chain powered by V_{SENSE} in the Event Generator starts to oscillate, which draws the Energy on C_{sense}. As a result, C_{sense} starts to discharge as is shown in the red line.

4.2.2 *Signal Generator*

The inverter chains in the event generator can not provide oscillation by themselves. The reason we don't use two ring oscillators to generate oscillation in the event generator is that it will be very hard to synchronize each other as they are powered independently usually under different voltages, which are V_{SENSE} and V_{LOW}. Hence, a signal generator is needed to trigger the two inverter chains at the same time.

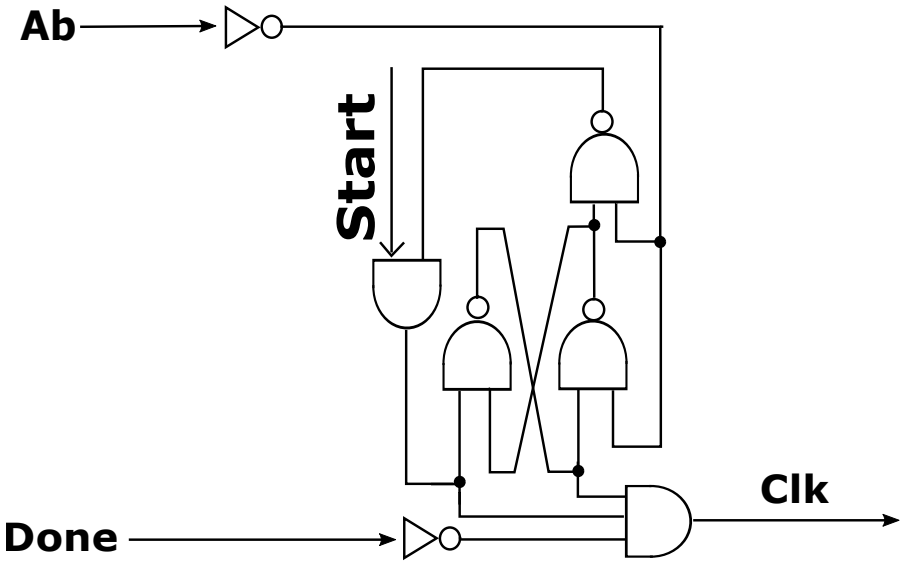


Figure 4.4: Schematic of the signal generator

Fig. 4.4 shows the schematic of the signal generator. 'Ab' and 'Done' are both coming from the event comparator. 'Ab' is the output signal from the MUTEX while 'Done' is the output signal from the C-element (The operation of 'Ab' and 'Done' will be explained in section 4.2.4). The 'Start' signal decides when to start the 'Clk' signal. 'Ab' signal decides when to disable it through the SR latch. There are three states in the operation of the signal generator.

The first step is the initial state, where the 'Start' signal equals to logic 'o'. As can be seen in Fig. 4.5, if 'Start'=o, then the

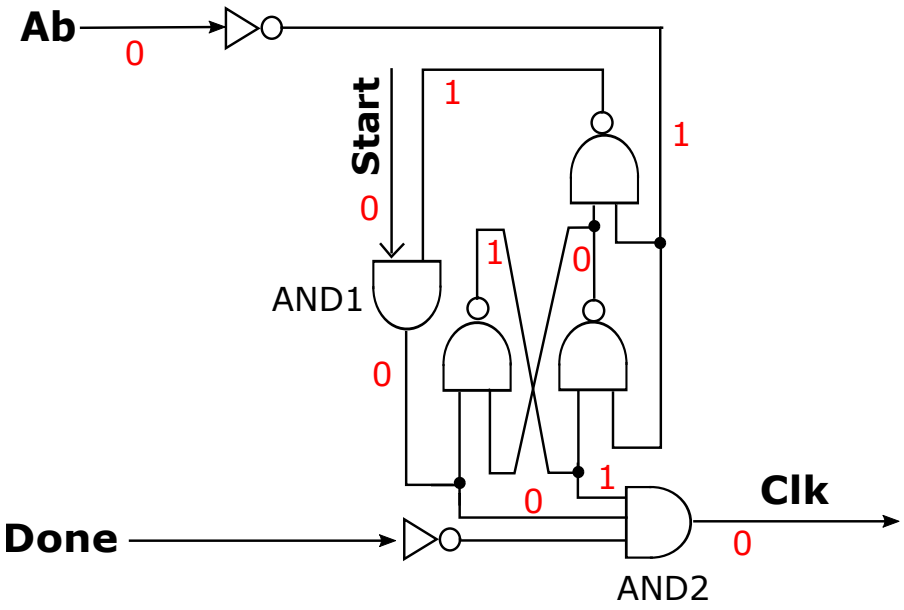


Figure 4.5: Initial state of the signal generator

output of the AND gate 'AND1' must be logic '0', regardless of the other input of it. In this case, the output of the AND gate 'AND2' must be logic '0' as well for the same reason. The 'Clk' then will not be triggered in any circumstance, which means no oscillations are happening in the event generator for both two inverter chains. In this case, the output of the SR latch are logic '1' and logic '0' respectively according to their inputs.

When 'Start' signal is triggered to logic '1', the second step starts. During this time, V_{SENSE} is larger than V_{LOW}. Hence, 'Ab' is always logic '0'. Fig. 4.6 shows the logic states of the signal generator. In this case, the two inputs of 'AND2' are always logic '1'. Hence, the output of 'Clk' only depends on the 'Done' signal based on the comparison results in the event comparator.

When V_{SENSE} drops to the same voltage level of V_{LOW}, 'Ab' triggers to logic '1'. The third stage starts shown in Fig. 4.7. In this stage, the two outputs of the SR latch change to logic '0' and '1' based on their inputs. Hence, one of the inputs of 'AND2' becomes logic '0', which disables the 'Clk' signal. The

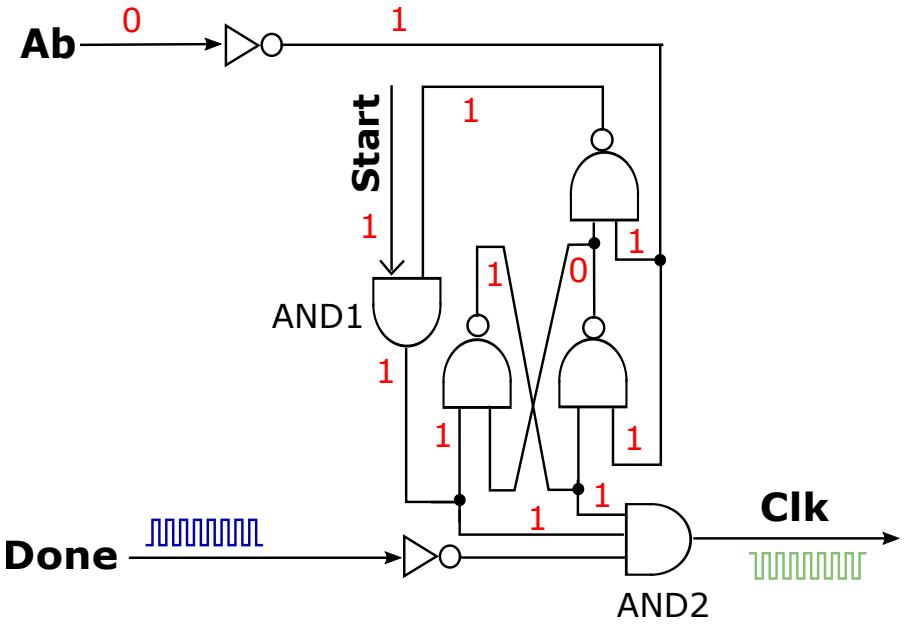


Figure 4.6: State 2 of the signal generator

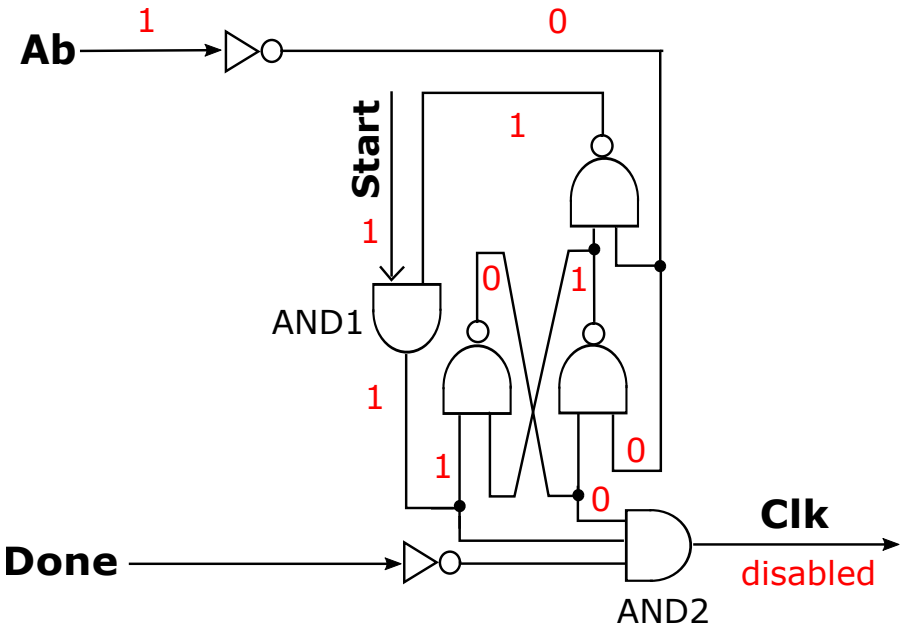


Figure 4.7: State 3 of the signal generator

two inverter chains in the event generator then stop oscillation and the event comparator stops comparison until the round of next sensing for a new V_{HIGH} and C_{SENSE} .

The timing diagram of the signal generator including all three stages is shown in Fig. 4.8. It clearly shows that before stage 1, no signal is triggered. After the 'Start' signal is triggered in stage 2, the 'Clk' signal keeps triggering until in stage 3, where 'Ab' becomes logic '1' and thus disables 'Clk' and 'Done'.

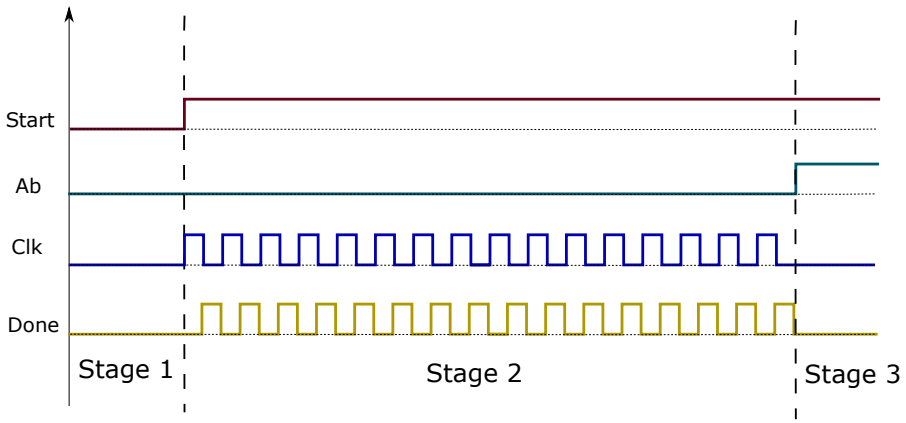


Figure 4.8: Timing diagram of the signal generator

4.2.3 *Event Generator*

The Event Generator shown in 4.9 contains two 16-stage inverter chains. The upper inverter chain is powered by V_{SENSE} and the bottom one is powered by a reference voltage V_{LOW}. The event generator is triggered by a level-up *Clk* signal from the level shifter (originally generated from the event generator). The two inverter chains inside the signal generator generate two events with different delays when V_{SENSE} and V_{LOW} are different.

Fig. 4.10 illustrates the outputs of the event generator at the beginning, middle and ending states. The top square wave is the output of the top inverter chain Signal(H), the bottom one is

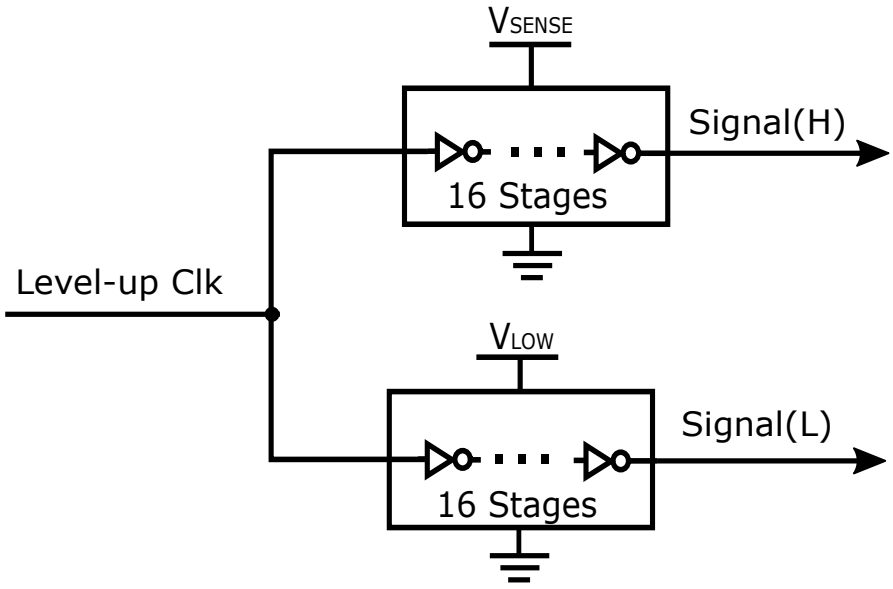


Figure 4.9: Event Generator

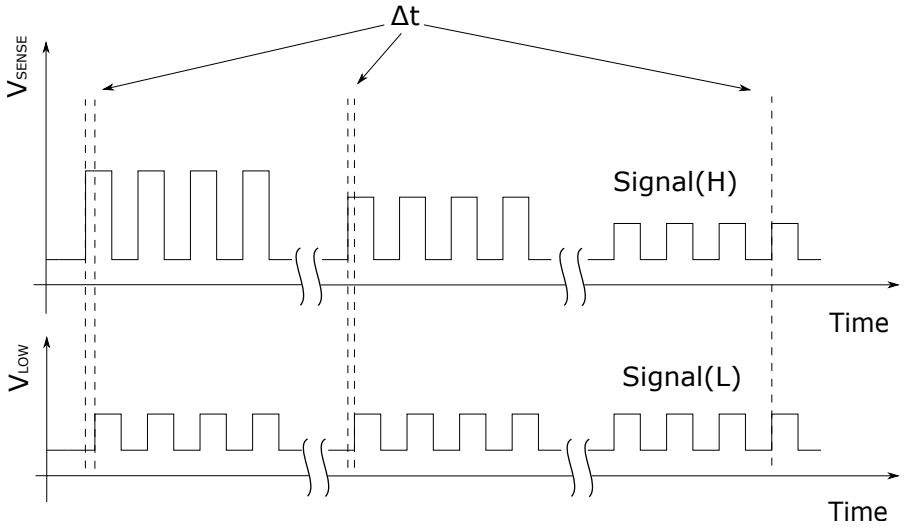


Figure 4.10: Output of event generator

the output of the bottom inverter chain Signal(L). The delays of these two inverter chains are related to their power supply. The amplitude of Signal(H) keeps decreasing because the oscillation itself draws the energy stored in C_{SENSE} (i.e. V_{SENSE} drops). In the beginning, V_{SENSE} is larger than V_{LOW}. This means the propagation delay of Signal(H) is smaller than of Signal(L). Hence, Signal(H) comes earlier than Signal(L). The time difference between their rising edges, Δt is large. Because V_{SENSE} drops gradually, Δt, becomes smaller. When V_{SENSE} eventually drops to the same level of V_{LOW}, their propagation delays become the same, which means $\Delta t=0$.

One way of tuning the precision vs. sensing delay and energy consumption trade-off is through adjusting the sizes of the upper and lower inverter chains in the event generator. In this design, in order to give a fair comparison with the existing work [32], two 16-stage inverter chains are used as well.

4.2.4 *Event Comparator*

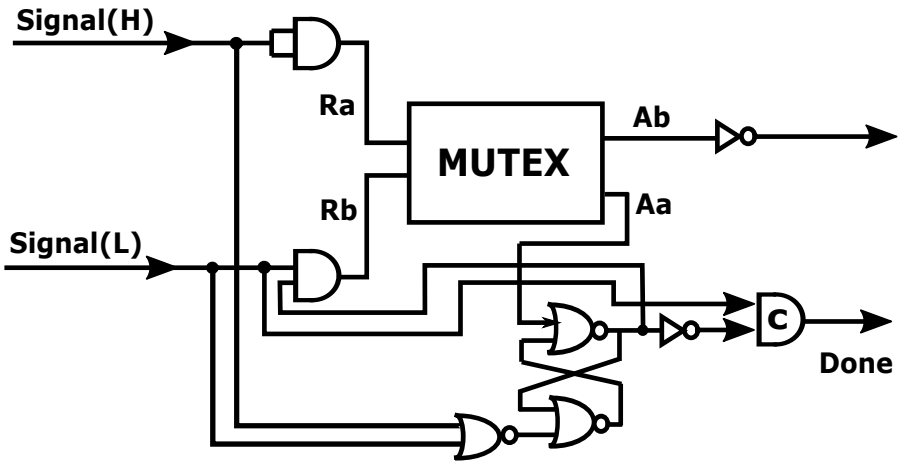


Figure 4.11: Schematic of event comparator

Fig. 4.11 shows the schematic of the event comparator. The event comparator only compares the two events in their rising edges. A first clock signal 'Clk' triggers the event generator. Two events Signal(H) and Signal(L) are then generated by their corresponding inverter chains, which arrive in the MUTEX independently after their respective delays. If Signal(H) comes earlier than Signal(L), 'Ra' wins the arbitration. Thus, 'Aa' becomes high. This updates the SR latch below the MUTEX to block 'Rb' to remove any potential glitches. After updating, Signal(L) comes to raise the 'Done' signal by using a C-element. The truth table of C-element is shown in Fig. 4.1. When two inputs of the C-element are both logic '0', it outputs '0'. When both inputs are logic '1', it outputs '1'. Otherwise, it keeps the previous output value [69]. During this state, 'Ab' is low, the 'Clk' signal only depends on the 'Done' signal. Hence, 'Clk' falls ('Done' goes through an inverter). This makes sure that both inverter chains have completed their run before the 'Clk' falling. The low 'Clk' signal passes through the event generator, and Signal(H) and Signal(L) become low. During this time, both 'Ra' and 'Rb' are low and hence 'Aa' is withdrawn to low, and 'Done' becomes low. Again, the three NOR gates are used to realize the control of this mechanism. As a result, 'Clk' then goes up again. The above process repeats until Signal(L) comes earlier than Signal(H). In this scenario, Ab becomes high. As discussed in section 4.2.2 before, it stops 'Clk' signal until the next round of sensing for a new V_{HIGH} or C_{SENSE}.

As Signal(H) and Signal(L) are two independent events in time, metastability may happen when they are very close to each other and to be compared during the end of sensing. The MUTEX may take some time to decide which event 'wins' the

Table 4.1: Truth table of C-element [69]

x_1	x_2	y_n
0	0	0
0	1	y_{n-1}
1	0	y_{n-1}
1	1	1

comparison. The comparator does not issue a valid result until it has resolved any metastability inside, making sure that its output signal can only take the values of logic '0' or '1' securely and no non-deterministic middle value can be sent out. In other words, the value of the comparison is always correct with or without metastability, which could only cause a non-deterministic delay in the worst case. This delay is tolerable as the entire sensing system is asynchronous and metastability settling time is usually very short.

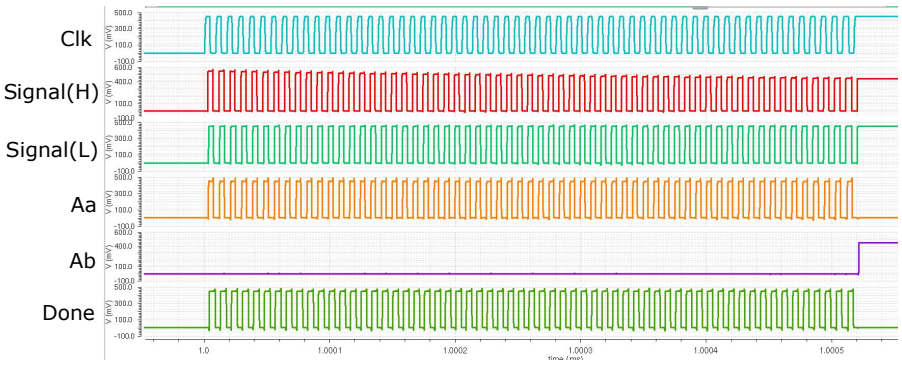


Figure 4.12: Timing diagram of event comparator

Fig. 4.12 shows the simulation results of the event comparator timing diagram. The simulation is based on UMC 90nm CMOS technology. V_{HIGH} is set to 550mV, V_{LOW} is set to 450mV and C_{SENSE} is 50pF to present a short and clear operation of the event comparator in a complete timing diagram. As can be seen, a first rising edge of 'Clk' signal triggers Signal(H) and Signal(L). When the voltage V_{HIGH} powering the upper inverter chain is higher than the reference voltage V_{LOW}, which powers

the bottom inverter chain, i.e Signal(H) is faster than Signal(L), 'Aa' keeps oscillating, as well as 'Done' and 'Clk'. The 'Clk' signal keeps going up and down as an oscillator to trigger each round of Signal(H) and Signal(L) as described before. In the end, V_{HIGH} becomes equal to or smaller than V_{LOW}, i.e Signal(L) comes at the same time as or earlier than Signal(H). The last comparison of Signal(H) and Signal(L) in the rising edge stops 'Aa' and triggers 'Ab' from logic '0' to '1'. Thus, 'Done' is disabled and thus the signal generator stops 'Clk'. The comparison of Signal(H) and Signal(L) is then finished.

4.2.5 *Level shifter*

The voltage level of logic '1' in *Clk* signal coming from the signal generator is V_{LOW}. It can not directly drive the upper inverter chain powered by a higher voltage V_{SENSE}. Hence, a level shifter is required.

A level shifter is commonly used in digital circuits. It solves the problem that how to drive a higher voltage logic circuit from a lower voltage logic circuit without changing the logic value [29]. In this design, the level shifter takes a given *Clk* signal on the voltage level of V_{LOW} logic side, and converts it to the appropriate voltage (V_{SENSE}) but still keeps the same logic value as an input to drive the event generator's upper inverter chain. In other words, the digital logics keep the same before and after level shifting. However, the voltage level on logic '1' changes from V_{LOW} to V_{SENSE} after level shifting.

Fig. 4.13 shows the schematic of the level shifter. M_{P1} and M_{P2} are two PMOS transistors. M_{N1} and M_{N2} are two NMOS transistors. Two buffers are used to enhance the input signal *Clk*

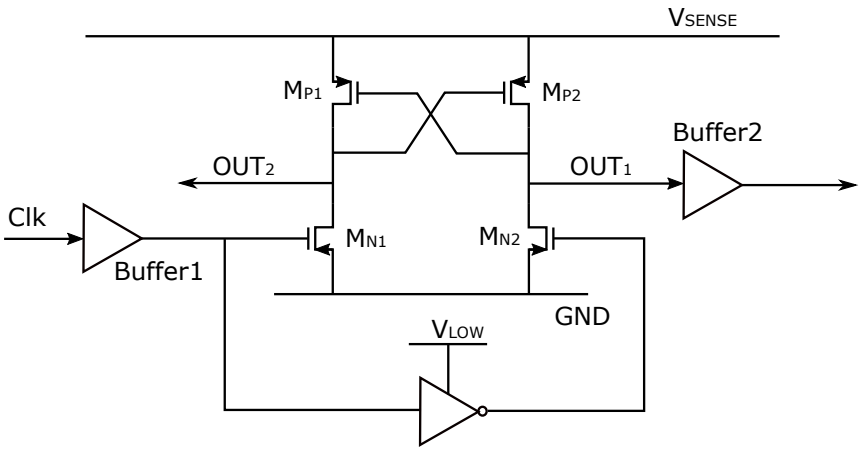


Figure 4.13: Schematic of the level shifter

and output signal OUT_1. An inverter powered by V_{LOW} is used to make sure M_{N1} and M_{N2} have inverse inputs.

Fig. 4.14 shows the operation of the level shifter when the input *Clk* signal is at logic '0'. In this scenario, M_{N1} and M_{P2} are off, while M_{P1} and M_{N2} are on. Hence the output signal OUT_1 is at logic '0'.

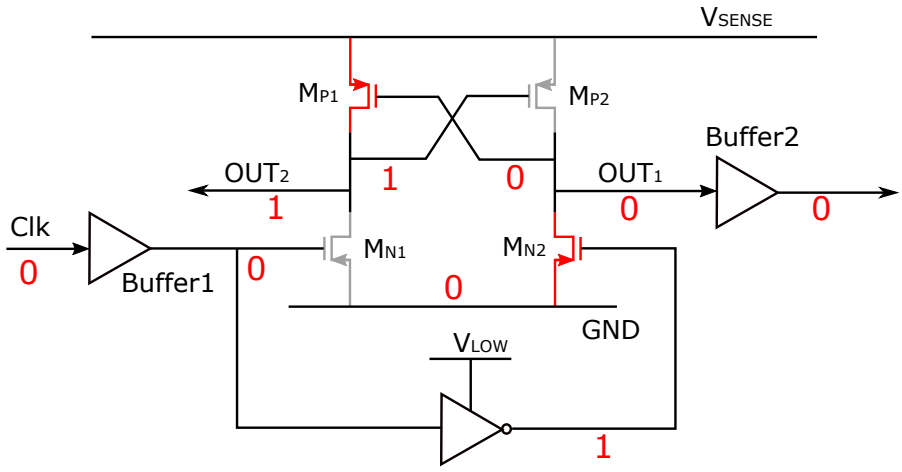


Figure 4.14: When *Clk* signal is at logic '0'

Fig. 4.15 shows the operation of the level shifter when the input *Clk* signal is at logic '1'. In this scenario, M_{N1} and M_{P2} are on, while M_{P1} and M_{N2} are off. Hence V_{SENSE} goes through M_{P2} which leads the output signal OUT_1 becoming logic '1' with the voltage level of V_{SENSE}.

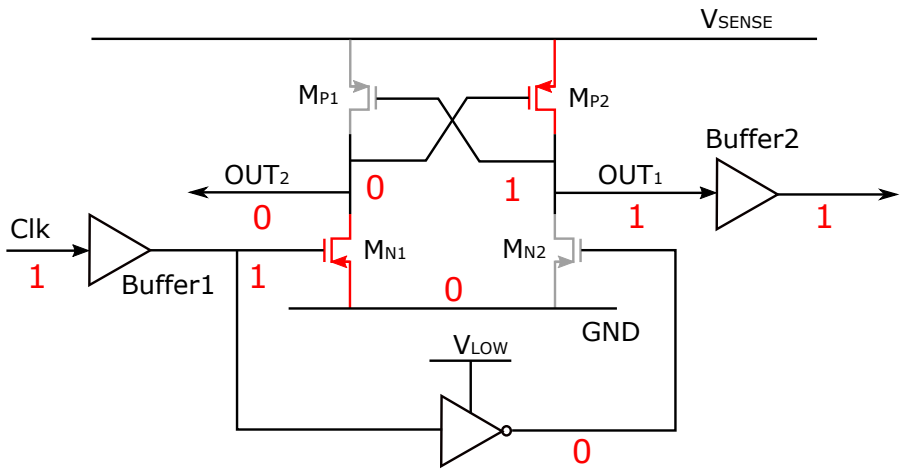


Figure 4.15: When *Clk* signal is at logic '1'

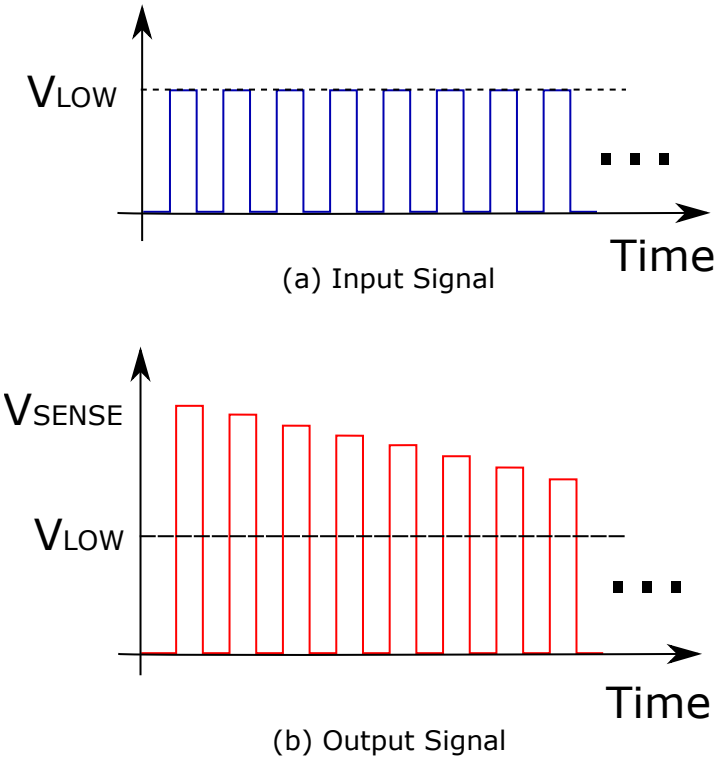


Figure 4.16: The operation of the level shifter

The operation of the level shifter is shown in Fig. 4.16, where (a) is the input signal (*Clk*) and (b) is the output signal after level shifting. The voltage level of logic'1' transforms from V_{LOW} into V_{SENSE} with small propagation delays. However, the logic of '0' and '1' still keep the same.

Since the upper inverter chain in the event generator is the only circuit which requires the supply voltage V_{SENSE}, by using the level shifter, the rest of the circuit can still work on V_{LOW} to save the power without affecting the operation in the event generator.

4.2.6 *Event counter mechanism*

A 20-bit counter (same number of bits as [32]) is built to count the number of transitions of the *Clk* signal. Fig. 4.17 shows the schematic of the 20-bit counter. The JK flip flops are triggered by the *Clk* signal from the signal generator and each of them is connected with an AND gate. The J and K are tied together. The generated Q represents the binary code D_{out}. V_{LOW} is the input of J and K in the first flip flop. For the rest 19 flip flops, the output of the previous AND gate becomes the input of J and K. The principle of the circuit is that for n=0 to 19, the frequency of $D_{out} < n >$ is $(1/2)^{n+1}$ of the *Clk* signal.

The timing diagram of the counting mechanism is shown in Fig. 4.18. $D_{out} < 0 >$ is triggered when detecting the first rising edge of the *Clk* signal. According to the principle of the JK flip flop, the frequency of $D_{out} < 0 >$ signal is half of the *Clk* signal. $D_{out} < 1 >$ is triggered at the first falling edge of $D_{out} < 0 >$ and the frequency of $D_{out} < 1 >$ signal is half of the $D_{out} < 0 >$. The following D_{out}s obey this rule until the counter counts the

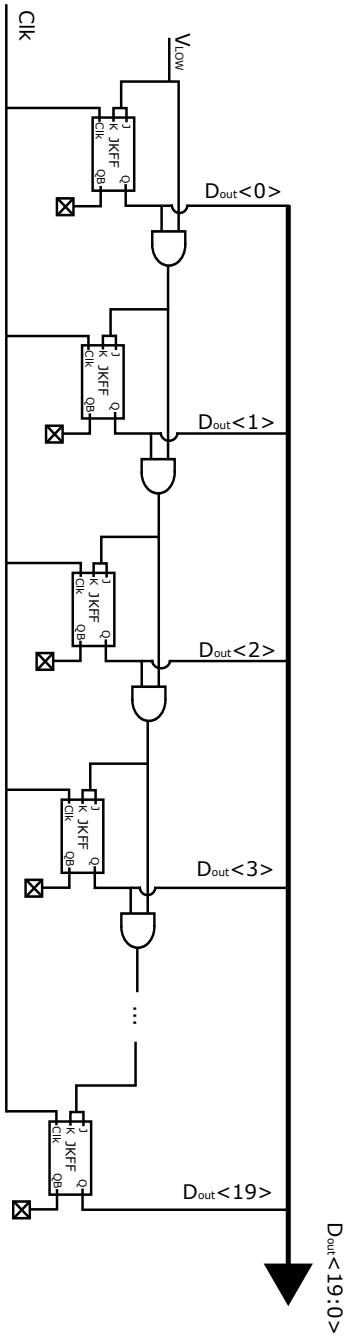


Figure 4.17: schematic of the counter

whole number of transitions of the *Clk* signal. This figure also shows two examples of counting a certain number (5 and 16) of transitions of the *Clk* signal.

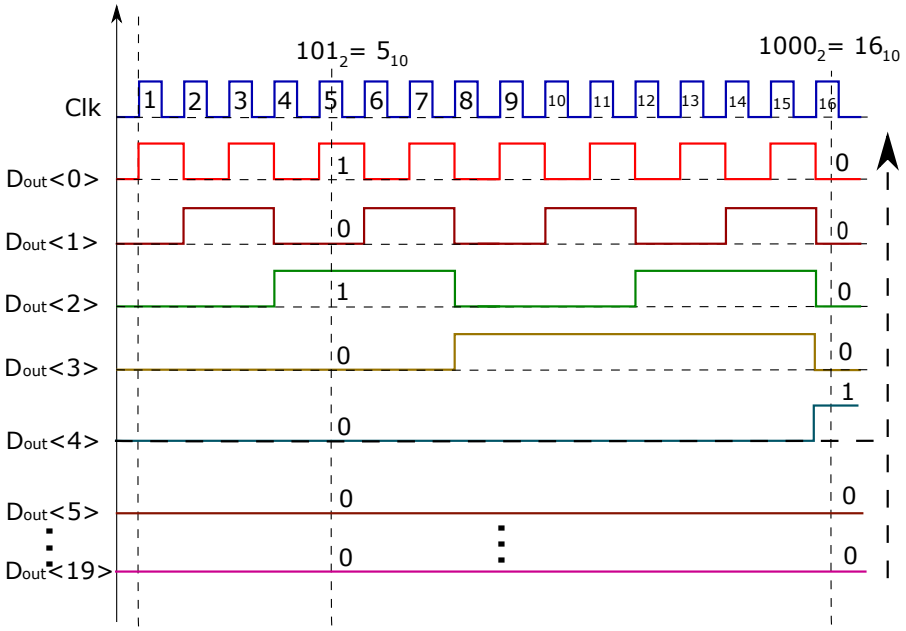


Figure 4.18: Timing diagram of the counter

Table. 4.2 shows the truth table of the counter. The *Clk* transitions are decimal numbers while the rest are binary numbers. This counter can count up to 2^{20} of *Clk* transitions.

Table 4.2: Truth table of the 20 bit counter

Clk transitions	$D_{out} < 19 >$	...	$D_{out} < 2 >$	$D_{out} < 1 >$	$D_{out} < 0 >$
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
...	...	...	...	...	...
$2^{20} - 1$	1	1	1	1	0
2^{20}	1	1	1	1	1

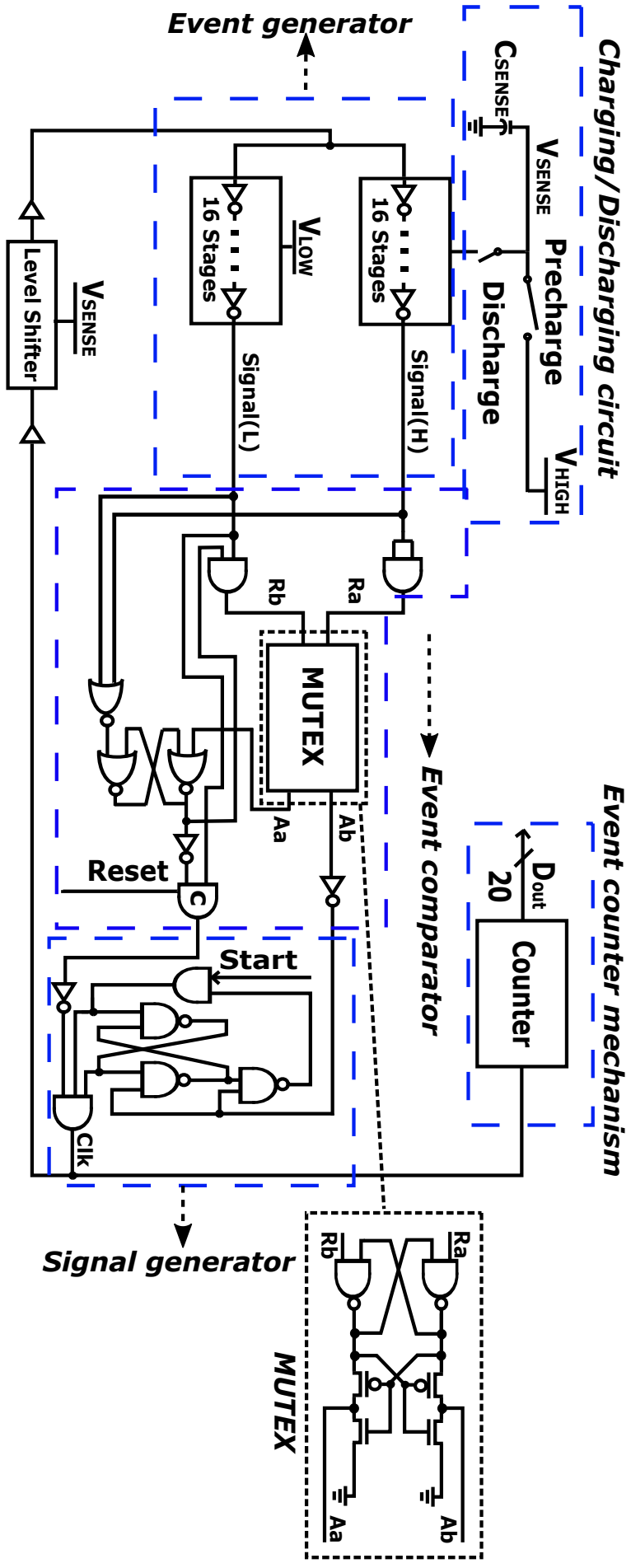


Figure 4.19: complete design

4.3 PHYSICAL IMPLEMENTATION

Fig. 4.19 shows the complete schematic of the QDC with six different parts implemented. The QDC designed in this chapter was fabricated at a 350nm AMS technology in a pin grid array (PGA) package shown in Fig. 4.20 covering an area of 1000µm by 996.45µm including the bonding pads. It contains three parts. The core circuit (173.2µm by 27.8µm without pads) includes the event generator, event comparator, signal generator and level shifter. The 20-bit counter (704.6µm by 27.8µm without pads) counts the number of transitions of the clock signal from the main circuit. There is also a 100 pF on-chip capacitor (892.9µm by 131µm without pads) built inside to test the circuit. It is not directly connected to the main circuit so an off-chip capacitor can also be tested. The design is laid out in two power supplies i.e one for the upper invert chain in the event generator (VDDS) and one for the rest of blocks in the QDC (VDD). The physical layout of the QDC and its verifications including Layout verse schematic (LVS) and Design Rule Check (DRC) were performed using analogue tool called Cadence Virtuoso.

4.4 SUMMARY

This chapter shows the implementation of the proposed design and the detailed circuit of each block. The charging/discharging circuit is used to initially charge and discharge C_{SENSE}. The level shifter converts the clock signal to a desired voltage level with the same logic. The signal generator triggers and stops the clock. The event generator generates produces two events and the their delays are compared by the event comparator. The counter

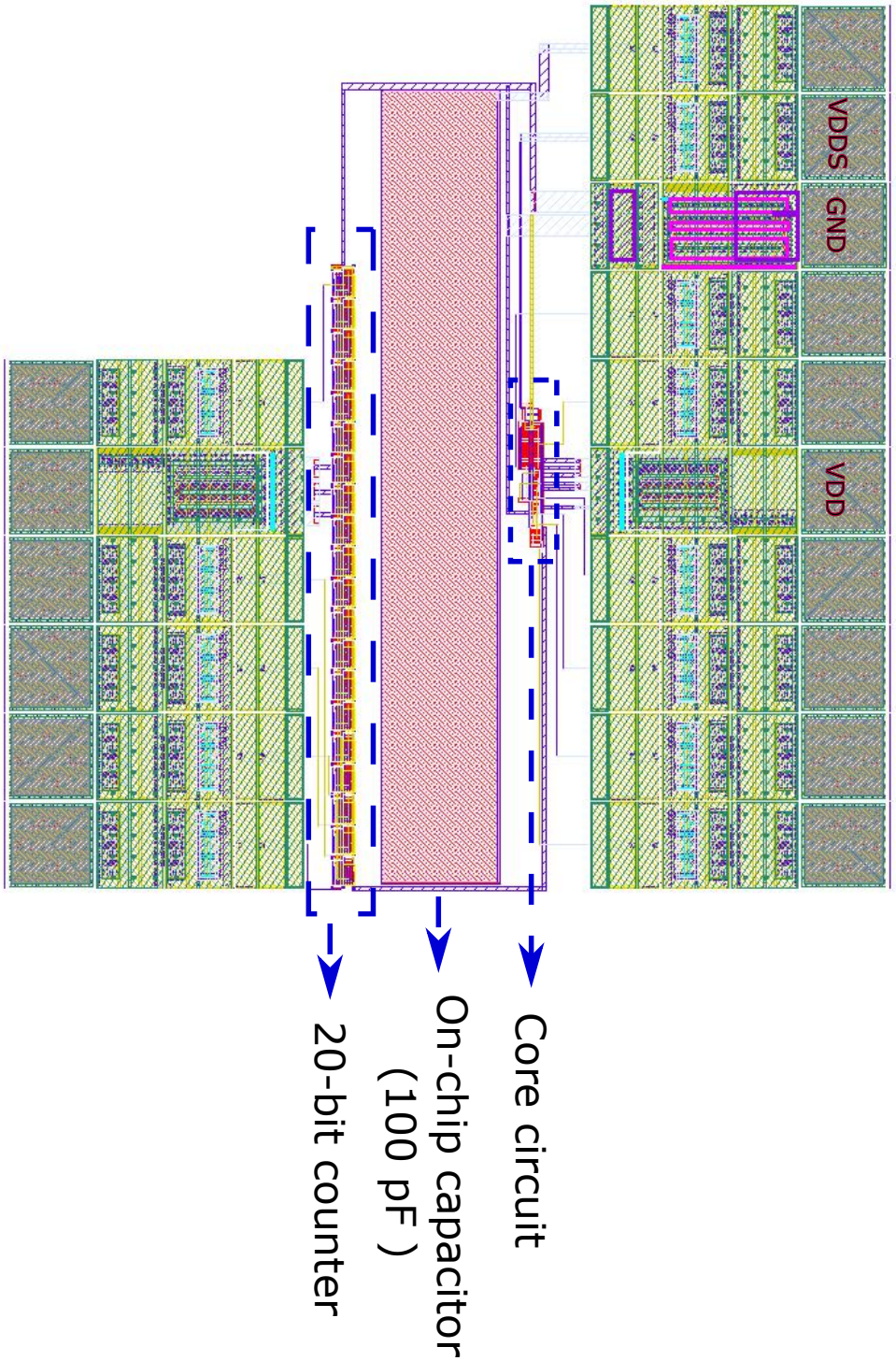


Figure 4.20: complete design. The design is implemented in a 350nm process and covers an area of 1000µm by 996.45µm. The QDC consists of the charging/discharging circuit, event generator, event comparator, signal generator and level shifter.

counts the number of steps taken to discharge C_{SENSE} from the voltage V_{HIGH} to V_{LOW}. In the end, the layout of the designed QDC with all the circuits implemented including a core circuit, a 20-bit counter and a 100pF on-chip capacitor is provided.

5

EXPERIMENTAL RESULTS AND VALIDATIONS

This chapter shows both of the simulation and chip results of the designed QDC. The simulation results include the output codes, response time, power consumption and Energy usage with the comparison to the existing work. The chips results part firstly introduce the general set-up of the test platform including the fabricated chip, PCB design, PGA socket and the equipment of testing. Then it shows the analysis of experimental results of the tested chip.

5.1 SIMULATION RESULTS

The simulation results are based on UMC 90nm CMOS technology. Fig. 5.1 shows a simulation result of the design. V_{HIGH} is set to 1V, which means that V_{SENSE} is 1V at the beginning, V_{LOW} is set to 0.45V and C_{SENSE}=50pF. These parameters are only used to show the concept of the proposed mechanism as an example. For sensing, only one of V_{HIGH} and C_{SENSE} will be fixed.

The rising of the 'Start' signal triggers the discharging of V_{SENSE} and the 'Clk' signal starts to be generated. When V_{SENSE} drops to V_{LOW}, the delay of the inverter chain powered by V_{SENSE} catches up with the delay of the other inverter chain powered by V_{LOW}. After that, Ab will be generated to high and the 'Clk' stops oscillating. Then the 20-bit counter outputs the total amount of Clk rising signals, when $V_{SENSE} > V_{LOW}$.

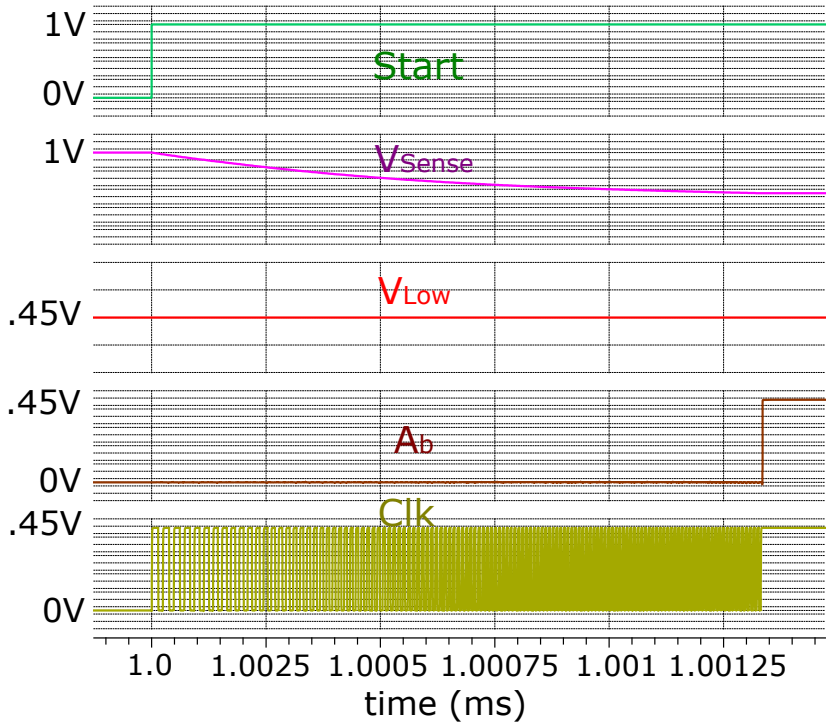


Figure 5.1: Simulation Results

5.1.1 *Output codes for sensing capacitance*

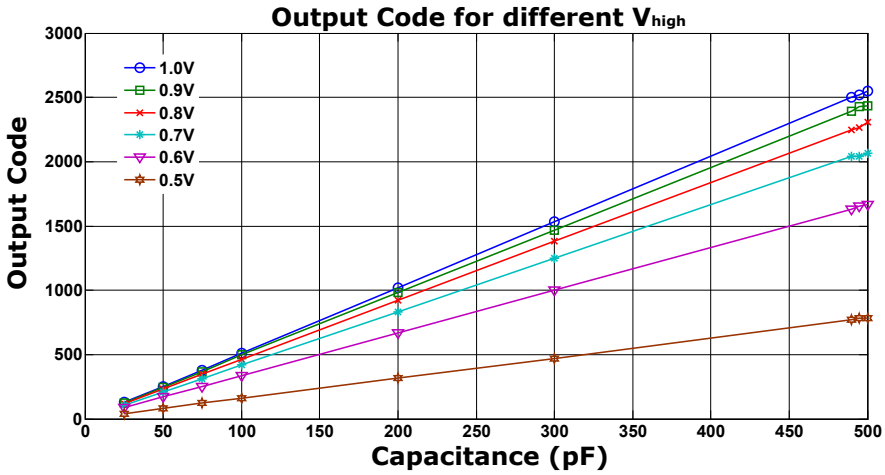


Figure 5.2: Simulation Results

After this initial demonstration, experiments have been done to characterize the design as a capacitance sensor as shown in

Fig. 5.2. Here, different V_{HIGH} values are used from 0.5V to 1V, shown in different colours in the figure, and V_{LOW} is set to 0.45V. These experiments produced a relationship between the output code and C_{SENSE} given any valid V_{HIGH} value. For example, set V_{HIGH}=0.8V, with V_{LOW}=0.45V. If output code = 232, then we can say that C_{SENSE} = 50pF and if output code = 2306, then we can derive that C_{SENSE} = 500pF. As can be seen from Fig. 5.2, the output codes under the same V_{HIGH} for different capacitance values are linear as is discussed in Section 3.1.3.1. For each value of V_{HIGH}, we can determine a specific formula for the output code to C_{SENSE} relationship. This means that for a fixed V_{LOW}, if we know the output codes and V_{HIGH}, we will be able to calculate the value of the capacitance. The value of V_{HIGH} can be used to tune the sensing precision vs. speed and energy trade-off. The higher V_{HIGH} is, the higher the sensing precision is, at the cost of longer sensing time and greater sensing energy consumption. This is because for the same C_{SENSE}, charging to a higher voltage needs more energy and leads to the discharging process taking longer,which will be shown in Section 5.1.4.

5.1.2 *Output codes for sensing voltage*

Fig. 5.3 shows another set of experiments to characterize the design as a voltage sensor. Here several fixed values of capacitors are used. For example, in Fig. 5.3, different colours of lines represent different C_{SENSE} values, from 25pF to 500pF. V_{LOW} is set to 0.45V again. When setting C_{SENSE} = 500pF, with V_{LOW}=0.45V, if output code = 1664, then we can find that V_{HIGH} = 0.6V and if output code = 2306, then we can derive that V_{HIGH} = 0.8V. As can be seen from Fig. 5.3, with any fixed C_{SENSE} value, the

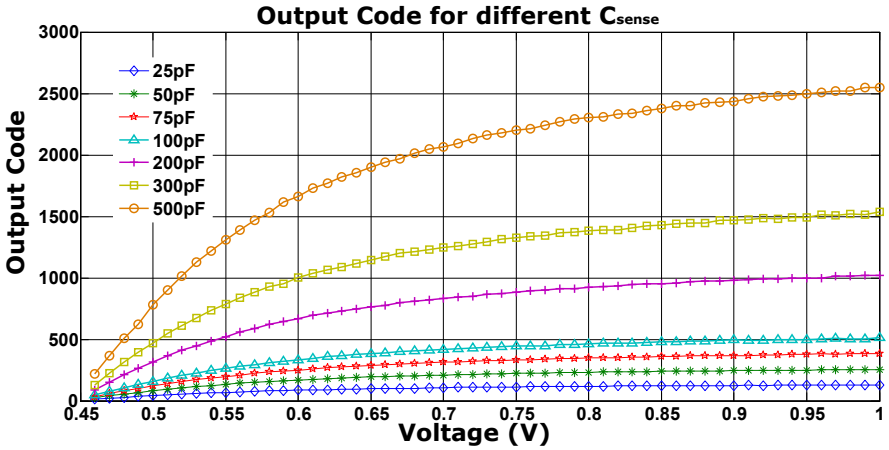


Figure 5.3: Simulation Results

output codes have a logarithmic relationship with V_{HIGH} values as is discussed in Section 3.1.3.2. For each value of C_{SENSE}, we can determine the specific formula for the relationship between output code and V_{HIGH}. Then, if we know the output codes and V_{LOW}, we will be able to calculate V_{HIGH}, similar to when the design is used for capacitance sensing. Also similarly, the value of C_{SENSE} can be used to tune the sensing precision vs. response time and energy trade-off. The higher of the value of the fixed C_{SENSE}, the higher the precision of the measurement is, at the cost of longer sensing time and greater sensing energy. This is because using the same V_{HIGH} to charge a larger C_{SENSE} takes greater energy, leading to a longer discharging process.

5.1.3 *Overall performance for QDC*

Fig. 5.4 shows a 3D overall performance of the design in terms of different V_{HIGH} (with the range from 0.5V to 1V), C_{SENSE} (with the range from 50pF to 500pF) and the resulting output codes when V_{LOW} is set to 0.45V. It shows that when sensing

capacitance or voltage, for a higher V_{HIGH} and higher C_{SENSE}, more output codes are generated.

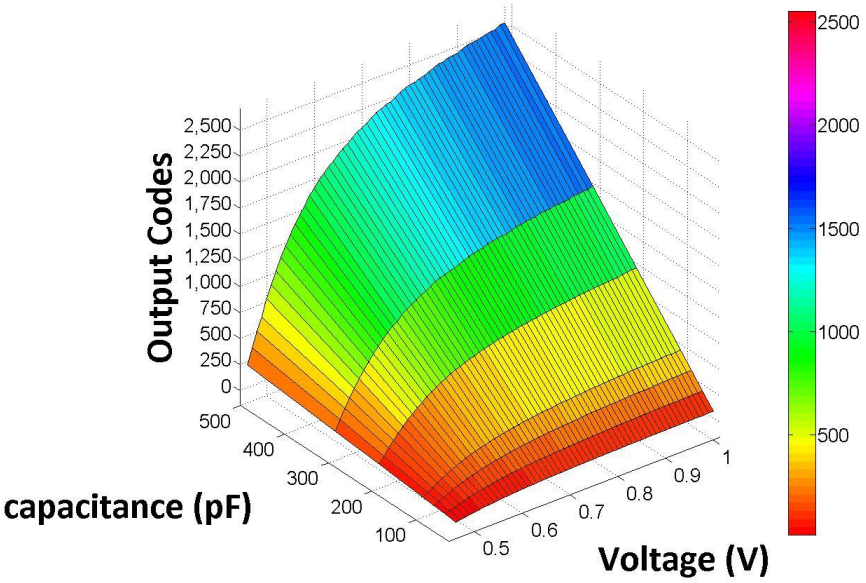


Figure 5.4: Overall Performance

5.1.4 *Performance comparison*

The characterization experiments demonstrated the viability of this design for its two intended uses. Next this design is compared with existing work [32] for performance metrics including output codes, response time, average power and energy usage per sensing round. In this comparison, V_{LOW} is set to 0.45V and C_{SENSE} is set to 50 pF. V_{HIGH} varies from 0.5V to 1V. Fig. 5.5 shows the comparison of these performance metrics, which are all based on the UMC 90nm CMOS technology simulation results.

Fig. 5.5(a) shows the comparison of output codes. The output codes of this work and [32] are almost the same. However, as discussed in chapter 2, the design in [32] may have the problem

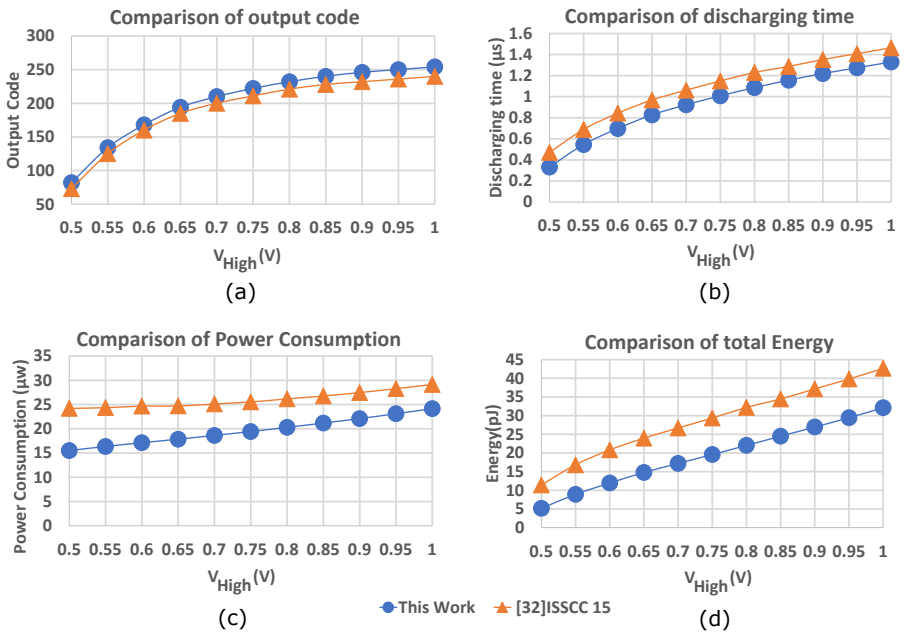


Figure 5.5: Simulation Results

of metastability which affects the resolution while this work aviods this problem.

Fig. 5.5(b) shows the comparison of response time. In this work, the response time means the time from the triggering of 'Start' signal to the going up of 'Ab' signal, while in [32], the 'Finish' Signal falling indicates that. On average, the discharging time from V_{HIGH} to V_{LOW} of C_{SENSE} in this work is 12.8% faster than [32].

Fig. 5.5(c) shows the comparison of power consumption. In general, more power is consumed when V_{HIGH} is greater. The average power consumption of this work is about 24.7% lower than [32].

The comparison data presented in this section is generated with all sensors having been tuned to provide exactly the same precision, in order that the circuit size, response time and energy comparisons are fair.

Finally, Fig. 5.5(d) shows the comparison of total energy used per round of sensing. In general, more energy is used when

V_{HIGH} is greater as well. The average energy usage of this work is about 32.7% lower than [32].

	Number of gates in [32]			Number of gates in this work			Difference
	core	counter	total	core	counter	total	
Inv.	63	104	167	43	19	62	63%
Buf.	4	0	4	2	0	2	50%
P. Trans	2	0	2	2	0	2	0
Trans Ga	1	0	1	1	0	1	0
Nand2	25	52	77	18	19	37	53%
Nand3	4	0	4	2	0	2	50%
LS	3	0	3	1	0	1	66%
Flip-Flop	0	52	52	0	20	20	62%
Total			310			126	59%

Figure 5.6: Implementation size comparison

Another way of tuning the precision vs. sensing delay and energy consumption trade-off is through adjusting the sizes of the upper and lower inverter chains in the event generator. The comparison data presented in this chapter is generated with all sensors having been tuned to provide exactly the same precision, in order that the circuit size, response time and energy comparisons are fair. Given the target of biomedical, environmental and mobile applications, the complexity of the solution is also an important metric. In general, the fewer transistors used, the lower the system unit price, and the faster a system will perform consuming less power and energy. Fig. 5.6 shows the comparison in terms of the number of gates and flip flops used between this work and [32]. In total, the design in [32] used 258 gates and 52 flip-flops. In this work, the circuits contain 106 gates, which is 59% fewer and 20 flipflops, which is 62% fewer.

5.2 CHIP RESULTS

5.2.1 *Test Setup*

5.2.1.1 *Fabricated chip*

Fig. 5.7 shows the micrograph of the tested chip based on 350nm AMS technology. It covers an total area of 0.996mm^2 with the bonding pads, 0.048mm^2 of which is covered by the core circuit, 0.116mm^2 by the 100pF on-chip capacitor and 0.05mm^2 by the 20-bit counter. The chip was packaged in 100-pin PGA package.

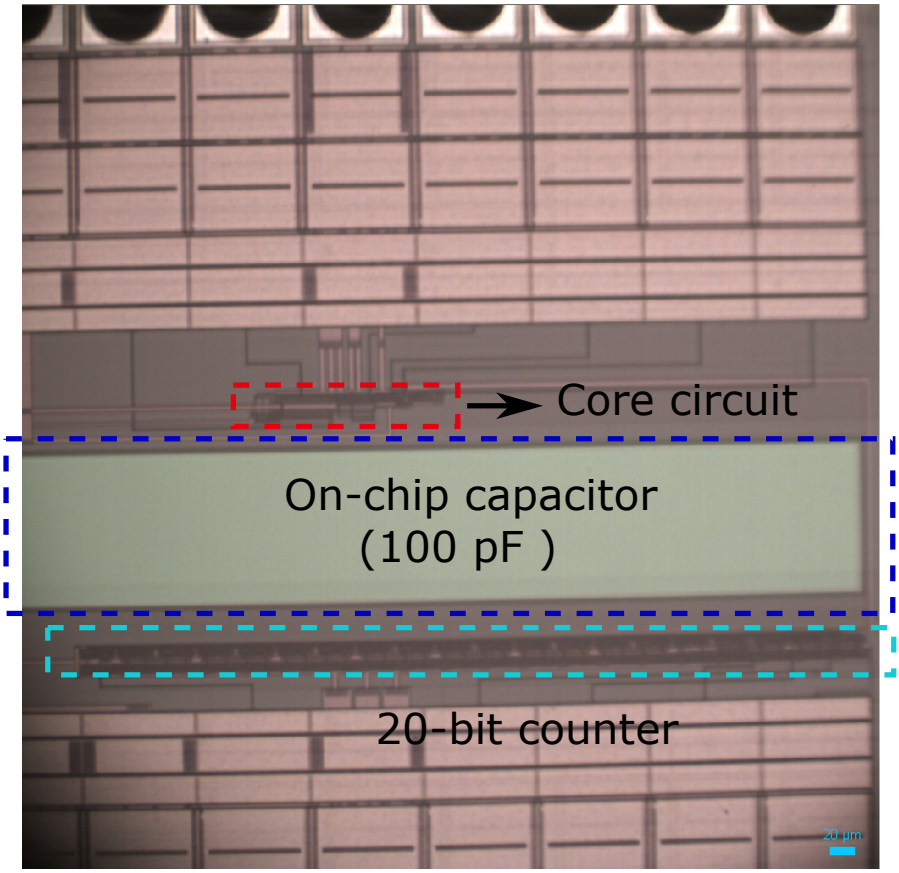


Figure 5.7: Test Chip Micrograph

5.2.1.2 *Printed Circuit Board and PGA sockets*

A customized single layer PCB with the dimension of 9.2cm by 6.38cm was designed and fabricated for testing the chip to make sure all the inputs and outputs of the chip have corresponding connection points on the board. Fig. 5.8 shows the layout of the designed PCB. In addition, A 169 contacts PGA socket shown in Fig. 5.9 is also needed to connect the chip with the PCB. The PGA contacts inside the socket and the PCB are soldered together instead of directly soldering the pins on the tested chip with the PCB. Hence, it is easy to detach the chip from the PCB for other purpose of use. Fig. 5.10 shows the tested chip on the PCB with the PGA socket in between.

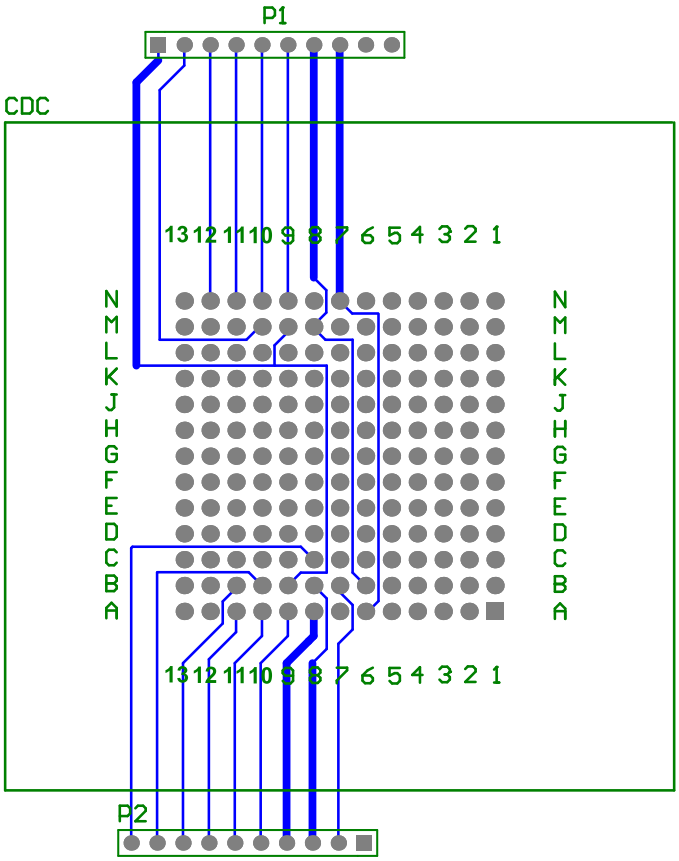


Figure 5.8: Test PCB layout

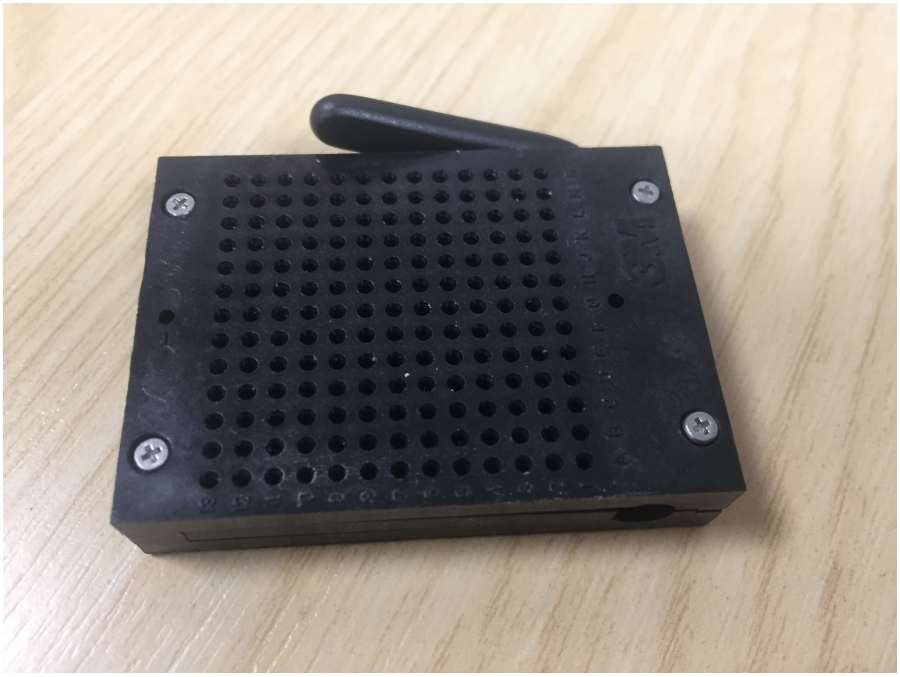


Figure 5.9: 169 Contacts PGA Socket

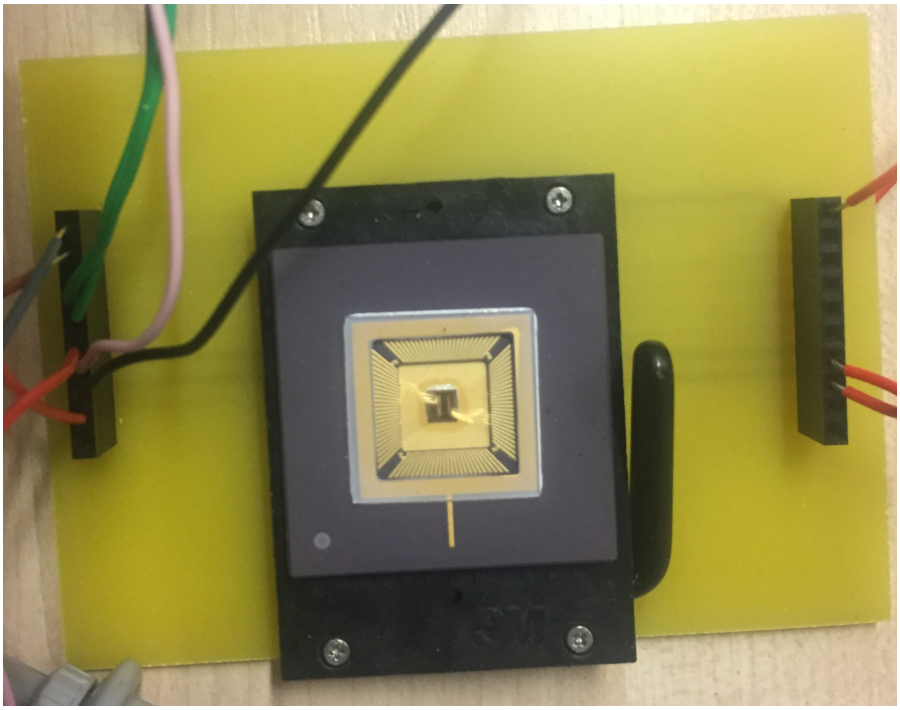


Figure 5.10: final chip

5.2.1.3 *Equipment*

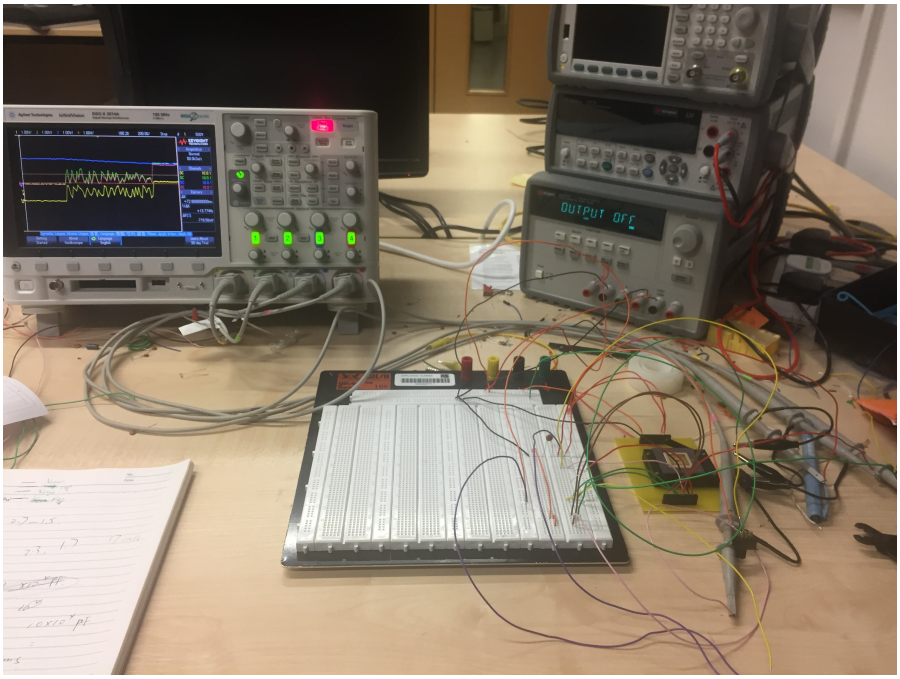


Figure 5.11: Picture of the test setup

Fig. 5.11 shows the equipment used to test the chip. The PCB is connected to a power supply source (Keysight E3631A) and a digital storage oscilloscope (Agilent Technologies DSO-X 2014A). The Keysight E3631A power supply provides two voltage outputs. One for charging the sensed capacitance and one for powering the chip. The Agilent Technologies DSO-X 2014A Mixed Signal Oscilloscope shows the resulting waveform of the output signals generated by the chip.

5.2.2 *Test Result*

Fig. 5.12 and Fig. 5.13 show the operations of the QDC under different values of capacitances. In Fig. 5.12, V_{HIGH} is set to 2.5V, V_{LOW} is set to 1.5V and an off-chip capacitor C_{SENSE} is set to 10µF. The result shows that Signal(H) starts to drop from 1.7V,

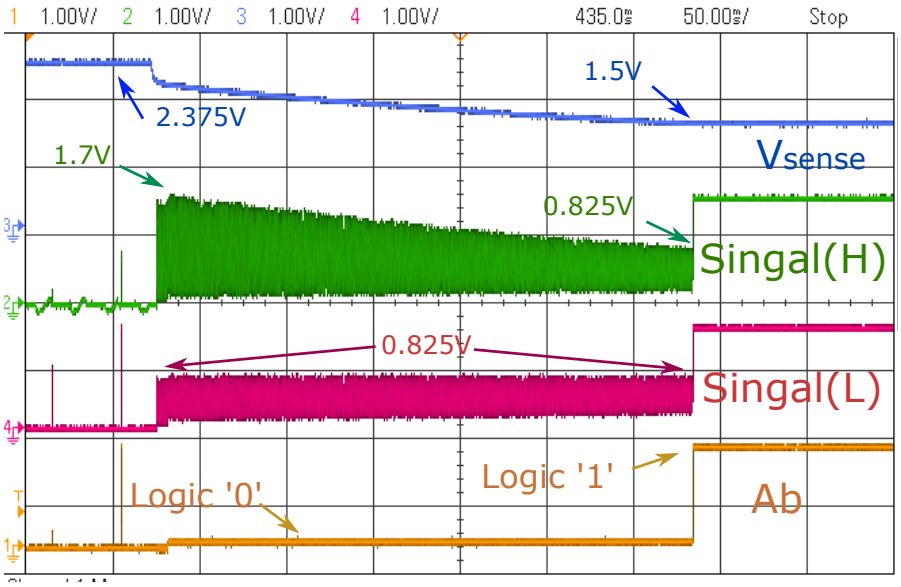


Figure 5.12: Chip performance with a 10µF capacitor

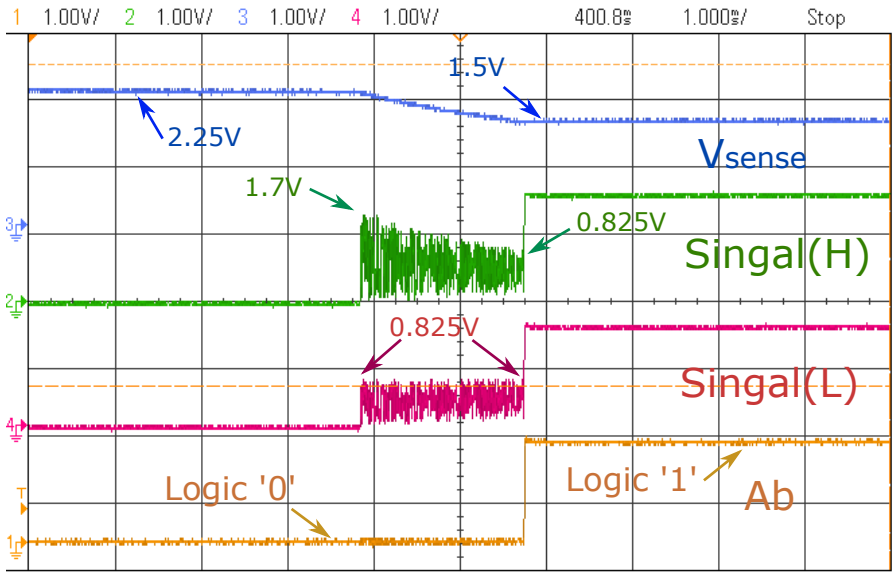


Figure 5.13: Chip performance with a 100nF capacitor

until the voltage exactly equals to Signal(L), which is 0.825V. Once the delay of Signal(H) and Signal(L) become the same, 'Ab' triggers from logic '0' to logic '1'. The discharging time is 485ms. Compared with Fig. 5.12, Fig. 5.13 shows the operation under a 100nF off-chip capacitor and the rest setup remains the same. As can be seen, the obvious difference is that the discharging time decreases to 1.8ms with less iteration for both Signal(H) and Signal(L). In other words, for discharging a capacitor from one value to another value in the QDC, the smaller the capacitor is, the less time it takes.

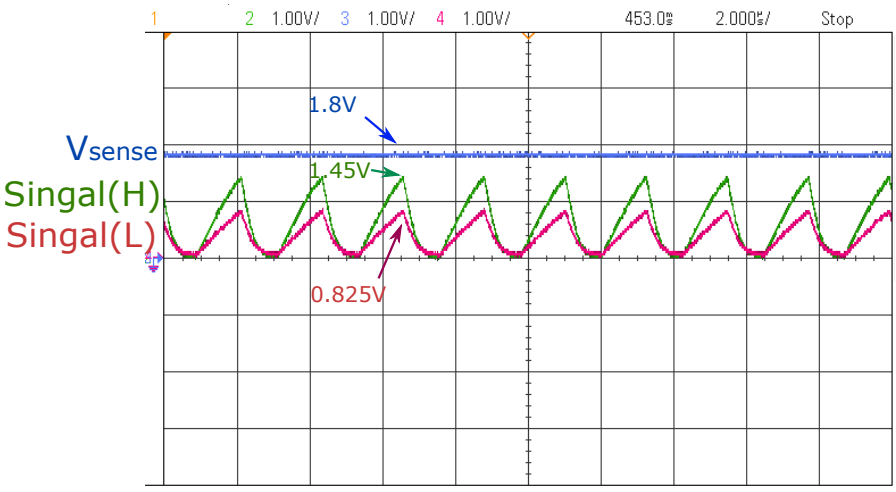


Figure 5.14: Zoom-in signals when V_{SENSE} drops to 1.8V

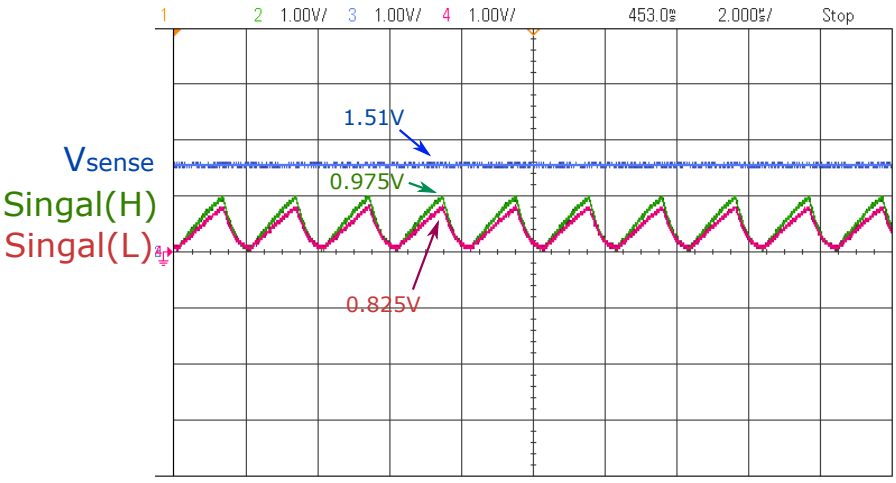


Figure 5.15: Zoom-in signals when V_{SENSE} drops to 1.51V

Fig. 5.14 and Fig. 5.15 show the zoom-in signals during the operation in Fig. 5.12. Fig. 5.14 shows when V_{SENSE} drops to around 1.8V. In this scenario, Signal(H) comes earlier than Signal(L) with a higher peak amplitude. Fig. 5.14 shows when V_{SENSE} drops to around 1.51V. In this scenario, Signal(H) still comes earlier than Signal(L) with a higher peak amplitude but with a smaller delay comparing with Fig. 5.14.

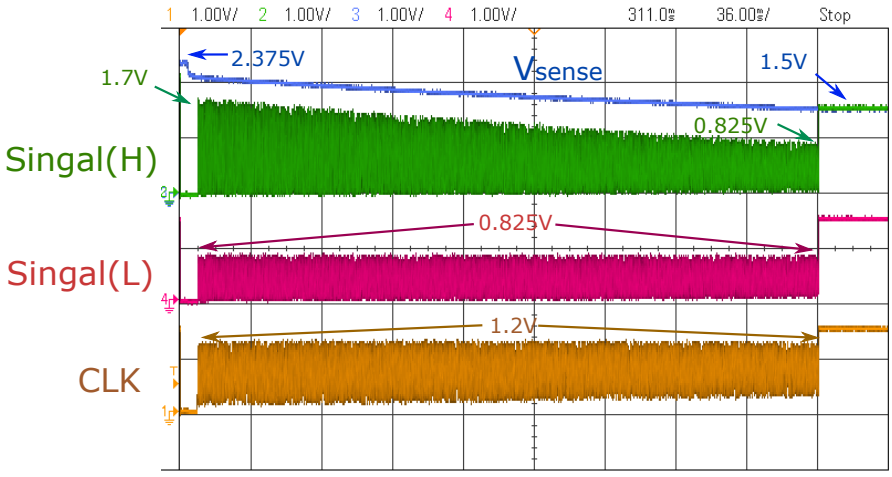


Figure 5.16: Chip performance with the 'CLK' signal

The on-chip 100pF capacitor test did not show the sufficient result. By analysing the performance of the off-chip capacitor test, the cause may be the malfunction of the level-shifter for two reasons. Firstly, The level-shifter drains some power from C_{SENSE}. In 90nm technology, the power consumption for level-shifter is tolerable and the upper inverter chain in the event generator drains most of the energy from C_{SENSE}. However, in the 350nm technology chip, for testing a 100pF on-chip capacitor, which stores relatively small charge in C_{SENSE} (Q=CV), the level-shifter consumes most of the energy from C_{SENSE}. In this scenario, C_{SENSE} provides limited energy to drive the upper inverter chain. The discharging of C_{SENSE} is then not slow enough to generate a code. Hence, it is impossible to test with

the on-chip capacitor. Secondly, the level-shifter may not work as expected to drive the 'CLK' signal to the required voltage. That may be why in Fig .5.16 (same setup as in Fig. 5.12), the off-chip capacitor test shows that the peak values of Signal(H) and Signal(L) are lower than expected. The peak value of Signal(H) should be the same value as V_{SENSE} and the peak value of Signal(L) should be 1.5V. Meanwhile, the peak value of 'CLK' signal (before inputting to the level shifter) is 1.2V which performs better than Signal(H) and Signal(L).

Testing with an off-chip capacitor inevitably is less ideal compared with testing with an on-chip one. Other additional issues include losses across off-chip wires and chip interfaces. However, qualitatively, the chip results still show the correct trends of the signals. Signal(H) and Signal(L) do stop oscillation once their delay become the same, i.e. V_{SENSE}=V_{LOW}, by triggering the signal 'Ab'.

5.3 SUMMARY

This Chapter firstly showed the simulation results of the QDC and the output codes when it is sensing capacitance and voltage. Compared with [32], it saves 25% and 33% on power and energy consumption respectively. The use of number of gates is also reduced 57% which means the new method has a less system complexity. The fabricated chip is also showed in this chapter as well as its performance. Unfortunately, the on-chip capacitor test did not show the sufficient result possibility due to the malfunction of the level-shifter which will be redesigned and improved in the future. However, qualitatively, the off-chip

capacitor testing results shows the correct trends during the operation of sensing.

6

CONCLUSIONS AND FUTURE WORK

6.1 SUMMARY AND CONCLUSION

In this thesis an all-digital QDC was proposed as a sensor interface for sensing capacitance and voltage. Compared to a CDC which uses the sensed capacitance value as a simple signal, a QDC is used to convert the amount of charge stored in a capacitor to a binary output code. The stored energy can also be used as a part of power supply for the circuit which saves the power.

Chapter 3 discusses the design steps from an RC load CDC to the proposed digital solution. The general theory of capacitance/voltage to digital conversion through discharging for sensing both capacitance and voltage is presented in this chapter as well. For capacitive sensing, it achieves linearity between the output codes and the sensed capacitance value. For voltage sensing, the output codes are related to the sensed voltage value logarithmically, which displays a variable precision across the sensing voltage range.

Chapter 4 shows the detailed implementation of the proposed QDC with an asynchronous solution. It compares the propagation delay of two inverter chains separately powered by a charged capacitance and a reference voltage by an event comparator. Different from other existing digital CDCs, this design introduces a new detection mechanism in the event comparator which directly detects a charged capacitance discharging to a

reference voltage without using extra delays. This removes the need for any extra correction. As a result, in this solution, all possible metastability is restricted to one point. The MUTEX inside the event comparator is used to filter out any propagation of possible metastability at this one point. By doing this, the system complexity is reduced.

Chapter 5 presents the simulation results of the design which proved the theory discussed in Chapter 3. The new method has less than half the circuit size, and 25% and 33% savings on power and energy consumption with less response time and system complexity compared with the state of art benchmark. Besides, the system performance is not affected. A test chip was fabricated in a 350nm AMS technology consisting of the QDC. The chip results shows the correct trends during the operation of sensing.

6.2 FUTURE WORK

Although there are many advantages of the presented research, there are still some aspects needed to be improved. For example, the charging and discharging are manually controlled so noise might appear during the moment the circuit starting to discharge. The wire resistance is not fully considered as well. These needs to be discovered in the future.

Moreover, many further research topics can be explored based on the proposed theory and architectures in this thesis. Some recommendations for the future work are presented below.

Due to the fact that the test chip was fabricated on a 350nm AMS technology, it requires a higher supply voltage. As a result, the overall power consumption was not low. The level-shifter

should be improved to provide a better performance. A fabrication of the design in a lower geometry could bring a better system performance.

The QDC as a sensor interface is a core part of the sensor. In the next step, a complete sensing system may be designed with the proposed QDC implemented, i.e. a dual use sensor for capacitive and voltage sensing. Moreover, this is a one channel QDC. In future, it would be desirable to design a multi-channel sensing system as in many sensing environments, more than one channel is needed to sense different targets at one time.

This work opens up exciting new opportunities of research in related areas. For example, the wearable/implantable wireless sensor system is challenging due to the total system power/energy budget. These types of sensor measure various physical quantities which may based on the capacitance values. Another application is EH systems, voltage levels are monitored during energy accumulation. One hot trend for EH systems is batteryless where low power consumption is very important. Our QDC may be a potential candidate for it.

Backmatter

Part II

Thesis Appendices

A

SCHEMATIC OF THE DESIGNS

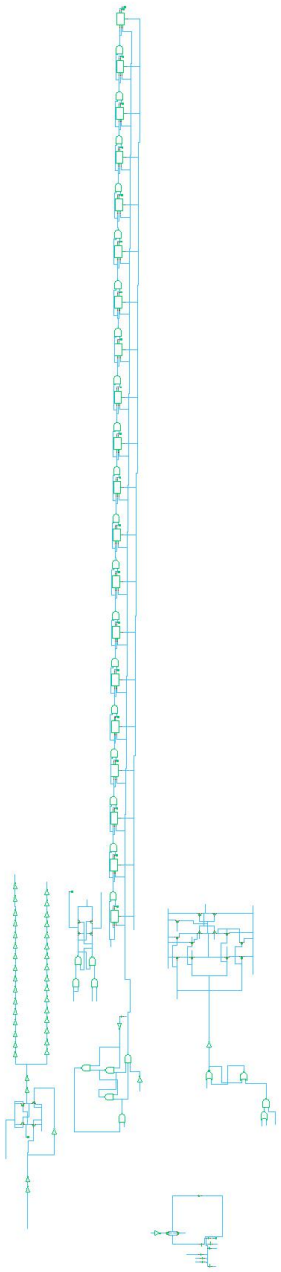


Figure A.1: Schematic of QDC design in 90nm technology

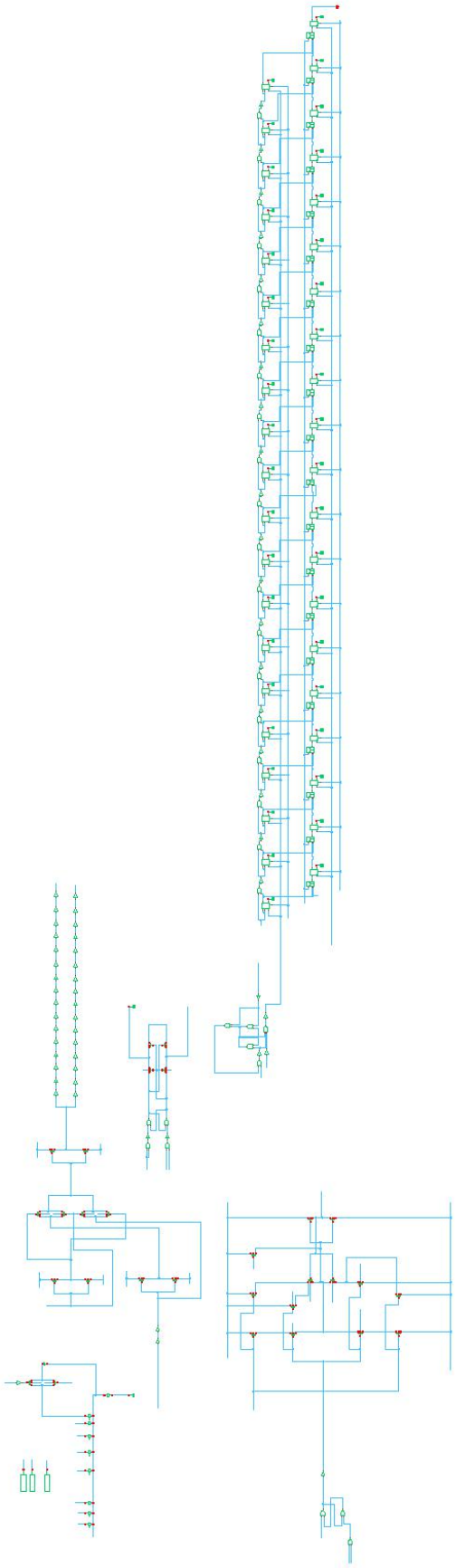


Figure A.2: Schematic of QDC design in 350nm technology

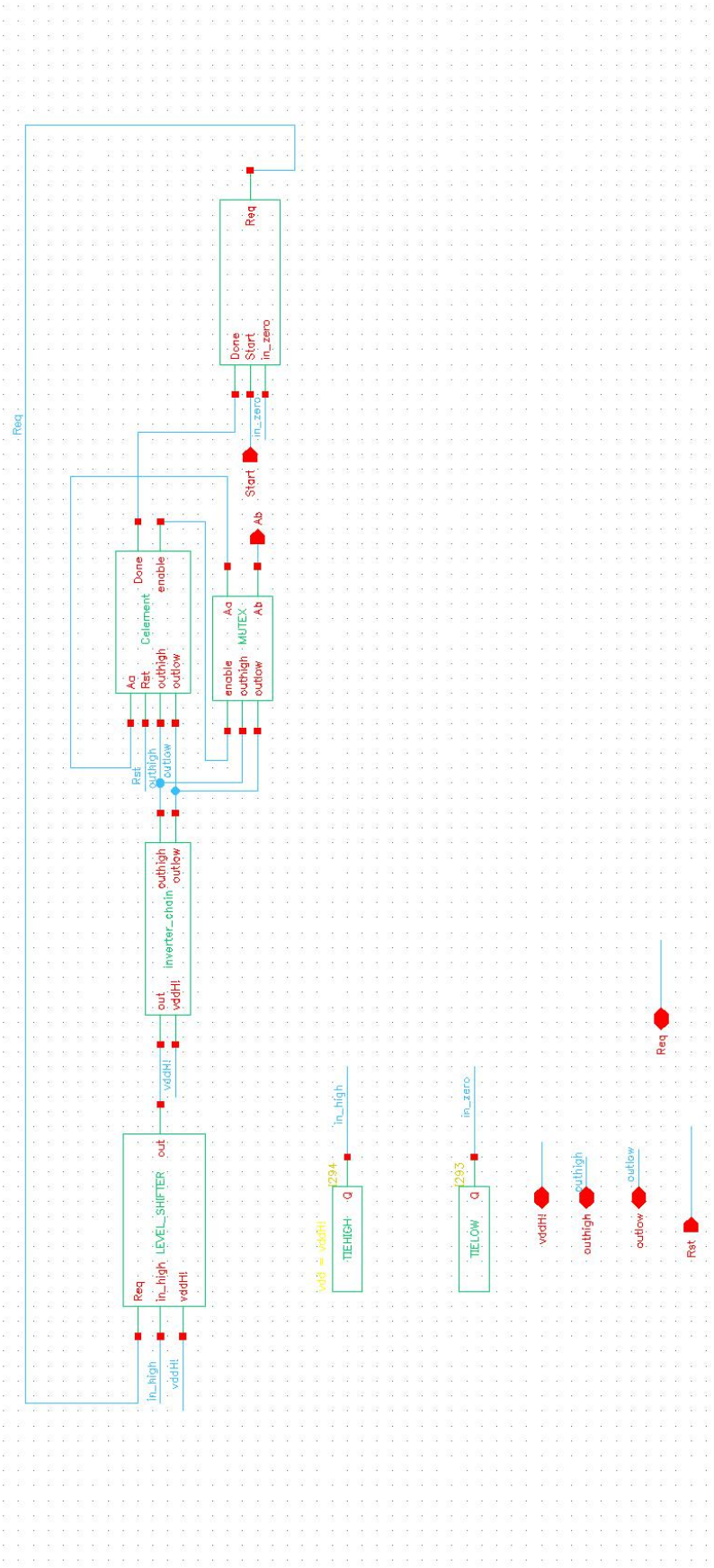


Figure A.3: Schematic of blocks for the core circuit in 350nm technology

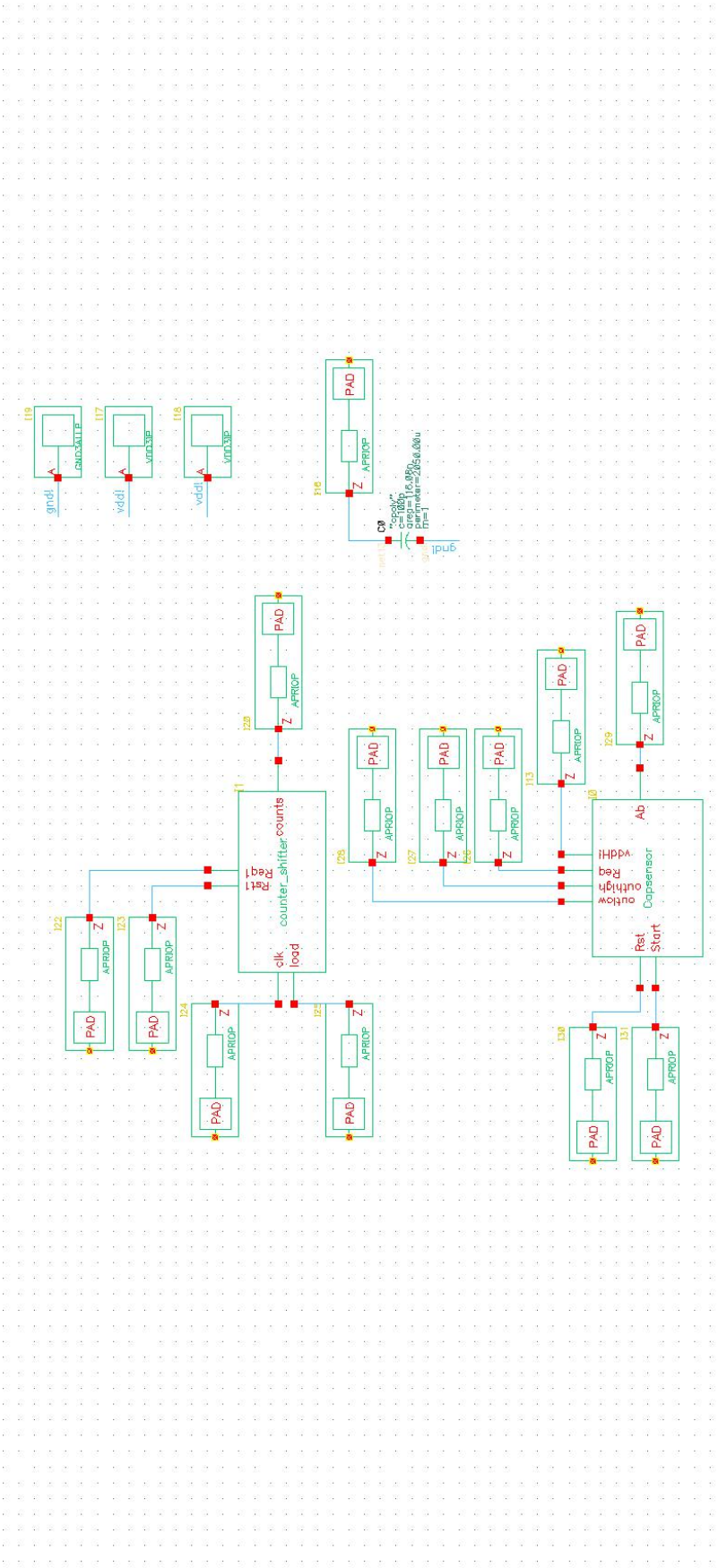


Figure A.4: Schematic of blocks for the complete design in 350nm technology

Part III

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