Online ISSN 1848-3380, Print ISSN 0005-1144
ATKAFF 54(2), 210–216(2013)

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Design and Implementation of a Low Supply Voltage Voltage Type Sense Amplifier with Low Current Consumption for RFID Transponder

DOI 10.7305/automatika.54-2.119
UDK 621.375.4.027.2
IFAC 4.4

Original scientific paper

Current or voltage-type sense amplifier (SA) is the key element for sensing process of RFID transponder EEPROM. The performance of the EEPROM is influenced by the SA features like memory access time, power dissipation and the reliability. However, larger current or power dissipation put limitations on using current type SA with respect to voltage type SA. A low voltage SA with lower current consumption is presented in this research work, which is compatible with the low power applications like RFID transponder EEPROM. In this research, 0.18μm process is employed to design the low voltage SA with lower power consumption. The simulated results of the output showed that voltage type SA is able to operate under a low power supply voltage (VDD). In addition, only 32 μA current is dissipated by the modified voltage type SA during read period. Moreover, the proposed voltage type SA provides better reliability than the circuits presented in other research papers.

Key words: Transponder, EEPROM, RFID, Sense amplifier

Dizajn i implementacija naponskog mjernog pojačala za RFID transponder s niskim naponom napajanja i malom potrošnjom struje. Strujno ili naponsko mjerno pojačalo (MP) je ključni element očitanja RFID transpondera s EEPROM-om. Na učinak EEPROM-a utječu svojstva pojačala kao što su vrijeme pristupa memoriji, energetski gubici i pouzdanost. Veliki gubici struje i energije ograničavaju mogućnost korištenja strujnog mjernog pojačala u odnosu na naponsko. U ovom radu prikazano je niskonaponsko mjerno pojačalo s malom potrošnjom energije koje je prikladno za korištenje kod RFID transpondera s EEPROM-om. Koristi se proces od 0.18μm za dizajniranje niskonaponskog pojačala male potrošnje. Simulacije izlaznog napona su pokazale da naponsko mjerno pojačalo može raditi s niskim naponom napajanja. Tijekom vremena očitanja na modificiranom naponskom pojačalu troši se samo 32μA struje. Predloženo naponsko mjerno pojačalo ima bolju pouzdanost od onih prikazanih u drugim člancima.

Ključne riječi: transponder, EEPROM, RFID, mjerno pojačalo

1 INTRODUCTION

In low voltage applications like RFID transponder, EEPROM is used as a storage device. RFID is the technology for automated identification of products, objects or human. RFID system requires EEPROM memory for high-speed read/write operation. At present, a key design aspect for RFID tag IC is the low power dissipation and low cost [1-3]. Therefore, in RFID transponders embedded non-volatile memories (NVM) like EEPROM play a vital role. In fact, EEPROM has become very significant alternative for any application requiring NVM over the last few years [4].

Reading/writing process is the most significant factor for low-power RFID transponders EEPROM [5-6]. The power of the EEPROM SA must be low to increase RFID reading speed [7]. In EEPROM, the read access time is a key factor to determine the read path, which is strongly affected by the SA. One of the main challenges for new generation NVM is to develop a robust and high-speed read circuit with a low VDD. As the power supply becomes lower, the design of a high-speed low-power SA becomes very critical [8-9]. Moreover, the reliability of the SA has to be improved to make consistent operations of RFID transponders.

Generally, the current sensing method is widely employed to design a conventional SA in EPROM read operation. Due to the advanced speed and reliability features, current type SA has been used more frequently than volt-

age type SA [9]. However, conventional current sensing method has the drawbacks of higher power dissipation and larger time for sensing. Moreover, current type SA requires extra control logic to prevent incorrect read out current. As a result, current type SA is unacceptable to low power applications like RFID transponders. Consequently, lower current and power consumption made voltage type SA superior to current type SA, which is compatible in RFID tag EEPROM [9-10].

To attain reduced sensing current, numerous voltage-type SA circuits have been designed for NVM. However, at lower VDD the reading consistency issues and higher reading current is experienced by the researchers [11]. In 2009, Liu et al. proposed voltage type SA with low cost, low power and reliability. The circuit is implemented using SMIC 0.35μm CMOS process [12]. In $VDD = 3.3$ V the charging time is 35 ns for the voltage type SA. In addition, the highest average current consumption during the sense period is 40μA. However, the lowest VDD required for the design was 1.4 V. However, the voltage claimed by Liu et al. is not as low as VDD for RFID transponder.

In this research, a low voltage SA for EEPROM memories in RFID tag is designed to attain the lower reading current/power. This design overcomes the limitations of the conventional current SA. Low voltage sensing method has been used in this design to achieve better circuit performance, and decreasing sensing time. To reduce the reading current/power an additional capacitor is used in this design. The proposed low voltage-type SA is designed in CEDEC $0.18 - \mu$m CMOS process. Simulations results show that the modified low voltage-type SA performs better than the SA designed by Liu et al. [12].

2 CONVENTIONAL SA

Though the floating-gate devices have many limitations, low power design on circuit level is still the best solution for RFID applications [13]. NVM type EEPROM circuits block diagram is shown in Figure 1, where the NVM cell array is used to store data.

The control unit, row and column decoders and high-voltage switches are used inside EEPROM to control logic operations. On the other hand, the charge pump is used to generate a high voltage for writing operations. The SAs are useful for sensing the *'0'* and *'1'* bit. Whereas, the input/output (I/O $< 7 : 0 >$) interface is used for transferring output data.

Several researchers treat the design of conventional SAs using current sensing method [7, 9, 14]. Figure 2 shows the circuit diagram of the conventional SA.

In the conventional SA circuit, the measurement of *'0'* and *'1'* is classified by using a differential circuit for reliability between the read out current and a reference current. However, the circuit has some drawbacks:

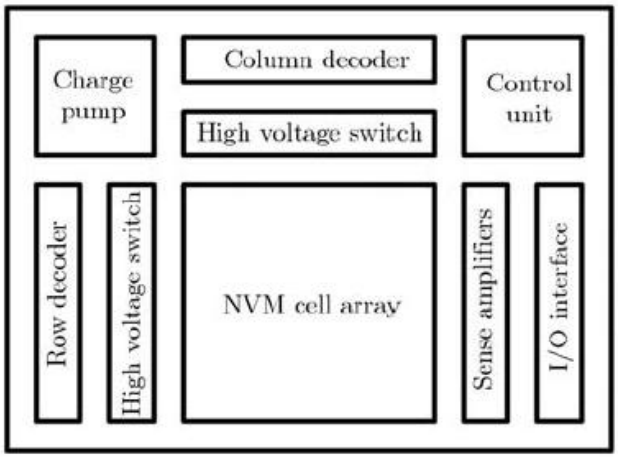

Fig. 1. Block diagram of an EEPROM [10]

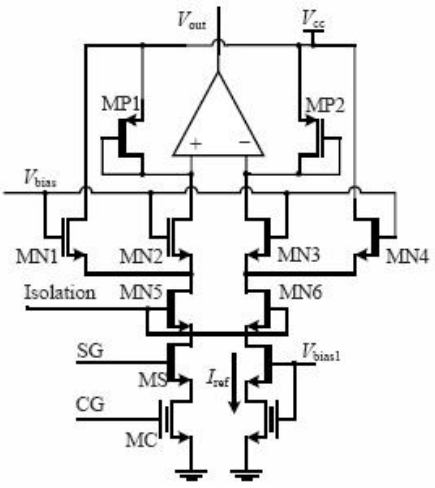

Fig. 2. The circuit diagram of conventional SA [7, 9, 14]

1. High power consumption is pointed as the most common problem of the conventional SA. A large reference current I_{ref} is required by the conventional SA circuit to differentiate between '0' and '1' data, which is typically the average of the read out currents. Tens of μA reference current is needed for reliability [10]. Thus, a large amount of read out current: $I_{ref}\varepsilon(nI_{ref}, 3nI_{ref})$ is required for the conventional SA for reading parallel data. Where, n is the number of bits read out in parallel [12].

2. Floating gate transistor changes the *'0'* and *'1'* current levels by attribute degeneration. Thus, for *'0'* and *'1'* the perfect selection of I_{ref} is differed from the initial average of the read out currents. Therefore, a minor variation between the read out current and the refer-

ence current for one level to other is produced. This distinction of the current necessitates more time for sensing [15].

3. The conventional SA circuit is constructed with many floating gate transistor which store charge. Hence, it is important to use an extra control logic circuit to prevent incorrect read out current and correctly manage the charge stored on key nodes.

However, to reduce the sensing time and to make the power consumption lower, a low voltage SA is essential for non-volatile memories like EEPROM in RFID tag. Moreover, to avoid incorrect read out current, the low voltage SA will not require an extra control logic circuit.

3 PROPOSED SA

The compact model (CM) of the floating gate (FG) [16] devices has been used in conventional SA for circuit simulations. However, this compact model experienced two main limitations. First, thin gate oxide transistors with lightly or medium-doped drain (LDD/MDD) diffusions are the main aim of MOS compact model. More than 7nm thickness is used as the oxide of the FG devices while the source and drain junction is usually abrupt. As a result, the existing transistor models might become essential to adapt with this same type of devices. Second, between the control gate node and the source, drain and body nodes, few coupling capacitance exist. Moreover, two neighbor cells may be affected by the coupling capacitance as memory cells are getting closer and smaller one to each other. Based on these limitations, a voltage-mode SA is designed with only one capacitor between the control gate node and the source, drain and body nodes. This method reduces the effect of coupling capacitance between the transistors. Moreover, this method is useful to achieve the lower sensing power/current and higher reading fidelity without speed deprivation compared to the conventional SA.

Figure 3 shows the improved designed SA circuit composed of charge controlling and voltage sensing circuits. The memory cell consist of a FG transistor MC and a select transistor MS. To reduce the coupling capacitance between two adjacent memory cells only one capacitor has been used between the control gate and the FG node (which is the gate of the MOS transistor MC).

In the modified SA, the selected sensing path is controlled by the control gate (CG) and transistor MC and a selecting gate (SG) with the transistor MS. The task of the decoders is to control this selecting gate and the terminal CG is determined by a voltage between the two thresholds of memory cells.

For the improved voltage-type SA, the EEPROM memory cell implemented in 27°C operating conditions of the

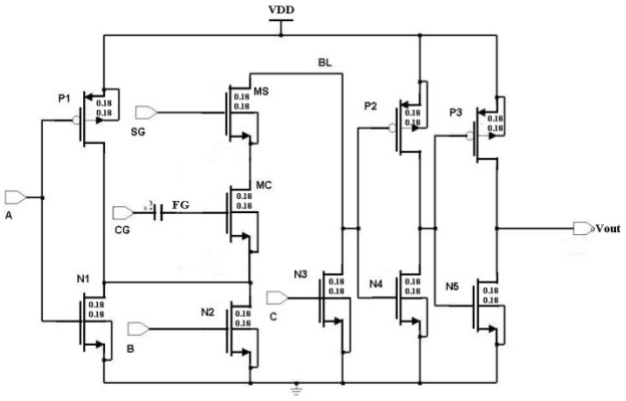

Fig. 3. Schematic diagram of the proposed low voltage-type SA

CEDEC $0.18-\mu$m CMOS process. The threshold voltage of transistor MC is set to 1.5V to store a $'0'$ signal; and the threshold voltage is set to -1V to store a $'1'$ signal. Fig. 3 shows that the operation states of this SA are controlled by the three control terminals: A, B and C.

This modified voltage SA has two states: working state and out-of-work state. In the out-of-work state, to ensure the drain and source of the memory cell are at low level, all the three inputs A, B and C are set to $'1'$. On the other hand, for the working state, voltage on CG is $V_{CG} = (P+Q)/2$ and voltage on SG is $V_{SG} = V_{dd}$ where, P is the threshold voltage of the MC when storing a $'0'$ signal, and Q when storing a $'1'$ signal.

At the beginning to turn off N2 and N3 transistor, inputs C and B are set to $'0'$. After that, A is set to $'0'$. At this time, $V_{out} = 0$ when the stored signal of MC is $'0'$. Additionally, when the stored signal is $'0'$, the BL (bit line) is charged to $V_{BL} = min(V_{dd} - V_{tms}, 1.5 - V_{tmc})$, where, V_{tms} is the threshold voltage for MS transistor, and V_{tmc} is the threshold voltage for transistor MC. The stored signal $'1'$ will be generated correctly at V_{out} as long as, $V_{BL} > \frac{V_{dd}}{2}$.

In Figure 3, for sensing the stored voltage $'0'$ or $'1'$ at transistor MC, the drain and source of MOS transistors employ bidirectional conduction [11]. This voltage mode SA enables costs to be reduced; since it has no bias circuit. The parasitic capacitance is utilized as the charging load at the drain of N3 transistor. To decrease the charged voltage, the threshold voltage of the two inverter composed of NMOS transistors N4, N5 and PMOS transistors P2, P3 have been added. This will result in a shorter charging time of BL and makes the lower read power dissipation. Additionally, the modified voltage type SA is capable of resisting the degeneration features of the floating gate transistor by using a voltage sensing method rather than a current sensing method. The transient current and charges for charging in

one read process are described respectively, by the following equations:

$$\frac{\partial(V_{BLT}C_{N3})}{\partial t} = \beta(V_{CG} - V_{tmc} - V_{BLT})^2 \quad (1)$$

$$\int_0^T \beta(V_{CG}-V_{tmc}-V_{BLT})^2 dt = C_{N3}(V_{CG}-V_{tmc}) \quad (2)$$

where, V_{BLT} is the transient voltage of the BL, C_{N3} is the parasitic capacitance at the drain of N3 , and T is the charging time $\beta = \mu_n C_{ox} W/(2L)$.

Using equation (1) and (2), the average charging time and current can be obtained during one read period.

4 RESULTS AND DISCUSSION

The 27°C operating condition has been set for the modified voltage-type SA and the conventional SAs.They are designed and simulated in CEDEC 0.18μm CMOS process. Simulations are done to evaluate the circuit performance of the modified SA with the previously reported voltage type SA [12]. The transistors involved in the sensing circuitry were of equal size $W/L = 0.18\mu/0.18\mu$. The significant design factors are listed in Table 1.

Table 1. Main design parameters

VDD (Min/Max)	C1	W/L	SG	CG
1V/3V	0.1pF	$0.18\mu/0.18\mu$	3V	1.5V

By using, the critical design parameters listed in the above table the output data $V(out)$ for the modified SA is shown in Figure 4 under 2.6 V as VDD. As shown in Fig. 4 the modified voltage type SA reads $'0'$ data at the beginning. At 0.4μs the SA reads $'1'$. The circuit is also able to work for the supply voltage longer than 2.6 V, but above this operating voltage, the circuit experiences noise.

Furthermore, depending on the principle of the memory cell, VCG in equation (1) is the best value for voltage sensing and a lower voltage can be set for VCG. By equation (2) and regulating the threshold voltage of the inverter in Figure 3, the modified voltage mode SA is capable of operating at voltages as low as 1 V. The V_{out} data for a 1 V as VDD are shown in Figure 5.

The simulation results in Figure 5 show that the voltage required by the voltage-type SA can be significantly reduced from 2.6 V to 1 V, where the voltage was controlled by CG. In order to show the correct behavior of the voltage-type SA, the VDD is set to 1 V and the capacitive load to 0.1 pF.

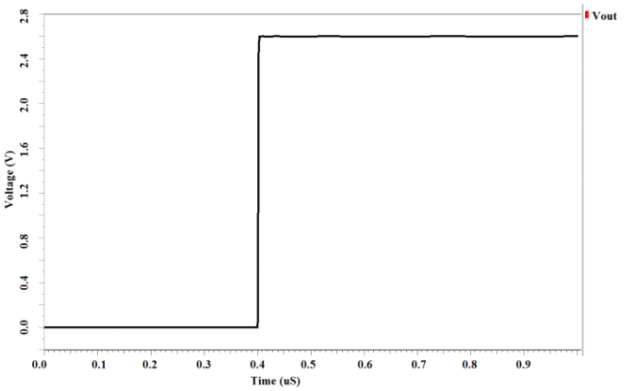

Fig. 4. Simulation waveforms of $V(out)$ under $VDD = 2.6V$

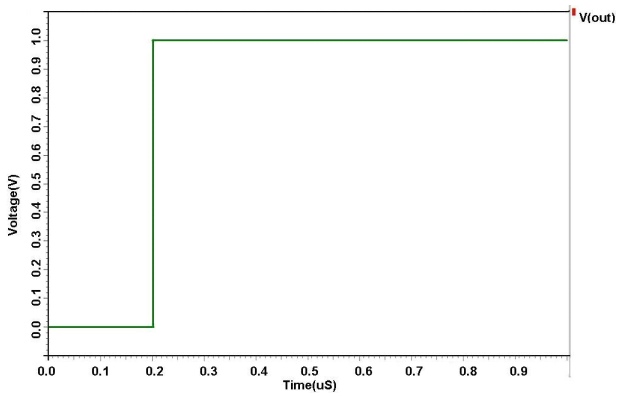

Fig. 5. Simulated waveforms of $V(out)$ when $Vdd = 1V$

The corresponding current consumption for the modified voltage type SA is shown in Figure 6. Here the average current consumption during the read period is only 32μA for the maximum clock speed of 20 MHz. This feature is useful for some electronic systems focused on low voltage and low power such as RFID transponder.

Figure 7 presents a comparison results among the V_{out} data, the average current consumption during the read period, and the corresponding bit line voltage under 1 V as VDD. The figure further proves that the SA is capable of operating at a voltage as low as 1 V. The circuit is also able to work for the supply voltage longer than 1 V, but in this operating voltage, the circuit experiences noise.

Generally, the required working temperature range of the RFID tag is from -25°C to 85°C. As, the modified voltage-type SA circuit is able to work within the temperature range from -25°C to 125°C. Therefore, this modified circuit has no power differentiation in working temperature of RFID tag.

A performance evaluation study of voltage type SA between this work and Liu et al. on the low voltage function-

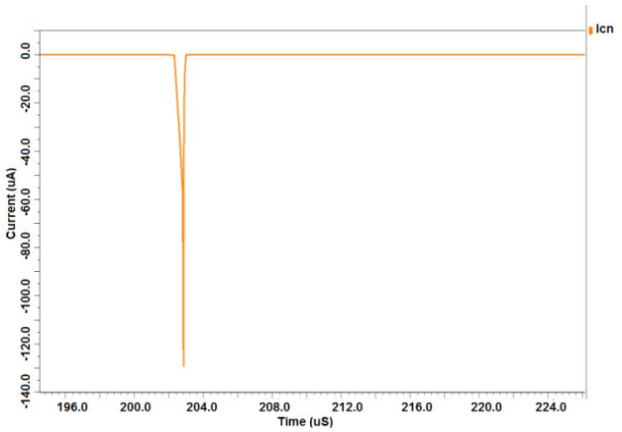

Fig. 6. Simulation waveforms of the current consumption I_{cn} for voltage type SA

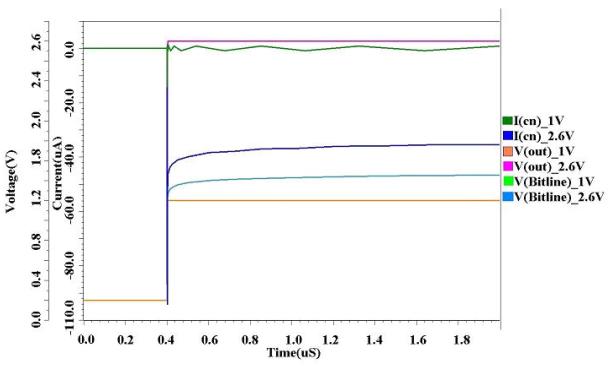

Fig. 7. Simulated waveforms of I_{cn}, $V(out)$ and $V(BL)$ under $VDD = 1V$

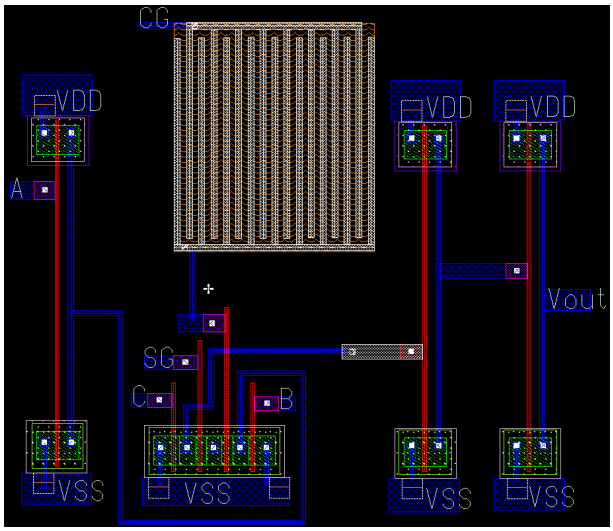

Fig. 8. A layout design of the low voltage-type SA

ality with current consumption is shown in 2.

Table 2. Performance evaluation of the voltage-type SA between Liu et al. and this work

Research	**CMOS Technology**	**Vdd (Min)**	**Vdd (Max)**	**Average current consumption**
Liu et. al.	0.35μm	1.4 V	3.3 V	40μA
This Work	0.18μm	1 V	2.6 V	32μA

From the study, it is shown that the circuit is able to work within 1 V to 2.6 V as VDD, which is lower than the Liu et al. Moreover, the modified circuit required lower current 32 μA during read period, whereas, Liu et al. SA consumed 40 μA. Hence, the comparison study proves that the proposed voltage type SA performs better than Liu et al.

The modified low voltage-type SA circuit layout is designed in CEDEC 0.18-μm CMOS process. In Figure 8, the completed chip layout of the modified low voltage SA is presented. In this layout, the capacitor connected with the control gate transistor is about 0.1pF. This small capacitor only takes a small area of the circuit to reduce the cost of the whole chip. In this research, $W/L = 0.18\mu/0.18\mu$ is the size for each cell of the MOS transistors, which also proves that the modified SA circuit size is lower than the circuit size designed by Liu et al.

5 CONCLUSION

An improved design and a comparative study of low voltage SA circuit using a voltage sensing method is presented in this research. The modified circuit has been designed by using the CEDEC 0.18-μm CMOS embedded EEPROM process. In this research, the bidirectional conduction between the drain and source of MOS transistors is used to sense the stored voltage *('0'/'1')* at the floating gate transistors. According to the performance evaluation results, it has been proven that, the circuit is capable of working under a low voltage range from 1 V to 2.6 V. Moreover, the required current dissipation during read period for the proposed design is lower than the design of Liu et al. Furthermore, the measured results confirm that this low voltage SA is free from the power delineation caused by the temperature change. Additionally, the circuit size reduced significantly by using small transistors and capacitors.

ACKNOWLEDGMENT

This work was supported by the researh grant Arus Perdana (UKM-AP-ICT-20-2010) and Brain Gain Malaysia (MOSTI/BGM/R&D/20) from Universiti Kebangsaan Malaysia and the Ministry of Science, Technology and Innovation (MOSTI) respectively.

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Received: 2011-10-08
Accepted: 2012-06-30