ISSN 1330-3651 (Print), ISSN 1848-6339 (Online)
UDC/UDK 621.382.049.77:621.374.4

A CMOS POWER SPLITTER FOR 2,45 GHz ISM BAND RFID READER IN 0,18 µm CMOS TECHNOLOGY

M. Jasim Uddin, Anis N. Nordin, M. B. I. Reaz, Mohammad Arif Sobhan Bhuiyan

Original scientific paper

Radio frequency identification (RFID) is one of the most rapidly growing technologies to be utilized in almost every sector for storing and retrieving data wirelessly. Current advancements in CMOS technology help the scientists and technologists to reduce the size and improve the functionalities of the RFID circuits. In this paper, the design of an RF-CMOS power splitter circuit in 0,18 µm Silterra RF-CMOS technology is illustrated for a 2,45 GHz RFID reader. Wilkinson power divider is chosen for the proposed power splitter circuit with on-chip inductors and capacitors. The proposed power splitter achieves a maximum insertion loss of 10 dB. AWR Microwave Office® is used for the simulation of the circuit and for determination of its S-parameters. To design the inductors with accurate values in 2,45 GHz Sonnet® is used whereas Cadence® is used for capacitor and resistor layout.

Keywords: *CMOS (Complementary metal–oxide–semiconductor), RFID, Reader, Power splitter*

CMOS razdvajač snage za 2,45 GHz čitač polja ISM RFID u 0,18 µm CMOS tehnologiji

Izvorni znanstveni članak

Identifikacija radio frekvencije (RFID) je jedna od najbrže rastućih tehnologija uporabljiva u gotovo svakom sektoru za pohranu i bežično uzimanje podataka. Trenutni napredak u CMOS tehnologiji pomaže znanstvenicima i tehnolozima smanjiti dimenzije i poboljšati funkcionalnost RFID sklopova. U ovom radu ilustrirana je konstrukcija jednog RF-CMOS razdvajača snage električnog kruga u 0,18 µm Silterra RF-CMOS tehnologiji za 2,45 GHz RFID čitač. Wilkinsonov razdjelnik snage izabran je za predloženi razdvajač snage električnog kruga s induktorima i kondenzatorima na čipu. Predloženi razdvajač snage ostvaruje najveći gubitak zbog umetanja od 10 dB. AWR Microwave Office® koristi se za simulaciju električnog kruga i za određivanje njegovih S-parametara. Za konstruiranje induktora s točnim vrijednostima u 2,45 GHz rabljen je Sonnet® dok je Cadence® rabljen za razmještaj kondenzatora i otpornika.

Ključne riječi: *CMOS, RFID, čitač, razdvajač snage*

1 Introduction

Power splitters split the power from a single port to two or more ports in load circuits by a certain percentage depending on the architecture. Power splitters are usually composed of a number of common components such as capacitors, inductors, resistors etc. Several types of power splitters are found in different circuits such as transformer type Wilkinson splitter, lumped element quadrature Wilkinson power splitter, hybrid splitter, phase splitter, mixed lumped distributed element power splitter, etc. In practice, power splitters are designed to operate in some standard frequency bands such as low frequency (120 ÷ 135 kHz), high frequency (10 ÷ 15 MHz), ultra high frequency (UHF) (850 ÷ 950 MHz) and microwave frequency (2,45 GHz) [1]. At present, power splitters are being used in a wide range of applications including antenna designs, wireless communications, digital communications, optical communications, CATV transmission systems, airborne systems, transfusion medicine, etc. [2 ÷ 4].

A Radio Frequency Identification (RFID) is a recognition system, which remotely stores and recovers data from any objects. To store and recover the data, it uses a tag or transponder. It is an object applied to or attached into a product, animal, or even a person for identification and tracking. The two key parts of a RFID system consist of two fundamental components – a transponder (i.e. the tag itself) and a transceiver (i.e. the reader). An RFID tag is an integrated circuit with an antenna and acts as a storage medium. A reader reads tag data by using wireless communication. A RFID tag can be passive (draw power from the reader), active (battery powered) or semi- passive (requires battery, but the tag lies inactive until a signal is received from the reader).

Today RFID is used in various areas of public and private sectors. It is used in hospitals and the pharmacy. In addition, some organizations use RFID to track mail and security, to manage hazardous materials, to collect toll, to make people aware about tsunami, bird-flu, etc. Moreover RFID has been used in warehouse management, supply chain management, reverse logistics, shipment tracking and asset tracking, etc.

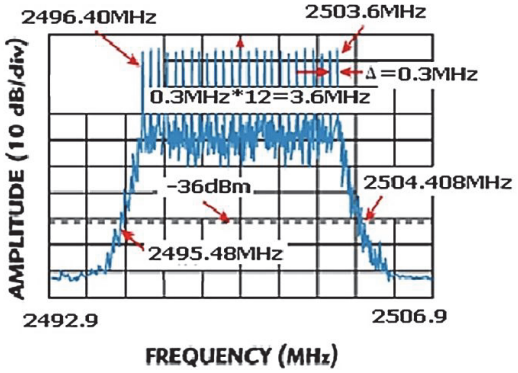

Figure 1 The transmit 25 channel spectrum of an RFID reader centered at 2,5 GHz ISM band

RFID readers being an essential component of RFID system got the attraction of the scientists due to the explosive RFID market throughout the world. The explosive RFID market has resulted in inauguration of numerous devices fulfilling the needs of the industry associated with RFID [5, 6]. The automatic identification technology of RFID is achieved with the reader reading or writing information on tags wirelessly. Due to the large

market of RFID in industry, the International Telecommunication Union (ITU) has prescribed a standard, known as the Industrial, Scientific and Medical radio band to serve these high-demand industries [5, 7].

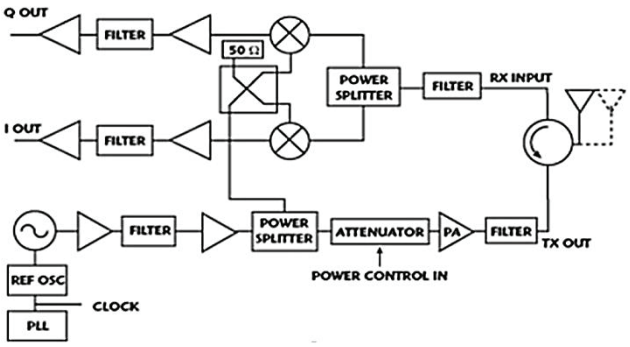

Figure 2 RFID Reader Circuit architecture block diagram

As the demand for ISM reader circuits is fairly high, this paper presents the preliminary design of a power splitter for a 2,45 GHz reader chip. A typical transmit spectrum of a 25 channel, 300 kHz spaced reader centered at 2,45 GHz is shown in Fig. 1. To achieve this, a simple RFID reader architecture based on the design presented by [8] is proposed for this project and shown in Fig. 2. Design simplicity is achieved by using the homodyne receiver architecture, eliminating the need for image rejection filters. Transmitting blocks operate at 2,45 GHz to further reduce the output signal filtering requirement. Power splitters were utilized to split the 2,4 GHz signal and feed it into the mixers [9].

2 Power splitter design

To integrate oscillators, surface acoustic wave resonators and filters on CMOS chips has been shown in [10]. The next component which is heavily utilized in the reader circuit architecture is the power splitter. Illustrating its importance, this paper focuses on the design of the power splitter circuit. Various power splitters have been designed to date. One such example is the Wilkinson power splitter employing 1/4 λ micro-strip lines, which shows a good performance in the high frequency band [11]. The major drawback of this design is its large size, originating from the use of a 1/4 λ micro-strip. The usage of on-chip inductors in 0,18 µm RF-CMOS instead of microstrips for our proposed design allows us to shrink the inductor layout to occupy 200 µm × 200 µm. Our proposed power splitter circuit is shown in Fig. 3, comprising of four inductors and three capacitors. Simulations regarding design specifications were conducted using AWR Microwave Office©.

Power splitter does not load the RFID reader circuit. The proposed power splitter is designed to achieve minimum insertion loss. This is illustrated in Fig. 4, which indicates that $|S_{21}|$ dB = –3,065 dB and $|S_{31}|$ dB = –11,87 dB, respectively at the frequency of interest. This indicates that a maximum insertion loss of 10 dB will be caused by the power splitter. Phase shifts caused by the circuit can be analyzed by simulating the $\angle s_{21}$ and $\angle s_{31}$ respectively. The simulation results are shown in Fig. 5, where $\angle s_{21} = -85{,}51^\circ$ and $\angle s_{31} = -132^\circ$.

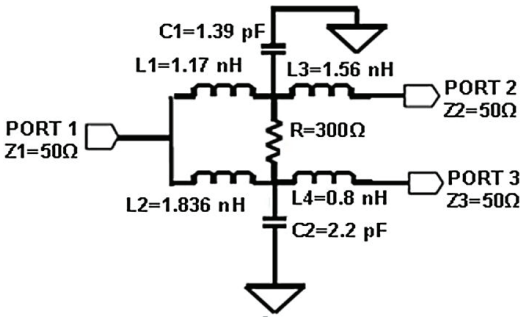

Figure 3 Power splitter circuit

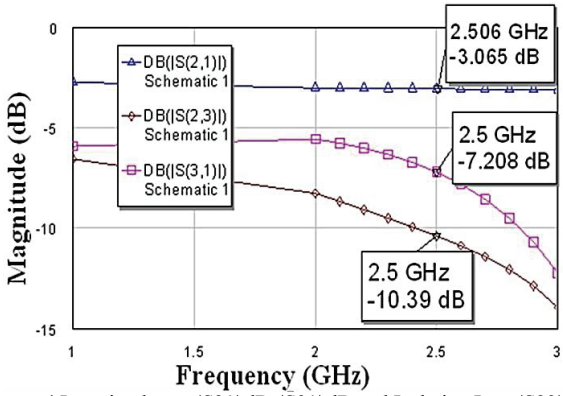

Figure 4 Insertion losses |S21| dB, |S31| dB and Isolation Loss |S23| dB of the power splitter circuit

The normalized matching characteristics of the power splitter circuit are shown in Fig. 6, indicating that matching circuitry will have to be designed for all three ports for optimum performance.

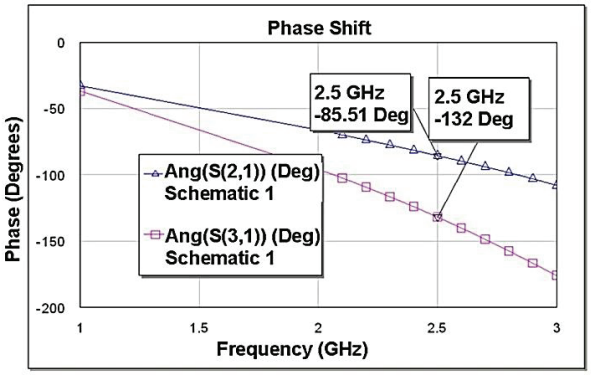

Figure 5 S_{21} and S_{31} Phase transmission characteristics

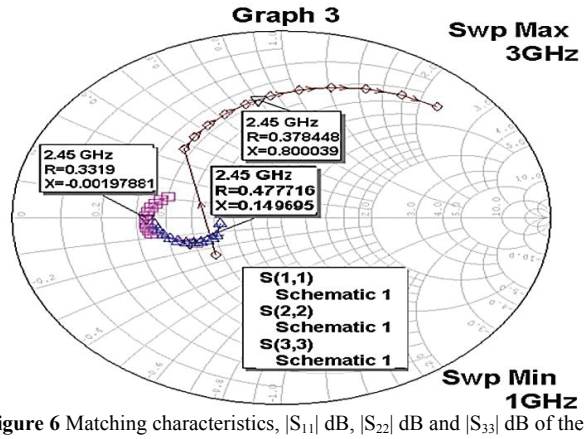

Figure 6 Matching characteristics, $|S_{11}|$ dB, $|S_{22}|$ dB and $|S_{33}|$ dB of the power splitter circuit

3 Inductor, capacitor and resistor layout design

CMOS technology has been widely adopted in the low cost radio frequency (RF) applications for its mature and mass productivity [12]. Additionally, its high fT transistor's characteristics are comparable with the GaAs ICs in the low gigahertz frequency ranges. It is our intention to fabricate the entire circuit as shown in Fig. 3 using CMOS technology. The CMOS fabrication reduces the parasites due to bond wires and interconnects which is substantial in the GHz range. This paper illustrates the implementation of spiral inductors using RF-CMOS 0,18 µm technology. The layout of the spiral inductor and its key parameters are shown in Fig. 7 and the cross-section of its CMOS layers is shown in Fig. 8 respectively. The top most metal (Metal 6) in this RF-CMOS process technology was used as the inductor while the port connections were made using both Metal 5 and Metal 6.

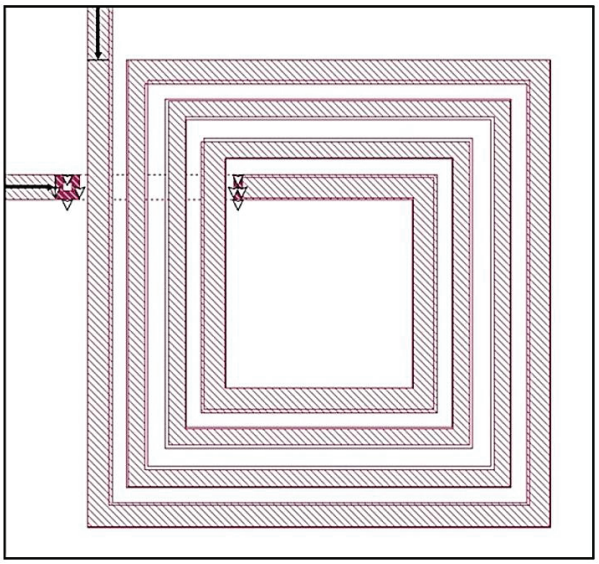

Figure 7 Layout of spiral inductor and key dimensions

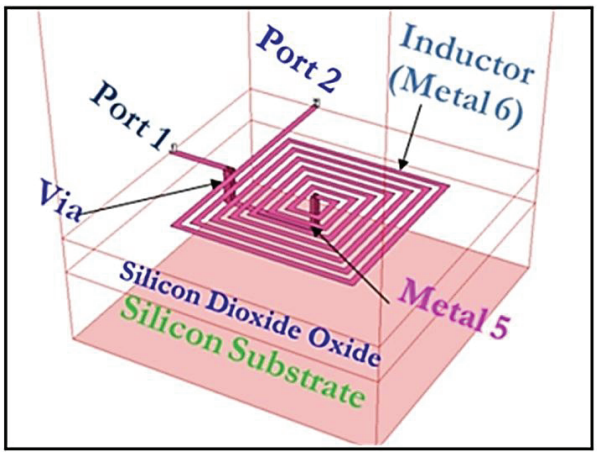

Figure 8 Cross-section of RF-CMOS inductor model in SONNET®

The inductance of planar spiral inductors can be calculated based on the modified Wheeler formula as shown in (1) below:

$$L_{\mathrm{mw}} = K_1 \mu \frac{n^2 d_{\mathrm{avg}}}{1 + K_2 r}, \tag{1}$$

where L_{mw} is the inductance value calculated using modified Wheeler formula, K_1 = 2,34 and K_2 = 2,75 are constants for square spiral inductors, n is the number of turns, μ is the permeability of the conductor and d_{avg} is the average diameter of the inductor defined in (2) [13, 14].

$$d_{\mathrm{avg}} = \frac{d_{\mathrm{out}} + d_{\mathrm{in}}}{2}. \tag{2}$$

The term r, or the fill factor is defined in (3). The relationship between d_{out} and d_{in} is shown in (4).

$$r = \frac{d_{\mathrm{out}} - d_{\mathrm{in}}}{d_{\mathrm{out}} + d_{\mathrm{in}}}, \tag{3}$$

$$d_{\mathrm{out}} = d_{\mathrm{in}} + 2nw + 2(n-1)s. \tag{4}$$

The inductor simulation model in Sonnet® was built based on the theoretically calculated inductor dimensions using (1 ÷ 4). SONNET is a planar electromagnetic solver, providing approximations for the electromagnetic analysis. Inductors can be generated quickly and easily by specifying the thicknesses of the surrounding layers and the outer diameter, d_{out}. The thicknesses of the inductor layers were as specified in Tab. 1.

Table 1 Inductor layer specifications in SONNET®

Layer	Thickness (µm)	$\varepsilon_{\mathrm{rel}}$
Silicon (loss free)	200	11,9
Silicon dioxide	0,7	3,9
Air	205	1,0

For a more accurate analysis, finite element analysis (FEA) of the electromagnetic field surrounding the inductor was simulated using CST Microwave Studio™. The FEA model requires more in-depth specifications of the inductor layout. It allows the user to draw the exact layout of the inductor, complete with the via layers, providing a more accurate model of the inductor fabricated in RF-CMOS technology. Tab. 2 provides the parameters of the inductor drawn using CST Microwave Studio™. The FEA simulations generate not only the inductance values versus frequency as shown in Fig. 9, but also the quality factor of the inductor which is shown in Fig. 10. Fig. 9 indicates that L1 has inductance value of 1,13 nH at the frequency of interest of 2,5 GHz. The quality factor at 2,5 GHz is $2{,}644 \times 10^{13}$ as shown in Fig. 10.

Table 2 Inductor layer specifications in CST Microwave Studio ™

Layer	Thickness (µm)	Material
Substrate	200	Silicon
Silicon dioxide	2,56	Oxide
Metal 5	0,53	Perfect Electric Conductor (PEC)
Via	0,3	Perfect Electric Conductor (PEC)
Inductor	2,39	Perfect Electric Conductor (PEC)

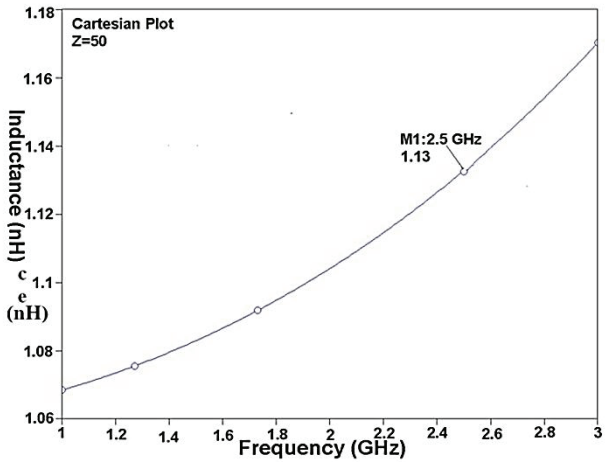

Figure 9 Inductance versus frequency simulation results for L1 using CST Microwave Studio™

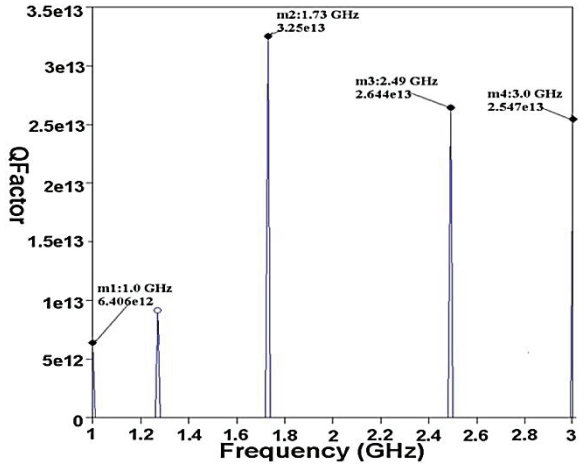

Figure 10 Quality factor versus frequency simulation results for L1 using CST Microwave Studio™

Tab. 3 summarizes the dimensions of the four inductors and compares the simulation results of i) Sonnet® and ii) CST Microwave StudioTM simulation of the inductors' layout. It can be seen from Tab. 3 that the dimensions specified by Sonnet® produced very similar inductance values when simulated using the CST electromagnetic simulator.

The capacitors (C1, C2 and C3) were designed using standard RF-CMOS layers, Metal 1 and Metal 2. The typical layout of the metal-metal capacitor is shown in Fig. 11. An N-well resistor was used to implement the 300 Ohms resistor. The dimensions of the n-well resistor were 180 nm × 450 nm. The design parameters for all 3 capacitors are summarized in Tab. 4.

Table 3 Inductor dimensions and simulation results

Item	Width (µm)	Spacing (µm)	Outer diameter, d_o / µm	L Sonnet® (nH)	FEM Simulation L / nH
L1	8,6	8,1	275	1,170	1,130
L2	8,6	8,1	350	1,836	1,862
L3	8,6	8,1	335	1,545	1,561
L4	8,6	8,4	250	0,800	0,877

Table 4 Capacitor parameters

Item	Width (µm)	Length (µm)	Capacitance (pF)
C1	13,04	14,8	1,39
C2	21,16	22,6	2,2

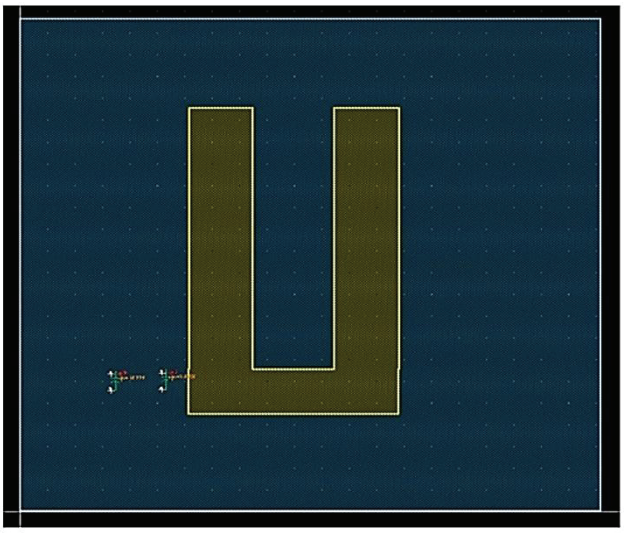

Figure 11 Capacitance layout for C3. Extracted capacitances indicate that there are two capacitors in parallel, 12,77 pF and 2,068 pF, yielding the desired value of 2,2 pF

4 Conclusion

This paper illustrates the design and simulation results for a power splitter circuit for ISM RFID reader circuits. The circuit utilized four inductors, three capacitors and a resistor. The functionality of the power splitter circuit was verified and integrated on an RF-CMOS chip. The design overcomes the major drawback of Wilkinson design' large size and reduced to inductor layout to occupy 200 µm × 200 µm. The proposed power splitter achieves a maximum insertion loss of 10 dB.

5 References

[1] Jalalifar, M.; Uddin, M. J. Power Splitter Architectures and Applications. // Progress In Electromagnetics Research C. 18, (2011), pp. 231-244.

[2] Zhu, S. ; Lo, G. Q. ; Kwong, D. L. Nanoplasmonic Power Splitters Based on The Horizontal Nanoplasmonic Slot Waveguide. // Applied Physics Letters. 99, 3(2011), pp. 031112 - 031112-3.

[3] Shuenn-Yuh Lee ; Chun-Cheng Lai. A 1-V Wideband Low-Power CMOS Active Differential Power Splitter for Wireless Communication. // IEEE Transactions On Microwave Theory And Techniques. 55, 8(2007), pp. 1593-1600.

[4] Clive Hohberger; Rodeina Davis; Lynne Briggs; Alfonso Gutierrez; Dhamaraj Veeramani. Applying Radio-Frequency Identification (RFID) Technology In Transfusion Medicine. // Biologicals. 40, 3(2012), pp. 209-213.

[5] Mohd-Yasin, F.; Khaw, M. K.; Reaz, M. B. I. Radio Frequency Identification: Evolution of Reader and Antenna Circuit Design. // Microwave Journal. 49, (2007), p. 5.

[6] Xiaowei Zhu ; Samar K. Mukhopadhyay; Hisashi Kurata. A Review Of RFID Technology And Its Managerial Applications in Different Industries. // Journal of Engineering and Technology Management. 29, 1(2012), pp. 152-167.

[7] Changzhan Gu; Zhiguang Fan; Shaoyuan Zheng; Jiangtao Huangfu; Lixin Ran. A System Design for the Reader of Microwave Radio Frequency Identification. // PIERS Online, 3, 7(2007), pp. 960-963.

[8] Michael M. Elsbury; Paul D. Dresselhaus; Norman F. Bergren; Charles J. Burroughs; Samuel P. Benz; Zoya Popović. Broadband Lumped-Element Integrated N-Way Power Dividers for Voltage Standards. // IEEE Transactions On Microwave Theory And Techniques. 57, 8(2009), pp. 2055-2063.
[9] Aminghasem Safarian; Lei Zhou; Payam Heydari. CMOS Distributed Active Power Combiners and Splitters for Multi-Antenna UWB Beamforming Transceivers. // IEEE Journal of Solid-State Circuits. 42, 7(2007), pp. 1481-1491.
[10] Nordin, A. N.; Zaghloul, M. E. Modeling and Fabrication of CMOS Surface Acoustic Wave Resonators. // IEEE Transactions on Microwave Theory and Techniques. 55, 5(2007), pp. 992-1001.
[11] Kim, D. I.; Jung, S. W.; Yun, Y. A high performance transformer-type Wilkinson power splitter with compensating circuit for CATV transmission system and optimal design method. // IEEE Transactions on Consumer Electronics. 50, 3(2004), pp. 934-940.
[12] Abidi, A. A. RF CMOS come of age. // IEEE Microwave Magazine. 4, 4(2003), pp. 47-60.
[13] Jenei, S.; Nauwelaers, B. K. J. C.; Decoutere, S. Physics-Based Closed-Form Inductance Expression for Compact Modeling of Integrated Spiral Inductors. // IEEE Solid-State Circuits. 37, 1(2002), pp. 77-80.
[14] Mohan, S. S.; Hershenson, M. D. M.; Boyd, S. P.; Lee, T. H. Simple Accurate Expressions for Planar Spiral Inductances. // IEEE Solid-State Circuits. 34, 10(1999), pp. 1419-1424.

Authors' addresses

M. Jasim Uddin, M.Sc.
International Islamic University Malaysia
Department of Electrical and Computer Engineering
53100 Kuala Lumpur, Malaysia

Anis N. Nordin, Ph.D.
International Islamic University Malaysia
Department of Electrical and Computer Engineering
53100 Kuala Lumpur, Malaysia

M. B. I. Reaz, Ph.D.
Universiti Kebangsaan Malaysia
Department of Electrical, Electronic and Systems Engineering
43600 Bangi, Selangor, Malaysia
Tel: +603-89216311
E-mail: mamun.reaz@gmail.com

Mohammad Arif Sobhan Bhuiyan, M.Sc.
Universiti Kebangsaan Malaysia
Department of Electrical, Electronic and Systems Engineering
43600 Bangi, Selangor, Malaysia
Tel: +603-89216311