Poly-Si passivating contacts formed via spin-on doping for c-Si solar cells

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Declaration

I certify that this thesis does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any published or written form by another person, except where due reference is made in the text. The work in this thesis is conducted by myself, except for the contributions made by others as described in the Acknowledgements.

Zetao Ding

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Abstract

With the constant improvement of crystalline silicon solar cells over the last decades, the carrier recombination and transportation at the contacts have become limiting factors to efficiency improvement for crystalline silicon solar cells. A potential solution is to use passivating contact, which suppresses carrier recombination while simultaneously ensures efficient majority carrier transportation. The polycrystalline silicon (poly-Si) passivating contact has shown a low carrier recombination current density, a low contact resistivity and a high thermal stability which can be easily integrated with the current high efficiency industrial silicon solar cell production lines. A wide range of doping methods have been employed to fabricate poly-Si passivating contacts, but only a small amount of work has been presented on spin-on doping process.

The spin-on doping technique involves less dangerous dopant precursors than other doping techniques like dopant gas diffusion and a simpler process tool than *e.g.* ion implantation, and it may promote the doping process versatility based on its features of diverse dopant elements, wide dopant concentration range, and the ability of single-side doping. However, more comprehensive and detailed investigations are required for the poly-Si passivating contacts fabrication by using spin-on doping. Thus, in this thesis we focus on the application of spin-on doping process on industrially processed poly-Si passivating contacts. We performed detailed investigations on phosphorus and boron spin-on dopants.

For both phosphorus and boron spin-on doping, the various spin speed and acceleration during spin coating process show slight impacts on passivation quality. Besides, a longer baking time leads to better passivation and lower sheet resistance. In addition, the drive-in process yields large impacts on passivation and electrical properties. Implied open-circuit voltages of ~730 or 705 mV are obtained after 975 or 950 °C drive-in process and a forming gas annealing (FGA), for phosphorus or boron case respectively. A low contact resistivity below 5 $m\Omega \cdot cm^2$ for both, phosphorus or boron, spin-on doping cases were achieved. These results are to our knowledge the highest iV_{OC} values achieved by spin-on doping to date and are close to the performance of gas diffused or ion implanted poly-Si contacts. This shows the potential of spin-on doping process as alternative to traditional gas diffusion or ion implantation doping methods.

Keywords: spin-on doping, liquid dopant, polycrystalline silicon, polySi, poly-Si, passivating contact, solar cell, TOPCon, POLO.

Content

I. Introduction

This chapter presents a short review on crystalline silicon (c-Si) solar cells, including the status of high efficiency silicon solar cells, their operation fundamentals, and approaches to improve their conversion efficiencies. At the end, the motivation and outline for this thesis are presented.

1.1 Advantages and recent developments of c-Si photovoltaic techniques

Solar energy is a clean and abundant energy source, which can sufficiently provide the global energy consumption [1]. Photovoltaic (PV) devices, or solar cells, are able to convert solar energy directly into electrical power. The dominant PV technology is c-Si solar cells, which has a worldwide market share of 90 – 95% [2]. Silicon has an indirect energy bandgap of ~1.12 eV [3], which is within the theoretical optimal bandgap (1.1 – 1.4 eV) for solar radiation absorption [4]. Besides, silicon is inert and shows much lower toxic level than Arsenide compound-based semiconductor, reducing the danger during material and device fabrication considerably. Furthermore, the abundance of silicon in the Earth and well-established technologies endow silicon solar cells with high performance and low costs.

The theoretical upper limit of silicon solar cell efficiency was calculated to be 29.4% [5]. A meaningful milestone on the way of approaching this limit is 25%, which was reported firstly by UNSW in 1999 based on passivated emitter and rear contact (PERC) structure (PERL 25%, PERT 24.5%) [6, 7]. Till 2020, the improvements of processes and cell structures have witnessed the increase in c-Si solar cell efficiency to above 26%. In 2017, a tunnel oxide passivated contact (TOPCon) cell of 25.7% efficiency was reported by Richter *et al.* from Fraunhofer Institute for Solar Energy Systems (Fraunhofer ISE) [8]. In the following year, this record was surpassed by a polycrystalline silicon on oxide-interdigitated back contact (POLO-IBC) cell with efficiency of 26.1% fabricated by Haase *et al.* from Institute for Solar Energy Research Hamelin (ISFH) [9]. The highest efficiency for silicon solar cell to date is 26.7% from a cell with heterojunction-interdigitated back contact (HJ-IBC) structure, reported by Yoshikawa *et al.* from KANEKA Corporation in 2017 [10].

1.2 Operation principles of c-Si solar cells

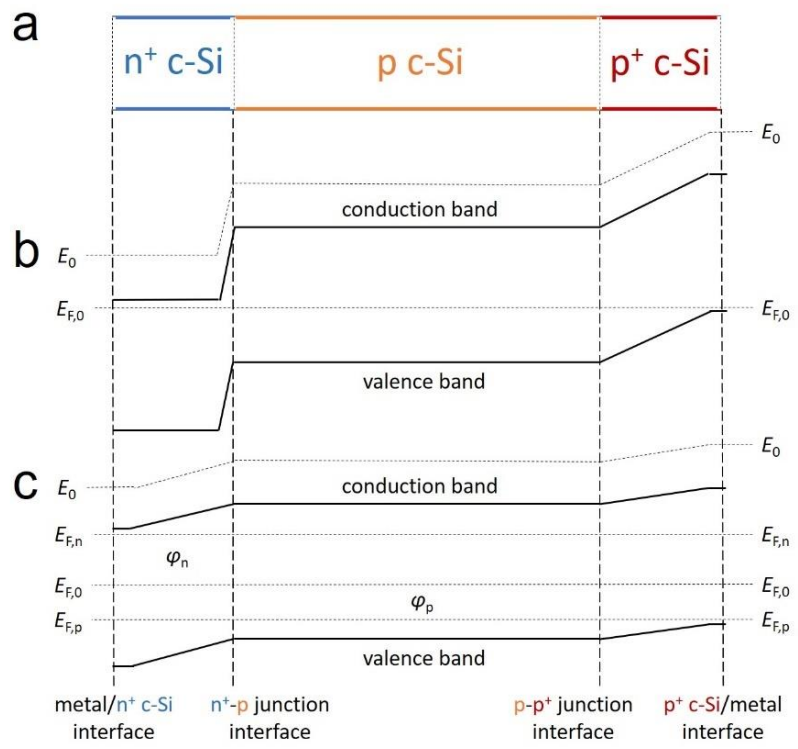


Figure 1.1 (a) Simple schematic of a n^+-p-p^+ silicon solar cell structure; its band diagram in (b) dark and equilibrium condition and in (c) illuminated and quasi-steady state [3, 11].

Figure 1.1 displays a sketch of the structure of the main part of a n^+-p-p^+ silicon solar cell and its band diagrams under dark equilibrium condition or illumination state. In dark thermal equilibrium condition, the carriers will be excited by thermal energy and will recombine before being collected. As a result, the carrier recombination rate is equal to carrier generation rate ($R_{th} = G_{th}$). In illuminated condition and quasi-steady state (*e.g.*, open-circuit condition), apparent voltage and current output will be measured. The silicon will absorb incident photons, which have energy higher than silicon bandgap ($h\nu > E_g$), and produce free electrons and holes. Consequently, as shown in figure 1.1b, a large potential difference (φ_n) will be formed between electron quasi-Fermi energy level ($E_{F,n}$) and intrinsic Fermi energy level ($E_{F,0}$). And a potential difference (φ_p) will also appear between $E_{F,0}$ and hole quasi-Fermi energy level ($E_{F,p}$). The theorical voltage output is the sum of φ_n and φ_p, as shown in equation 1.1:

$$V_{out} = \left(\frac{E_{F,n} - E_{F,0}}{q}\right) + \left(\frac{E_{F,0} - E_{F,p}}{q}\right) = \varphi_n + \varphi_p = \frac{k_B T}{q} ln\left(\frac{(n_0+\Delta_n)(p_0+\Delta_p)}{n_i^2}\right) \quad (1.1)$$

where k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. In this equation, n_0 and p_0 is the intrinsic electron density and hole density respectively. Δ_n and Δ_p

is the photo-generated electron density and hole density respectively. n_i is the total intrinsic carrier density in silicon, which is 8.3×10^9 cm^{-3} at 25 °C [12]. It can be found that, higher densities of photo-generated electrons and holes will lead to higher voltage output (V_{out}). After connecting to the load, the excessive electrons will move from n-type Si into external circuit, through the external circuit and then move into p-type Si to neutralize excessive holes.

The cell performance can be characterized by the function of current density (J) on voltage (V), which can be described by the diode equation. Ignoring the recombination in depletion region, its dark J-V characteristics is described as:

$$J = J_0\left[exp\left(\frac{qV}{kT}\right) - 1\right] = \left(\frac{qD_e n_i^2}{L_e N_A} + \frac{qD_h n_i^2}{L_h N_D}\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1.2)$$

where J_0 is the saturated current density; D is the diffusion coefficient; L is the diffusion length; n_i is the intrinsic carrier density; N_A and N_D are the doping concentrations for p-type and n-type dopants respectively. This dark J-V curve is plotted in dashed line in figure 1.2 [13, 14]. It can be deduced that for a specific condition, the higher doping concentration of either p-type dopant (N_A) or n-type dopant (N_D) will lead to higher majority carrier density, thus lower saturated recombination current density (J_0). At illuminated condition, the photo-generated current density (J_L) can be expressed by equation 1.3:

$$J_L = qG(W + L_e + L_h) \quad (1.3)$$

where G is the bulk generation rate, W is the depletion width, and L is the diffusion length. Consequently, the J under illumination is equal to dark J minors J_L, as expressed by equation 1.4:

$$J = J_0\left[exp\left(\frac{qV}{kT}\right) - 1\right] - J_L \quad (1.4)$$

This illuminated J-V curve is also plotted as solid line in figure 1.2 [13, 14]. From the illuminated J-V curve, we can gain the essential parameters for a silicon solar cell, *e.g.*, open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF), efficiency (η), *etc*. Open-circuit voltage is the voltage value of a cell with interrupted outer circuit, *i.e.*, x-intercept of illuminated J-V curve. V_{OC} is the highest voltage for a cell. Short-circuit current density is the maximum current density of a cell when no load is on outer circuit, *i.e.*, y-intercept of the illuminated J-V curve. Fill factor is the ratio of product of current and voltage at the maximum power point over the product of open-circuit voltage multiplied by the short-circuit current density. The light to electricity conversion efficiency

is obtained from the maximum power point as the ratio of generated power and incoming power by illumination.

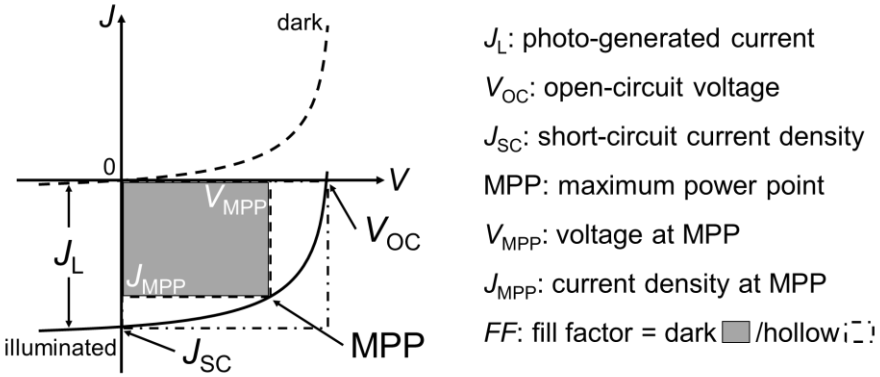


Figure 1.2 (left) Typical *J-V* curves of a silicon solar cell under dark and illuminated situations. (right) The meanings of related items [13, 14].

1.3 Efficiency-limiting factors and solutions

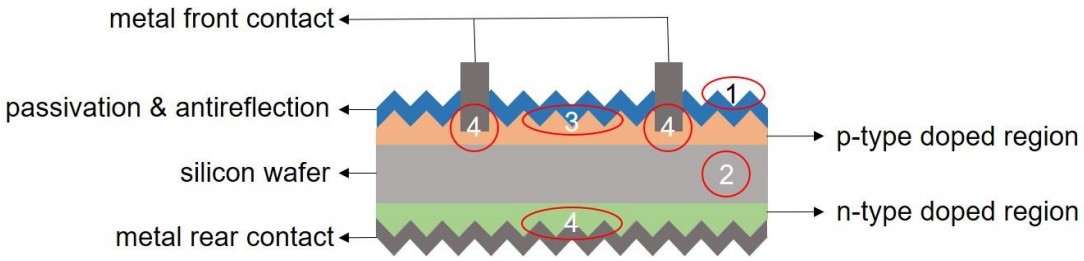


Figure 1.3 Sketch of the structure of a typical diffused silicon solar cell. Region 1 is front layer. Region 2 is wafer bulk. Region 3 is wafer/front layer interface. Region 4 is wafer/contact interface.

Figure 1.3 displays the basic structure of a conventional n-type silicon solar cell with front p-n junction. According to the working principles described above, the cell efficiency can be improved via mainly three directions: low carrier transportation resistance, high carrier generation, and low carrier recombination [15].

The low carrier transportation resistance is beneficial to improve current density output (J_{out}) and fill factor (*FF*). The low carrier transportation resistance in whole circuit requires low resistances in wafer bulk (region 2 in figure 1.3) and at silicon/contact interfaces (region 4 in figure 1.3). The wafer with higher doping level and less grain boundary defects shows lower bulk resistance [16]. Also, a thinner wafer or a special cell structure (such as double-side contact cell [17]) contributes to reduce carrier transportation length. At silicon/contact interface, a direct connection between diffused silicon region and metal contact offers low contact resistivity [18, 19].

To generate more carriers, more absorption of incident photons is required, which involves surface texturing, anti-reflection layer, and cell architecture, *etc*. For surface texturing, a widely used structure is the random upwards pyramids on surface, which can be achieved via a chemical anisotropic etching [20]. For anti-reflection coating (region 1), a single-layer (*e.g.* SiO_x [21]) or double-layer (*e.g.* MgF/ZnS [19]) coating can effectively reduce light reflection, but the latter one needs a separate passivation layer. The PECVD silicon nitride (SiN_x) [22] film combines the effects of anti-reflection and surface passivation, which is widely employed in current PV manufacturing. In terms of cell architectures, thin metal contacts on front side are designed to reduce the shadow of incident light. The gridded front contact fingers [23] explore more front surface area under incident light, but a larger separation between fingers increases the current pathway in the wafer and thus the series resistance. This negative effect can be relieved by a deeper diffusion on the wafer surface increasing the lateral conductivity. Closely-spaced front contacts are able to reduce current pathway and series resistance, but will result in more shadowing at the same time [24]. To avoid contact shadowing completely and reduce internal series resistance at the same time, the interdigitated back contacts (IBC) configuration was introduced [25], which resulted in 15% efficiency for light intensity of 5 – 28 W/cm^2. In recent 10 years, the cells using the IBC structure have offered an efficiency over 25% [26], holding currently the world record of cell efficiency (~26.7% [10]).

Before discussing approaches to suppress carrier recombination, some basic recombination mechanisms need to be mentioned. Carrier recombination happens in silicon bulk (region 2 in figure 1.3), at wafer surface (region 3), and at wafer/contact interface (region 4). In wafer bulk (region 2), carrier recombination can be divided into mainly three processes: radiative recombination, Auger recombination, and Shockley-Read-Hall (SRH) recombination [13, 27-29]. These recombination processes are sketched in figure 1.4.

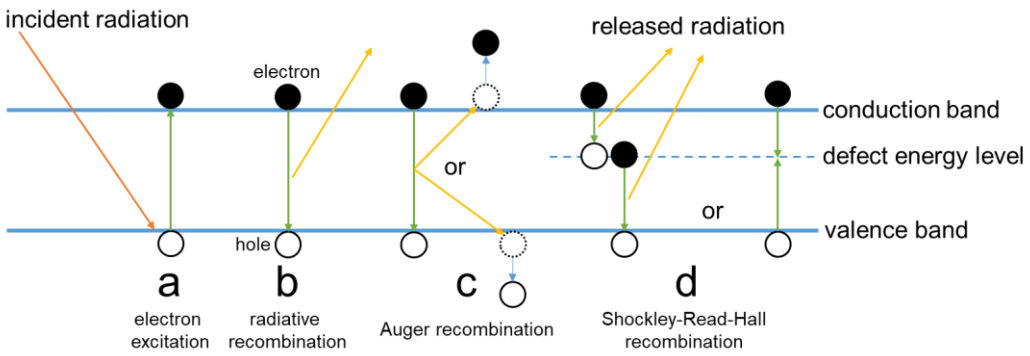


Figure 1.4 Sketches of carrier behaviours in silicon wafer bulk: (a) electron excitation, (b) radiative recombination, (c) Auger recombination, and (d) SRH recombination [30, 31].

In radiative recombination (process b), excited electrons fall into valence band, combine with holes, and emit radiation. This recombination is unavoidable, but it is relatively small in silicon as silicon has an indirect bandgap [3]. In semiconductor with indirect bandgap, radiative recombination requires additional phonons. In Auger recombination (process c) [3, 13, 31-33], three particles are involved. Similar to radiative recombination, the excited electron falls back to valence band and recombines with a hole, emitting some energy. However, this energy will be transferred to another electron ("eeh" process) near conduction band edge or hole ("ehh" process) near valence band edge, exciting it into a higher (or lower) energy level. The Auger recombination rate (R_{Auger}) is positively related to carrier densities, as expressed in equation 1.5 below [33]:

$$R_{Auger} = C_n n^2 p + C_p p^2 n \tag{1.5}$$

where C_n and C_p are the Auger coefficients in n- and p-type silicon respectively, and n and p are the respective densities of electrons and holes. In heavily doped n- or p-type silicon, an electron or hole can be easily excited, leading to high electron or hole density near band edge and thus increasing Auger recombination rate. Thus, it is important to control doping level in the doped silicon regions. In SRH recombination (process d), the defect energy levels offer intermediate states within bandgap, making electrons falling to valence band easier [30]. These defect energy levels within the band gap can capture free carriers, leading to carrier recombination process [13, 31]. The defect energy levels are crucial for SRH recombination, so reducing defects within wafer bulk is indispensable to suppress SRH recombination.

The silicon surface (region 3 in figure 1.3) has a high density of recombination centres due to broken dangling bonds. These dangling bonds can be passivated by using oxide (SiO_x) layers. For example, the cell structures named as "passivated emitter solar cell" (PESC) and "metal-insulator-NP junction"

(MINP) employ high quality thermal oxide passivating layer on front side, resulted in efficiencies over 18% in 1984 [19, 34]. The thermal oxide passivating layers were formed on both sides, acting as a part of the structure named "passivated emitter and rear cell" (PERC) [35]. Together with direct metal-wafer contact, this cell structure improved efficiency to 22.8% [35]. Afterwards, based on oxide layer-passivated both sides, textured front surface, and locally diffused rear emitters, the cell efficiency increased to ~25% [7, 36]. Apart from silicon oxide layers, silicon nitride (SiN_x) and aluminium oxide (AlO_x) layers are also explored as an effective surface passivation layer in silicon solar cells [37]. For SiN_x formed via plasma-enhanced chemical vapor deposition (PECVD), the passivation effects depend on Si:N ratio. Si-rich state shows more chemical passivation, while N-rich state has strong positive fixed charges and shows more field effect passivation [38, 39]. This feature makes N-rich SiN_x especially suitable to passivate n-type surfaces [40]. On the contrary, thin AlO_x film has strong negative fixed charges, meaning that aluminium oxide may be more suitable to passivate p-type surfaces [41]. For example, a cell with boron-doped Si regions passivated by AlO_x exhibited a V_{OC} of ~700 mV [42]. Compared to passivation layers above, the intrinsic hydrogenated amorphous silicon (a-Si:H) layer shows strong passivation effect via low temperature deposition process. For example, for deposition temperature 200 – 275 °C, the measured surface carrier recombination velocity (S_{eff}) of a-Si:H passivated surface was lower than 10 cm/s [43]. The silicon solar cells with the world record efficiency of 26.7% use a-Si:H as the passivation layer [10]. Furthermore, the stacks of these passivation materials have shown comparable or stronger passivation than their single layers [44-46].

The recombination at wafer/contact interface (region 4 in figure 1.3) also takes a major part of total carrier recombination. It has become a limiting factor for silicon solar cells to achieve high conversion efficiencies [47]. The direct contacting of metal with the silicon wafer will introduce a high density of electronically active states at the silicon/metal interface. These interface states lie within the silicon bandgap, which will result in high recombination [48]. The sketches of band diagram of metal/n- and p-type Si contacts are shown in Figure 1.5. It is of great significance to diminish the interface states at and near wafer/metal contact interface. The approaches of reducing silicon/metal contact interface recombination, as discussed above, are the motivations in this work.

Similar to the case of wafer surface passivation, reducing carrier concentrations near wafer/contact

interface also helps to suppress recombination [49]. However, for wafer/contact interface, while minority carriers should be kept away from interface, the majority carriers should move to and across wafer/contact interface, which can be both achieved by passivating contacts. The passivation processes towards silicon/contact interface should reduce carrier recombination but avoid impedance on majority carrier transportation.

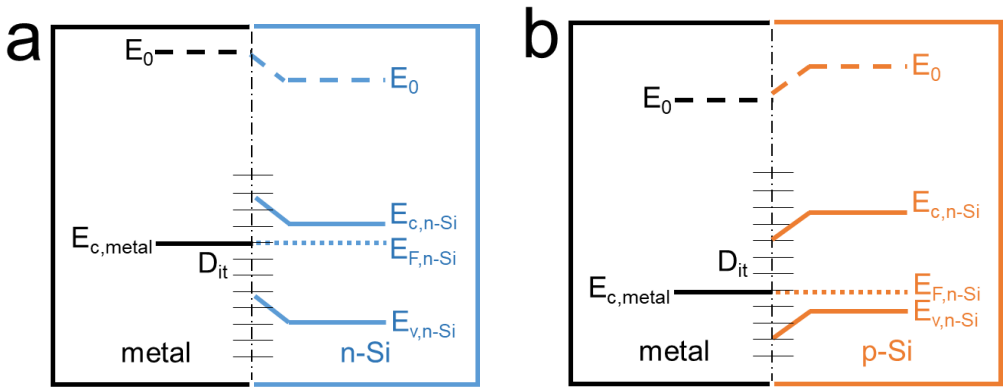


Figure 1.5 Schematic idealized equilibrium band diagrams for (a) metal/n-Si contact and (b) metal/p-Si contact [48, 50]. E_0 is the vacuum energy level; $E_{c,metal}$ is the energy level of conduction band of metal; $E_{c,n\text{-}Si}$ and $E_{v,n\text{-}Si}$ are the energy levels of conduction and valence band of n-type silicon respectively; $E_{F,n\text{-}Si}$ is the energy level of Fermi energy in n-type Si, which is aligned with $E_{c,metal}$; $E_{c,p\text{-}Si}$ and $E_{v,p\text{-}Si}$ are the energy levels of conduction and valence band in p-type silicon respectively; $E_{F,p\text{-}Si}$ is the energy level of Fermi energy in p-type Si, which is also aligned with $E_{c,metal}$; D_{it} is the interface defect density at the metal/silicon interface. Aluminium is chosen as the metal here.

1.4 Features and main types of passivating contacts

The passivating contacts use ultrathin dielectric or conductive layers to passivate Si surface, and achieve carrier selectivity via asymmetries in work functions, tunnelling, or carrier mobilities at the c-Si/contact interface, and energy-selective defect bands [51-53]. A good passivating contact should have low carrier recombination and a good carrier conductivity simultaneously [47].

To realize the performance described above, mainly four types of passivating contacts have been presented: dopant-free passivating contacts, dielectric interlayer structure, silicon heterojunction structure, and doped silicon/dielectric layer stack structure. Because the topic of this thesis is poly-Si passivating contact, the explanations here focus mainly on the latter three kinds of passivating contacts.

1.4.1 Dielectric interlayer structure:

A tunnel barrier (such as an ultrathin dielectric or insulator layer) between c-Si and metal contributes to interfacial passivation. The ultrathin interfacial layer will passivate the interface defects between silicon and metal, and minimize the fermi level pinning effect [54]. Meanwhile, together with metal with different work functions, the dielectric layers with asymmetrical tunnelling probabilities for electrons and holes also show selectivity on carriers.

The idea of involving insulator interlayer originated from the early metal-insulator-semiconductor (MIS) structure [55-57]. In 1975, S. J. Fonash confirmed that an interlayer in metal-semiconductor junction was necessary [55]. In 1978 Pulfrey reviewed some theories for MIS contacts and discussed the possible reasons in detail [56]. Based on this detailed discussion, Godfrey and Green obtained a 20 mV increase in V_{OC} by optimizing SiO_x interlayer, leading to an efficiency of 17.6% [57]. However, the insulator interlayer produced a higher contact resistivity than metal-silicon direct contact. To solve this problem, A.W. Blakers introduced an n-type doped layer below SiO_x layer, which decreased contact resistivity and further reduced the carrier recombination at SiO_x/n-type Si interface. Consequently, this metal-insulator-n-p junction (MINP) cell demonstrated a V_{OC} of 678 mV [58] and an efficiency above 18% [19].

1.4.2 Silicon heterojunction:

The silicon heterojunction (SHJ) passivating contact features a stack of doped amorphous silicon over intrinsic hydrogenated amorphous silicon (a-Si:H) [59]. The intrinsic a-Si:H interlayer passivates wafer surface effectively and the doped a-Si layer ensures the carrier conductivity and carrier selectivity [60]. The silicon heterojunctions take advantages of low process temperature and simple cell structure with excellent surface passivation of a-Si:H layers [59]. But there are still some disadvantages, mainly including notably low J_{SC} [61], and poor thermal stability at high temperature [62, 63].

The observed reasonable carrier mobilities [64] and surface passivation effect [65] of a-Si:H, together with substitutional doping methods (addition dopant precursors during a-Si deposition) towards a-Si:H enabled the application of SHJ into silicon solar cells [66]. Along with the development, the SHJ-based silicon cells witness the efficiency increase to 21% on 10 cm×10 cm

wafers by the mid-2000s [67], 24.7% from double-side contacted SHJ cell in 2014 [68], and 26.7% from HJ-IBC cell in 2017 [10], which is the highest efficiency record so far for silicon solar cells.

1.4.3 Doped silicon/dielectric interlayer stack:

From the discussion above, we can find that in MIS scheme a thin insulator layer leads to higher V_{OC} but also higher contact resistance; in SHJ scheme the a-Si:H stack passivates wafer surface and shows lower contact resistance than dielectric interlayer, but it is thermally unstable. As an alternative for the two contact structures above, a stack of doped polycrystalline silicon (poly-Si) film over ultrathin dielectric layer is able to combine the advantages of both MIS and SHJ technologies. This kind of poly-Si based contact structures were invented in 1980s [69-72], named as semi-insulating polycrystalline silicon (SIPOS) and showing low contact recombination current density (J_{0C}, 20 – 50 fA/cm^2) as well as low contact resistivity (ρ_C, ~0.01 mΩ·cm^2) for silicon solar cells. Around 2014, this kind of structure received a revival achieved by Feldmann *et al.* [73], Römer *et al.* [74], and Yan *et al.* [75], *etc*. The ultrathin SiO_x layer, which is the key component, passivates the c-Si/SiO_x interface by reducing the surface defect state density, but still allowing carriers to transfer from wafer to doped poly-Si layer. At the same time, the highly doped poly-Si layer will show high selectivity and conductivity towards the excessive carriers and form ohmic contact with metal electrodes. Detailed discussion of operation principles of poly-Si passivating contacts can be found in section 2.1. The poly-Si passivating contacts have the potential to surpass SHJ contacts by achieving similar low carrier recombination, lower contact resistivity, and higher thermal stability [3].

The passivating contacts with doped poly-Si/SiO_x structure are sometimes described by acronyms like “TOPCon” (tunnel oxide passivated contact) by Fraunhofer ISE [8, 76], “POLO” (poly-Si on oxide) by ISFH [77], “monoPoly^{TM}” (monofacial poly-Si contact) by Solar Energy Research Institute of Singapore [78], “PERPoly” (passivated emitter rear poly-Si) by Energy Research Centre of the Netherlands [79], “PeRFeCT” (Passivated Emitter and Front ConTacts) by Delft University of Technology [80], *etc*.

Recently, the poly-Si based passivating contact structure has successfully enabled solar cell conversion efficiency exceeding 25% [8, 81], even approaching 26% [82]. ISFH has demonstrated IBC solar cells with an efficiency of 26.1% by integrating both n- and p-type poly-Si passivating

contacts into IBC solar cell structure [9]. For cells with poly-Si passivating contacts on both sides, Peibst *et al.* prepared poly-Si passivating contacts on industrial large area wafer with textured front side and planar rear side, which led to cell efficiency of ~22.3% [83].

1.5 Thesis motivation and outline

Compared to other passivating contacts as discussed above, poly-Si passivating contacts have much lower carrier recombination density values, lower contact resistivity and a higher thermal stability. One of the key elements to form such high-performing poly-Si contacts is the implementation and control of the doping. One promising *ex-situ* doping approach is the spin-on doping process, which involves less damage, less dangerous dopant precursors and simpler process tools compared to other doping methods, such as *in-situ* doped silicon deposition, dopant gas diffusion, and ion implantation, *etc*. These processes involve toxic and dangerous dopant materials, and complicated facilities. The advantages and disadvantages of these doping methods will be discussed more in Chapter 2. In addition, spin-on doping is able to use diverse dopant species with a wide range of dopant concentrations [84], and offers single side doping [85]. However, only a few works have been done on the application of spin-on doping for poly-Si [84, 86-89], and more investigations are required to make spin-on doping method more reliable for poly-Si passivating contacts.

In this thesis, phosphorus and boron spin-on dopants are used to fabricate n-type and p-type poly-Si passivating contacts, respectively. The influences of phosphorus and boron spin-on doping processes on poly-Si passivating contact formation and performance are explored and analysed. The process parameters include spin coating speed, spin coating time, spin acceleration, doses of dopant-containing solutions, hard baking time, drive-in temperature, drive-in time, as well as as-deposited amorphous silicon thickness. The prepared poly-Si passivating contacts are characterized by implied open-circuit voltage (iV_{OC}), carrier recombination current density (J_0), doping profile, and contact resistivity (ρ_C), *etc*.

In chapter 1, the advantages, basic operation principles and approaches to improve efficiency of a crystalline silicon solar cell are discussed.

In chapter 2, some properties and phenomena of poly-Si passivating contacts are discussed. Then some mainstream doping approaches for poly-Si contacts are summarized.

Chapter 3 presents detailed discussions on the spin-on doping method. Firstly, the features of spin-on doping and material sources are discussed. Next, the applications of spin-on doping for silicon solar cells and poly-Si passivating contacts are presented.

Chapter 4 provides an overview of the fabrication processes and measurement methods implemented in this thesis.

Chapter 5 demonstrates the results and analysis on the impact of P spin-on doping processes on poly-Si contact performance based on industrial planar a-Si/SiO_x/c-Si/SiO_x/a-Si substrates.

Chapter 6 investigates the influences of boron spin-on doping on the quality of p-type poly-Si passivating contacts. The substrates are industrial planar a-Si/SiO_x/c-Si/SiO_x/a-Si structures.

Chapter 7 gives conclusions and outlooks of this thesis.

II. Fundamental and fabrication of poly-Si passivating contacts

In this chapter, the basic structure of a poly-Si passivating contact, and their physical mechanisms are reviewed. We summarize main doping methods for fabricating poly-Si passivating contacts.

2.1 Structure and physical properties

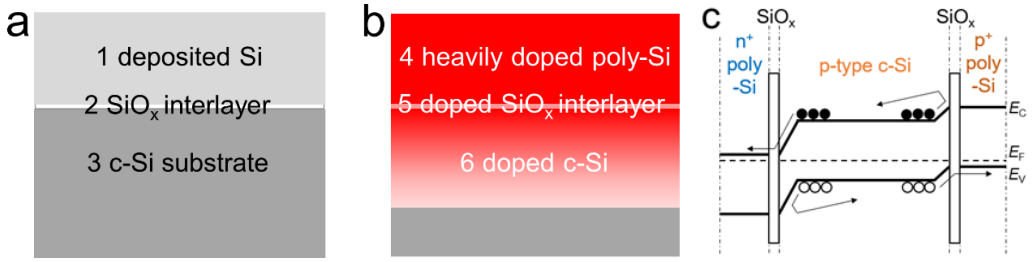


Figure 2.1 (a) A sketch of the precursor for a poly-Si passivating contact before the dopant diffusion process; (b) The basic structure of a poly-Si passivating contact; (c) the band diagram of n- and p-type poly-Si passivating contacts [90].

The basic structure of a poly-Si passivating contact is indicated in figure 2.1. In figure 2.1a, region 1 contains intrinsic amorphous silicon (a-Si) or polycrystalline silicon films (poly-Si). Region 2 is an ultrathin SiO_x layer with a thickness ranging from 1 nm to 3 nm. Region 3 is the crystalline silicon substrate. After a high temperature process, dopants are in-diffused and poly-Si passivating contact is formed, as shown in figure 2.1b. Region 4 represents the n- or p-type heavily doped poly-Si layer. Region 5 is the doped SiO_x ultrathin interlayer. Region 6 indicates the shallow doped region in silicon substrate.

The physical mechanisms of the poly-Si passivating contacts remain in investigation and discussion. First, the key element of a poly-Si passivating contact is the ultrathin SiO_x interlayer. After a high temperature annealing, this ultrathin interlayer will passivate dangling bonds at SiO_x/c-Si interface by allowing bond reorganization [11]. The defect density, represented by interface state density (D_{it}), will then become lower, meaning less recombination centres [74, 91-99]. Besides, during high temperature treatments, this oxide interlayer performs a diffusion barrier that slows down dopant in-diffusion from poly-Si film towards c-Si substrate [75, 95]. This contributes to form a highly doped but shallow region in c-Si below SiO_x interlayer, which will be discussed later. In addition, though SiO_x is dielectric, its ultrathin interlayer allows carrier transport from c-Si to poly-Si. But the mechanism of carrier transport across SiO_x interlayer strongly depends on the oxide thickness

[54]. Some researchers find that the transport is achieved by tunnelling effect for thin (< 1.5 nm) oxide interlayer [73, 100-104], while other investigations indicated that the pinholes on thick (> 2 nm) oxide interlayer enables this transportation [72, 90, 105-107]. The exact mechanisms of carrier transport remain widely investigated.

Secondly, the highly doped poly-Si layer also plays an important role in a poly-Si passivating contact. After a high temperature treatment, the amorphous silicon film will become partially crystallized and a high level of dopants get activated [73, 108]. This will form large work function difference between poly-Si and c-Si, leading to a shifting of quasi-Fermi level in the wafer to align with the quasi-Fermi level in poly-Si, resulting in a high band bending near SiO_x interlayer [11, 47, 108, 109]. As a result, a strong field effect passivation is obtained and minority carrier density (MCD) near SiO_x/c-Si interface is reduced [13, 90, 110, 111]. At the same time, this highly doped poly-Si efficiently extracts the majority carriers, which enhances carrier selection.

Thirdly, as mentioned above, a highly doped but shallow region in c-Si below SiO_x interlayer is essential. The active dopant concentration at c-Si surface is almost as high as in poly-Si, but concentration decreases steeply with increased depth in c-Si [109]. This provides a built-in electrical field in c-Si below SiO_x, which helps to reduce minority carrier density at SiO_x/c-Si interface [3]. This shallow region is also beneficial for lateral transport of majority carriers near c-Si surface.

2.2 Fabrication approaches of poly-Si passivating contacts

The process of introducing dopants into the poly-Si is an essential step and can be separated into *in-situ* doping approaches and *ex-situ* doping approaches.

2.2.1 *In-situ* doping approaches

One of the common approaches to form doped poly-Si precursors is *in-situ* doping. The dopants (phosphorus or boron are commonly used) can be introduced during either plasma enhanced chemical vapor deposition (PECVD) [76, 94, 112-116], low pressure chemical vapor deposition (LPCVD) [117, 118], or physical vapor deposition (PVD) [98]. In 2014, Feldmann *et al.* deposited *in-situ* doped a-Si layer by chemical vapor deposition (CVD) to form symmetric n^+-a-Si/SiO_x/c-Si/SiO_x/n^+-a-Si and symmetric p^+-a-Si/SiO_x/c-Si/SiO_x/p^+-a-Si structures [76]. After the high

temperature process and a hydrogenation process, the optimal iV_{OC} values of n-type contact and p-type contact were 720 mV and 680 mV, respectively. In 2016, Nemeth *et al.* fabricated high performance high-low junction and p-n junction for solar cell via in-situ doping a-Si:H during PECVD process [112]. They revealed that compared with wet-chemical silicon oxide, the thermally formed silicon oxide interlayer has less defects within it, is more resistant to damaging, and can passivate wafer surface more effective. In 2017, Larionova *et al.* compared the performances of boron doped poly-Si contacts with *in-situ* doped PECVD and *in-situ* doped LPCVD [117]. The contact recombination current density (J_{0C}) of the two kinds of samples both decreased when the annealing temperature increased from 800 °C to 900 °C, but that of p^+ LPCVD contact increased if the temperature was higher than 900 °C while p^+ PECVD contact's J_{0C} kept decreasing. The lowest J_{0C} values of PECVD- and LPCVD- p-type contacts were ~15 and ~18 fA/cm^2 for 1000 and 900 °C drive-in process, respectively. Despite of chemical vapor deposition, the physical vapor deposition also showed potential for highly performing poly-Si contacts. In 2018, Yan *et al*. deposited boron dopant and amorphous silicon simultaneously by PVD [98]. After the high temperature annealing, the samples showed J_{0C} less than 20 fA/cm^2 and contact resistivity (ρ_C) below 50 mΩ·cm^2.The *in-situ* doping approach simplifies the processes by eliminating either the ion implantation or the dopant diffusion [119].

2.2.2 *Ex-situ* doping approaches

In contrary to the *in-situ* approach, *ex-situ* doping separates the silicon film deposition from the doping process, which makes the optimization of either process more convenient.

<1> Dopant-containing gas diffusion

One common *ex-situ* doping approach is to introduce dopants from gas sources, such as $POCl_3$ and BBr_3. The first trial was carried out by Römer *et al*. in 2014. The undoped silicon film was deposited above silicon oxide layer (1.2 – 3.6 nm), followed by a high temperature annealing step and then a $POCl_3$ or BBr_3 diffusion step. They achieved the combination of low recombination current densities J_{0C} < 20 fA/cm² and low specific contact resistances < 100 mΩ·cm² [74]. In 2015, Yan *et al.* deposited intrinsic amorphous silicon on ultrathin SiO_x layer (~1.4 nm) with PECVD followed by a high temperature POCl3 diffusion. After the forming gas annealing, a low J_{0C} < 5 fA/cm^2 was obtained, and the contact resistivity ρ_C increased from 16 mΩ·cm^2 to 70 mΩ·cm^2 with i-Si thickness

ranging from 30 nm to 60 nm [75]. One year later, they published a work about boron diffused poly-Si passivating contact based on PECVD intrinsic a-Si and BBr_3 diffusion. The recombination current parameter J_{0C} ranging from about 16 fA/cm^2 to about 30 fA/cm^2 and the contact resistivity was about 8 mΩ·cm^2 for a range of intrinsic a-Si thickness from 36 nm to 46 nm [120]. In another case, some progress towards doped LPCVD passivating contacts has been made. In 2017, Çiftpinar *et al.* applied $POCl_3$ and BBr_3 diffusion on LPCVD-deposited intrinsic poly-Si/SiO_x structure and achieved excellent results. The n-type 100 nm poly-Si passivating contact showed an implied open-circuit voltage of 744 mV after SiN_x hydrogenation, and the p-type 200 nm poly-Si contact had an iV_{OC} of 728 mV [18]. The deposition and diffusion of gas dopants offer significantly higher throughput and provides an effective removal of Fe impurities at the same time; this method also induces less damage into the crystal lattice [121]. Recently in solar cell industry, $POCl_3$ diffusion has helped to manufacture excellent poly-Si passivating contacts on large-area industrial wafers and achieve high average open circuit voltage over 700 mV as well as high average efficiency over 23% for a large number of cells (more than 20000 pieces) [122].

<2> Ion implantation

Ion implantation is also widely implemented to introduce dopants into poly-Si. In 2014, Peibst *et al.* [123] and Römer *et al.* [124] fabricated both n- and p-type poly-Si/SiO_x contacts using ion implantation, achieving lowest J_{0C} ~1.3 fA/cm^2 (highest iV_{OC} 742 mV) and < 5 fA/cm^2 (714 mV), respectively. Also in 2014, Feldmann *et al.* implanted P and B ions into the a-Si layer prepared by PECVD on SiO_x ultrathin layer. They surveyed the influences of implantation energy, ion dose, and high temperature annealing step on the quality of contact. The high passivation performance, iV_{OC} of 725 mV and 694 mV for n-type and p-type contact, respectively, open a new route to form passivating contact [125]. Afterwards, in 2017 Feldmann *et al.* deposited amorphous silicon by LPCVD and loaded phosphorus and boron dopants by ion implantation. Excellent passivation with iV_{OC} of 733 mV and 696 mV were found for n-type and p-type poly-Si contact, respectively [126]. In 2016, Yang *et al.* also obtained high iV_{OC} of 721 mV and 692 mV from n-type and p-type poly-Si contact structures. They pointed out that excellent interface passivation requires high dopant concentration within poly-Si layer and shallow dopant diffusion in c-Si [127]. Besides boron dopant, gallium was studied to form p-type poly-Si contacts by Young *et al*. using ion implantation. The optimal passivation for PECVD and LPCVD poly-Si samples reached 728 mV and 734 mV,

respectively [128]. The key advantages of ion implantation method are the localized doping and precise control of doping dose [125]. Besides, till now the lowest J_{0C} for poly-Si passivating contacts was achieved via ion implantation [124].

<3> Liquid dopant source

The doping methods as discussed above involve complex facilities (ion implantation) and/or dangerous dopant sources (*e.g.*, PH_3 or B_2H_6 during deposition, $POCl_3$ or BBr_3 for tube furnace diffusion), which increases the fabrication costs remarkably and thus limits the further development of these doping processes. Compared with these methods, the doping methods using liquid dopant sources have some significant advantages:

- In liquid sources, the dopant concentrations can be constrained in relatively narrow ranges, though not as precisely as using ion implantation [129];
- The sources can convey special dopant elements that are difficult for other methods [130];
- Diverse liquids can be applied on different positions on one substrate, which will improve the versatility of processes [131];

Based on the features, the liquid dopant sources can combine with printing technology, such as the screen-printing, the inkjet-printing, and the spin-on doping, *etc*.

The screen-printing technique seems to have not yet been applied on poly-Si passivating contact fabrication. The inkjet-printing is a contactless and mask less technology that uses less material waste and has a high degree of compatibility with large scale production [132]. These features make inkjet-printing applicable in many fields of silicon solar cell [133]. The inkjet-printing has been applied to form n- and p-type poly-Si passivating contacts in 2018, showing considerably high iV_{OC}s of 726 mV for phosphorus-doped contact and 692 mV for boron-doped one [134]. After optimization, the iV_{OC} for phosphorus-doped inkjet-printed contact increased to 733 mV [135] and a cell efficiency of 17.1% was obtained with the contribution of this inkjet-printed n-type contact [136].

Different from printed liquid dopant sources, the spin-on doping technique can spread liquid dopants on a large area wafer uniformly [137]. This technique has been widely used to form field effect transistors, electroluminescence devices, and optoelectronic devices [137-139]. Recently the spin-on doping method has also been applied in the poly-Si passivating contacts. Fogel *et al.* loaded the

phosphorus and boron dopants onto the symmetric a-Si/SiO_x/c-Si/SiO_x/a-Si structures with spin-on dopants and diffused dopants into samples using high temperature annealing [140]. Then the structures were coated with Al_2O_3 layers via atomic layer deposition and were annealed in forming gas. The samples with P doped PECVD poly-Si and LPCVD poly-Si showed a final iV_{OC} of about 710 mV and 720 mV, respectively; and the samples with B doped PECVD poly-Si and LPCVD poly-Si showed the final iV_{OC} of about 665 mV and 680 mV, respectively. Ga-doped poly-Si passivating contacts via spin-on doping also exhibited high iV_{OC} above 730 mV after AlO_x hydrogenation [89, 140]. These outcomes indicate spin-on doping is a potential substitution of common gas diffusion or ion implantation.

However, there is only limited work so far published on spin-on doping processes for poly-Si passivating contacts and many parameters of the exact fabrication steps (the spin-coating, the baking, the thermal treatment, *etc.*) remain to be investigated. For example, the spin-coating process involves spin speed, spin acceleration, spin time, and dose of spin-on dopant solution. Baking temperature and time matters to the drying process. Drive-in temperature and dwell time show large effects during high temperature treatment. Especially, the applicability of this doping method to industrially processed poly-Si passivating contacts has not been studied yet. This thesis will explore the impact of phosphorus or boron spin-on doping processes on poly-Si contact properties using precursors obtained from industrial production lines.

III. Spin-on doping technique

This chapter presents a literature review on the spin-on doping for silicon solar cells and using spin-on dopants to fabricate poly-Si passivating contacts.

3.1 Advantages, material sources, and basic findings

A spin-on doping process usually involves a step of spin coating a liquid dopant source on substrate surface, followed by a thermal treatment to activate and diffuse dopants in silicon substrates. Compared to other doping processes, the spin-on doping has several advantages [84, 141, 142]:

i. The spin-on film may contain diverse chemical elements as dopants in one dopant source.

ii. The spin-on doping can be used for dopants which are inconvenient or impossible for other doping processes, such as Al, Ga, As, Sb, Pt or Pd, *etc* [84].

iii. Spin-on doping is much less dangerous than conventional gas diffusion doping [143].

iv. Spin-on doping can be easily implemented with rapid thermal annealing [144, 145] or laser process [146, 147].

v. The spin-on dopant films can work not only for forming back surface field [148, 149], but also for the passivation [150-153], anti-reflection [153-156], and gettering effect [157, 158].

vi. In addition, the spin-on doping can realize the front side dopant diffusion and rear side dopant diffusion with different dopants at the same time with a single thermal annealing [85, 159].

The spin-on dopant liquids can be composed with various material sources, forming organic-inorganic mixtures, pure inorganic solutions, or pure organic liquids. In organic-inorganic mixtures, silicon-containing organics (such as tetraethyl orthosilicate) are Si sources, alcohol acts as solvents, and dopant-containing chemicals (such as P_2O_5 and B_2O_3) provide dopants [129, 142, 144, 160-163]. To avoid carbon residues in substrates after high temperature treatments, pure inorganic spin-on liquids are introduced. In these liquids, dopant-containing inorganics (such as phosphoric acid and boric acid) are dopant precursors and pure water is used as solvent [148, 164-167]. However, some pure organic spin-on sources have also been reported leaving no carbon residue after thermal processes. The key components are dopant-containing polymers, *e.g.*, poly(diethyl vinyl

phosphonate) and poly(vinyl boronic acid pinacol ester) [168, 169]. Based on the wide range of material sources, diverse chemical elements can be carried by spin-on liquids in inorganic chemical compounds or polymers.

The research on spin-on-doping has found that, in general, the final doping profile and therefore the sheet resistance depends on the subsequent thermal treatment, the dopant concentration in spin-on sources, as well as the spin coating process. Both higher anneal temperature and higher spin-on dopant concentration lead to lower sheet resistance, and the anneal diffuses and activates dopants [33]. The higher temperature shows a stronger effect on sheet resistance compared to the dopant concentration in the spin-on sources [161]. However, when the solubility of the dopant in silicon is approached [162], the active dopant concentration in silicon will reach saturation, and sheet resistance will saturate at the lowest level [161]. The thickness of spun films will be lower for higher spin speed or lower solution viscosity. The spin speed and spin acceleration can be factors which influence the R_{sh} uniformity [142]. After the preparation the spin-on dopant solutions may be unstable, but after aging for some time, the solution will become stable and uniform, which is beneficial for uniform doping [162].

3.2 Application of spin-on doping for silicon solar cells

A number of trials and explorations have shown that the spin-on doping process is a promising doping technique for achieving high efficiency silicon solar cell. The textured solar cell fabricated using P spin-on doping instead of conventional gas doping displayed an efficiency of 14% [170], which suggested that the spin-on doping could be a low cost and industrially compatible fabrication process for c-Si solar cell. Ahmad *et al*. applied the phosphorus acid doping on p-type wafer by spin-on process and thermal treatment [165]. With optimized dopant concentration (40% weight ratio) and drive-in process (900 °C for 30 min), the sample was subjected to thermal oxidation to form 50 – 150 nm oxide anti-reflection layer. The final cell efficiency reached 13%. The spin-on doping process can be easily integrated with rapid thermal process (RTP). Sivoththaman *et al*. applied phosphoric acid solution on wafer directly using spin-on process [164]. After the optimization of RTP conditions, an efficiency above 15% was achieved on the large area (10 cm×10 cm) cells. Cousins *et al*. achieved independent control of light and heavy diffusions of selective

emitter formation for solar cells [171]. The lightly doped spin-on glass (SOG) was spun on substrate directly, followed by undoped SiO_2 SOG spinning. Then grooves through these two layers into the wafer were scribed. Afterwards a film of highly doped SOG was spun. After drive-in process, lightly diffused silicon below surface but heavily diffused regions in grooves were obtained.

For boron spin-on doping on n-type wafers, some exciting results are also achieved. Lee *et al.* used spin-on B dopant for BSF formation, which yielded a cell with an efficiency of 14.6% and a V_{OC} of 594 mV [172]. In 2013, a large area bifacial cell fabricated using spin-on boron doping demonstrated an efficiency of ~19.4%, which was similar to that of large area cell based on BBr_3 diffusion [173]. Singha *et al*. supported the possibility of replacing conventional BBr_3 diffusion with B spin-on dopant by obtaining almost the same effective carrier lifetime from the two doping processes [174]. Like what traditional BBr_3 diffusion does, B spin-on doping also forms a boron-rich layer (BRL) after drive-in process, which is harmful to cell performance. Singha *et al*. conducted a series of experiments to suppress the impacts from BRL. The dopant sources are mainly commercial B spin-on dopant (SOD) solution and lab-made diluted boric acid (BA) solution. Firstly, they tried three processes, including diluting B-containing solution, low temperature oxidation, and hot HNO_3 oxidation, to reduce the BRL [175, 176]. For 850 – 900 °C drive-in process, a 700 °C oxidation would reduce BRL thickness considerably and a nitric acid oxidation would remove BRL almost completely. The optimized low-temperature oxidation process was 700 °C for 20 min [177], which improved bulk minority carrier lifetime remarkably. After this, they adjusted the dopant concentration in both kinds of spin-on solutions [178, 179]. It was found that, a lower dopant concentration would clearly lead to a thinner BRL and a higher sheet resistance. Then, the influences of dopant concentration, drive-in temperature, and drive-in dwell time were investigated comprehensively. For the two kinds of spin-on solutions, it was observed that a lower dopant concentration, a lower drive-in temperature, and a shorter dwell time would produce a thinner BRL [180, 181]. For commercial B-SOD the BRL should be removed totally, but for BA solution a BRL thinner than 20 nm could improve passivation quality. In terms of optical property, a thicker B-SOD-derived BRL would reflect more incident light of low wavelength range, but let more light of IR region transmit [182]. Recently, based on the results above, Singha *et al*. optimized the spin-on

doping process using commercial B-SOD [183]. Without any passivation, the implied open-circuit voltage reached about 600 mV, and the estimated cell efficiency was 14.8% via PC1D simulation.

As described above for advantages of spin-on doing, the simultaneous doping on two wafer sides with different dopants can be realized under one drive-in process. By achieving simultaneous diffusions using spin-on dopant sources, Ebong *et al*. successfully reduced the number of high temperature treatment steps for fabricating Double Sided Buried Contact (DSBC) silicon cells with an efficiency of ~15% [184]. Krygowski *et al*. also employed spin-on doping to fabricate cell samples [185], which eventually showed an emitter saturated current density of ~100 fA/cm^2 and a cell efficiency of 19 – 20%. After optimizing the P concentration in spin-on film, Noël *et al*. reported an efficiency of 17.5% from a 25 cm^2 cell using simultaneous doping of P and Al [85]. The spin-on doping of phosphoric acid and boric acid for front emitter and rear BSF respectively yielded a cell efficiency up to 19.2% [159]. These results show that c-Si cells of considerable efficiency can be fabricated via bi-facial simultaneous doping using spin-on doping.

3.3 Spin-on doping for poly-Si passivating contacts

Based on the results discussed above, researchers explored the pathway of using spin-on doping to fabricate poly-Si passivating contacts. In 2017, Fogel *et al*. tried the spin-on doping processes for IBC cells on intrinsic silicon (i-Si) layers deposited by PECVD or LPCVD above the ultra-thin thermal SiO_x layers [140]. After depositing 50 nm a-Si via PECVD, a pre-anneal consist of 850 °C anneal and ALD Al_2O_3 hydrogenation was performed, followed by a lifetime test. Yet for 100 nm intrinsic poly-Si, a lifetime test was performed directly after LPCVD without a pre-anneal process. The iV_{OC} for LPCVD sample (~590 mV) is lower than for PECVD sample (~705 mV). This was attributed to Al_2O_3 hydrogenation on PECVD sample. Afterwards, Al_2O_3 film on PECVD sample was removed using HF, and both PECVD sample and LPCVD sample were coated by P-containing SOG films via spin coating. The lifetimes were measured after 850 °C-60 min N_2 annealing and Al_2O_3 hydrogenation, separately. After dopant diffusion, the lower iV_{OC} for LPCVD sample (~565 mV vs. ~640 mV) was ascribed to insufficient active dopants near SiO_x interlayer. However, after Al_2O_3 hydrogenation the LPCVD sample showed higher iV_{OC} of ~720 mV than PECVD sample of ~705 mV. The contact resistivity values were measured using transfer length method (TLM) method.

The contact resistivity for PECVD and LPCVD sample was 24 and 16 mΩ/cm^2, respectively. For B spin-on doping, a similar process flow was implemented. The initial iV_{OC} for PECVD sample was ~700 mV while for LPCVD sample it was ~575 mV. After dopant diffusion and Al_2O_3 hydrogenation, the final iV_{OC} for PECVD sample was ~665 mV and for LPCVD sample was ~685 mV. The authors owed this difference to more B-O complexes as recombination centres in diffused wafer base for PECVD sample [186]. The contact resistivity for LPCVD sample was 0.31 mΩ/cm^2. Unfortunately, the B doped PECVD sample did not have contact resistivity measurement because of the low final iV_{OC}.

Compared with P or B spin-on doping, the Ga spin-on doping is able to form p-type poly-Si contacts with high passivation quality. Fogel *et al*. also investigated the impacts of Ga dopants [140]. For the sample with 20 nm PECVD silicon, the initial iV_{OC} was ~700 mV before activation. After 60 min diffusion as well as Al_2O_3 hydrogenation, the iV_{OC} increased to ~730 mV. For LPCVD-deposited 100 nm silicon, the initial was ~590 mV, but a longer diffusion dwell time followed by Al_2O_3 hydrogenation improved the passivation quality up to iV_{OC} of ~710 mV. Comparing the results for Ga doping and B/P doping, we can observe some obvious difference. Based on PECVD silicon layers, the higher final iV_{OC} for Ga-doped sample than for B-doped one suggested that diffused Ga dopants seem not form detrimental complexes in wafer below SiO_x interlayer. For samples with LPCVD silicon layers, Ga in-diffusion led to lower final iV_{OC} than P dopant, which was regarded as the consequence of much lower diffusion coefficient and solid solubility limit of Ga in Si [187, 188]. These factors supressed the active Ga concentration near SiO_x interlayer. Another research also obtained high iV_{OC} above 730 mV for Ga spin-on dopant using 50 nm PECVD a-Si after 850 °C-30 min thermal treatment followed by Alneal (Alumina anneal) [89]. However, although Ga-doped poly-Si contacts showed promising passivation quality, their contact resistivity was relatively high. The authors explained this issue was due to the low solid solution limit of Ga in Si, oxide formed on Ga contact surface, as well as the depletion or inertness of Ga dopant in poly-Si [89].

The promising results of spin-on doping discussed above motivated us for further detailed investigations on fabricating poly-Si passivating contacts via spin-on doping technique. Different from Fogel's work, in which investigations were based on lab wafers and lab processes, we did explorations on the impacts of spin-on doping process based on industrial wafers and industrial

processes, such as industrial thermal oxidation and LPCVD Si deposition. As described in section 3.1, spin-on doping is more convenient and safer than other doping approaches. The cost of solar cell fabrication may be lowered considerably if spin-on doping technique shows high compatibility with industrial wafers and processes. On another hand, we added systematic studies on the dependence of passivating contacts quality on spin-on doping process. This process is related to the as-deposited LPCVD a-Si thickness, spin coating process, hard baking step, and high temperature drive-in annealing, which are also the key parts in this work.

IV. Methods of fabrication and characterization

This chapter includes details of fabrication process flow, sample structure, and characterization techniques. We present in detail the passivation measurement, doping profile measurement, and contact resistivity measurement.

4.1 General description

This thesis aims to study in detail the influence of a promising doping method, spin-on doping process, on the performance of n-type and p-type poly-Si passivating contacts. The experiments are conducted on industrially processed wafers with industrial thermal oxide interlayers and industrial LPCVD silicon films fabricated at Jinko Solar. These results may help to push the application of spin-on doping in industrial poly-Si passivating contact production. The impacts of following parameters will be investigated: drive-in temperature, drive-in time, intrinsic amorphous Si layer thickness, spin coating speed, spin coating acceleration, spin coating time, and volume of Spin-on Glass (SOG) solution, and baking time, *etc*. The dopants are phosphorus or boron which are dissolved in Spin-on Glass solutions. The basic fabrication processes and measurements involved in this thesis are listed as table 4.1. The basic process flow and sample structure schemes are displayed in figure 4.1.

Table 4.1 The processes and measurements used in this research.

Processes	**Characterizations & measurements**
Industrial wet chemical polishing: planar surface	Ellipsometry: layer or film thickness
Thermal oxidation: SiO_x ultrathin layer	PL imaging: passivation uniformity
LPCVD: intrinsic amorphous Si film	Photoconductance decay: τ_{eff}, J_0, iV_{OC}
Spin coating: Spin-on-Glass film	ECV: active doping profile
Tube furnace anneal: drive-in & activation	4-point probe: R_{sheet}
HF dip: Spin-on Glass removal	Cox-Strack or TLM: $\rho_{contact}$
Forming gas annealing: hydrogenation	
Al evaporation: metal contact pads/fingers	

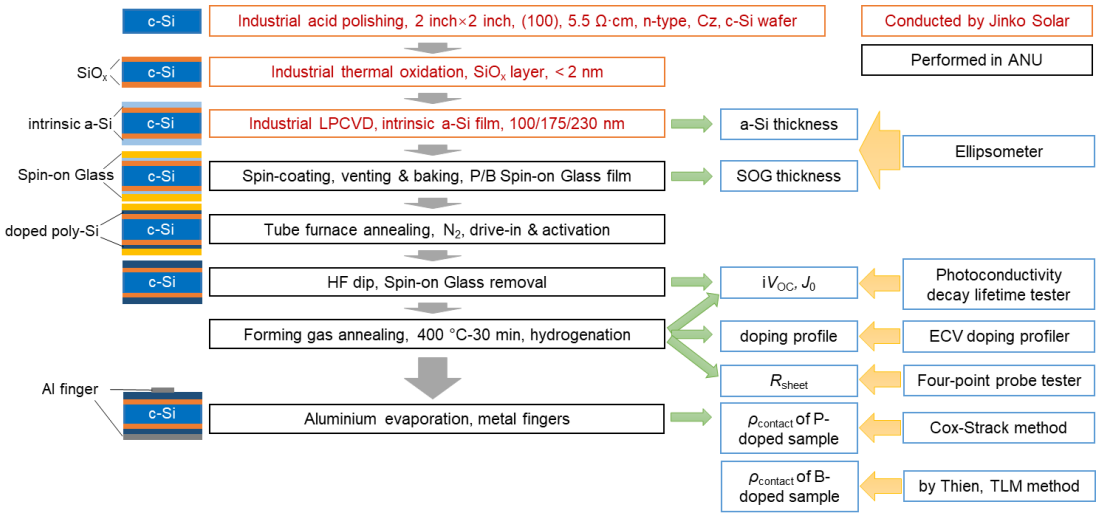


Figure 4.1 The sample structure schemes, process flow, and measurements in this research.

All processes were conducted based on 2 in.×2 in. square (100)-oriented commercial 5.5 ± 0.4 Ω·cm n-type Cz wafers with a thickness of 160 – 170 μm. The saw damages of wafers were removed using industrial wet chemical etching process. The ultrathin silicon oxide layers (thickness < 2 nm [75, 120, 189]) were formed by thermal oxidation on both sides of wafers within pure O_2 at 600 °C for 5 min in a tube furnace. Then silicon oxide layers were capped by intrinsic amorphous Si layers deposited by LPCVD at 520 – 550 °C [79, 92, 111]. All the previous steps were performed by Jinko Solar using industrial mass production tools. The Spin-on Glass solutions are P-containing P-250 ([P] 5×10^{21} cm^{-3}) and B-containing B-1500 ([B] 7.2×10^{21} cm^{-3}) purchased from Desert Silicon. After RCA cleaning, the dopant-rich Spin-on Glass (SOG) films were formed by spin-coating using Laurell WS-650-23NPPB spin-coater. The drying processes include venting (room temperature for 10 min in air), soft baking (90 °C for 10 min in air), and hard baking (200 °C). The spin speed, spin time, spin acceleration, SOG solution volume, as well as hard baking time were varied to explore their impacts on the electric performances of the poly-Si passivating contacts. The drive-in and activation processes were performed using traditional tube furnace in N_2. The drive-in temperature (900 – 1050 °C for P doping, 850 – 1000 °C for B doping) and dwell time (30 – 120 min for P doping, 10 – 90 min for B doping) were varied. After removal of dopant-rich SOG films using diluted hydrofluoric acid (HF), hydrogenation was performed via forming gas annealing (vol_{Ar}:vol_{H2} = 95:5) at 400 °C for 30 min. Finally, the Al contacts were formed on wafer surface via thermal evaporation (30 – 40 °C). For P-doping case, the metal contact samples were sintered in forming

gas at 200 °C for 10 min, while for B-doping case sintering was at 250 °C for 10 min. The PL images were taken for some metallized samples.

The thicknesses of intrinsic amorphous silicon films and SOG films were measured by a focused ellipsometer (J.A. Woollam ESM-300) at the Australian National Fabrication Facility (ANFF) after LPCVD and baked spin coating process, separately. The passivation quality, represented by implied open-circuit voltage (iV_{OC}), was measured by a Sinton WCT-120 Photo-conductance Lifetime tester based on Photoconductance Decay (PCD) method [190] before and after FGA. The passivation uniformity was checked using BT Imaging photoluminescence (PL) images after FGA. The recombination current density (J_0) values were calculated using Kane-Swanson theory [191]. After FGA, the active doping profiles were measured by WEP Wafer Profiler CVP21 based on electrochemical capacitance-voltage (ECV) theory [192, 193]. The contribution of Auger recombination to the overall J_0 as well as the sheet resistances were simulated via EDNA2 [194], using the measured active dopant profiles as inputs, but without the profile parts in poly-Si layers. The contact resistivity was measured by Keithley Sourcemeters 2400 using *I-V* curves based on Cox-Strack theory [195] for P-doped poly-Si contacts or transfer length method (TLM) [196, 197] for B-doped poly-Si contacts. The passivation quality of these metallized samples was also checked by PL imaging.

4.2 Key processes in fabrication

4.2.1 Thermal oxidation

Among the diverse oxidation methods, thermal oxidation takes the advantages of stability and large production throughput. Uniform ultrathin oxide layers can be formed on thousands of wafers in one batch [122, 198, 199]. In our work, the ultrathin silicon oxide layers were formed on both sides of wafer using thermal oxidation process performed by Jinko Solar with an industrial LPCVD tool. Additionally, the thin oxide can be easily integrated with LPCVD poly-Si deposition process, which simplifies the fabrication process and avoids contamination during the sample transportations.

4.2.2 LPCVD Si deposition

In this thesis, the intrinsic silicon films above SiO_x layers on both sides of wafer were prepared by Jinko Solar using an industrial low-pressure chemical vapor deposition (LPCVD) tool. LPCVD deposition is a two-side deposition process. The most important feature of LPCVD is its high-production capability and low cost [200-205]. Besides, LPCVD process can fabricate uniform silicon films in terms of both crystallinity and thickness [201-205]. Furthermore, the growth rate and crystallinity of silicon films are controllable, which should be attributed to its low pressure and relatively low deposition temperature during process [201, 203].

4.2.3 Forming gas annealing

During hydrogenation process, activated molecular hydrogen will diffuse into semiconductor and combine with dangling bonds, thus reducing interface state density (D_{it}) [206, 207]. As a result, the carrier recombination is suppressed, and thus more carriers are collected. Therefore, a hydrogenation process is an essential step for surface passivation of silicon. The work in this thesis focuses on spin-on doping for poly-Si passivating contacts, so only forming gas annealing (FGA) was employed. This process uses common tube furnace at temperature of 400 – 500 °C [37, 207].

4.3 Key characterizations and measurements

4.3.1 Photoconductance decay and Suns-V_{OC} theories for passivation quality

The surface passivation qualities of silicon wafers, which can be quantified as effective lifetime (τ_{eff}), saturated recombination current density (J_0), and implied open-circuit voltage (iV_{OC}), were measured using Sinton WCT-120 lifetime tester [190] based on photoconductivity decay theory and Kane-Swanson method [191], as indicated in figure 4.2.

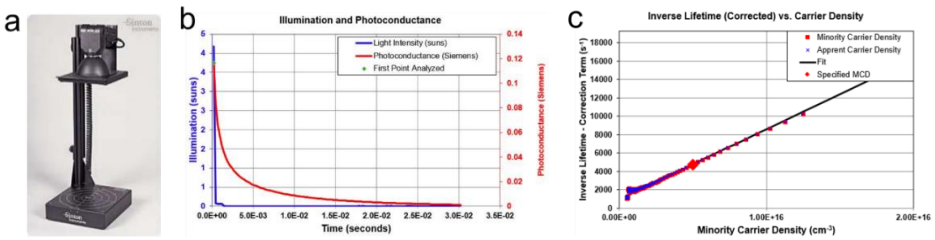


Figure 4.2 (a) A photo of Sinton WCT-120 lifetime tester [208]; (b) an example photoconduction decay curve; (c) an example inverse carrier lifetime curve.

The test sample is placed above a coil, which measures the conductance in test sample via inductive

coupling technique [190]. A flash towards test sample excites a high density of photo-generated carriers leading to an increase in conductance. After stopping the flash, the excited carriers will recombine quickly, leading to conductance decrease as shown by red curve in figure 4.2b. Based on conductance changes of silicon samples, the carrier lifetime and corresponding minority carrier density can be calculated. According to Kane-Swanson method, when the carrier diffusion length is much larger than wafer thickness, and carrier diffusion velocity is much higher than effective recombination velocity, the carrier density in wafer will change rapidly and uniformly (such as excessive electron density Δ_n) [191].

In this case, the effective lifetime (τ_{eff}) can be expressed as equation 4.1 below [209]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{intr}} + \frac{1}{\tau_{SRH}} + \frac{J_0}{qWn_i^2}(N_D + \Delta_n) \tag{4.1}$$

where τ_{intr} is the radiative and Auger recombination-related lifetime in wafer base; τ_{SRH} is the Shockley-Read-Hall lifetime in wafer base; W is wafer thickness, q is elementary electric charge, and n_i is intrinsic carrier concentration (8.3×10^9 cm^{-3} for silicon at 25 °C [12]). Besides, N_D is the base doping level. It can be found that effective lifetime depends on excessive minority carrier density. The curve of corrected inverse lifetime ($1/\tau_{eff}$ - $1/\tau_{intr}$) over Δ_n can be fitted into a straight line, as the black line presented in figure 4.2c. Thus, based on the equation 4.1, recombination current density (J_0) can be extracted from the slope of corrected inverse lifetime vs. Δ_n curve for a specific excessive minority carrier density, as shown in figure 4.2c.

To know overall passivation quality of a silicon wafer with poly-Si passivating contact, the implied open-circuit voltage (iV_{OC}) (at 1 sun) is used. Just after obtaining PCD curve, the iV_{OC} is calculated by the lifetime tester using the equation 4.2 below [190, 210]:

$$iV_{oc} = \frac{kT}{q} ln\left[\frac{\Delta_n}{n_i^2}(\Delta_n + N_D)\right] \tag{4.2}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, n_i is the intrinsic carrier density, and N_D is the n-type donor dopant density in wafer (N_A corresponding to p-type acceptor dopant density). It can be found that under a specific donor or acceptor dopant density, the iV_{OC} is positively correlated with maximal excessive minority carrier density [210]. Because Δ_n is calculated using wafer bulk resistivity and wafer thickness, iV_{OC} is affected by these two wafer parameters. The error bars of iV_{OC} values are obtained by recalculating iV_{OC} in Sinton WCT-120 considering the range in bulk resistivity (5.1 – 5.9 Ω·cm) and wafer thickness (160 – 170

μm).

4.3.2 Electrochemical capacitance-voltage profiling for doping profiles

In the electrochemical capacitance voltage (ECV) measurements, metal contact is replaced with an electrolyte solution to perform capacitance-voltage measurement [192]. This method has many advantages [192, 193, 211-214] as the etching process and ECV measurement can be performed in the same cell and controlled precisely, so that the etch/measure cycle can be repeated automatically and profiles can be plotted continuously. Besides, the measurement has a clear depth resolution and the depth will not be limited by the electrical breakdown. This method provides information of electrically active dopants.

For calculating the concentration of electrically active dopant at a specific depth, some items need to be introduced. A is the effective area of electrolyte/semiconductor contact, C is measured capacitance, V is applied voltage bias, q is element charge, and ε is effective dielectric constant. The active dopant concentration $N(w)$ corresponding to etching depth w can be expressed as equation 4.3 [192, 193]:

$$N_{(w)} = -\left(\frac{C^3}{q\varepsilon A^2}\right)\left(\frac{dC}{dV}\right)^{-1} \tag{4.3}$$

After obtaining the capacitance at specific voltage bias and specific depth, the electrically active dopant density can be calculated. We used this tool to find out the amount of active dopants in our poly-Si contact structure from the spin-on doping processes. The error bars of the data for doping profiles are extracted directly by the ECV system.

4.3.3 Cox-Strack method and TLM method for contact resistivity measurement

The contact resistivity plays an important role in solar cell performance. There are two methods we used to measure contact resistivity, *i.e.* Cox-Strack method [195] and transfer length method (TLM) or transmission line model method [196, 215].

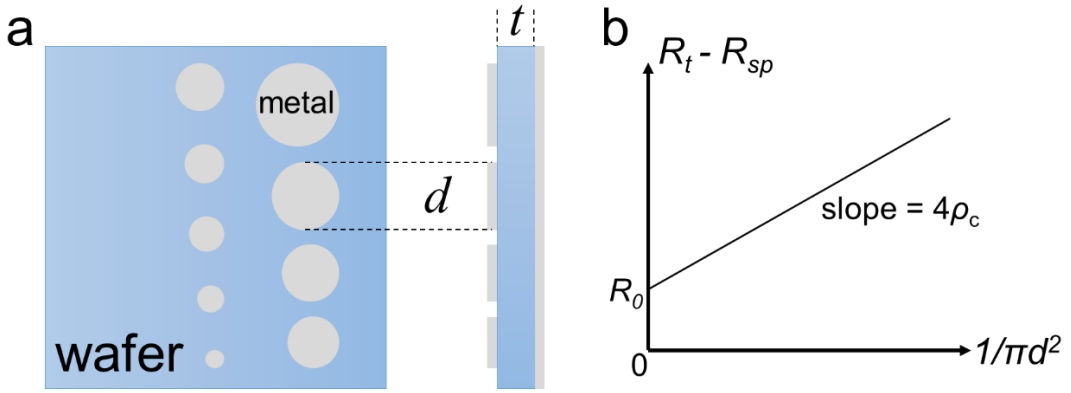


Figure 4.3 (a) The sketch of sample structure and (b) typical plot of Cox-Strack measurement [195, 216].

Figure 4.3 displays the sketch of a sample for Cox-Strack method. In Cox-Strack method, a set of round metal disks with increasing diameter (0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6, and 0.8 cm) are formed on the front side of sample, while the rear side is fully covered with metal film. Because the area of rear metal film is much larger than front metal contacted areas, the impact from rear side/metal interface and rear metal film can be ignored. The measured total resistance (R_t) is the sum of spreading resistance (R_{sp}), contact resistance (R_c), and residual resistance (R_0). The equation can be expressed as below:

$$R_t = R_{sp} + R_c + R_0 = \frac{\rho}{\pi d}\tan^{-1}\frac{4t}{d} + \frac{4\rho_c}{\pi d^2} + R_0 \tag{4.4}$$

where, ρ is substrate resistivity, d is disk diameter, t is substrate thickness, ρ_c is contact resistivity (or specific contact resistance). Then equation 4.4 can be transformed to equation 4.5:

$$R_t - R_{sp} = R_t - \frac{\rho}{\pi d}\tan^{-1}\frac{4t}{d} = R_c + R_0 = \frac{4\rho_c}{\pi d^2} + R_0 \tag{4.5}$$

For a specific metal disk, the total resistance can be calculated via measured *I-V* curve, and the spreading resistance can also be obtained using the first item in equation 4.4. Therefore, for metal disks with a series of diameters, a series of total resistances and spreading resistances can be attained. Then the difference between R_t and R_{sp} (R_t - R_{sp}) will show a linear dependence over $1/\pi d^2$, as plotted in figure 4.3b. The y-intercept refers to R_0. The contact resistivity (ρ_c) can be calculated from the slope ($4\rho_c$). The unit is usually $m\Omega\cdot cm^2$. The errors of contact resistivity values were obtained using different bulk resistivity (ρ, 5.1 – 5.9 $\Omega\cdot$cm) and varied wafer thickness (t, 160 – 170 μm).

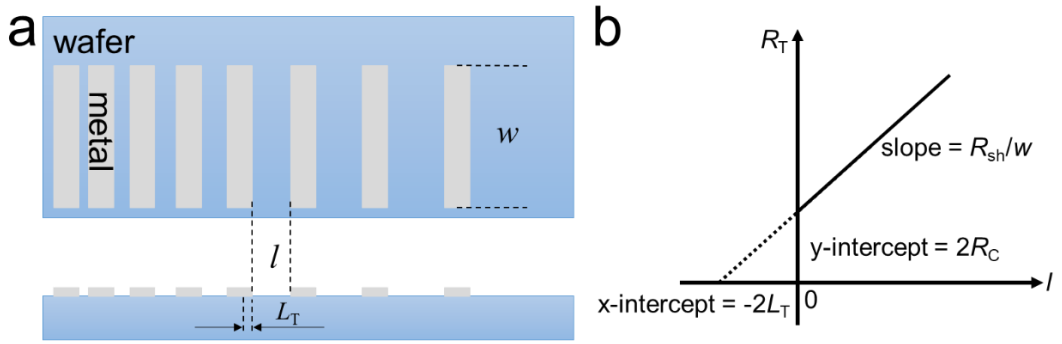


Figure 4.4 (a) The distribution of fingers on wafer surface and (b) typical plot for TLM measurement [196, 216].

Figure 4.4 shows the typical structure of the sample for TLM method. A set of rectangle metal fingers are formed on the single side surface. The dimension of these fingers is same, where w is the width. But the interval (l) between two rectangle metal contacts varies. The measured total resistance (R_t) is given by equation 4.6:

$$R_t = 2R_c + \frac{R_{sh}}{w} l \tag{4.6}$$

where R_c is contact resistance, and R_{sh} is sheet resistance. The curve of measured R_t values as a function of l can be fitted by a straight line, as shown in figure 4.4b, then the slope, x-intercept, and y-intercept can be extracted. The slope is the ratio of R_{sh} over w, y-intercept equals $2R_c$, and x-intercept is equal to $-2L_T$. L_T is the "transfer length" below finger within which carriers transfer between metal and substrate effectively. Therefore, the contact resistivity can be expressed via equation 4.7:

$$\rho_c = R_c L_T w \tag{4.7}$$

The conventional unit is also $m\Omega \cdot cm^2$. We did three TLM measurements for each sample to obtain the errors of contact resistivity.

V Phosphorus doped poly-Si passivating contacts fabricated via spin-on doping

In this chapter, we investigated the impacts of spin coating process, baking process, drive-in temperature, drive-in dwell time, as well as deposited intrinsic silicon film thickness on the performance of n-type poly-Si contacts.

5.1 Doped silicon regions from P spin-on doping

The P spin-on doping was firstly applied directly on crystalline silicon substrates to form doped regions in silicon substrate after high temperature processes. The wafer orientation was (100) and resistivity was about 100 Ω·cm. The saw damage on surface was processed in tetra-methyl ammonium hydroxide (TMAH) solution. Then these wafers were spin coated by a spin-on glass solution directly, skipping the RCA cleaning. We skipped RCA cleaning in these experiments as we cared more about sheet resistance and doping profile than about passivation quality. The spin-on solution was Spin-on Glass (SOG) P-250 ([P] 5×10^{21} cm^{-3}) purchased from Desert Silicon. This SOG solution was also used in the following sections. The spin coating was performed with spin speed of 3000 rpm, spin acceleration of 1000 r/s^2, spin time of 30 s, and solution volume of 90 μL. The hard baking was conducted in air at 200 °C for 5 min on a hotplate. The drive-in dwell time was 60 min. After drive-in process, the remained SOG films were removed by an HF dip. After samples cooling down, the dependences of iV_{OC}, R_{sh}, and doping profile on drive-in temperature were measured using Sinton WCT-120 lifetime tester [190], 4-point probe method, and ECV profiler WEP CVP21, respectively. The results are displayed in figure 5.1.

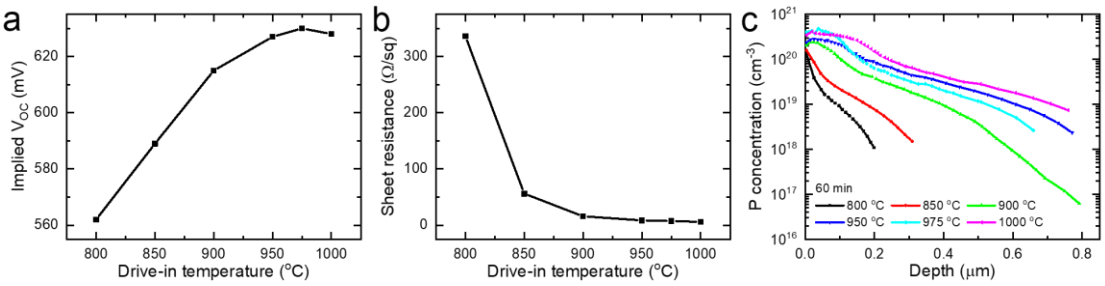


Figure 5.1 The dependences of (a) iV_{OC}, (b) R_{sh}, and (c) doping profile on drive-in temperature for n-type wafer doped by P spin-on doping.

The iV_{OC} increases gradually with a higher drive-in temperature and reaches 630 mV. The sheet resistance decreases fast from 800 °C to 850 °C and then decreases slowly below 50 Ω/sq till 1000 °C. The widely used drive-in temperature for $POCl_3$ diffusion is lower, with a range from 840 °C to 850 °C [217-219]. In our 850 °C doping profile, the active P concentration near wafer surface is ~2×10^{20} cm^{-3}, and concentration of 1 – 2×10^{18} cm^{-3} is observed at ~0.3 μm depth. This doping profile shows lower near-surface concentration and deeper in-diffusion than the doping profiles obtained from $POCl_3$ diffusion, as indicated in ref. [217, 218], but has almost the same concentration distribution as the doping profile for highest passivation in ref. [219]. The possible reason of this difference may be the shorter drive-in dwell time in ref. [217, 218]. The doping profiles show that a higher drive-in temperature leads to higher active dopant concentration near wafer surface and deeper profile in wafer bulk, which may reduce the density of minority carrier and suppress the carrier recombination.

5.2 Impacts of spin coating process on passivation quality for poly-Si passivating contact

The aim of this section is to study how the spin coating process impacts passivation quality of poly-Si passivating contact, which can be indicated by implied V_{OC} and passivation uniformity. There are four parameters examined in this process: spin speed, spin time, spin acceleration, and volume of spin-on dopant solution. The samples before spin coating in this section were symmetric a-Si/SiO_x/c-Si/SiO_x/a-Si structures. The fabrication details can be found in chapter 4. The substrates with this symmetric structure were also used in the following sections. After an RCA cleaning, these substrates were spin coated by spin-on solution SOG P-250 on both sides. The ranges of spin speed (1000 – 5000 rpm), spin time (5 – 60 s), spin acceleration (250 – 2000 r/$s^{2)}$, and solution volume (30 – 180 μL) were used. Following the hard baking at 200 °C for 5 min, the thicknesses of SOG films were also measured by the focused ellipsometer in ANFF. The results are shown in figure 5.2 a – d. Then the samples were annealed and activated in N_2 at 975 °C for 60 min in a tube furnace. During high temperature thermal processes, the a-Si films would be crystallized to poly-Si. The iV_{OC} values and passivation uniformity were checked after an HF dip to remove remained SOG films and after a forming gas annealing (FGA) process. The FGA was performed in a tube furnace in forming gas (5% H_2, 95% Ar) at 400 °C for 30 min. The results are displayed in figure 5.2 e – f.

The passivation uniformity was exhibited by photoluminescence (PL) images as shown in figure 5.3.

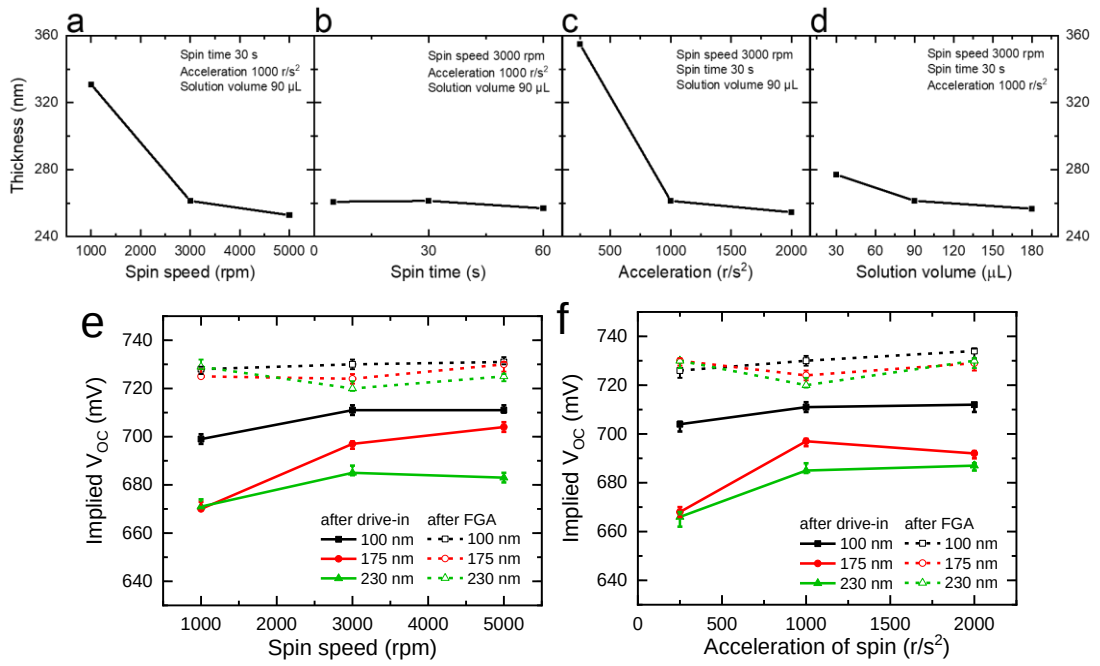


Figure 5.2 The phosphorus-containing SOG thickness as a function of (a) spin speed, (b) spin time, (c) spin acceleration, and (d) solution volume; iV_{OC} values of samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) coated by (e) various spin speeds and (f) spin accelerations, after annealing at 975 °C for 60 min (filled symbols, solid lines) and after FGA (open symbols, dashed lines).

From figure 5.2 a – d, we can find that the spin speed and spin acceleration have larger impacts on the thickness of P Spin-on Glass film, compared to spin time and solution volume. The film thickness decreases apparently with a higher spin speed or acceleration, while a higher spin time or solution volume leads to a slightly thinner SOG film. The film thickness corresponding to 3000 rpm, 30 s, 1000 r/s^2, and 90 µL is 260 – 265 nm.

Generally, as figure 5.2 e – f show, an increased spin speed or spin acceleration results in a higher iV_{OC} before FGA but only slightly influences iV_{OC} after FGA, for all three poly-Si thicknesses. Before FGA the largest iV_{OC} change comes from sample with 175 nm poly-Si, which is about 30 mV. After FGA, the iV_{OC} values for three poly-Si thicknesses fluctuate within 15 mV range. The highest iV_{OC} is ~734 mV after FGA, which belongs to 100 nm poly-Si sample coated with 3000 rpm spin speed and 2000 r/s^2 acceleration.

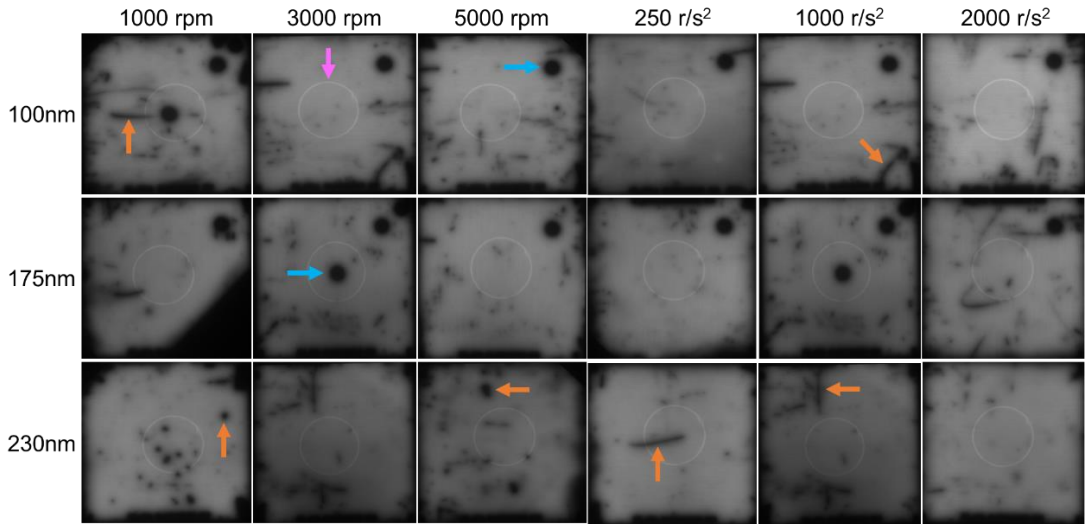


Figure 5.3 The PL images of n-type poly-Si passivating contact samples coated using various spin speeds and different spin accelerations. The poly-Si thickness included 100, 175, and 230 nm. The exposure time was 0.5 s, and illumination intensity was 0.875 suns for all samples.

Figure 5.3 exhibits the PL images to show passivation quality and uniformity on each sample. The 4 inch^2 square substrates with three poly-Si thicknesses were coated with different spin speeds and spin accelerations. The big round black spots at the centre or top right corner (blue arrow) refer to the etched area during ECV profile measurements. The other small round spots and bar-like spots (orange arrow) may represent defects from contaminations, scratches, *etc.* during fabrication processes. Besides, the large white circles in the centre (pink arrow) are measurement artefacts from the inductance coil implemented in the PL chuck. We found that after FGA, the trend of PL intensity for different spin coating conditions is not clear, which corresponds to the iV_{OC} results in figure 5.2. However, some samples show that the PL intensity for thicker poly-Si is lower, such as the cases for 3000 and 5000 rpm spin speed. On samples not shown here, we achieved a uniform passivation on 4 inch wafers with poly-Si contact structure, similar to the work by Yang *et al.* [220], which implies a promising passivation uniformity for P spin-on doping process.

5.3 The dependence of passivation quality on hard baking process

In this section we explored the impact of hard baking time on iV_{OC} and sheet resistance of poly-Si contacts. The symmetric substrates and spin-on solution were the same with which described in section 5.2. The intrinsic a-Si thickness was only 100 nm in this section. The spin coating conditions were 2000 rpm spin speed, 15 s spin time, 1000 r/s^2 acceleration, and 100 µL solution volume. After

drying at room temperature and soft baking at 90 °C, the samples were hard baked on a hotplate at 200 °C for 3 – 12 min. Following the drive-in process at 950 °C for 60 min and an HF dip, the FGA was conducted. The iV_{OC} values were measured both before and after FGA, but the sheet resistance and ECV doping profiles were measured just after FGA. The results are displayed in figure 5.4.

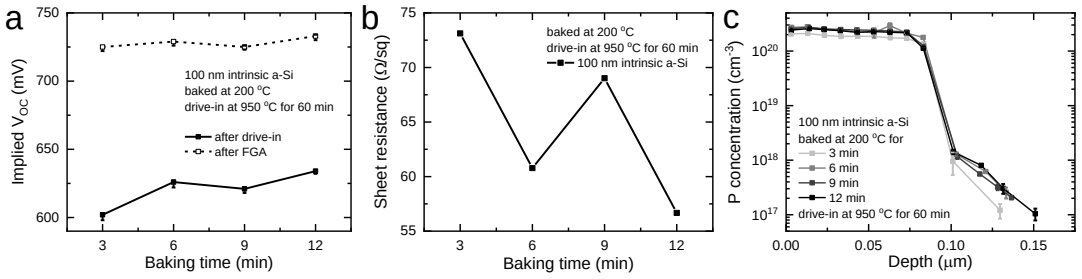


Figure 5.4 The (a) iV_{OC} values (before and after FGA), (b) R_{sh}, and (c) doping profiles for 100 nm deposited Si samples for various hard baking time.

Figure 5.4a shows that after drive-in process the iV_{OC} increases from ~600 mV to ~630 mV, corresponding to 3 min and 12 min baking respectively. After FGA, this trend becomes less obvious with an iV_{OC} change between 725 and 730 mV, which is close to the error bar range. On another hand, it can be found from figure 5.4b that the sheet resistance (R_{sh}) decreases, though not linearly, from ~73 Ω/sq down to ~57 Ω/sq when baking time increases from 3 min to 12 min. The doping profiles with error bars (figure 5.4c) shows when baking time ramps up from 3 min to 6 min, doping profile reaches higher and deeper level, but the change in doping profile for 6 – 12 min baking is less apparent. The iV_{OC} before FGA and the R_{sh} changes for 3 – 6 min baking may be explained by the higher and deeper profile, induced by more evaporated solvent in as-spun film thus speeding film solidification and driving more dopants into substrate [221-224]. However, this effect is relatively weak for 6 – 12 min baking as we observe similar doping profiles. From these results it can be deduced that for this spin-on solution P-250, 6 min baking is sufficient for achieving high passivation and low sheet resistance.

5.4 Impacts of drive-in temperature on passivation quality and contact resistivity

After studying the influences of the former two steps in spin-on doping process, we investigated the impacts of drive-in temperature, which was thought as the most important role in deciding performance of a poly-Si passivating contact. Indeed, the drive-in process controls ex-situ doping

level in poly-Si film and c-Si wafer, as well as the damage extent of silicon oxide interlayer. The major process flow was similar to that in section 5.3, except for intrinsic a-Si thickness, hard baking time, and drive-in process. The a-Si (or poly-Si) thickness in this section included 100 (black), 175 (red), and 230 (green) nm. The hard baking time was 5 min. The drive-in temperature ranged from 900 °C to 1050 °C, and drive-in dwell time was set as 60 min. The iV_{OC} for 850 °C drive-in was too low to be measured, even after FGA. The iV_{OC} for 230 nm poly-Si kept increasing from 950 °C to 1000 °C, showing no trend of decrease or saturation. So, we extended the temperature up to 1050 °C.

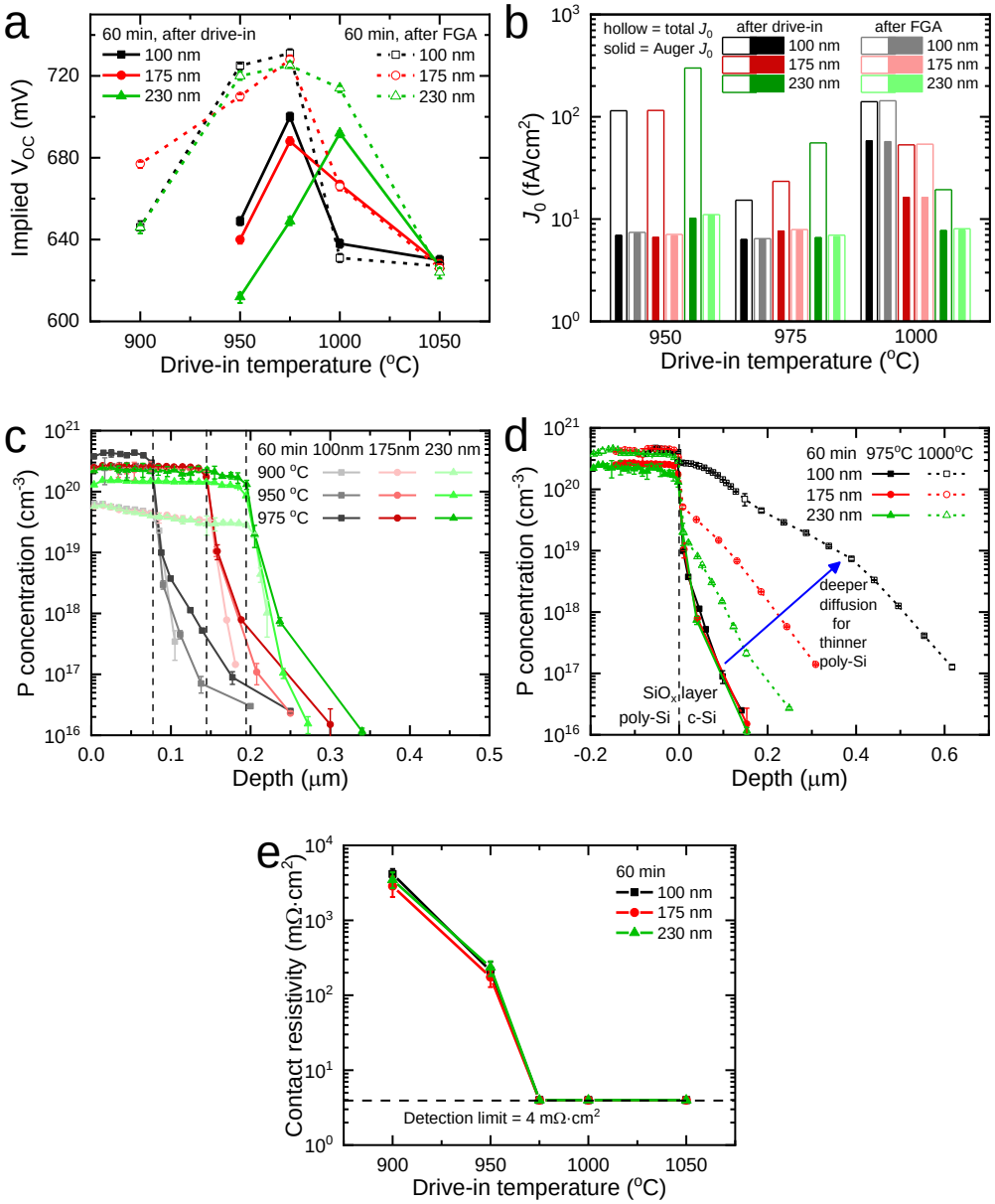


Figure 5.5 (a) iV_{OC} values of P-doped samples for poly-Si thicknesses of 100 (black), 175 (red) and 230 (green) nm annealed for 60 min at different temperatures (filled symbols, solid lines) and after FGA (open symbols, dashed

lines); (b) measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for the three poly-Si thicknesses before and after FGA; the doping profiles of 100, 175, and 230 nm poly-Si samples annealed at (c) 900 – 975 °C and (d) 975 – 1000 °C. The dashed lines indicate the position of the SiO_x interlayers; (e) the corresponding values of contact resistivity after FGA.

Figure 5.5a shows the impact of the drive-in temperature on the passivation quality, via the iV_{OC}, of poly-Si passivating contacts before (full symbol, solid line) and after FGA (open symbol, dashed line). The iV_{OC} values were measured using Photoconductance Decay (PCD) method with a Sinton WCT-120 lifetime tester [190]. Before FGA, the iV_{OC} values for all poly-Si thicknesses first increase with higher drive-in temperature, reaching their maximum, and then decrease at excessively high temperature. The iV_{OC} data for 900 °C is too low to be obtained under the same measurement conditions as for other samples and are consequently not shown here. The optimal drive-in temperature increases for thicker poly-Si, in other words, the iV_{OC} values for 100, 175 nm poly-Si reach the highest values at 975 °C, and the 230 nm poly-Si sample has the highest iV_{OC} at 1000 °C. After FGA, similar iV_{OC} trends are observed. As drive-in temperature increases, the iV_{OC} values for the three poly-Si thicknesses all increase, reaching their maximum about 730 mV at 975 °C. When temperature increases further, the iV_{OC} values all decrease remarkably with a greater reduction for thinner poly-Si layer. The highest iV_{OC} value of 733 mV is obtained for 100 nm poly-Si and 975 °C drive-in temperature. The decrease in passivation quality at excessively high temperatures has also been reported for $POCl_3$ diffused [75, 99, 225] and P implanted [93, 126, 226] poly-Si contacts, even though in these cases the optimal drive-in temperatures are substantially lower (800 – 900 °C). This divergence is probably the consequence of the robust dopant-rich spin-on glass/poly-Si interface [95, 99, 127]. Compared to $POCl_3$ diffusion or P ion implantation, the dopants for spin-on doping may need to overcome a higher energy barrier at SOG/poly-Si interface to achieve in-diffusion.

The increased passivation quality with higher temperature may be explained by an increased doping level leading to enhanced band bending [73] and field-effect [95]. Figure 5.5c displays the ECV doping profiles for three poly-Si thicknesses under 900 – 975 °C. A high doping level in the poly-Si and a considerable dopant diffusion into the c-Si (doping profile tail) are essential to achieve good passivation. For drive-in temperatures below the optimal point, a higher temperature induces higher doping level in the poly-Si, which is more apparent for thinner poly-Si layers. The high

concentration of activated dopants in poly-Si may form a strong band bending near SiO_x/c-Si interface [73] reducing minority carrier density [127]. Meanwhile, a higher temperature leads to higher active dopant concentration in c-Si below SiO_x interlayer and deeper dopant diffusion into the c-Si substrate, which forms stronger built-in electrical field [3] and helps to suppress the minority carrier density near the SiO_x/c-Si interface. The larger increase in doping levels in poly-Si and c-Si below SiO_x may explain lower optimal temperature for thinner poly-Si. Figure 5.5b shows in hollow bars the total recombination current density ($J_{0,total}$), extracted from the PCD measurements using the Kane-Swanson method [191], and in filled bars the Auger contribution ($J_{0,Auger}$) simulated using EDNA2 [194] based on the corresponding doping profiles using only the diffused part in the c-Si wafer. The analysis reveals that after 950 °C drive-in, $J_{0,Auger}$ for three poly-Si thicknesses take small fraction in $J_{0,total}$, meaning that recombination at SiO_x/c-Si interface are dominating. When the temperature increases from 950 °C to 975 °C, we observe almost unchanged $J_{0,Auger}$ (except for 230 nm poly-Si) but notably reduced $J_{0,total}$. This trend could be due to a lower interface defect state density (thus less recombination centres) at SiO_x/c-Si interface for higher annealing temperature, achieved via Si-O bonding rearrangement [97]. This is supported by the observation that after FGA anneal, these defect states can be passivated reaching similar J_0 values for 950 °C to 975 °C. Here the direct evidence of lower interface state density is not presented, but we admit that the characterization of interface state density via capacitance-voltage (C-V) analysis is meaningful and deserves more investigation in the future. Furthermore, for 950 °C after FGA, the $J_{0,total}$ for three poly-Si thicknesses is reduced significantly, indicating that the SiO_x break-up is little and the defects near SiO_x interlayer can be passivated effectively by FGA.

However, when the drive-in temperature is higher than the optimal point, the iV_{OC} values for all three poly-Si thicknesses decrease sharply, down to ~635 mV at 1050 °C. Figure 5.5d compares the doping profiles at 975 °C and 1000 °C, demonstrating that after 1000 °C drive-in the doping profile in c-Si becomes deeper, which is more remarkable for thinner poly-Si. At 1000 °C, the doping profile for 230 nm poly-Si shows that doping level in the poly-Si becomes higher, but dopant diffusion into the c-Si remains relatively shallow compared to 100 or 175 nm poly-Si. The slightly deeper profile tail in c-Si leads to an increase in $J_{0,Auger}$, while a higher doping level in poly-Si may lead to higher band bending, thus lower $J_{0,total}$. These may explain the higher iV_{OC} for 230 nm poly-

Si. Furthermore, the $J_{0,total}$ decrease after FGA for 230 nm poly-Si means FGA can still passivate defects near SiO_x interlayer. However, for 100 or 175 nm poly-Si at 1000 °C, the dopant diffusion into the c-Si is relatively deep, leading to high Auger recombination. At the same time, considerable densities of defects may be formed near the SiO_x/c-Si interface during drive-in process [74, 126]. The high $J_{0,total}$, high $J_{0,Auger}$, and almost no FGA-induced $J_{0,total}$ decrease support that, the heavy Auger recombination and seriously damaged SiO_x interlayer may both contribute to poor passivation for 100 or 175 nm poly-Si [75, 227].

Figure 5.5e presents the corresponding contact resistivity of samples shown in figure 5.5a, measured using the Cox-Strack method [195]. A detection limit of contact resistivity was introduced based on the variations of wafer base resistivity (ρ) and wafer thickness (t). To attain the detection limit of contact resistivity (ρ_c), we firstly found the largest absolute deviation of measured ρ from the mean ρ (5.5 Ω·cm), and worked out the ratio of this deviation over the mean ρ. Then this ratio was multiplied by measured total resistance (R_t) to get the largest absolute deviation of R_t, which acted as the upper limit of contact resistance (R_c) that we were able to measure accurately. Afterwards the R_c upper limit was used together with the second item in equation 4.4 to calculate the upper limit of ρ_c, *i.e.,* contact resistivity detection limit. When the drive-in temperature increases from 900 °C to 975 °C, the contact resistivities of all samples decrease substantially from over 3×10^3 mΩ·cm^2 to below the detection limit of 4 mΩ·cm^2. With further higher drive-in temperature, the contact resistivities remain below this detection limit. The pronounced reduction and low values of contact resistivity can be explained by the increased dopant concentration in poly-Si and c-Si near the SiO_x/c-Si interface, and possibly to a stronger break-up of oxide interlayer produced by higher drive-in temperature [74]. To check whether the passivation remains after metallization, we compare the PL image for an Al metallized poly-Si contact sample (a), as displayed in figure 5.6, to a sample without Al metallization (b). Here, Al is covering the full rear side of the sample while on the front the circular pads of the Cox-Stack measurements are visible in figure 5.6a. Besides, the two samples for figure 5.6 both had 600 °C thermal SiO_x and 175 nm intrinsic a-Si. Also, they both went through 975 °C-60 min annealing and 400 °C-30 min FGA process. A slightly higher PL intensity can be observed from metallized sample in (a) than for the sample without metallization (b), which may be explained by light reflection from Al film on rear side. Therefore, we assume that the metal did not

punch through poly-Si and SiO_x interlayer and the high passivation remained. This means that the low contact resistivity values were not at the sacrifice of passivation.

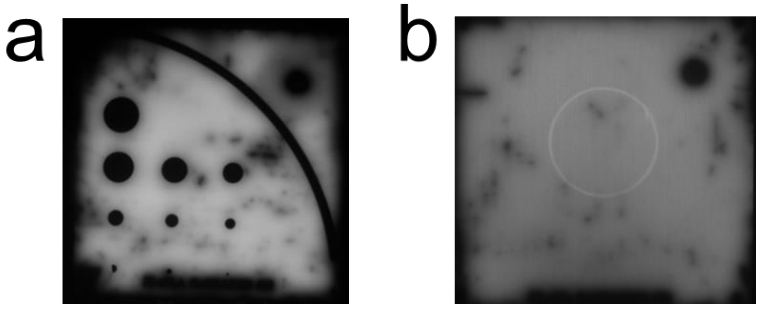
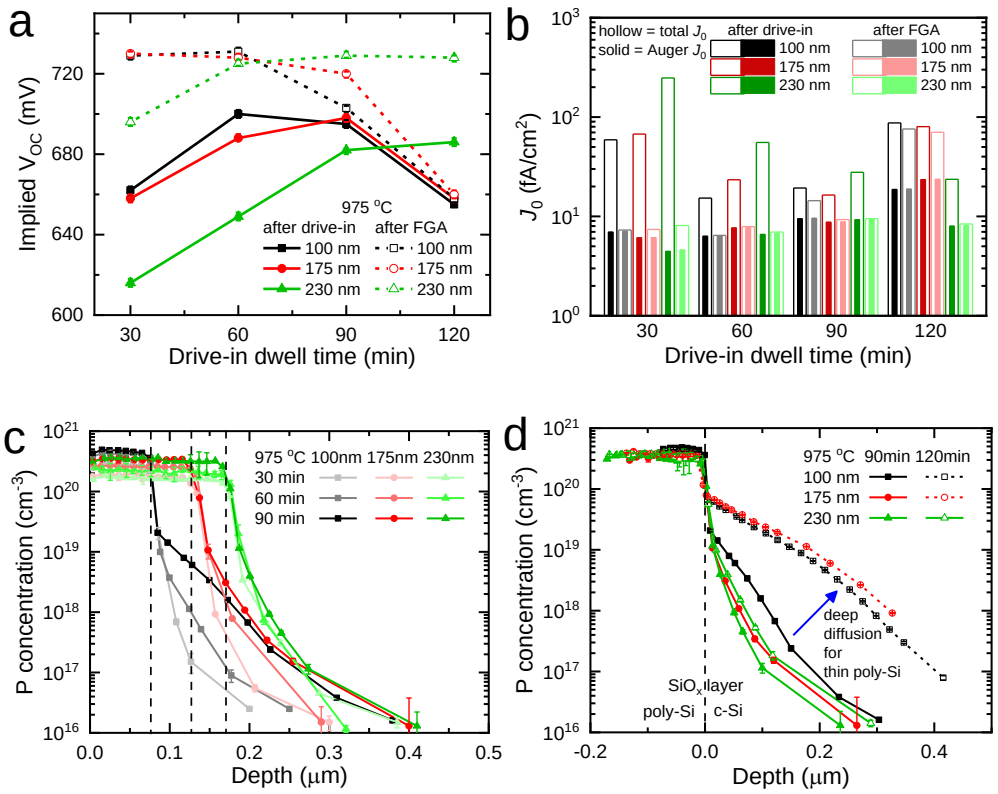


Figure 5.6 PL images of the P-doped poly-Si passivating contact samples (a) after Al metallization and (b) without Al metallization. The anneal setting for the samples presented here was 975 °C for 60 min. The PL settings were same to figure 5.3, *i.e.*, under 0.875 suns for 0.5 s.

5.5 Impacts of drive-in dwell time on passivation and electrical property



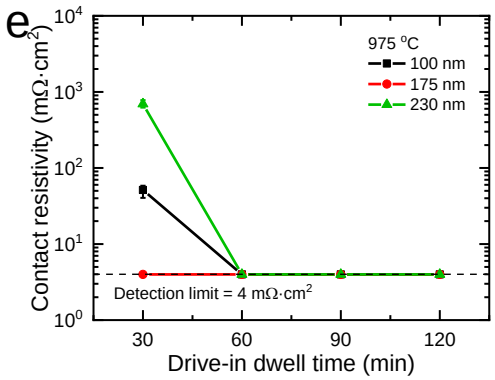


Figure 5.7 (a) iV_{OC} values of P-doped samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) annealed at 975 °C for different durations (filled symbols, solid lines) and after FGA (open symbols, dashed lines); (b) measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for the three poly-Si thicknesses before and after FGA; the corresponding doping profiles of 100, 175 and 230 nm poly-Si samples annealed at 975 °C for (c) 30 – 90 min and (d) 90 – 120 min. The dashed lines indicate the positions of the SiO_x interlayers; (e) the corresponding values of contact resistivity after FGA.

After exploring the influence of drive-in temperature, the impact of drive-in dwell time was studied at a temperature of 975 °C. The other processes remain same as in section 5.4. Figure 5.7a displays the iV_{OC} values for 100 nm (black), 175 nm (red) and 230 nm (green) poly-Si as a function of drive-in dwell time, before (filled symbols, solid lines) and after FGA (open symbols, dashed lines). Similar to the case of drive-in temperature, the iV_{OC} values for all poly-Si thicknesses before FGA increase with a longer drive-in time, reaching a maximum, and then turn to decrease for excessive drive-in. Thicker poly-Si requires longer optimal dwell time. The highest iV_{OC} for 100 and 175 nm poly-Si is obtained for 60 min and 90 min drive-in, respectively. But for 230 nm poly-Si, the iV_{OC} increases with longer drive-in time and still does not show maximum after 120 min drive-in. After FGA, the passivation quality displays different dependences on drive-in time for various poly-Si thicknesses. For thin poly-Si (*i.e.*, 100 and 175 nm), iV_{OC} decreases with longer dwell time, whereas thick poly-Si (230 nm) sample exhibits an increasing trend. High iV_{OC} values above 730 mV are observed for all three poly-Si thicknesses after 60 min drive-in followed by FGA. These iV_{OC} values are higher than reported P spin-on doped poly-Si contact [88], but are still slightly lower than those for $POCl_3$ diffusion [228] or P implantation [123].

Figure 5.7 c – d present the doping profiles for the three poly-Si thicknesses for varied drive-in dwell time. With longer dwell time, the doping level in poly-Si increases and the dopant in-diffusion into c-Si becomes deeper, which is more pronounced for thinner poly-Si. These trends are similar

to the case of higher drive-in temperature, as shown in figure 5.5 c – d. Before reaching optimal doping levels, higher doping concentration in the poly-Si forms larger difference in work functions between poly-Si and c-Si, leading to a higher band bending near the SiO_x/c-Si interface [73]. At the same time, a deeper dopant in-diffusion presumably forms a stronger built-in electrical field [3], which shields more minority carriers from reaching the SiO_x/c-Si interface, thus reducing carrier recombination. Besides, a longer annealing time may allow more Si-O bonds to be rearranged, producing fewer recombination centres [97]. The interface defect state density can be quantitively measured by capacitance-voltage (C-V) analysis with mercury probe systems and deserves more investigation in the future. The shorter optimal dwell time for thinner poly-Si may be ascribed to larger increase in doping levels in poly-Si and c-Si. Figure 5.7b demonstrates the J_0 analysis of measured total recombination and the simulated Auger recombination for the three poly-Si thicknesses for 30 – 120 min drive-in. The $J_{0,total}$ values decrease with longer drive-in time until reaching their minimums. This means total carrier recombination decrease may be induced by higher band bending, deeper profile tail, and lower D_{it}, which may explain iV_{OC} increase after longer drive-in process. In addition, as mentioned in the previous subsection, a thicker poly-Si layer slows down dopant in-diffusion, therefore a longer drive-in time is required to obtain optimum iV_{OC} [95, 229]. It can also be observed that, after a relatively short dwell time drive-in, such as 30 min, $J_{0,total}$ is relatively high, but can be reduced considerably by FGA. This means interface recombination is dominating and defects near SiO_x/c-Si interface can be passivated efficiently by FGA.

However, as shown in figure 5.7 c – d, longer drive-in time results in deeper doping profile in c-Si, thus heavier Auger recombination. This trend is evidenced by increased $J_{0,Auger}$ shown in figure 5.7b. At the same time, the decrease in $J_{0,total}$ caused by FGA also shrinks with longer dwell time. These results indicate that, for a relatively long drive-in time, Auger recombination may take a major role in total carrier recombination. Additionally, the SiO_x interlayer may by seriously damaged by massive dopant in-diffusion during annealing, as described in literature by SEM images of defect-rich SiO_x interlayer in ref. [104]. For example, the iV_{OC} values for 100 and 175 nm poly-Si both exhibit decreasing trends for excessively long drive-in time, down to ~660 mV for 120 min. Figure 5.7d shows that the dopant in-diffusions for 100 and 175 nm poly-Si increase strongly from 90 min to 120 min drive-in, which could be responsible for the notably higher $J_{0,total}$ and $J_{0,Auger}$ for 100 and

175 nm poly-Si after 120 min drive-in than the case for 90 min drive-in. Also, $J_{0,total}$ for 100 and 175 nm poly-Si shows tiny drop after FGA, suggesting that SiO_x interlayers may have been heavily distorted. Therefore, the low iV_{OC} after excessive drive-in may be the consequence of heavy Auger recombination [230] and high interface recombination [75, 227].

Figure 5.7e presents the corresponding contact resistivity of samples shown in figure 5.7a. The values of contact resistivity of 100 and 230 nm poly-Si samples decrease from ~50 and ~700 mΩ·cm^2 respectively for 30 min drive-in to below the detection limit of ~4.0 mΩ·cm^2 for 60 min drive-in. The contact resistivity of 175 nm poly-Si sample remains below the detection limit for all tested dwell times. With a longer drive-in, more dopants are diffused into poly-Si and c-Si substrate, which could decrease the resistivity towards majority carriers. Besides, the strong dopant in-diffusion for 100 and 175 nm poly-Si indicates that possibly considerable break-up in SiO_x interlayer appears, which is beneficial to carrier transportation [74].

In section 5.4 and 5.5 above, the dependences of passivation and contact resistivity of P-doped poly-Si contacts over drive-in temperature, dwell time and poly-Si thickness are discussed. Another key property of poly-Si contact is the short-circuit current density loss resulted from parasitic absorption towards incident photons, especially when place at the front side of a solar cell [231]. According to the fact that poly-Si passivating contacts are commonly used on rear side of solar cells, the characterization of optical behaviours of the spin-on doped samples were beyond the scope of this work. However, there have been many studies on the optical property of n-type poly-Si films. Feldmann *et al*. and Padhamnath *et al*. both hold the view that higher doping level or thickness of poly-Si will lead to stronger free carrier absorption, forming more loss in short circuit current density [126, 229, 232]. Specifically, a 200 nm poly-Si with ~4×10^{20} cm^{-3} dopant concentration shows a near infra-red (NIR) loss of 2.49 mA/cm^2 [233]. Therefore, the NIR losses of the 100 and 175 nm poly-Si spin-on doped poly-Si samples in section 5.4 and 5.5 are assumed to be lower than this value, while the 230 nm poly-Si samples may show similar optical losses as in Ref. [233] due to the similar doping levels and poly-Si thickness.

5.6 Summary

In this chapter, we explored the ability of phosphorus spin-on doping on fabricating poly-Si passivating contacts based on n-type industrial wafers, and investigated the impacts of spin coating, hard baking, drive-in temperature, drive-in dwell time, as well as deposited Si thickness on the quality of poly-Si passivating contacts. We found that:

- Though higher spin speed or spin acceleration during spin coating leads to thinner Spin-on Glass films, the eventual implied open-circuit voltages after FGA are only slightly affected.
- A uniform passivation across 4 inch^2 wafer is achieved for a wide range of spin speed or spin acceleration.
- Prolonged 200 °C baking time improves iV_{OC} both before and after FGA, and reduces sheet resistance notably.
- After drive-in, the sample with thicker deposited Si film (*e.g.*, 230 nm) requires higher optimal drive-in temperature and longer optimal drive-in time.
- After FGA, optimal drive-in temperature for all three poly-Si thicknesses is 975 °C, but thicker deposited Si still calls for longer optimal drive-in time.
- From the ECV profiles and J_0 analysis of both drive-in temperature and dwell time, it is found that the passivation quality depends strongly on the amount of dopants in the poly-Si layer, the c-Si region below the SiO_x interlayer, as well as damage content of SiO_x interlayer.
- After optimization, high iV_{OC} ~730 mV together with low contact resistivity below 4 mΩ·cm^2 were obtained after 975 °C-60 min drive-in followed by FGA. This shows the potential of P spin-on doping as a promising substitution to conventional $POCl_3$ diffusion process.

VI Utilization of boron spin-on doping to form p-type poly-Si passivating contacts

In this chapter, B spin-on doping was employed to form p-type poly-Si passivating contacts on industrial processed symmetrical a-Si/SiO_x/c-Si/SiO_x/a-Si samples. The influences of some specific steps of spin-on doping, *i.e.*, spin coating, 200 °C baking, and drive-in process, were studied for poly-Si contacts with different deposited silicon thicknesses.

6.1 p-type regions on n-type wafer via B spin-on doping

To check the ability of B spin-on doping on forming emitters, the B-containing spin-on dopant solution was applied on n-type wafers directly. The wafers were (100)-orientated, 100 Ω·cm Cz wafers. We firstly used TMAH solution to remove the saw damages on wafer surface. Without an RCA cleaning, these wafers were coated by the Spin-on Glass (SOG) solution, B-1500 ([B] 7.2×10^{21} cm^{-3}), using spin coating process. Similar to section 5.1, the RCA cleaning was skipped as here we focused on doping profiles and sheet resistance on which an RCA cleaning has little impact. The SOG solution was also employed in following sections. During spin coating process, the spin speed, spin acceleration, spin time, and solution volume were 3000 rpm, 1000 r/s^2, 30 s, and 100 μL, respectively. The SOG films were formed after the hard baking at 200 °C for 6 min. Afterwards, these samples were subjected into 60 min drive-in process at temperature from 800 to 1000 °C, followed by an HF dip to remove SOG films. At last, we used Sinton WCT-120 lifetime tester [190], 4-point probe method, and ECV profiler WEP CVP21 to measure the iV_{OC}, R_{sh}, and doping profiles. The iV_{OC} and R_{sh} are indicated as function of drive-in temperature, as shown in figure 6.1.

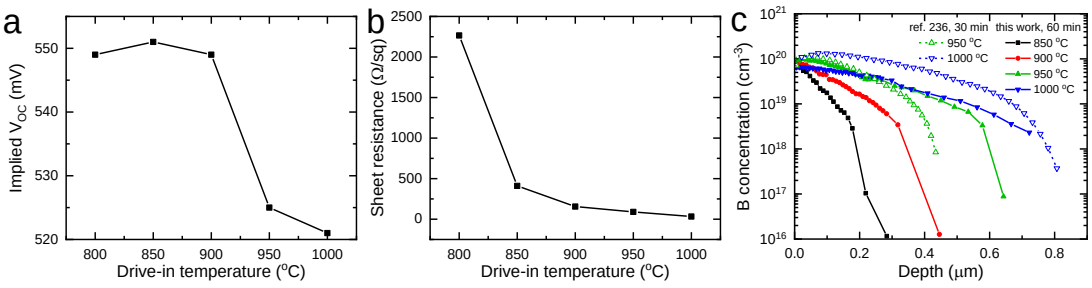


Figure 6.1 The impacts of drive-in temperature on (a) implied open-circuit voltage, (b) sheet resistance, and (c) doping profile for B spin-on doping on n-type wafers.

From figure 6.1 we can find that the iV_{OC}s for all samples remain consistently low with a range of 520 – 550 mV for drive-in temperature of 800 – 1000 °C. Similar to P-doped samples, the R_{sh} decreases remarkably from 2250 Ω/sq at 800 °C down to 500 Ω/sq at 850 °C, and then decreases slowly, keeping below 250 Ω/sq for temperature above 900 °C. According to these results, 900 °C may be the suitable drive-in temperature for B-1500 dopant to dope wafer directly. However, the typical temperature of BBr_3 diffusion used for doping wafers is higher than 900 °C [234], even over 1000 °C [235]. Figure 6.1c displays the active dopant concentration distribution for 850 – 1000 °C drive-in. Compared to doping profiles after BBr_3 diffusion in ref. [236], as overlayed in figure 6.1c, our 950 °C profile shows similar active dopant concentration near wafer surface, but a bit deeper profile in wafer bulk. However, after 1000 °C diffusion, the doping profile in this work has similar depth in wafer but lower doping level compared to the BBr_3 diffused profile [236]. This comparison means B spin-on doping has opportunity to produce similar doping level and profile as conventional BBr_3 diffusion does. The differences in the profiles may be explained by the different annealing dwell times and differences in ramping up and down speed.

6.2 Impacts of spin coating process on passivation quality of poly-Si passivating contacts

In this section, we explored how the passivation quality on passivating contacts, indicated as iV_{OC}, changes with varying spin coating parameters, including spin speed, spin time, spin acceleration, and spin-on solution volume. The substrates have symmetric structure of a-Si/SiO_x/c-Si/SiO_x/a-Si that contain < 2 nm silicon oxide interlayers [75, 120, 189] and intrinsic amorphous silicon films [79, 92, 111]. More details of fabrication can be found in chapter 4. Via a focused ellipsometer (J.A. Woollam ESM-300) in ANFF, the thicknesses of deposited intrinsic a-Si films were measured to be 100, 175, and 230 nm. In this thesis, we use black colour, red colour, and green colour to show 100, 175, and 230 nm intrinsic Si films, respectively. These sandwich-like substrates were also used in the following sections. Before spin coating process, these symmetric substrates were cleaned with RCA solutions. The consumption of a-Si thickness during RCA cleaning is likely to be negligible compared to the thickness of the whole a-Si layer. In spin coating process, the spin-on solution was SOG B-1500, and the ranges of spin speed, spin time, spin acceleration, and solution volume were set as 1000 – 5000 rpm, 5 – 60 s, 250 – 2000 r/s^2, and 25 – 200 μL, respectively. After spin coating,

room temperature venting and hard baking process, the solid SOG films were achieved on both sides of the wafers. The SOG film thicknesses were also measured by the focused ellipsometer in ANFF, as shown in figure 6.2 a – d. Afterwards, the samples were subjected to high temperature annealing at 950 °C for 60 min in N_2 for dopant in-diffusion and activation. During this thermal treatment, a-Si is transformed to poly-Si phase. Following an HF dip and an FGA process at 400 °C for 30 min, the iV_{OC} values and uniformity were obtained using Sinton WCT-120 lifetime tester [190] and photoluminescence (PL) imaging, respectively. The results are demonstrated in figure 6.2 e – f and figure 6.3, respectively.

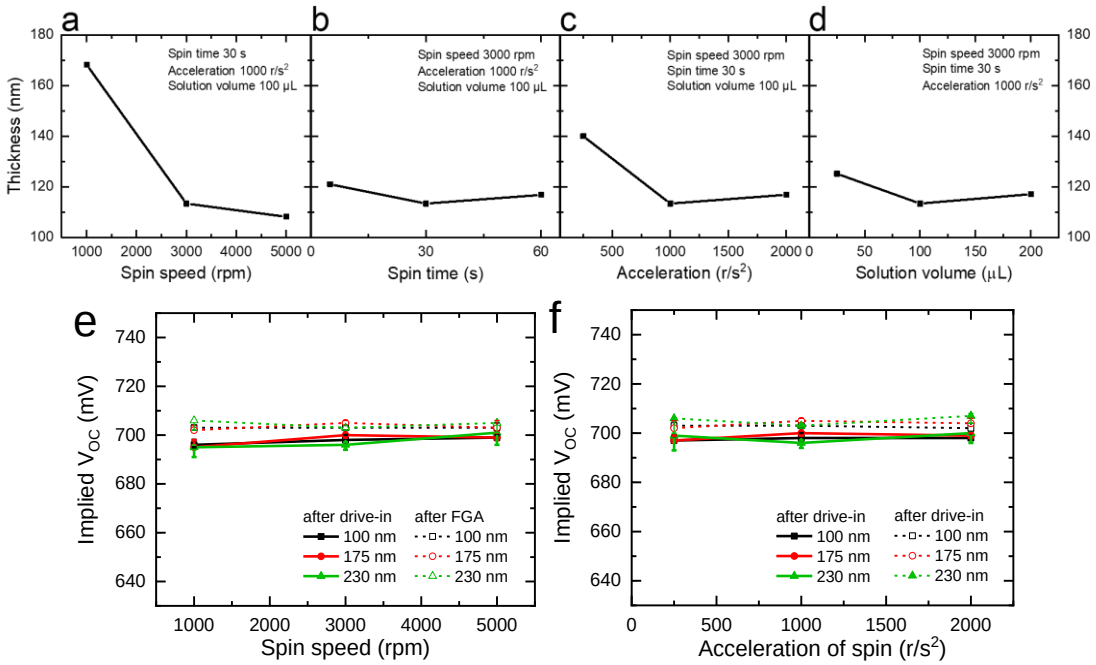


Figure 6.2 The correlation of boron-containing SOG thickness with (a) spin speed, (b) spin time, (c) spin acceleration, and (d) solution volume; the impacts of (e) spin speed and (f) spin acceleration on iV_{OC} values for 100 nm (black), 175 nm (red) and 230 nm (green) poly-Si, after 950 °C-60 min drive-in process (filled symbols, solid lines) and FGA process (open symbols, dashed lines).

Similar to the case of P Spin-on Glass, the spin speed and spin acceleration show stronger influences on the thickness of B Spin-on Glass film than spin time or solution volume. The film thickness decreases significantly as increasing the spin speed. Different spin acceleration leads to minor thickness variations. However, the SOG film thickness for varied spin time and solution volume just changes within 10 – 15 nm. The spin coating parameters of 3000 rpm, 30 s, 1000 r/s^2, and 100 µL lead to ~115 nm thick B SOG films.

From figure 6.2 e – f, it can be found that for three poly-Si thicknesses, the varied spin speed and spin acceleration result only in minor changes in iV_{OC} both before and after FGA. The largest iV_{OC} increase, 5 mV, is observed for 230 nm poly-Si before FGA, when spin speed increases from 1000 rpm to 5000 rpm. The highest iV_{OC} ~706 mV is obtained from the 230 nm poly-Si sample under 1000 rpm spin speed (with spin time 30 s, acceleration 1000 r/s^2, and solution volume 100 µL), or under 2000 r/s^2 spin acceleration (with spin speed 3000 rpm, spin time 30 s, together with solution volume 100 µL).

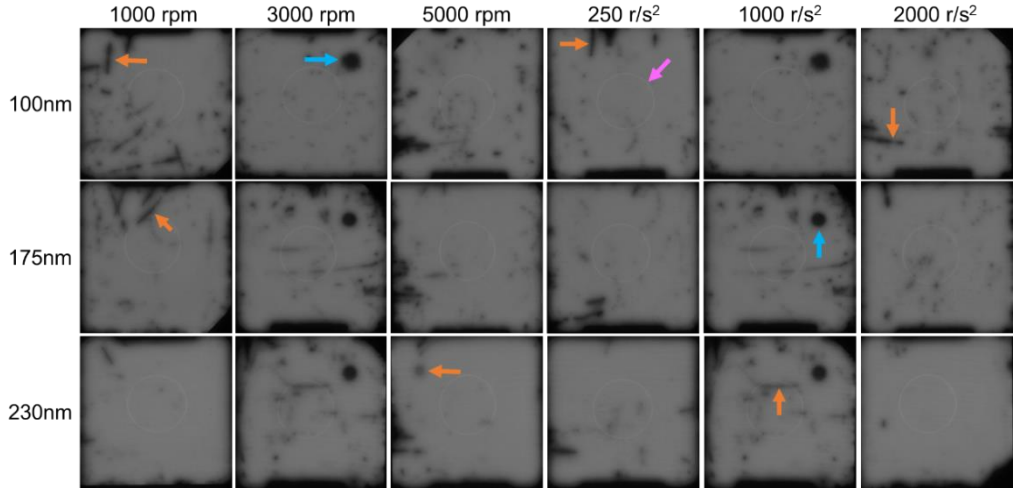


Figure 6.3 The PL images of p-type poly-Si passivating contact samples coated with various spin speeds and different spin accelerations. The left 100, 175, and 230 nm indicate the poly-Si thickness. The exposure time was 0.5 s, and illumination intensity was 0.875 suns for all the samples.

Figure 6.3 exhibits the PL images of samples with three poly-Si thicknesses, coated using different spin speeds and accelerations. The samples were 4 inch^2 squares. The big round black spots at top right corner (blue arrow) are ascribed to dopant profiling etched defects. The damages and contaminations during fabrication may be responsible for the other small round or bar-like spots in images (orange arrow). Additionally, the large white circles in the centre (pink arrow) result from the inductance coil in chuck. The images confirm the results from lifetime measurements (figure 6.2) with a similar PL intensity among samples, meaning that different spin speeds and accelerations have small impacts on passivation. Besides, the PL intensity within each sample is uniform, indicating that B spin-on doping is able to form uniform passivation for poly-Si passivating contacts. These findings mean that, for SOG B-1500 solution, different settings of spin coating process yield only little influence on passivation quality, and uniform passivation can be achieved on substrates under a specific spin coating setting.

6.3 The passivation quality as a function of hard baking time

The hard baking at 200 °C shows some positive effects on improving passivation quality [221-224]: it is able to evaporate solvent and organic additions in as-spun SOG films, densifying SOG films and reducing carbon contamination during dopant in-diffusion. Therefore, in this section we extended hard baking time from 3 min to 12 min. The substrates were also sandwich-like a-Si/SiO_x/c-Si/SiO_x/a-Si stacks, with an intrinsic a-Si thickness of 175 nm. The spin-on solution B-1500 was applied on both sides of substrates using the spin coating setting of 3000 rpm-15 s-1000 r/s^2-100 µL. After drying at room temperature and soft baking at 90 °C, the samples were hard baked. Then the samples were subjected to drive-in process at 950 °C for 60 min, followed by HF dip and iV_{OC} measurement. Then, the FGA was performed before the measurements of sheet resistance and doping profiles, as well as another iV_{OC} measurement. Figure 6.4 displays the results.

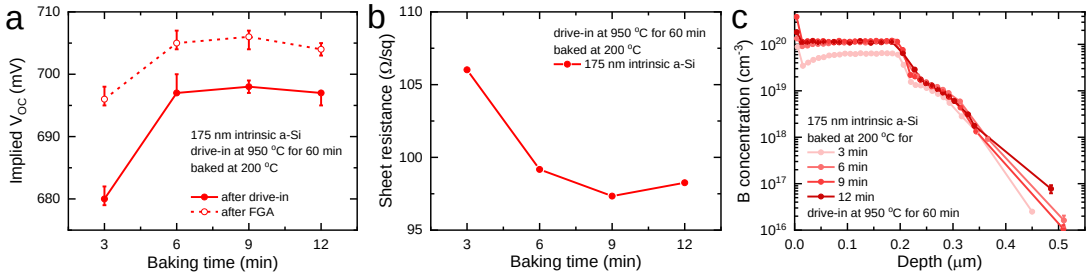
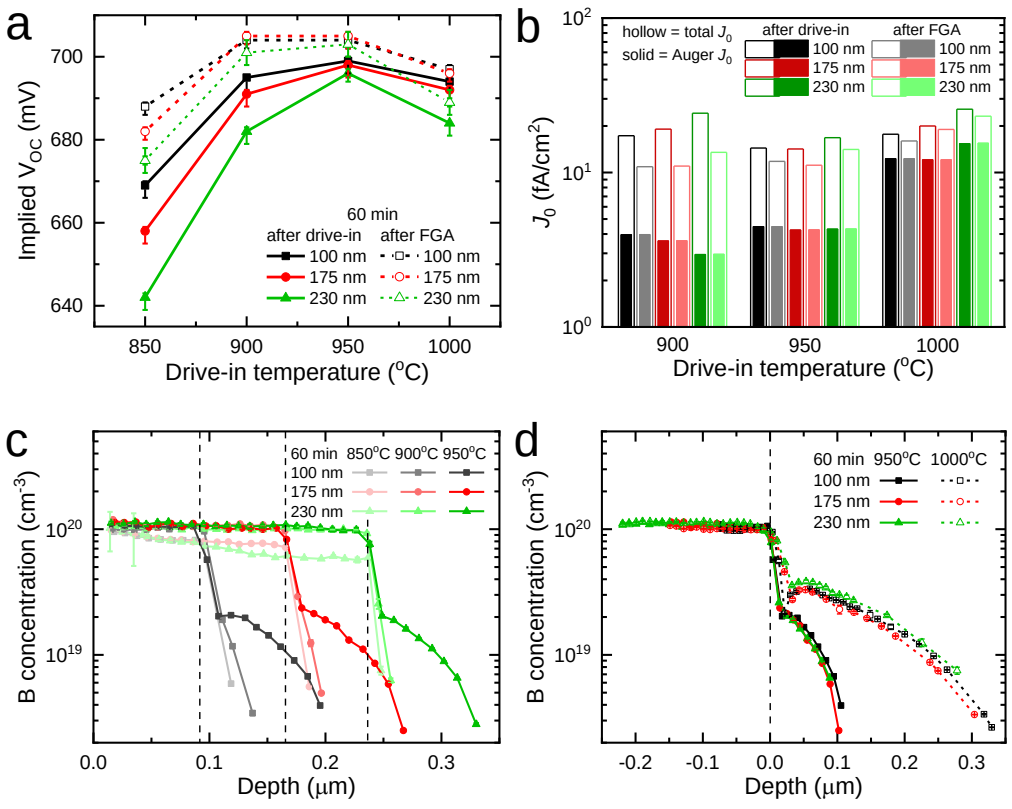


Figure 6.4 The dependence of (a) iV_{OC} before and after FGA, (b) sheet resistance, and (c) doping profiles on various hard baking dwell times for 175 nm poly-Si samples for B spin-on doping.

As figure 6.4a shows, when hard baking time increases from 3 min to 9 min, higher iV_{OC} values are observed both before and after FGA, showing highest iV_{OC} ~706 mV after 9 min baking and FGA. On another hand, R_{sh} decreases with longer baking time, reaching minimum ~97.5 Ω/sq for 9 min baking, as figure 6.4b shows. Assisted by doping profiles in figure 6.4c, it can be found that a hard baking with longer time drives more dopants into poly-Si and c-Si, forming higher doping level in poly-Si and deeper doping profile in c-Si. This may support the positive effects of hard baking as mentioned above [221-224], though we do not have direct evidence for contaminants evaporation and spin-on film densification. The iV_{OC} decrease for 12 min baking may be ascribed to the slightly higher R_{sh}. It can be concluded from the results that 9 min may be the optimal hard baking time for this SOG B-1500 to produce high iV_{OC} together with low sheet resistance.

6.4 Impacts of drive-in temperature on poly-Si passivating contact quality

Based on results of preliminary sections, we investigated the impacts of drive-in temperature on poly-Si passivating contact quality. The drive-in process controls poly-Si crystallinity, dopant in-diffusion from SOG to poly-Si film and c-Si wafer, and the silicon oxide interlayer damage. The major process flow was similar to that in section 6.3, except that the a-Si (or poly-Si) films with thicknesses of 100 (black), 175 (red), and 230 (green) nm were involved. Besides, the spin time was set to 30 s, and the baking time at 200 °C was 3 min. Afterwards, the as-coated samples were thermally treated in N_2 using a quartz tube furnace to drive-in and activate the dopants at various temperatures between 850 °C to 1000 °C. The drive-in dwell time was set as 60 min. Then the boron-silica glasses were removed in 3% HF solution. Finally, the samples were hydrogenated using forming gas annealing (FGA, 5% H_2, 95% Ar) at 400 °C for 30 min. The details of characterizations and measurements involved here have been described in section 4.1.



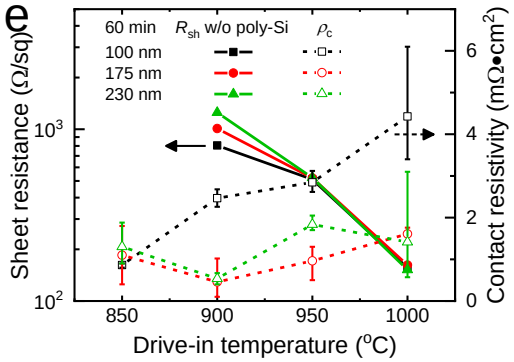


Figure 6.5 (a) iV_{OC} values of B-doped samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) annealed for 60 min at different temperatures (filled symbols, solid lines) and after FGA (open symbols, dashed lines); (b) measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for 900 – 1000 °C annealing and three poly-Si thicknesses before and after FGA; the corresponding doping profiles for annealing at (c) 850 – 950 °C and (d) 950 – 1000 °C. The dashed lines indicate the position of the SiO_x interlayers; (e) the corresponding values of sheet resistance without poly-Si layers and contact resistivity containing poly-Si layers after FGA. The contact resistivity was measured by Thien N. Truong [237].

Figure 6.5a shows the dependences of implied V_{OC} for 100 (black), 175 (red) and 230 (green) nm poly-Si layers on drive-in temperature before and after FGA. Before FGA, the iV_{OC} values for three poly-Si thicknesses first increase and then decrease as the drive-in temperature increases, reaching their maximum at 950 °C. The highest iV_{OC} is 699 mV for 100 nm poly-Si sample. Similar iV_{OC} trends are observed after FGA. The iV_{OC} values increase with higher drive-in temperature and keep a plateau of 701 – 705 mV between 900 °C and 950 °C, and then decrease at higher temperature. For both, before and after FGA, the sample with thicker poly-Si layer shows lower iV_{OC} than thinner poly-Si thicknesses.

The active doping concentration in poly-Si and in c-Si below SiO_x interlayer, together with the defect level density at SiO_x/c-Si interface affect the iV_{OC}. Figure 6.5c presents the changes in ECV doping profiles for three poly-Si thicknesses when temperature increases from 850 °C to 950 °C. These doping profiles show that a higher drive-in temperature leads to higher doping levels in both poly-Si and c-Si regions. As a result, a higher band-bending [73] is achieved near SiO_x/c-Si interface, and a stronger built-in electrical field [3] is formed in c-Si below SiO_x. These two factors both contribute to resist minority carriers from reaching the defect-rich SiO_x/c-Si interface. On another hand, a higher drive-in temperature may enhance the bond rearrangement at SiO_x/c-Si interface, which reduces the density of interface defect states (D_{it}) and recombination centres [238]. All these factors contribute to improve passivation quality. Furthermore, it can be found that the improvement

in iV_{OC} with higher drive-in temperature is stronger for thicker poly-Si compared to thinner poly-Si, which has also been observed by Padhamnath *et al*. [229]. Figure 6.5b demonstrates the comparison of total recombination current density ($J_{0,total}$) and Auger recombination current density ($J_{0,Auger}$) for 900 – 1000 °C. The increased temperature from 900 °C to 950 °C leads to lower $J_{0,total}$, which can be explained by the lower interface recombination based on reduced minority carrier concentration at the interface and less recombination centres. For 900 °C drive-in, $J_{0,Auger}$ is relatively low but $J_{0,total}$ is high, implying a dominating interface recombination. FGA results in considerable $J_{0,total}$ decrease, which means defects near SiO_x/c-Si interface can be passivated effectively by hydrogen in forming gas annealing.

However, for 1000 °C drive-in, the iV_{OC} values for three poly-Si thicknesses decrease remarkably. As shown by doping profiles in figure 6.5d, at 1000 °C a large amount of B dopants is diffused into c-Si. This suggests a high Auger recombination contribution and SiO_x interlayer may be damaged [239]. The defects formed on SiO_x interlayer after a similar process has been observed in SEM images after using TMAH to selectively etch away poly-Si to make pinholes visible [104], which may support our reasoning. Figure 6.5b shows that, at 1000 °C the simulated Auger contribution for all three poly-Si thicknesses becomes the dominating factor in $J_{0,total}$. At the same time, the heavy interface recombination is widely regarded as another cause of iV_{OC} decrease [120, 227]. As figure 6.5b shows, FGA leads to minor decrease of $J_{0,total}$, which may suggest a stronger damage on SiO_x interlayer with increased dwell temperature [74, 126]. The damage may be related to dopant in-diffusion [74, 240] and charged B dopants accumulated at SiO_x/c-Si interface [240]. Therefore, the Auger recombination together with distortion on the SiO_x interlayer may be the main drivers for the reduced passivation quality at excessively high temperature. At 1000 °C, the B diffusivity may be high enough to overcome the impediment effect from poly-Si [230], forming similar doping levels in poly-Si for three poly-Si thicknesses. In c-Si region below SiO_x, similar profile tails were obtained, with a slightly higher profile for 230 nm poly-Si. Corresponding to this, both the $J_{0,total}$ and $J_{0,Auger}$ for 230 nm poly-Si are slightly higher than for the 100 and 175 nm poly-Si, resulting in ~10 mV iV_{OC} drop.

Generally, the iV_{OC} increase induced by FGA is more significant for lower drive-in temperature or thicker poly-Si layer. For a specific poly-Si thickness, a higher drive-in temperature may form more

destruction on SiO_x interlayer and drive more dopants into c-Si [74, 126], limiting the room of iV_{OC} improvement after FGA. For example, the iV_{OC} increase for 230 nm poly-Si corresponding to 850 °C drive-in is ~33 mV, which is much larger than that of ~5 mV for 1000 °C drive-in. On another hand, for a specific drive-in temperature below 950 °C, a thicker poly-Si layer may exhibit a somewhat stronger impediment effect on boron in-diffusion [120]. This makes the SiO_x interlayer less damaged thus the H passivation more effective. For instance, for 900 °C drive-in, the iV_{OC} ramping range for 230 nm poly-Si is about 20 mV, which is almost double of that for 100 nm poly-Si. The possible reasoning may be evidenced by the ECV doping profiles displayed in figure 6.5c and d, as well as the impact from accumulated active dopants near SiO_x/c-Si [75, 225] which is not presented here.

Figure 6.5e displays the sheet resistances and contact resistivity values for three poly-Si thicknesses for drive-in temperature of 850 – 1000 °C. The sheet resistance was calculated using the doping profile without the poly-Si part as input in the software EDNA2 [194], while the contact resistivity was measured from samples containing the poly-Si layer. A decreasing trend in R_{sh} with higher drive-in temperature is observed for all three poly-Si thicknesses. For 850 °C drive-in, the diffusion into the c-Si below the SiOx was too weak to calculate a meaningful R_{sh} using EDNA2. For 950 °C drive-in, the sheet resistances are around 520 Ω/sq, and reach lowest values around 155 Ω/sq at 1000 °C. No clear trend is observed for the contact resistivity values for the three poly-Si thicknesses but all are below 5 mΩ·cm^2. More details about metallized samples preparation and measurement can be found in ref. [237].

6.5 Impacts of drive-in dwell time on poly-Si passivating contact

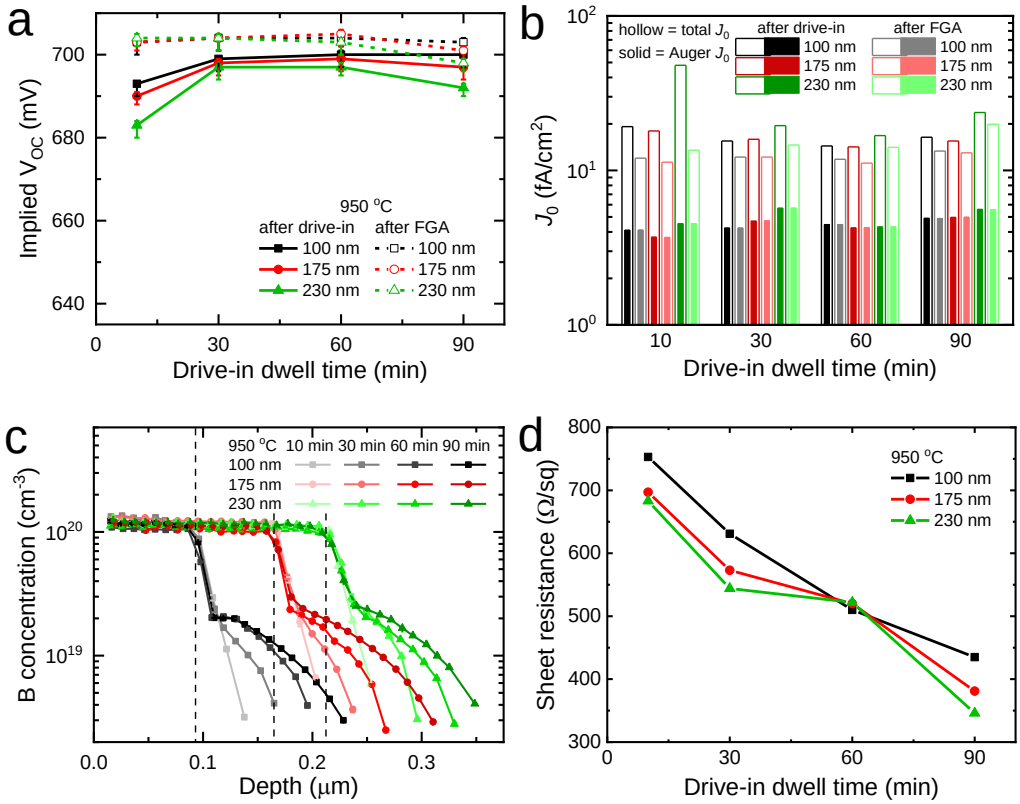


Figure 6.6 (a) iV_{OC} values of B-doped samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) annealed at 950 °C for different durations (filled symbols, solid lines) and after FGA (open symbols, dashed lines); (b) measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for 10 – 90 min drive-in and three poly-Si thicknesses before and after FGA; (c) the corresponding doping profiles for annealing at 950 °C for 10 – 90 min. The dashed lines indicate the positions of the SiO_x interlayers; (d) the corresponding values of sheet resistance without poly-Si layers after FGA.

Figure 6.6a displays the impacts of drive-in dwell time at 950 °C on iV_{OC} values for 100 (black), 175 (red) and 230 (green) nm poly-Si before and after FGA. The Spin-on Glass, spin coating, and baking process were same as in section 6.4. Compared to drive-in temperature, drive-in dwell time provides less influence on iV_{OC}, producing a change in iV_{OC} values in the range of ~20 mV before FGA and less than 10 mV after FGA. Before FGA, the iV_{OC} values for three poly-Si thicknesses increase with longer drive-in time and then decrease at long drive-in time. The highest iV_{OC} of ~699 mV is obtained for 100 nm poly-Si after 60 – 90 min drive-in. After FGA, the iV_{OC} for three poly-Si thicknesses all remain almost stable at ~705 mV for 10 – 60 min drive-in. However, low iV_{OC} values were observed for long annealing time. Again, the thicker poly-Si leads to larger changes in iV_{OC} under extended drive-in. The highest iV_{OC} obtained here is to our knowledge the highest so far

reported for B spin-on doped poly-Si contact [88], but there is still room for improvement in comparison with BBr_3-diffused [241] or B-implanted [238] samples.

It can be seen from figure 6.6c that the drive-in dwell time at 950 °C shows less impact on B in-diffusion compared to drive-in temperature. A longer drive-in will diffuse more dopants into c-Si, but changes the doping level in poly-Si only slightly. The more diffused dopants for longer drive-in may lead to stronger built-in electrical field [3], which contributes to reduce the minority carrier concentration near SiO_x/c-Si interface. Besides, an extended drive-in process may offer more time to perform rearrangement of SiO_x/c-Si interface bonds to reduce interface state density (D_{it}) [238]. The lower D_{it} may be evidenced by capacitance-voltage (C-V) analysis in the future [97]. These two aspects may explain the iV_{OC} increase for dwell times of 10 – 30 min. The J_0 analysis in figure 6.6b shows considerable decrease in $J_{0,total}$ but tiny increase in $J_{0,Auger}$ increasing the drive-in from 10 to 30 min. This suggests that even though dopant in-diffusion is higher, the contribution from Auger recombination is still relatively weak, and interface recombination remains as major part in total recombination. In addition, when drive-in time is extended from 10 min to 30 min, a larger iV_{OC} increase is observed for thicker poly-Si. This may be explained by the slightly stronger dopant in-diffusion for 230 nm poly-Si compared to 100 nm poly-Si after 30 min drive-in, which is supported by the slightly larger change in R_{sh} for 230 nm poly-Si.

Though not remarkable, the descending trend in iV_{OC} is attained for excessively prolonged drive-in dwell time. As shown in figure 6.6c, the drive-in process for more than 30 min keeps diffusing more dopants into c-Si, forming deeper doping profiles in c-Si for three poly-Si thicknesses. When the optimal doping profiles in c-Si are surpassed, the Auger and interface recombination may overwhelm the positive effects of built-in field and interface bond rearrangement [74], leading to lower iV_{OC}. Some evidence can be found from the increased $J_{0,Auger}$ contribution to the measured $J_{0,total}$ values as plotted in figure 6.6b.. Furthermore, similar to the case of high drive-in temperature, a thicker poly-Si layer yields a larger iV_{OC} decrease for long drive-in time. After 90 min drive-in, iV_{OC} for 230 nm poly-Si is ~8 mV lower than that for 100 nm poly-Si. This may be a result of the slightly higher Auger recombination, or the higher D_{it} at SiO_x/c-Si interface due to more accumulated inactive boron dopants. The latter phenomenon has been observed by SIMS data in ref. [230, 242, 243].

The iV_{OC} increase induced by FGA can be influenced by both drive-in dwell time and poly-Si thickness. Similar to the impact of a higher drive-in temperature on hydrogenation, for a specific poly-Si thickness, a longer drive-in will damage the SiO_x interlayer more heavily and form deeper doping profile, thus lead to less response to H passivation [126]. For example, for 230 nm poly-Si, FGA results in ~20 mV iV_{OC} increase for 10 min drive-in, but only ~6 mV increase for 90 min drive-in. As plotted in figure 6.6b, the high $J_{0,total}$ after 10 min drive-in and notable $J_{0,total}$ decrease after FGA indicate the weakly damaged SiO_x interlayers. However, the $J_{0,total}$ after 90 min drive-in is high and $J_{0,total}$ decrease after FGA is less, which suggests SiO_x interlayers have been more distorted and Auger recombination becomes slightly higher.

Figure 6.6d displays the sheet resistances for drive-in dwell time of 10 – 90 min. As in the case in section 6.4, the R_{sh} values were simulated in EDNA2 [194] using the doping profiles below SiO_x interlayers. Like the case of higher drive-in temperature, the sheet resistances for three poly-Si thicknesses decrease with increasing anneal time. The lowest R_{sh} of ~350 Ω/sq belongs to 230 nm poly-Si sample for 90 min drive-in. R_{sh}s for 30 min drive-in and three poly-Si thicknesses locate within 540 – 640 Ω/sq.

The section 6.4 and 6.5 demonstrate the correlations of passivation and electrical properties with drive-in temperature, dwell time, as well as poly-Si thickness. Another important characteristic of p-type poly-Si contacts is the parasitic absorption, but this measurement is out of the scope of this thesis and is moved to future work. However, literature points out that highly doped p-type poly-Si results in apparent current density losses, which increases with higher doping level or thicker poly-Si [244, 245]. We assume that p-type spin-on doped poly-Si behaves similar to poly-Si contacts fabricated by other methods in terms of parasitic absorption.

6.6 Summary

In this chapter, we studied the potential of boron spin-on doping to form p-type poly-Si passivating contacts based on industrial wafers and processes. The impacts of spin coating process, hard baking time, drive-in temperature, drive-in dwell time, and intrinsic silicon thickness on passivation quality and electrical property were investigated. We found that:

- The varied spin speed or spin acceleration shows slight influence on iV_{OC} both before and

after FGA.

- A uniform passivation across square 4 inch^2 wafer independently of spin coating parameter is achieved.
- A longer hard baking time leads to higher iV_{OC} both before and after FGA, as well as a lower sheet resistance.
- Before FGA, the increased drive-in thermal budget produces optimal iV_{OC} values at 950 °C temperature for 30 – 60 min dwell time for 100, 175, and 230 nm intrinsic silicon.
- The FGA improves iV_{OC} values for all drive-in thermal budgets and three poly-Si thicknesses. This effect is larger for lower temperature, shorter dwell time, or thicker intrinsic silicon.
- After FGA the highest iV_{OC} is ~705 mV, corresponding to 950 °C temperature and 10 – 60 min dwell time for three intrinsic silicon thicknesses. The contact resistivity for three intrinsic silicon thicknesses all keep below 5 mΩ·cm^2 at 850 – 1000 °C drive-in temperature.
- Higher drive-in temperature or longer dwell time leads to sheet resistance decrease, especially in case of drive-in temperature and for thinner intrinsic silicon. The sheet resistance for thicker intrinsic silicon is lower because R_{sh} samples contain doped poly-Si layers. The lowest sheet resistance around 50 Ω/sq was obtained for 230 nm intrinsic silicon after 1000 °C-60 min drive-in.
- Varied drive-in temperature leads to differences in doping levels in poly-Si and c-Si below SiO_x interlayer, but drive-in dwell time only impacts doping profiles in c-Si.
- The high iV_{OC} from B spin-on doping here indicates that B spin-on doping may be a potential alternative for conventional BBr_3 diffusion.

VII. Conclusion and outlook

7.1 Conclusion

In this thesis, we fabricated n-type and p-type poly-Si passivating contacts using P and B spin-on doping methods on industrial symmetrical a-Si/SiO_x/c-Si/SiO_x/a-Si substrates. We explored the impacts of spin coating processes (*e.g.*, spin speed, spin time, spin acceleration, spin-on dopant solution volume), hard baking time, drive-in annealing (*e.g.*, temperature and dwell time), as well as intrinsic amorphous silicon thickness (*e.g.*, 100, 175, and 230 nm) on performance of poly-Si passivating contacts. The passivation quality is characterized by implied open-circuit voltage, and the electrical property is represented by contact resistivity and sheet resistance.

We found that:

- For both P and B spin-on doping processes, spin speed and acceleration lead to larger difference of spin-on glass film thickness, but only slight change in passivation quality, especially for B spin-on doping.
- For both P and B spin-on doping processes, longer time of 200 °C baking results in a lower sheet resistance and a higher iV_{OC} before and after forming gas annealing. This process shows a stronger influence on P-doped poly-Si passivating contacts than on B-doped cases.
- After high temperature treatments, the P-doped poly-Si contact with thicker deposited silicon film requires higher drive-in temperature or longer dwell time to reach optimized passivation quality. The samples with 100 and 175 nm intrinsic silicon obtain optimal passivation at 975 °C for 60 and 90 min respectively, but 230 nm intrinsic silicon sample gets optimal passivation at 1000 °C for 60 min or at 975 °C for more than 120 min.
- After high temperature treatments, the optimal passivation for B-doped poly-Si contact, independently of the deposited silicon thickness, is achieved after 950 °C drive-in for 30 – 60 min dwell time.
- The influence of forming gas annealing on passivation quality is found to be stronger for P-doped poly-Si compared to B-doped ones. Passivation improvement is more notable for lower drive-in temperature, less dwell time, and thicker deposited silicon film.
- After forming gas annealing, the P-doped sample with 100 nm intrinsic silicon film shows maximal iV_{OC} ~733 mV corresponding to 975 °C-60 min drive-in. The B-doped samples

for all three intrinsic silicon thicknesses show optimal iV_{OC} of ~705 mV after 950 °C drive-in for 10 – 60 min followed by forming gas annealing.

- For P spin-on doping, the values of contact resistivity are less than 4 mΩ·cm^2 for all samples for drive-in at temperature of 975 °C or higher and dwell time of 60 min or longer. For B spin-on doping, the contact resistivity for three deposited silicon thicknesses all keep below 5 mΩ·cm^2 for drive-in temperature between 850 °C and 1000 °C.

These high iV_{OC}s and low contact resistivity values of spin-on doping indicate that the spin-on doping method is a promising alternative approach to conventional gas diffusion doping method to form n-type or p-type poly-Si passivating contacts.

7.2 Outlook

According to the results in this thesis, more work is required:

- The promising results on passivation and electrical transport should be implemented and tested on full proof-of-concept solar cell devices and full-sized industrial cells.
- More effort should be made to investigate the trade-off between passivation and optical absorption.
- The liquid dopant source allows exploring a wide range of other p-type dopant materials, such as Ga and Al, to further push the passivation quality while maintaining low contact resistivity for poly-Si passivating contacts.
- Optimizing and aligning the P and B spin-on doping processes allows to deposit n-type doping on one side and p-type doping on another side, and therefore to fabricate a cell using only one thermal treatment.
- Spin-on dopants may be applied on wafers with different surface morphology, *e.g.*, textured surfaces, to study the trade-off between carrier generation and recombination.
- Spin-on doping may be combined with laser process and/or rapid thermal process to form localized poly-Si passivating contacts and shallow junctions below the ultrathin silicon oxide interlayers.
- Based on the high performance, the focus should be the tolerance of cells via spin-on doping method towards industrial metallization process and long-term operation.

List of publications

The achievements during the MPhil program are listed below:

- Zetao Ding*, Di Yan, Wenhao Chen, Sieu Pheng Phang, Chris Samundsett, Zhao Wang, Jie Yang, Peiting Zheng, Xinyu Zhang, Josua Stuckelberger, Yimao Wan, Daniel Macdonald, "Phosphorus doped poly-Si/SiO_x passivating contact via spin-on doping". Poster presentation in 29th International Photovoltaic Science and Engineering Conference (PVSEC29) in Xi'an China (2019).
- Zetao Ding*, Di Yan, Josua Stuckelberger, Sieu Pheng Phang, Wenhao Chen, Christian Samundsett, Jie Yang, Zhao Wang, Peiting Zheng, Xinyu Zhang, Yimao Wan, Daniel Macdonald, "Phosphorus-doped polycrystalline silicon passivating contacts via spin-on doping", *Solar Energy Materials and Solar Cells*, vol. 221, p. 110902, 2021. doi: 10.1016/j.solmat.2020.110902.
- Zetao Ding, Thien N. Truong*, Hieu T. Nguyen, Di Yan, Jie Yang, Zhao Wang, Peiting Zheng, Xinyu Zhang, Yimao Wan, Daniel Macdonald, Josua Stuckelberger*, "Boron spin-on doping for poly-Si/SiO_x passivating contacts", *ACS Applied Energy Materials*, vol. 4, p. 4993, 2021. doi: 10.1021/acsaem.1c00550.

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