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Enhanced Operation Frequencies of Bipolar Double-Flux-Quantum Amplifiers Fabricated Using 10-kA/cm^2 Nb/AlO$_x$/Nb Integration Process

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We have demonstrated digital-to-analog (D/A) operations using single-flux-quantum (SFQ) pulse-frequency modulation (PFM) D/A converters for future AC voltage standards. In this paper, for improvement of SFQ-PFM D/A converters, we investigated a double-flux-quantum amplifier (DFQA) and a magnetically-coupling SFQ driver/receiver circuit (MC-SFQ-DR) fabricated using a 10-kA/cm^2 Nb/AlO$_x$/Nb integration process. The critical current density J_c of 10-kA/cm^2 was four times larger than that of the integration process we had used. A DFQA and an MC-SFQ-DR included unshunted Josephson junctions, and therefore, it was unclear if the high-J_c process improved their performances. We measured test chips cooled in a liquid helium bath. The maximum input voltages for a +20-fold and a −20-fold DFQA were 147 and 126 μV, for which the corresponding Josephson frequencies were 70.9 and 61.1 GHz. It was confirmed that the operation frequencies of the DFQAs and MC-SFQ-DR were improved by approximately two fold.

1. Introduction

Voltage standards based on the AC Josephson effect are unique applications of superconducting Josephson circuits. In addition to established DC voltage standards, AC voltage standards are under development.[1)-7)] We have been working single-flux-quantum (SFQ) pulse-frequency modulation (PFM) D/A converters,[8)-12)] in which the pulse repetition frequencies are modulated in accordance with the digital input signals, resulting in modulated analog output voltages of quantum accuracy.[2),5)] So far, we succeeded to synthesize voltage waveforms using a 9-bit SFQ PFM D/A converter,[8),9)] in which two main circuit components, a variable SFQ pulse number multiplier (V-PNM) and a double-flux-quantum amplifier (DFQA),[13)-19)] were implemented. For synthesizing a sinusoidal voltage waveform, its maximum voltage and frequency were 2.54 mV and 46.9 kHz, respectively, which were mainly limited by the maximum operation frequency (12.3 GHz) of the V-PNM and the multiplication factor (100-fold) of the DFQA.[9)]

To synthesize a voltage sinusoidal of higher resolution and larger amplitude, the maximum SFQ pulse frequency and the multiplication factor should be improved. Especially, we have found that the clock frequency in the V-PNM would limit the performance of SFQ PFM D/A converters, whereas the voltage multiplication factor as large as 1000 fold was realized using standalone DFQAs.[14),15),19)] One method to improve the performance of SFQ digital circuitry is introduction of integration processes with higher Josephson critical current densities (J_c's), because the scaling rule suggests that clock frequencies of SFQ digital circuitry are approximately proportional to the square root of J_c.[20)] Recently, we have had opportunities to integrate our SFQ circuits using a 10-kA/cm^2 Nb/AlO$_x$/Nb process,[21)] referred to as HSTP, of National Institute of Advanced Industrial Science and Technology (AIST), which could double the operation speed in comparison with our previous circuits fabricated using a 2.5-kA/cm^2 Nb/AlO$_x$/Nb process,[22)] referred to as STP2, of AIST.

It should be noted that a DFQA includes unshunted Nb/AlO$_x$/Nb junctions. A magnetically-coupling SFQ driver/receiver circuit (MC-SFQ-DR) connecting a V-PNM and a DFQA also comprises unshunted junctions.[23),24)] This is because dynamic behaviors of unshutned Nb/AlO$_x$/Nb junctions are used for generation of double flux quanta via 4π phase leap. The smaller capacitance and smaller subgap resistance of high-J_c junctions would change dynamics of unshunted junctions and could make negative effects on operations of these circuits.

In this paper, we describe our DFQAs and MC-SFQ-DR designed for the AIST HSTP. We first simulated circuit operations assuming the HSTP junction parameters. Next, we fabricated test circuits using the AIST HSTP and measured their characteristics at liquid helium temperature. The results demonstrated that the performance of these circuits was improved without significant negative effects by using the AIST HSTP.

2. Numerical simulation magnetically-coupling SFQ driver/receiver and ±20-fold DFQAs designed for the AIST HSTP

2.1 Junction parameters for STP2 and HSTP used in numerical simulation

As described above, J_c values for HSTP and STP2 are 10-kA/cm^2 and 2.5-kA/cm^2, respectively. We assumed that the specific junction capacitance C_s, the specific subgap resistance R_{sg}, and the J_cR_{sg} product for HSTP were 6.4 μF/cm^2, 1.0 μΩcm^2, and 10 mV, respectively, whereas those for STP2 were 22 μF/cm^2, 2.0 μΩcm^2, and 20 mV.[25)]
We used the JSIM program for numerical analog circuit simulation. In JSIM simulation, a periodic pulse train was assumed for the SFQ input by using a spice *PULSE* source instead of the overbiasing method that was used in experiments. No thermal noises were included in simulation, that is, zero temperature was assumed.

2.2 Magnetically-coupling SFQ driver/receiver circuit

As described above, an MC-SFQ-DR is used in SFQ PFM D/A converters to transfer SFQ pulses from a V-PNM to a DFQA, especially to a DFQA realizing negative voltage multiplication. [11)] The circuit configuration is presented in Fig. 1. The final two junctions in the driver are unshunted to generate DFQ, which enhances the induced current in the receiver.

For fabrication using HSTP, we employed the inductance and I_c's as the same as those fabricated using STP2, whereas the shunting resistance values were chosen to realize critical damping, except for the unshunted junctions.
Figure 2 shows simulation results demonstrating the bias conditions for correct operation of the MC-SFQ-DR connected to a −20-fold DFQA (details described in the next

subsection). Results for SFQ pulse frequencies f_{IN} of 20 and 60 GHz are presented. When f_{IN} was set to 20 GHz, the operation range of the driver bias current I_{DR} was from 0.61 to 1.3 mA for the receiver bias current I_{RC} of 0.32 mA. By contrast, when f_{IN} was 60 GHz (slightly lower than 64.5 Hz, the maximum input repetition frequency of the −20-fold DFQA described in the section 2.4), the operation range was divided in to two regions. As shown in as shown in Fig. 2 (b), the lower bias current region (Region I) was from 0.69 to 0.88 mA, and the higher bias region (Region II) was from 1.1 to 1.3 mA respectively. Numerical results of the junction phase evolution for I_{DR} of 0.76 mA (Region I), 1.1 mA (Region II), and 0.99 mA (outside of Regions I or II) are shown in Fig. 3. The colors of the phase waveforms correspond to those of the Josephson junctions in Fig. 1. In Regions I and II, 2π and 4π phase leap (SFQ and DFQ generation) occurred at JJ_{DR} for every input SFQ pulse, respectively. Then, 2π phase leap occurred periodically at JJ_{RC1} and completed SFQ propagation correctly. The phase evolution of JJ_{DR} for I_{DR} of 0.99 mA (outside of Regions I or II), on the other hand, included mixed 2π or 4π phase leaps, that is, the number of generated flux quanta for every input SFQ pulse was not fixed. In this case, JJ_{RC2} switched aperiodically, resulting in failure of SFQ propagation. There seems to be a room of reoptimization of the MC-SFQ-DR for HSTP, which we are now conducting. Although the bias margin is reduced, these numerical results suggest that the MC-SFQ-DR with the HSTP parameters should work for the input SFQ pulse train higher than 60 GHz, which is roughly twofold increase in comparison with that of STP2. That is, HSTP enhances the speed performance of the MC-SFQ-DR as well as that of conventional RSFQ digital circuits.

2.3 Device parameters of 3-junction loop

Figure 4(a) shows the equivalent circuit of a 3-junctoin loop (3JL) that is a fundamental component of a DFQA. JJ_A and JJ_C are critically damped by external resistor, whereas JJ_B is unshunted for DFQ generation. An SFQ pulse fed from JJ_A propagates to the next stage through JJ_C with DFQ generation at JJ_B. The voltage multiplication factor of a DFQA is increased by stacking 3JLs; the output average voltage V_{OUT} is expressed for the input average voltage V_{IN} as

$$V_{OUT} = (N+1)\cdot V_{IN} = (N+1)\cdot \Phi_0 \cdot f_{IN}, (1)$$

where Φ_0 is the flux quantum (a physical constant), whereas N and f_{IN} are the number of stacked 3JLs and the frequency (i.e., the number of flux quanta per unit time) fed through the DFQA, respectively.

We have studied two types of DFQAs with different principles for controlling the propagation direction of SFQ pulses from JJ_A to JJ_C. One is the critical-current-controlled type DFQA (I_c-DFQA), in which the propagation direction is controlled by using the difference between the critical current (I_c) values of JJ_A and JJ_C.[13)14)-17)] (An SFQ pulse propagates through JJ_C having a smaller I_c value.) The other is the phase-damping-controlled type DFQA (β_c-DFQA),[17,18)] in which the propagation direction is controlled by using the difference between the McCumber parameter (β_c) values of JJ_A and JJ_C.[18),19)] (An SFQ pulse propagates through JJ_C having a larger β_c value.) Here, βc is given by

$$\beta_c = \frac{2\pi I_c R^2 C}{\Phi_0}, (2)$$

where R and C are the resistance (the subgap resistance for an unshunted junction, or the combined resistance of the subgap resistance and the external shunting resistance for an externally shunted junction) and the capacitance of a Josephson junction, respectively.

In this study, we focused on the I_c-DFQA and redesigned its parameters for HSTP, because I_c-DFQAs in our previous works demonstrated robust operation more than β_c-DFQAs. (In our experiments, operation of β_c-DFQAs looked sensitive to parameter deviation.) Table I shows the 3JL parameters used for STP2 and redesigned for HSTP. When we redesigned the I_c-DFQA for HSTP, we tried to keep the inductances, I_c values, and β_c values as same as those for STP2, except for the C and R_{sg} of JJ_B which were intrinsically determined by the fabrication process.

2.4 Numerical simulation for ±20-fold DFQAs

We designed series-connected DFQAs including a +20- and a −20-fold DFQA each of which was composed of 19-stacked 3JLs. The circuit configuration is shown in Fig. 5(a). Input SFQ pulses for the +20-fold DFQA were directly fed through a Josephson transmission line (JTL),[26)] whereas those for the −20-fold DFQA were fed via an MC-SFQ-DR.

Numerical input-output characteristics are presented in Fig.6 as red and blue circles, where the ideal ±20-fold voltage multiplication is presented by dashed straight lines. In simulation, input SFQ pulses were fed to either +20- or −20-fold DFQA, and therefore, the characteristics were investigated separately. The input voltage V_{IN} was derived using the AC Josephson effect with the repetition frequency f_{IN} of periodic pulses, that is, $V_{IN} = \Phi_0 \cdot f_{IN}$. Relative error was also derived using Eq. (3).

$$Relative\ error = \frac{\{V_{OUT} - (\pm 20 \cdot V_{IN})\}}{(\pm 20 \cdot V_{IN})} \times 100\%, \quad (3)$$

As in the previous research, operations with relative error of ±1% or less were regarded as correct operation. For the +20-fold DFQA, the maximum input repetition frequency f_{INMAX}, the maximum input voltage V_{INMAX}, and the maximum output voltage V_{OUTMAX} were determined as 62.5 GHz, 129 μV, and 2.58 mV, respectively. On the other hand, for the −20-fold DFQA, those were determined as 64.5 GHz, 133 μV, and −2.68 mV, respectively. We should note that the MC-SFQ-DR itself worked correctly no less than 80 GHz.

Although there was concern about the effect of β_c reduction of JJ_B on DFQ generation, it was found from the simulation results that correct voltage multiplication was realized by DFQAs with the HSTP parameters.

These numerical results suggest that the ±20-fold DFQAs with the MC-SFQ-DR should work for the input SFQ pulse train of repetition frequencies beyond 60 GHz, which is roughly twofold increase in comparison with that of STP2. That is, the high-J_c integration process HSTP also would enhance the speed performance of the I_c-DFQA as well as conventional RSFQ digital circuits.

3. Experimental results and discussion

3.1 Physical layouts of MC-SFQ-DR and ±20-fold DFQAs

To confirm the circuit characteristics, we designed ±20-fold DFQAs as presented in Fig. 5(a). An MC-SFQ-DR was also included. The InductEx program was used for extraction of self-inductances, mutual-inductances, and coupling factors.[27)-29)] Photomicrographs of a single 3JL and a test circuit fabricated using HSTP are respectively shown in Fig. 4(b) and Fig. 5(b). As can be seen in Fig. 5(b), Series-connected nineteen 3JLs were placed in a straight line for ±20-fold DFQAs. We refer to this layout as the STRAIGHT type. Besides, because 3JLs should be placed like a meander pattern for a larger number N of 3JLs (that is, a larger multiplication factor such as 1000-fold), we also designed other two physical layouts of +20-fold DFQAs including turns of 3JL stacks. There were two types of turns, the INSIDE type and OUTSIDE type; in the INSIDE type, the flux bias line 1 was placed inside at corners, whereas in the OUTSIDE type, the flux bias line 1 was placed outside at corners. Photomicrographs of +20-fold DFQA of the INSIDE and OUTSIDE type are presented in Fig. 7.

3.2 Experimental results

The experiment was conducted by cooling a test chip with liquid helium bath.

First, we measured characteristics of +20-fold DFQAs of three types, STRAIGHT, INSIDE and OUTSIDE. Input SFQ pulses were fed by the overbiasing method. The V_{IN}—V_{OUT} characteristics were observed on a digital oscilloscope (OCS) via 100-fold low noise preamplifiers. Experimental results are depicted in Fig. 8. The dashed line represents the ideal +20-fold voltage multiplication. +20-fold DFQAs of STRAIGHT, INSIDE, and OUTSIDE types operated correctly up to V_{IN} of 140 μV, for which the corresponding f_{IN} was 67.7 GHz. No significant difference was confirmed among these three types.

Next, to evaluate voltages precisely, we measured V_{IN}—V_{OUT} characteristics of a +20-fold DFQA of INSIDE type and a −20-fold DFQA of STRAIGHT type using digital multimeters (DMMs). No preamplifiers were used. The results are shown in Fig. 9 which are essentially the same as those presented in our technical report.[30] For the +20-fold DFQA of INSIDE type, V_{INMAX}, V_{OUTMAX}, and f_{INMAX} were determined as 147 μV, 2.90 mV, and 70.9 GHz, respectively, for relative errors less than ±1%. On the other hand, those for the −20-fold DFQA of STRAIGHT type were respectively determined as 126 μV, −2.51 mV, and 61.1 GHz.

The experimental values for the +20-fold DFQA were slightly better than the numerical results; the experimental f_{INMAX} was 8 GHz higher than the numerical value, which could be attributed to the bias condition finely tuned in experiments. The experimental values for the −20-fold DFQA of STRAIGHT type were comparable with the numerical ones. It should be noted that the relative errors for the −20-fold DFQA did not fall well into ±1% range. Operation errors of the MC-SFQ-DR used to feed SFQ pulses to the −20-fold DFQA could be the reason, because the +20-fold DFQA without an MC-SFQ-DR worked well (see Fig. 5 for the circuit configuration). We found that the bias margins for correct operation of the −20-fold DFQA were sometimes substantially reduced, and that they were resurged by heating up and cooling down the test chip. It suggested that magnetic flux was trapped in and released from the test chip. In the MC-SFQ-DR, we employed a hole in the ground plane to make the magnetic coupling stronger, which could have a role of flux trapping site. Such flux trapping could reduce the bias margins of the MC-SFQ-DR.[31] Elimination of a hole in the ground plane would be effective to avoid flux trapping, resulting in the stable operation. Magnetic shielding around the test chip should also be improved.

In addition to the comparison between the experimental and numerical results for HSTP, we also compared between the experimental f_{INMAX} for HSTP and that for STP2, which is tabulated in Table II.[32] It is found that f_{INMAX} values were improved twofold (and more) by changing the integration process from STP2 to HSTP.

4. Conclusions

For improvement of SFQ-PFM D/A converters, we investigated a DFQA and an MC-SFQ-DR fabricated using the AIST HSTP. The J_c value of the AIST HSTP was 10-kA/cm^2 and four times larger than that of the AIST STP2 (2.5-kA/cm^2) we had used. In general, switching speed of SFQ logic circuits is expected to be proportional to square root of J_c. However, a DFQA and an MC-SFQ-DR included unshunted Josephson junctions for DFQ generation, and therefore, it was unclear if the high-J_c process improved their performances. We redesigned the device parameters of the MC-SFQ-DR and the 3JL, the fundamental cell of a DFQA, for the AIST HSTP. Numerical simulation demonstrated that the +20-fold and −20-fold DFQA operated for the input SFQ repetition frequencies up to 62.5 and 64.5 GHz. These frequencies were approximately two-fold of that assuming the parameters of the AIST STP2. Next, we measured test chips cooled in a liquid helium bath. The maximum input voltages for a +20-fold and a −20-fold DFQA were 147 and 126 μV, for which the corresponding Josephson frequencies were 70.9 and 61.1 GHz. It was confirmed that the operation frequencies of the DFQAs and MC-SFQ-DR were improved by introducing high-J_c integration process.

Acknowledgments

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Figure Captions

Fig. 1. (Color online) Equivalent circuit of a magnetically-coupling SFQ driver/receiver circuit (MC-SFQ-DR). Critical currents and external shunt resistors of JJ_{DR}, JJ_{RC1}, and JJ_{RC2} are as follows. : I_{JJDR} = 153 μA, I_{JJRC1} = 169 μA, R_{JJRC1} = 4.42 Ω, I_{JJRC2} = 100 μA, and R_{JJRC2} =7.46 Ω. The colors of JJ_{DR}, JJ_{RC1} and JJ_{RC2} correspond to the curves of switching characteristics shown in Fig.3.

Fig. 2. (Color online) Bias margins on the I_{DR}—I_{RC} plane of an MC-SFQ-DR for the input frequency f_{IN} of (a) 20 GHz and (b) 60 GHz. Correct −20-fold voltage multiplication was confirmed at the bias conditions filled in yellow.

Fig. 3. (Color online) Switching characteristics of the MC-SFQ-DR for I_{DR} of (a) 0.76 mA (SFQ mode operation), (b) 1.1 mA (DFQ mode operation), and (c) 0.99 mA (mixed mode operation).

Fig. 4. (Color online) (a) Equivalent circuit and (b) photomicrograph of a 3-junction loop (3JL) acting as a single stage of a double-flux-quantum amplifier (DFQA). JJ_A and JJ_B are critically damped by external resistors, whereas JJ_C is unshunted for DFQ generation. SFQ pulses fed from JJ_A propagate to the next stage through JJ_C after DFQ generation at JJ_B.

Fig. 5. (Color online) (a)Schematic and (b) photomicrograph of series-connected +20-fold and −20-fold DFQAs. Each DFQA works independently except for the common line used for voltage measurement. For the +20-fold and −20-fold DFQA, the input SFQ pulse trains are respectively generated at the lower and upper Josephson junction labelled as "over-biasing junction". In this work, the +20-fold and −20-fold DFQA were tested one by one.

Fig. 6. (Color online) Input-output voltage characteristics of (a) +20-fold and (b) −20-fold DFQAs that were obtained in jsim simulation. The upper and lower horizontal axis represent the SFQ repetition frequency f_{IN} and the corresponding input voltage V_{IN}, respectively.

Fig. 7. (Color online) Photomicrograph of +20-fold DFQAs including the INSIDE and OUTSIDE types for realizing meander patterns.

Fig. 8. (Color online) Input-output characteristics of three types of +20-fold DFQAs obtained by a digital oscilloscope via 100-fold preamplifiers. Bias current were set as follows: STRAIGH type (I_{SB} = 0.480 mA, I_{FB1} = 2.85 mA, I_{FB2} = 0.160 mA). OUTSIDE type (I_{SB} = 0.425 mA, I_{FB1} = 6.44 mA, I_{FB2} = 0 mA). INSIDE type (I_{SB} = 0.410 mA, I_{FB1} = 5.18 mA, I_{FB2} = 0 mA).

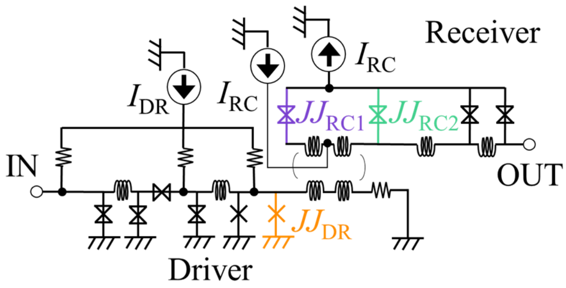
Fig. 9. (Color online) Input-output characteristics of +20-fold DFQA INSIDE type and −20-fold DFQA STRAIGHT type obtained by digital multi-meter. The relative error at each input-output voltage is indicated by cross marks. Each bias current correspond to Fig. 5 (a) is as follows: +20-fold DFQA INSIDE type (I_{SBP} = 0.430 mA, I_{FB1P} = 2.00 mA, I_{FB2P} = 0 mA). −20-fold DFQA STRAIGHT type (I_{SBN+} = 0.425 mA, I_{SBN-} = −0.425 mA, I_{FBN1} = −1.50 mA, I_{FB2N} = 0 mA, I_{DR} = 0.562mA, I_{RC} = 0.321mA).

Table I Comparison of 3JL parameters used in β_c-DFQA and I_c-DFQAs.

		β_c-DFQA (STP2)	I_c-DFQA (STP2)	I_c-DFQA (HSTP)
L_1/pH		2.9	1.6	
L_2/pH		0.68	1.9	
L_3/pH		0.62	0.7	
L_4/pH		1.5	neglected	
M_1/pH		0.36	0.27	
M_2/pH		none	0.16	
JJ_A	I_c/μA	100	240	237
	R_{shunt}/Ω	0.58	1.6	3.3
	β_c	0.022	0.98	1.1
JJ_B	I_c/μA	210	220	219
	R_{shunt}/Ω	unshunted	unshunted	unshunted
JJ_C	I_c/μA	130	140	139
	R_{shunt}/Ω	35	2.8	5.55
	β_c	138	1.0	1.1

Table II Comparison of f_{INMAX} between DFQA fabricated by using 2.5-kA/cm2 and 10-kA/cm2 process.

	f_{INMAX}/GHz		Ratio
	2.5-kA/cm^2 (STP2)	10-kA/cm^2 (HSTP)	HSTP/STP2
+20-fold	26.5	70.9	2.68
−20-fold	28.9	61.1	2.11



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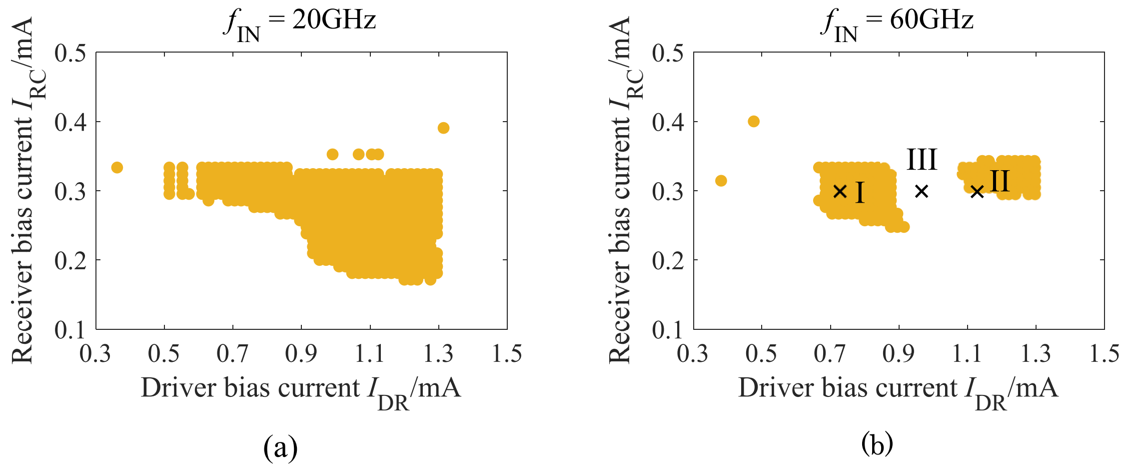


Fig. 2. (Color online) Bias margins on the I_{DR}—I_{RC} plane of an MC-SFQ-DR for the input frequency f_{IN} of (a) 20 GHz and (b) 60 GHz. Correct −20-fold voltage multiplication was confirmed at the bias conditions filled in yellow.

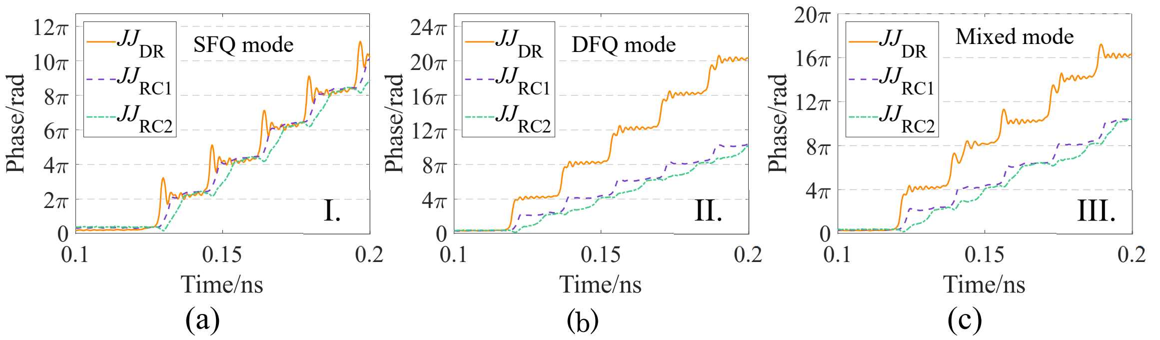


Fig. 3. (Color online) Switching characteristics of the MC-SFQ-DR for I_{DR} of (a) 0.76 mA (SFQ mode operation), (b) 1.1 mA (DFQ mode operation), and (c) 0.99 mA (mixed mode operation).

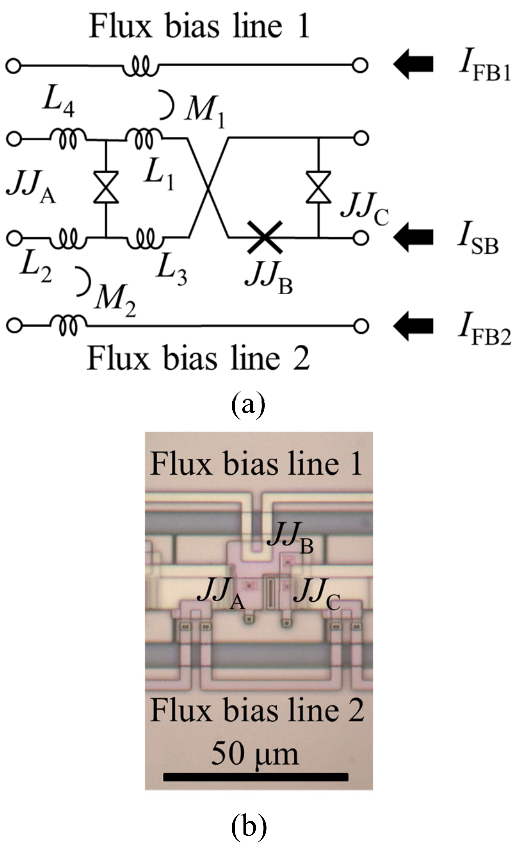
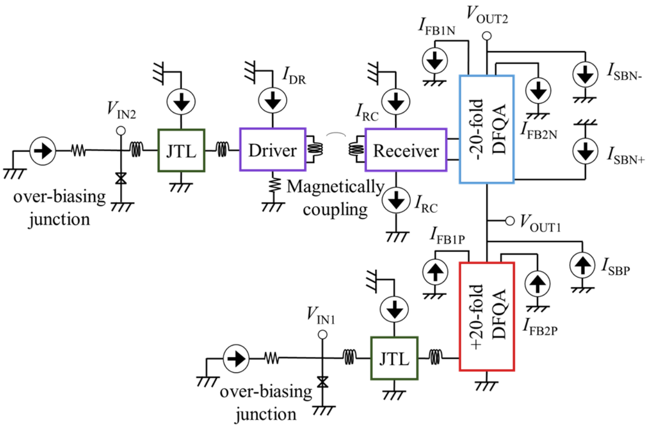
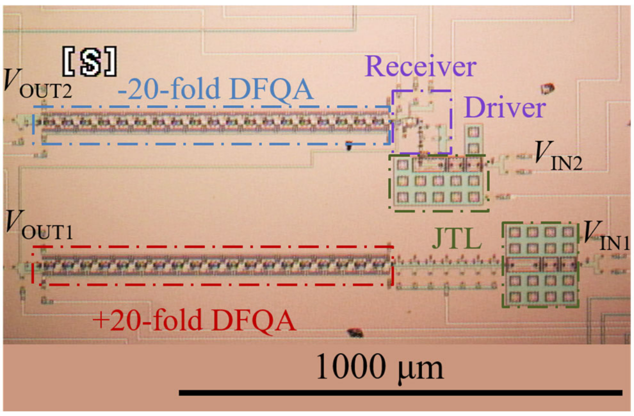


Fig. 4. (Color online) (a) Equivalent circuit and (b) photomicrograph of a 3-junction loop (3JL) acting as a single stage of a double-flux-quantum amplifier (DFQA). JJ_A and JJ_B are critically damped by external resistors, whereas JJ_C is

unshunted for DFQ generation. SFQ pulses fed from JJ_A propagate to the next stage through JJ_C after DFQ generation at JJ_B.



(a)



(b)

Fig. 5. (Color online) (a)Schematic and (b) photomicrograph of series-connected +20-fold and −20-fold DFQAs. Each DFQA works independently except for the common line used for voltage measurement. For the +20-fold and −20-fold DFQA, the input SFQ pulse trains are respectively generated at the lower and upper Josephson junction labelled as "over-biasing junction". In this work, the +20-fold and −20-fold DFQA were tested one by one.

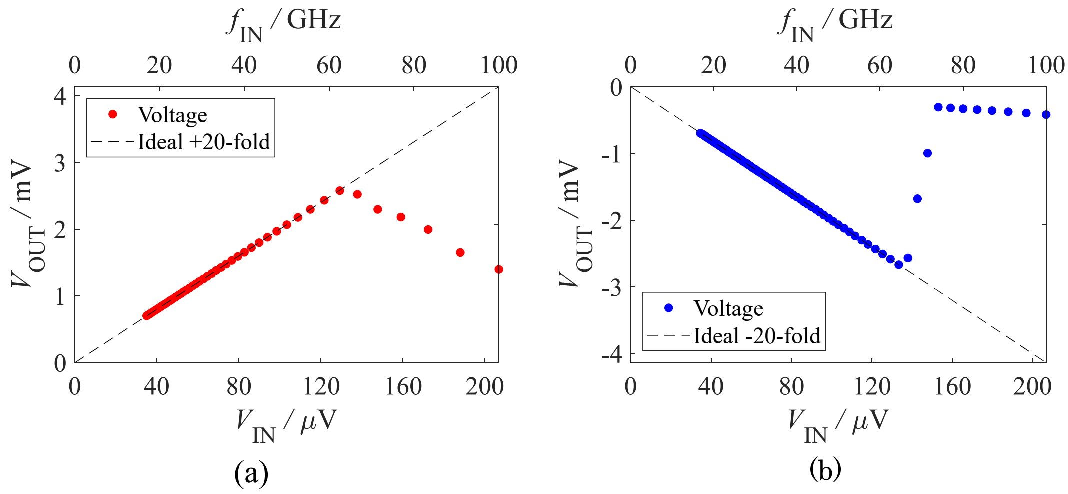


Fig. 6. (Color online) Input-output voltage characteristics of (a) +20-fold and (b) −20-fold DFQAs that were obtained in jsim simulation. The upper and lower horizontal axis represent the SFQ repetition frequency f_{IN} and the corresponding input voltage V_{IN}, respectively.

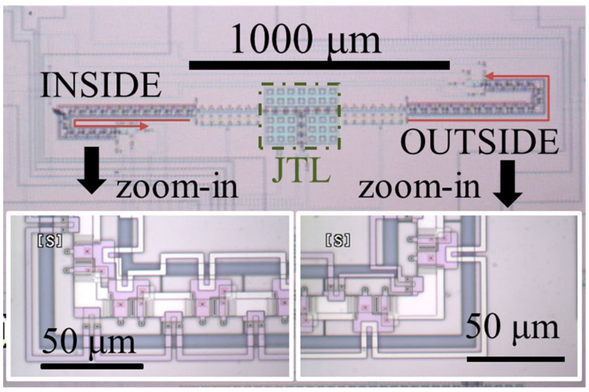


Fig. 7. (Color online) Photomicrograph of +20-fold DFQAs including the INSIDE and OUTSIDE types for realizing meander patterns.

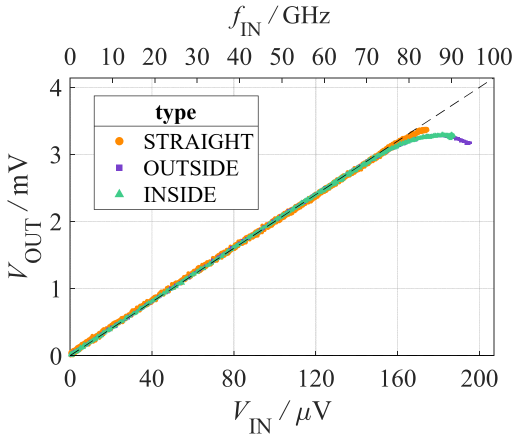
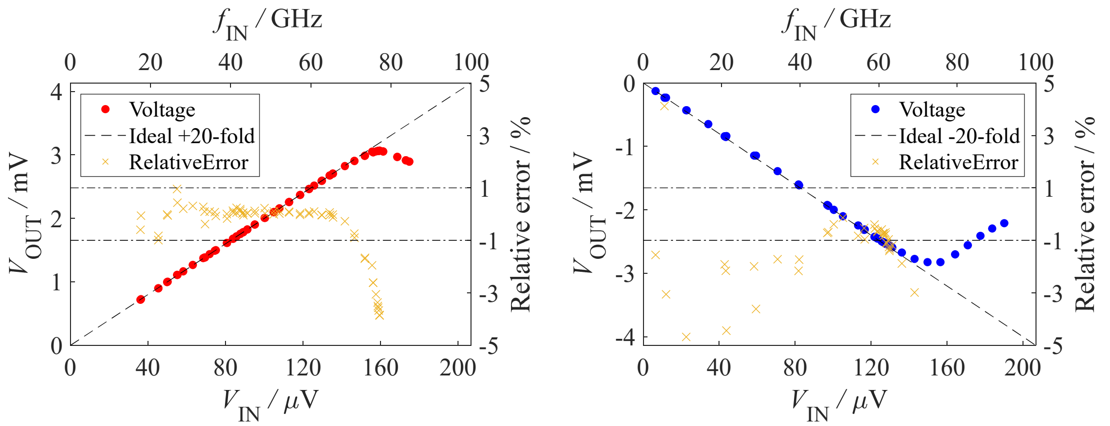


Fig. 8. (Color online) Input-output characteristics of three types of +20-fold DFQAs obtained by a digital oscilloscope via 100-fold preamplifiers. Bias current were set as follows: STRAIGH type (I_{SB} = 0.480 mA, I_{FB1} = 2.85 mA, I_{FB2} = 0.160 mA). OUTSIDE type (I_{SB} = 0.425 mA, I_{FB1} = 6.44 mA, I_{FB2} = 0 mA). INSIDE type (I_{SB} = 0.410 mA, I_{FB1} = 5.18 mA, I_{FB2} = 0 mA).



(a) (b)

Fig. 9. (Color online) Input-output characteristics of +20-fold DFQA INSIDE type and −20-fold DFQA STRAIGHT type obtained by digital multi-meter. The relative error at each input-output voltage is indicated by cross marks. Each bias current correspond to Fig. 5 (a) is as follows: +20-fold DFQA INSIDE type (I_{SBP} = 0.430 mA, I_{FB1P} = 2.00 mA, I_{FB2P} = 0 mA). −20-fold DFQA STRAIGHT type (I_{SBN+} = 0.425 mA, I_{SBN-} = −0.425 mA, I_{FBN1} = −1.50 mA, I_{FB2N} = 0 mA, I_{DR} = 0.562mA, I_{RC} = 0.321mA).