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# Design and Validation of A High-Power, High Density All Silicon Carbide Three-Level Inverter

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# ABSTRACT

Transportation electrification is clearly the road toward the future. Compared to internal combustion engine, the electrified vehicle has less carbon-dioxide emission, less maintenance costs and less operation costs. It also offers higher efficiency and safety margin. More importantly, it relieves human's dependence on conventional fossil energy. In the electrification progress, the revolution of electric traction drive systems is one of the most important milestone. The traction system should keep high efficiency to avoid performance reduction. Moreover, the motor drive should be designed within limited space without sacrificing output power rating. Based on the road map from US Drive Electrical and Electronics Technical Team, US Department of Energy, a gap is still there between roadmap target and the state-of-art. To fill the gap, this dissertation performs a systematic research in motor drive system for traction inverters. This paper starts from optimal theoretical design of power converters by using loss model and real-time simulation system. Based on optimal paper design, hardware design is implemented. The component design for converter, such as the laminated busbar, are the focus in this dissertation. The optimized busbar structure can effectively reduce stray inductance in the current-commutation loop, reducing switching overshoots of power modules and increasing semiconductor reliability. The system-level design and trade-off is also analyzed and illustrated by using a 250kW three-level T-type neutral-point clamped converter. The design has reached high efficiency and high-power density. The converter system is also evaluated through comprehensive tests, such as double-pulse tests and continuous tests. The test setup, test condition and test result analysis are discussed in the dissertation. In the end, the dissertation also proposed an improved impedance characterization method for components parasitic inductance measurement in traction drive systems, such as

laminated busbar, power module and capacitors. The characterization shares better accuracy and can be customized for device under test with any geometry.

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# DEDICATION

This dissertation is dedicated to my dearest fiancé, Zhao Yuan, and my beloved parents, Xueming Wang and Xia Wang.

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1. Z. Wang et al., "A Compact 250 kW Silicon Carbide MOSFET based Three-Level Traction Inverter for Heavy Equipment Applications," 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, 2018, pp. 1129-1134.
   ***Chapter 2 is made up of this paper***

2. Z. Wang, Y. Wu, M. H. Mahmud, Z. Zhao, Y. Zhao and H. A. Mantooth, "Design and Validation of A 250-kW All-Silicon Carbide High-Density Three-Level T-Type Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 578-588, March 2020.
   ***Chapter 3 is made up of this paper***

3. Z. Wang, Y. Wu, M. Mahmud, Z. Yuan, Y. Zhao and H. A. Mantooth, "Busbar Design and Optimization for Voltage Overshoot Mitigation of A Silicon Carbide High-Power Three-Phase T-Type Inverter," in IEEE Transactions on Power Electronics.
   ***Chapter 4 is made up of this paper***

4. Z. Wang et al., " Fixtures Design Considerations for Impedance Measurement." 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phenix, AZ, 2021.
   ***Chapter 5 is made up of this paper***

# CHAPTER 1

# INTRODUCTION

## 1.1 Motivation and challenges

Transportation electrification has been a trend for many years. The electrified vehicle offers great benefits compared to the conventional internal combustion engine (ICE) including less carbon-dioxide emission, less dependents on fossil energies, less operation costs, less maintenance, higher safety rating and better efficiency. The recent breakthrough battery technologies further making the high-performance and heavy-duty electrified vehicles possible.

Nevertheless, the electric traction drive systems (ETDS) could be a bottleneck. With the limited vehicle space, the power electronics motor drive should have high power density to deliver sufficient energy at limited time. Besides, ETDS are required to maintain high efficiency in various operation conditions to keep long mileage.

Accordingly, the office of efficiency and renewable energy, department of energy (DOE) has proposed US Drive Electrical and Electronics Technical Team (EETT) Roadmap [1], which proposed design targets of ETDS in 2025, as seen table 1-1. A power density over 33kW/L and 88% volume reduction is required.

It is seen a huge gap between the state-of-art and the 2025 target. To fill the gap, tremendous works have been made in several aspects. For example, the topology innovation and selection are one of the keys to improve motor drive performance. It is seen that the conventional three-phase two-level topology enjoys simple structure, high reliability, and low conduction loss [2]. However, its insufficient output-THD performance [3], high EMI noise introduced by high dv/dt [4], and extraneous switching loss [5] could limit its performance for high power motor drive.

Table 1-1 DOE EETT Roadmap for Power Electronics Converters in Year of 2020 and 2025 [1]

| Technical Targets of Power-electronics Equipment in Electrified Vehicles | | | |
|---|---|---|---|
| | Years / Items | 2020 | 2025 |
| ETDS | Cost | 4.7 $/kW | 3.3 $/kW |
| | Power Density | 5.7 kW/L | 50 kW/L |
| On-board Charger | Cost | 50 $/kW | 35$/kW |
| | Specific Power | 3 kW/kg | 4 kW/kg |
| | Power Density | 3.5 kW/L | 4.6 kW/L |
| | Efficiency | 97.0% | 98.0% |
| Buck DC/DC Converter (325V to 14V) | Cost | <50 $/kW | 30 $/kW |
| | Specific Power | >1.2 kW/kg | 4 kW/kg |
| | Power Density | >3.0 kW/L | 4.6 kW/L |
| | Efficiency | > 94.0% | 98.0% |

Recently, the three-level neutral-point clamped converter (3L-NPC) and three-level active neutral-point clamped converter (3L-ANPC) gains more and more attentions. The University of Tennessee and General Electric have demonstrated its efficiency of 99.0% through designing a 1-MW 3L-ANPC motor-drive prototypes [6,7]. Such a topology can greatly reduce switching loss, dv/dt noise and limit THD. Because each device only needs to withstand half DC-link voltage, higher DC-link voltage can be utilized for given device ratings. Or the lower voltage-rating semiconductors can be used for the given DC-link voltages. However, 3L-NPC and 3L-ANPC

increase the counts of power semiconductor per phase, causing higher conductional loss and more complicated hardware design and optimization.

Three-level T-type neutral-point clamped topology (3L-TNPC) also has great potential in motor drive applications [8]. Compared to the two-level converter, 3L-TNPC has advantages of common three-level topologies, such as low dv/dt, low switching loss and lower output THD [9]. When compared it to 3L-NPC and 3L-ANPC, the 3L-TNPC has less switch counts and conduction loss [10]. However, the 3L-TNPC's external-leg has higher voltage stress compared to the 3L-NPC and 3L-ANPC. And the conduction loss of 3L-TNPC is lower than 3L-NPC but it is higher than two level converters [11]. Working with Advanced Research Projects Agency–Energy (Apar-E), and the Center for Power Optimization of Electro-thermal Systems (POETS), the University of Arkansas has built three prototypes of 3L-TNPC with power density over 25kW/L, and peak efficiency greater than 99.0% [12,13].

Besides the two-level converter and three-level converter, researchers also found a place for nine-level converters in high-performance motor drive. The recent research in Dr. Pilawa's group from the University of California Berkeley and the University of Illinois at Urbana-Champaign Urban demonstrates that nine-level switch-cap converters deliver power up to 200kVA with high efficiency high power density [14].

Great efforts are made in applying advanced semiconductors in motor drive. The wide-bandgap (WBG) based devices, such as Silicon-carbide (SiC) Metal–oxide–semiconductor Field-effect Transistor (MOSFET) [15], SiC junction-gate field-effect transistor (JFET) [16], SiC diode [17], Gallium Nitride (GaN) High-electron-mobility Transistors (HEMT) [18] and GaN field-effect transistor (FET) [19].

Compared to the conventional Si material, the WBG materials have higher break-down E-field, higher drift velocity, better thermal conductivity, and can handle higher carrier concentration. As a result, the WBG-based power semiconductors offer better figure-of-merit. For example, at the given bare-die dimension, the SiC-MOSFET and GaN HEMT offers lower on-state resistance and lower switching loss compared to the Si-IGBT and Si-MOSFET [20].

As a result, applying such devices into motor drive can bring benefits. For example, the [21] replaces four Si-Diodes by SiC-diodes in a 3L-NPC converter, reducing total loss by about 13%. Additionally, [22] combines SiC-MOSFET and Si-IGBT as a hybrid switch unit. It allows Si-IGBT carries majority conduction loss and SiC-MOSFET offers lower switching loss. The 3L-TNPC converter based on hybrid-switch concept can offer efficiency over 99.0% at switching frequency of 20kHz. Moreover, [23] utilizes full-SiC-MOSFET module in a 450-kVA converter. The full-SiC-MOSFET enables over tripled switching frequency and can keep peak efficiency over 99.47%.

## 1.2 Research objectives

Though tremendous efforts are made in improving motor drive performance, it is still seen a huge gap between the state-of-art and the 2025 target. To fill the gap, research should be made in the following aspects.

1. High-accuracy modeling system to guide motor drive design, such as semiconductor loss modeling and estimation, DC-link ripple modeling, and hardware parasitic modeling.

2. Understanding the system-level trade-off of motor drive systems, including

- The trade-off between different motor-drive topologies,

- The trade-off between switching loss, conduction loss and output THD,

3. Multi-dimensional integration of power electronics system to achieve

- Optimized parasitic control,
- Optimized thermal dissipation,
- Compact converter-level packaging with high power density.

4. Fully utilize the advantages of wide bandgap devices, such as Silicon-carbide metal–oxide–semiconductor field-effect transistor (MOSFET), including

- Optimized SiC-MOSFET configuration with optimized conduction loss and switching loss,
- Minimized stray inductance of SiC-MOSFET's commutation loop for overshoot mitigation,
- Proper switching speed with sufficient switching loss reduction,
- Well-controlled junction temperature

## 1.3 Dissertation outline

Chapter 2 is at the inverter's paper-design stage. After determining the topology and fully understanding its advantages, this chapter discusses the decision of specifications. First of all, a real-time simulation model is built, which can use the look- up table to recall the information from the datasheet, and by judging the operation mode of the switch device, we can see the conduction and switching loss distribution in real time. At the same time, the dc-bus voltage and switching frequency are easy to be adjusted, so through case studies, the best dc-bus and switching frequency

for our topology application scenarios are determined. At the same time, the hardware selection of dc-link capacitor is also preliminarily determined considering the requirements of capacitance and RMS current. Finally, through HIL simulation, the inverter's modulation is verified. This chapter paved the way for subsequent hardware design and experiments in the following chapters.

Chapter 3 is a summary of the inverter hardware design and high-power test results. The beginning is an in-depth analysis of the operation mode of the SiC MOSFET based T-type inverter. There is also a summary of power loss under various voltage and current directions. The next step is to use the real-time simulation mentioned in Chapter 2 to analyze the loss distribution, and find the module with higher power loss. This is very helpful for the subsequent cold plate design. At the same time, by breaking down the loss, we can find the main source of total loss is the conduction loss. These simulation results can help to initially determine whether the efficiency target can be achieved theoretically. Next, the clamped inductor test (CIL) is introduced. Through the switching loss results obtained from the CIL, we can optimize the accuracy of the loss model. This chapter also explains the phenomenon that the oscillation of T-type inverter is larger than that of two-level inverter. The following of this chapter explains the selection of module, gate driver, and dc-link cap, and also briefly introduces the design of the laminated bus bar. Finally, this chapter shows the results of the full-power test. Through the analysis of the power analyzer measurement, the target efficiency of 98.5% is achieved.

Chapter 4 focuses on the design of the laminated bus bar of this inverter. First, it theoretically explains why the laminated bus bar with low stray inductance has benefit to the whole inverter system, and then introduces the composition of the specific T-type inverter bus bar. Then the design difficulty considering the specific module layout is pointed out. Then this chapter summarizes and analyzes all the current communication loops (CCLs) of the inverter and obtained

the guidance of optimizing bus bar design. Next, the busbar design principles in the traditional method are elaborated, and self-inductance and mutual inductance are introduced at the same time. The final bus bar design of this inverter is introduced in detail. In the design process, we found that reducing self-inductance and increasing mutual inductance are two effective ways for reducing the total stray inductance. Based on this analysis, this chapter proposes a new bus bar 3-dimentional (3D) design concept. The bus bar layer buried under others at certain potentials can reduce self-inductance and increase mutual inductance. This chapter proves that the new bus bar design concept can effectively reduce total stray inductance through Q3D simulation and direct measurement with impedance analyzer. In addition, the article also proposed a hybrid bus bar structure with PCB snubber circuit using high-frequency capacitors. Finally, it is proved through experiments that the new 3D concept bus bar with low ESL dc-link capacitor can effectively reduce the Vds overshoot. Additionally, the hybrid bus bar structure with PCB snubber circuit can also suppress Vds overshoot.

Chapter 5 introduces the issue of how the fixture should be designed when the impedance analyzer is used to measure non-standard components. Through the previous chapters, we have learned that the stray inductance in the entire CCL has an impact on the Vds overshoot of the switch device. So, in the components' design and selection stages, it is particularly important to accurately know the internal inductance of each component. At present, when measuring with an impedance analyzer, high-precision fixtures are mainly designed for SMD and lead terminal components. In the design of high-power converters, we need to know some non-standard components' inductance, such as bulk dc-link capacitors and customized bus bar, which requires us to design a fixture to connect these devices with the impedance analyzer. This chapter discusses the design of this fixture to improve the accuracy of the measurement. First of all, as a comparison,

a leaded film capacitor is selected as the standard reference, and it is measured by two commercial fixtures and impedance analyzers. Then three PCB customized fixtures were designed, and the standard film capacitor is measured again. Through comparative experiments, we found one of the customized designs is closest to the commercial fixture measurement results, then the design guidance is summarized. In the end, experiments are conducted to verify this optimal design. The CCL inductance of a 2-L inverter is measured through an impedance analyzer and fixture. The results proved that the inductance derived from the Q3D simulation results and double-pulse-test (DPT) Vds waveform oscillation frequency are highly consistent with our fixture measurement results, thus proving the accuracy of the customized fixture measurement.

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# CHAPTER 2

# A COMPACT 250 KW SILICON CARBIDE MOSFET BASED THREE-LEVEL TRACTION INVERTER FOR HEAVY EQUIPMENT APPLICATIONS



## 2.1 Abstract

A sustained effort is required to realize the aggressive targets of electrification of heavy equipment, e.g., the heavy-duty off-road vehicles, due to numerous emerging challenges, which are different from those in the automotive industry. Heavy equipment manufacturers are increasingly investing in new generation of power electronics technology to fulfill the high performance and reliability targets under harsh environments while reducing fuel consumption and staying cost competitive. In this work, a holistic power electronic circuits design is proposed to achieve 4× power density at 98% peak efficiency for a compact 250 kW three-phase three-level (3-L) T-type traction inverter. The proposed T-type inverter is designed using the best-in-class silicon carbide (SiC) power modules. Most importantly a multi-objective optimization approach to trade the volumetric power density (kW/l) against SiC device type (650, 900 and 1200 V), dc bus voltage, switching frequency, the size of the passive components. T-type inverter system design guidance is given in this work, including loss calculation, dc-link capacitor selection, thermal management solution, and bussing structure. In addition, the hardware-in-the-loop

simulation study is performed to validate the performance of the control system designed for the traction inverter.

## 2.2 Introduction

The electrified drivetrain of the heavy equipment demands outstanding efficiency at low costs. Recently, significant amount of research effort has gone into the development of highly efficient and compact traction inverters [1], [2], since the improved efficiency and power density coupled with lower losses in the motor and lighter weight all combine to produce more powerful, more energy efficient heavy equipment that is expected to reduce more than 25% operating costs [3]. To reduce the size and cost of passive components, the switching frequency often needs to be increased to medium range, e.g., 10-25 kHz. With higher switching frequency, conventional 2-level silicon (Si) based power converters will have significantly increased losses that require bulky cooling systems. Potential loss reduction can be achieved through either topology innovation or the adoption of wide bandgap (WBG) power semiconductor devices. It has been proven that multi-level topologies, e.g., the 3-level (3-L) neutral point clamped converter and T-type converter, have better efficiency if the switching frequency is higher than 10 kHz [4]. The rapid development of a new generation WBG technologies opens up the possibility of high efficiency and high-performance operation at higher switching frequencies. In this work, a system-level multi-objective optimization is proposed to realize a compact 250 kW T-type that will fully exploit the benefits of both the SiC devices and the 3-level topology.

The main circuit topology is built upon the T-type inverter [5], which combines the positive aspects of two-level converters, such as low conduction losses and simple operation principles with the advantages of a three-level converter such as low switching losses and superior output voltage quality. The schematic of the proposed traction inverter system is shown in Fig. 2.1, which

includes the dc-link capacitors, gate drivers, various voltage and current sensors, and the main T-type inverter realized by two sets of SiC MOSFET half-bridge modules at different voltage ratings.

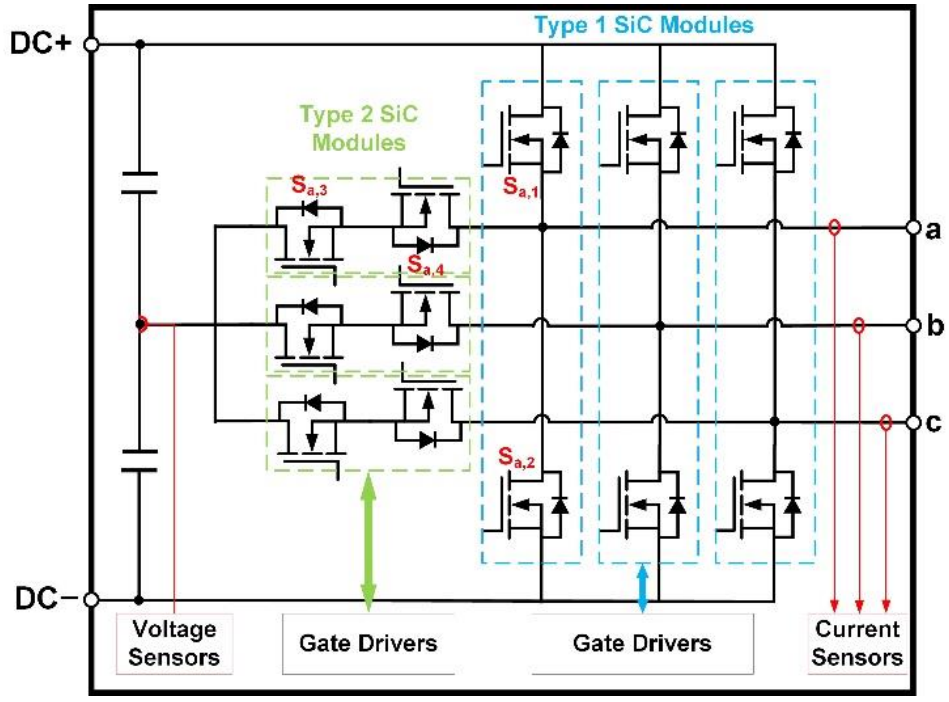



Figure 2-1 Schematic of proposed traction inverter system.

In this work, the multi-objective optimization approach is proposed to trade power density (kW/l) against SiC device type (650, 900, 1200V), switching frequency, dc bus voltage, the dc-link capacitor, and thermal management solutions.

Silicon Carbide (SiC) devices have the ability to operate at higher voltage. At a given power rating, the higher dc bus voltage of the inverter enables cable size reduction, resulting in significant copper savings and an overall weight reduction of the electric drivetrain [3]. In addition, a higher dc bus voltage will extend the constant torque-speed range of the motors. Therefore, in this work, the dc bus voltage is intended to increase from 700 V normally used for heavy-duty vehicles to an optimal value for most efficient design, which is higher than 850 V.

The selected voltage rating of the SiC devices is determined by the topology and the dc bus voltage. As shown in Fig. 1, $S_{a,1}$ and $S_{a,2}$ need to block full dc bus voltage, while $S_{a,3}$ and $S_{a,4}$ only need to block half of the dc bus voltage. All SiC devices are packaged into Wolfspeed's HT-3000 platform as shown in Fig. 2.2 [6], but the configuration of the devices in the module may be different. For instance, $S_{a,1}$ and $S_{a,2}$ are packaged as a standard half-bridge module, while Sa,3 and Sa,4 are packaged in a module using a common-source configuration.


Figure 2-2 Wolfspeed's all SiC high-performance half-bridge power module.

In this work, space vector pulse-width modulation (SVPWM) is used for its higher dc bus voltage utilization. An inverter system level loss model in real-time is firstly designed to estimate the system semiconductor losses based on the possible operation states. The comparison of simulation results on different dc voltages as well as the switching frequency is done to help system design from loss aspect. Then dc-link capacitor selection procedure is introduced considering both minimum capacitance calculation and capacitor root-mean-square (RMS) current calculation. In addition, thermal management solutions and bussing structure are also mentioned in this work briefly. Finally, the hardware-in-the-loop (HIL) simulation study is performed to validate the performance of designed T-type traction inverter system.

## 2.3 Instantaneous fundamental-cycle average loss calculation

Semiconductor power loss analysis plays a critical role in inverter system design, which not only gives guidance in the thermal design but also indicates the major contributors to the losses, which in turn helps to improve system efficiency. Two major parts, conduction loss and switching loss are included in semiconductor power loss analysis in this work. Due to the physical structure difference among various power devices, e.g., IGBTs, MOSFETs, and etc., the device loss models are slightly different, especially when the current and voltage are in the opposite direction. The following loss analysis presented in this work focuses on SiC MOSFETs, and the real-time loss model can be applied to various topologies. Most of the existing loss calculation methods are based on mathematical models, and they usually assume some ideal conditions, for instance, neglecting harmonics [7]. On the other hand, mathematical models are often case by case when gate control part varies. As a result, building a flexible generic real-time loss model benefits a lot in inverter design.

In this work, six CAS325M12HM2 1.2 kV SiC MOSFET modules are used in the design, in which main switches, $S_{a,1}$ and $S_{a,2}$, are configured in the standard half bridge structure, while middle switches, $S_{a,3}$ and $S_{a,4}$, are using common-source configuration. It is assumed that electrical characteristics of single MOSFET chip in both these two kinds of modules are the same. According to [8], the loss model is built in Matlab Simulink. The overall flow chart of real-time loss calculation is shown in Fig. 2.3. Both instantaneous power loss and average loss over a fundamental cycle can be generated by the model. The sampling period, which is set as 0.5 μs, should be set small enough to ensure the accuracy. The instantaneous voltage and current information are read directly from MOSFET block measurement ports.

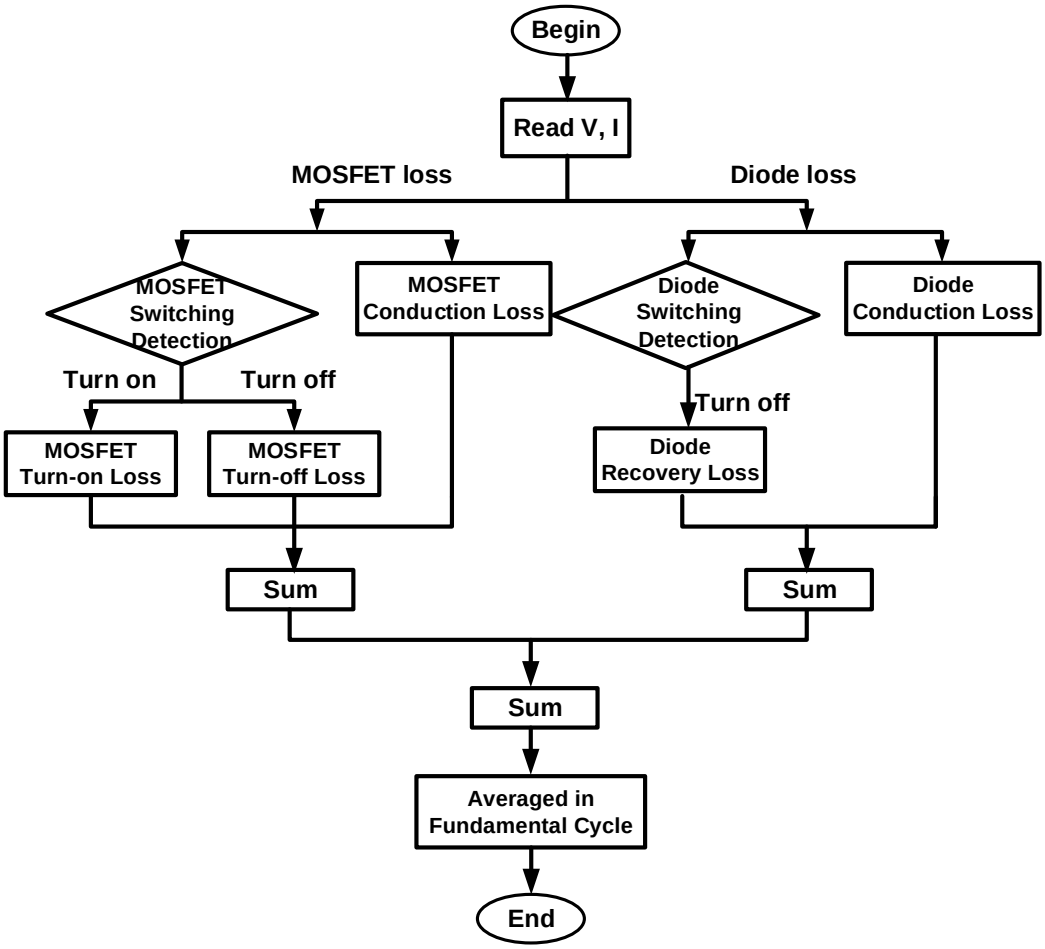



Figure 2-3 The overall flow chart of loss model.

### 2.3.1 MOSFETs

To determine the switching loss, the switching state should be detected firstly. Assume over two consecutive sampling periods, i.e., the kth and k-1th,

$$Ik > 0 \ \& \ Ik\text{-}1 = 0 \rightarrow \text{turn on}$$

$$Ik = 0 \ \& \ Ik\text{-}1 > 0 \rightarrow \text{turn off}$$

Once the switching state is detected, the turn-on and turn-off energy look-up table is used to determine the switching energy. Switching energy vs. $I_{DS}$ is usually tested at 25 °C and presented in the datasheet. Temperature conversion should be done using the figure of switching energy vs.

the junction temperature, Tj. Till now, the value of switching energy has been corrected by temperature and current, but not the voltage, e.g., $V_{DS\text{-}test}$ is 800 V. It can be assumed that Eon and Eoff are proportional with VDS, then equation (2-1), (2-2) can be used to calculate the final loss energy.

$$E_{on} = \frac{E_{on,I_k} \cdot V_{DS-test}}{V_{k-1}} \tag{2-1}$$

$$E_{off} = \frac{E_{off,I_{k-1}} \cdot V_{DS-test}}{V_k} \tag{2-2}$$

For conduction loss, due to the physical structure of MOSFETs, it can be regarded when current and voltage are in the opposite direction, current will go through MOSFET itself in steady state, not the antiparallel diode. So both drain-source/source-drain voltage vs. current in 1st and 3rd quadrant need to be considered. Look-up tables are built using the data when Vgs = 20 V, then conduction power loss can be calculated by equation (2-3).

$$P_{\text{con.}} = V_{DS} \cdot I_D \cdot S \tag{2-3}$$

where S represents switching state, either 0 or 1.

### 2.3.2 Diodes

For switching loss, diode turn-on loss is usually neglected since it is very small. Reverse recovery energy Err or reverse recovery charge Qrr is usually given in the datasheet. Based on these information, the switching state detection and switching energy correction can be done by previous the MOSFET loss calculation procedure. In this work, since SiC Schottky diodes have

already been anti-paralleled in the module used in this work, the diode reverse recovery loss is neglected.

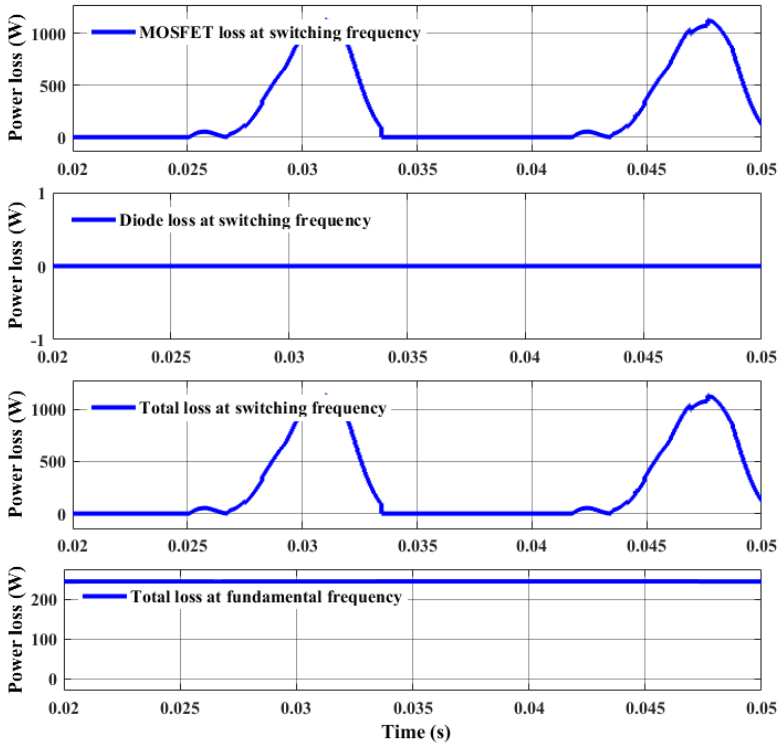
For conduction loss, the antiparallel diode characteristic in the datasheet is needed when Vgs = –5 V and at the actual operating temperature. Then conduction power loss can be calculated by

$$P_{\text{con.}} = V_{DS} \cdot I_D \cdot \overline{S} \tag{2-4}$$

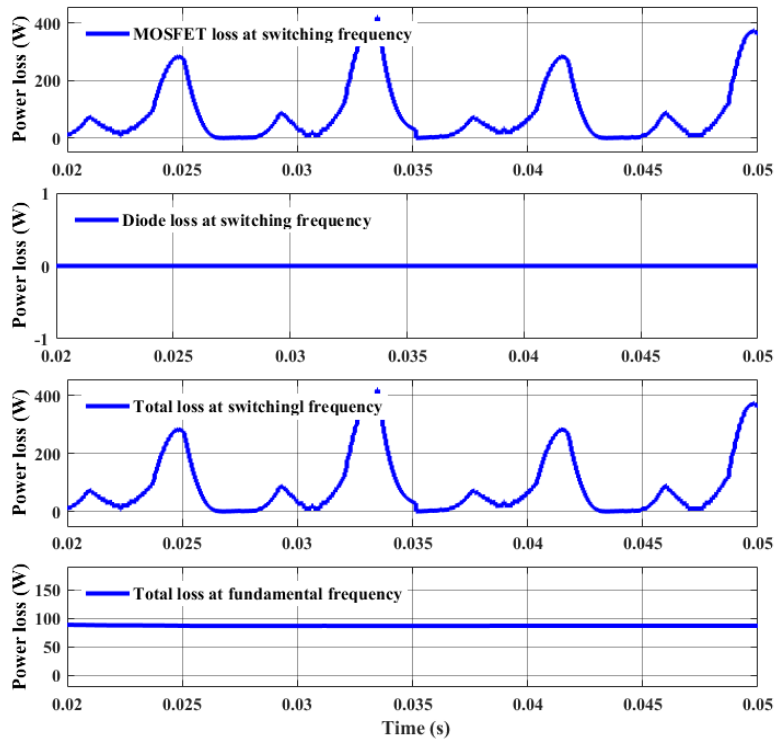
Real-time simulation results of power loss are shown in Fig. 2-4, in which both MOSFET and diode instantaneous losses are captured. Meanwhile, average power loss over the fundamental frequency is also given, which is very useful in thermal design. Due to the symmetry of modulation waveform, the loss on $S_{a,1}$ and $S_{a,2}$ are equal, similar for $S_{a,3}$ and $S_{a,4}$.

Table 2-1 Power loss simulation result on 700, 800, 900 V dc bus when $f_s$ = 20 kHz

| **Vdc (V)** | **m** | **Power loss on S1 (W)** | | | **Power loss on S3 (W)** | | | **3-phase total (W)** | **Percentage on system power (%)** |
|---|---|---|---|---|---|---|---|---|---|
| | | Sw. | Con. | Total | Sw. | Con. | Total | | |
| **700** | 0.97 | 47 | 198 | 245 | 6 | 79 | 85 | 1980 | 0.792 |
| **800** | 0.849 | 56 | 173 | 229 | 7 | 119 | 126 | 2130 | 0.852 |
| **900** | 0.754 | 61 | 153 | 214 | 8 | 149 | 157 | 2226 | 0.890 |




(a)




(b)

Figure 2-4 Simulation result of power losses when Vdc = 700 V, pf = 0.8, fs = 20 kHz for (a) $S_{a,2}$ in main switch bridge (b) $S_{a,4}$ in the middle switch bridge.

Table 2-2 Power loss simulation result on 700, 800, 900 V dc bus when $f_s$ = 40 kHz

| **Vdc (V)** | **m** | **Power loss on S1 (W)** | | | **Power loss on S3 (W)** | | | **3-phase total (W)** | **Percentage on system power (%)** |
|---|---|---|---|---|---|---|---|---|---|
| | | Sw. | Con. | Total | Sw. | Con. | Total | | |
| **700** | 0.97 | 93 | 194 | 287 | 13 | 76 | 89 | 2256 | 0.902 |
| **800** | 0.849 | 108 | 167 | 275 | 14 | 116 | 130 | 2430 | 0.972 |
| **900** | 0.754 | 122 | 149 | 271 | 16 | 146 | 162 | 2598 | 1.039 |

### 2.3.3 A case study of DC bus voltage

In this work, the design target is a 250 kW traction drive inverter with T-type topology with rated 480 Vrms line-to-line voltage and 300 Arms phase current. The modulation index needs to be tuned to coordinate the dc bus voltage. 700 V, 800 V, 900 V are selected to be compared in this work. The loss result is listed in Table 2-1. Switching frequency is set to be 20 kHz here, and power factor is 0.8. Due to the T-type operation characteristics, the conduction power loss on the diode is 0 with RL load. In addition to the aforementioned zero reverse recovery energy in SiC Schottky diodes. The total diode loss is assumed as 0. Therefore, only MOSFET loss data is given in Table 2-1.

From Table 2-1, it can be seen that 700 V DC results in the smallest total power losses, which is around 0.79% of the total inverter power, which means the 98% peak efficiency is achievable even considering other type losses. In addition, the modulation index has a critical impact on conduction loss. The conduction loss on $S_{a,1}$ is proportional to modulation index, but reversed for $S_{a,3}$. Here assumed middle bridge also use 1.2 kV module, but actually only half of the dc voltage rating is enough for middle bridge module. If 650 V device is used in middle bridge, the $R_{ds\text{-}on}$ will

be reduced significantly, and therefore the loss will also reduce. The tradeoff between power loss and loss distribution should also be noticed. Although the 900 V dc bus case has 12.42% more power loss than 700 V case, the loss distribution is more even on the two modules per phase. Finally, switching loss in middle bridges $S_{a,3}$ is almost negligible, conduction loss accounts for the major loss. This is mainly because when current and voltage is in the same direction, the MOSFET is "soft" switching. Here the small switching loss comes from the 0.8 power factor. The larger the power factor, the smaller the middle bridge switching loss.

### 2.3.4 A case study of switching frequency

Since CAS325M12HM2 can work at a switching frequency much higher than 20 kHz, the power loss at 40 kHz switching frequency is also compared in Table 2-2. As can be seen from the table, when switching frequency increases to 40 kHz, conduction loss decreases slightly, while switching loss increases dramatically. As a result, although higher switching frequency can give better output voltage quality, the tradeoff between output quality and power loss needs to be considered.

## 2.4 DC-link capacitor selection

Because the dc bus has stray inductance and resistance and the dc side current is pulsating, the dc-link capacitor is needed to solve potential EMI issues. Also, dc-link capacitor takes large portion of the overall inverter volume, the dc link capacitor selection will obviously affect the system power density. The dc-link capacitance depends on the energy of current ripple need to be absorbed and the rating of RMS current. DC-link current ripple includes not only load current at the fundamental frequency, but also current at PWM switching frequency and their harmonic contents.

According to [9], theoretical minimum dc-link capacitance in a three-phase 3-L converter is derived as equation (2-5). This calculation method is based on two main considerations: the maximum input power and the maximum allowable voltage fluctuation.

$$C_{d,\min} \geq \frac{\Delta P_{Max} \cdot T_d}{2V_{dc} \cdot \Delta V_{dc}} \tag{2-5}$$

where $\Delta P_{Max}$ is maximum power variation of inverter; $T_d$ is response time of voltage control loop (5 to 10 times of switching period); and $\Delta V_{dc}$ is maximum allowable voltage fluctuation.

In this work, $\Delta P_{Max}$ is set to 30% of the full power, and $\Delta V_{dc}$ is set to 15% of the dc bus voltage. Then the minimum dc-link capacitance is

$$C_{d,\min} \geq \frac{\Delta P_{Max}(30\% \times 250k) \cdot T_d(10/20k)}{2V_{dc}(700) \cdot \Delta V_{dc}(15\% \times 700)} = 255\mu F \tag{2-6}$$

From equation (2-7), it can be seen that to keep the capacitor working at allowable temperature; the RMS current needs to be predicted when selecting the capacitor [10].

$$T_c = T_a + I_{CAPRMS}^2 R_{ESR} R_{th,c-a} \tag{2-7}$$

where $T_c$ is the capacitor temperature, $T_a$ is the ambient temperature, $R_{ESR}$ is the equivalent series resistance of the capacitor, $R_{th,c\text{-}a}$ is the thermal resistance between capacitor and ambient.

The DC-link capacitor RMS current is related to PWM modulation index and power factor. According to [10], for the 3-L inverter, it can be derived as following

$$I_{AVG} = \frac{3}{4} I_N M \cos(\phi) \tag{2-8}$$

$$I_{RMS} = \sqrt{\frac{3I_N^2 M(\sqrt{3} + \frac{2}{\sqrt{3}}\cos(2\phi))}{4\pi}} \tag{2-9}$$

$$I_{CAPRMS} = \sqrt{I_{RMS}^2 - I_{AVG}^2} \tag{2-10}$$

where $I_N$ is the phase peak current.

Also, the capacitance, ESR, ESL are all changing with temperature and switching frequency, these need to be noticed during the capacitor selection. Due to safety concerns, it is better to select components' parameters larger than the calculated value. Since the temperature has a significant impact on the dc-link capacitor, proper thermal management approach needs to be considered, such as natural or forced air cooling or liquid cooling. In addition, attaching the capacitors directly to bus bar will be beneficial for cooling.

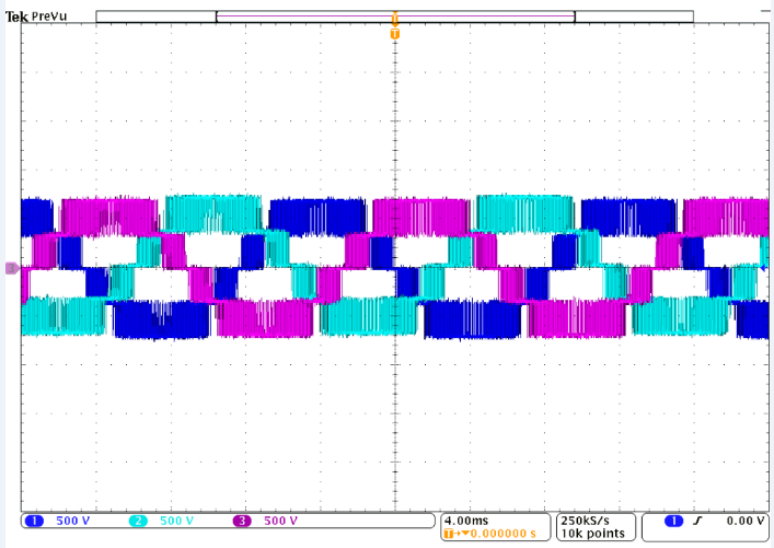
In this work, the calculated RMS current is 173 A, and 225 μF capacitance is needed. To give sufficient safety margin, six film capacitors FFVE6K0227K are selected, they are 3×220 μF in series.

## 2.5 Thermal management and bussing structure

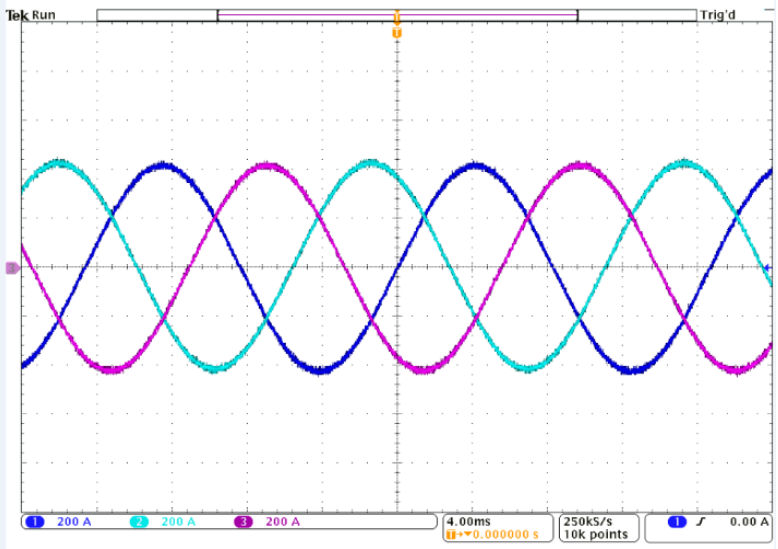
The loss calculation can guide the selection of proper thermal management approach, using proper heatsink or cold plate. Datasheet indicates that the limitation of power dissipation is related to module case temperature. After the average power loss over the fundamental period is known, it is obvious that main switch bridge has more heat dissipation than middle switch bridge. In this work, the maximum calculated power loss is 245×2 = 490W per module. This information can be translated to the maximum allowable case temperature. Based on the performance and cost, proper heatsink and cold plate can be determined.

For high power inverter, bus bar design is a significant part. Bus bar can withstand higher current than traditional cables, and also has much lower impedance, such that the reliability is enhanced. For dc bus bar, 400 circular mils/A is the traditional basis for the design of single conductor, and 5% more cross-sectional area of a conductor needs to be added for each additional conductor laminated into the bus structure [11]. Capacitance between different conductor levels is

preferred to be large, and inductance need to be small so that the overall impedance will be much smaller. This will benefit the noise attenuation. As a result, within the tolerance of voltage rating, the thickness of insulation layer should be as thin as possible. Skin effect needs to be considered for AC bus bar design.




(a)




(b)

Fig. 2-5 HIL simulation result when $V_{dc}$ = 700 V, pf = 0.8, fs = 20 kHz (a) line-to-line voltage (b) phase current.

## 2.6 Preliminary real-time simulation results

To evaluate the performance of the proposed T-type traction inverter, hardware-in-the-loop (HIL) simulation is performed. The HIL simulation is mainly used to validate the effectiveness of controller design. In this work, the control algorithms are implemented in the control platform designed using TI's TMS320F28379D dual-core microcontroller. As shown in Fig. 2-5, HIL studies have been performed to validate the capability of the controller to synthesize a 480 Vrms three-phase output voltage. The switching frequency is set 20 kHz, DC bus is 700 V, and power factor is simulated at 0.8. Both three-phase line-to-line voltage and phase current waveforms are given.

## 2.7 Conclusion

In this work, to design a compact 250 kW three-level T-type traction inverter, a holistic PE design approach is proposed trade the power density (kW/l) against SiC device type, the dc bus voltage, the switching frequency, and the heat dissipation method. The real-time loss calculation model is given in this work, which can be applied to other circuit topology. The dc-link capacitor selection approach is also briefly introduced. Thermal management and bus bar design are also important for the integrated high-power density inverter system design. Finally, preliminary HIL simulation study is performed to validate the performance of the designed control for the traction inverter system.

## Acknowledgment

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# CHAPTER 3

# DESIGN AND VALIDATION OF A 250 KW ALL SILICON CARBIDE HIGH-DENSITY THREE-LEVEL T-TYPE INVERTER



## 3.1 Abstract

This paper presents a comprehensive design and validation of a compact all silicon carbide (SiC) 250 kW T-type traction inverter with a power density of 25 kW/l and 98.5% peak efficiency. All the operation modes and switching transitions in a T-type phase leg are analyzed to model the semiconductor power losses over a fundamental cycle. Special attention has been paid to investigate the behavior and losses due to the reverse conduction of the SiC MOSFETs. Then a loss model is built based upon this analysis to calculate the device loss distribution and system efficiency, which is further used to determine the optimal switching frequency. In addition, detailed inverter system design and prototyping procedure, including the selection of SiC modules and dc-link capacitors, and the optimization of a 4-layer laminated busbar, are presented. In this work, the T-type phase leg is formed by a normal half bridge module and a common source module. The switching performance and losses in this configuration are different from two-level topology that only uses one SiC module. Therefore, the switching performance and the associated switching energy in each switch position are characterized using a custom clamped inductive load (CIL) test

setup designed for a T-type phase leg. The performance of the full power traction inverter prototype has been verified experimentally using pulse testing and continuous power testing.

## 3.2 Introduction

A sustained effort is required to realize the aggressive targets of electrification of heavy equipment, e.g., the heavy-duty and off-road vehicles [1], due to numerous emerging challenges, which are different from those in the automotive industry. Heavy equipment manufacturers are increasingly investing in the new generation power electronics technology [2], [3] to fulfill the high performance and reliability targets under harsh environments while reducing fuel consumption and staying cost-competitive. The potential solutions to enable high-density and high-efficiency traction inverters are still needed to reduce the volume and lower the cost of the electric or hybrid electric drivetrain. For instance, using the emerging wide-bandgap (WBG) devices, the inverter switching frequency can be moved into the medium frequency range, e.g., 10-25 kHz, but still as efficient as the state-of-the-art (SOA) silicon-based solution. The increase of the switching frequency can reduce the volume and cost of passive components significantly [4].

The conventional two-level inverter still dominates the market. However, a significant amount of effort from both industry and academia has gone into the research and development of new topologies to address the issues with the 2-L inverters, such as the harmonics in output voltage and relatively low efficiency at a higher switching frequency. In contrast to 2-L inverters, multi-level inverters can generate output voltage waveforms with lower harmonics to better resemble the sinusoidal references [5]-[7]. Moreover, lower *dv/dt* and electromagnetic interference (EMI) emissions also could be achieved using multi-level topology, such that bulky filters can be replaced by smaller volume and lower cost counterparts. Three-level (3-L) inverters, e.g., neutral-point-

clamped (NPC) inverters, active-NPC (ANPC), and T-type NPC are the most commonly used among multi-level inverter topologies [8]-[10]. Especially, in most of the high-power industrial applications, NPC is the most mature 3-L inverter topology since introduced in 1981 [11]-[13]. For lower power and low voltage applications, the NPC suffers from higher conduction loss due to the series connection of two devices in the conduction paths. In contrast, T-type topology has a smaller number of devices in the conduction path, which notably decreases the conduction loss. However, the switching losses in the T-type topology may be higher than that of the NPC due to higher voltage stress over a single switch position and devices with higher voltage rating are needed. These issues can be potentially addressed by emerging WBG devices.

In this work, silicon-carbide (SiC) MOSFETs are used, which has much less switching energy than the conventional silicon device. There are several reports on the development of T-type inverters using either silicon or SiC modules or even hybrid switches. Reference [14] presented a 10 kVA T-type converter using silicon IGBTs. A 100-kW single-phase T-type power electronics building block (PEBB) is reported in [15], in which both silicon and SiC modules were used to build hybrid switches. Addition cables and/or busbars are needed to build a three-phase system using single-phase PEBBs, which further complicates the design and may affect the overall system performance. Reference [16] reported a 60 kW five-level interleaved T-type inverter using SiC T-type modules, which however are not commercially available on the market.

In this paper, a compact three-phase 250 kW all-SiC T-type traction inverter is designed and prototyped to fully exploit the benefits of both SiC devices and the 3-L T-type topology. Each T-type phase leg consists of a half-bridge (HB) module and a common-source (CS) module. Both the HB and CS modules are commercially available. The schematic of the proposed traction inverter system is shown in Fig. 3-1, where S1 and S4 are the two switch positions in the HB

module, while S2 and S3 belong to the CS module. The optimal switching frequency in this design is 20 kHz, which selected based on the desired peak efficiency is 98.5%. The power density target is 25 kW/L. For a three-phase 3-L SiC inverter at this power rating, the optimization of the commutation loop, especially to ensure low parasitic inductance, is critical to the switching performance of SiC modules. The switching characteristics of a 2-L SiC MOSFET phase leg have been extensively studied [17]-[19]. However, the switching characteristics of the 3-L T-type phase leg have not been discussed in detail. Therefore, in this work, a clamped-inductive load (CIL) test setup is designed to capture the switching behavior of each switch position in a T-type configuration. A thorough analysis of the captured results is also presented.

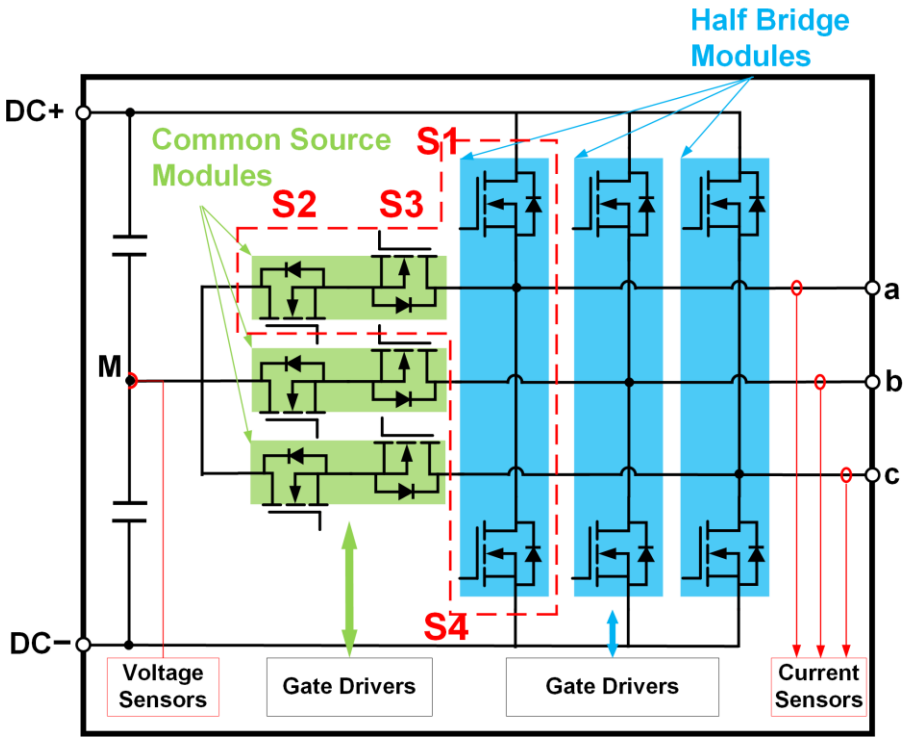



Fig. 3-1 A schematic of the proposed T-type traction inverter.

In this work, a comprehensive analysis of the operating modes and switching loops in a T-type phase leg is presented to derive the corresponding loss distribution. Then a real-time system loss model is built to determine the optimal switching frequency while meeting the efficiency target.

From CIL test results, the switching energy associated with turn-on, turn-off, and reverse recovery is calculated, which are used to further enhance the accuracy of the loss model. In addition to the investigation of a T-type phase leg, this paper also presents the design and optimization at the system level, in this context, the three-phase T-type inverter. To fulfill the design requirements, power modules, gate drivers, and dc-link capacitors need to be carefully selected. In addition, the laminated busbar and cold plate need to be optimized. The design flow and components selection procedure of a three-phase SiC inverter will provide design guidance for future applications.

## 3.3 Operating modes analysis and loss evaluation of a T-type phase leg

### 3.3.1 The operating modes of a T-type phase leg

The topology of a 3-L T-type converter is shown in Fig. 1. The switching states P, O, N of a T-type converter are defined in Table 3-1 [10]. These three switching states lead to three voltage levels of phase-neutral voltage $V_{xM}$, i.e., $+V_{dc}/2$, 0, and $-V_{dc}/2$, where $x = a, b, or\ c$. The operation of a T-type phase leg over one fundamental cycle can be divided into four intervals, as shown in Fig. 3-2. In this work, the direction of load current, i.e., $I_o$, is defined as positive when flowing from inverter output terminal to the load. Table 3-2 summarizes the relationship among the range of the output voltage phase angle, load current direction, voltage polarity in each interval, where φ is the load power factor (pf) angle.

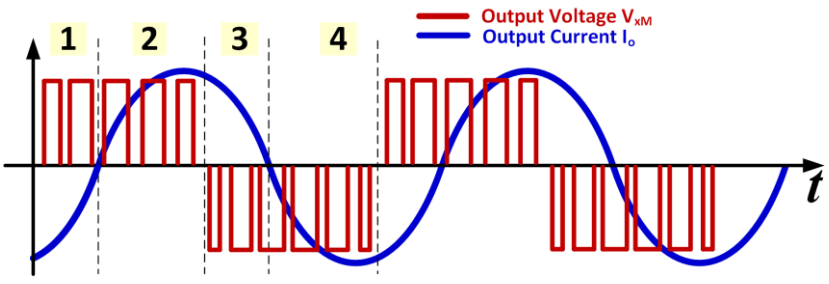



Fig. 3-2 An illustration of four operating intervals in a T-type phase leg.

Table 3-1 Switching states

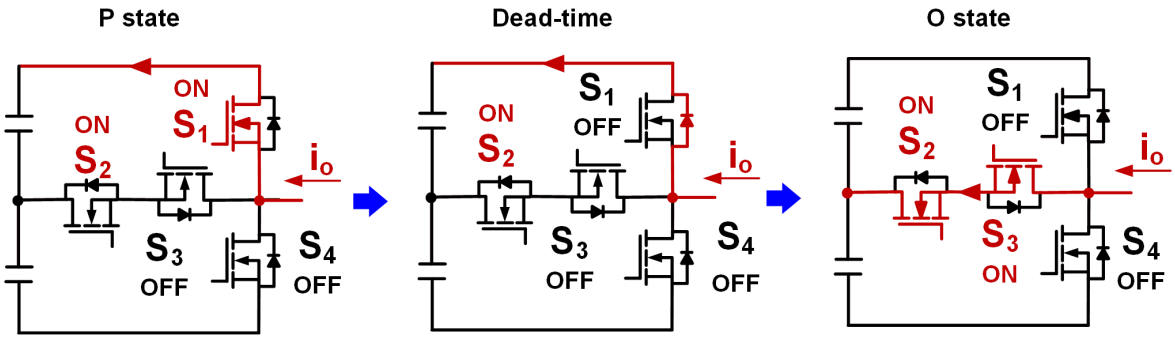
| State | $V_{xN}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
|---|---|---|---|---|---|
| P | $+V_{dc}/2$ | on | on | off | off |
| O | 0 | off | on | on | off |
| N | $-V_{dc}/2$ | off | off | on | on |

Table 3-2 Device conduction intervals

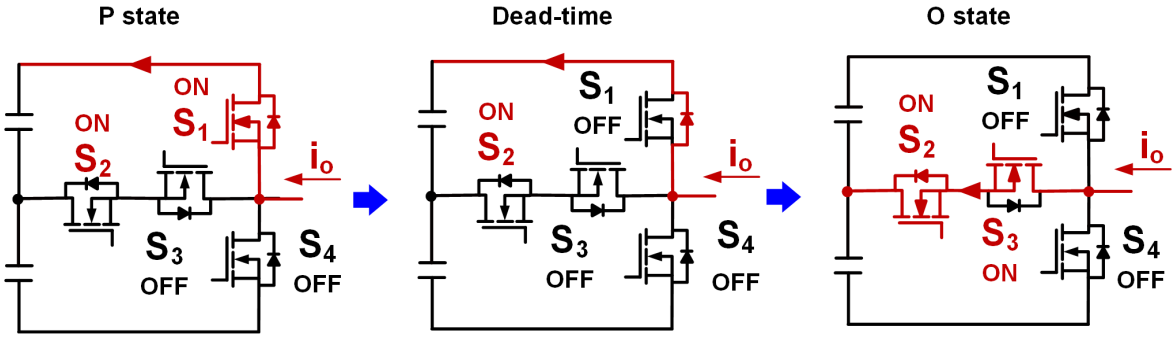
| Interval Number | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Phase Angle of $V_o$ | $[0, \varphi]$ | $[\varphi, \pi]$ | $[\pi, \pi + \varphi]$ | $[\pi + \varphi, 2\pi]$ |
| Current Direction | $I_o < 0$ | $I_o > 0$ | $I_o > 0$ | $I_o < 0$ |
| Voltage Polarity | $V_o > 0$ | | $V_o < 0$ | |

Figure 3-3. illustrates the switching transition from P state to O state during interval 1, where $I_o$ is negative, the fundament component of the line-to-neutral output voltage, i.e., $V_{xM}$, is positive and the actual line-to-neutral output voltage is switching between zero (O state) and $+V_{dc}/2$ (P state), $V_{dc}$ is the voltage across the entire dc link. In this case, the polarity of $V_{xM}$ and $I_o$ are the opposite. Therefore, SiC MOSFET in switching position S1 works in the reverse conduction mode or operates in the third quadrant. In the reverse conduction mode [20], switch position S1 may have two different loss mechanisms. When load current is low, only the MOSFET in switch position S1 carries the current, as shown in Fig. 3-3(a). When load current is high enough, which leads to the voltage drop across the MOSFET exceeds the threshold voltage of the antiparallel diode, the diode conducts and carries a portion of the load current, as shown in Fig. 3-3(b). For HB modules used in this work, the threshold current for the anti-parallel diode turn-on is temperature dependent. For instance, when using 18 V gate-source voltage, at 25 °C, the anti-parallel diode turns on when source current is higher than 250 A, while at 150 °C, the anti-parallel

diode turns on when source current is higher than 130 A. Therefore, the conduction loss at high current can be a critical contributor for the loss in the presented design.




(a)




(b)

Fig. 3-3 The operating mode when $V_{xM} > 0$ and $I_o < 0$ with (a) low load current and (b) high load current. (S1 to S4 are the four switch positions in a T-type phase leg. The ON or OFF associated with each switch position stands for the gate signal in that particular operating mode.)

The IGBT-based T-type converter loss analysis has been developed in [10], [21], while this work provides the SiC MOSFETs based T-type converter loss analysis. Using Fig. 3-3(a) as an example, the 1st operating mode is in P state, i.e., $V_{xM}$ is positive, and the load current flows from the source to the drain of the MOSFET in S1, which therefore works in the reverse conduction mode having a reverse conduction loss, i.e., $E_{con\_R}$. Although the turn-on gate signal is applied to the S2, there is no current flowing through the CS module, since S3 is in the OFF state. The gate signals applied to S1 and S3 are always complimentary with dead-time inserted to avoid short

through. The 2nd operating mode is during the dead-time, where both S1 and S3 are in the OFF states; the load current goes through the antiparallel diode in S1, i.e., D1. During the transition from the 1st operating mode to the 2nd one, the load current shifts from the MOSFET in S1 to its anti-parallel diode. Due to the conduction of the anti-parallel diode, the voltage across the MOSFET is close to zero when it turns off. Therefore, the turn-off process of MOSFET is close to the zero voltage switching (ZVS), and the turn-off loss in the MOSFET is negligible. Then once the turn-on gate signal is applied to S3, the current is gradually commutated from the D1 to the CS module, which is the clamping leg. In the very end of this operating mode, D1 has a reverse recovery with an associated loss, i.e., Err. In the 3rd operating mode, which is an O state operation, $I_o$ is still negative. S3 works in the forward conduction mode, while S2 operates in reverse conduction mode. Since the turn-on gate signal is always applied to S2 during the interval 1, there is no switching loss in S2. But there are conduction losses in both S2 and S3 and the switching loss in S3 in the third operating mode. As a summary for the switching transition from P state to O state during interval 1, the semiconductor losses here are distributed among S1, S2, and S3, including the reverse recovery loss ($E_{rr}$) and reverse conduction loss ($E_{con\_R}$) on switch position S1, reverse conduction loss ($E_{con\_R}$) on switch position S2, switching loss ($E_{sw}$) and forward conduction loss ($E_{con\_F}$) on switch position S3. The same approach can be applied to analyze the high current case shown in Fig. 3-3(b). However, the analysis could be more complicated, since during P state, both MOSFET and antiparallel diode in S1 are in the ON state.

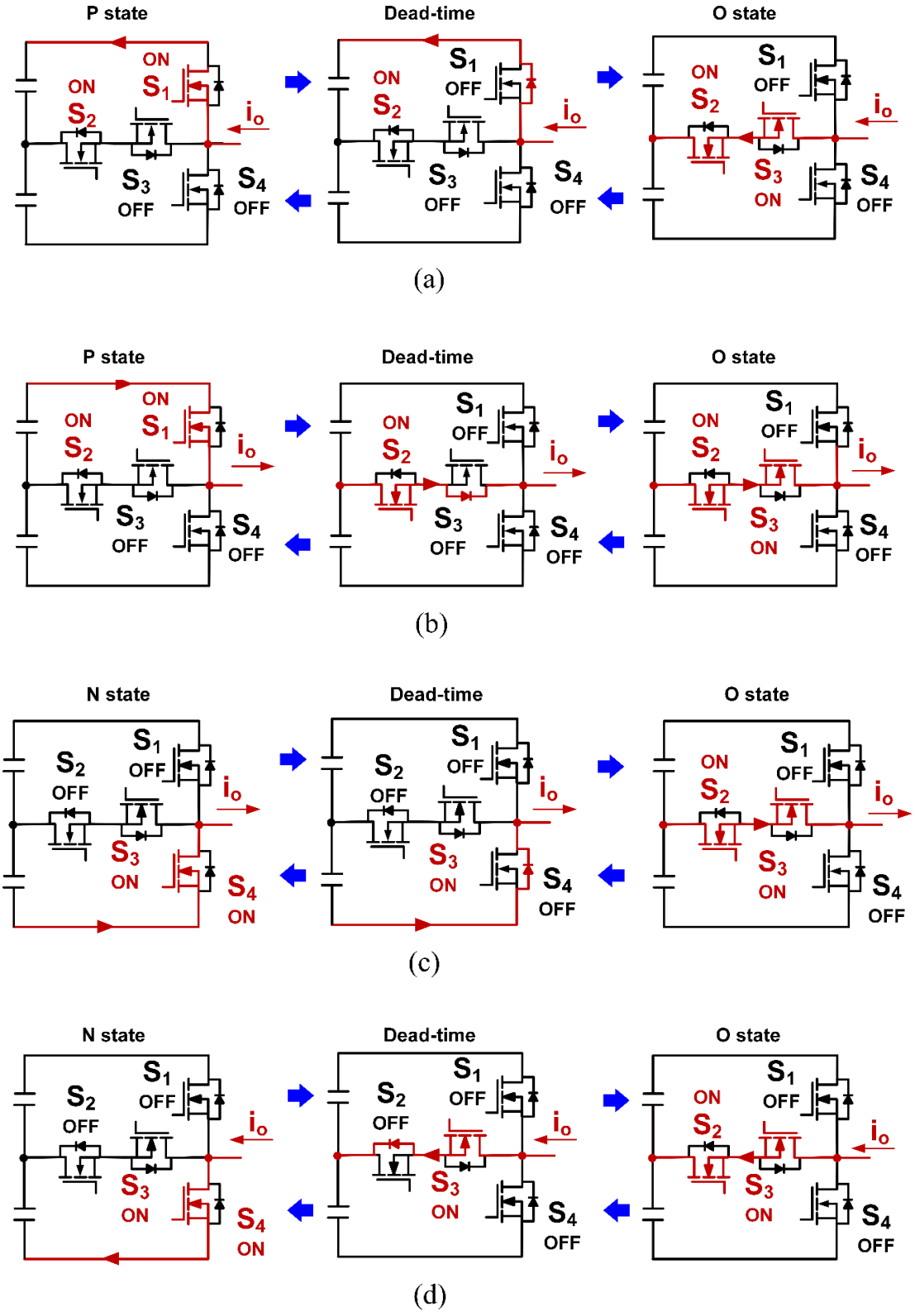



Fig. 3-4 An illustration for the switching transitions when (a) $V_{xM} > 0$ and $I_o < 0$; (b) $V_{xM} > 0$ and $I_o > 0$; (c) $V_{xM} < 0$ and $I_o > 0$; and (d) $V_{xM} < 0$ and $I_o < 0$.

Table 3-3 Device power loss distributions

| Time interval | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| S1 | $E_{rr} + E_{con\_R}$ | $E_{on} + E_{off} + E_{con\_F}$ | - | - |
| S2 | $E_{con\_R}$ | $E_{con\_F}$ | $E_{on} + E_{off} + E_{con\_F}$ | $E_{rr} + E_{con\_R}$ |
| S3 | $E_{on} + E_{off} + E_{con\_F}$ | $E_{rr} + E_{con\_R}$ | $E_{con\_R}$ | $E_{con\_F}$ |
| S4 | - | - | $E_{rr} + E_{con\_R}$ | $E_{on} + E_{off} + E_{con\_F}$ |

Table 3-4 Device switching loss distributions

| Switching Transition | Switching Loss ($E_{sw}$) $i_0 \geq 0$ | Switching Loss ($E_{sw}$) $i_0 < 0$ |
|---|---|---|
| P → O | $E_{off, S1}$ | $E_{rr, S1}$, $E_{on, S3}$ |
| O → P | $E_{rr, S3}$, $E_{on, S1}$ | $E_{off, S3}$ |
| N → O | $E_{rr, S4}$, $E_{on, S2}$ | $E_{off, S4}$ |
| O → N | $E_{off, S2}$ | $E_{rr, S2}$, $E_{on, S4}$ |

The operating modes in all four time intervals are summarized in Fig. 3-4 given low load current. The procedure for interval 1 presented earlier can be used for the analysis of other intervals. One thing should be noticed that, as shown in Fig. 3-4(a), from O state to P state, when the MOSFET is S1 is turning on, due to the freewheeling of D1, the voltage across the MOSFET is close to zero. This leads to a turn-on process similar to zero voltage switching. Therefore, the turn-on switching loss for S1 can be ignored in this case. Similarly, as shown in Fig. 3-4(b), from P state to O state, when the MOSFET in S3 is turning on, due to the freewheeling of the antiparallel diode in S3, the switching loss for S3 can be ignored. A summary of the power losses associated with each switch

position is presented in Table 3-3, which can provide a detailed power loss distribution and can guide the loss modeling and converter efficiency analysis. In addition, the specific switching loss during each switching transition are summarized in Table 3-4.

### 3.3.2 Semiconductor loss evaluation

Semiconductor power losses account for a large portion of the overall system loss. Therefore, a comprehensive device loss analysis is critical not only for the system efficiency estimation but also the thermal design. In this section, the power loss of the proposed T-type inverter is calculated. The data of the conduction and switching losses are extracted from datasheet provided by the manufacturer.

The conduction loss of a MOSFET [20] in the 1st quadrant or 3rd quadrant can be expressed as (1) and (2), respectively

$$P_{con\_F} = I_D^2 \cdot R_{DS(on)\_F} \tag{3-1}$$

$$P_{con\_R} = \begin{cases} I_D^2 \cdot R_{DS(on)\_R}, & I_D \le I_{SC} \\ I_D^2 \cdot R'_{DS(on)\_R} + V_{TH} \cdot I_D, & I_D > I_{SC} \end{cases} \tag{3-2}$$

where $I_D$ and $I_{SC}$ are the MOSFET current and the threshold current, respectively; $R_{DS(on)\_F}$ and $R_{DS(on)\_R}$ are the on-state resistance of the device; $R'_{DS(on)\_R}$ and $V_{TH}$ are the equivalent resistance and voltage source of the MOSFET and diode parallel circuit, respectively.

The switching loss can be regarded as proportional to the test voltage of the device [21]. The turn-on loss $E_{on}$ and turn off loss $E_{off}$ can be approximated as equation (3-3) and (3-4), respectively.

$$E_{on} = \frac{E_{on0} \cdot V_{DS-test}}{V_{DS0}} \tag{3-3}$$

$$E_{off} = \frac{E_{off\,0} \cdot V_{DS-test}}{V_{DS0}} \tag{3-4}$$

where, $E_{on0}$ and $E_{off\,0}$ are turn on and turn off losses at the voltage specified in the datasheet, respectively; $V_{DS0}$ is the voltage used in the switching characterization process for the datasheet; $V_{DS-test}$ is the actual voltage in the application.

The diode reverse recovery loss can be expressed as,

$$E_{rr} = \frac{E_{\mathrm{rr}0} \cdot V_{DS-test}}{V_{DS0}} \tag{3-5}$$

where $E_{\mathrm{rr}0}$ is the diode reverse recovery loss at the voltage specified in the datasheet. For SiC diode, the reverse recovery loss can be ignored when compared to other losses.

Reference [22] presented a detailed real-time loss modeling approach for the MOSFET-based T-type inverter using Matlab Simulink with case studies showing the power loss and system efficiency of a 250 kW T-type traction inverter with 700 V, 800 V, 900 V bus voltage at 20 kHz and 40 kHz switching frequency. In this paper, the average power losses of all the switch positions in a T-type phase leg over a fundamental cycle is shown in Fig. 3-5, which is simulated based on 250 kVA output power, 0.8 load power factor, 700 V dc bus, and 20 kHz switching frequency. It has been observed that the majority of losses come from conduction loss, and the total loss is not evenly distributed among the four switch positions, i.e., HB module has much higher losses than the CS module. When determining the flow rate of the cold plate, more attention needs to be paid to HB module to ensure its junction temperature can be limited within the safe operating range.

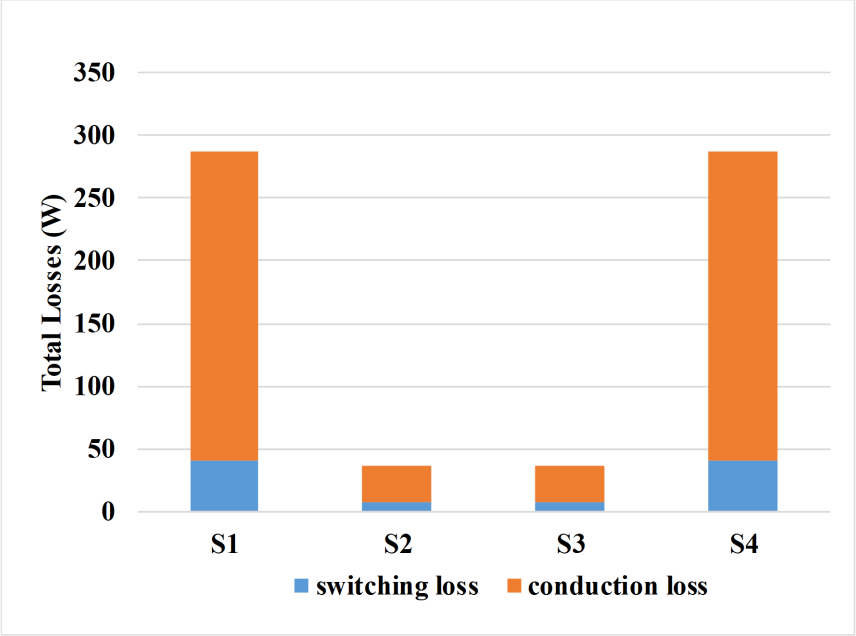



Fig. 3-5 The distribution of the average power losses with a 0.8 power factor load.

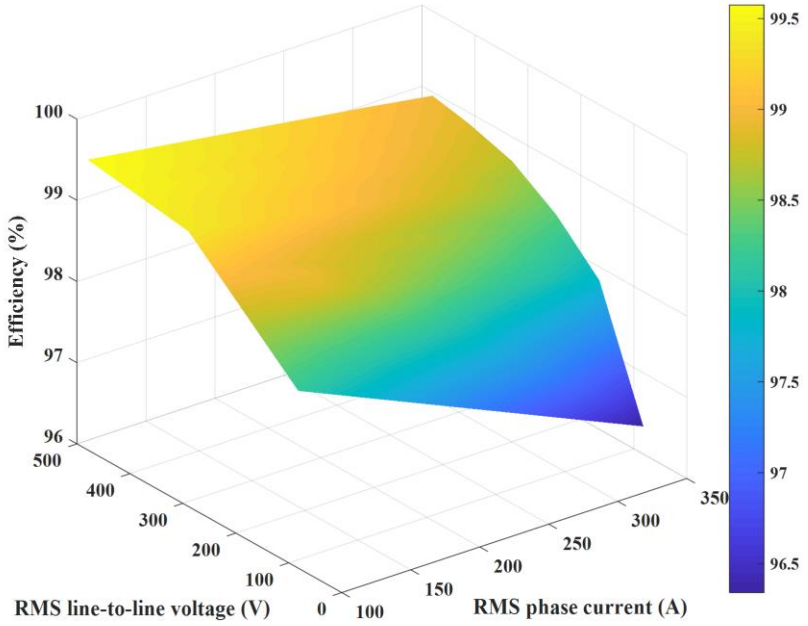



Fig. 3-6 The efficiency map obtained using simulation-based loss model.

Figure 3-6 shows the efficiency map of the traction inverter on different operation points. As can be seen, higher efficiency is achieved under high output voltage and relatively low phase current scenarios, due to the reduction of conduction loss. All the operation points on the efficiency map are greater than 98.5%, though considering the losses in other system components, e.g., the capacitor bank, gate drivers, filters, etc., the efficiency of the overall traction inverter system will be slightly lower.

## 3.4 Switching characterization of SiC modules in a T-type configuration

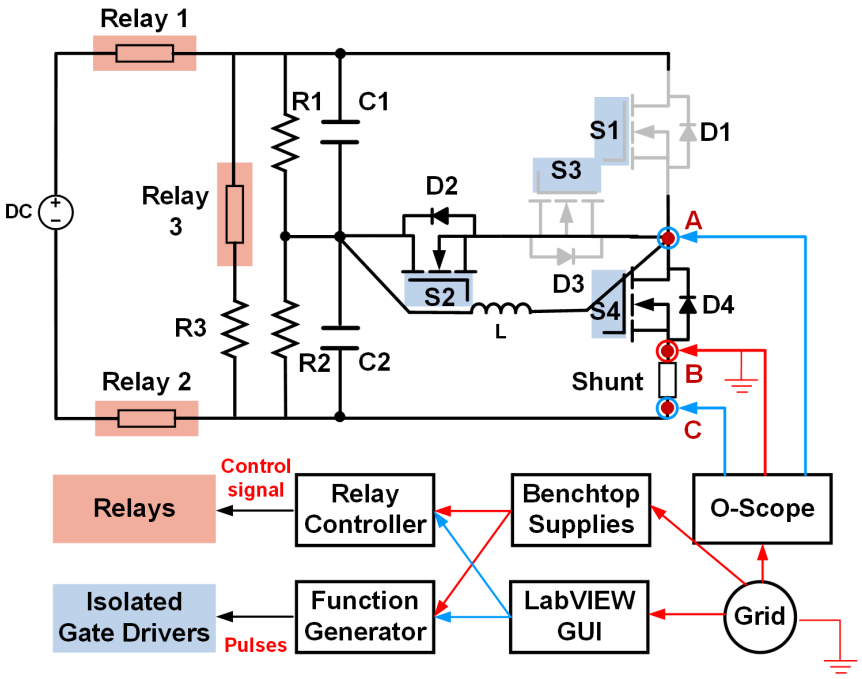
### 3.4.1 Clamped inductive load (CIL) test

To fully understand the switching behavior of modules in a T-type configuration, performing CIL tests for all switch positions is the most straightforward approach. In addition, due to the use of T-type topology, the loss at each switch position may not be identical to that in the datasheet, which is characterized using an individual module. In this work, a CIL test setup for a T-type phase leg is developed. Comprehensive CIL tests were performed to evaluate switching characteristics and collect loss information.

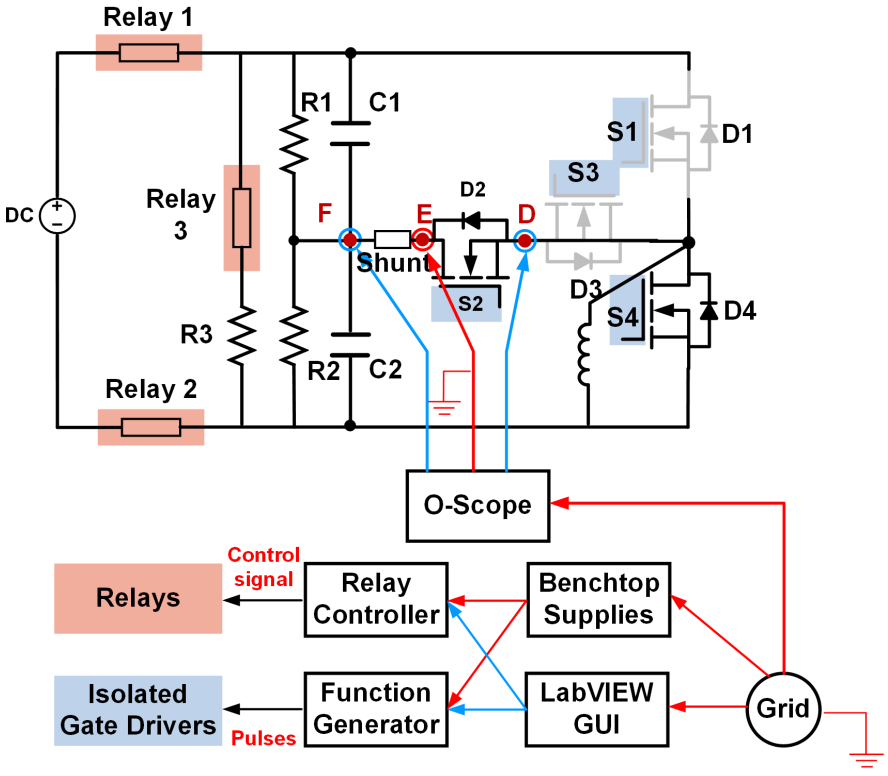
The schematics of the CIL tests for different switching positions are shown in Fig. 3-7, in which S1 and S4 are the top and bottom switch positions in the HB module, while S2 and S3 are switch positions in the CS module. The schematic of the CIL test for HB module is shown in Fig. 3-7(a) and gate pulses are applied to S4 in the HB module, which is the device under test (DUT), and the body diode of S2 in the CS module is the freewheeling diode. In this test, the gate signals for S1 and S2 are always low, while the gate signal for S3 is always high. In this way, D2 and S4 form the standard configuration for a CIL test. The schematic of the CIL tests for CS modules is shown in Fig. 3-7(b). Gate pulses are applied to S2 in the CS module, which is the DUT, and the

anti-parallel diode of S4 in HB module is the freewheeling diode. In this test, the gate signals for S1 and S4 are always low, while the gate signal for S3 is always high.

The designed printed circuit board (PCB) based CIL test setup is shown in Fig. 3-8. The PCB was optimized to minimize the loop parasitic impedances. The load used for CIL test is an air-core inductor with an inductance of 40.2 μH. The modules are mounted on the bottom of the PCB. A 2.5 mΩ bar strap type current viewing resistor (CVR) is chosen for drain-source current measurement instead of other measurement methods, e.g., Rogowski coil, current transformer, etc., due to its high bandwidth and convenience. Drain-source and gate-source voltage are measured by differential probes THDP0200. Since this is a CIL setup for a T-type phase leg, two sets of DC-link capacitors are connected in series, and voltage divider resistors are used to provide a neutral point. All controls are implemented in a dSPACE MicroLabBox. In this work, the gate resistance on the gate driver are different for turn-on and turn-off process, i.e., turn-on gate resistance $R_{gon}$ is 5 Ω while turn-off gate resistance $R_{goff}$ is 2.5 Ω.




(a)




(b)

Fig. 3-7 Schematic of CIL test for (a) HB module and (b) CS module.

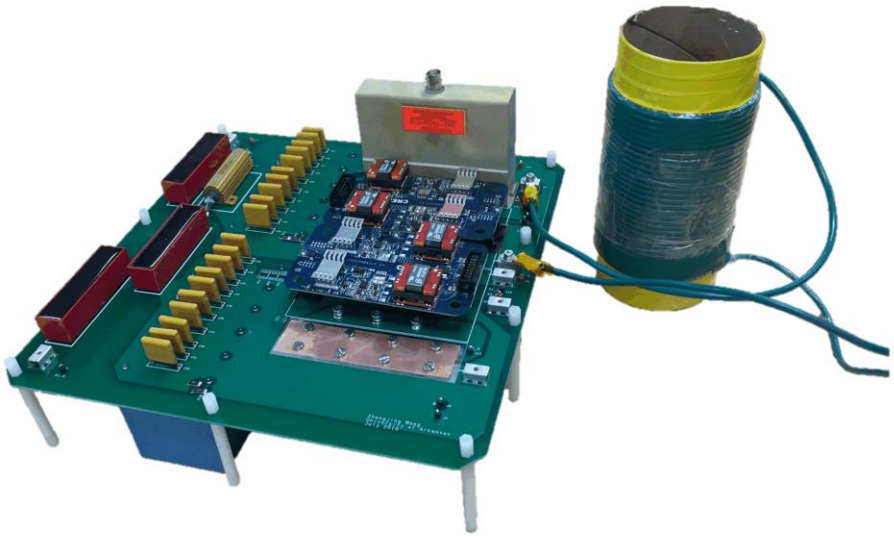


Fig. 3-8 The CIL test setup for a T-type phase leg.

To ensure an accurate loss calculation, current and voltage alignment is performed on probe channels using the de-skew functions on the oscilloscope. For instance, the 3 ns mismatch is compensated on an isolated voltage probe. The CIL test results presented in this work were collected at the room temperature, with 700 V dc-link voltage and varying the load currents from 50 A up to 450 A. One set of typical CIL test results are shown in Fig. 3-9, when the load current is 150 A. Fig. 3-10 shows the switching energy $E_{sw}$ and reverse recovery energy $E_{RR}$ calculated for the switch positions in both HB and CS modules based on the measured waveforms. As can be seen, both turn-on energy $E_{on}$ and turn-off energy $E_{off}$ increase with the load current, and the switching loss of the CS module is larger than that of the HB module. It should be noted that reverse recovery energy $E_{RR}$ is pretty small for both body diode and the anti-parallel diode.

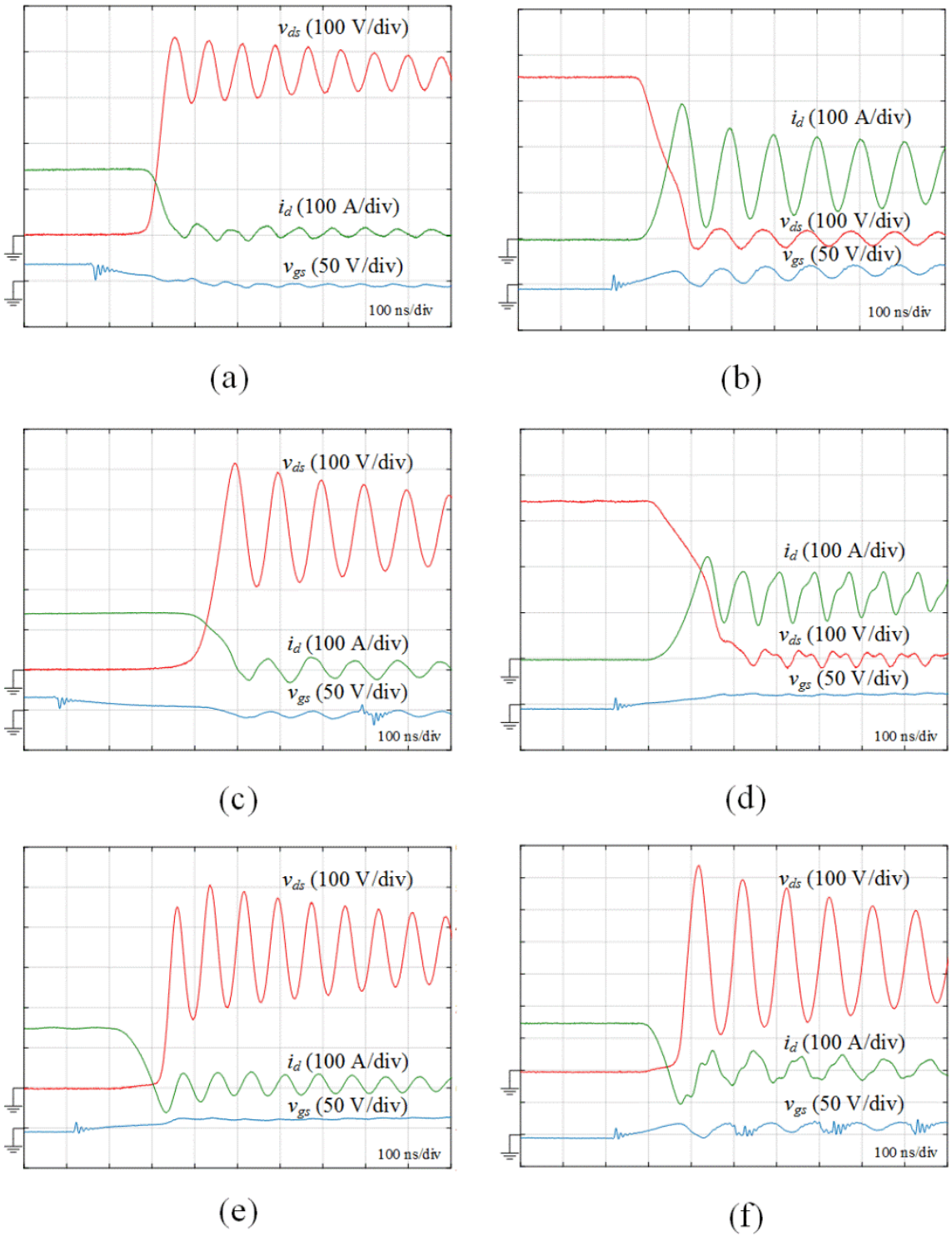



Fig. 3-9 Switching waveforms of the T-type modules at $V_{dc}$ = 700 V, $I_{ds}$ = 150 A with $R_{gon}$ = 5 Ω and $R_{goff}$ = 2.5 Ω: (a) turn-off of S4, (b) turn-on of S4, (c) turn-off of S2, (d) turn-on of S2, (e) turn-off of D4, and (f) turn-off of D2.

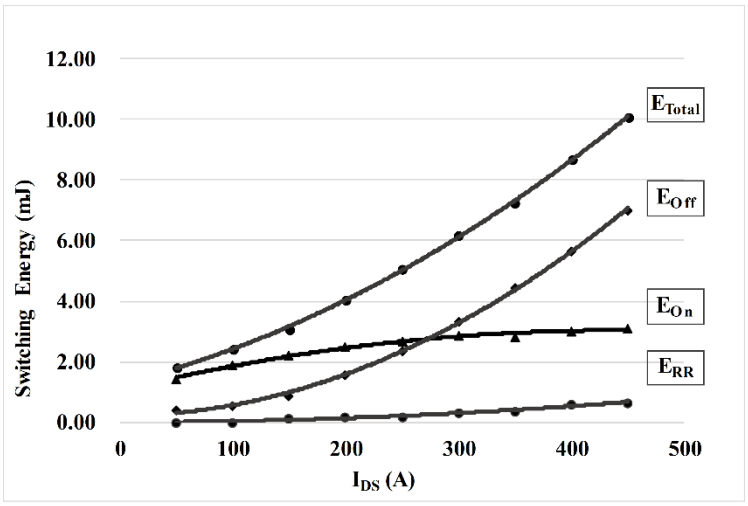
### 3.4.2 Switching waveform and switching energy analysis

As the results shown in Fig. 3-9, both $v_{ds}$ and $i_{ds}$ have much higher oscillations comparing to the typical 2-L CIL test results using only one half bridge power module. One of the major reasons is the higher loop inductance in the CIL setup for a T-type phase leg. The equivalent circuits for the 2-L (Fig. 3-11(a)) and 3-L (Fig. 3-11(b)) double pulse test are shown below. The capacitors shown in the figures represent the high-frequency decoupling capacitors, which has negligible parasitic inductance. $L_{dc+}$, $L_{dc-}$, $L_{dcM}$, $L_{ac}$, $L_{module}$ represent parasitic inductance on PCB dc+ layer, dc- layer, dc middle layer, ac layer and stray inductance from modules, respectively. As can be seen from the following figure blue shaded area, the 2-L and 3-L current commutation loops are similar to each other. The difference is that the loop inductance in the 3-L double pulse test is larger than that for 2-L. The extra inductance mainly comes from the extra module and Lac, which is L4 in the Fig. 3-11 (c) and (d). Since v = L·di/dt, when loop inductance L is increased, the magnitude of the voltage overshoot and oscillation are increased accordingly. To verify the correctness of this hypothesis, a simulation for CIL test is conducted in LTSpice. As shown in Fig. 3-11 (c) and (d), except the L4 in (d) is 10 nH larger than that in (c), all other parameters are the same. Fig. 3-11(e) and (f) are the simulation results obtained using (c) and (d), respectively. Obvious oscillation in both $v_{ds}$ and $i_{ds}$ can be observed in (f), with much higher voltage overshoot and longer settling time.

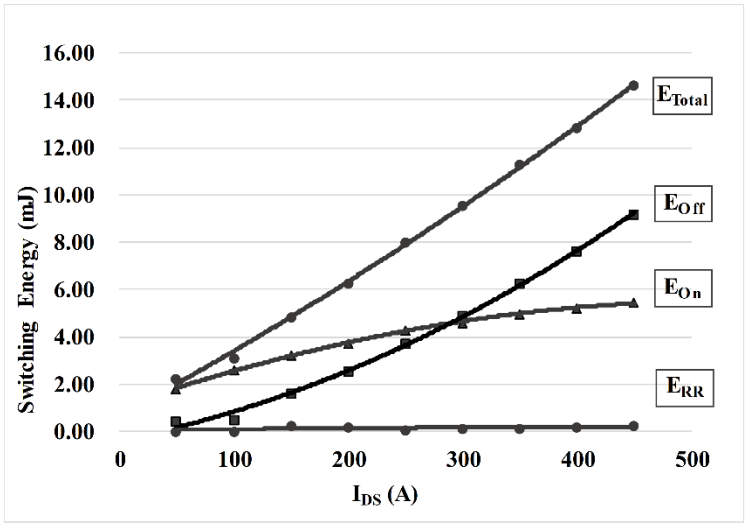
During turn-off transient, there is a positive *di/dt* going through the freewheeling diode and a negative *di/dt* at the same value going through the MOSFET, leading to a switching commutation loop. The increase of the stray inductance in any part of the switching loop, which consists of the freewheeling diode, the MOSFET, dc-link capacitor and PCB traces, will result in an increase in the total loop inductance. Because of the large *di/dt*, a voltage drop will be induced on the loop

inductance, which further leads to large voltage overshoot in $V_{ds}$. The loop inductance also resonates with the MOSFET output capacitance, which contributes to the ringing as well. Due to the MOSFET output capacitor, current oscillation will be proportional to *dv/dt*. The same principle is also applied to the turn-on transient. In addition, larger loop inductance leads to more energy stored during the switching transients, which increases the settling time. Comparing the switching waveforms of various switch positions presented in Fig. 3-9, it can be seen that the voltage overshoot and oscillation is larger on the switches in the CS module than that on the switches in the HB module during turn-off transient. Meanwhile, the current overshoot and oscillation are more severe on the switch positions in the HB module than that on the switch positions in the CS module during turn-on transient.

When comparing to the datasheet, the $E_{off}$ presented in Fig. 3-10 is larger than the datasheet value, while $E_{on}$ is smaller than the datasheet value. One of the major factors for this phenomenon is still the increase of the loop stray inductance. According to [23], for a SiC MOSFET, a larger stray inductance will lead to less turn-on loss and larger turn-off loss, which results in a reduced overall switching loss. This is actually a trade-off between device voltage stress and switching loss due to the loop parasitic inductance.




(a)




(b)

Figure 3-10 Measured switching energy of T-type module at $V_{dc}$ = 700 V, with $R_{gon}$ = 5 Ω and $Rg_{off}$ = 2.5 Ω: (a) S4, (b) S2.

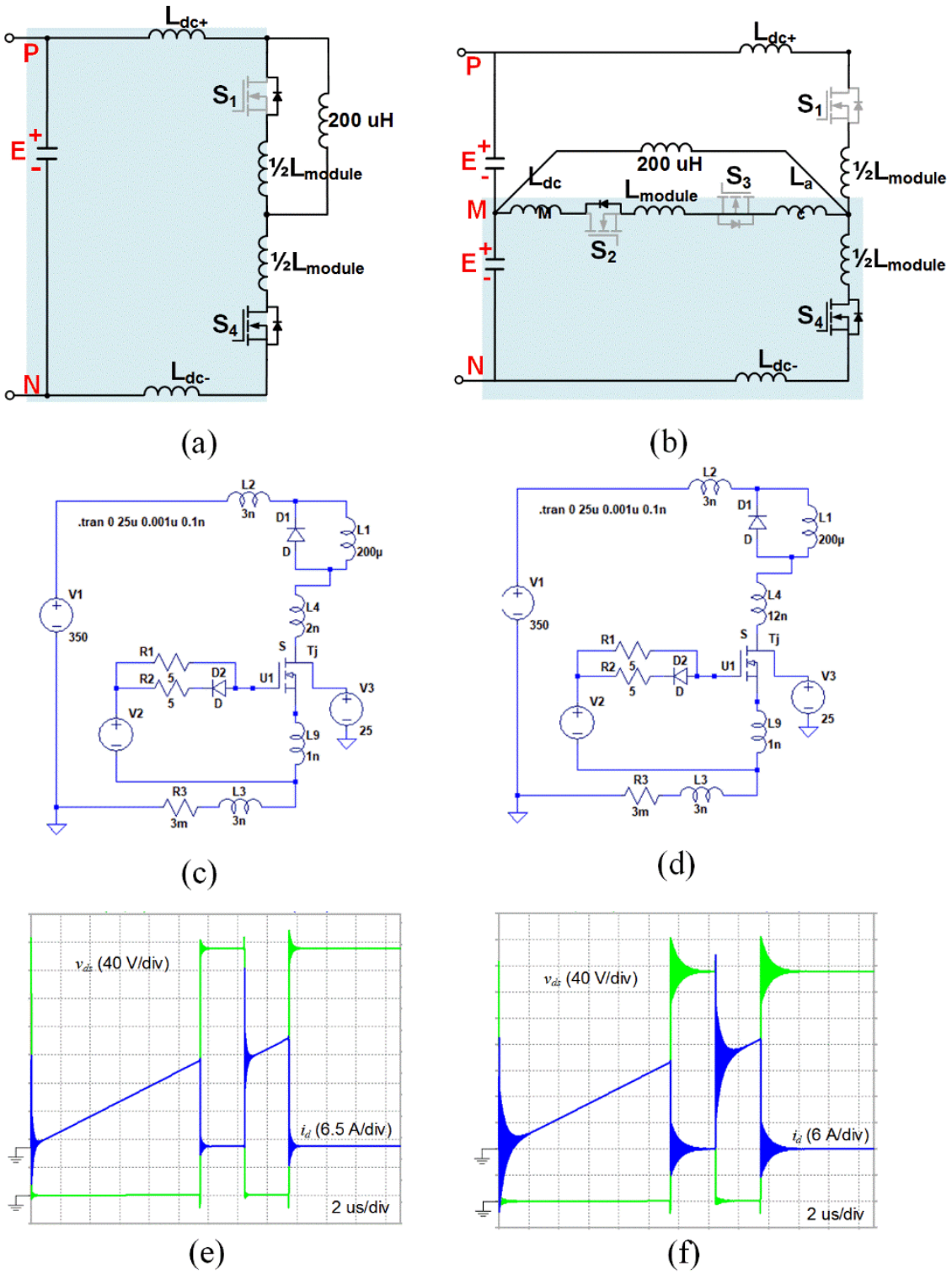



Figure 3-11 Equivalent circuit of DPT for (a) an HB module and (b) a T-type phase leg, (c) and (d) are the corresponding simulation circuit, (e) and (f) are corresponding switching waveforms, respectively.

## 3.5 Full power prototype

### 3.5.1 SiC modules and gate drivers

As mentioned in the introduction, all SiC MOSFET power modules are used in this paper. Due to the lack of SiC T-type modules, to build a T-type phase leg using commercial off-the-shelf (COTS) modules, there are two approaches. One is using three HB modules, as shown in Fig. 3-12(a). In this configuration, the clamping leg is comprised of two HB modules. The other method is using one HB module and one module in CS or the common-drain (CD) configurations, as shown in Fig. 3-12(b). Compared to the first approach, using a CS or CD module will significantly reduce the hardware cost and increase the power density.

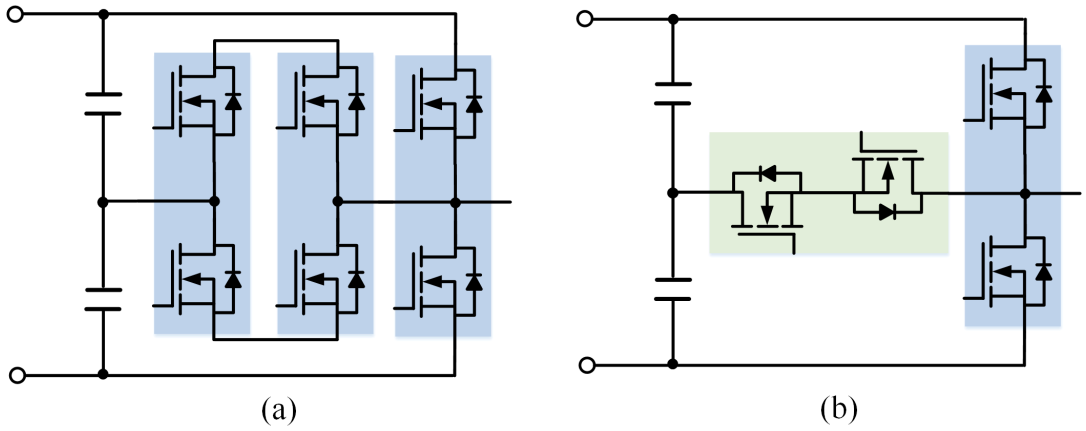



Figure 3-12 T-type configuration built by (a) three HB modules (b) one HB module and one CS module.

In this paper, the CS module is selected as the clamping leg. As discussed in [10], the switch position in the HB module needs to withstand the full DC bus voltage, while the switch position in the clamping leg only needs to withstand half of the DC bus voltage. The DC bus voltage used in this work is 700V. Further considering the voltage overshoot during the switching transient, 1200 V HB SiC MOSFET module and 900 V CS SiC MOSFET module are chosen. To drive the modules, a COTS dual-channel differential isolated gate diver from Wolfspeed is used, which

includes two separate channels to drive both switch positions in a module. The configuration of the gate driver for CS module is slightly different from that for the HB module, since both switch positions may need to be ON at the same time, which should be prohibited in HB module to avoid the short through.

### 3.5.2 DC-link capacitor

The volume of the dc-link capacitors usually takes a large portion of the volume of the overall inverter system. Therefore the design and selection of proper dc-link capacitor are critical to the volumetric power density of the inverter. In this work, two important factors are considered, i.e., the minimum capacitance and the rating of root-mean-square (RMS) current. The minimum capacitance in the dc-link [24] in a three-phase 3-L converter can be expressed as

$$C_{d,\min} \geq \frac{\Delta P_{Max} \cdot T_d}{2V_{dc} \cdot \Delta V_{dc}} \tag{3-6}$$

where $\Delta P_{Max}$ is maximum power variation of the inverter; $T_d$ is the response time of the voltage control loop (5 to 10 times of a switching period); $\Delta V_{dc}$ is maximum allowable voltage fluctuation. In this work, $\Delta P_{Max}$ is set to be 30% of the full power, and $\Delta V_{dc}$ is set to be 15% of the dc bus voltage. Therefore the minimum dc-link capacitance is

$$C_{d,\min} \geq \frac{\Delta P_{Max}(=30\% \times 250\text{kW}) \cdot T_d(=10/20\text{kHz})}{2V_{dc}(=700V) \cdot \Delta V_{dc}(=15\% \times 700V)} = 255\ \mu\text{F} \tag{3-7}$$

The DC-link capacitor RMS current is a function of the modulation index, power factor, and not only the load current at the fundamental frequency but also current at switching frequency and their harmonic contents. According to [25], for a 3-L inverter, it can be derived as follows

$$I_{AVG} = \frac{3}{4} I_N M \cos(\phi) \tag{3-8}$$

$$I_{RMS} = \sqrt{\frac{3I_N^2 M(\sqrt{3} + \frac{2}{\sqrt{3}}\cos(2\phi))}{4\pi}} \tag{3-9}$$

$$I_{CAPRMS} = \sqrt{I_{RMS}^2 - I_{AVG}^2} \tag{3-10}$$

where $I_N$ is the phase peak current. In this work, the calculated RMS current is 173 A, and 225 μF capacitance is needed. Since the SiC devices can efficiently operate at a higher switching frequency, the capacitance needed for dc-link can be dramatically reduced [1]. This can potentially lead to a significant increase in volumetric power density since the capacitors in the dc link usually take 1/3 or even more space in a traction inverter.

### 3.5.3 Laminated busbar

To achieve low impedance and high reliability, a laminated bus bar is designed in this work to withstand high current. As shown in Fig. 3-13(a), there are four different voltage levels in busbar, i.e., DC+, DC-, DC0, and AC. Different from only one current commutation loop in a two-level inverter, there are two commutation loops in each T-type phase leg, i.e., green and blue shaded paths. To minimize the stray inductance, laminated layers is adopted in the busbar design. Meanwhile, since both the modules and dc-link capacitors are supposed to contact with the busbar tightly, spacers with different height are inserted to create a flat surface on the bottom of busbar. As the spacer brings extra parasitic inductance, a thinner spacer is preferred, and the lower layer will have a thinner spacer. The solid blue lines represent the busbars, and the yellow circles show the spacers. The exploded view of the laminated bus bar is shown in Fig. 3-13(b). The conductive layers, DC+, DC-, DC0, AC, are placed from top to bottom. The HB and CS modules in each

phase are placed as close as possible to each other, but needs to meet the voltage clearance distance. In this way, the total stray inductance of the bus bar can be reduced.

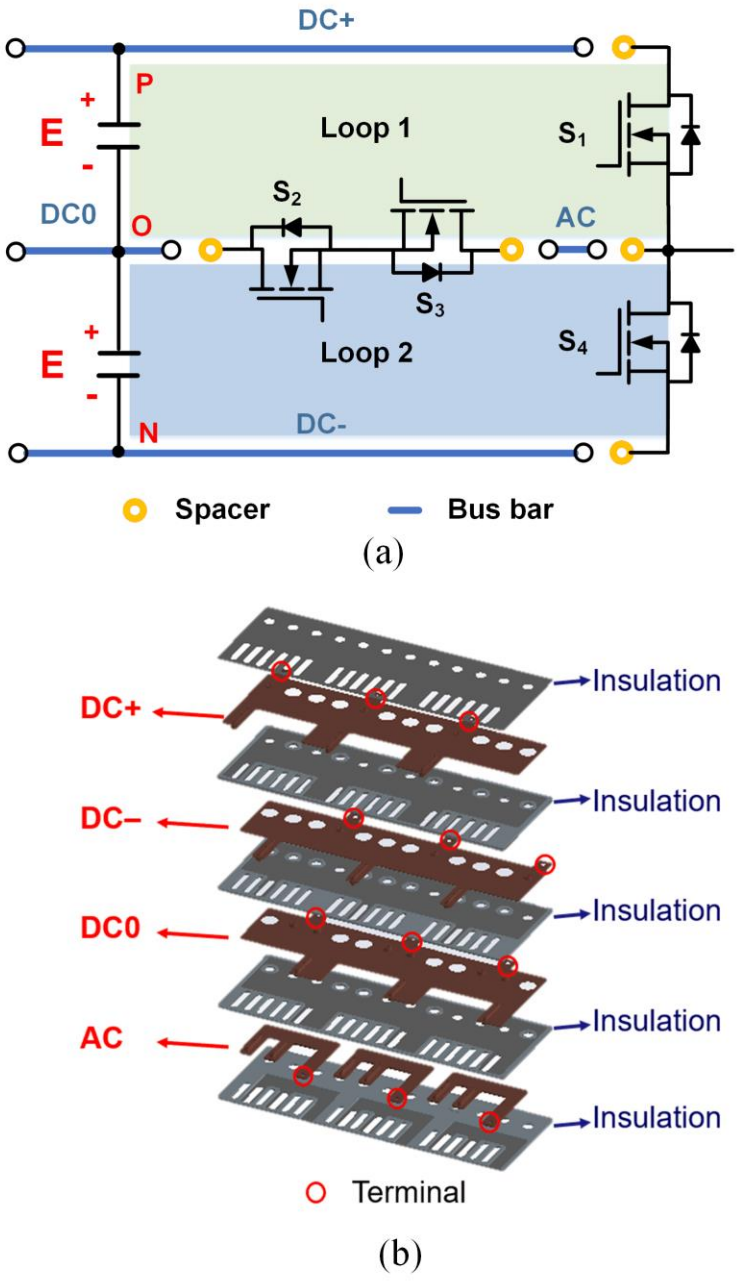



Figure 3-13 T-type phase leg (a) circuit with busbar (b) exploded view.

The laminated bus bar used copper as a conductive material and the PET material as an insulation layer. The insulation layer is 0.5 mm thickness inner and 0.25 mm outer to meet the

insulation requirement between different layers. Three sets of terminals, i.e., DC+, DC0 and DC-, are used on the DC input side, so DC layer thickness can be reduced to 1.5 mm to handle 300 A current. Meanwhile, one AC output is given in each phase, and the AC layer thickness is 3 mm to go through 300 A RMS. The stray inductance of the laminated busbar is analyzed using Q3D FEA simulations, one commutation loop in each phase of busbar has around 22 nH parasitic inductance, which includes the stray inductance from laminated busbar and the spacers. The stray inductances of the bus bar extracted using Q3D are presented in Table 3-5.

Table 3-5 Stray inductance of the bus bar extracted using Q3D

| | Phase A (nH) | Phase B (nH) | Phase C (nH) |
|---|---|---|---|
| Loop 1 | 21.76 | 20.53 | 22.17 |
| Loop 2 | 23.12 | 22.31 | 23.57 |

Fig. 3-14 A picture of the traction inverter prototype.

## 3.6 Experimental studies

The proposed T-type inverter was prototyped as shown in Fig. 3-14. The CIL tests were also performed using the actual prototype to evaluate the switching performance of the SiC modules. The test setup is shown in Fig. 3-15. The drain to source voltage is measured by using a differential probe THDP0200, while load current is measured by a current probe TRCP0600 since it's difficult to mount CVR on the busbar. DC bus voltage is set at 700V. A typical multiple-pulse CIL test result is shown in Fig. 3-16, in which the load current was gradually increased from 0 A up to 400 A with a step size of 50 A. Although obvious ringing can be observed, both current and voltage are within the safe operating region of the module.

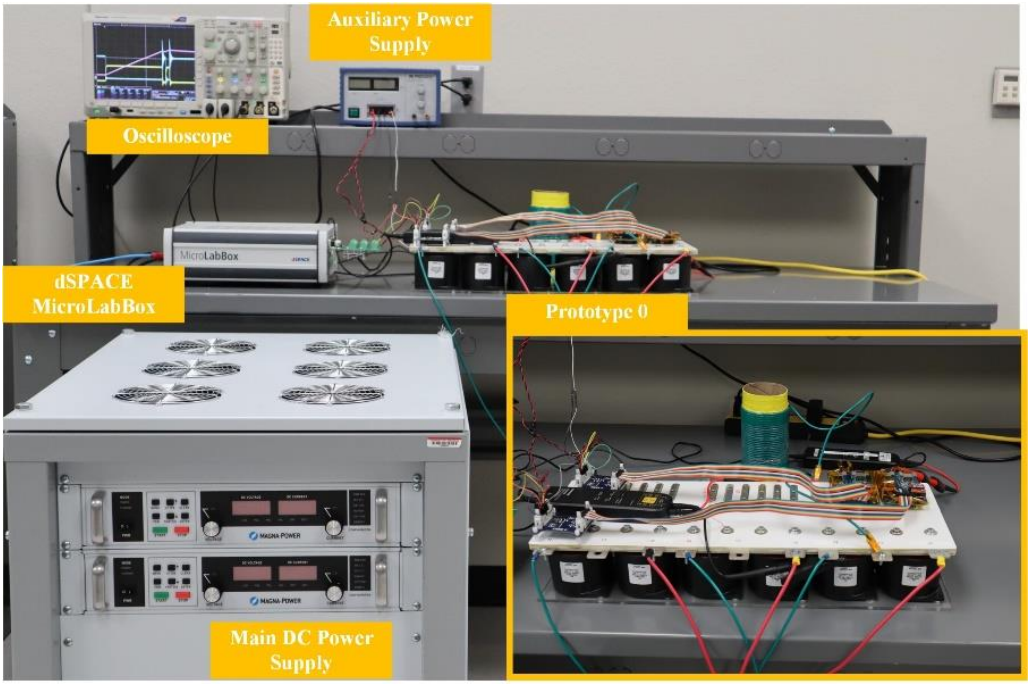



Fig. 3-15 The CIL test setup for actual prototype.

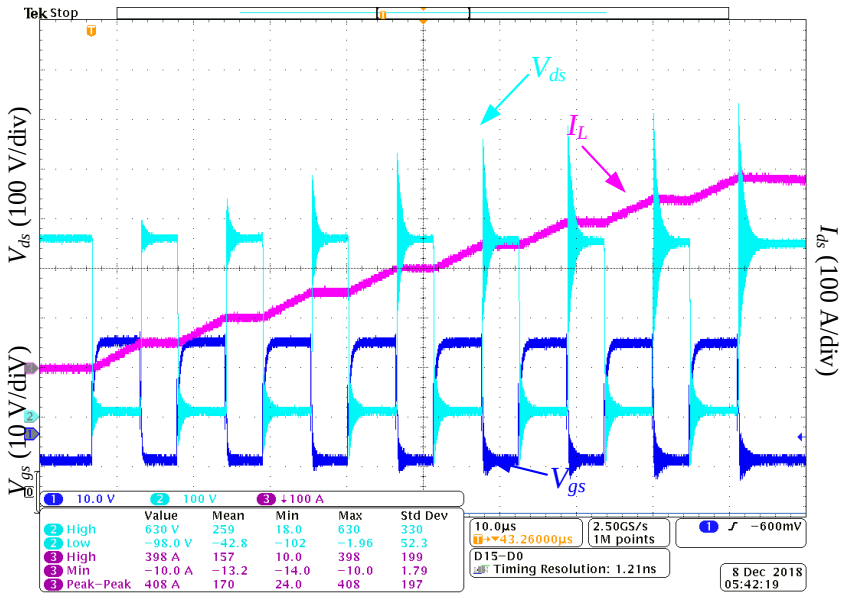
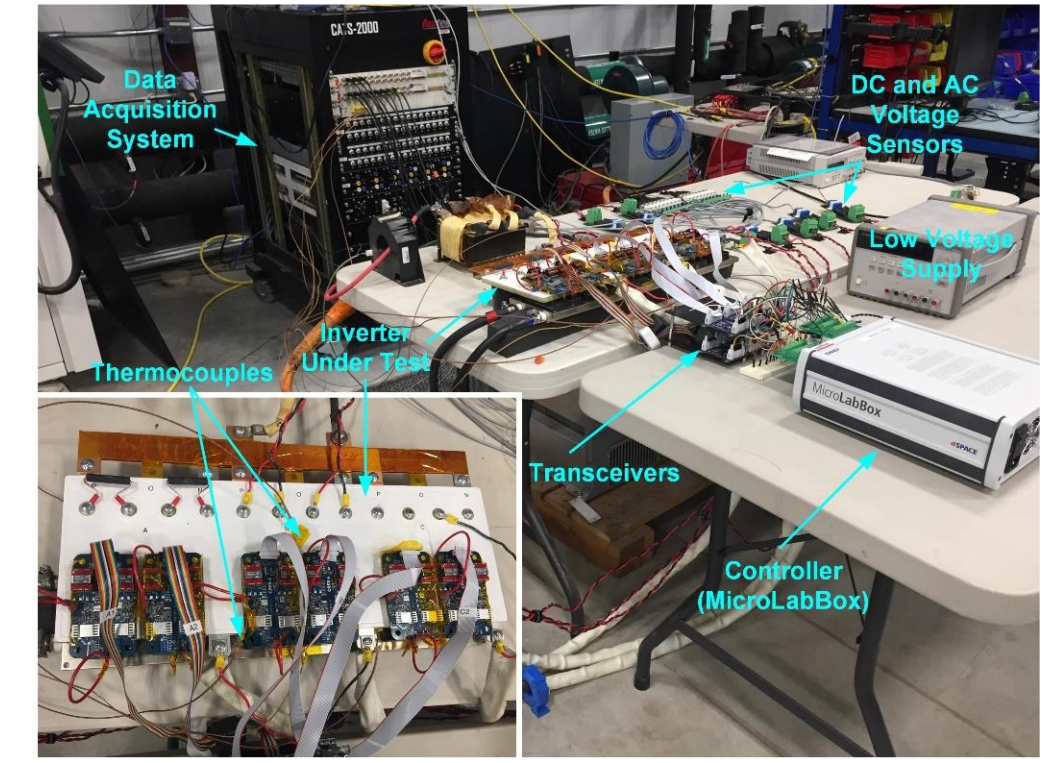


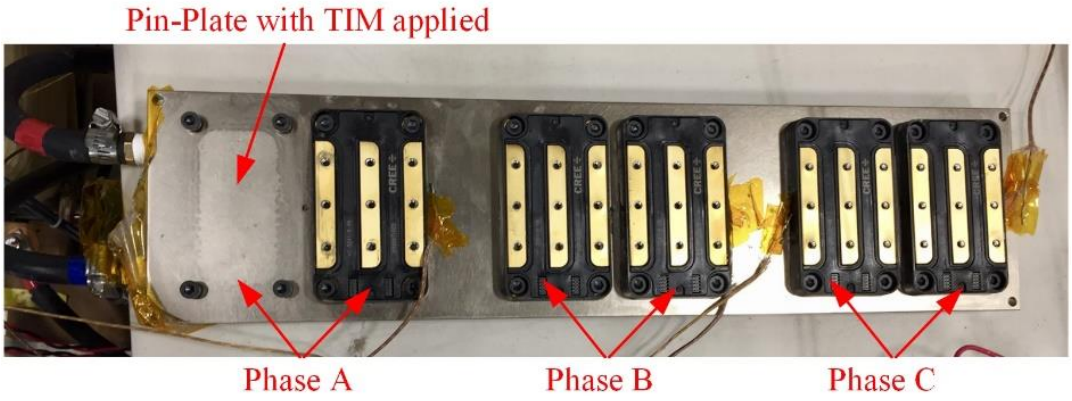

Fig. 3-16 A typical prototype-based CIL test result.

The high power testing for the prototype has also been performed to validate the performance of the inverter. The test setup is shown in Fig. 3-17(a). The inverter is connected to a high power resistive load bank via an LC filter designed to bypass the switching noises. The phase current and inverter terminal voltages are captured by using both oscilloscope and sensors, whose outputs are captured by a data acquisition system (DAQ). The gate signals are generated using dSPACE MicroLabBox. The details of the custom cold plate with mounted modules are shown in Fig. 3-17(b). Fig. 3-18 shows the experimental waveforms of the inverter stage at full power, when dc bus voltage is 700 V and output line-to-line voltage at the inverter terminal is a typical 5 level waveform with 400V rms. The filtered output phase current and line-to-line voltage are sinusoidal. The test result shows the THD on line voltage is 29.28%, which represents a 47.5% reduction compared to the conventional 2-L topology. This is critical for EMI mitigation and passive filter volume reduction. At each load power, the inverter was operated for sufficient time, which may even longer than an hour, to reach the thermal equilibrium and then the efficiency was measured

over the coolant. Fig. 3-19 shows the measured efficiency versus load power. As can be seen, the target peak efficiency of 98.5% has been achieved.




(a)




(b)

Fig. 3-17 (a) The test setup for high power testing and (b) a picture of the cold plate with one module removed.

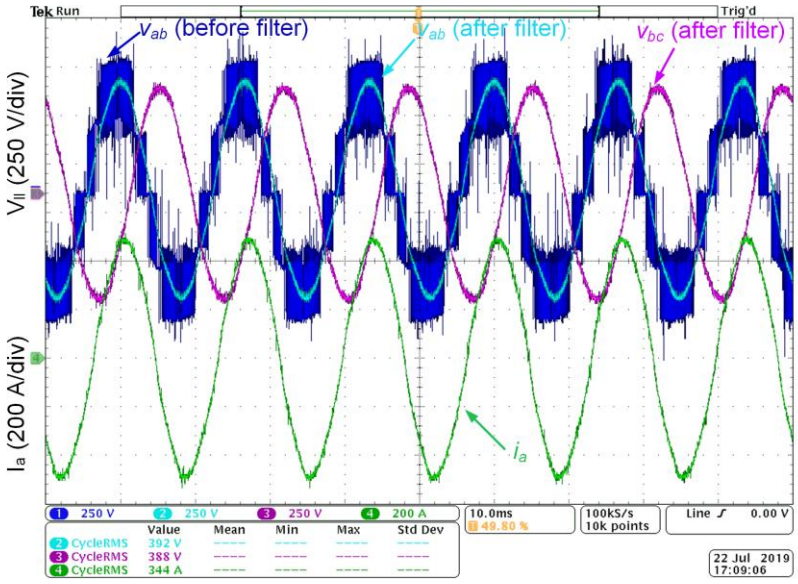



Fig. 3-18 Three-phase continuous test result.

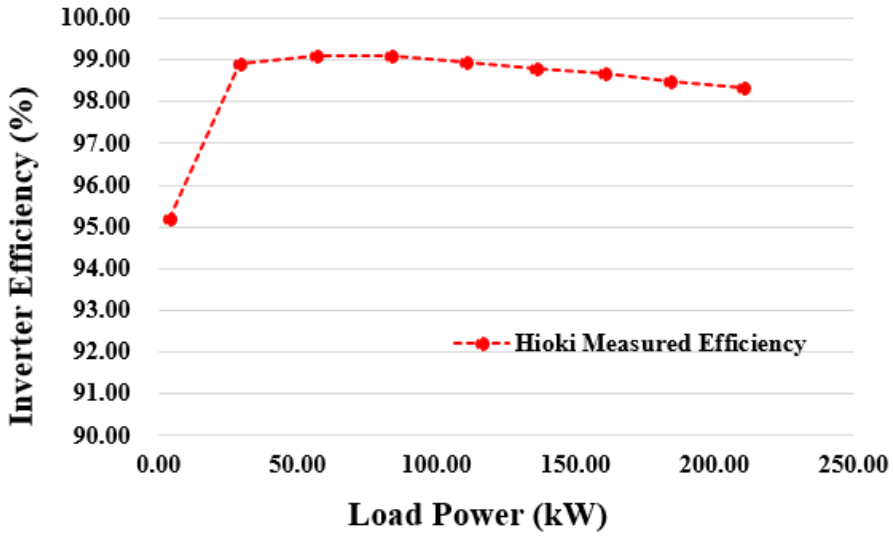



Fig. 3-19 Measured efficiency curve.

## 3.7 Conclusion

This paper presents a detailed design procedure of a high power density of 250 kW three-phase three-level T-type traction inverter. Comparing with the existing T-type topology work, the power rating and power density is much higher. A comprehensive analysis of the operating modes and current commutation loops in a T-type phase leg are provided. Moreover, comprehensive CIL tests

have been conducted to evaluate the switching characteristics. Based on the analysis for the power losses and switching performance, major components in the inverter system, such as power modules and dc-link capacitors are selected to satisfy the design requirements. In addition, an optimized busbar is designed to minimize the stray inductance and satisfy the output power requirements. The experimental results of pulse testing and high power testing are presented to validate the performance of the inverter prototype.

**Acknowledgment**

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency hereof. Full power testing in this work was conducted at the National Center for Reliable Electric Power Transmission (NCREPT), the University of Arkansas' High-Power Test Facility.

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# CHAPTER 4

# BUSBAR DESIGN AND OPTIMIZATION FOR VOLTAGE OVERSHOOT MITIGATION OF A SILICON CARBIDE HIGH-POWER THREE-PHASE T-TYPE INVERTER



## 4.1 Abstract

Silicon carbide (SiC) devices have faster switching speed than that of the conventional silicon (Si) devices, which however may cause excessive device voltage overshoot. Although larger gate resistance can help to restrain the overshoot, it slows down the switching speed and increases switching losses [1]. There are other methods that can mitigate the voltage overshoot, e.g., using low inductance busbars, adding snubber circuits, and etc. In this work, a 250kW SiC T-type inverter is investigated. Current commutation loops (CCLs) are firstly analyzed using a single-phase equivalent circuit. Then detailed busbar design methods, especially a three-dimensional (3D) busbar design concept, are proposed to select the optimal stacking order for the multi-layer laminated busbar and to address constraints posed by the physical terminal arrangements of SiC modules and dc-link capacitors. The stray inductance in each CCL is extracted via a 3D finite element analysis and validated on the actual inverter busbar prototypes using an impedance analyzer. To further minimize the busbar stray inductance, a hybrid bus bar structure with buffer circuit printed circuit board (PCB) using high-frequency decoupling capacitors is designed and

evaluated in this work. Finally, the effectiveness of the designed busbars as well as the buffer circuit are validated using experimental studies.

## 4.2 Introduction

The conventional two-level (2-L) inverter still dominates the motor drive market, especially for the low voltage applications. However, a significant amount of research effort has gone into the development of new inverter topologies to reduce the harmonics in output voltage and improve efficiency. Recently, multi-level inverters, which can generate low-harmonic output waveform to better resemble sinusoidal references [2], [3], have attracted substantial attention for not only the medium voltage drives but also the low voltage applications. Three-level (3-L) inverters, e.g., neutral-point-clamped (NPC) inverters, active-NPC (ANPC), and T-type (TNPC) inverter are the most commonly used among multi-level inverters [4]-[6]. Compared to the NPC or ANPC, which has six switch positions per phase, the T-type topology only has four switch positions per phase, although two of these devices need to withstand higher voltage stress. The development of a new generation of WBG devices with higher breakdown voltage and lower switching loss could potentially remove this limitation. In this work, the design of a T-type traction inverter, which can exploit the benefits of 3-L T-type topology and the silicon carbide (SiC) MOSFET modules, is presented.

When using SiC devices, the potential excessive voltage overshoot and ringing need to be mitigated. For SiC devices, the overshoot voltage during turn-off transient is a common issue, and if not handling properly, it may significantly reduce the device lifetime or even cause device failure [30], [31]. The voltage overshoot is mainly related to the fast switching of a SiC device, e.g., high *di/dt*, and the total stray inductance in the current commutation loops (CCLs) [32], [33]. The SiC devices can switch ten times faster than their silicon counterparts, which lead to 5~10 times higher

*di/dt*. To retain the merit of fast switching speed, the minimization of total stray inductance becomes the most critical path mitigating the voltage overshoot. The stray inductance in a CCL may come from 1) the parasitic inductance of the DC link capacitors; 2) the stray inductance of the semiconductor devices or power modules; 3) the stray inductance on the bus bars connecting the capacitors and the power devices. Hence, it is preferred to use capacitors and power devices/modules with low parasitic inductance. In a high-power voltage source inverter, the bussing structure needs to be designed and optimized to ensure low inductance connection between the DC capacitors and the power modules. The laminated bus bar structure, which consists of multiple copper sheets, separated from each other by a dielectric material, is commonly used since it can effectively reduce the stray inductance. A properly designed bus bar could potentially reduce the voltage overshoot, electromagnetic interference (EMI) emission, switching losses, and thermal stress [7]-[10], at the same time enhance the system mechanical strength.

Generally speaking, the laminated bus bar design is case by case and needs to be optimized based on the power module to be used and the potential applications. Different circuits topology and power rating also affect the bus bar design. For instance, bus bar design examples for single-phase H-bridge inverters [11], [12], a three-phase inverter [13], and single-phase T-type phase legs [14], [15], [26] can be found in the existing literatures. Usually, the objective of bus bar design and optimization is to achieve the lowest impedance of the busbar itself, at the same time, ensure system specifications can be met. Multilevel topology has lower *dv/dt* and EMI, but its bus bar design can be complicated. Especially multiple co-existing CCLs will make the bus bar design difficult, since low stray inductance and the symmetry of CCLs among different phases need to be considered [16]-[18].

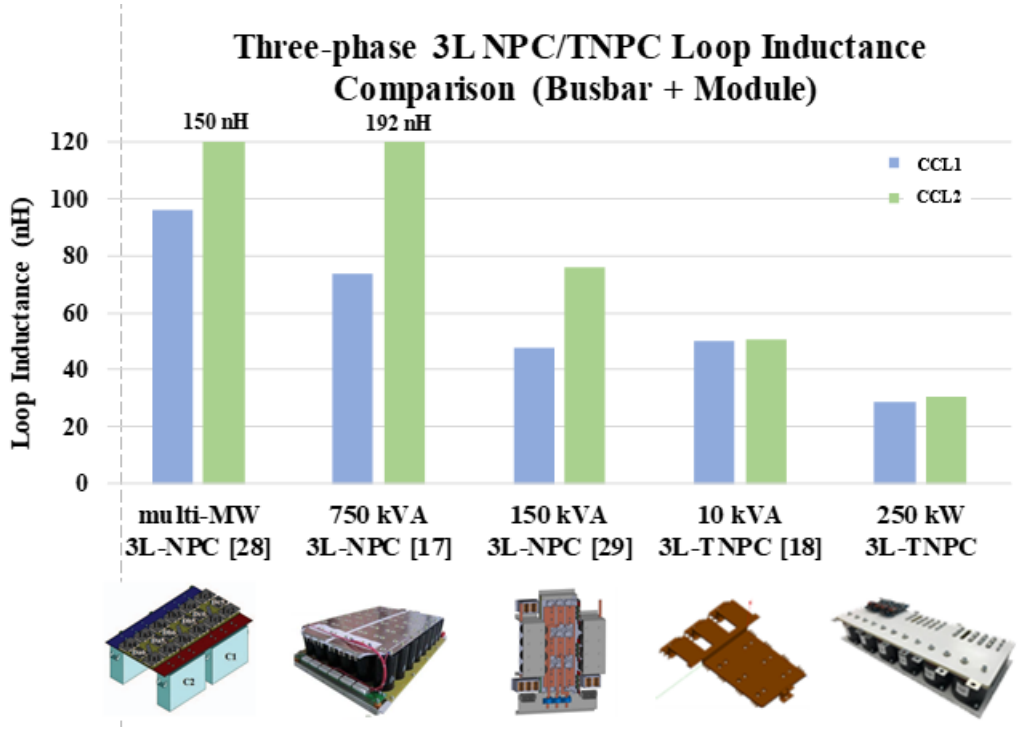



Fig. 4-1 Comparison of loop inductance for three-phase 3L inverters.

In this work, the design and optimization process of a multi-layer laminated busbar, which is proposed to improve the switching performance and reduce voltage overshoot, for a three-phase three-level T-type inverter is presented. This 250-kW all-SiC T-type traction inverter is designed for heavy equipment applications [27]. Novel 3-D busbar structure and hybrid bus bar with PCB snubber board are proposed which can achieve lower busbar inductance than published three-phase 3-level inverter literature, as shown in Fig. 4-1 [17], [18], [28], [29].

The analysis of CCLs in a three-level T-type inverter is presented in Section 4.3, which leads to the bus bar optimization process described in section 4.4. In Section 4.5, the laminated bus bar models are evaluated using finite element analysis (FEA) to obtain the stray inductance in each CCL, which is further verified using the inductance measurement by the impedance analyzer for the bus bar prototypes. Since high-frequency decoupling capacitor can provide the lower inductance path during switching transients, it also can restrain voltage overshoot, so a hybrid bus

bar structure with snubber PCB board designed for the T-type inverter is also presented in this work, which is in Section 4.6. Finally, experiments are conducted to verify the validity of busbar design, snubber board design and the veracity of theoretical analysis in Section 4.7**.**

## 4.3 Modeling and analysis of current commutation loops in a T-type inverter

### 4.3.1 The effects of parasitic inductance

To study the voltage overshoot of a power device, the dynamic model for the turn-off transient needs to be established. Taken the 2-L double pulse test circuit as an example, its equivalent circuit during turn-off is shown in Fig. 4-2(a). There is only one CCL in this configuration, where the *R* and *L* represent the lumped equivalent series resistance (ESR) and equivalent series inductance (ESL) in the conduction path, and *C* stands for output capacitance of the device, i.e., $C_{oss}$. Using small signal theory, the dynamic model for the turn-off transient can be simplified into a second order RLC circuit, as shown in Fig. 4-2(b). The corresponding circuit model and the transfer function from the commutation current to the voltage stress with the zero initial conditions could be written as (4-1) and (4-2), respectively.

$$(sCU_C + I)\cdot(R + sL) + U_C = 0 \tag{4-1}$$

$$G(s) = \frac{U_c(s)}{I(s)} = -\frac{\frac{L}{C}s + \frac{R}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{4-2}$$

According to (4-2), the drain-source voltage can be regarded as the step response of a second order RLC circuit. Therefore, the overshoot $\sigma$ and damping ratio $\zeta$ can be expressed as:

$$\sigma\%=e^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}}\times 100\% \tag{4-3}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{4-4}$$

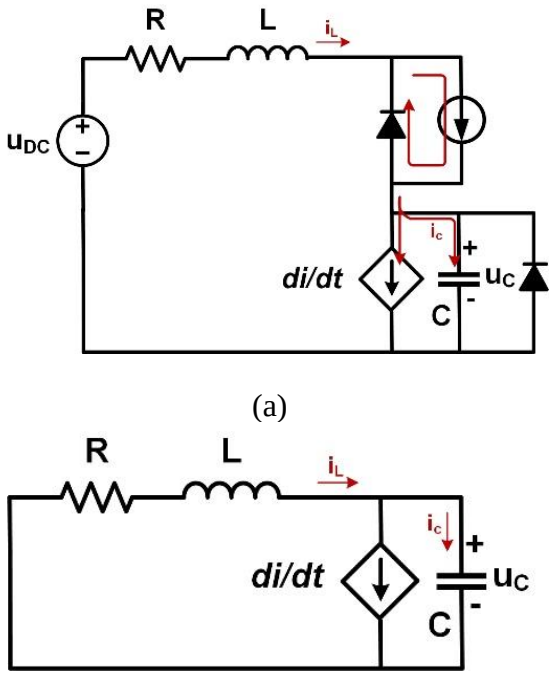



Fig. 4-2 Dynamic model of a single device turn-off transient: (a) an equivalent circuit and (b) a small signal simplified second-order RLC circuit.

It can be concluded from (4-3) that to reduce the overshoot, the damping ratio needs to be increased. According to (4-4), increasing *R* and/or *C* or decreasing *L* can increase the damping ratio. *R* is the parasitic resistance in the CCL, which is related to the heat generation. Increasing *R* could lead to thermal issues, which may be harmful to the components in the CCL. *C* is the output capacitance of the device, which is an intrinsic parameter of the device itself. While for SiC devices, the output capacitance is usually much smaller than that of the Si devices, which contributes higher overshoot for SiC devices. To sum up, the most efficient approach to mitigating voltage overshoot is to keep *L*, the loop stray inductance, as low as possible.


(a)


(b)

Fig. 4-3 Pictures of (a) the Wolfspeed SiC module [25] used in this work and (b) a laminated busbar with embedded spacers.

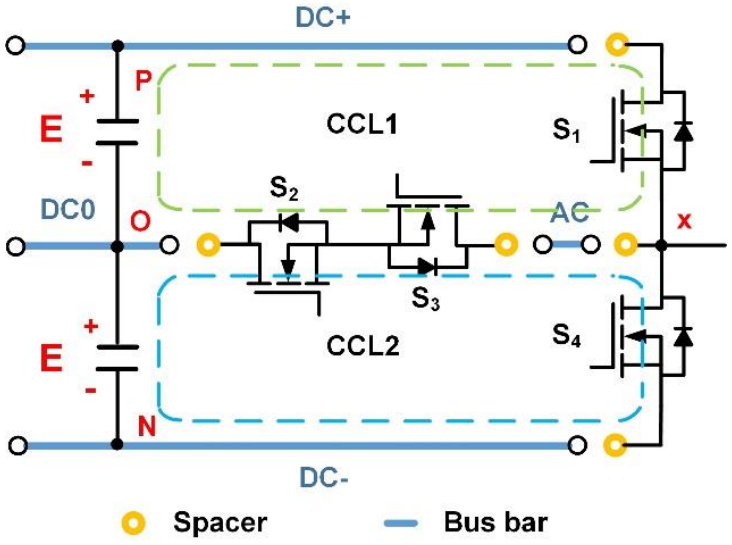



Fig. 4-4 A detailed equivalent circuit model of a T-type phase leg.

### 4.3.2 A practical circuit model for a T-type phase leg

The SiC power modules, both half-bridge (HB) modules and common-source (CS) modules, used in this works were prototyped by Wolfspeed. Given the power lead frames shown in Fig. 4-3(a), to enable a compact integration of the busbar, modules, and dc-link capacitors, cylindrical spacers were used to create a flat surface on the bottom of the bus bars, as shown in Fig. 4-3(b). A practical circuit model for a T-type phase leg considering the busbar and spacers is shown in Fig. 4-4. S2 and S3 are the two switch positions in the CS module, which serves as the clamping leg. While S1 and S4 are the two switch positions in the HB module. The blue lines are the layers in the busbar and the yellow circles represent spacers. As can be seen, for a T-type phase leg, the busbar consists of various layers with different voltage levels, i.e., DC+, DC-, DC0, and AC. In addition, different from only one CCL in a single phase 2-L inverter, there are two CCLs in each phase of a T-type inverter, i.e., green and blue dash lines.

Table 4-1 Switching states

| State | $V_{xO}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
|---|---|---|---|---|---|
| P | $+V_{dc}/2$ | on | on | off | off |
| O | 0 | off | on | on | off |
| N | $-V_{dc}/2$ | off | off | on | on |

### 4.3.3 Modeling and analysis of CCLs in a T-type phase leg

All the CCLs in the circuit and the stray inductance distributions must be thoroughly investigated to ensure a low inductance busbar design. Fig. 4-5 illustrates the current commutation process in a single-phase T-type inverter. As shown in Fig. 4-5, each CCL consists of dc-link capacitors, switch positions, spacers and multiple layers in the busbar. The switching states P, O,

N of a T-type converter are defined in Table 4-1 [6]. These three switching states lead to three voltage levels of phase-neutral voltage $V_{xO}$, i.e., $+V_{dc}/2$, 0, and $-V_{dc}/2$, where *x = a, b, or c*.

The first type of CCL, i.e., CCL1 occurs during the transition between P state and O state. Taking the transition from P state to O state as an example. In the beginning, the circuit is in P state, i.e., S1 and S2 are ON, while S3 and S4 are OFF. In the meantime, the load current flows through S1, as shown in Fig. 4-5(a). During the turn-off of S1, the load current commutates from S1 to the clamping leg, i.e., the current flowing through S1 decreases, and the current flowing through the clamping leg increases with the same *di/dt*. Due to the loop inductance, there is an overshoot in the drain-source voltage of S1, when it turns off. In the end, the circuit is in O state, i.e., the S1 is OFF and the clamping leg carries the load current, as shown in Fig. 4-5(b). The corresponding CCL, which is denoted as CCL1 is shown in Fig. 4-5(c), including top dc-link capacitors, S1, S2, and S3 switch positions and the DC+ DC0 and AC layers in the busbar.

The second type of CCL, i.e., CCL2, occurs during the transition between the N state and the O state. Taking the transition from N state to O state as an example. In the beginning, the circuit is in N state, i.e., S3, S4 are ON, while and S1 and S2 are OFF. In the meantime, the load current flows through S4, as shown in Fig. 4-5(d). During the turn-off of S4, the current commutates from S4 to the clamping leg, i.e., the current flowing through S4 decreases, and the current flowing through the clamping leg increases at the same *di/dt*. Due to loop inductance, there is an overshoot in the drain-source voltage of S4. In the end, the circuit is in the O state, i.e., S4 is OFF, and the clamping leg carries the load current, as shown in Fig. 4-5(e). The corresponding CCL, which is denoted as CCL2 is shown in Fig. 4-5(f), including bottom dc-link capacitors, S2, S3, and S4 switch positions and the DC-, DC0, and AC layers in the busbar.

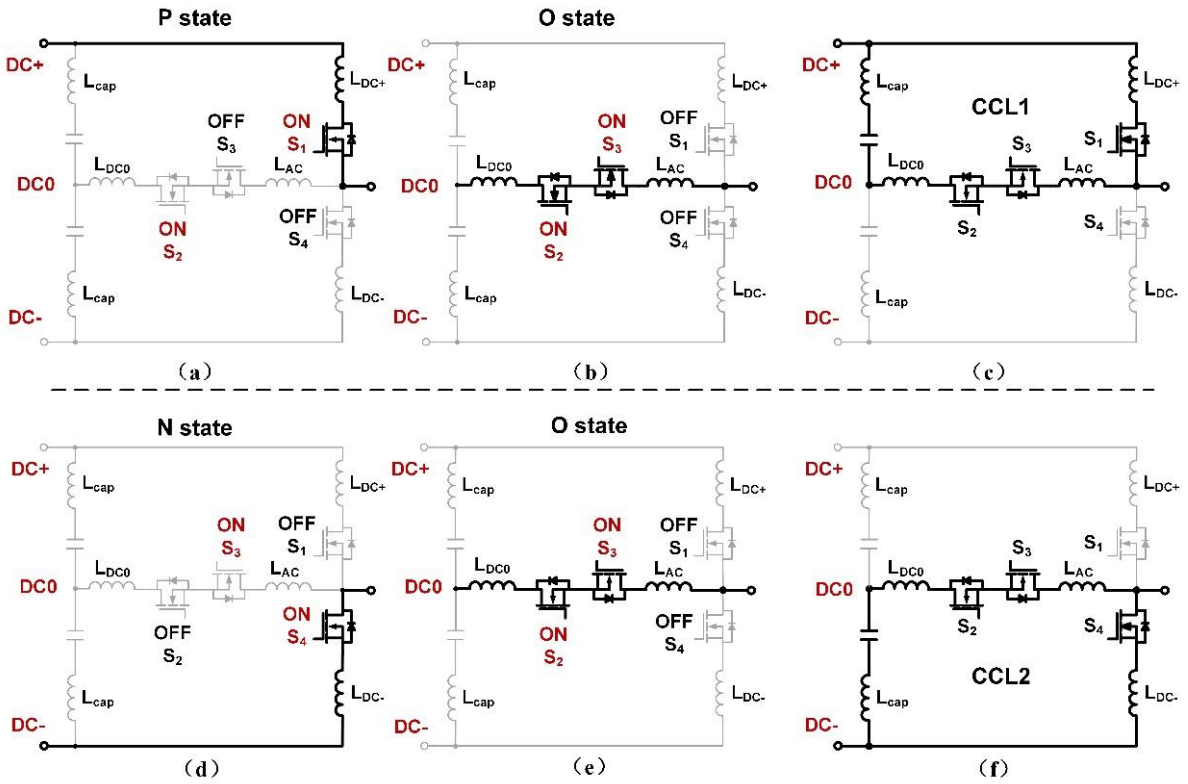



Fig. 4-5 CCLs in a T-type inverter. Note, black solid portion represents conduction paths in (a), (b), (d) and (e), and represents the CCLs in (c) and (f).

To optimize the bussing structure, the CCLs should be designed symmetrically, such that the switching performance of S1 and S4 can be close enough to each other. Based on the above analysis, both CCLs contain one clamping leg module and part of the bus bars. Given the symmetric layout of S1 and S4 in the HB power module, to achieve symmetric design for CCLs, the top and bottom DC-link capacitor bank, as well as the bus bars in each loop, should have similar stray inductances.

Each CCL consists of DC-link capacitors, SiC MOSFET switch positions, laminated bus bars, connecting screws, and spacers. The loop inductance of the CCLs shown in Fig. 4-4(c) and (f) can be expressed as:

$$L_{CCL} = L_{cap} + L_{module} + L_{busbar} \tag{5}$$

$$L_{CCL1} = L_{cap} + \frac{1}{2}L_{HB} + L_{CS} + L_{DC+} + L_{DC0} + L_{\mathrm{AC}} \tag{6}$$

$$L_{CCL2} = L_{cap} + \frac{1}{2}L_{HB} + L_{CS} + L_{\mathrm{DC-}} + L_{DC0} + L_{\mathrm{AC}} \tag{7}$$

Where $L_{cap}$ is the ESL of dc-link capacitors, $L_{module}$ is the parasitic inductance of SiC MOSFET module, $L_{busbar}$ is the parasitic inductance of laminated busbar including spacers, $L_{HB}$ is the parasitic inductance of HB module, $L_{CS}$ is the parasitic inductance of CS module, $L_{DC+}$, $L_{DC-}$ and $L_{DC0}$ are the parasitic inductances of DC+ layer, DC- layer and DC0 layer, respectively, $L_{AC}$ is the parasitic inductance of AC layer in the busbar. Besides selecting modules, capacitors, and screws with lower stray inductance, to further reduce the stray inductance, the design and optimization of the busing structure should be the main focus.

## 4.4 Multi-layer laminated busbar design process

### 4.4.1 The busbar design principles

The laminated busbar usually consists of multiple conduction layers separated by the thin layer of insulation materials. The generic structure of a two-layer laminated busbar is shown in Fig. 4-6. The length, width, thickness of each layer is represented by *l*, *w*, and *t*, respectively, while *d* is the distance between two layers. The cross-sectional area of each layer, which is the product of the conductor's width and thickness, determines its current carrying capability. The relationship between current carrying capability and cross-section area [19] can be expressed as

$$A=400 \cdot I \cdot 0.785 \cdot \left[1 + 0.05\left(N - 1\right)\right] \cdot 10^{-6} \tag{4-8}$$

Where $A$ is the cross-sectional area of the conductor measured in inches$^2$, $I$ is the maximum current in amperes, $N$ is the total number of the conductors in the bus assembly. 400 circular mils

per ampere is a traditional basis for the design of single conductors. Since bus bars are not round, circular mils must be converted to square mils by multiplying 0.785.

The planar layout of the busbar is usually decided by the footprint of modules and dc-link capacitors, as well as how they are placed. To meet the criteria of the maximum allowed current density, e.g., 5 A/mm2, the most direct way to adjust the cross-sectional area of the bus bar is to vary the thickness. Obviously, the thicker the bus bar, the lower the current density without considering the skin effect. However, increasing the thickness will increase the weight of the bus bar. Therefore, it is usually required to trade the current density against the weight of the bus bars based on the specifications for particular applications.

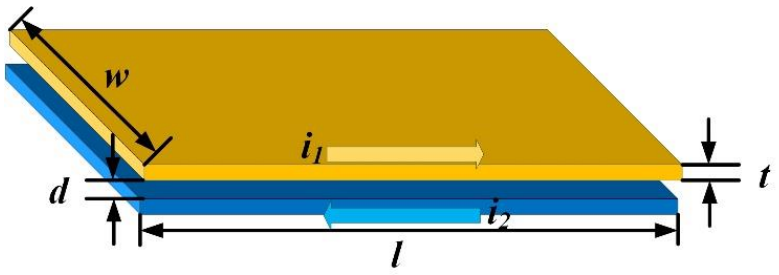



Fig. 4-6 Model of a generic two-layer laminated busbar.

The self-inductance of a single layer busbar [20], [21] can be expressed as:

$$L_{self} = 2\times10^{-4} l\left[\ln\left(\frac{2l}{w+t}\right)+0.5+0.2235\left(\frac{w+t}{l}\right)\right]\mu H \tag{4-9}$$

The *l*, *w*, *t* are measured in *mm*. The *l* and *w* usually depend on the footprint of the modules and capacitor, while *t* is usually decided by the current density requirement. To reduce the self-inductance, the layout of the busbar needs to be carefully considered. Due to the proximity effect, the high-frequency current distribution tends to concentrate on the adjacent surface of the copper

bar. Two laminated layers with opposite current directions lead to opposing magnetic flux lines, which will weaken the radiated emissions of each other. Thus, mutual inductance exists, which has a negative value when two bus bars carrying current in opposite directions. Take the two-layer bus bar as an example, the total stray inductance can be expressed as

$$L_{total} = L_{self\,1} + L_{self\,2} + 2 \times L_{mutual} \tag{4-10}$$

Since the mutual inductance is a negative number when two current directions are opposite, and self-inductance is positive, the principle of busbar design optimization becomes reducing the self-inductance and increasing the negative mutual inductance, which is related to the overlap area and the distance between different layers. To enlarge the mutual inductance, larger overlap area and smaller vertical distance between conductive layers are preferred. Furthermore, the strong coupling provides good immunity to external magnetic interferences [22].

### 4.4.2 Busbar design process for a three-phase T-type inverter

A systematic busbar design process for a T-Type inverter is presented in this section. The layout of the busbar should be symmetric, and the stray inductance in each CCL should be minimized. One possible placement of modules and capacitors of a three-phase T-type inverter is shown as Fig. 4-7(a), while the corresponding schematic is shown in Fig. 4-7(b). It is obvious that each phase consists of the same components, one HB module, one CS module and two series-connected capacitors. This placement ensures each phase has almost identical CCLs, and the layout of all three phases is highly symmetrical to each other. To fit the way that components placed in Fig. 4-7(a), the planar layout of the laminated busbars are shown in Fig. 4-8. Since the CCLs are almost the same among the three phases, the details for phase A are illustrated as an example. High-frequency current flow paths are presented in Fig. 4-9, along the CCLs. Due to the existence

of two CCLs, i.e., CCL1 and CCL2, with two possible current flow directions, four high-frequency current flow paths are shown.

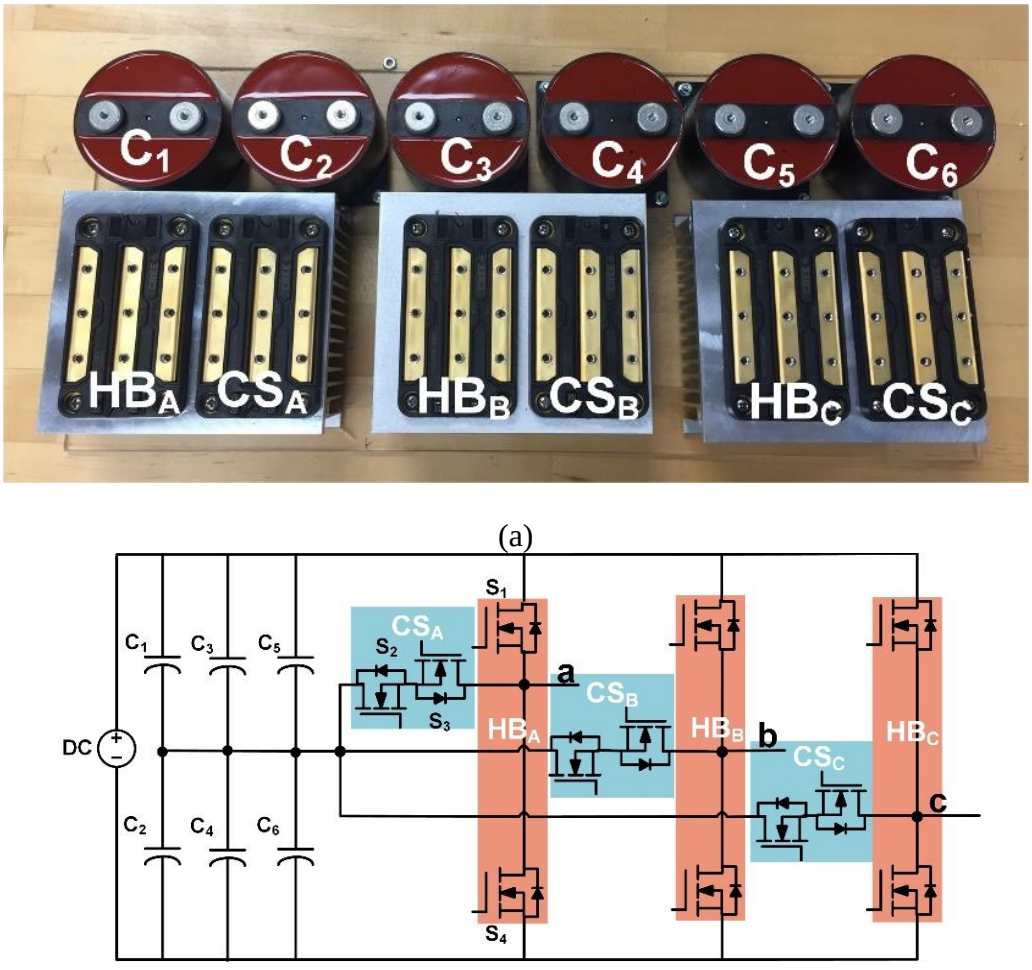
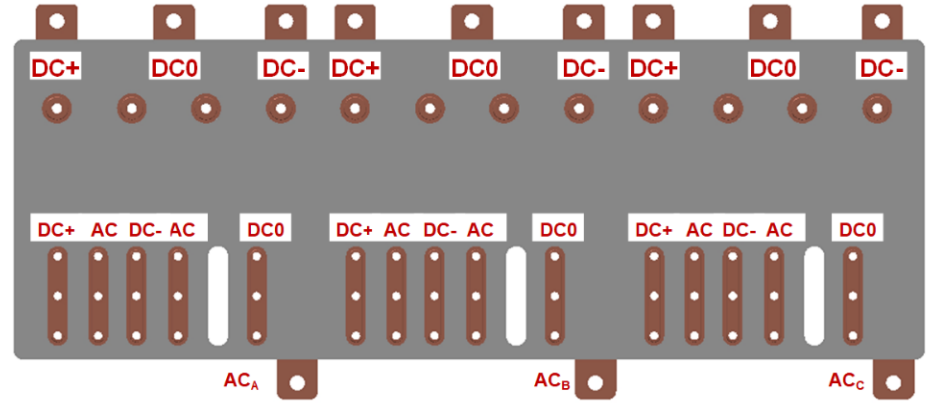
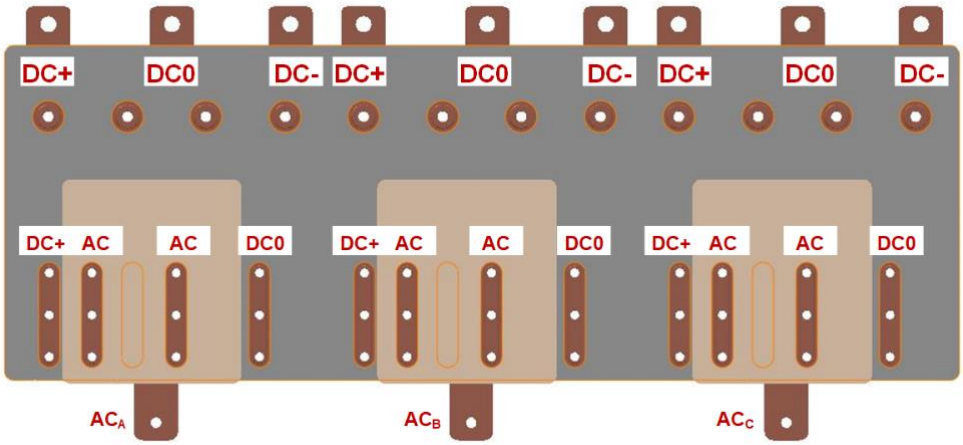



Fig. 4-7 (a) A possible placement of the major components in a T-type inverter and (b) it's corresponding schematic.




(a)




(b)

Fig. 4-8 The planar layout of the laminated busbar for a three-phase T-type inverter: (a) Design I and (b) Design II.

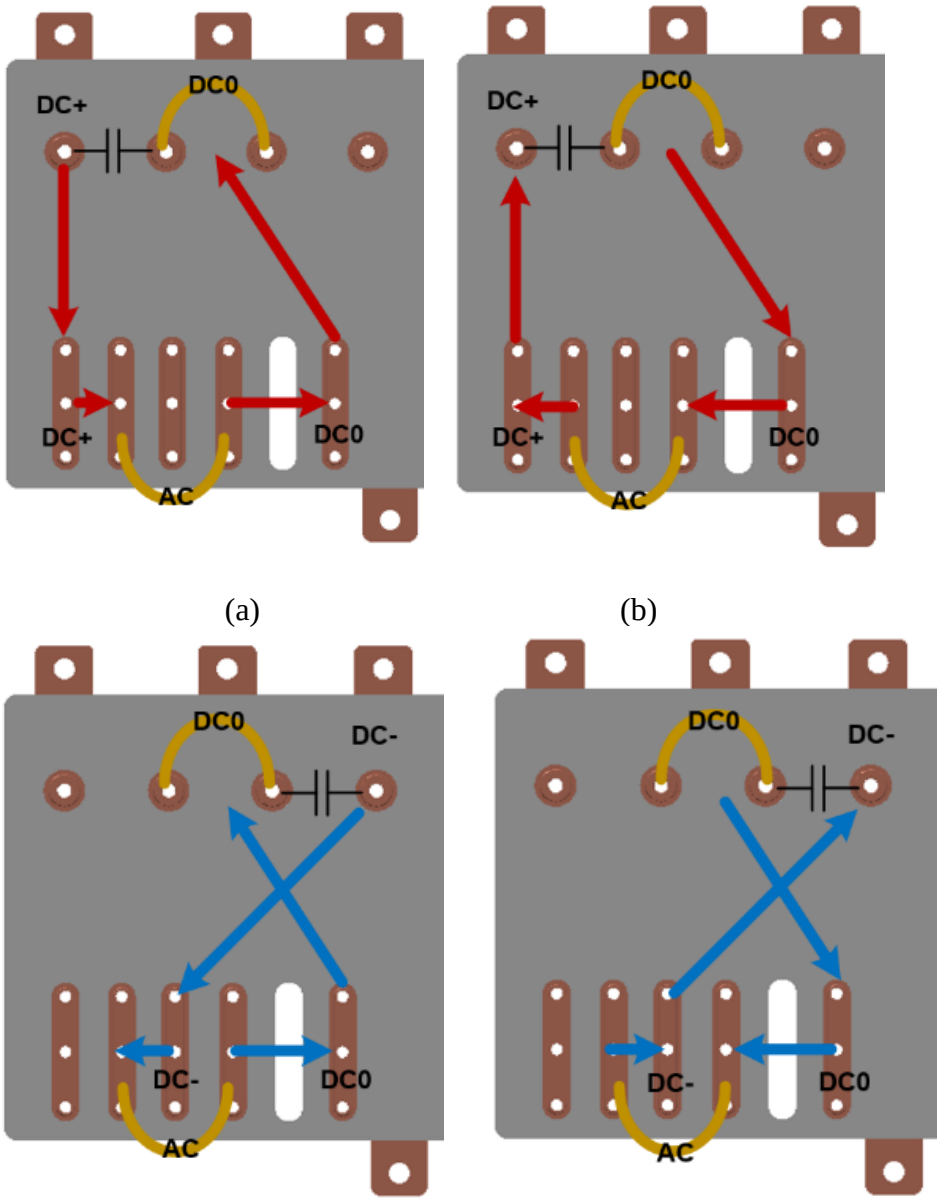



Fig. 4-9 High-frequency current flow paths in different CCLs: (a) CCL1 with positive current (b) CCL1 with negative current (c) CCL2 with negative current (d) CCL2 with positive current.

Figure 4-10 shows the relationship between the spacer thickness $\Delta t$ and the parasitic inductance $\Delta L$ of each layer. It is obvious to see the spacer thickness has a significant influence on parasitic inductance; each millimeter increment will lead to nearly 0.2 nH addition to the parasitic inductance, which means the thinner spacer is better. Since the rate of the parasitic inductance increase is similar for layers with different voltage levels, to minimize the total loop inductance,

the task can be simplified to minimize the total spacer thickness. Due to the existing of multiple layers and the bottom layer has the shortest spacer, the stacking order of various layers in a busing structure needs to be optimized.

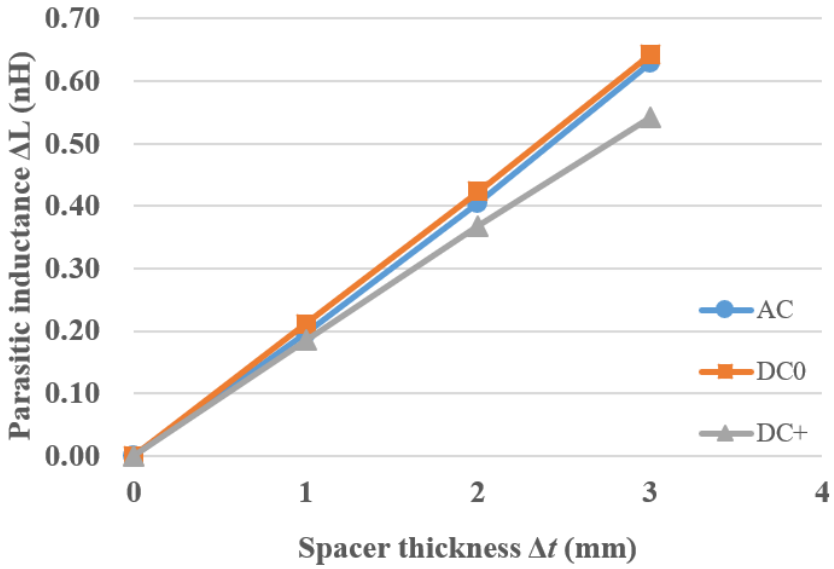
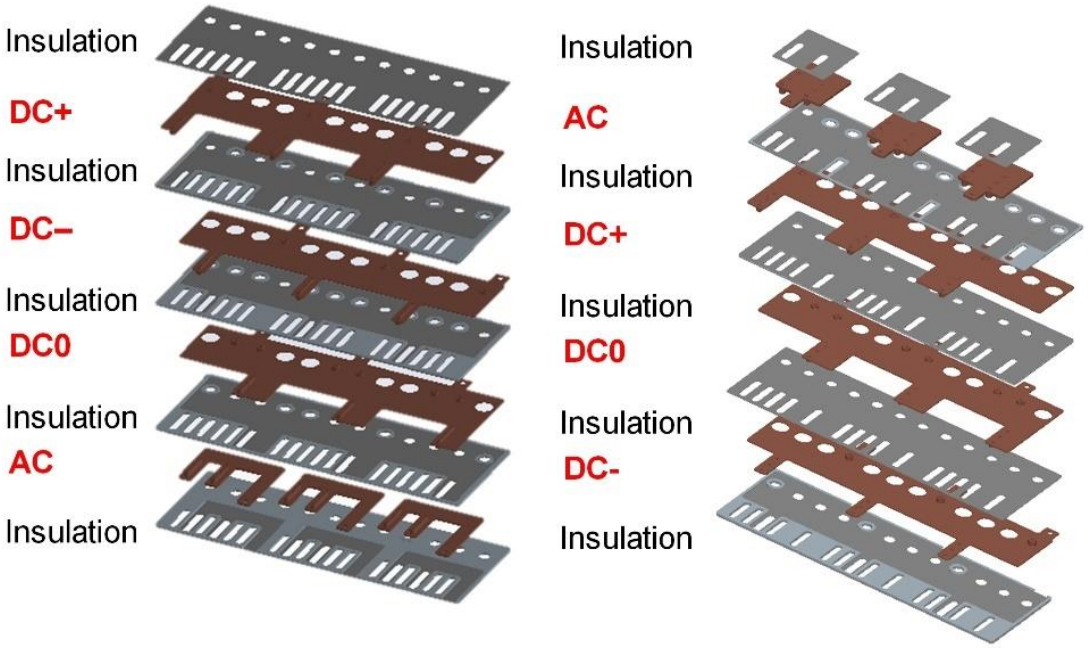



Fig. 4-10 Relationship between spacer thickness $\Delta t$ and the parasitic inductance $\Delta L$.

The busbar design shown in Fig. 4-8(a) is straightforward, denoted as Design I. Due to the use of two modules for one T-type phase leg, part of the AC layer is shared by both CCLs, Therefore, the parasitic inductance of the AC layer is very critical. This is the reason why the AC layer is also laminated. In Design I, the AC bus bar is placed on the very bottom, such that its spacer can be thinnest. DC0 layer is also shared by both CCLs, and it is placed on the second from the bottom, then DC+ and DC- layers, respectively. The exploded view of this bus bar design is shown in Fig. 4-11(a). In the actual laminated bus assembly, copper is used as the conductive material due to its good electrical conductivity and mechanical strength. Four conductive layers are laminated with the overlap area set to be the largest. The insulation layers used PET material with 0.5 mm thick for inner layers and 0.25 mm outer layers to meet the voltage insulation requirement between

different voltage levels. High current density is usually concentrated on power terminals. Therefore, three sets of terminals are used in DC+, DC0, and DC- input sides to achieve low current density and even current distribution. As such, the thickness of dc layers can be reduced to 1.5 mm to carry 300 A in total. Meanwhile, one AC output is given in each phase, the AC power terminals cannot be split into multiple terminals in this case, so the thickness of the ac layer is set to be 3 mm to carry 300 A rms current.



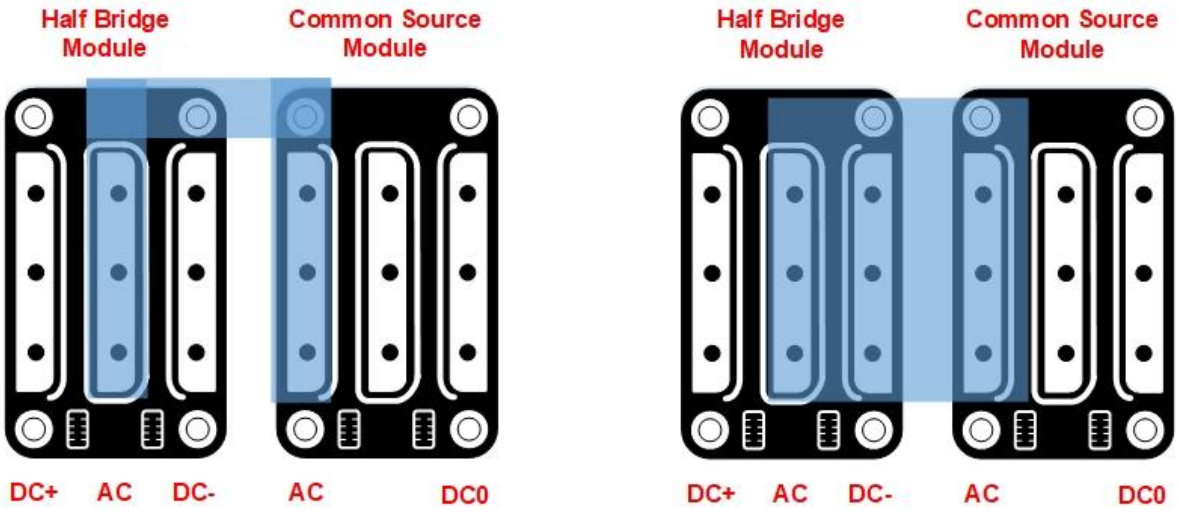

(a) (b)

Fig. 4-11 Exploded view of two bus bar designs (a) Design I and (b) Design II.

### 4.4.3 An enhanced bus bar design – a 3D design concept

The terminal layout of the power module and the gate/signal pins poses significant challenges to the busbar optimization. As shown in Fig. 4-4, the AC layer connects the AC output terminal of the HB module and one of the power terminals of the CS module. Since the AC layer is shared with both CCLs, it is critical to minimize its stray inductance. Therefore, using the shortest path to

connect those two terminals is preferred, for instance, as shown in Fig. 4-12(b). However, due to the laminate nature of multi-layer bus assembly, if the bus bar shown in Fig. 4-12(b) is placed on the bottom, to bolt it down to the DC- terminal of the HB module, screw holes and corresponding cut out for voltage insulation need to be made through the top layer of the bus bar to the bottom layer. As shown in Fig. 4-12(a), a U-shape AC bus bar is designed to connect the AC terminal of the HB module, and a power terminal of the CS module. This will not affect the lamination of the top layers, but it will significant elongate the current flow path and increase the parasitic inductance of the AC layer.




(a) (b)

Fig. 4-12 A diagram showing AC layer connection in the (a) Design I and (b) Design II.

To address this issue, a 3-dimension busbar design concept is proposed in this work. The main idea is to leverage the thickness of the busbar assembly to resolve the challenges posed by the physical terminal layout of the power modules, that is bury part of screws under a separate flexible bar. The planar layout of the proposed new busbar is shown in Fig. 4-8(b). The exploded view of the enhanced design, i.e., Design II, is shown in Fig. 4-11(b). Compared to the Design I shown in Fig. 4-11(a), the stack order of the layers in the enhanced design was changed to AC,

DC+, DC0, DC- from top to bottom. To enlarge the laminated area between the AC layer and other layers and shorten the current flow path, it is moved to the very top. And it is the mentioned separate flexible bar. The cross-sectional views of CCLs in Design I and Design II are illustrated in Fig. 4-13. In Design II, to ensure the AC layer is a complete wide copper plate, the DC- layer bolt is buried under the new AC bar as shown in Fig. 4-13(c) and (d). In addition, DC+, DC0, and DC- layers were laminated into a bus assembly, while the AC layer is built as an individual layer to be placed on top of the laminated busbar. Using this approach, screws can be used to bolt bus bar down to DC- terminal. Due to the thickness of the laminated bus bar, those screws are buried underneath the AC layer without affecting the optimized geometry of the AC layer. Moving the AC bus bar to the top using the proposed 3-D bussing structure will significantly reduce the parasitic inductance due to the enhance AC layer geometry. In addition, the parasitic inductance of total spacers in the new design keeps almost the same as the previous design. Moreover, Design II also leads to a 24% weight reduction compared to the Design I.

## 4.5 Busbar parasitic inductance extraction

### 4.5.1 Simulation studies using finite element analysis

This section presents the simulation and measurement results to validate the effectiveness of the proposed low inductance busbar designs. There are several ways to obtain the parasitic inductance of a laminated busbar, such as the finite element analysis (FEA) or partial element equivalent circuit (PEEC) using numerical software simulation tools, and directly measured by time domain reflectometry (TDR) [22]. The principle of the FEA method is solving Maxwell's equations, while PEEC reduces the computational cost by breaking large size connectors into small parts. TDR is relatively complicated and needs special software and hardware. Therefore, FEA and PEEC are more commonly used. In this work, ANSOFT Q3D was used for simulation studies,

and the results for Design I and II are presented in Tables 4-2 and 4-3, respectively. Simulations are carried out at 1 MHz, which emulate the frequency of MOSFET's switching transients. As can be seen, the simulated loop parasitic inductance in the Design II is around 17nH in each CCL, which represents over 20% reduction compared to the Design I.

Table 4-2 FEA simulation results for bus bar Design I

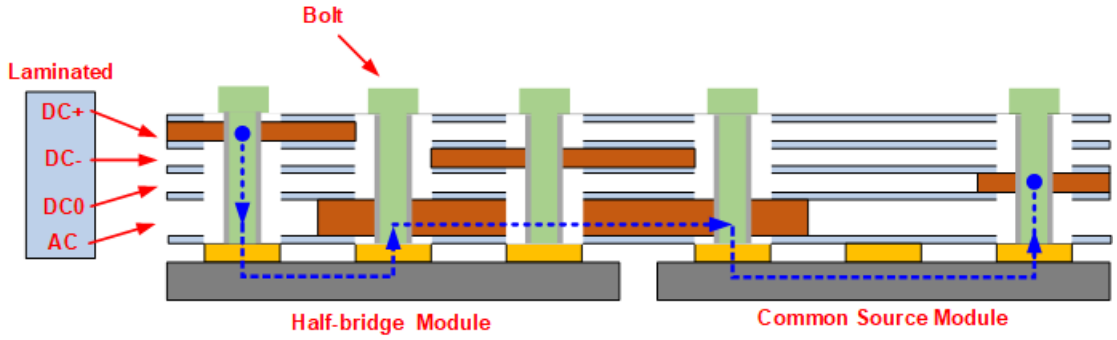
| | Phase A (nH) | Phase B (nH) | Phase C (nH) |
|---|---|---|---|
| CCL1 | 21.76 | 20.53 | 22.17 |
| CCL2 | 23.12 | 22.31 | 23.57 |

Table 4-3 FEA simulation results for bus bar Design II

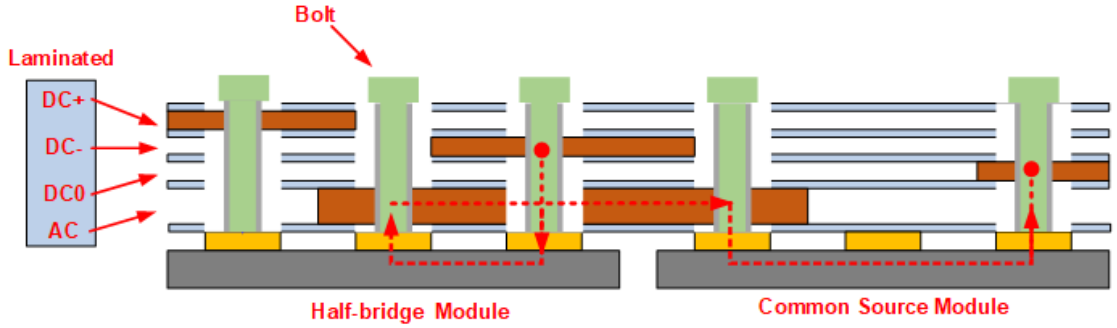
| | Phase A (nH) | Phase B (nH) | Phase C (nH) |
|---|---|---|---|
| CCL1 | 17.46 | 16.68 | 18.28 |
| CCL2 | 17.08 | 16.14 | 17.38 |

Table 4-4 Measured total inductance of busbar Design I with CAP I

| | Phase A (nH) | Phase B (nH) | Phase C (nH) |
|---|---|---|---|
| CCL1 | 30.05 | 27.91 | 28.08 |
| CCL2 | 28.42 | 27.22 | 29.16 |




(a)

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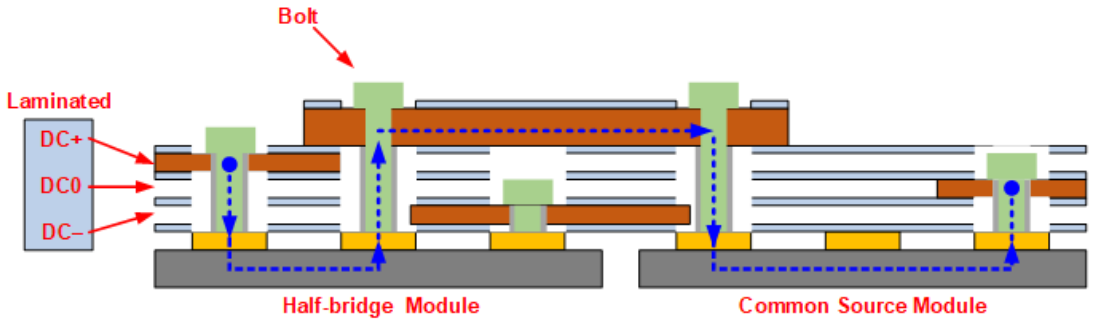
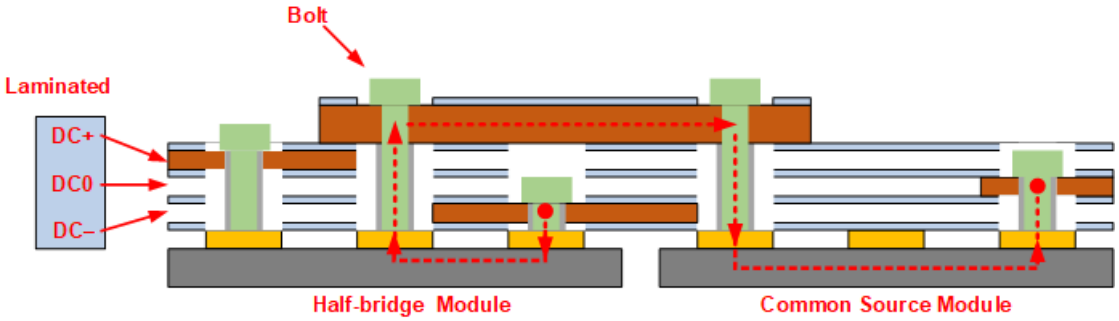



(c)




(d)

Fig. 4-13 Cross section views of bus bars for (a) Design I CCL1, (b) Design I CCL2, (b) Design II CCL1 and (d) Design II CCL2.

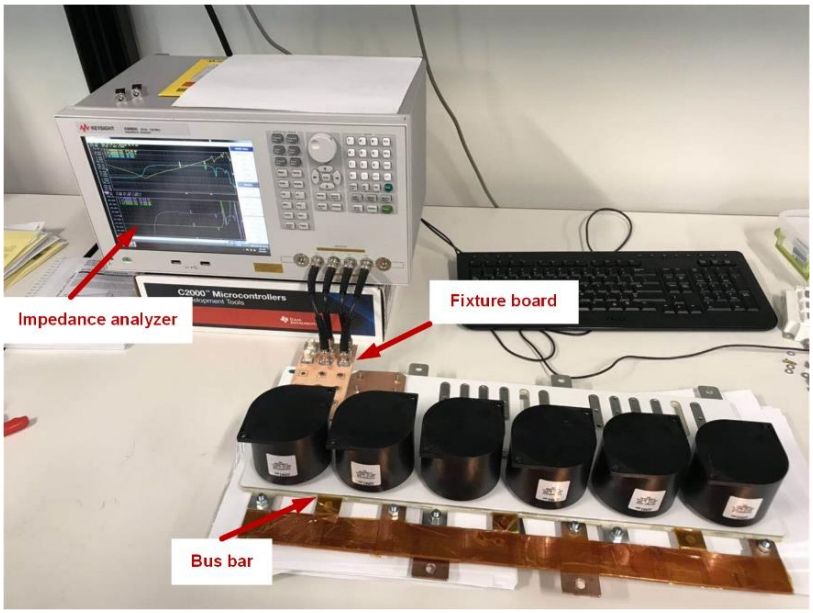
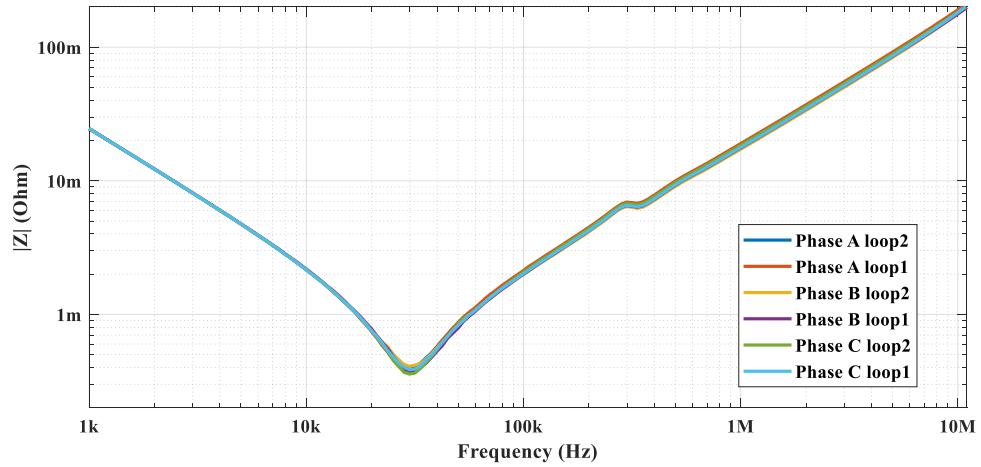



Fig. 4-14 Impedance analyzer extraction setup.

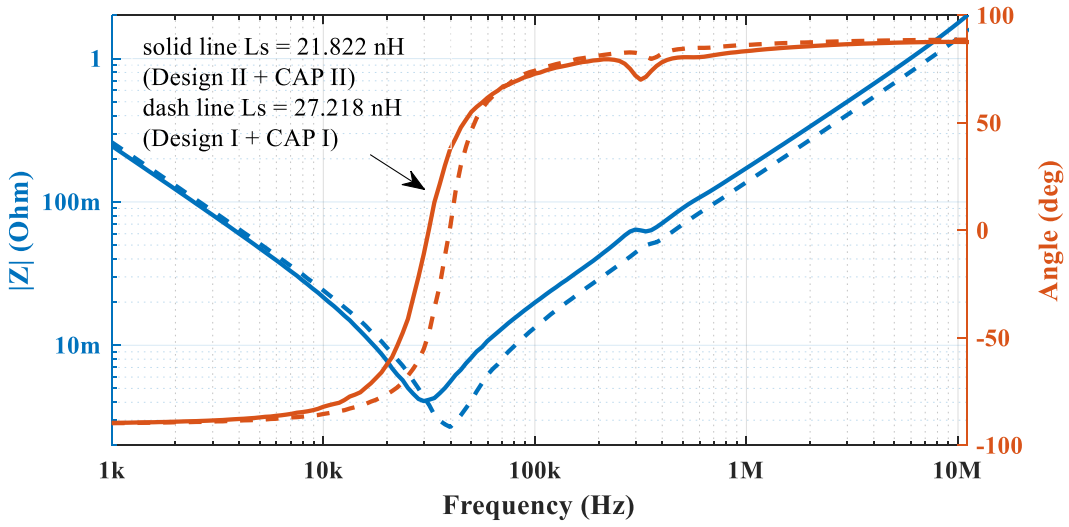
### 4.5.2 Stay inductance measurement using impedance analyzer

The ESL in the DC-link capacitors contributes a significant amount to the entire loop parasitic inductance. The selection process of the DC-link capacitor was presented in [23]. In this work, two kinds of commercial off-the-shelf (COTS) capacitors with similar electrical parameters were investigated. The measured ESL for of them, i.e., CAP I, is 20 nH. While the other capacitor, i.e., CAP II, has lower ESL, which is around 13.9 nH each. The impedance of bus assembly and capacitors are measured by using the Keysight impedance analyzer, and the setup is shown in Fig. 4-14. Fixture boards are designed to connect the dc-link capacitor/bus bars to the impedance analyzer. [34] The DC-link capacitors were bolted on the busbar during the measurement. One copper sheet is used to short the CS module. The measurements were taken between two power terminal spacers for the HB module, i.e., between DC+ and AC for CCL I and between DC- and AC for CCL II. Fig. 4-15(a) shows the measured impedance in each CCL of the busbar Design I with CAP I, and the results were summarized in Table 4-4. The frequency responses and measured parasitic inductances of all CCLs are very close to each other, which validated the symmetrical

bus bar design. Fig. 4-15(b) shows a comparison between Design I with CAP I and Design II with CAP II, which clear shows over 20% reduction in total loop parasitic inductance, from 27.218 nH to 21.822 nH.




(a)




(b)

Fig. 4-15 (a) measured loop impedance of busbar Design I with CAP I and (b) a loop impedance comparison between the busbar Design I with CAP I and busbar Design II with CAP II.

## 4.6 A hybrid bus bar structure with PCB snubber circuit using high-frequency capacitors

In the high-frequency range, the decoupling capacitors $C_{dec}$ can be regarded as a short circuit, which provides a path to the high-frequency current components, which helps to mitigate the voltage overshoot. According to [24], the selection of $C_{dec}$ should meet the following requirement:

$$C_{dec} > 250 \times C_{oss} \tag{4-11}$$

where $C_{oss}$ is the output capacitance of the SiC MOSFET. Multilayer ceramic capacitors (MLCC) are utilized in this work for the decoupling capacitor bank $C_{dec}$. In this T-type topology, $C_{dec}$ is placed between both DC+, DC0, and DC-, DC0, as shown in Fig. 4-16. To reduce the impact brought by ESL of $C_{dec}$, eight 0.33 μF MLCCs are paralleled together to form a capacitor bank across each switch position. The decoupling capacitors should be placed as close to the modules as possible, so the snubber board in this work is directly bolted on top of the busbar, formed a hybrid bus bar structure with snubber a PCB board as shown in Fig. 4-18(d).

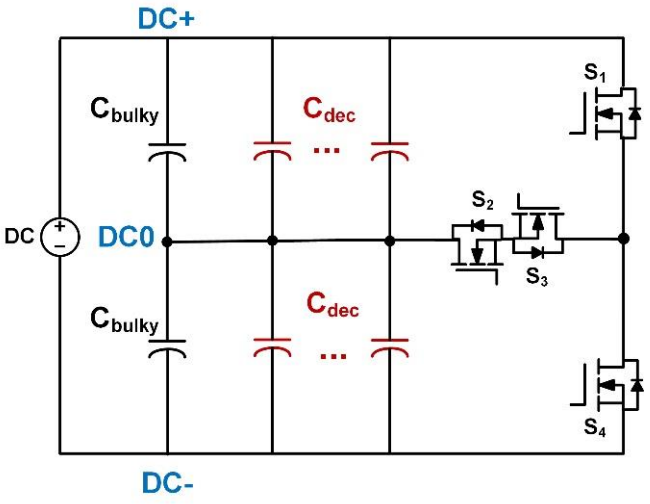



Fig. 4-16 Schematic of T-type topology with decoupling capacitors.

## 4.7 Experimental studies

The T-type inverter was prototyped as shown in Fig. 4-17. Table 4-5 shows the inverter system specifications that are related to the busbar design. Each phase leg consists of one HB module and one CS module. Six 220 μF DC-link capacitors rated at 600 V are used in 2×3 configuration, i.e., 2 capacitors in series and 3 of them in parallel, to form a capacitor bank, which is 330 μF with 1.2 kV voltage rating.

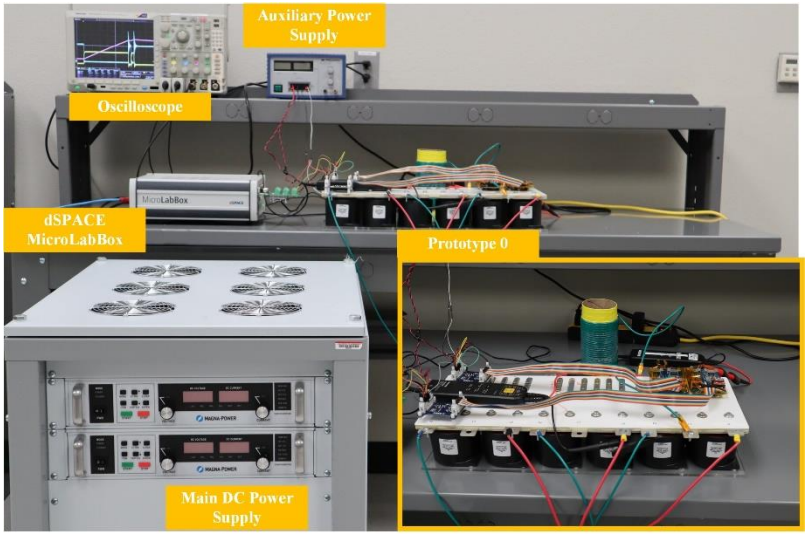
Fig. 4-17 A picture of the T-type inverter prototype.

Table 4-5 Inverter system specifications

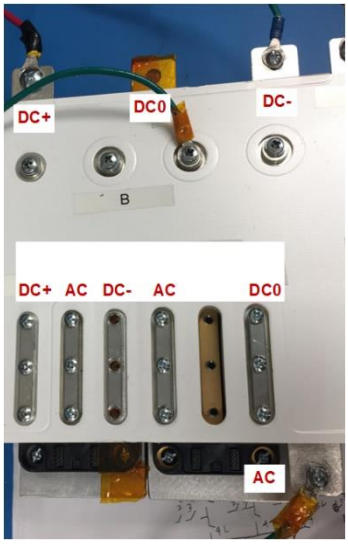
| Parameters | Value |
|---|---|
| Rated power | 250 kW |
| DC-bus voltage | 700 V |
| Phase RMS current | 300 A |
| Switching frequency | 20 kHz |

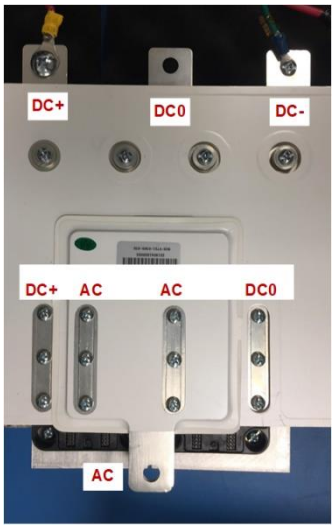
Double pulse tests (DPTs) were performed using the actual prototype to evaluate the switching performance of the modules and the designs of the busbar. The test setup is shown in Fig. 4-18(a). Three configurations are tested, including the busbar Design I with CAP I, the busbar Design II with CAP II, the busbar Design I with CAP I, and the snubber circuit board. The load used for DPT is an air-core inductor with an inductance of 40.2 μH, while turn-off gate resistance $R_{goff}$ is 2.5 Ω. The pulses are generated by dSPACE MicroLabBox. The drain to source voltage is measured by using a differential probe THDP0200, and Rogowski coil is used to sense the inductor current. The schematic of the DPT test for the HB module is shown in Fig. 4-19. The gate pulses are applied to S4 in the HB module, which is the device under test (DUT), and the body diode of S2 in the CS module is the freewheeling diode. In this test, the gate signals for S1 and S2 are always low, while the gate signal for S3 is always high. In this way, D2 and S4 form the standard configuration for a clamped inductive load (CIL) test [27].

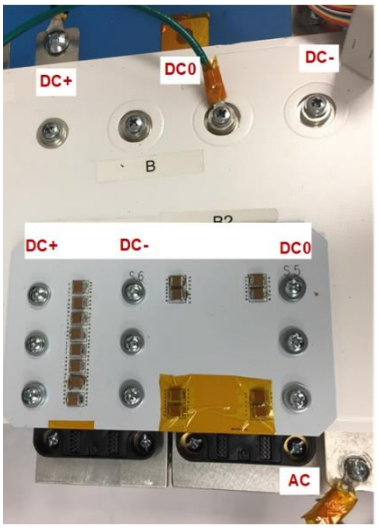
A comparison of all three cases is shown in Fig. 4-20, where the DPT was performed at 700 V DC bus voltage and 450 A load current. Fig. 4-20 shows the drain to source voltage, i.e., Vds of phase B bottom switch position S4 during the turn-off transient, which reflects the CCL2 inductance in phase B. It can be concluded that busbar Design II with CAP II has much lower voltage overshoot than the Design I with CAP I, where a 74 V voltage overshoot reduction can be observed. The design of the snubber board is also effective, which shows over 100 V voltage overshoot reduction. Fig. 4-21 compares the magnitude of voltage overshoot for three cases when DPT tests were performed at different load current. It can be observed that the mitigation of voltage overshoot is consistent from low current to high current. And it is worthwhile noted that voltage overshoot in the case using enhanced busbar design is similar to that in the case using a snubber circuit.




(a)




(b) (c) (d)

Fig. 4-18 (a) The CIL test setup and details of (b) busbar Design I, (c) busbar Design II and (d) busbar Design I with snubbers.

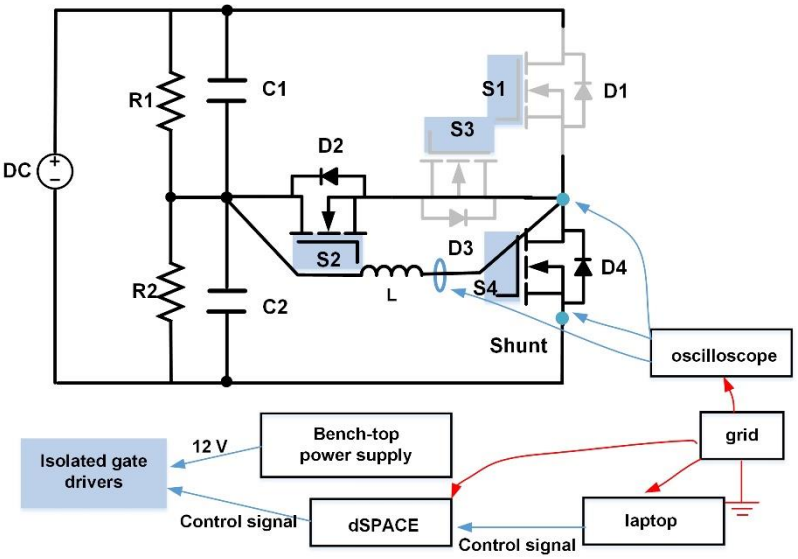



Fig. 4-19 Schematic of CIL test for HB module.

Additional multiple-pulse tests (MPTs) were performed using different configurations, i.e., case I busbar Design I with CAP I, case II busbar Design II with CAP I, and case III busbar Design II with CAP II. The purpose of these tests was to validate the impact of stray inductance from busbar and dc-link capacitors under variable *di/dt*. According to [35], *di/dt* increases with the load current. As can be seen in Fig. 4-22, the voltage overshoot with eight load current conditions from 50 A to 400 A with 50 A interval are measured. Under individual load current, which means individual *di/dt*, it can be seen the voltage overshoot performance comparison like Fig. 4-20 is the same. From Fig. 4-22(a) and (b), it can be observed that voltage overshoot is reduced using a busbar with lower parasitic inductance, while the comparison between Fig. 4-22(b) and (c) clearly shows the voltage overshoot mitigation caused by using DC link capacitors with lower ESL.

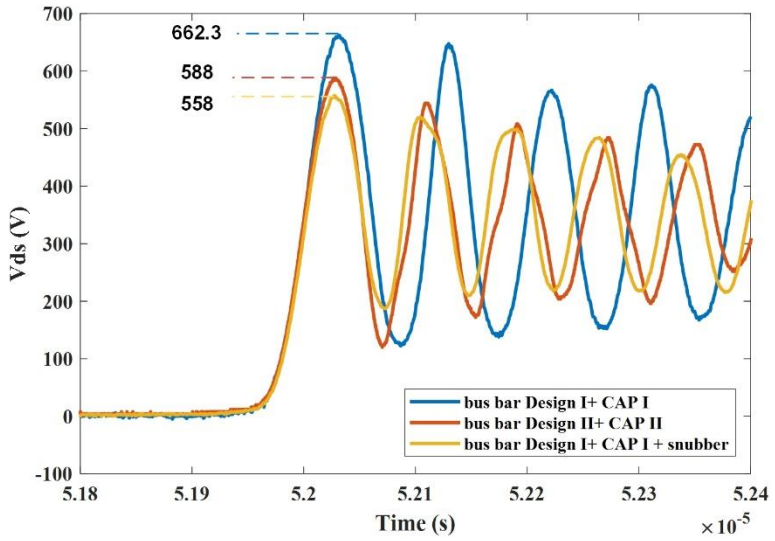



Fig. 4-20 Comparisons of drain to source voltage with 700V dc bus and 450A load current.

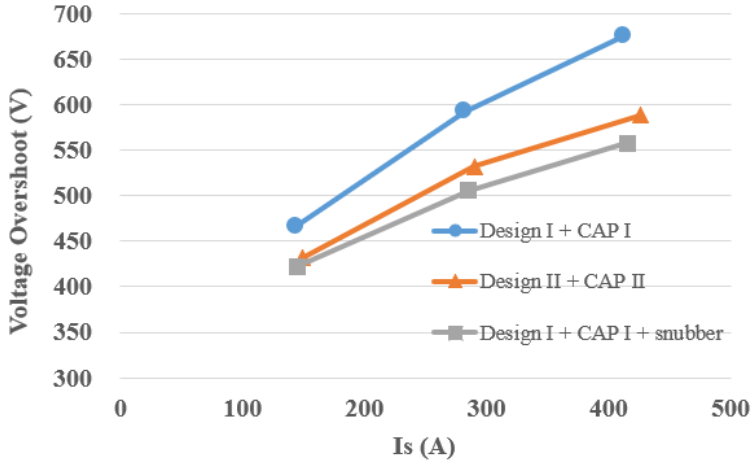
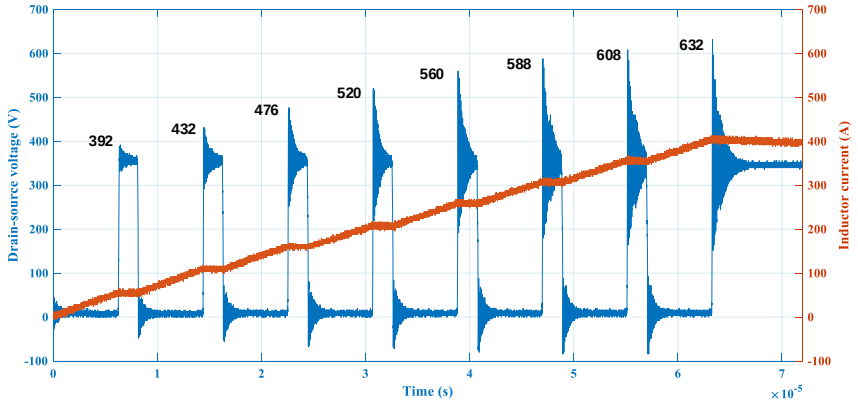
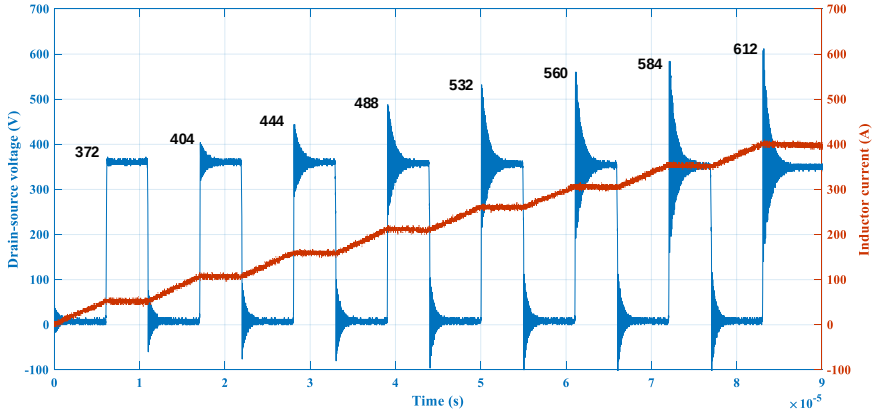


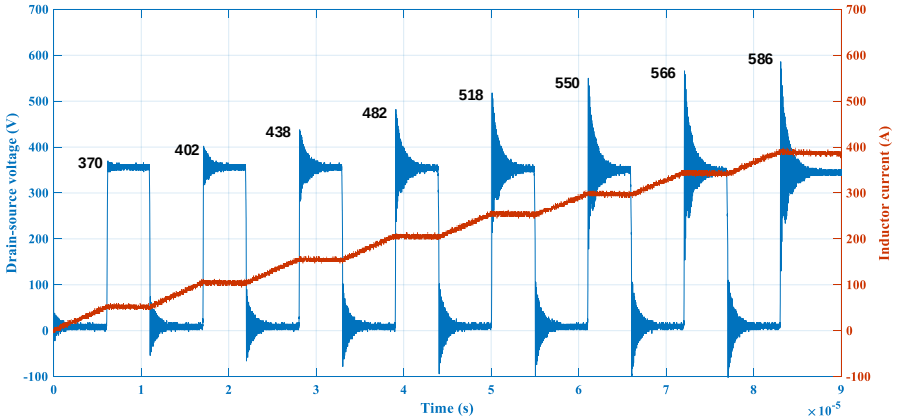

Fig. 4-21 Comparison of voltage overshoot with various load currents.




(a)




(b)




(c)

Fig. 4-22 The drain to source voltage and load current waveforms during the MPTs for (a) busbar Design I + CAP I (b) busbar Design II + CAP I (c) busbar Design II + CAP II.

## 4.8 Conclusion

This paper presented a comprehensive study of the voltage overshoot issues and minimization for a three-phase T-type inverter, including busbar design optimization and adding additional the decoupling circuit. The analysis of CCLs in a single phase T-type phase leg was presented. Then the busbar design and optimization process were described in detail. A novel 3-dimensional bury-screw busbar is proposed to minimize the bus bar parasitic inductance. Stray inductance in each CCL is extracted via FEA simulation and captured using an impedance analyzer. Furthermore, a hybrid bus bar structure with PCB snubber circuit was designed and evaluated to reduce voltage overshoot. Finally, the experimental results were presented to validate the effectiveness of busbar and buffer circuit design.

## Acknowledgment

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# CHAPTER 5

# FIXTURES DESIGN CONSIDERATIONS FOR IMPEDANCE MEASUREMENT



## 5.1 Abstract

The parasitic impedance in a current commutation loop (CCL) is a major factor for the switching performance of power electronics especially the wide bandgap (WBG) devices, which usually generate high *di/dt*. The terminals of components in a CCL may not always be standard. The fixture adapter with clip lead may not be accurate enough for WBG application, while the commercial high bandwidth fixture adapters are not always available. Therefore, it is critical to design fixture adapter boards to make a better interface and mitigate measurement errors. In this work, detailed fixture design procedures are presented. These design methods were validated by comparing with the commercial fixture adapters. In addition, various considerations to further improve the measurement accuracy are discussed, summarized, and evaluated through tests. The dc-link capacitors and the busbar for a half-bridge module are regarded as the device under test, whose impedance is extracted using the proposed fixture design. Finally, the experimental results from the double pulse test verified the accuracy of the proposed fixture design, with an error of less than 1%.

## 5.2 Introduction

The large stray inductance over a current commutation loop (CCL) may lead to switching oscillations, voltage overshoot, and additional power losses [1], [2], especially when using silicon

carbide (SiC) devices. The stray inductances in a high-power CCL may come from 1) dc-link capacitors, 2) the power modules [3], [4], and 3) busbars connecting capacitors to power modules [4]-[7]. For dc-link capacitors, their stray inductance information provided by the manufactures is usually the reference value instead of the actual value, and it is difficult to obtain through the simulation. As a result, it is recommended to measure and compare the stray inductance by using an impedance analyzer during the capacitor selection process. In addition, when a busbar is built, it is necessary to measure the parasitic inductance before its application to ensure its performance can match the finite element analysis (FEA) simulation result [8]-[10] in the early stage. The problem is that the most accurate off-the-shelf adapter fixture with high-bandwidth, e.g., greater than 10MHz, is designed for surface mount device (SMD) or leaded passive device, as shown in Fig. 5-1(a) and (b). When it comes to larger components like dc-link capacitor and custom busbars with screw terminals, the only choice for adapter fixture is clip lead, as shown in Fig. 5-1(c), most of which designed with low-bandwidth accuracy, e.g., less than 100kHz. Meanwhile, the connection between clip leads and device under test (DUT) is not stable, and the measurement result will change when the position of clip leads slightly moves. To solve this problem and make better interface between the impedance analyzer and DUT with different kinds of terminals, it is better to build customized adapter fixtures.

References [11] and [12] claimed that an impedance analyzer with a custom fixture board was used to measure the busbar impedance. However, no details on the fixture board design have been presented. In [13], custom fixture boards were designed for impedance measurement of power modules, and the results obtained using commercial and custom fixtures were compared with each other. However, there are no fixture board design considerations and guidance presented in this literature. In this work, a detailed design procedure on the fixture adapters is presented, which has

not been discussed in the existing literature. In addition, various fixture designs are compared to conclude design guidance. Furthermore, the proposed design approach has been validated by experimental studies.


(a)


(b)

(c)

Fig. 5-1 Commercial fixture adapter of impedance analyzer (a) for SMD (b) for leaded passive device (c) with clip lead.

## 5.3 Measurement by using the commercial fixture adapter

To validate the accuracy of custom fixture designs, a leaded 800V 30 µF capacitor DCP4L053007HD4KSSD from WIMA is selected as a DUT, whose parasitic inductance was

measured by using commercial adapters and custom fixture adapters. Two off-the-shelf fixtures were used, i.e., a B-WIC (1 Hz - 50 MHz) with Bode 100 (1 Hz - 40 MHz), as shown in Fig. 5-2(a) and a 16047E (up to 120 MHz) with impedance analyzer E4990A (20 Hz - 30 MHz), as shown in Fig. 5-2(b).

The measured DUT parasitic inductance, Ls, at 10MHz, using different methods are summarized in Table 5-1. It should be noted that before the measurement, standard open/short/load and open/short calibrations [8] have been completed for B-WIC and 16047E, respectively.

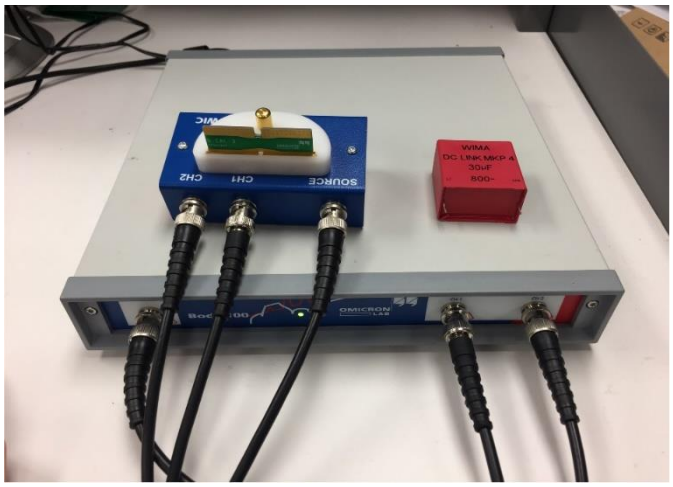
Table 5-1 Measurement result by different methods

| Fixture adapter | Ls (nH) @ 10MHz |
|---|---|
| B-WIC (commercial) | 27.006 |
| 16047E(commercial) | 28.027 |
| Method 1 (customized) | 29.242 |
| Method 2 (customized) | 25.183 |
| Method 3 (customized) | 28.257 |

## 5.4 Design approach for the custom fixture adapter boards

In this section, three fixture design methods are presented for four-terminal (4T) sensing impedance analyzer E4990A. The 4T sensing approach, known as Kelvin sensing [8], uses separate pairs of the current-carrying and the voltage-sensing electrodes to enhance the accuracy compared to the two-terminal (2T) sensing methods. Therefore, the customized fixtures all have four BNC connecters to interface with E4990A, while the inner two ports are for voltage measuring named sense, the outer two ports are for current measuring named force. A pair of sense traces are independent with force traces, such that they do not induce the voltage drop across the force leads

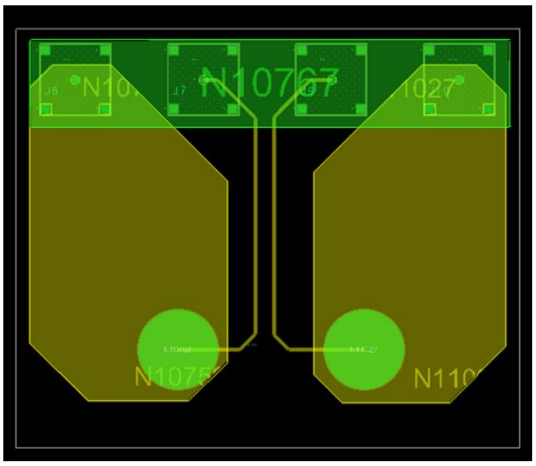
or contacts. Since almost no current flows to the measuring instrument, the voltage drop in the sense leads is negligible.



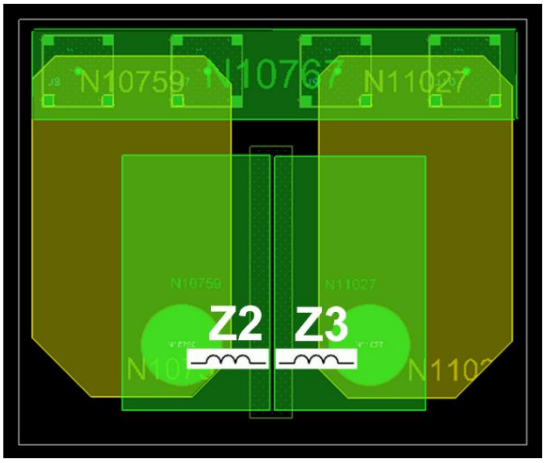

(a)


(b)

Fig. 5-2 Setup for commercial fixture adapters with impedance analyzers (a) B-WIC with Bode 100 (b) 16047E with E4990A.



(a)

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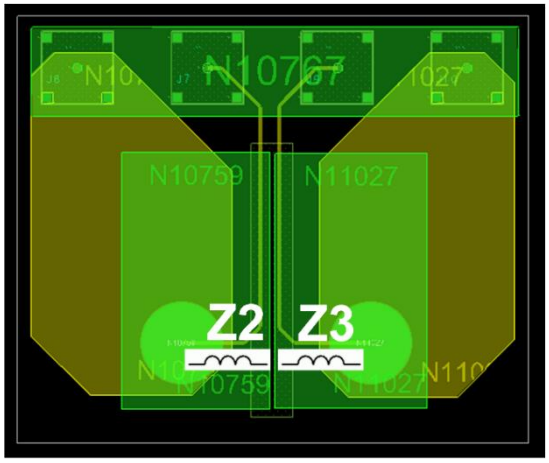



(c)

Fig. 5-3 PCB layout for three customized fixture designs (a) Method 1 (b) Method 2 (c) Method 3.

The PCB layouts of three fixture adapters are shown in Fig. 5-3. Since the impedance of DUT is very small, the current will be large; all force traces use a large gauge to avoid overheating. The traces for the force and sense in Method 2 are the same, while force and sense traces are separated from each other in Methods 1 and 3. In Method 3, the copper layer and solder mask layer are placed on top, which can help the short/load calibration, while in Method 1, the short calibration can be accomplished by using a copper bar, and it is hard to provide load calibration.

Instead of using the BNC cables to connect the fixture board to the impedance analyzer, four L-shape BNC plugs are utilized to mitigate their impact to the measurement. The test setup is shown in Fig. 5-4, and the measurement results are summarized as part of the Table 5-1. As shown in Fig. 5-4(a), a copper bar is used in Method 1 for the short calibration. It should be noted the impedance of the copper bar itself, Z1, should be considered and compensated. For Methods 2 and 3, 0 Ω and 100 Ω SMD resistors are soldered for short/load calibration, respectively. It should be noted that the impedance of the green top traces Z2 and Z3 in these two methods should be considered and compensated.

As can be seen from Table 5-1, the Ls measured using Method 2 is much lower than others, due to the force and sense sharing the same traces, which violates the rules for Kelvin sensing. At the same time, due to the lack of load calibration, the error of Method 1 is greater than Method 3. From the comparisons among these three custom fixture designs, several considerations for the fixture adapter design are summarized as follows.


(a)


(b)


(c)

Fig. 5-4 Test setups for (a) Method 1with an external copper bar connected for the short calibration, (b) Method 2 or 3 and (c) zoomed-in view for Method 3.

1) The force and sense traces should be separated, otherwise, its performance would be similar to the 2T sensing.

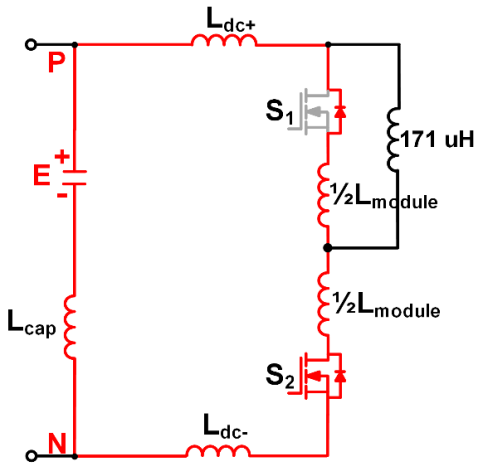
2) Recommend using a large gauge for force trace and small gauge for sense trace.

3) Method 1 and Method 3 has higher accuracy with an error less than 5% compared to the commercial fixtures.

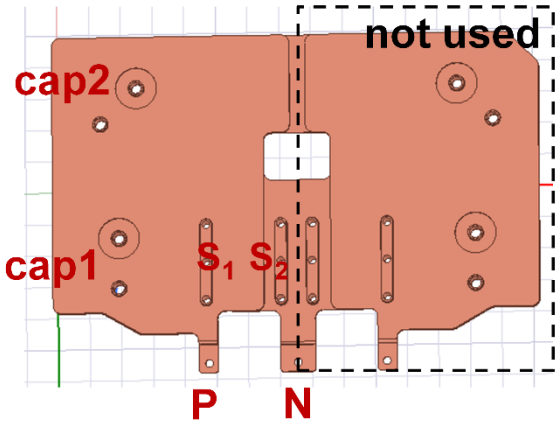
4) It is preferred to use Method 3 since it performs all the open/short/load calibrations.

## 5.5 Experimental validations

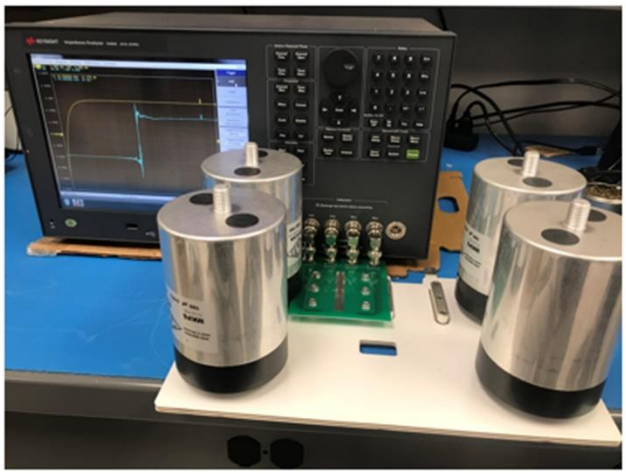
A single-phase HB inverter is used to verify the accuracy of proposed fixture design Method 3, which consists of two 1500V 195 μF WIMA dc-link capacitors DCP6S06195E000 in parallel, a laminated copper busbar and a 1.2 kV SiC HB power module CAS325M12HM2 from Wolfspeed. The schematic of the DPT is shown in Fig. 5-5(a), where the CCL inductance includes the stray inductances of dc-link capacitors, HB module, and busbar. The layout of the busbar was originally designed to connect two HB modules in series, as shown in Fig. 5-5(b). In the DPT test, only one HB is connected to the busbar. The setup for impedance measurement is shown in Fig. 5-5(c), where the capacitors and busbar are connected together as the DUT. The fixture adapter was designed based on Method 3. All open/short/load calibrations were completed before measurement. The result indicates that the summation of $L_{cap}$, $L_{dc+}$ and $L_{dc-}$ equal 18.81 nH at 20MHz, where $L_{cap}$ is the parasitic inductance in dc-link capacitors, and $L_{dc+}$, $L_{dc-}$ represent the parasitic inductance in dc+ and dc- layers of the bus bar, respectively, as shown in Fig. 5-5(a).




(a)




(b)



(c)

Fig. 5-5 HB inverter (a) schematic of its DPT (b) its bus bar layout (c) setup for its impedance measurement (bus bar + dc-link capacitors).

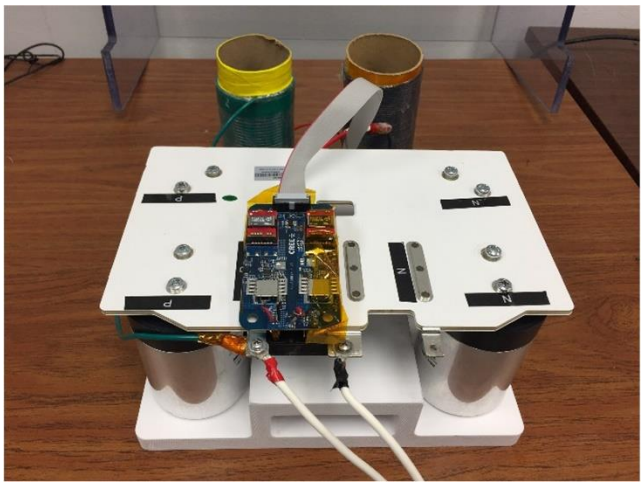
DPT is widely used to evaluate the performance of the power device, and the CCL inductance can be calculated by the resonant frequency from equation (5-1).

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{5-1}$$

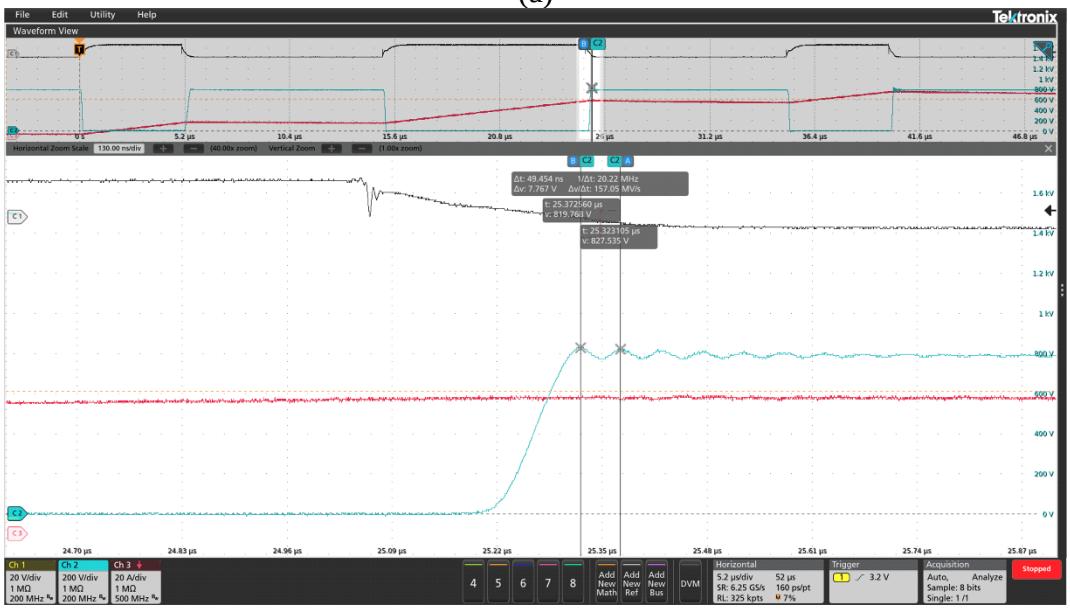
where L is the CCL inductance, as the summation of $L_{cap}$, $L_{dc+}$, $L_{dc-}$ and $L_{module}$; $L_{module}$ is the internal parasitic inductance of the HB module. C is the $C_{oss}$ of the switching device and equals 2.578 nF within the module used in this work.

The DPT setup is shown in Fig. 5-6(a). The load used for DPT is two series-connected air-core inductors with a total inductance of 171 μH. To drive the module, a dual-channel differential isolated gate diver from Wolfspeed is used. DC bus is 800 V. Gate pulses are applied to $S_2$, and the anti-parallel diode of $S_1$ is the freewheeling diode. Drain-source and gate-source voltage are measured by differential probes THDP0200. Inductor current is measured by PEM 30 MHz Rogowski coil.

From the $V_{ds}$ waveform during the turn-off shown in Fig. 5-6(b), it can be seen that the resonant frequency is 20.22 MHz. Then it can be calculated using equation (5-1) and C value from module's datasheet, L equals 24 nH according to the DPT result. Lmodule can be obtained from module's datasheet, which is 5 nH. Then from impedance measurement result, L = 18.81 + 5 = 23.81 nH, with only 0.79% difference comparing from the DPT result. Therefore, the accuracy of fixture design Method 3 can be verified.



(a)




(b)

Fig. 5-6 Half-bridge inverter DPT (a) setup (b) turn-off waveforms.

## 5.6 Conclusion

This paper presents the three different fixture adapter design methods for 4T impedance analyzers. The measurement results are also compared with the commercial ones. Based on their parasitic inductance measurement results, the design considerations and guidance are summarized. Finally, the DPT experimental results have verified that the proposed fixture board design Method 3 is accurate enough.

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# CHAPTER 6

# FIXTURES DESIGN CONSIDERATIONS FOR IMPEDANCE MEASUREMENT

## 6.1 Conclusion

With the increasing application scenarios of high-power inverter, people have much higher requirements for the performance of inverters. Higher power density and higher efficiency are required. In order to meet these two requirements, the emerging SiC MOSFET power device is gradually being applied. At the same time, people also hope to find a new and efficient topology to replace the existing traditional 2-L inverter. Three-level T-type inverter has the advantage of 2-L inverters' low conduction loss, and also can reduce the switching loss and increase the output voltage quality. This dissertation presents a comprehensive design and evaluation methods for high-performance traction converters for EV and other heavy-duty equipment. The dissertation systematically demonstrates the converter design strategy from paper design which optimize the converter regarding optimal topology, DC-link voltage and switching frequency, hardware implementation which reveals key design considerations and busbar optimization strategy, and hardware evaluation which characterize hardware performance by impedance analyzer, double-pulse tests, continuous tests, and thermal evaluation. The dissertation starts with the simulation built-up on paper-design stage, and determines the DC voltage and switching frequency through case studies. At the same time, the CCLs and operation modes of the inverter are analyzed. Then the selection of DC-link capacitors and customized bus bar design were carried out. The experimental part includes HIL simulation verification of the modulation, CIL test and full-power test. The last two chapters of the dissertation also optimized the bus bar design and the impedance analyzer fixture design.

In detail, Chapter 2 discusses converter-level paper design, which optimize the converter configuration based on high-accuracy loss model. This chapter theoretically compared different topology candidates to thoroughly understand the advantages and disadvantages of each topology. Then the optimization of a given topology is implemented by a real-time simulation model, which estimates both switching loss and conduction loss in real time by using switching and conduction loss data table, and operation-model judgement unit for power semiconductors. With the model, the optimal switching frequency and DC-link voltage are fine tuned in order to derive the optimal efficiency design space with satisfaction of load requirements. With DC-link ripple specification, the model also guides the DC-link capacitor design by estimating capacitance and root-mean-squared current. Different modulation strategy can also be verified through the real-time model.

Chapter 3 moves to hardware design and evaluation of the converter. Choosing three-level T-type neutral-point-clamped converter as the topology, this chapter provides operation-mode analysis to reveal the soft-switching and hard-switching behaviors of the converter which is based on SiC-MOSFET. Then the switching loss can be estimated. Using the HIL-based real-time simulation platform built by Chapter 2, the conduction loss and loss distribution of each SiC-MOSFET can be estimated. The loss data can be used to estimated efficiency and determine if efficiency target is achieved. The loss is also one of the important parameters in designing thermal management system. Because SiC-MOSFET has less switching loss, the loss model reveals that the majority efficiency drop is caused by high conductional loss due to SiC-MOSFET on state resistance. The key consideration for selecting gate driver, power module, DC-link capacitors are explained. Eventually, the clamped-inductor test is introduced to evaluate switching performance of the converter. The principle of switching oscillation issue of three-level t-type neutral-point converter is explained. Using clamped-inductor test, switching loss estimation for the designed

converter is explained. Eventually, the converter hardware prototype is present with tested efficiency over 98.5%

In Chapter 4, the details of laminated busbar design are focused. The busbar connects key components in a converter, such as power modules and capacitors. Because the laminated busbar is involved in current communication loop, its stray inductance value should be kept low to limit switching overshoots and switching oscillations. The composition of busbar T-type neutral point clamped converter is proposed. It considers all current commutation loop in T-type converter, and then utilize it as a guidance for busbar design. The influences of self-inductance and mutual inductance are carefully discussed. The influence of DC-link capacitor ESL is discussed as well. In the end, the converter based on designed busbar is introduced. Experiments are conducted to verify the design converter.

Though low-impedance busbar can be designed, evaluating its inductance value can still be difficult. The major challenge is to figure out a fixture design strategy for impedance analyzer in order to characterize non-standard components. Conventionally, the fixture for impedance analyzer is mainly designed for SMD and lead-terminal components. However, accurately measuring the parasitic inductance for non-standard components is difficult. For example, different kinds of DC-link capacitors and busbars with different geometries. Thus, the design of custom fixture board is necessary. In Chapter 5, design of customized fixture board for different kinds of DUT are discussed with the focus on improving measurement accuracy. This chapter starts with a collection the two measurement results for one film capacitor, which are characterized by two commercial fixtures. Taking the measurement results as references, three independent measurements are performed for the same capacitor by using three different customized fixture PCBs. The higher-accuracy fixture PCB can be found by comparing the results to the reference.

The design principle is then summarized and explained in detail. Based on design principle, new fixture PCB is customized for a busbar of 2-level converter. The measurement results show a good alignment to double-pule test results.

## 6.2 Future work

This dissertation has presented the topic about traction converter design, optimization, and evaluation from the aspect of optimal paper design, hardware design and implementation, impedance characterization, testing and evaluation. Busbar, power module and capacitors in this dissertation are designed with margins before reaching SOA boundary. As a result of dissertation, a high-performance traction motor drive is designed with high efficiency and high-power density.

In the future, any breakthrough technology in power electronics area can potentially change the game and might great improve the performance. For example, the DC-link capacitors take a large portions of converter weight and volume. Besides, the large ESL of capacitors limits the switching speed of SiC-MOSFET and reduce system efficiency. The improvement of DC-link capacitors can be foreseen in the near future, including increased current density, capacitance and reduced ESL.

This dissertation has demonstrated the great potential of three-level t-type neutral-point clamped converter in EV applications. However, each single phase of the converter is still built by combination of multiple power modules. Such multiple-module configurations lead to more complicated busbar structure. And the stray inductance is not the optimal because each power module introduces additional terminal inductance. Moreover, the power density could not be optimized in such configuration. In the future work, the design of full-SiC-MOSFET based power module for three-level t-type neutral-point clamped converter is necessary. The integrated power

module has the potential to further improve power density, efficiency, and costs. The system-level design can be simplified and straightforward based on the customized power module.

Improvement of thermal conductivity is one of the most important topics in the future traction converters. Because the positive correlation between on-state resistance and junction temperature, the conventional thermal management system could cause higher conduction loss due to high junction temperature. Besides, the cooling system, such as cold plate dominates the system weights. To further improve the thermal conductivity, advanced cooling system should be researched and implemented in traction converters. Recently, it is seen the pin-fin based cold plate shows great potential, which significantly reduces thermal resistance of cold plate. However, the structure requires advanced metal processing technical. Besides, the baseplate of the power module can integrate with cold plate to avoid using of thermal-interfacing material (TIM).

Busbar is considered for high-power traction converters because of thick copper eliminates conductional loss and pathway overheating. Recently, implementation of thick-copper PCB is another possible choice. Compared to busbar, the thick-copper PCB offers possibility of complicated vias and combination of both signal traces and power plate. However, careful estimation on PCB loss and PCB temperature should be performed.