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Distributed Modeling Approach for Electrical and Thermal Analysis of High-Frequency Transistors

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Analysis of High-Frequency Transistors

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of the requirements for the degree of
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by

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Abstract

The research conducted in this dissertation is focused on developing modeling approaches for analyzing high-frequency transistors and present solutions for optimizing the device output power and gain. First, a literature review of different transistor types utilized in high-frequency regions is conducted and gallium nitride high electron mobility transistor is identified as the promising device for these bands. Different structural configurations and operating modes of these transistors are explained, and their applications are discussed. Equivalent circuit models and physics-based models are also introduced and their limitations for analyzing the small-signal and large-signal behavior of these devices are explained. Next, a model is developed to investigate the thermal properties of different semiconductor substrates. Heat dissipation issues associated with some substrate materials, such as sapphire, silicon, and silicon carbide are identified, and thinning the substrates is proposed as a preliminary solution for addressing them. This leads to a comprehensive and universal approach to increase the heat dissipation capabilities of any substrate material and 2X-3X improvement is achieved according to this novel technique.

Moreover, for analyzing the electrical behavior of these devices, a small-signal model is developed to examine the operation of transistors in the linear regions. This model is obtained based on an equivalent circuit which includes the distributed effects of the device at higher frequency bands. In other words, the wave propagation effects and phase velocity mismatches are considered when developing the model. The obtained results from the developed simulation tool are then compared with the measurements and excellent agreement is achieved between the two cases, which serves as the proof for validation. Additionally, this model is extended to predict and analyze the nonlinear behavior of these transistors and the developed tool is validated according to the obtained large-signal analysis results from measurement. Based on the

developed modeling approach, a novel fabrication technique is also proposed which ensures the high-frequency operability of current devices with the available fabrication technologies, without forfeiting the gain and output power. The technical details regarding this approach and a sample configuration of the electrode model for the transistor based on the proposed design are also provided.

Acknowledgement

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Dedication

To the loving memory of the victims of Flight PS752

And to the memory of Howard C. Baskerville,

who could not be indifferent to the sufferings of people fighting for their rights

Epigraph

“Let the future tell the truth and evaluate each one according to his work and accomplishments.

The present is theirs; the future, for which I have really worked, is mine”

— Nikola Tesla

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List of published papers

Chapter 2: A. G. Avval, E. Larique, and S. M. El-Ghazaly, "Heterojunction field effect transistors" *Reference Module in Materials Science and Materials Engineering*, Amsterdam, The Netherlands: Elsevier, 2018.

Chapter 3: A. G. Avval, S. Yu, G. J. Salamo, and S. M. El-Ghazaly, "Apparatus and method to reduce the thermal resistance of semiconductor substrates," U.S. Patent Application US20200194333A1, Jun. 2020.

Chapter 4: A. G. Avval and S. M. El-Ghazaly, "Distributed-Model-Based Approach for Electrical and Thermal Analysis of High-Frequency GaN HEMTs," *IEEE Access*, vol. 8, pp. 152333-152341, 2020.

Chapter 5: A. G. Avval and S. M. El-Ghazaly, "Increasing transistor gain using metamaterial electrodes," U.S. Patent Application, Serial No. 62/986,906, filed on 03/09/2020.

Chapter 1

Introduction

1.1 Introduction

Systems and devices with high output powers, operating at high-frequency bands have penetrated almost every aspect of the applications in the areas of wireless communications, remote sensing, and aerospace, to name only a few. These two features are the most critical properties of the devices that embody the future of many systems in achieving higher data rates. One of the main categories of these systems is the active microwave devices that, as the name indicates, is expected to operate at the microwave (MW) and millimeter-wave (mm-wave) frequency bands in order to meet the broad bandwidths and reconfigurability requirements. In general, many technologies operating at this frequency range owe their emergence and advancements to the material properties of gallium nitride (GaN) utilized in high electron mobility transistor (HEMT) devices. High saturation velocity, high electron mobility, high sheet carrier density, and high breakdown voltage are some of the characteristics associated with GaN that make it a material that meets the requirements of building high-power amplifiers (HPAs) capable of working at high operating frequencies.

These high-frequency transistors are incorporated in many of the complicated contemporary systems in order to drive a multitude of compact passive and active circuit components and elements that are accompanied by numerous discontinuity levels and transmission line sections. Charge transport, thermal properties, and electromagnetic-wave propagations are some of the topics that must be addressed in such high-performance mm-wave systems, and this must be conducted on more than an individual basis. The reason is mainly due to their diverse physical dimensions in the structure and various frequency scales and power levels while operating. Understanding these subject matters has offered technical cognizance to

enhance the device performance of mm-wave transistors for various applications in terms of increasing their efficiency, gain, bandwidth, and output power.

The gain and RF output power for mm-wave transistors are directly related to the device width, which signifies the direction along the device electrodes perpendicular to the flow of charges. At mm-wave bands, the device electrodes may act as transmission lines due to their large size relative to the wavelength of the guided wave inside the device. In typical transistor configurations, the input impedance (gate to source) and output impedance (drain to source) are significantly different. Consequently, the phase velocities of the propagating waves on the input line, gate electrode, and output line, drain electrode, will be different. This phase velocity mismatch, when exists, causes significant degradations in the device performance, such as reducing the available gain and output power and limiting the maximum operating frequency. To avoid the phase-cancellation effects, the fabricated device width is normally limited to at least less than one-twentieth of the propagating wavelength, which makes the effects of the velocity mismatch ignorable. Consequently, a sufficient number of transistor fingers needs to be incorporated in order to obtain the desired output power. Therefore, numerous interconnects are introduced to the device design which adds more parasitic elements to the system. Hence, in addition to optimizing the semiconductor structure, rearranging the electrode layouts to reduce the phase-velocity mismatch, increase the efficiency, and minimize the effects of discontinuities and signal losses, are of great importance in designing mm-wave transistors.

In this research, three main issues associated with the operation of high-frequency transistors are identified and appropriate solutions are provided. The first issue is related to the thermal management, where the devices are not capable of sufficiently dissipating the internally generated heat. The second problem relates to the limitations with the developed circuit models

for analyzing these devices, where the required reliability and comprehensiveness are not offered by the modeling approaches. The last issue is about the presence of a phase velocity mismatch with the devices operating at mm-wave frequency bands which notably reduces the gain of the device and imposes fabrication limitation. These issues will be briefly explained in the following sections and the extended discussions will be provided in the next chapters.

1.2 Thermal management and heat dissipation issues

Transistor operations are mainly associated with different gain values and output power densities provided at specific frequency bands along with other figures of merit. One of the important factors that has a huge effect on these operating modes and needs to be studied and analyzed when characterizing a semiconductor device, is the operation over different temperature gradients. In GaN HEMTs, due to being a high-power device, a great amount of internal heat is generated, and it affects the electrical behavior of the transistor [1]. Hence, information about the maximum temperature that the device channel can handle is very vital. The generated heat in the channel layer is normally dissipated through the substrate layer and deciding on the optimized material type and structure for this layer is a very critical stage of device design and development [2].

For all types of transistors that are operating at high voltage levels, the created current in the output is very large which translates into the generation of high temperature gradients. These local hot spots that are generally in the vicinity of the gate electrode, if not cooled efficiently, hinder the proper operation of the device or even damage the structure of the transistor. Therefore, the heat handling and dissipation capabilities of the device is very important for a reliable transistor operation at high frequency ranges and high output power levels. The solution

provided in this research is associated with the thermal conductance of the substrate platform on which the device is grown, which leads to improvements in power handling capabilities of the transistor.

For this purpose, different substrate materials and structures are modeled, and rigorous simulation are conducted to identify the thermal issues and present solutions. The initial material to be tested is sapphire which possesses specific characteristics suitable for high-frequency and high-power operations. However, sapphire has a low heat conductivity which gives rise to numerous heat dissipation issues and results in being substituted with other semiconductor substrates, such as silicon carbide, in many applications. This imposes some cost limitations as sapphire is a much cheaper option. In this research, all the simulations are conducted in COSMOL Multiphysics where the dimensions for the structures and the boundary conditions are defined according to practical experiments. The initial step for proposing a holistic fabrication approach for solving the heat dissipation issues with substrates is to consider utilizing thinner platforms in device structures. The simulation results associated with this design is promising and an analytical approach is also employed to further validate the obtained results. From practical viewpoints, the thinner substrates are achieved either prior or after the fabrication process.

The heat transfer model utilized in this study is the conduction heat transfer that mainly relates to temperature gradients in a solid structure. For increasing the heat conduction coefficient, which results in a decrement in thermal resistance of the material, a selective etching process is utilized which is applied on the substrate from backside. The resulting configuration is a substrate which is comprised of materials such as silicon, sapphire, and silicon carbide and includes a plurality of spaced-apart heat sinks that are filled with one or more materials with high

heat conductivity such as copper. The etched section is generally in the shape of a truncated cone for facilitating the process. Practically, the filling process for the hollow etched section is performed through sputtering [3]. For the optimized design, the improvement for the silicon, silicon carbide, and sapphire substrates is 78%, 101%, and 288%, respectively. All the details related to the thermal modeling and optimization of the device structure will be provided in Chapter 3.

1.3 Device analysis and distributed modeling approach

In the recent years, there has been an increasing demand for developing high-power and high-frequency devices for many applications in wireless communication systems, where the circuit models have played a major role in optimizing the design process for advanced state-of-the-art monolithic microwave integrated circuits (MMICs). One of the most critical features of the models developed for individual devices at radio frequency (RF) ranges, is the wideband accuracy. For the microwave and mm-wave ranges, the operation of the devices become distinctly different than their low-frequency counterparts and performance degradations are normally observed in their behavior. The developed equivalent circuit models for these operating bands are comprised of intrinsic- and extrinsic-level elements and the performance drop is generally associated with both of these sections [4]. Hence, for establishing universally-satisfactory circuit models, which incorporate the complicated device topology, the properties of different materials used in fabrication, and underlying physical behavior of the device, care must be taken in identifying the extrinsic parasitic elements of the device interconnects and they must be considered as important components similar to the bias-dependent active elements.

The parasitic couplings of the devices operating at high frequency ranges are mainly referred to as linear elements which depend on the electrode structures, interconnects, and probe pad models. These elements are primarily extracted based on characterizing the fabricated device according to the measurement data. In other words, for a circuit model to be developed when there is a slight variation in the configuration, a new device based on the updated topology must be fabricated and characterized. This process is not cost-efficient and requires long processing times. Additionally, this procedure demands using numerical curve-fitting practices which suffer from convergence to physically-illogical local minima [5]. The key objective for developing a circuit model is to have a simulation platform that provides a tool for design optimizations before the fabrication stage.

In this research, an equivalent circuit model is developed for the analysis of a GaN transistor for the W-band frequencies and beyond. This model is developed solely based on the physical structure of the device and according to the conformal mapping theorem and incremental inductance rule without utilizing the experimental data of the fabricated device. Moreover, the model incorporates the electromagnetic-wave propagation effects and wave-particle interactions by taking advantage of the distributed concepts. This ensures that the model maintains its accuracy at higher frequency bands. The simulation results are provided for different operating modes and the model is validated by the measurement results obtained from the fabricated device. A brief explanation of the model development along with the preliminary results is presented here.

1.3.1 Device structure and circuit model development

The configuration of a nitrogen-polar mm-wave GaN MISHEMT device fabricated by Guidry *et al.* is demonstrated in Fig. 1.1 [6]. The device is grown on a silicon carbide substrate and consists of a GaN buffer layer, an AlGaN back-barrier, a 9.3 nm GaN channel, a 2.6 nm AlGaN layer, and a 47 nm GaN cap. The gate stem height is 250 nm and the trapezoidal form of the gate top ensures the sufficient reduction of the parasitic resistance on the input electrode. The device has a 25 μm width for each of its fingers and the multi-finger layout of the device is designed based on a T-configuration.

The frequency at which the device is operating determines the electromagnetic wavelength of the guided wave inside the device. At higher operating frequencies, the device width and the active component dimensions become comparable to the wavelength, which makes the lumped-element conventional small-signal equivalent circuits inaccurate for modeling, due to the phase velocity mismatch in the input and output. In order to take into account the wave propagation effects, the intrinsic equivalent circuit is combined with the transmission line system, called the extrinsic section, and the resulting configuration is depicted in Fig. 1.2. This model is a typical 19-element small-signal equivalent circuit and is considered as the unit-cell for the distributed model utilized at higher frequencies. In order to simplify the element extraction technique, a quasi-transverse electromagnetic (quasi-TEM) approximation, valid for microwave range operating frequencies, is also considered. The parameters are extracted as follows:

Extrinsic Capacitance: To obtain the values for the coupled capacitors between drain, source, and gate electrodes, the proposed model in is simulated in COMSOL Multiphysics. This tool is used as the 3D Laplace solver for our equations. The conductors are considered to be made of gold and all the boundary conditions are defined accordingly. Since the coupling effects

must be observed on these elements, one of the conductors is excited with a defined voltage and the charge is measured on the other two conductors. The capacitance value is equal to the observed charge divided by the voltage.

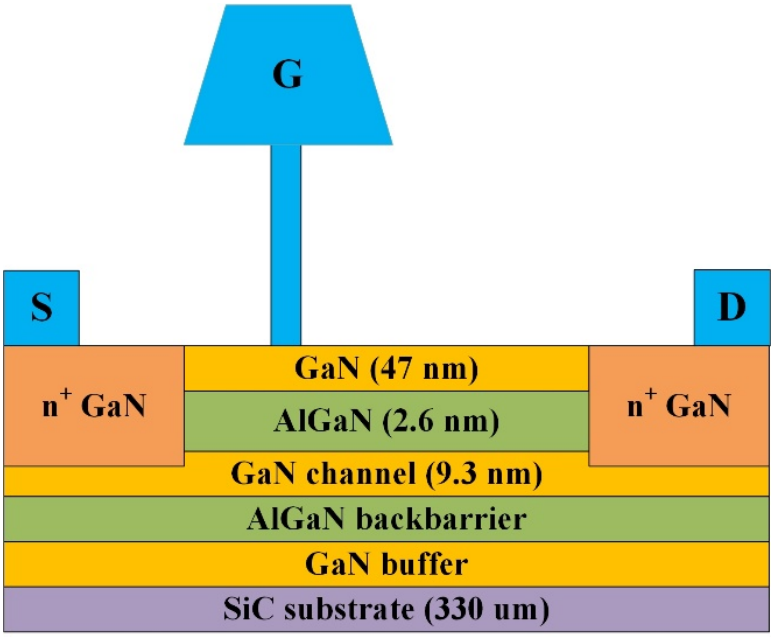

Fig. 1.1 GaN MISHEMT cross-section.

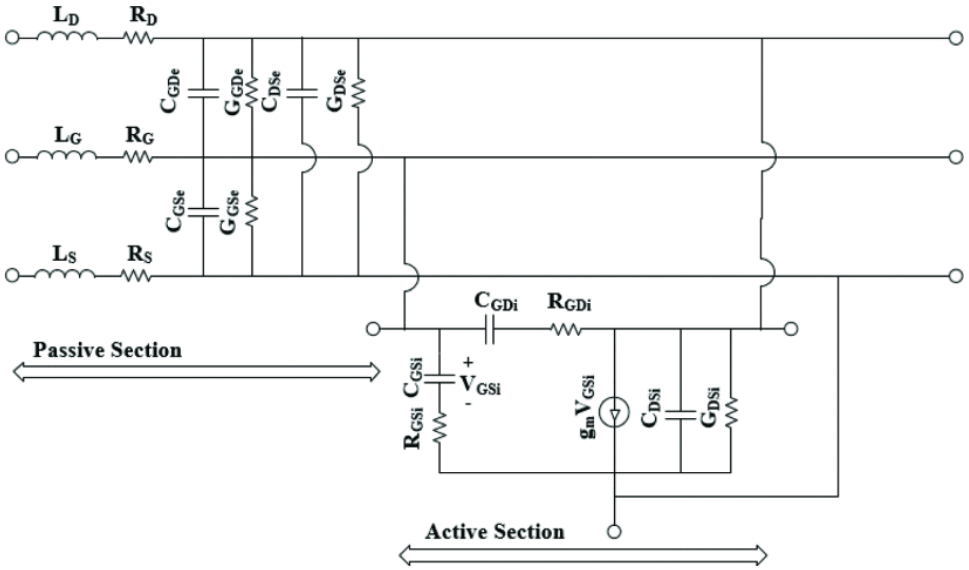

Fig. 1.2 19-element small-signal equivalent model for high frequency transistors and the representative of a unit-cell for the distributed model.

Extrinsic Inductance: According to quasi-TEM approximation, the magnetic field solution around the device is not affected by the presence of III-Nitride semiconductor layers and the substrate under the conductors. Therefore, similar to obtaining the capacitance, the same device is structured in COMSOL Multiphysics without considering the semiconductor layers. First, the capacitance on each line is measured by exciting one electrode and observing the charge on that same electrode. Then, as the phase velocity is the same as the speed of light in free space, the inductance of each line is calculated using Equation (1.1). c is the speed of light in free space and L and C are the inductance and capacitance per unit width of the device, respectively.

$$L = \frac{1}{C \times c^2} \tag{1.1}$$

Extrinsic Conductance: Similar to the approach implemented for finding the extrinsic capacitance, the device structure is arranged in COMSOL. To define the conductivity parameter of the semiconductor layers, carrier concentration and mobility of electrons and holes are considered. This parameter is mostly controlled by the characteristics of the channel layer and the 2DEG (two-dimensional electron gas) layer in high-frequency devices. Due to the coupling nature of the conductance in this model, a voltage is applied on a conductor and the current is observed on the other two electrodes.

Extrinsic Resistance: The conductor loss for all the electrodes is obtained using Wheeler's incremental inductance rule [7]. As the magnetic field penetrates into the electrode, an internal inductance is created. To obtain the value of the internal inductance, first, the external inductance is calculated as mentioned above. Then, all the dimensions of the conductors are reduced by half the skin depth and the external inductance is calculated again. The difference

between the external inductance of these two cases is equal to the internal inductance, which is multiplied by the angular frequency to give us the value of resistance on each line.

Intrinsic Elements: The parameters for the intrinsic section of the device are also obtained using the already developed extraction methods as explained in [8]. These parameters are dependent on the bias point and represent the active characteristics of the transistor. The obtained values for the full small-signal equivalent model are summarized in Table 1.1. The parameters are provided in per-unit width of the device.

Table 1.1 Small-Signal parameter values

Extrinsic Parameters		**Intrinsic Parameters**
$L_S = 2.40\ nH/cm$	$C_{GDe} = 314\ fF/cm$	$C_{GSi} = 8.38\ pF/cm$
$L_G = 2.58\ nH/cm$	$C_{GSe} = 898\ fF/cm$	$R_{GSi} = 5.56\ m\Omega.cm$
$L_D = 4.48\ nH/cm$	$C_{DSe} = 572\ fF/cm$	$C_{GDi} = 332\ fF/cm$
$R_S = 60\ \Omega/cm$	$G_{GDe} = 22\ mS/cm$	$R_{GDi} = 238\ m\Omega.cm$
$R_G = 165\ \Omega/cm$	$G_{GSe} = 63\ mS/cm$	$C_{DSi} = 21.5\ pF/cm$
$R_D = 60\ \Omega/cm$	$G_{DS} = 29\ mS/cm$	$G_{DSi} = 1.70\ S/cm$
		$g_m = 6.10\ S/cm$

1.3.2 Distributed model

The distributed model applied in this research begins with connecting N unit cells of the small-signal equivalent model, shown in Fig. 1.2, to represent the whole width of the device. To decide on the value for N, the wavelength of the propagating signal is calculated and as a rule of thumb, the unit cell length (ΔZ) must be at least 10 times smaller than that. The source and boundary conditions are then incorporated into the distributed model. For analyzing the governing equations to find the voltage and current values at different operating frequencies, a

finite-difference time-domain approach is utilized. Initially, all the parameters are set to zero and then all the currents and voltages are updated at each time interval. Initially, the finite difference method was solved based on an explicit scheme, where the current was updated first and then the new value for the voltage was obtained based on that [8-9]. Since the explicit method is potentially unstable, to satisfy the Courant stability condition and the convergence of the proposed method, the temporal step size, Δt, was on the order of 10^{-16} seconds. This value was very small and increased the computation time of the simulation.

In a later study, the proposed scheme becomes an unconditionally stable implicit method. All the currents and voltages are defined in a coupled set of equations and to obtain the solution, iterative or matrix techniques are utilized, starting from initial transient states to a final steady-state condition. The two governing relations in Equations (1.2) and (1.3) denote the behavior of the parameters on different lines and nodes and the implicit finite difference scheme is applied to them. The time step Δt for this scheme is on the order of 10^{-13} seconds, which makes the computation time become much smaller than the explicit case.

$$V + RI + L\frac{\partial I}{\partial t} = V_s \tag{1.2}$$

$$I + GV + C\frac{\partial V}{\partial t} = 0 \tag{1.3}$$

1.3.3 Simulation results and model validation

Fig. 1.3 (a) depicts the current in the input and output of the device. It is obtained for a ΔZ of 20 μm and a temporal step size of 2e-16 seconds (explicit scheme). The input current is the gate current at the very first cell and the output is the current on the drain line of the last cell. The current gain of the device is 5.5 dB. As illustrated in this figure, it takes some time for the output current to start to have some values. This is the time at which the wave reaches the end of

the device and the calculated velocity using this time needs to satisfy the Courant condition if the solution is stable.

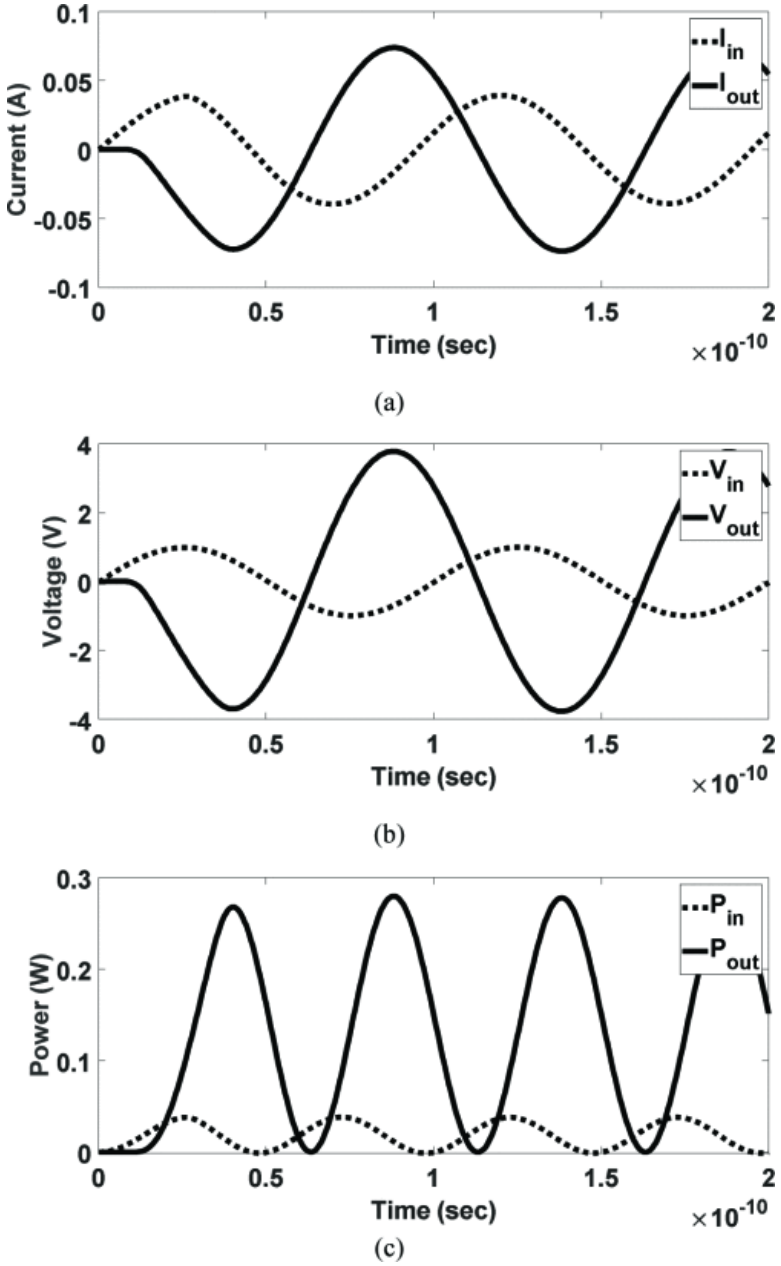

Fig. 1.3 Obtained results at the input and output of the device over time.

Similarly, Fig. 1.3 (b) and (c) show the input and output voltages and powers for the same analysis. The voltage gain and power gain are 11.7 dB and 17.2 dB, respectively. It is clear that the power gain is the sum of current and voltage gains. The proposed model here is merely a

small-signal model and will not be able to handle any DC or large signal analysis. Comparing the obtained current gain with the results in [10] signifies a good agreement mainly in higher frequency ranges (6-67 GHz).

After developing the distributed model, the boundary conditions are applied based on the multi-finger configuration of the device and pad layouts. The small-signal results are obtained under 12 V and 500 mA/mm class-AB bias condition. Fig. 1.4 and Fig. 1.5 show the comparison between the simulation and measurement results for the 2×25 μm GaN MISHEMT device. The current gain (h_{21}), maximum available gain (MAG), and unilateral gain (U) are obtained over the frequency range of 0.25-67 GHz. According to the device width and the maximum operating frequency, using two unit-cells is sufficient for ensuring that the wave propagation effects are included in the model. For the case of current gain, the load impedance is set to zero and for the MAG, the impedance at the output is matched to the circuit. For obtaining the U gain through simulation, the internal feedback is ignored in the circuit model. The obtained simulation results have a good agreement with the measurement results, which validates the proposed method in this research.

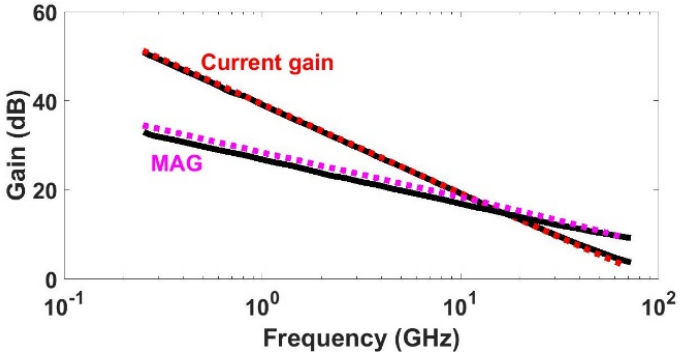

Fig. 1.4 Simulated (dashed) and measured (solid) current gain and MAG results over 0.25-67 GHz.

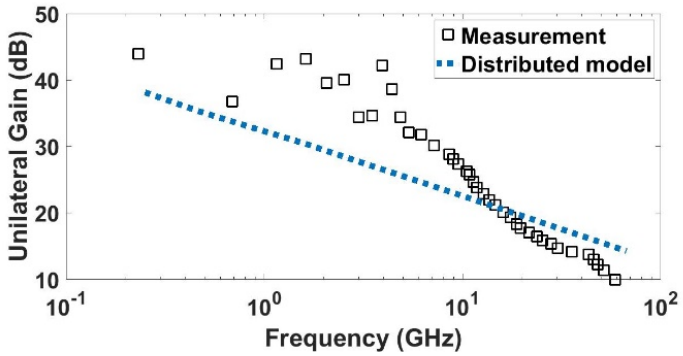

Fig. 1.5 Unilateral gain comparison results over 0.25-67 GHz.

For extending the small-signal model to the large-signal model, the values for the intrinsic elements need to be obtained for different bias points. Subsequently, the data points are incorporated in the FDTD code, and the results are obtained according to the applied input power. It is worth noting that the extrinsic elements will remain the same for different bias points and operating frequencies as they represent the electrode configurations and device pad layouts. The detailed explanation of how to account for the nonlinear effects and electromagnetic wave propagations, and how to solve the phase mismatch issues will be presented in Chapters 4 and 5.

1.4 Optimized electrode design

The wave propagation effects and mismatch issues have a significant impact on how the devices are fabricated and operated. Here is an example where these effects are explained, and a solution is provided. The wavelength for a wave propagating in free space at 60 GHz is equal to 5 mm. However, for a guided wave operating at the same frequency inside a semiconductor device such as HEMT, since the propagation speed is almost one-third of that in free space, the guided wavelength becomes roughly 1.67 mm. If the device width is assumed to be equal to 0.3 mm, since the number is not smaller than at least one-tenth of the guided wavelength, this

dimension becomes comparable to it. As a result, the electromagnetic-wave propagation effects will be significant and there will be a phase velocity mismatch at the input and output ports of the device. In order to have a point of comparison, the value for the current gain of the mentioned device operating at 60 GHz is calculated, which is equal to 3.85 dB.

In order to assess and compare the effects of the mismatch on the device gain, the phase velocity is obtained on the gate and drain electrodes. First, the device is simulated in an even or gate excitation mode and the per-unit-width extrinsic capacitance on the gate line is calculated. Adding the capacitance from the intrinsic section of the model to this value yields the total capacitance for the even mode analysis. By incorporating the per-unit-width value for the gate inductance in Equation (1.4) the input phase velocity is calculated. Similarly, another simulation is conducted for analyzing the device in an odd or drain excitation mode condition and the extrinsic capacitance of the drain line is obtained and then added to the intrinsic value. Subsequently, the resultant capacitance and the drain inductance value is plugged in Equation (1.4) to obtain the phase velocity value on the drain conductor. Table 1.2 demonstrates the parameter values for the two analyses along with the obtained phase velocities.

$$v_{ph} = \frac{1}{\sqrt{LC}} \tag{1.4}$$

Table 1.2 Parameter values associated with calculating the phase velocity for the even/odd mode analyses.

Electrode	Extrinsic Capacitance (F/cm)	Total Capacitance (F/cm)	Line Inductance (H/cm)	Phase Velocity (cm/s)
Gate (input)	1.21e-12	1.04e-11	2.58e-9	6.10e+9
Drain (output)	8.26e-13	2.95e-12	4.48e-9	8.70e+9

Clearly, there is a 43% phase velocity mismatch on the input, gate electrode, and output, drain electrode, which will affect the gain of the device. To improve the performance of this transistor, and other millimeter-wave transistors in general, the electrodes must be designed so as to provide matched phase velocities on the ports. In other words, the optimized electrode layouts will compensate for the mismatch in phase velocity induced by the intrinsic properties of the transistor. The proposed design approach in this work is to utilize the metamaterial concepts for redesigning the electrodes. The technique is to arrange the electrode layouts in some defined repeating patterns to enable the device to manipulate the electromagnetic waves. The transistors designed based on the new electrode configurations may be realized in wider fingers due to the matched phase velocities at the input and output ports. In other words, the electromagnetic-wave effects are compensated and the limitation of keeping the transistor width less than one-tenth of the guided wavelength is eliminated. Consequently, a much smaller number of wider devices will be capable of providing a certain power and the losses, discontinuities, and transistor footprint will be significantly reduced.

The proposed metamaterial concept is applied to the drain electrode in order to achieve a matched phase velocity at the input and output ports. The aforementioned even mode analysis procedure is utilized for the new design and the new values are obtained for the per-unit-width capacitance and inductance of the drain line. The new phase velocity on the drain conductor is calculated and the results are presented in Table 1.3. Evidently, the new drain phase velocity is identical to the phase velocity of the gate electrode. The current gain for the new design is calculated for the device with a width of 300 μm and operating frequency of 60 GHz. This value increased by a factor of 130% compared to the conventional case and reached the value of 8.86

dB. Chapter 5 will explicitly explain how this approach is developed and an example of the electrode configuration will also be provided.

Table 1.3 Parameter values associated with calculating the phase velocity on the metamaterial drain electrode.

Metamaterial Electrode	Extrinsic Capacitance (F/cm)	Total Capacitance (F/cm)	Line Inductance (H/cm)	Phase Velocity (cm/s)
Drain (output)	1.39e-12	3.51e-12	7.35e-9	6.22e+9

1.5 Dissertation objectives and motivation

One of the major challenges in developing systems for high-frequency applications is the lack of accurate, comprehensive, and universally satisfactory modeling approaches. To make sure that the systems in 5G and 6G technologies have the required efficiency to provide enough output in the designated frequency ranges, every aspect of the device operation must be optimized. This optimization is generally performed by the modeling approaches developed for transistors. However, the already developed approaches have several limitations. These models are mainly developed after the fabrication process and the measurement results are utilized in obtaining the model. This is probably the most important limitation with the available modeling approaches. The optimization must be performed before the fabrication stage to save money, time, and resources. Additionally, in mm-wave ranges, the models are generally developed for a specific device type and frequency range and if the operating mode changes, the model does not yield accurate results. Hence, there is a huge demand for modeling techniques that addresses the mentioned limitations.

The overall objective of this research is to develop a technique that can be utilized for modeling transistors regardless of the device type, operating mode, and frequency range. For this

purpose, the technique needs to be based on the physical structure of the device to make sure that any device type can be modeled using this technique and the tool is available before the fabrication stage. Additionally, the model needs to include some physical phenomena, specific to the mm-wave frequency range, to make ensure that the developed approach is accurate independent of the operating frequency. Moreover, to make sure that the developed model is comprehensive, both the electrical and thermal properties of the device must be considered in the process.

1.6 Dissertation organization

This dissertation is organized into six chapters. Chapter 1 introduces the background, problems to be addressed in this research, preliminary results, and motivations and objectives. Chapter 2 explains the review of relevant literature for this research related to the device types, different modeling approaches, and their applications. Chapter 3 presents the thermal modeling procedure of the transistor along with a patented fabrication technique for enhancing the heat dissipation capabilities of the device. Chapter 4 discusses the developed small-signal model along with the device analysis and model validation process. Chapter 5 presents the large-signal analysis of the device, and a patented fabrication technique is also demonstrated which solves the device limitations for operating at higher frequency bands. Lastly, chapter 6 summarizes the research and presents the contributions and future work.

1.7 References

[1] S. Cheng, C. Li, C. Liu, and P. Chou, "Characterization and thermal analysis of packaged AlGaN/GaN power HEMT," *2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2011, pp. 195-197.

[2] A. Syed, M. J. Islam, S. M. Hasanuzzaman, A. K. Podder, M. S. Islam, and A. G. Bhuiyan, "Theoretical analysis of substrate effects on the DC performance of AlGaN/GaN high electron mobility transistor," *2016 5th International Conference on Informatics Electronics and Vision (ICIEV)*, pp. 961-966, 2016.

[3] G. Greczynski, J. Jensen, and L. Hultman, "CrNx Films Prepared by DC Magnetron Sputtering and High-Power Pulsed Magnetron Sputtering: A Comparative Study," *IEEE Transactions on Plasma Science*, vol. 38, no. 11, pp. 3046-3056, Nov. 2010.

[4] Y. Karisan, C. Caglayan, G. C. Trichopoulos and K. Sertel, "Lumped-element equivalent-circuit modeling of millimeter-wave HEMT parasitics through full-wave electromagnetic analysis," in IEEE Trans. Microw. Theory Techn., vol. 64, no. 5, pp. 1419-1430, May 2016.

[5] F. Y. Huang, X. S. Tang, Z. N. Wei, L. H. Zhang, and N. Jiang, "An improved small-signal equivalent circuit for GaN high-electron mobility transistors," in IEEE Electron Device Lett., vol. 37, no. 11, pp. 1399-1402, Nov. 2016.

[6] M. Guidry et al., "Small-signal model extraction of mm-wave N-polar GaN MISHEMT exhibiting record performance: analysis of gain and validation by 94 GHz loadpull," 2016 IEEE MTT-S Int. Microw. Symp. (IMS), San Francisco, CA, 2016, pp. 1-4.

[7] H. A. Wheeler, "Formulas for the skin effect," *Proceedings of the IRE*, vol. 30, no. 9, pp. 412-424, 1942.

[8] A. G. Avval and S. M. El-Ghazaly, "A new small-signal modelling approach for analyzing HEMTs over a broad frequency range," *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 706-709, 2019.

[9] A. Ghadimi and S. Asadi, "Modelling of composite right/left-handed active multiconductor transmission lines (AMCTL) in time domain," *Int J Numer Model.*, 2018.

[10] X. Zheng et al., "High frequency N-polar GaN planar MIS-HEMTs on sapphire with high breakdown and low dispersion," *2016 Lester Eastman Conference (LEC)*, pp. 42-45, 2016.

Chapter 2

Heterojunction field effect transistors

Authors: Amirreza G. Avval, Emmanuel Larique, Samir M. El-Ghazaly

2.1 Introduction

A FET is essentially a semiconductor current path whose conductance is controlled by applying an electric field perpendicular to the current. This field and the carrier density in the semiconductor channel are changed by a voltage imposed on a metal gate. The more electrons in the channel, the higher its conductivity and better performance is obtained from the transistor. Moreover, with the development of heterostructure science and technology, heterojunction FETs now offer potential advantages in microwave, millimeter-wave, and high-speed digital integrated circuit applications over the former homojunction devices [1].

Contrary to the conventional GaAs metal semiconductor field effect transistor (MESFET) which has been one of the most widely used device structures for microwave applications [2], heterojunction field effect transistors (HFET) are more mature semiconductor components of the new generation of III-V transistors. Different names are used for these devices signifying the underlying physical mechanism or structural configuration. Examples are high electron mobility transistor (HEMT), selectively doped heterojunction transistor (SDHT), modulation-doped FET (MODFET), and two-dimensional electron gas FET (TEGFET). For convenience, only the HEMT types will be covered in this chapter. Despite their different names, all these components are based on the same physical theory.

With the recent advancements in mobile communication applications, TV broadcasting, and satellite communications, microwave transistors and wide bandgap materials have been the area of focus for many research groups and these components play a critical role in many technology viewpoints. Table 2.1 presents the material properties of some microwave

semiconductors where the advantages of GaN semiconductor over its counterparts can be readily explained [3]. A high output power per unit width and high temperature operation require a semiconductor material with higher bandgap. This leads to fabricating compact devices that are easily matched when integrated with other circuit elements and the need for extra cooling will be either eliminated or reduced. For using a device in high power mode, a high voltage operation is necessary for the device, and this is fulfilled by using a material with high breakdown field. This will either reduce or completely eliminate the need for a step-down converter in devices. A high gain and high velocity are the two enabling features of the demand for a low noise device generally used in all types of receivers with a high dynamic range. Additionally, a high electron velocity in a HEMT topology will have a performance advantage of an optimum band allocation and it is required that the material used in the device indicate a high linearity and high frequency operation. All these demands and features make GaN devices be a reliable choice for many advanced operations [4].

Table 2.1 Properties of competing semiconductor materials [3].

Material	Mobility	Dielectric Constant	Bandgap	Breakdown Field	Tmax
Si	1300	11.4	1.12	$0.3*10^6$	300 °C
GaAs	5000	13.1	1.42	$0.4*10^6$	300 °C
4H-SiC	260	9.7	3.2	$3.5*10^6$	600 °C
GaN	1500	9.5	3.4	$2.0*10^6$	700 °C

There are many reports on GaN HEMTs operating at high frequencies as power amplifiers with high output power densities and power added efficiencies. Some high-power examples are 10.5 W/mm operating at 40 GHz [5], 13.7 W/mm at 30 GHz [6], and 41.4 W/mm

at 4 GHz [7]. Millimeter-wave N-polar GaN MISHEMT on SiC substrate with 6.5 W/mm power density operating at 94 GHz [8] and a 4.2 W/mm device at the same operating frequency fabricated on sapphire substrate [9] are also two reports on high frequency operations of GaN HEMTs.

2.2 Passive and active characteristics of HEMTs

2.2.1 Metallic passive structure

The cross-section of a HEMT is illustrated in Fig. 2.1. Three metal electrode contacts are made to the surface of the semiconductor structure. These contacts are named source, gate, and drain. The figure shows several important geometric dimensions: L, z, L_{gs}, L_{gd}, L_s, and L_d. The most important dimension that characterizes the HEMT physical structure is the gate length L. This dimension is critical in determining the maximum frequency limits for HEMT structures. The cutoff frequency (f_t) is given by Equation (2.1), where v_s is the saturation velocity of the carrier. The gate width z affects the device performance significantly. It can vary from about 100 to 2000 times the gate length. The device current is directly proportional to gate width because the cross-sectional area available for channel current is proportional to z.

$$f_t = \frac{v_s}{2\pi L} \tag{2.1}$$

The range of these dimensions used in the fabrication of HEMTs is typically identical to that used in MESFET fabrication, so the physical layouts of HEMTs and MESFETs are usually identical [10]. For both MESFETs and HEMTs a transistor referred to as a 4×75 μm device is composed of four gate electrodes, each being 75 μm wide. However, the important phenomena controlling the operation of MESFETs and HEMTs are different. Indeed, the HEMT structure is significantly more complex than the MESFET one. This complexity is associated with

fabrication difficulties, added costs, and lower yields. The primary motivation for pursuing such a structure is a notable improvement in the high frequency and power performance.

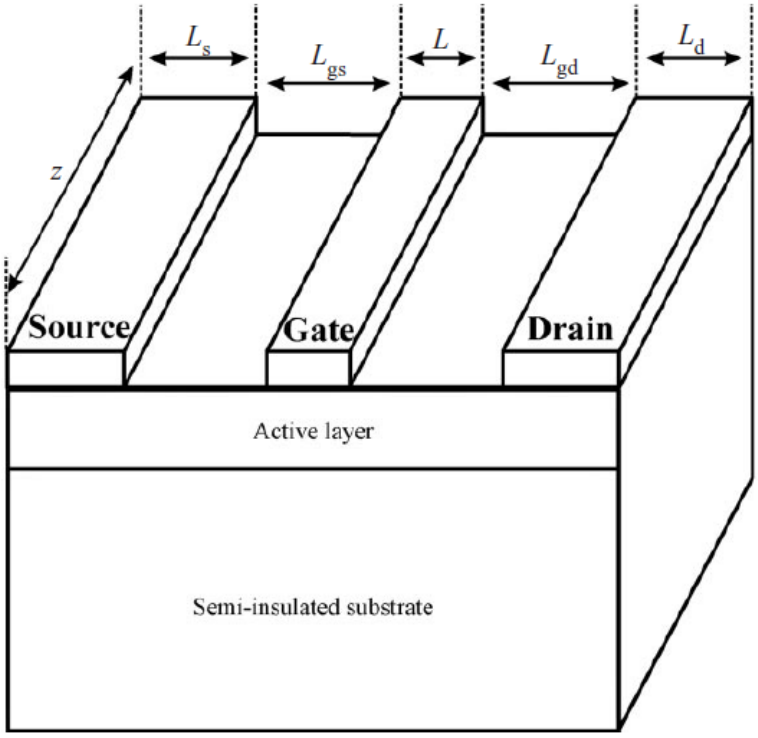

Fig. 2.1 A HEMT structure along with important dimensions.

2.2.2 Intrinsic semiconductor structure

The heterojunction FETs are formed between semiconductors of different compositions, lattice constants, and bandgaps, such as AlGaN/GaN and InGaAs/InP. A schematic cross-section of a conventional n-AlGaN HEMT structure is shown in Fig. 2.2. Typical doping densities and thicknesses of the various epitaxial layers are indicated. The dimensions of both the n-type AlGaN and the undoped AlGaN spacer layer are critical in determining the device behavior. The idea of modulation doping is to separate the carriers from ionized impurities so that they can attain a mobility that is not affected by scattering phenomena due to crystal structure defects, lattice vibrations excited thermally, and impurities in the crystal [11]. To grow a device wafer,

several different layers are grown on a semi-insulating substrate: first, an undoped GaN layer, then an undoped AlGaN spacer, and finally an n-type GaN layer below the drain and source contacts.

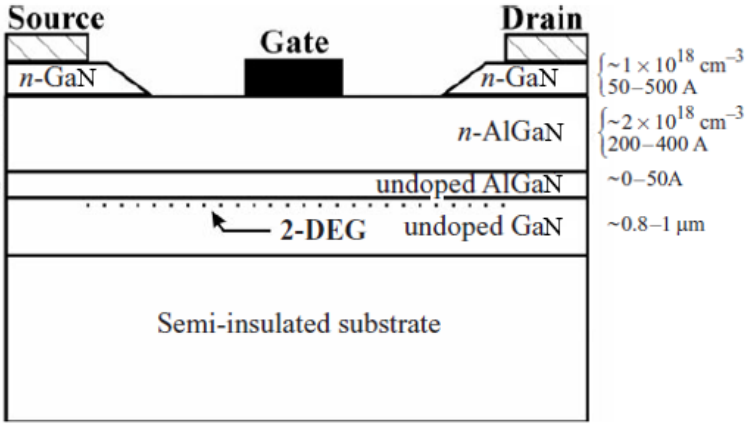

Fig. 2.2 Layer structure of a conventional HEMT.

With this multilayered structure, electrons are naturally transferred from the upper doped n-AlGaN (higher bandgap) to the lower undoped GaN layer (lower bandgap), thus forming a two-dimensional electron gas (2-DEG) layer with a high sheet carrier concentration at the heterostructure interface. Since the conduction band edge of GaN lies below the donor states in AlGaN, free electrons diffuse out of the donor states of AlGaN into the donor states of GaN. The band diagrams of the two semiconductors, with their Fermi energies $\mathcal{E}_{f1}$ and $\mathcal{E}_{f2}$, work functions ϕ_1 and ϕ_2, electron affinities X_1 and X_2, and bandgap energies E_{g1} and E_{g2}, are shown in Fig. 2.3, before and after the junction is made. The work function is the energy needed to excite an electron from the Fermi level into vacuum, while the electron affinity is the energy required to excite an electron from the bottom of the conduction band into vacuum.

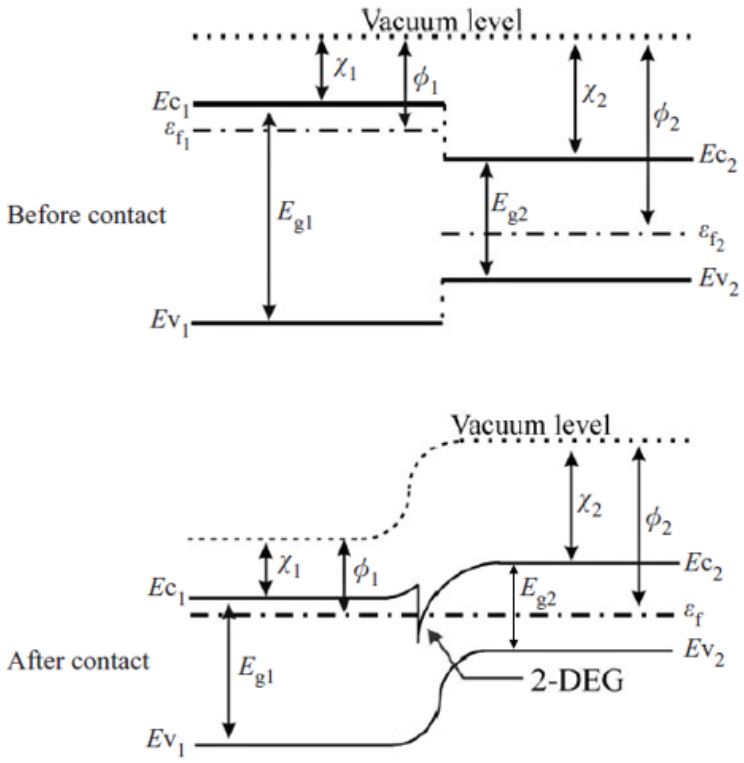

Fig. 2.3 Electron energy band diagram before and after contact formation.

The resulting electron potential energy profile suggests how charge contributed by the dopant atoms transfers into the GaN layer just to the right of the heterojunction. The transferred electrons are confined to the GaN layer due to the energy barrier at the heterointerface. In the design of a FET this 2-DEG layer is used as the channel region. The sheet carrier concentration (n_s) is controlled by the application of a potential at the metal Schottky barrier gate placed on the n-AlGaN layer. Increasing the negative bias applied to the gate decreases the depth (in electron energy) of the potential well at the AlGaN/GaN boundary. Note that in the MESFET, bias on the gate terminal controls the depth of the undepleted channel, while in the HEMT, gate bias controls the carrier density. However, both of these effects result in control of the maximum channel current [12].

The flow of channel current occurs via the drain and source ohmic contacts placed on either side of, and parallel to, the gate metallization. For low values of drain-to-source bias, a current flows from the drain to the source through the electron gas. In this case, the average velocity of carriers is linearly proportional to the field strength. This is demonstrated in Equation (2.2), where E is the electric field strength and μ_n is the low field electron mobility. This mobility is usually a strong function of doping density. For high electric field values, when the drain to source bias level is increased, the steady-state carrier velocity becomes limited and the current levels saturate. The saturation current is determined primarily by the sheet carrier density of the 2-DEG that forms in the structure.

$$v = \mu_n E \tag{2.2}$$

For this reason, an undoped AlGaN layer between the n-type AlGaN and undoped GaN is added [13]. This layer is referred to as a spacer layer and serves to separate the electrons flowing in the 2-DEG from the dopant ions in the wide-bandgap material. Without such a layer, electrons in the 2-DEG may collide with an ionized doping impurity. These collisions are termed scattering events and have the effect of temporarily randomizing the direction of movements for the particles. Then again, the electric field begins to accelerate the particles until the next scattering event occurs. This scattering reduces electron mobility and, therefore, diminishes the effect exploited in the device. Fig. 2.4 presents the classical I-V characteristics of a 4×75 μm HEMT.

So far only the conventional AlGaN/GaN HEMT has been considered. However, to obtain better noise and power performances, pseudomorphic HEMTs are now often used. One way of improving the performance of the HEMT is to use InGaN as the two-dimensional electron gas channel material instead of GaN. The benefits of using a thin InGaN layer as the

pseudomorphic channel in a HEMT include the enhanced electron transport in InGaN compared with GaN, improved confinement of carriers in the quantum well channel, and the layer conduction band discontinuity at the AlGaN/InGaN heterointerface which allows even higher sheet charge density and, hence, higher current density and transconductance than is possible with an AlGaN/GaN conventional HEMT. As seen in Fig. 2.5, the GaN-based pseudomorphic HEMT differs from the conventional AlGaN/GaN HEMT in that a thin layer of InGaN is inserted between the doped AlGaN barrier layer and the GaN buffer. There is a lattice constant mismatch between the InGaN channel layer and the AlGaN donor and GaN buffer layers, but the strain from this lattice mismatch is taken up entirely in the thin InGaN quantum well.

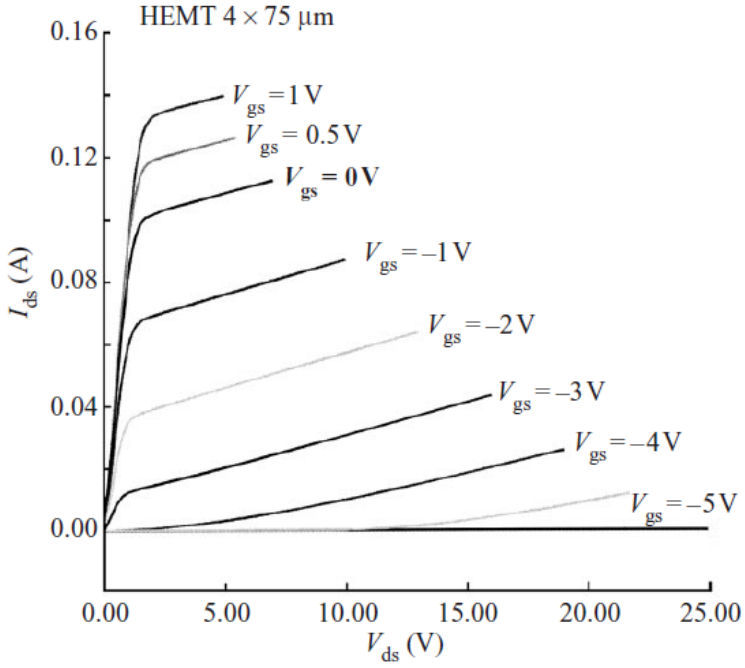

Fig. 2.4 I-V characteristics for the conventional HEMT.

2.2.3 Schottky and ohmic contacts

Connections between the bulk semiconductor and other electrical components or equipment are established via a number of different types of semiconductor contacts. The

properties of these contacts are as critical to overall device performance as the properties of the semiconductor.

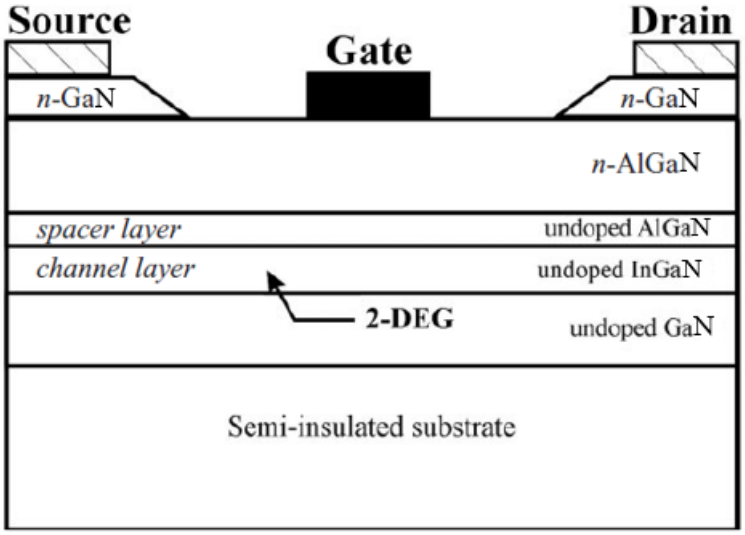

Fig. 2.5 Layer structure of a pseudomorphic HEMT.

Schottky gate contact: These junctions are special cases of the more general class of metal-semiconductor contacts. The current-voltage characteristics of these junctions are very similar to that of a p-n junction, although there are important differences in the mechanism of current flow and carrier type participation. Both electrons and holes contribute to the current in p-n junctions, whereas Schottky diodes are unipolar devices. Fig. 2.6 shows the equilibrium band diagram of a metal of work function ϕ_m and an n-type semiconductor of work function ϕ_s. The electron affinity of the semiconductor, measured in energy from the edge of the conduction band to the vacuum level, is X_s [14]. It is assumed that the Fermi level in the metal is lower than that of the semiconductor.

When a contact is made between the metal and the semiconductor, electrons are transferred from the semiconductor to the metal until the Fermi levels are aligned. The current in the metal-semiconductor contact under bias is determined by the flow of electrons from

semiconductor to metal and vice-versa. When the metal is biased positively with respect to the semiconductor, the barrier from the semiconductor to the metal is lowered and the electron flow from semiconductor to metal is enhanced. Under reverse bias the barrier increases and the probability of an electron moving into the metal decreases. Finally, applying an appropriate bias voltage can effectively control the 2-DEG sheet charge concentration. Moreover, for an appropriately selected n-AlGaN thickness, the maximum 2-DEG sheet carrier concentration (n_{so}) can be realized with the application of a gate bias voltage. It would maintain the borderline between the state of a complete depletion and the onset of the carrier conduction in the n-AlGaN layer under the gate electrodes.

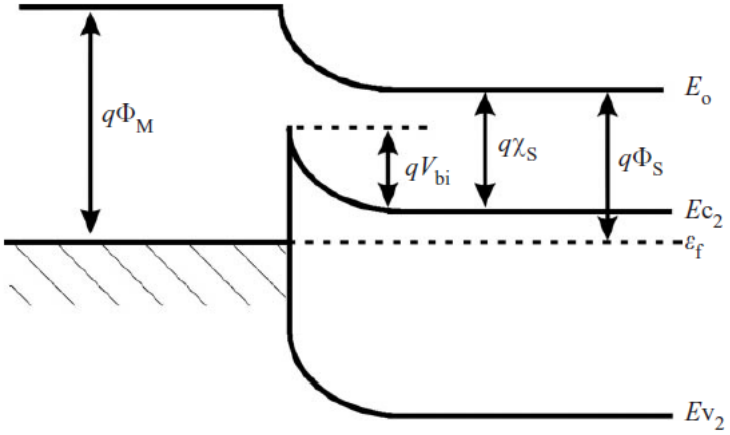

Fig. 2.6 Electron energy band diagram for a Schottky contact.

Ohmic drain and source contacts: The electron energy band diagram for a metal-semiconductor junction with $\phi_s > \phi_m$ is shown in Fig. 2.7. The electrical characteristics of an ideal ohmic contact are purely resistive in nature. This means that the current through the contact is linearly proportional to the voltage drop across it. Good ohmic contacts to semiconductor devices are essential for the realization of near-ideal device performances. The common technique to form reliable ohmic contacts is to heavily dope the region under the metal contact. It

serves the purpose of preventing oxidation of the AlGaN layer and of reducing the parasitic source resistance by providing a conduction path parallel to the 2-DEG.

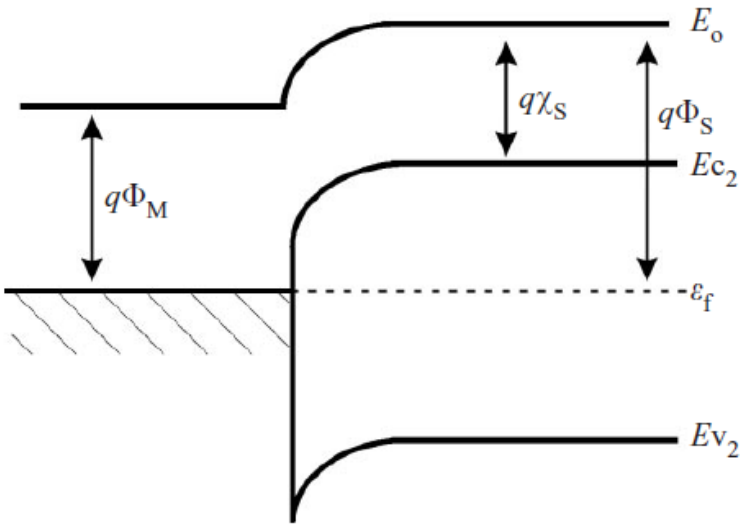

Fig. 2.7 Electron energy band diagram for an ohmic contact.

2.2.4 Fabrication of heterojunction FETs

These high-speed device structures are most commonly prepared by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) because of the high degree of compositional and dimensional control coupled with the precise placement of donors. The HEMT material quality is affected mainly by impurities, defects, heterointerface roughness, and compositional mismatch strain. High material quality and optimal layer design are the keys to achieve good device performance. For a successful monolithic integration of digital or microwave HEMTs, surface morphology, layer thickness, and doping uniformity should also be well controlled.

The growth by MBE is accomplished under non-equilibrium conditions and is principally governed by surface processes. MBE is a controlled thermal evaporation process under ultrahigh vacuum conditions. It is achieved by the evaporation or sublimation of heated sources, such as

aluminum, gallium, and arsenic, thereby forming molecular beams that impinge on a heated substrate such as GaN. The layer composition and doping level are controlled by the molecular beam fluxes and hence the temperature of the cells. The MOCVD growth technique has emerged as being technologically important for the production of single layers, heterojunctions, and quantum well structures with excellent control over layer thickness and doping and the achievement of hyper-abrupt isotype and anisotype junctions. The main advantages of MOCVD are high throughput and multilayer growth. Other than the MBE and MOCVD technologies, another technology for HEMT growth is metal-organic molecular beam. This new growth technique combines the advantages of MOCVD and MBE.

2.3 New design of AlGaN/GaN HEMT

There are two different polarizations for a GaN crystal. Fig. 2.8 shows the atomic structure for N and Ga polarizations [15]. In N-polar heterostructures the electric field induced through the polarization is in the opposite direction of this field in Ga-polar configuration. This results in formation of a 2-DEG in the N-polar structure which is above the wide bandgap AlGaN shown in Fig. 2.9 [16]. In GaN HEMT structure with N polarity, the first layer of GaN will be deposited on the substrate to account for the buffer layer. The next AlGaN or AlN layer is the barrier layer and the other GaN layer comes on top as the channel layer. The reduction in effective gate-channel length is a result of fabricating the N-polar GaN HEMTs which leads to scaling shorter gate lengths. Additionally, as the channel layer has a narrower bandgap and low barrier to electrons, the contact to 2-DEG is made through here and a low contact resistance can be obtained [16]. Furthermore, the presence of AlGaN barrier reduces the short channel effects in N-polar devices.

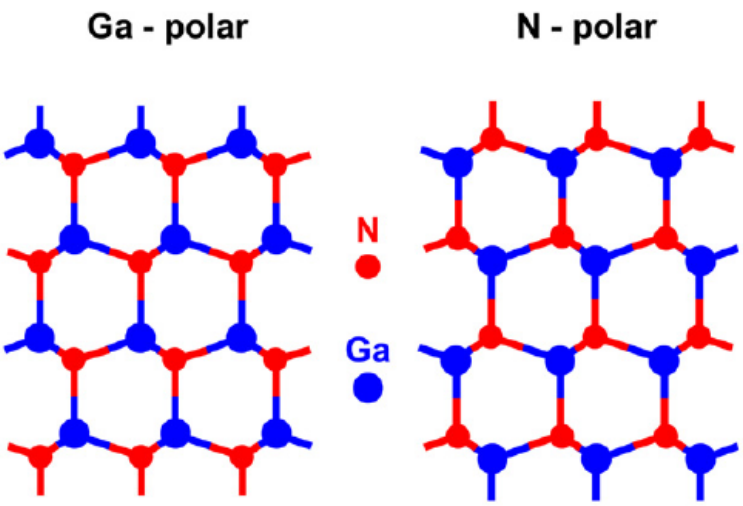

Fig. 2.8 Atomic structure for Ga-polar and N-polar GaN [15].

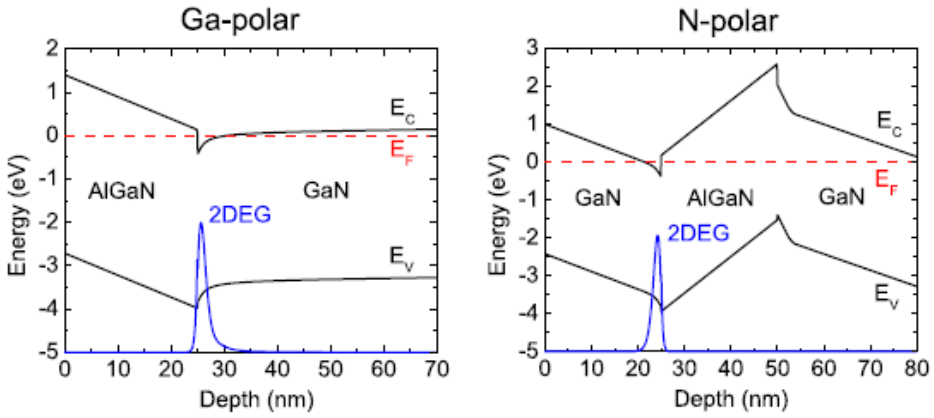

Fig. 2.9 Energy band diagram of Ga-polar and N-polar heterostructures [16].

A new GaN HEMT design is presented in Fig. 2.10 [17]. The current is maximized by high mobility along with large electron densities. A layer of $Al_xGa_{1-x}N$ is combined with a cap and a gate dielectric so as to minimize gate leakage and have a high breakdown voltage. The substrate used here is SiC with a good heat conductivity and mechanical strength. The intrinsic device performance is sometimes degraded in higher frequencies. This is mainly due to parasitic resistances formed at very thin gate lengths. Therefore, the gate in this configuration is made in a

mushroom or T shape configuration in order to increase the cross-sectional area that carries the current which results in the reduction in resistance. A higher power added efficiency and output power densities are obtained using this device compared to the conventional HEMT structures [17].

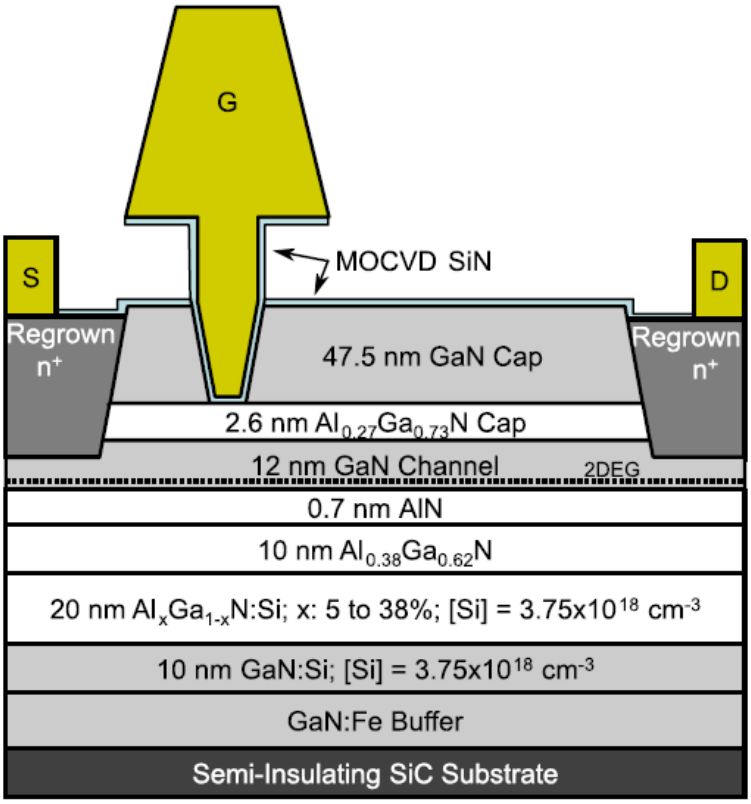

Fig. 2.10 The cross-section of a new N-polar HEMT design [17].

2.4 HEMT modeling

A great number of different semiconductor device models exist. The most usually employed is certainly the equivalent circuit model, which is based on the electrical performance of the device at its external terminals. There are two main advantages of equivalent circuit models. First, they are easy to implement in circuit design and analysis procedures. Most computer-aided design (CAD) tools used today can only accept circuit models because most

models were initially developed to model the circuit's electrical properties at low alternating current or radio frequencies. The second, and the most important, advantage of equivalent circuit models is the computational efficiency. This is a very important factor, particularly for circuit optimization, where several simulation iterations are required for the analysis of large-scale integrated circuits. Some numerical methods have shown a good compatibility with most of these circuit models [18]. This topic has been thoroughly discussed and different approaches are evaluated throughout the chapters of this dissertation.

2.4.1 Electrical equivalent models

Two types of models have been developed: small-signal and large-signal model.

Small-signal model: HEMT models provide a link between measured S parameters and electrical processes occurring within the device. From the section view in Fig. 2.11, which shows the physical origin of the circuit, we can obtain the model topology in Fig. 2.12, where each element provides a lumped element approximation to some aspects of the device. Although other circuit topologies involving additional elements have been described in the literature, this topology developed for microstrip technology has been shown to provide an excellent match to measure S-parameters through 30 GHz [19].

Basically, this conventional small-signal equivalent circuit can be divided into two parts: the intrinsic elements, which are functions of the biasing conditions, and the extrinsic elements that are independent of the biasing conditions. The transconductance, g_m, varies directly with the gain. It is a measure of the incremental change in the output current I_{ds} for a given change in input voltage V_{gs}, at constant V_{ds} (Equation (2.3)).

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=const} \tag{2.3}$$

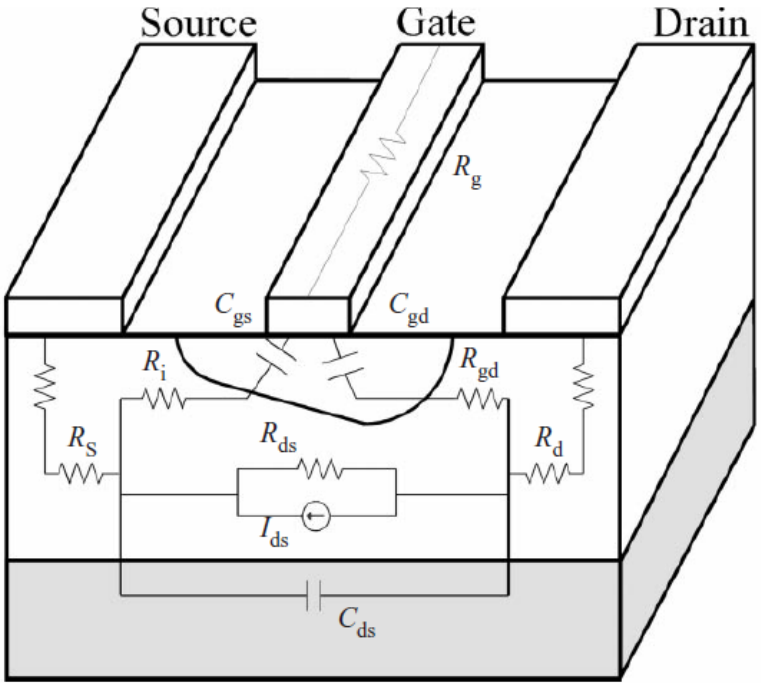

Fig. 2.11 Physical origin of the equivalent circuit model for HEMT.

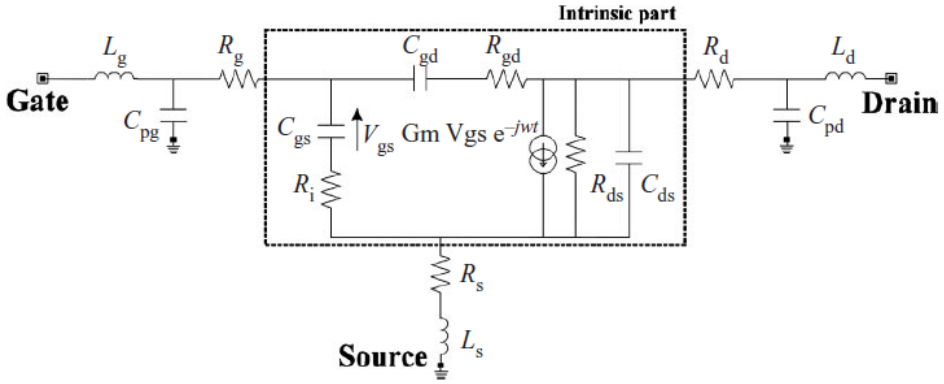

Fig. 2.12 Small-signal HEMT model.

The conductance, G_d, is a measure of the incremental change in output current I_{ds} for a given change in output voltage V_{ds}, at constant V_{gs} (Equation (2.4)).

$$G_d = \frac{1}{R_{ds}} = \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{gs}=const} \tag{2.4}$$

The capacitances C_{gs} and C_{gd} model the change in the depletion charge under the gate with respect to the gate-source and gate-drain voltages, respectively (Equations (2.5) and (2.6)).

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{ds}=const} \tag{2.5}$$

$$C_{gd} = \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{V_{gs}=const} \tag{2.6}$$

C_{ds} takes into account the electromagnetic coupling between the highly doped regions under the source and drain contacts. R_i and R_{gd} represent the channel resistances. L_g, L_d, and L_s arise primarily from metal contact pads deposited on the device surface. In microstrip technology L_s is due to via-holes. R_s and R_d account for the contact resistances of the ohmic contacts as well as any bulk resistance leading up to the active channel. The gate resistance R_g results from the metallization resistance of the gate Schottky contact. C_{pg} and C_{pd} are the pad capacitances of the HEMT and depend on the calibration measurements realized to characterize the transistor. Combined with L_g and L_d inductances, they provide a simple representation for the metal contact pads.

Large-signal model: The complete topology of the classical nonlinear model is shown in Fig. 2.13. Compared with the previous model in Fig. 2.12, several elements have been added or modified so as to take into account the bias dependency. The drain-source current, I_{ds}, is controlled by voltages V_{gs} and V_{ds} and is the main transistor nonlinearity. A mathematical function including adjustable parameters approximates some I-V measurements. A time constant τ represents the electron transit time under the gate. Two diodes I_{gs} and I_{gd} characterize the input gate current. They are also modeled by analytical expression. On the other hand, reactive nonlinearities are extracted from S-parameter measurements. R_i, R_{gd}, τ, and C_{ds} are usually independent of the gate and drain excitation voltages, while C_{gs} and C_{gd} are highly dependent on

the gate and drain excitation voltages, so it is very important to consider these elements to be nonlinear. These capacitances are mainly described by analytical model. C_{gs} and C_{gd} are controlled by voltages V_{gs} and V_{gd}, respectively.

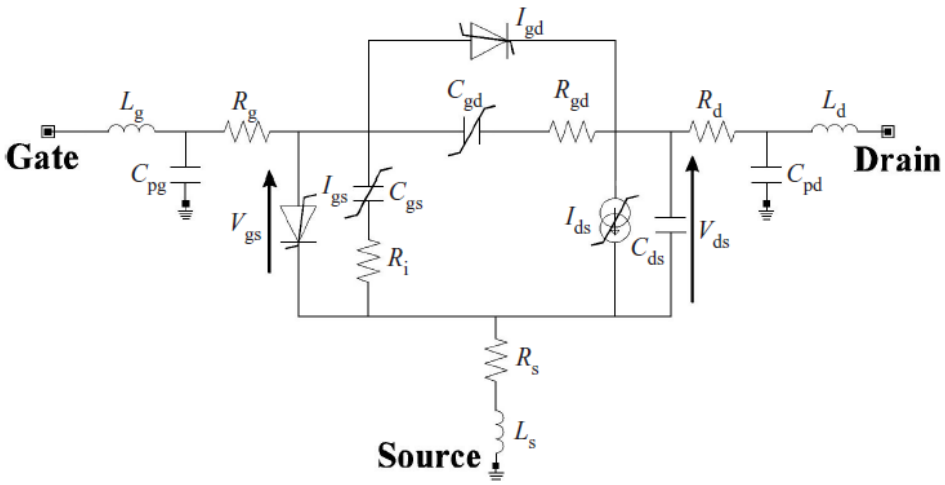

Fig. 2.13 Large signal HEMT model.

For high-frequency applications, equivalent circuit models become increasingly complex to describe accurately the operation of the device. In most cases, the circuit elements have a strong dependence on operating conditions. The bias conditions, operating frequency, temperature, and signal level influence the values of equivalent circuit elements. This limits the usefulness of these models. Another major problem associated with equivalent circuit models is the fact that it is difficult to relate circuit element values to physical and process parameters, such as device geometry, doping profile carrier types, and mobility. Consequently, it is practically impossible to use equivalent circuit models to design and develop new types of devices. In these cases, it is necessary to use physics-based models.

Limitations of the electrical equivalent model: In all equivalent circuit models, there is an underlying assumption that separates the electronic physics inside the device from the

electromagnetic wave propagation. While this assumption is acceptable at radio frequencies and the lower end of microwave range, it is no longer obvious at the high end of the microwave frequency range and the millimeter wave range for several reasons:

(I) Device dimensions become comparable with the electromagnetic wavelength and distributed effects due to wave propagation become important and must be accounted for in the model. This can be achieved only with a full-wave modeling technique.

(II) The electromagnetic wave period becomes of the same order as the charge carrier transit time and relaxation times. Consequently, the coupling between the electromagnetic wave and the charge carriers becomes important in carrier transport and the transient response of the devices.

(III) Under large-signal operation conditions, time-varying fields can be large compared to DC bias fields. The wave-particle interaction is highly nonlinear and involves multi-frequency conversion and the generation of several harmonics. Hence, accurate analysis of circuit-device interactions requires simulations over very wide frequency bands in order to detect all the relevant harmonics content that affects the circuit performance. This reinforces the need for full-wave electromagnetic device models.

2.4.2 Physics-based models

In contrast to equivalent circuit models, physical models are based on the physics of carrier transport inside the device. These models can provide better insight and understanding of the device operation under different operating conditions. Physical models also provide a link

between physical and process parameters (doping profile, gate length, recessed gate depth, etc.) and electrical performance parameters (DC characteristics, RF transconductance, junction capacitances, etc.). For these reasons, physical device models should be essential tools, not only in the development of new devices, but also in performance and yield optimizations of microwave circuit design. The major limitation of such models, however, is that they are computationally intensive, preventing their direct use in circuit design. In most cases, it is inevitable to introduce simplifying assumptions in order to make the model computationally tractable.

The most commonly used physics-based models can be classified into two categories: particle-based models and fluid-based or hydrodynamic models. The first category is represented by the Monte-Carlo technique. The second is based on a set of conservation or continuity equations that can be derived from the Boltzmann transport equation (BTE). These models usually involve several approximations that vary from the simplest to the more complex: analytical models, drift-diffusion models, energy models, and full-hydrodynamic models. Up until the 1970s semiconductor devices were well modeled with the drift-diffusion transport approach. This approach includes a drift velocity controlled by the electric field and carrier diffusion density gradients. In a spatially homogeneous system, it reduces to Ohm's law for low electric fields. It assumes that the microscopic distribution of momentum and energy over the charge carriers at any location and time inside the device is equal to which one would find in a large sample with a DC field equal to the local instantaneous field.

The assumptions in the drift-diffusion model, however, break down for submicron devices, where carrier transport is predominantly nonstationary. For small-signal devices with gate lengths of less than 0.5 μm nonstationary transport effects, such as hot electron effects and

velocity over-shoot, become very important and must be accounted for in the device model. Semi-classical device models have been developed to include energy and momentum relaxation effects while at the same time providing computationally efficient models. These models deal with charge carriers as classical particles whose motion properties, such as effective mass and scattering effects, are derived from quantum models.

Attempts to develop simpler models that can take into account the nonstationary effects such as velocity over-shoot have culminated in the formulation of the hydrodynamic model. This model consists of the set of coupled and highly nonlinear conservation equations derived from the zero, first, and second order moments of the Boltzmann transport equation. An alternative to these previous models is a full-wave electromagnetic analysis of the passive distributed metallic part of the transistor combined with a physics-based device simulation used to characterize the active contribution of the component. This approach is known as the global modeling of circuits.

2.5 HEMT applications

The main characteristics of HEMTs are:

- high electron mobility
- small source resistance
- high cutoff frequency (f_t) due to high electron velocity in large electric fields
- high transconductance due to small gate to channel separation
- high output resistance
- high Schottky barrier height due to deposition of Schottky metal on AlGaN instead of on GaN

By using these characteristics engineers have developed a great number of microwave circuit applications. A list of applications where heterojunction FETs have enabled some improvements is discussed below:

- Low-noise and small-signal amplifiers (LNA) are circuits designed to operate as linear gain blocks, with specific requirements determined by their location within the system. They are typically operated at input power levels well below power saturation and may keep the overall system noise figure small [20].
- Power amplifiers are typically used in communication systems to provide sufficient signal power to allow transmission from one site to another. They are usually designed for maximum efficiency rather than linearity or low noise.
- Oscillators are used to perform frequency conversion of a desired signal. To obtain extremely low noise HEMT oscillators, the dielectric resonator is integrated for stabilization [21].
- Mixers are three-port devices that function to convert an input RF signal in conjunction with LO signal to an intermediate signal IF. The IF signal may be either the sum or the difference between LO and RF signals. Ideally, a mixer performs this frequency conversion with perfect fidelity, without intermodulation distortion, with high isolation between all three ports and a low noise figure.
- HEMTs can also be used in a variable attenuator, which is defined as a two-port device that allows adjustment of the signal amplitude by application of an external voltage or current.

2.6 Conclusion

The analysis of device performance and structural characteristics of high electron mobility transistors have been discussed in this chapter. Based on the available literature, GaN seems to be the reliable choice to be used as the active section in HEMT devices offering a high output power density, high operational frequency, and satisfactory power added efficiency. The typical thicknesses and doping densities for different layers are provided and the formation of contacts are explained. Layer growth methods are briefly discussed and a new HEMT device along with the structural modifications is described. Furthermore, a small-signal model is depicted to account for the equivalent circuit in a frequency range lower than 30 GHz. The limitations for the small-signal model are also explained and a description of physical-based models are presented. Last but not the least, some general HEMT applications are discussed both for high and low operating frequencies. Performance characteristics reported in this article for microwave and millimeter-wave heterojunction FETs continue to improve. Minimum noise figures are reduced, while the frequencies of operation and maximum output powers are increased. These factors ensure that interest in HEMT will continue for a long time.

2.9 References

[1] F. Ali, A. Gupta, *HEMTs & HBTs: Devices, Fabrication and Circuits*, Artech House, 1991.

[2] M. Shur, *GaAs Devices and Circuits*, Plenum, New York, 1987.

[3] M. Golio, *RF and Microwave Semiconductor Handbook*, Ed. Boca Raton, FL: CRC, 2003.

[4] U. K. Mishra, P. Parikh, and Yi-Feng Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022-1031, Jun 2002.

[5] T. Palacios *et al.*, "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 781-783, Nov. 2005.

[6] Y. F. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, and A. Burk, "High-voltage millimeter-wave GaN HEMTs with 13.7 W/mm power density," *IEEE IEDM Tech. Dig.* 405-407, 2007.

[7] Y. F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm Double Field-plated GaN HEMTs," *Proc. 64th Device Res. Conf.*, pp. 151–152, 2006.

[8] S. Wienecke *et al.*, "N-Polar GaN Cap MISHEMT with Record Power Density Exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 359-362, March 2017.

[9] B. Romanczyk *et al.*, "mm-Wave N-polar GaN MISHEMT with a self-aligned recessed gate exhibiting record 4.2 W/mm at 94 GHz on Sapphire," *2016 74th Annual Device Research Conference (DRC)*, Newark, DE, 2016, pp. 1-2.

[10] S. M. Hammadi, S. M. El-Ghazaly, "Air-bridge gate MESFET: a new structure to reduce wave propagation effects in high frequency transistors," *IEEE Trans. Microwave Theory Techniques*, 890-9.

[11] J. M. Golio, *Microwave MESFETs & HEMTs*, Artech House, 1991.

[12] R. Anholt, *Electrical and Thermal Characterization of MESFETs, HEMTs and HBTs*, Artech House, 1994.

[13] P. H. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs*, Artech House, 1989.

[14] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, 1981.

[15] S. Keller *et al.* "Recent Progress in Metal-Organic Chemical Vapor Deposition of (000$\bar{1}$) N-Polar Group-III Nitrides," *Semiconductor Science and Technology*, 1 Nov. 2014.

[16] M. H. Wong *et al.*, "N-polar GaN epitaxy and high electron mobility transistors," *Semiconductor Science and Technology*, vol. 28, no. 7, 2013.

[17] B. Romanczyk *et al.*, "Demonstration of Constant 8 W/mm Power Density at 10, 30, and 94 GHz in State-of-the-Art Millimeter-Wave N-Polar GaN MISHEMTs," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 45-50, Jan. 2018.

[18] A. Ghadimi, S. Asadi, "Modelling of composite right/left-handed active multiconductor transmission lines (AMCTL) in time domain," *Int J Numer Model.*, 2018.

[19] G. Dambrine *et al.*, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Techniques*, 1151-9, 1988.

[20] S. Wang, *Fundamentals of Semiconductor Theory and Device Physics*, Prentice Hall, Englewood Cliffs, NJ, 1989.

[21] S. Jang, Y. Chang, J. Chiou and W. Lai, “A single GaN HEMT oscillator with four-path inductors,” *2018 7th International Symposium on Next Generation Electronics (ISNE)*, 2018, pp. 1-2.

Chapter 3

Apparatus and method to reduce the thermal resistance of semiconductor substrates

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3.1 Introduction

Any type of circuit component that has the ability to electrically control the electron flow is called a switch. The switch may depend on an active device in its operation [1]. Some of these active devices allow a voltage to control the current flow through them while some devices do the job by another controlling current signal. In these types of switches, electricity is controlling the electricity. These two categories of switches are commonly referred to as voltage-controlled devices and current-controlled devices, respectively. Vacuum tubes, transistors, diodes, and silicon-controlled rectifiers are some of the examples of active devices [2-3]. Initially, transistors were made as current-controlled devices, but voltage-controlled transistors were also developed thereafter.

Different terms are used for these transistors, such as bipolar junction transistor (BJT) [4], field-effect transistor (FET) [5], metal-oxide-semiconductor FET (MOSFET) [6], metal-semiconductor FET (MESFET) [7], heterojunction bipolar transistor (HBT) [8], and high electron mobility transistor (HEMT). The terms mark the structural configurations and physical mechanisms associated with these devices, which demonstrate the fundamental settings for the operation. These devices are often developed for high-speed, low-noise, or high-power applications such as small-signal amplifiers [9], power amplifiers, mixers [10], and oscillators [11] operating over a wide frequency range. The other category of applications is the RF circuits and systems, where the devices are used in cellular communications and RADARs in an integrated circuit configuration.

The main solid-state materials for designing high-performance transistors and power amplifiers are Silicon (Si), Gallium Arsenide (GaAs), Silicon Germanium (SiGe), Aluminum Gallium Nitride (AlGaN), Silicon Carbide (SiC), and Gallium Nitride (GaN). These are used for the formation of channel layers, buffer layers, and substrates in most transistor devices. Devices and circuits that are based on silicon are the forerunners of all semiconductor devices. However, the recent upsurge in wireless communication applications, 5G technology, electric cars, solar cells, and power switches, demands high-frequency operations, high power handling, and high-temperature performance of the devices where silicon may not be able to fulfill the needs. This is one of the reasons for the recent focus of many research groups on some wide-bandgap semiconductors.

These devices are mainly characterized by the operating frequency, output power density, and power-added efficiency. However, for a thorough characterization of semiconductor devices, the study of device operation over different temperature ranges is also very vital, especially for high power devices such as GaN-based HEMTs, where a great amount of heat is generated which affects the underlying physics of the device [12]. It is therefore very important to determine what the maximum channel temperature is under specific operating modes. Hence, other than the materials chosen for the active layers, deciding on the best option for the semiconductor substrate is also very critical, for it serves as the layer where the generated heat in the channel layer is dissipated. For a device operating at a high-voltage level, the output current is very large which, consequently, generates a high temperature gradient. This temperature may either damage the device or prevent it from functioning properly, if the heat dissipation does not happen efficiently. Therefore, for a reliable device operating at high frequencies with a high

output power density, thermal management and heat handling are very important in the design process [13].

The present chapter provides a method, system, approach, and solution that increases the thermal conductance of a power semiconductor device that generates internal heat in the channel layer which needs to be dissipated through the substrate. This results in improving the power handling capabilities of semiconductor devices. A novel semiconductor substrate is introduced which is made of a first material including a plurality of spaced-apart depressions and an area surrounding the depressions filled with one or more materials having a heat conductivity greater than the first material.

3.2 Substrate modeling

Sapphire is a material that possesses high heat resistance, good electrical insulation, low dielectric loss, and stable dielectric constant which makes it a reliable candidate to be used as an insulating substrate in high-frequency transistors. In almost all high-power, high-frequency devices that are fabricated on a sapphire substrate, heat conductivity has been identified as an issue. This has limited the device operation at higher output power densities and some research groups have replaced it with other semi-insulating substrates. In [14], the proposed HEMT device is deposited on sapphire which operates at 94 GHz with an output power density of 2.9 W/mm. The authors have mentioned some limitations for the operation at higher powers pertaining to thermal management and replaced the substrate in another report with SiC [15], where the operating frequency is the same and the power density has improved to 6.5 W/mm. This limitation is based on the fact that thermal conductivity of sapphire is lower compared to

SiC [16]. However, compared to SiC, sapphire is much cheaper and available in different sizes and thicknesses that makes it a very cost-efficient choice.

To solve the thermal conductivity problem of sapphire substrates and provide a holistic optimization method, a fabrication technique is proposed. Fig. 3.1 shows a substrate for solid-state amplifiers in a cylinder-shaped configuration. The upper cylinder is made of sapphire and the lower part is the metallization section made of copper. Table 3.1 indicates the thermal properties of the two materials. The radius for the cylinders' cross-section is 1000 μm, the height of the sapphire cylinder 500 μm, and the height of the copper cylinder is 10 μm. A 1×100 μm rectangle is considered on top of the cross-section where a single-finger high-frequency transistor is deposited. The lower face of the cylinder has a fixed-temperature boundary condition, and is set to 293.15 K. All the other faces have a convective heat flux density boundary condition based on Equation (3.1), where T_{ext} is equal to 293.15 K and h, the heat transfer coefficient, equals 20 W/m^{2}K. All the simulations are conducted using COMSOL Multiphysics.

$$Q_0 = h \times (T_{ext} - T) \tag{3.1}$$

To test the heat dissipation capabilities of the sapphire substrate, a power of 1 W is applied to the rectangular section and the heat distribution results are depicted in Fig. 3.2. The bar at the right side of the figure indicates the temperature in Kelvin. Looking at the temperature gradient profile of this configuration, the maximum temperature of roughly 1080 K is seen at the top surface of the sapphire wafer. This high temperature is a result of low thermal conductivity of sapphire, and this substrate is not able to dissipate the generated heat. For a HEMT device operating at high frequencies, transconductance and drain current are the two vital figures of merit which are greatly affected by high temperature gradients. It should also be noted that the

thermal stability of sapphire is very high, and this temperature does not damage the structure of the wafer.

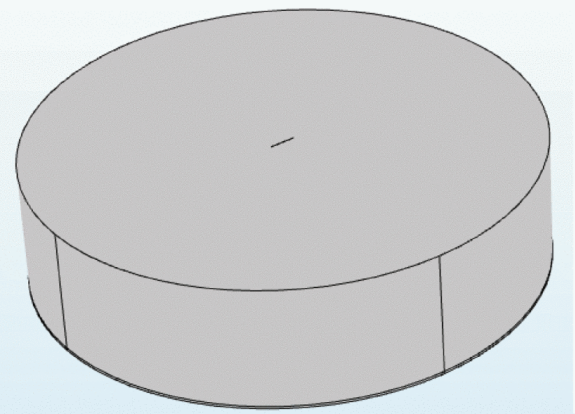

Fig. 3.1 Sapphire substrate with copper metallization.

Table 3.1 Thermal properties of sapphire and copper

Material	Thermal conductivity (W/m.K)	Density (Kg/m^3)	Heat capacity (J/Kg.K)
Sapphire	25.2	3980	761
Copper	385	8940	385

To find a solution, the same simulation is conducted on a thinner substrate. This time the sapphire wafer thickness is 100 μm and all the other dimensions stays the same as the previous case. The results of this case are shown in Fig. 3.3. The maximum temperature is now 1045 K and a subtle decrease in temperature is seen for the thinner substrate. For proving that the results obtained from simulation are correct, an approximate analytical approach is proposed. First, the thermal resistivity of the cylinder is calculated based on Equation (3.2), where σ is the thermal conductivity, l is the thickness of the wafer, and A is the area of the section where the power is applied. Using the value for the power or the dissipated heat (Q) inside the substrate, the temperature is calculated according to Equation (3.3), where ΔT is the temperature difference

between the top surface, where the temperature is maximum, and the fixed-temperature boundary condition at the bottom.

$$R = l/\sigma A \tag{3.2}$$

$$\Delta T = Q \times R \tag{3.3}$$

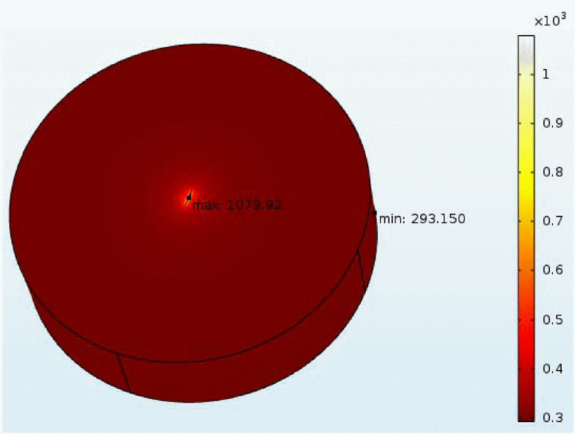

Fig. 3.2 Temperature distribution for a 500 μm sapphire substrate with copper metallization (P = 1 W).

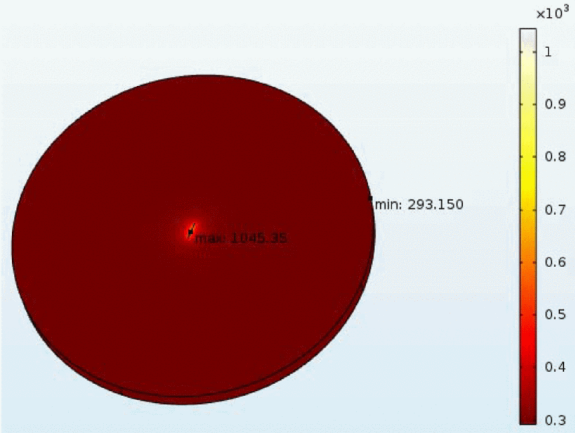

Fig. 3.3 Temperature distribution for a 100 μm sapphire substrate with copper metallization (P = 1 W).

Based on this analytical method, the maximum temperature for the sapphire with the thickness of 500 μm and 100 μm are 1165 K and 962 K, respectively. These two figures indicate a maximum temperature difference of 203 K, which may be considered quite significant

depending on specific applications. This became the initial stage for developing the holistic optimization approach and the proposed method seemed to be able to solve the issue of high temperature gradients for the case of devices on sapphire wafers and allow sapphire substrates to be utilized in higher power densities and frequencies.

Thinning down the wafer to a thickness of 100 μm or thinner is feasible and is done in two ways. The first procedure is applied subsequent to fabrication. The active device is deposited on the substrate and after that, the substrate is ground to the desired thickness starting at the backside of the wafer. The next method is prior to fabrication where a thinner substrate is used for the fabrication process. This substrate is fragile and may not bear the pressure of depositing solid-state materials. However, this issue is solved by a layer of thick metal sputtered on the backside of the wafer, such as titanium or copper, which provides a mechanical strength to the wafer.

3.3 Description of the proposed solution

The electrical current flow through the channel layer of a power semiconductor device leads to generation of a substantial amount of internal heat in an operating environment. The internally generated heat has to be removed properly. Otherwise, the temperature for the junctions of the semiconductor device would rise to values that may result in degradation of the device operation or catastrophic damage to the active region. To maintain the junction temperature below the maximum allowed values for a semiconductor device, the substrate must have the ability to dissipate the heat by facilitating and enabling the heat flow away from the device.

The heat transfer model discussed herein is the conduction heat transfer which occurs due to temperature gradients in a body. As shown in Fig. 3.4, the conductive heat energy is transferred from a hot surface (Face 100) to a cold surface (Face 102). The temperature of the object mainly depends on the separation between the two faces and its thermal conductivity. Heat transfer rate by conduction through the object can be expressed as Equation (3.4), where A is the cross-sectional area of the object, L is the distance between the two faces or the wall thickness, ΔT is the temperature difference between the two surfaces, and k is the thermal conductivity for the material in W/mK. A parameter called the thermal resistance of the material is defined which depends upon the thermal conductivity of the material, material thickness, and object area. This parameter is represented according to Equation (3.5). Obviously, the resistance can be decreased by increasing the thermal conductivity of the material.

$$P = \frac{kA}{L} \times \Delta T \tag{3.4}$$

$$R_C = \frac{L}{kA} \tag{3.5}$$

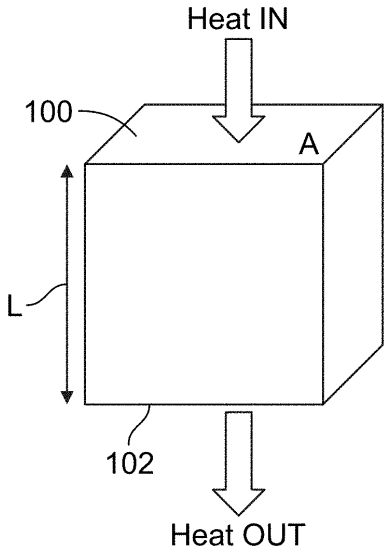

Fig. 3.4 Conductive heat flow in an object.

Silicon, sapphire, and silicon carbide are examples of semiconductor substrates that are used in fabrication of power devices. Most of these power devices have the functionality of amplification and thus a great amount of current flows through them. This current will lead to generation of high-temperature gradients and the substrate must have the capability of dissipating this heat either to the metallization on the backside or any heat sink mounted on the device. Fig. 3.5 shows an example of the path for the heat flow in a HEMT device. As shown, heat flows from channel (220) into the substrate (250), through interlayer (230) and back-barrier (240).

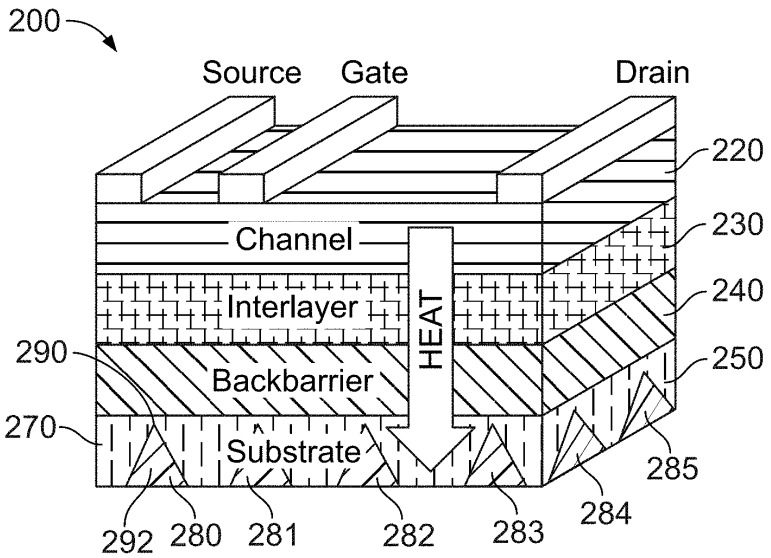

Fig. 3.5 Heat flow path in a GaN HEMT device.

3.4 Heat distribution results

To study the heat dissipation capabilities of this substrate, another simulation was conducted in COMSOL Multiphysics. Fig. 3.6 shows the substrate (300) under test. The difference between this configuration and the one shown in Fig. 3.1 is that the material for the substrate is silicon and an area of 100×100 μm is considered on top as the section where the electric power is applied, which also represents the spot where the multi-finger active device is

placed. The lower face (310) is coated with a very thin layer of copper and the same boundary conditions are considered. One watt of power is applied to section (350) on top and the temperature distribution results are obtained. Fig. 3.7 shows the heat distribution inside the substrate. The maximum temperature at point (350) where the power is applied, and the device is mounted on is roughly 330 K. It is understood that applying a power of 1 W is not the practical case and this is assumed only for the sake of this simulation. However, as many substrates are incapable of dissipating the required heat in many devices, this has been a limitation for many research groups dealing with high power circuits.

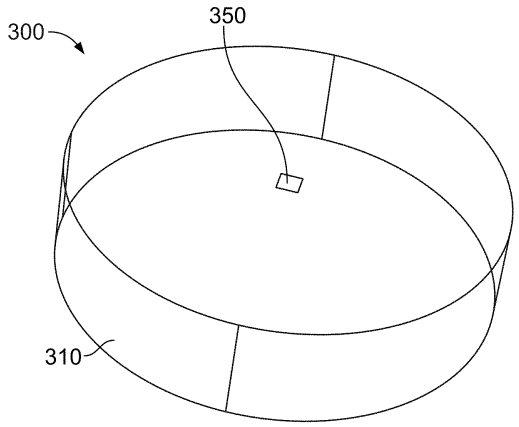

Fig. 3.6 Silicon substrate simulated in COMSOL.

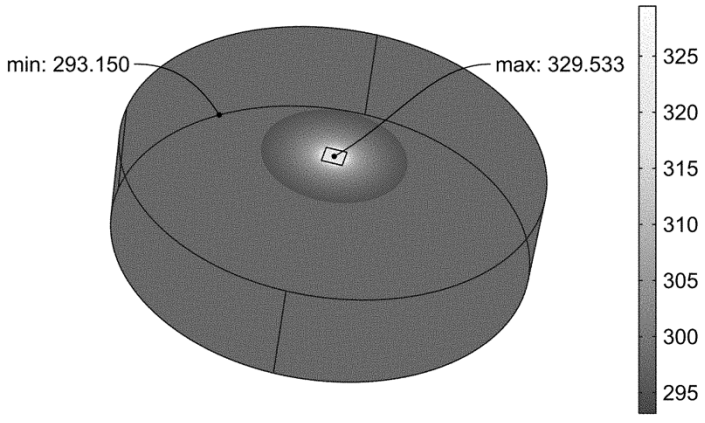

Fig. 3.7 Heat distribution in silicon substrate.

As discussed earlier, increasing the heat conduction coefficient of an object will result in a reduction in thermal resistance of the material. For this purpose, a selective etching process on the substrate from the backside is performed. The etching process of microfabrication is defined as chemically removing layers from the surface of a wafer during manufacturing [17]. Part of the wafer is protected from the etchant by a masking material which resists etching. According to the material being used as the substrate, different etching techniques might be used. In wet etching, the wafer is immersed in a bath of etchant [18], while in plasma etching, energetic free radicals are produced that react at the surface of the wafer [19].

There are two figures of merit for the etching process. Selectivity that deals with the ability of the etchant to remove the top layer of a multilayer structure without damaging the masking or underlying layers and isotropy that defines the direction for the etching process. As shown in Fig. 3.5, a semiconductor device (200) comprising a substrate (250) made of a first material (270) is provided. Substrate (250) includes a heat sink comprised of a plurality of spaced-apart truncated cones (280-285). Truncated cones (280-285) are filled with one or more second materials having a heat conductivity greater than first material (270). The second material may be comprised of a single material such as copper.

Fig. 3.8 shows that the substrate (500) is etched to form a truncated cone shape (510), but other shapes such as cylinders, circles, and squares may also be used to form depressions consisting of etched away material which is filled with highly conductive materials. A truncated cone is preferred because it does not require a high figure of merit for the etching process and removing a shape with a slope like a truncated cone is pretty straightforward. Substrate (500) may be made of Silicon, Gallium Arsenide, Silicon Germanium, Aluminum Gallium Nitride, Silicon Carbide, Gallium Nitride or a combination of these materials.

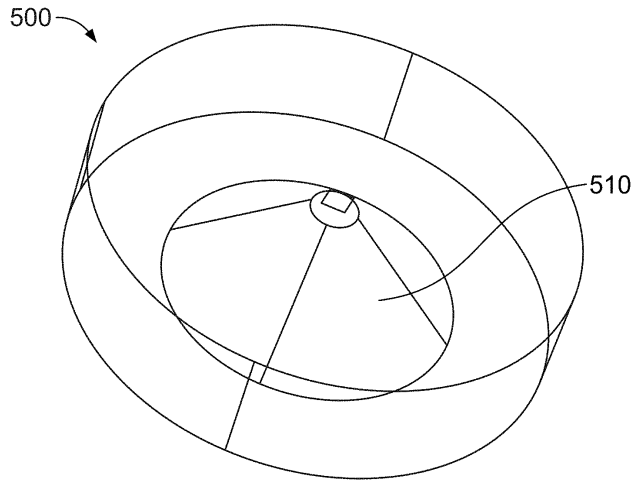

Fig. 3.8 Truncated cone shape etched into the silicon substrate.

A consideration behind choosing a truncated cone shape as the etched section is dictated by the present etching technology and its methodologies. A cylinder shape as the etched section may be used but there are a couple of drawbacks associated with this configuration: 1) In order to have an etched section in the shape of a cylinder, a hole needs to be drilled in the back of the substrate and today's technology is not capable of drilling on robust substrates such as sapphire. Therefore, in this case, the proposed method will lose its generality for all the substrate materials. 2) Even assuming that drilling a hole on the back of the substrate is practicable, the process of filling the etched section with a satisfactory conductor, which is normally done through sputtering, will not be feasible.

Additionally, robustness is one of the characteristics of the general substrates and platforms used in high-frequency devices and this feature is very prominent for sapphire material. However, when considering the case of etching a 500-micron substrate up to 490 microns, the section with a thickness of 10 microns will not have enough mechanical strength

and may easily break during the etching process. In this case, having a truncated cone shape will provide sufficient mechanical support on the sides which prevents this breakage.

Moreover, etching a truncated cone is based on the etching process itself. If it is assumed that a chemical etching is applied on the back of the substrate (which is applicable for all materials), even if the process starts on a section with a fairly small diameter, it will eventually end up in a larger diameter. The reason is that in the process of chemical etching the chemical material not only etches deep inside the substrate but also will have some effects on the sides and this is similar to a case when a stone is dropped in water and the ripples are created. Consequently, at every level of etching, a small section from the sides of the target area will also be affected by this process. The deeper one etches inside the substrate, the larger the effect of this phenomenon will be to the sides. Eventually, the shape of the etched volume will look like a truncated cone.

The next stage is to fill the etched section with a combination of conducting materials (i.e., multiple layers of different materials) which possesses a high heat conductivity. This is done by either electroplating [20] or another process known as sputtering [21]. In the latter process, a gaseous plasma is created and then the ions from this plasma are accelerated into the target material. The idea of choosing the etched section similar to a truncated cone shape will have additional advantages during the sputtering stage. For simplicity, copper is used as an example. Filling the backside of the substrate with copper will also produce additional mechanical strength and increase the robustness of the wafer. The same simulation is then conducted with the new configuration and the power of 1 W is applied to the section on top.

As shown in Fig. 3.9, the maximum temperature on top of the shape has been reduced to 324 K. A 20% reduction in the temperature difference between the ambient temperature and the

maximum temperature is obtained with the new configuration. The results of the simulation for different applied power values are shown in Table 3.2. A consistent reduction in temperature difference is observed in all cases.

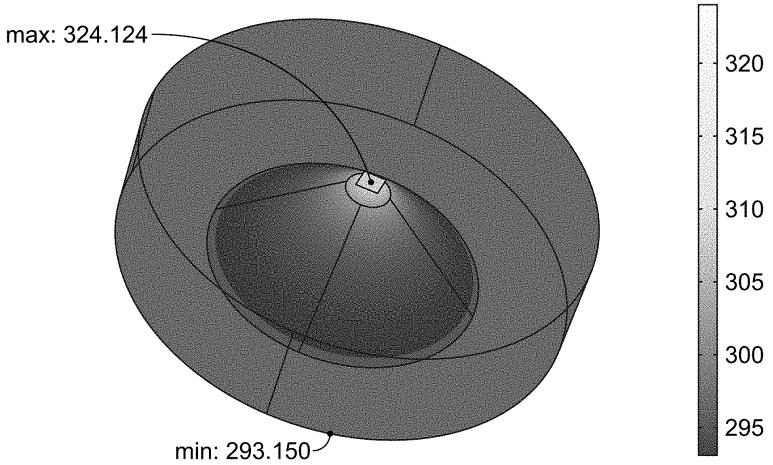

Fig. 3.9 Heat flow in a 500 μm silicon substrate etched on the backside (applied power=1 W).

Table 3.2 Results for different applied power values for silicon substrate (T = 0.5 mm).

Silicon substrate	Tmax without etching	Tmax with etching	Reduction in temperature difference
Power = 1 W	330	324	20%
Power = 2 W	366	355	18%
Power = 3 W	402	386	18%
Power = 4 W	439	417	18%
Power = 5 W	475	448	18%

The simulations were continued with different dimensions for the truncated cone, and it was concluded that the height of the cone is very vital in determining the maximum obtained temperature. Table 3.3 shows the simulation results for taller cone shapes etched into the silicon substrate. The other dimensions are the same as the previous case and the applied power is 5 W.

This reduction of the maximum temperature will eliminate the limitations in a large number of power devices, where the generated heat cannot be more than a certain value. The same process can be done on different substrates with different thermal conductivities and the temperature reduction in these substrates is prominent as well. Based on the application, substrate material, substrate thickness, and wafer dimensions may be adjusted.

Table 3.3 Results for different cone heights for silicon substrate (applied power = 5 W and T = 0.5 mm).

Silicon substrate	Tmax with etching	Reduction in temperature difference
Cone height = 460 μm	441	23%
Cone height = 470 μm	430	33%
Cone height = 480 μm	416	48%
Cone height = 490 μm	395	78%

The same simulation for two different substrate materials was conducted as well. Sapphire is utilized in a special technology called Integrated Microwave Photonics (IMWP) which incorporates microwave and photonics functions on a single chip. SiC is also a reliable substrate for many RF amplifiers working in a frequency range of 30-100 GHz. Due to the fact that the thermal conductivity of SiC is much higher than sapphire, this substrate material is mostly used in high power, high-frequency operations. Table 3.4 shows the same simulation conducted with these substrate materials. The applied power for all cases is 5 W and the truncated cone for the case of etched substrates has a height of 490 μm. The high value for the temperature reduction shows that the procedure provides consistent results for these cases as well.

Table 3.4 Results for different substrate materials for a cone height of 490 μm (P = 5 W and T = 0.5 mm).

Material	Tmax without etching	Tmax with etching	Reduction in temperature difference
Sapphire	1362	569	288%
SiC	518	405	101%

3.5 Conclusion

The holistic optimization technique evaluates the behavior of the devices based on different parameters. After deciding on the type of the device and material to be used based on the applications with high frequency operations and high output densities, the first issue addressed was the low thermal conductivity of the commonly used sapphire substrate. A model for the substrate was simulated in COMSOL Multiphysics. The results obtained from simulation was then proved with the calculation results. It was demonstrated that thinning the substrate can be a potential technique for solving the heat dissipation problem for sapphire. The research continued on developing more accurate analytical techniques for modeling the thermal behavior of substrates in high power conditions and a novel method was then proposed to fully cover the cases with different substrate materials and dimensions.

Other than the high-power and high-frequency transistors, solar cells will also greatly benefit from the proposed approach. Reducing the manufacturing costs and increasing power conversion efficiency are the two main goals in improving solar cells. The most commonly used material for fabricating solar cells is crystalline silicon, which is capable of yielding roughly 30% conversion efficiency in solar panels. The remaining energy is typically converted to internal heat and as the solar cell sizes are decreasing, this heat is considered as a bottleneck in

conversion efficiency. The proposed design approach provides designs and structures that dissipate the internally generated heat, which prevents cell degradation and increases the efficiency of the panels. The technology may also extend to a complete elimination or at least a reduction in the need for complicated cooling systems, such as water cooling, when fabricating panels for solar cells.

3.6 References

[1] P. Sojka, M. Pipiska, and M. Frivaldsky, "GaN power transistor switching performance in hard-switching and soft-switching modes," *2019 20th International Scientific Conference on Electric Power Engineering (EPE)*, 2019, pp. 1-5.

[2] V. D. Bochkov and M. M. Pogorelsky, "Investigation of charge distribution on the dielectric envelope of high-voltage vacuum tube," *Proceedings of 17th International Symposium on Discharges and Electrical Insulation in Vacuum*, 1996, pp. 415-419 vol.1.

[3] W. Liu, J. J. Liou, H. Yeh, H. Wang, Y. Li and K. S. Yeo, "Bidirectional Diode-Triggered Silicon-Controlled Rectifiers for Low-Voltage ESD Protection," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1360-1362, Oct. 2012.

[4] F. Zhao, I. Perez, Chih-Fang Huang, J. Torvik, and B. Van Zeghbroeck, "Analysis of transit times and minority carrier mobility in n-p-n 4H-SiC bipolar junction transistors," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2541-2545, Dec. 2005.

[5] W. Shockley, "A Unipolar "Field-Effect" Transistor," in *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365-1376, Nov. 1952.

[6] R. H. Dennard, F. H. Gaensslen, H. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256-268, Oct. 1974.

[7] H. Fukui, "Design of Microwave GaAs MESFET's for Broad-Band Low-Noise Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, no. 7, pp. 643-650, Jul. 1979.

[8] J. D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 572-589, May 1998.

[9] M. Motoyoshi, K. Takano, K. Katayama, and M. Fujishima, "135GHz CMOS small-signal amplifier with power-efficient bias method," *2013 Asia-Pacific Microwave Conference Proceedings (APMC)*, 2013, pp. 348-350.

[10] A. N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1939-1944, Dec. 1996.

[11] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717-724, May 1999.

[12] S. Cheng, C. Li, C. Liu, and P. Chou, "Characterization and thermal analysis of packaged AlGaN/GaN power HEMT," *2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2011, pp. 195-197.

[13] A. Syed, M. J. Islam, S. M. Hasanuzzaman, A. K. Podder, M. S. Islam, and A. G. Bhuiyan, "Theoretical analysis of substrate effects on the DC performance of AlGaN/GaN high electron mobility transistor," *2016 5th International Conference on Informatics Electronics and Vision (ICIEV)*, pp. 961-966, 2016.

[14] S. Wienecke *et al.*, "N-Polar Deep Recess MISHEMTs with Record 2. 9 W/mm at 94 GHz", *IEEE Electron Device Letters*, vol. 37, no. 6, pp. 713-716, June 2016.

[15] S. Wienecke *et al.*, "N-Polar GaN Cap MISHEMT with Record Power Density Exceeding 6. 5 W/mm at 94 GHz", *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 359-362, March 2017.

[16] J. C. Freeman, "Channel temperature model for microwave AlGaN/GaN power HEMTs on SiC and sapphire," *2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535)*, 2004, pp. 2031-2034 Vol.3.

[17] Seok-In Na *et al.*, "Selective wet etching of p-GaN for efficient GaN-based light-emitting diodes," *IEEE Photonics Technology Letters*, vol. 18, no. 14, pp. 1512-1514, July 2006.

[18] Y. B. Wu, G. F. Ding, H. Wang, and C. C. Zhang, "Efficient solution to selective wet etching of ultra-thick copper sacrificial layer with high selective etching ratio," *2011 16th International Solid-State Sensors, Actuators and Microsystems Conference*, 2011, pp. 1388-1391.

[19] D. Zhang and M. J. Kushner, "Surface and gas phase reactions for fluorocarbon plasma etching of Si and SiO/sub 2/," *ICOPS 2000. IEEE Conference Record - Abstracts. 27th IEEE International Conference on Plasma Science (Cat. No.00CH37087)*, 2000.

[20] J. Zhou, K. Zhu, C. Wang, W. He and H. Miao, "Quick development of copper electroplating formula for via and trench filling by an experiential method," *2020 21st International Conference on Electronic Packaging Technology (ICEPT)*, 2020, pp. 1-5.

[21] G. Greczynski, J. Jensen, and L. Hultman, “CrNx Films Prepared by DC Magnetron Sputtering and High-Power Pulsed Magnetron Sputtering: A Comparative Study,” *IEEE Transactions on Plasma Science*, vol. 38, no. 11, pp. 3046-3056, Nov. 2010.

Chapter 4

Distributed-model-based approach for electrical and thermal analysis of high-frequency GaN HEMTs

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4.1 Introduction

Wireless communication systems have penetrated almost every aspect of our daily lives with applications such as autonomous cars, personalized medicine, monitored healthcare, agricultural sensing, and merchandise inventory, to name only a few [1]. High output power and high operating frequency are the two most critical properties of the devices that embody the future of wireless communication systems in achieving higher data rates. Several examples of these systems can be found in 5G applications that are expected to operate at upper millimeter-wave (mm-wave) bands to meet the broad bandwidths and reconfigurability requirements. In general, all the technologies in this area owe their emergence and advancements to the material properties of gallium nitride (GaN) utilized in high electron mobility transistor (HEMT) devices [2]. High saturation velocity, high electron mobility, high sheet carrier density, and high breakdown voltage are some of these characteristics that make GaN a material that meets the requirements of building high-power amplifiers (HPAs) capable of working at high operating frequencies and temperatures [3].

The subject matter has attracted many research groups to enhance the device performance for various applications [4]. Consequently, developing accurate modeling techniques for these devices is demanded for having a simulation tool that predicts the device behavior and can be used at the design stage [5]. Equivalent circuit approach is the most typical transistor model which is used extensively in characterizing and designing integrated circuits or individual devices. A common high-frequency model of a GaN HEMT device is comprised of intrinsic and

extrinsic sections. The elements for the extrinsic section of the model demonstrate the effects of the electrode material and dimensions, transistor pads, and all the semiconductor layers under the conductors, whereas the intrinsic elements show the innate behavior and characteristics of the transistor when operating.

Many of the reported modeling procedures are based on S-parameter measurement results and I-V characteristics of the devices. These processes are considered along with the gate-forward and pinched-off measurements followed by a de-embedding process to separate the extrinsic section from intrinsic parameters [6]. Some techniques utilize the X-parameter measurements which eliminates the need for DC measurements and better incorporates the nonlinearities in the modeling process [7]. Initially, the parameter extraction techniques used a direct methodology with a very high sensitivity to the measurement results, but these methods were computationally inexpensive [8]. To address the limitations associated with the direct methods, optimization techniques were incorporated which reduces the sensitivity of the method to the measurement, provided that the improved technique yields reliable results for extraction [9]. A newly developed optimization technique is the Particle-Swarm-Optimization (PSO) which is applied to a GaN HEMT device accounting for high-frequency and high-power operations of the device by adding more elements to the model [10].

Developing system-level simulation tools is the direct outcome of the improved accuracy of circuit models [11]. Most of the contemporary devices in the area of advanced microwave systems are designed based upon highly varied physical dimensions and are operating in various frequency scales. Hence, the topics such as electromagnetic-wave propagations must be addressed in the modeling process [12]. Many of the already developed modeling techniques require the device fabrication and characterization in order to be able to find the element values

in the equivalent circuit model for different operating modes, power levels, and frequency ranges [13]. This procedure requires a great amount of processing time and imposes high operational costs, which is considered as one of the main limitations with the already reported circuit models and extraction techniques.

The main goal of introducing a modeling technique is to develop a simulation tool that is able to help in optimizing the device performance for different applications and operating frequencies, and this is supposed to be performed before going through the fabrication process. Additionally, the reliability of the results obtained from these techniques is normally satisfied at a specific frequency range and drastic changes are made to either the number of elements or the parameter values when the device is operating at higher frequencies. This is due to the fact that the effects associated with the wave propagation phenomenon are not considered in the process which may render the developed model inaccurate at higher frequency bands. The concept of distributed equivalent-circuit model that was initially introduced by Heinrich for traveling-wave FETs is believed to be the promising modeling approach that addresses the above-mentioned problems [14].

The limitations regarding the distributed effects when the device width is comparable to the wavelength were discussed by El-Ghazaly [15], where an inverted-gate field effect transistor was proposed to avoid the phase-cancellations in a common-gate configuration. The air-bridged gate MESFET was then proposed by Hammadi to reduce the wave propagation effects at high-frequency bands by keeping both the input and output signals in-phase along the device width [16]. Hammadi explicitly discussed approaches to incorporate the electromagnetic-wave effects in full-wave transistor models. Additionally, in [17], Al-Sunaidi proposed a full-wave physics-based model which takes into account the effects of wave-particle interactions on the

operation of high-frequency devices. Key observations of the research around this subject and the associated findings suggest that due to the coupling of the passive and active sections inside high-frequency devices and the complexity of the electron dynamics, it is crucial to have the required cognizance to the travelling-wave effects in these devices.

In this chapter, the distributed modeling approach is utilized to develop the small-signal equivalent circuit for a recently fabricated GaN HEMT device. This work, which builds upon the prior published research in [18-19], starts with discussing the details of the device structure. The developed small-signal model is presented and the extraction techniques for obtaining the parameter values for all the elements present in the model are discussed. It is also explained how the structural dimension of the device is used in the extraction process. The distributed model along with details of the utilized numerical method and how this model can be a representative of the entire device width are introduced and discussed. For validating the results, different gain parameters of the transistor are used to compare the simulation and measurement results obtained from the presented GaN HEMT device. The necessity of using the distributed model for wider devices operating at higher frequency ranges is also examined. Moreover, a study of the heat transfer phenomena for the distributed model developed for the GaN device on sapphire is presented here. The experiment demonstrates the heat distribution over the device width, and it is explained why the distribution of heat is critical to be considered while developing the equivalent circuit model.

4.2 Device configuration and modeling procedure

The cross-section of the 0.1-μm N-polar oriented GaN MISHEMT (Metal-Insulator-Semiconductor HEMT), developed by Zheng *et al.*, is demonstrated in Fig. 4.1, which describes

the different semiconductor layers with specific thicknesses and the associated doping profiles grown on an a-plane sapphire substrate [20]. The main advantage of the nitrogen-polar oriented GaN devices is their potential of providing sufficient power amplification in the W-band frequency range [21]. The growth technique for this device is the metal-organic chemical vapor deposition (MOCVD) and the materials used for the electrodes are gold and titanium. The dimensions of the drain and source electrodes are 0.12×6 μm. The gate top and gate stem dimensions are 0.53×0.45 μm and 0.22×0.1 μm, respectively. The spacing between the gate and source electrode is 0.3 μm which is relatively small compared to the 1.6 μm of gate-drain spacing. The attenuation of the signal along the gate electrode was one of the limitations with the initially structured HEMT devices due to the presence of a large parasitic resistance on the gate electrode. This limitation has been addressed in the recent devices by increasing the cross-sectional area of the gate metal strip in T- or mushroom-shaped configurations.

As discussed before, the 5G technology and generally all the wireless communication applications are expected to work at the mm-wave frequency range. Consequently, due to the current limitations on the device fabrication technologies, the dimensions of the active component (specifically the device width) become comparable to the electromagnetic wavelength of the propagating signal inside the device. As the input impedance of the transistor (gate electrode) is different than the output impedance (drain electrode), the wave propagation phenomenon affects the behavior of the device, and it is essential to include this effect in the modeling process. In consequence, the device electrodes must be considered as transmission lines [15]. This means that the lumped element models will not have sufficient accuracy to represent the operation of high-frequency devices. Considering the effects of wave-particle interactions in the developed equivalent circuit is the main contribution of the proposed approach

compared to the other distributed techniques, which ensures that the final model is independent of the operating frequency of the device.

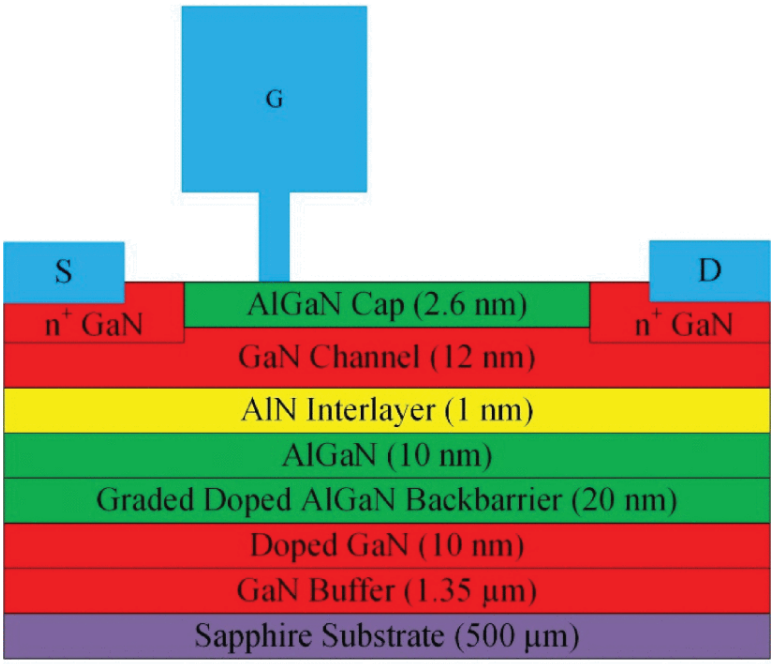

Fig. 4.1 Cross-section of the N-polar oriented GaN MISHEMT device.

The 19-element equivalent circuit model of the presented GaN MISHEMT device is demonstrated in Fig. 4.2. The extrinsic bias independent elements represent the passive section of the device, whereas the active part is formed by the intrinsic bias dependent components. There are specific physical descriptions and explanations associated with the elements of the model. R_{GSi} represents the resistance of the channel and R_{GDi} is complementary to that element in order to have symmetry in the circuit model. C_{GSi} and C_{GDi} demonstrate the charge modulation for the gate electrode when V_{GS} and V_{DS} change, respectively. Gate electrode contact is associated with a Schottky barrier and R_{Ge} shows the resistance to the flow of current along its metal strip. Furthermore, R_{De} and R_{Se} demonstrate the resistance of the drain and source ohmic contacts and the access region [22].

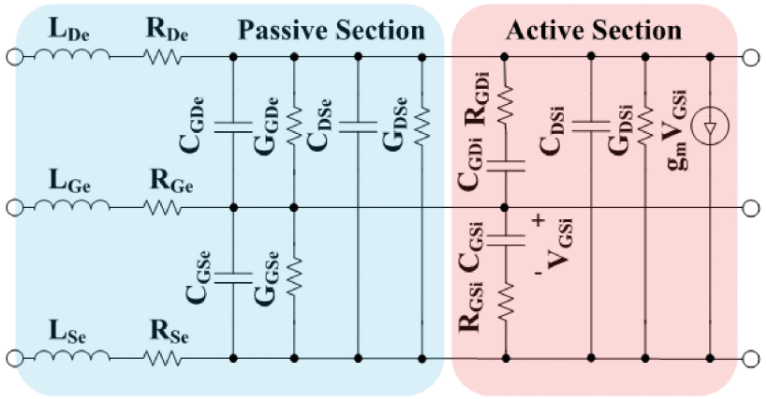

Fig. 4.2 Intrinsic and extrinsic sections of the equivalent circuit model for the GaN MISHEMT device [19].

4.2.1 Extrinsic elements extraction

The inductors and capacitors for the transmission line section are obtained using a three-dimensional electromagnetic equation solver. Depending on the device dimensions and the anticipated operating frequency band, the quasi-transverse electromagnetic approximations may be applied to simplify this step. The validity of this assumption is typically justified when the anticipated operating frequency is in the mm-wave range and as the separation between the source and drain electrode is quite short (2 µm) and the thickness for the active layer is in the range of 0.1 µm, the dominant mode is quasi-transverse electromagnetic [15]. In order to extract the values for the extrinsic mutual capacitors (i.e., C_{GSe}, C_{GDe}, and C_{DSe}), the transistor is modelled in COMSOL Multiphysics, as the 3D Laplace solver, and all the boundary conditions are defined. Based on the fabricated device in [20], the materials used for the electrodes are titanium and gold. Since the spacing between the electrodes is very short, most of the energy will be accumulated in the gap. In order to find the coupling capacitance between the electrodes, one conductor is excited with a defined voltage and then the charge is observed on the other two electrodes.

The other attribute resulting from the quasi-transverse electromagnetic mode propagation is that the semiconductor layers under the conductors do not affect the magnetic field and the same procedure applies for solving Laplace equation to obtain the inductors. First, the relative permittivity of the entire space, except for the electrodes, is assumed to be equal to free space permittivity and then the capacitance on each conductor (self-capacitance) is obtained. In any chosen medium and regardless of the geometry of the transmission line, phase velocity is equal to the speed of light and the inductance of the line is obtained using Equation (4.1), where v denotes the speed of light, C is the capacitance per unit width of the device, and L is the inductance per unit width. If the equivalent circuit is defined in such a way that mutual inductors are also present, the solution starts with obtaining the mutual capacitance between the lines.

$$v = \frac{1}{\sqrt{LC}} \tag{4.1}$$

The process for finding the conductance between the lines is very close to obtaining the capacitance, except that there is no need to define the magnetic walls as the boundary condition. The same structure is arranged, and the electrodes are excited with a voltage and then the current on the conductors are observed. To get an exact value for the current, a proper conductivity is needed to be defined and Equation (4.2) is used to find this parameter for each semiconductor layer present under the electrodes. Assuming that the conductivity is due entirely to electrons, σ represents the conductivity, q is the electron charge, μ is the electron mobility, and n denotes the carrier concentration. Obviously, thicker layers and the ones that are closer to the electrodes will have a more significant effect on the overall conductivity.

$$\sigma = q\mu n \tag{4.2}$$

In order to obtain the resistance of the electrodes or conductor loss, Wheeler's incremental inductance rule is applied [23]. Due to the lossy nature of the metal used as the

conductor, the magnetic field in the surrounding space will penetrate into the conductor which results in an internal inductance. Derivation of this internal inductance using direct methods is difficult, but based on the proposed method by Wheeler, it can be obtained using Equation (4.3). L_{in} is the internal inductance, L_{ext} represents the external inductance, and δ denotes the skin depth. The internal inductance is the difference between the external inductance for the normal case and a case where all sides of the conductor is reduced by an incremental amount equal to half the skin depth of the metal. Consequently, as the surface impedance caused by the current flow within the conductor has equal reactive and resistive components, the conductor loss is related to the internal inductance using Equation (4.4), where ω is the angular frequency and R is the resistance of the line.

$$L_{in} = L_{ext}(x) - L_{ext}\left(x - \frac{\delta}{2}\right) \tag{4.3}$$

$$R = \omega L_{in} \tag{4.4}$$

Equation (4.4) illustrates that the resistance of the line is a frequency dependent parameter. However, if we consider a case where the electrode dimensions are very small, the frequency of operation is in the GHz range, and the metal used for the electrodes has a good conductivity, the skin depth may be larger than at least half of the electrode dimension. In this case, the incremental inductance rule cannot be applied to obtain the conductor loss anymore and we assume that the current flow inside the conductor is uniform for that operating frequency. Consequently, the resistance is calculated using the resistivity of the material (ρ), length of the conductor (l), and the cross-sectional area (A) as expressed in Equation (4.5). Other than the extrinsic parameters for the device itself, the proposed extraction method may also be applied to the transistor pads which are used to connect to other devices and their effect cannot be neglected in higher frequencies.

$$R = \rho \frac{l}{A} \tag{4.5}$$

4.2.2 Intrinsic elements extraction

To estimate the values of the bias dependent intrinsic elements, the fabricated device is simulated in SILVACO. All the parameters associated with the different layers along with the two-dimensional electron gas (2DEG) density are included in the simulation. At a specific operating frequency, the Y-parameters of the device are obtained, and the intrinsic parameter values are calculated. There are two more elements, apart from the 7 intrinsic elements, associated with the gate-drain and gate-source current leakage, that due to possessing negligibly small values have been ignored. The derived Y-parameters and the derivation are accurate enough for acquiring all the intrinsic parameters, except the gate-drain resistance for some HEMTs with very narrow gate lengths operating at high frequencies. Therefore, an optimization scheme is required to fit the Y-parameters.

4.3 Distributed modeling approach and finite difference analysis

The first step to develop a distributed model is to divide the device width into N sections. Each of these sections will be named a unit cell hereafter and has a width of Δz. It is worth noting that the device width in a high-frequency HEMT device signifies the direction along the electrodes which is perpendicular to the flow of charges. The equivalent circuit model for each unit cell has already been demonstrated in Fig. 4.2 and for this model to be valid, the value for N and, consequently, Δz must be adjusted in a way that the unit cell width becomes much smaller than the propagating wavelength inside the device. All of these unit cells are then cascaded to represent the whole width of the device, as demonstrated in Fig. 4.3. The boundary and terminal

conditions must also be incorporated in this model, and this is performed according to the top view schematic of the device is Fig. 4.4 [21]. The device has two fingers, and the width of each finger is 25 μm. The source pad at the end of the device is grounded and a sinusoidal voltage source is applied to the gate electrode at the input side of the device.

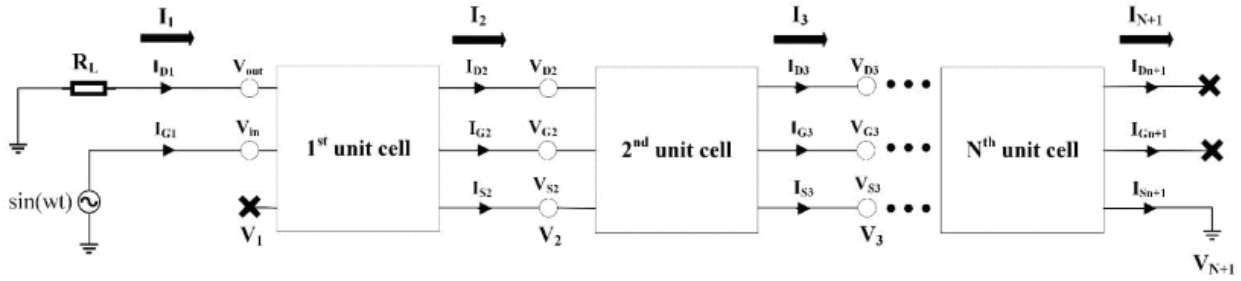

Fig. 4.3 Distributed model of the GaN MISHEMT device.

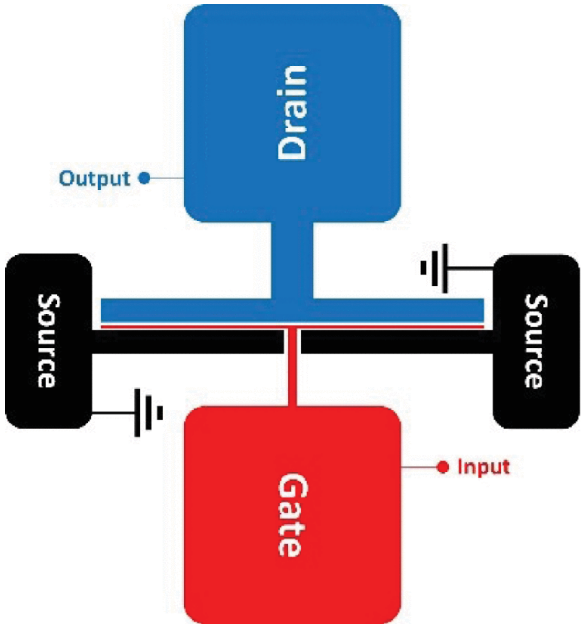

Fig. 4.4 Top-view schematic of the HEMT device for incorporating the boundary conditions.

The currents and voltages on the gate, drain, and source lines must be obtained at each temporal and spatial point based on the governing equations representing the properties of the coupled lines and the guided-wave propagations inside the device as demonstrated in

Equations (4.6) and (4.7). The superscript *t* denotes the time, *n* is the representation of the spatial point, and *i* , *j* , and *k* interchangeably show the gate, drain, and source lines. Due to the coupled nature of the system and since there are no analytical solutions for analyzing the six presented differential equations dominating this system, a finite-difference time-domain (FDTD) approach is utilized. In [18], an iterative explicit scheme was used to analyze the device, where a state of the system at a later time is calculated based on the current state of the system. As the explicit scheme is conditionally stable, there is a limitation associated with the temporal step size in order to satisfy the Courant stability condition. This condition is explained as the smaller value of the numerical time step compared to the time that the wave needs to travel to the adjacent grid point [24]. For analyzing complicated systems, Δt must be extremely small to keep the resultant numerical error bounded and this process increases the computation time of the solution. On the contrary, the developed iterative implicit scheme in this study involves both the values for the later time and the current state while solving the equations and, as a result, the scheme becomes unconditionally stable. This scheme allows the usage of larger temporal step sizes and makes the solution computationally efficient [25]. For the same practical circuit simulation, the time step was increased from 10^{-16} seconds for the explicit case to 10^{-13} seconds for the implicit scheme. It is also worth noting that for the mentioned schemes, the solution starts with an initial condition and then the final response is obtained when the desired convergence is achieved.

$$V^t_{i(n-1)} - V^t_{i(n)} = R_i I^t_{i(n)} + L_i \frac{\left(I^{t+\Delta t}_{i(n)} - I^t_{i(n)}\right)}{\Delta t} \tag{4.6}$$

$$I^t_{i(n)} - I^t_{i(n+1)} = G_{ij}\left(V^t_{i(n)} - V^t_{j(n)}\right) + G_{ik}\left(V^t_{i(n)} - V^t_{k(n)}\right) + C_{ij} \frac{\left(\left(V^{t+\Delta t}_{i(n)} - V^{t+\Delta t}_{j(n)}\right) - \left(V^t_{i(n)} - V^t_{j(n)}\right)\right)}{\Delta t} -$$

$$C_{ik} \frac{\left(\left(V^{t+\Delta t}_{i(n)} - V^{t+\Delta t}_{k(n)}\right) - \left(V^t_{i(n)} - V^t_{k(n)}\right)\right)}{\Delta t} \tag{4.7}$$

4.4 Simulation and model validation

To examine the validity of the simulation, the obtained results from the FDTD method are compared with the measurement results from the 2×25 µm N-polar GaN MISHEMT presented before. Fig. 4.5 shows the current gain (h_{21}) comparison where the load impedance of the model is set to zero and Fig 4.6 presents the comparison results for the maximum stable gain (MSG) between the measurement and simulation, in which the input and output impedances are matched to the circuit. Due to the fact that these comparisons are being made over the frequency range of 0.25-67 GHz, considering two unit cells of width 12.5 µm each is sufficient for this simulation. As demonstrated, excellent agreement is achieved for the case of current gain and there is a negligibly small average error of roughly 1 dB for the MSG results between the measurement and simulation. In consequence, the distributed modeling approach yields accurate results, and the validity of the method is proved. Also, based on the developed distributed model for the device, the extrinsic-level S-parameter simulation results are obtained, as depicted in Fig. 4.7, for the same frequency range and bias point. These S parameters exhibit the typical response expected from a high-frequency modern GaN HEMT, and phenomenologically agree with published results [26].

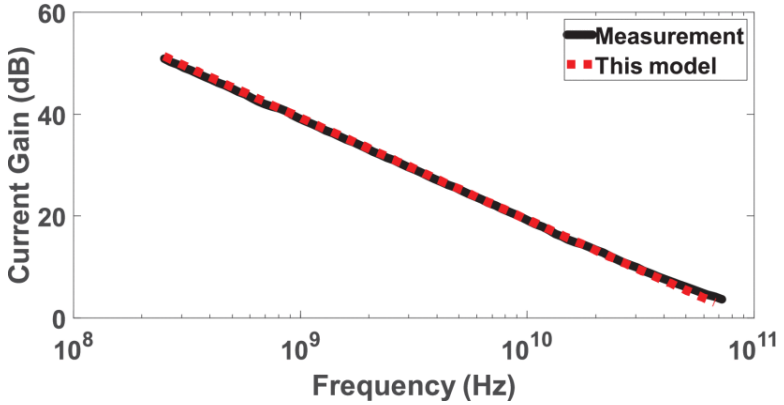

Fig. 4.5 Current gain comparison results between measurement and simulation over 0.25-67 GHz.

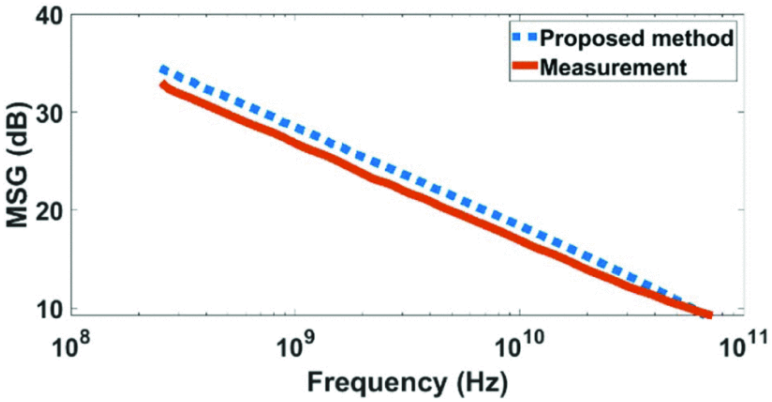

Fig. 4.6 MSG comparison between the proposed method and the measurement results.

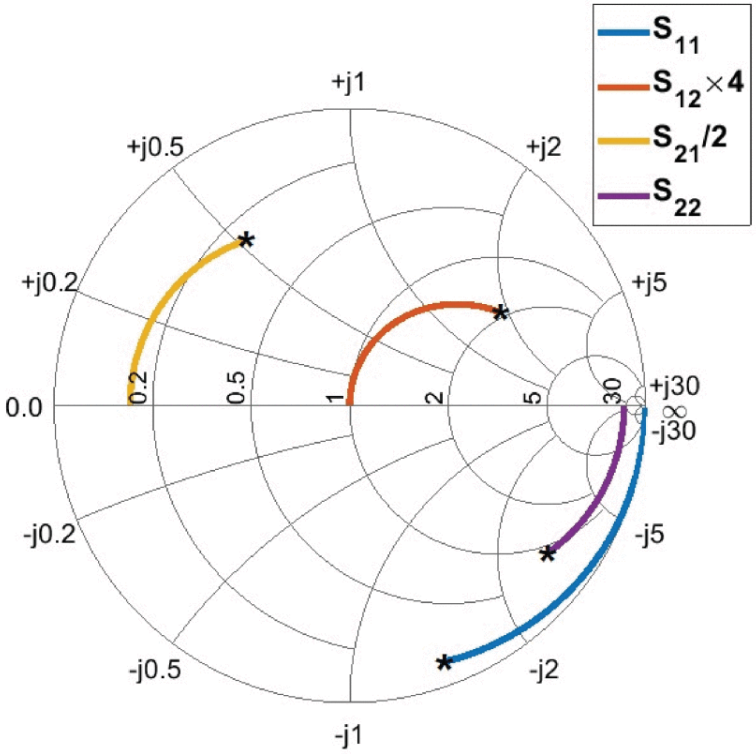

Fig. 4.7 S-parameter simulation results for the GaN HEMT device over 0.25-67 GHz frequency range. The asterisk on each curve represents the obtained results for the highest operating frequency (67 GHz).

To investigate the necessity of using a distributed modeling approach and illustrate the convergence of the results, a hypothetical device of width 100 µm is simulated over the frequency range of 70–150 GHz. The width and the operating frequency are considered in this

way to ensure that the electromagnetic-wave propagation effects are significant and observable in this case. The parameter values are adjusted, and the boundary conditions are defined accordingly. The current gain and maximum available gain (MAG) results are obtained for different number of unit cells in the distributed model and the results are shown in Fig. 4.8 and Fig. 4.9, respectively. The number of unit cells for each case represents the value for N and the unit cell width is equal to 100/N μm. For all of the mentioned cases, the device width is kept constant. Only, the number of unit cells and the unit cell width are varied. According to Fig. 4.8, the one unit cell case starts to deviate at around 85 GHz and the sensitivity of the current gain parameter to the case of two unit cells happens initially at 100 GHz [19]. This implies that since the unit cell width for these two cases is not sufficiently small compared to the wavelength of the guided wave at those frequency ranges, and due to the electromagnetic wave-propagation effects, the yielded results are inaccurate. For the cases of three unit cells and up, the results are consistent and the required convergence is achieved. In other words, to obtain accurate results for a device width of 100 μm over the frequency range of 70–150 GHz, the distributed equivalent circuit model must have at least three unit cells to ensure that the wave-propagation effects are taken into account.

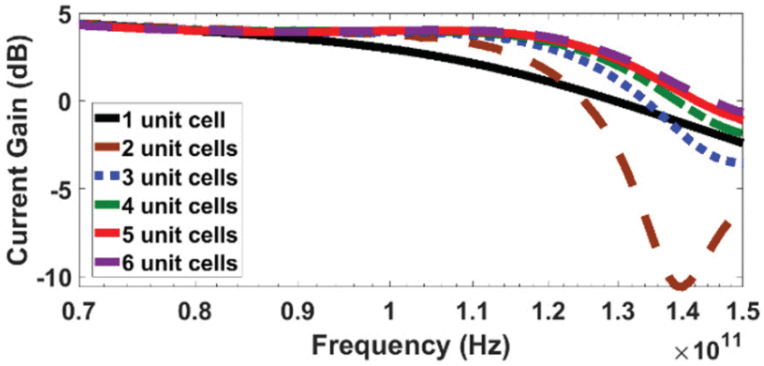

Fig. 4.8 Current gain results for different unit cell numbers over 70-150 GHz [19].

Similarly, as demonstrated in Fig. 4.9, the two cases of one and two unit cells are totally divergent and inaccurate and the consistency of the results starts from three-unit cells. In conclusion, for developing circuit models for wider devices operating at higher frequency ranges, it is necessary to use a distributed modeling approach and adjust the required number of unit cells accordingly. It is also worth noting that, for the lower frequency range, since the wavelength is large, the electrical behavior of the device is not affected by the wave propagation and the device can be modelled using lumped element equivalent circuits. This is the main reason for observing the device behavior at higher frequency bands.

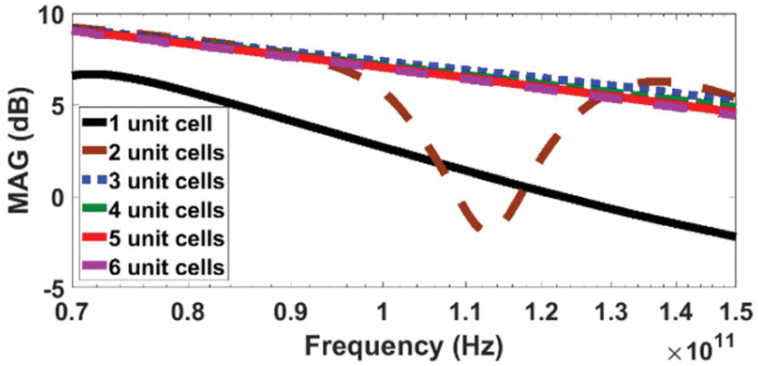

Fig. 4.9 MAG results for different unit cell numbers over 70-150 GHz.

4.5 Heat distribution effects

Improvements in fabrication technology have been identified as the primary reason for the increase in the speed of semiconductor devices which results in device size reductions. However, the dominant limitation for the speed or reduced size of the devices is the thermal resistance [27-31]. For high-power transistors, the ability of the device to dissipate the heat is one of the most important characteristics [32]. To identify this feature, the thermal resistance parameter is utilized which is defined as the temperature increase at the junction divided by the dissipated power [33]. When analyzing the device, the maximum power dissipation must be specified by determining the temperature that the junction can handle [34-35].

Experiments have shown that for transistors operating at higher frequencies, device failures may occur even below the power levels determined by the thermal resistance. Hence, for a thorough characterization of semiconductor devices, other than the electronic behavior of the transistors, the study of device operations under different temperature ranges is also very vital [36-37]. In high-power and high-frequency devices, a great amount of heat is generated in the channel layer, which flows through the other layers toward the substrate and affects the underlying physics of the device. The thermal limitations multiply when there are more interfaces in the device structure which makes it more sensitive to the excess generated heat.

In order to examine the heat distribution on the GaN HEMT device, an experiment is designed based on the configuration explained in Fig. 4.10. The cylinder represents the sapphire substrate that the device is grown on, with a circular base radius of 500 μm and a height of 100 μm. The cuboid on top of the cylinder is made of GaN to roughly represent all the semiconductor layers grown on the substrate. The cross-section of the cuboid is a 200×200 μm square and the height of that is equal to 2 μm. A rectangular area of 10×100 μm is considered on the top surface of this cuboid as the section representing the gate electrode and its vicinity, where the majority of the internal heat is generated along the device width while operating. A convection boundary condition is defined for all the surfaces except the bottom face of the cylinder. Since a heat sink is generally mounted on that side of the substrate, the internally generated heat reaching that surface is dissipated to the environment. Hence, that surface is defined with a temperature boundary condition set to the ambient temperature. To show the effects of heat distribution on the distributed model, another arrangement is considered in which the rectangular area on top is divided into five equal sections with a unit cell width of 20 μm.

This configuration is shown in the inset of Fig. 4.10. All the other device dimensions, materials used, and boundary conditions are defined similar to the typical case.

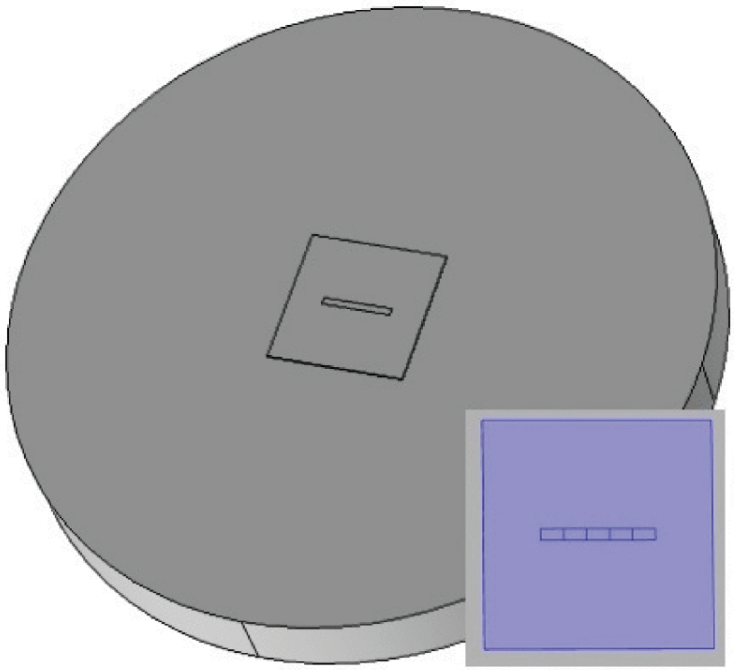

Fig. 4.10 Device structure for thermal analysis of GaN HEMT device on a sapphire substrate.

Fig. 4.11 shows the cross-section of the simulated model, not drawn to scale, and the assumed cut lines on which the temperature distribution is desired to be observed. CL1 (cut-line 1) is along the device width and CL3, CL4, and CL5 are drawn along the depth of the device. A power of 1 W is uniformly applied to the rectangular section of the typical case and 0.2 W to each unit cell of the distributed model. The temperature distribution at CL1 is depicted in Fig. 4.12, which shows the temperature for all the points through the device width. Based on this figure, the distribution for the two cases is in good agreement which proves that the distributed modeling approach offers consistent results from thermal point of view.

The unit cells at the two ends of the device show a distinctly different distribution compared to the middle unit cell and the temperature difference between the coldest and hottest

points of the device is about 118 K. In order to elaborate on this, the temperature distribution is also observed on CL3, CL4, and CL5, which are the cut lines over the first, second, and third unit cells. The obtained results are shown in Fig. 4.13 and, accordingly, the equivalent circuit model for each unit cell will be differently affected based on the thermal properties of the device. This phenomenon must be incorporated in extracting the extrinsic and intrinsic parameter values of the distributed model.

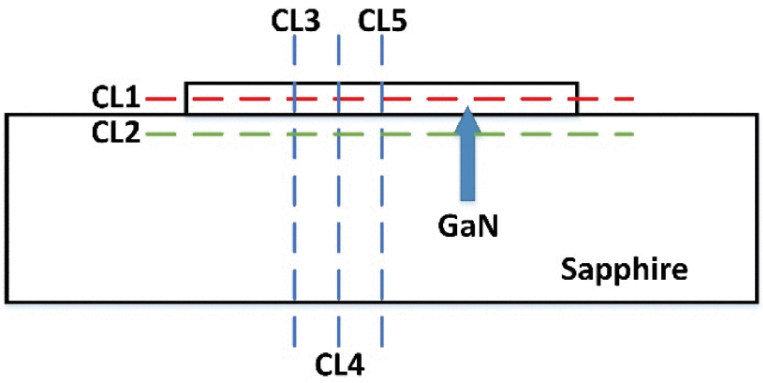

Fig. 4.11 Cross-section of the device and the cut lines to observe the temperature distribution.

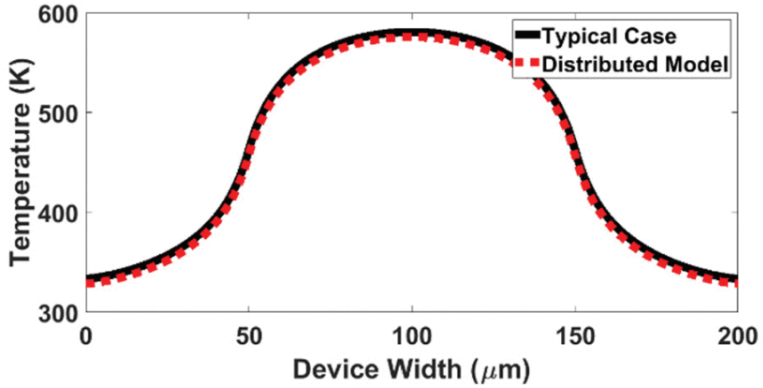

Fig. 4.12 The temperature distribution comparison between the typical and distributed model on CL1.

Another experiment is also designed to show the effect of the difference between the thermal conductivity of GaN and sapphire and how GaN semiconductor layers involve in

distributing the generated internal heat. The thermal conductivity parameter for sapphire is 25.2 W/m.K, whereas for GaN, with either a Wurtzite or Zinc Blende crystal structure, is 130 W/m.K. The GaN layer on top of the substrate in Fig. 4.10 is removed and the power of 1 W is applied directly to the same section on top of the sapphire substrate. The temperature distribution results on CL2 comparing the case when the power is applied to GaN and the other case when it is directly applied to sapphire substrate is demonstrated in Fig. 4.14. Despite the fact that the GaN layer compared to the sapphire substrate is very thin, due to the notable difference between the thermal conductivity of the two materials, the temperature distribution is markedly different. The temperature difference of the hottest points between the two cases is 155 K.

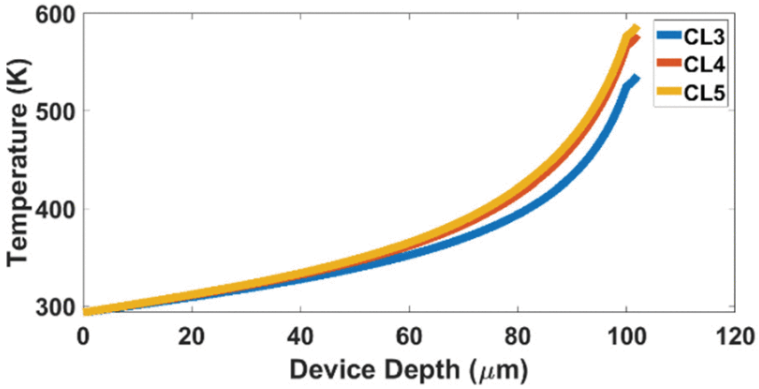

Fig. 4.13 Temperature distribution on three different unit cells.

Based on the fact that the width of the discussed GaN HEMT device in previous section, for which the electrical behavior was simulated, is relatively small, there was no need for parameter adjustments regarding the thermal properties. However, in other devices, the distributed model allows for semiconductor device properties to be adjusted at each segment to reflect the change in temperature. This is generally performed by either modifying the element values in the extrinsic and intrinsic sections of the equivalent circuit or by adding some elements to account for the changes.

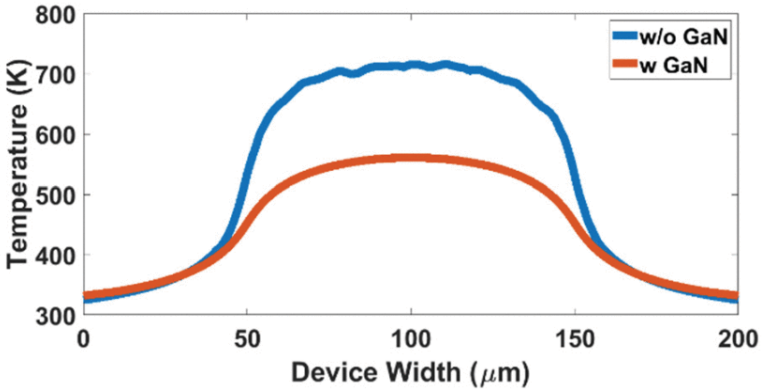

Fig. 4.14 Temperature distribution comparison with and without GaN layer on top of the substrate on CL2.

4.6 Conclusion

The studies conducted in this research explained the significance of using a distributed approach in developing an accurate equivalent circuit model valid for various devices operating at any frequency range and power level. Moreover, the thermal analysis of the presented device demonstrated that incorporating the heat distribution effects is a vital stage when developing the modeling techniques for simulating the electrical behavior of the devices. As discussed, the presented model is developed solely based upon the physical structure of the device and as long as the quasi-TEM approximation is valid, the device is capable of being expanded over all the dimensions. It is worth noting that this approximation holds true for all the Microwave and mm-wave devices for the current and future applications. The distributed modeling approach can also be expanded to account for different bias conditions by including the large signal analysis and all the typical nonlinearities inside semiconductor devices.

4.7 References

[1] M. Marzencki, P. Lin, T. Cho, J. Guo, B. Ngai, and B. Kaminska, “Remote health, activity, and asset monitoring with wireless sensor networks,” *Proc. IEEE 13th Int. Conf. e-Health Netw., Appl. Services*, Columbia, MO, USA, Jun. 2011, pp. 98–101.

[2] U. K. Mishra, S. Likun, T. E. Kazior, and Y.-F. Wu, “GaN-based RF power devices and amplifiers,” *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[3] A. G. Avval, E. Larique, and S. M. El-Ghazaly, “Heterojunction field effect transistors,” *Reference Module in Materials Science and Materials Engineering*. Amsterdam, The Netherlands: Elsevier, 2018.

[4] S. S. Pasayat, E. Ahmadi, B. Romanczyk, O. Koksaldi, A. Agarwal, M. Guidry, C. Gupta, C. Wurm, S. Keller, and U. K. Mishra, “First demonstration of RF N-polar GaN MIS-HEMTs grown on bulk GaN using PAMBE,” *Semicond. Sci. Technol.*, vol. 34, no. 4, Apr. 2019, Art. no. 045009.

[5] A. Jarndal, A. Z. Markos, and G. Kompa, “Improved modeling of GaN HEMTs on Si substrate for design of RF power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 644–651, Mar. 2011.

[6] G. Crupi, D. Xiao, D. M. M.-P. Schreurs, E. Limiti, A. Caddemi, W. De Raedt, and M. Germain, “Accurate multibias equivalent-circuit extraction for GaN HEMTs,” *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 10, pp. 3616–3622, Oct. 2006.

[7] D.E.Root, “Future device modeling trends,” *IEEE Microw. Mag.*, vol. 13, no. 7, pp. 45–59, Nov./Dec. 2012.

[8] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” *IEEE Trans. Microw. Theory Techn.*, vol. MTT-36, no. 7, pp. 1151–1159, Jul. 1988.

[9] R. Menozzi, A. Piazzi, and F. Contini, “Small-signal modeling for microwave FET linear circuits based on a genetic algorithm,” *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 43, no. 10, pp. 839–847, Oct. 1996.

[10] A. S. Hussein and A. H. Jarndal, “Reliable hybrid small-signal modeling of GaN HEMTs based on particle-swarm-optimization,” *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 9, pp. 1816–1824, Sep. 2018.

[11] Y. Wu, Y. Hao, J. Liu, and K. Kang, “A 220-GHz compact equivalent circuit model of CMOS transistors,” *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 7, pp. 651–653, Jul. 2017.

[12] S. El-Ghazaly and T. Itoh, “Inverted-gate field-effect transistors: Novel high-frequency structures,” *IEEE Trans. Electron Devices*, vol. ED-35, no. 7, pp. 810–817, Jul. 1988.

[13] R. J. Trew, “A zone-based approach for physics-based FETcompact models,” in *Proc. 21st Int. Conf. Microw., Radar Wireless Commun. (MIKON)*, Kraków, Poland, May 2016, pp. 1–4.

[14] W. Heinrich, “Distributed equivalent-circuit model for traveling-wave FET design,” *IEEE Trans. Microw. Theory Techn.*, vol. MTT-35, no. 5, pp. 487–491, May 1987.

[15] S. M. El-Ghazaly and T. Itoh, “Traveling-wave inverted-gate field-effect transistors: Concept, analysis, and potential,” *IEEE Trans. Microw. Theory Techn.*, vol. 37, no. 6, pp. 1027–1032, Jun. 1989.

[16] S. M. Hammadi and S. M. El-Ghazaly, “Air-bridged gate MESFET: A new structure to reduce wave propagation effects in high-frequency transistors,” *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 6, pp. 890–899, Jun. 1999.

[17] M. A. Alsunaidi, S. M. S. Imtiaz, and S. M. El-Ghazaly, “Electromagnetic wave effects on microwave transistors using a full-wave time-domain model,” *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 6, pp. 799–808, Jun. 1996.

[18] A. G. Avval and S. M. El-Ghazaly, “A new small-signal modelling approach for analyzing HEMTs over a broad frequency range,” *Proc. IEEE 62nd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Dallas, TX, USA, Aug. 2019, pp. 706–709.

[19] A. G. Avval and S. M. El-Ghazaly, “A reliable distributed modeling approach applied to high-frequency transistors,” in *Proc. IEEE Radio Wireless Symp. (RWS)*, San Antonio, TX, USA, Jan. 2020, pp. 1–4.

[20] X. Zheng, H. Li, E. Ahmadi, K. Hestroffer, M. Guidry, B. Romanczyk, S. Wienecke, S. Keller, and U. K. Mishra, “High frequency N-polar GaN planar MIS-HEMTs on sapphire with high breakdown and low dispersion,” *Proc. Lester Eastman Conf. (LEC)*, Bethlehem, PA, USA, Aug. 2016, pp. 42–45.

[21] M. Guidry, S. Wienecke, B. Romanczyk, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, S. Keller, and U. K. Mishra, “Small-signal model extraction of mm-wave N-polar GaN MISHEMT exhibiting record performance: Analysis of gain and validation by 94 GHz loadpull,” *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, May 2016, pp. 1–4.

[22] Z. Liu, “High frequency small-signal modelling of GaN high electron mobility transistors for RF applications,’’ M.S. thesis, Dept. Elect. Comput. Eng., Univ. Victoria, Victoria, BC, Canada, 2016.

[23] H.A.Wheeler, “Formulas for the skin effect,” *Proc. IRE*, vol. 30, no. 9, pp. 412–424, Sep. 1942.

[24] A. Ghadimi and S. Asadi, “Modelling of composite right/left-handed active multiconductor transmission lines (AMCTL) in time domain,” *Int. J. Numer. Model.*, vol. 31, no. 1, p. e2257, 2018.

[25] K. Afrooz, “Time domain analysis of field effect transistors using unconditionally stable finite difference method,” *IET Sci., Meas. Technol.*, vol. 10, no. 7, pp. 686–692, Oct. 2016.

[26] X. Zheng, H. Li, M. Guidry, B. Romanczyk, E. Ahmadi, K. Hestroffer, S. Wienecke, S. Keller, and U. K. Mishra, "Analysis of MOCVD SiN*x* passivated N-polar GaN MIS-HEMTs on sapphire with high f*max* · V*DS* ,*Q* ," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 409–412, Mar. 2018.

[27] A. Sarua, H. Ji, K. P. Hilton, D. J. Wallis, M. J. Uren, T. Martin, and M. Kuball, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3152–3158, Dec. 2007.

[28] J. Cho, Y. Li, D. H. Altman, W. E. Hoke, M. Asheghi, and K. E. Goodson, "Temperature dependent thermal resistances at GaN-substrate interfaces in GaN composite substrates," *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, La Jolla, CA, USA, Oct. 2012, pp. 1–4.

[29] G. J. Riedel, J. W. Pomeroy, K. P. Hilton, J. O. Maclean, D. J. Wallis, M. J. Uren, T. Martin, U. Forsberg, A. Lundskog, A. Kakanakova-Georgieva, G. Pozina, E. Janzen, R. Lossy, R. Pazirandeh, F. Brunner, J. Wurfl, and M. Kuball, "Reducing thermal resistance of AlGaN/GaN electronic devices using novel nucleation layers," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 103–106, Feb. 2009.

[30] A. Manoi, J. W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of thermal boundary resistance in AlGaN/GaN HEMTs on SiC substrates: Implications of the nucleation layer microstructure," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1395–1397, Dec. 2010.

[31] J. Chen, J. W. Pomeroy, N. Rorsman, C. Xia, C. Virojanadara, U. Forsberg, M. Kuball, and E. Janzén, "Low thermal resistance of a GaN-on-SiC transistor structure with improved structural properties at the interface," *J. Crystal Growth*, vol. 428, p. 54, Oct. 2015.

[32] R. Pagaila, "Semiconductor device and method of forming channels in back surface of FO-WLCSP for heat dissipation," U.S. Patent 9 431 316 B2, Aug. 30, 2016.

[33] A. G. Avval and S. M. El-Ghazaly, "Holistic optimization technique for solving low thermal conductivity of sapphire substrates in high frequency devices," *Proc. Texas Symp. Wireless Microw. Circuits Syst. (WMCS)*, Waco, TX, USA, Apr. 2018, pp. 1–4.

[34] B. Wrzecionko, J. Biela, and J. W. Kolar, "SiC power semiconductors in HEVs: Influence of junction temperature on power density, chip utilization and efficiency," *Proc. 35th Annu. Conf. IEEE Ind. Electron.*, Porto, Portugal, Nov. 2009, pp. 3834–3841.

[35] A. G. Avval, S. Yu, G. J. Salamo, and S. M. El-Ghazaly, "Apparatus and method to reduce the thermal resistance of semiconductor substrates," U.S. Patent 16 711 127, Jun. 18, 2020.

[36] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7183–7193, Oct. 2016.

[37] H. Wang, R. Zhu, H. Wang, M. Liserre, and F. Blaabjerg, “A thermal modeling method considering ambient temperature dynamics,” *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 6–9, Jan. 2020.

Chapter 5

Increasing transistor gain using metamaterial electrodes

Authors: Amirreza G. Avval, Samir M. El-Ghazaly

5.1 Introduction

The recent progress in semiconductor device fabrication techniques and microwave technology, in general, have been the key enablers for the development of high-frequency high-performance power amplifiers [1-2]. In order to achieve the desired performance at higher operating frequency bands, devices tend to be configured in smaller sizes and designed in compact structures. Higher cut-off frequency is commonly achieved by utilizing smaller gate lengths and is a direct outcome of the reduced gate-source capacitance and electron transit time. Moreover, the characteristics of active layers in semiconductor devices have been optimized thanks to the innate properties of wide-bandgap materials [3-5].

High efficiency, high power density, high gain, and high operating frequency are the main attributes of the device technologies utilized as the fundamental elements in developing solid-state power amplifiers for many of the microwave and millimeter-wave wireless communication applications. Recent millimeter-wave power amplifiers benefit from the underlying material properties of gallium nitride (GaN) along with its high electron mobility and breakdown voltage, which makes it the desired platform for fabricating devices such as high electron mobility transistors (HEMTs) [6]. These devices are now the essential components of many systems in applications such as satellite communications, 5G networks, and aerospace missions. In order to further optimize and improve these devices for achieving higher data rates in the mentioned applications, developing modeling approaches has been considered an indispensable stage in the design process. Researchers are seeking physics-based universally

satisfactory models to achieve accurate predictions for the performance of individual devices and integrated circuits in different operating modes and applications.

Transistor modeling techniques are generally divided into three groups: physical models, behavioral models, and equivalent circuit models [7]. The extraction of the physical models is based on the presence of various physical occurrences inside the device. On the other hand, behavioral models are developed according to the relations between different input and output values. Equivalent circuit models that are widely used for many of the recently developed technologies are generally extracted based on the experimental data of the device. However, as the various physical behaviors of the devices under different operating modes are understood, new terms and conditions must be introduced in order to improve the accuracy of these models. This requirement becomes even more complicated when the model is developed for complex mm-wave and RF systems with different nonlinearity levels to be taken into account [8].

One of the important topics in the contemporary millimeter-wave transistors is the electromagnetic wave propagations, which depends on the operating frequency of the device and the device dimensions. In general, the longest dimension of the device is the device width, that is the direction along the device electrodes, perpendicular to the electron flow. The phenomenon of wave propagations is observable when the wavelength of the guided wave inside the device becomes comparable to the device width (typically when the device width is larger than $\lambda/10$ but could be as small as $\lambda/20$ in some applications). These effects must be dealt with in two different aspects: device fabrication and circuit model development. According to the operating frequency of the device to be fabricated, the device width is typically kept at least 10 times smaller than the wavelength. This is to ensure that the phase velocity mismatch at the input and output ports of the device, which is a result of the wave propagation effects, does not have a significant impact

on deteriorating the gain of the device. A wider device relates to the added distributed transconductance effects and, hence, higher gain. However, reflections from open-ended device structures and the mismatch in phase velocity of the signals on the input and output conductors explain the fact that the performance of devices does not indefinitely improve by increasing the width. This is inherent to the structure of the device where the impedances on the gate and drain electrodes are different, which becomes more observable at higher operating frequency bands [9]. Having the required cognizance of this phenomenon provides enough information to eliminate its influence by considering some specific design rules [10].

As stated, to avoid the phase-cancelation effects, due to phase-velocity mismatch of the electromagnetic waves, the device width is kept at very small values compared to the wavelength of the guided wave inside the device, typically less than 10% [11]. Consequently, the gain-frequency relation maintains a linear behavior. However, when the device width becomes comparable to the wavelength at higher operating frequencies, the device gain does not decrease linearly and demonstrates a nonlinear performance like a sharp decrease or staying at a constant value. This imposes severe limitations on the cut-off frequency of the device and the bandwidth [12-13]. Accordingly, to obtain the required output, narrower (smaller width) transistors with multi-finger structures at device level and multi-stage configurations at amplifier level are utilized resulting in added discontinuities, extra transmission line sections, and being affected by nonlinear power combining properties [14-15]. This chapter provides insights into how the device behavior changes by increasing the frequency and presents solutions to eliminate the limitations for mm-wave high-performance devices.

On the other hand, the electromagnetic wave propagation effects must also be incorporated when developing equivalent circuit models for millimeter-wave devices, as it

significantly affects the accuracy of the models. When a circuit model for a device at the high-frequency range is developed without considering these effects, the model remains reliable up to a specific frequency range and it requires substantial modifications to yield accurate results at the upper frequency band. The concept of distributed modeling approach that was proposed for simulating traveling-wave FETs [16], has recently been utilized for this purpose and further enhanced for the recent complex device designs [17].

The developed equivalent circuit model in this chapter is utilized to accurately simulate the device behavior for a recently fabricated GaN MISHEMT (Metal-Insulator-semiconductor HEMT). Unlike many of the previously developed techniques, this model does not employ the experimental and measurement data of the fabricated device and the parameter extraction process is merely based on the physical structure of the device. The structural configuration of the device is provided which is utilized to extract the parameter values for the intrinsic and extrinsic sections. The concept of the distributed approach is then developed to eliminate the dependence of the model on the frequency which ensures the accuracy of the model over a broad operating frequency range. The small-signal and large-signal simulations are conducted, and the results are validated by measurement.

5.2 Device structure and equivalent circuit model

The specifications of the fabricated GaN MISHEMT device developed by Zheng *et al.* are demonstrated in Fig. 5.1 [18]. The device is grown on an a-plane sapphire substrate by metalorganic chemical vapor deposition (MOCVD). It consists of a semi-insulating GaN buffer, a Si-doped AlGaN back-barrier, an AlGaN interlayer, an unintentionally doped GaN channel, and an AlGaN cap. The gate electrode is structured in a trapezoidal form with a stem height of

220 nm, which ensures that the parasitic resistance on this electrode is sufficiently reduced. The device is nitrogen polar oriented which provides a better power amplification functionality compared to its gallium-oriented counterparts [19].

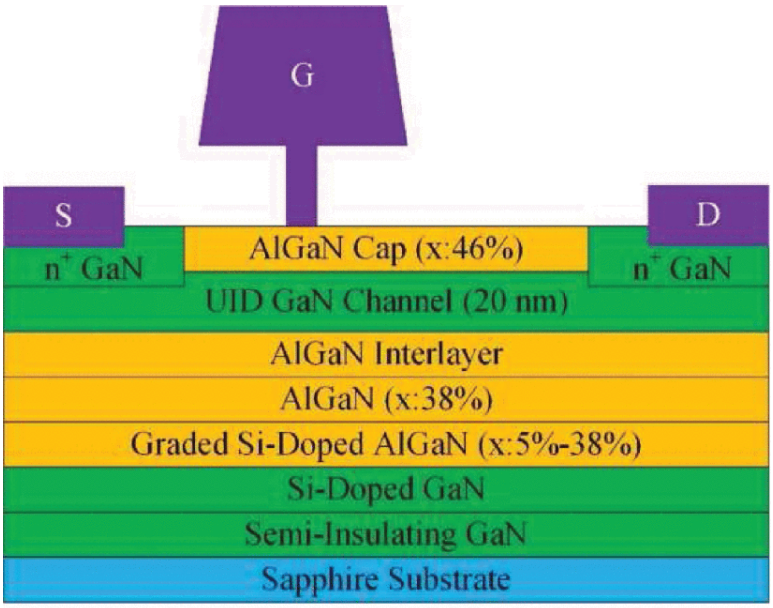

Fig. 5.1 Cross-section of the fabricated GaN MISHEMT device.

When the electromagnetic wavelength of the signal is comparable to the device width and since the impedance on the gate electrode (input port) is different than that of the drain electrode (output port), the wave propagation effects become observable. Hence, the distributed modeling approach in this work starts with considering the effects of the wave-particle interactions in developing the equivalent circuit model. This is performed by dividing the device width into N segments. Each of these segments is called a unit-cell which has a width of Δz. The number of segments and the unit-cell width are adapted according to the operating frequency of the device so as to keep the value of Δz much smaller than the wavelength of the propagating signal [20]. This way, the developed model will provide a universal equivalent circuit suitable at any operating frequency. Eventually, the entire device width will be represented by the cascaded

unit-cells. The GaN MISHEMT device has a 2-finger configuration, and the boundary conditions are incorporated according to the layout of the fabricated device in [18].

The distributed approach and the equivalent circuit representing each unit-cell are depicted in Fig. 5.2. The elements in the passive section are the extrinsic bias-independent elements and the active part represents the innate device behavior based on the bias-dependent components. The passive section represents pieces of transmission lines coupled together with three capacitances, each consisting of a pair of conductor planes. The logical sequence of the parameter-extraction approach starts with obtaining the per-unit-width values of these coupled capacitances. For this purpose, a conformal mapping technique is utilized in which the whole space surrounding the conductor planes is mapped onto an upper halfplane and then to the internal domain of a rectangle using Schwarz-Christoffel transformation [9,13]. Capacitance correction is then applied to account for the metallization thickness and fringing effects according to the Cohn's proposed method in [21]. For quasi-TEM approximation, the basic expression in Equation (5.1) can determine the inductance per-unit width of the extrinsic part.

$$L = \mu\epsilon/C \tag{5.1}$$

To account for the effect of skin penetration at higher frequencies, the per-unit-width resistances of the transmission lines are calculated using Wheeler's incremental inductance rule. To determine the internal inductance of the transmission line, the external inductance is obtained when the thickness of the conductor is reduced incrementally. Then, the per-unit-width resistance becomes equal to the amount of incremental change in inductance multiplied by the angular operating frequency. Table 5.1 shows the obtained per-unit-width values for the extrinsic parameters. The intrinsic parameters are obtained using the Y-parameters obtained for the two-port network at each bias point according to the proposed technique in [20].

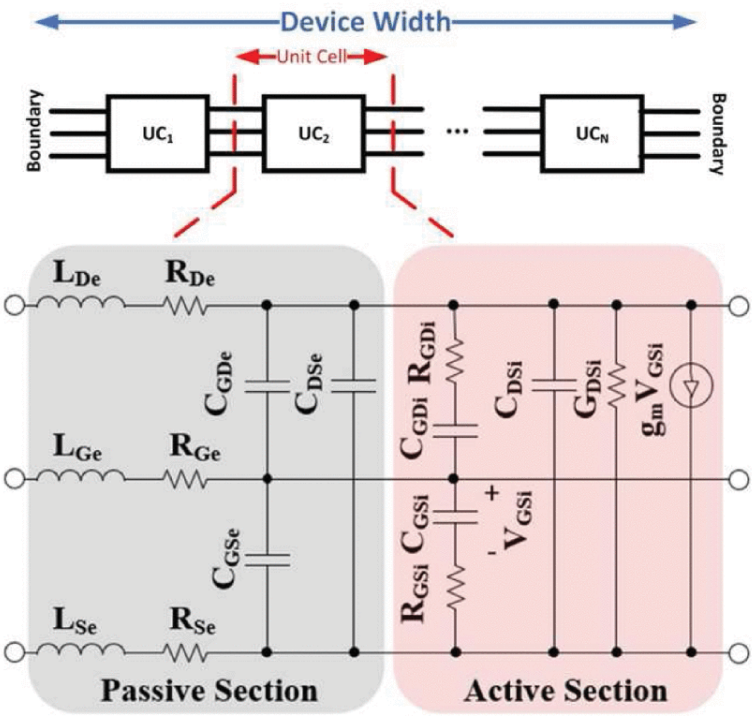

Fig. 5.2 Distributed model and equivalent circuit for each unit-cell of the device width.

Table 5.1 Per-unit-width extrinsic parameter values.

C_{GSe}	5.6 fF	L_{Ge}	48.4 pH	R_{Ge}	1.45 Ω
C_{GDe}	1.0 fF	L_{De}	38.3 pH	R_{De}	21.33 Ω
C_{DSe}	6.4 fF	L_{Se}	7.0 pH	R_{Se}	11.71 Ω

5.3 Small-signal analysis

The fabricated GaN MISHEMT device has a 2-finger configuration, a gate length of 0.1 µm, gate-source spacing of 0.2 µm, and gate-drain spacing of 1 µm. To compare the small-signal measurement and simulation results, two devices with widths of 50 µm (Device A) and 25 µm (Device B) are utilized. Device A is biased at a drain-source voltage of 5.5 V and a gate source voltage of -4.6 V and Device B is biased at a drain-source voltage of 11 V and gate-source voltage of -4.8 V. The current gain simulation results obtained from the distributed modeling approach is compared with the measurement results as depicted in Fig. 5.3 for Device A and

Device B. Excellent agreement is achieved for the two cases. For these simulations, five unit-cells are considered for developing the distributed model. This is to ensure that the unit-cell width is much smaller than the wavelength of the propagating signal inside the device.

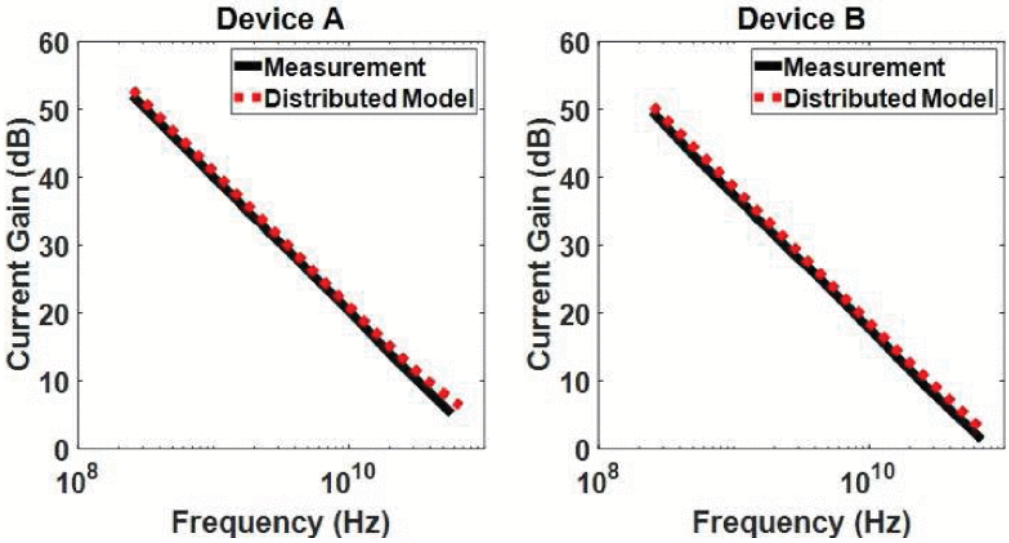

Fig. 5.3 Current gain comparison results for Device A biased at V_{DS}=5.5 V and V_{GS}=−4.6 V and Device B biased at V_{DS}=11 V and V_{GS}=−4.8 V over the frequency range of 0.25-67 GHz.

5.4 Large-signal analysis

After validating the model with the small-signal simulation, the large-signal simulation results are also obtained and compared with the measurement results for the same GaN MISHEMT device [22]. For this analysis, the width of the device under test is 75 μm and structured in a 2-finger configuration. The larger width for this case is to have a higher current under high-voltage conditions for a load power match. The large-signal performance is obtained under class-AB operation at 10 GHz, with an $I_{D,Q}$ of 100 mA/mm and $V_{DS,Q}$ of 20 V. According to the quiescent drain current value and the DC simulation results, the device is biased at a gate-source voltage of -3.75 V. The required intrinsic parameters for this case are derived and the same distributed scheme is utilized to obtain the simulation results. Fig. 5.4 represents the comparison results between the simulation and measurement for the output power (in W/mm) of

the device over a range of input power values. Similarly, there is a good agreement between the measurement and simulation results for the large-signal analysis, which further proves the validity of the developed model under different bias conditions. The same set of comparison results for the device gain is also demonstrated in Fig. 5.5.

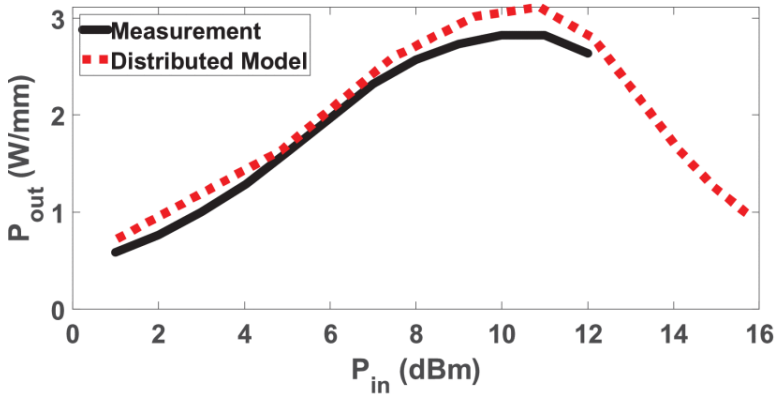

Fig. 5.4 Output power comparison results for the large-signal performance of the GaN MISHEMT at 10 GHz.

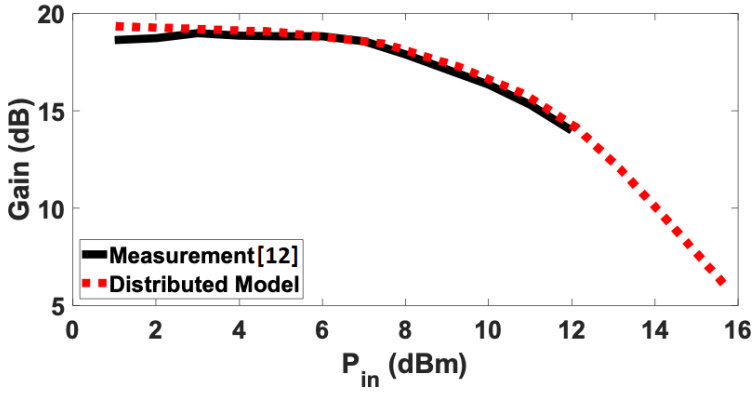

Fig. 5.5 Gain comparison results for the large-signal performance of the GaN MISHEMT at 10 GHz.

5.5 Operability limitations in mm-wave devices

To analyze the device behavior in different operating frequency bands, the current is observed over the device width. Fig. 5.6 shows the peak-to-peak value of the gate and drain

currents over the course of the device width for five different operating frequencies. The phase velocity of the signals at different operating frequencies are estimated by the simulator and, accordingly, the wavelengths are calculated. Since all the wavelength values are relatively large compared to the device width, the current signals for the gate and drain electrodes demonstrate a traveling wave pattern along the device. In other words, the electromagnetic wave propagation effects are not observable at these frequencies and the device can maintain its operation without the mismatch limitations.

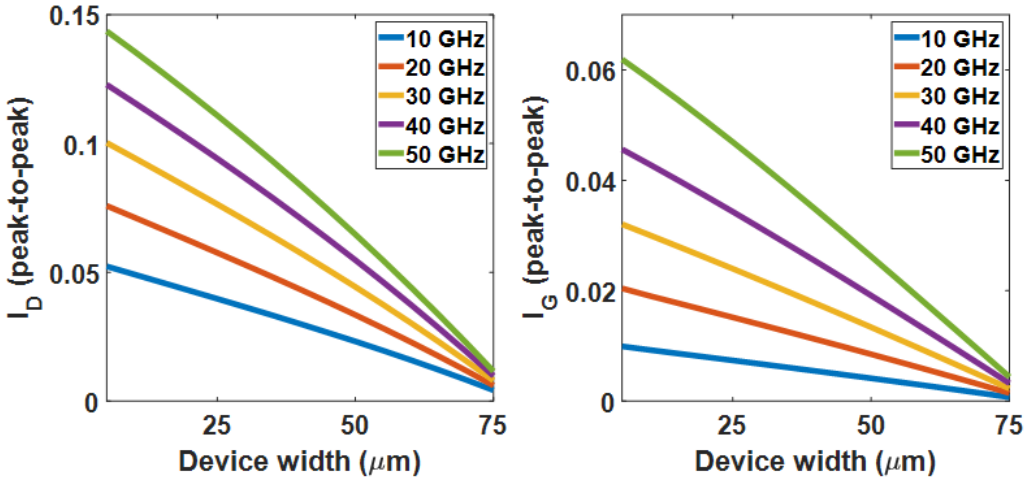

Fig. 5.6 Gate and drain currents along the device width for five different operating frequencies (traveling wave behavior).

Above a certain operating frequency, the linear relation between the output power and operating frequency changes due to the presence of a mismatch phenomenon inside the device. In other words, the signal distribution along the device width is shaped by the superposition of two or more waves that are propagating at the same frequency. These waves are identified as the main signal on one conductor, along with the reflections from the device end and the interactions from the signals on other two conductors. The reflection of the current/voltage signal from the other end of the device, as one of the reasons for the creation of a so-called standing wave, is

normally caused by an impedance mismatch or open-/short-circuit boundary conditions. As a result of this behaviour, the power transfer capabilities of the device are degraded, though a good portion of this reflection is zeroed by utilizing load pull systems, where the output impedance of the device is systematically varied to extract the best performance at the output.

Another important reason behind the creation of a standing wave for the current/voltage signals is the mismatch between the phases of the two signals on the drain and gate conductors. These two signals continuously affect each other along the device width which results in distortions in the propagating signals. This is considered as the main cause of degradation of the device gain where the linear relation between the device output and operating frequency is not maintained. Fig. 5.7 shows the current distributions on the gate and drain electrodes at a frequency range in which the wave propagation effects and, hence, phase velocity mismatch is observable. As shown in this figure, a superposition of a traveling wave and a standing wave is recognizable in both input and output currents, which is called a partial standing wave. This phenomenon is interpreted from a velocity viewpoint as well. For finding the phase velocity on the drain and gate electrodes, the already developed equation of $1/\sqrt{LC}$ is utilized, where L and C are, respectively, the per-unit width inductance and capacitance of the line for each conductor. According to the specifications of the fabricated HEMT, the phase velocities on the gate and drain lines have a 20% mismatch. This is mainly due to the large value of the gate-source capacitance which is a result of having a wider depletion region in the vicinity of the gate electrode and, accordingly, reduction of the phase velocity of the gate signal.

5.6 Solution for high-frequency operability

As already discussed in the previous section, a phase velocity mismatch is an indication of observable wave propagation effects inside the device. Fig. 5.8 shows the output power of the fabricated HEMT over a broad frequency band. Obviously, the nonlinear relation is observed due to the creation of partial standing waves at higher operating frequencies. The dashed line in this figure shows the results for a case where the wave propagation effects are compensated. It is worth noting that for the normal case, the dispersion of the transconductance is not considered in the model as our main goal is to show the effects of the mismatch in the phase velocity of the input and output conductors. By removing these effects, the device performance, which is demonstrated by the blue line, will be improved to be in the shaded yellow section and the maximum improvement (fully linear performance) is depicted by the dashed red line.

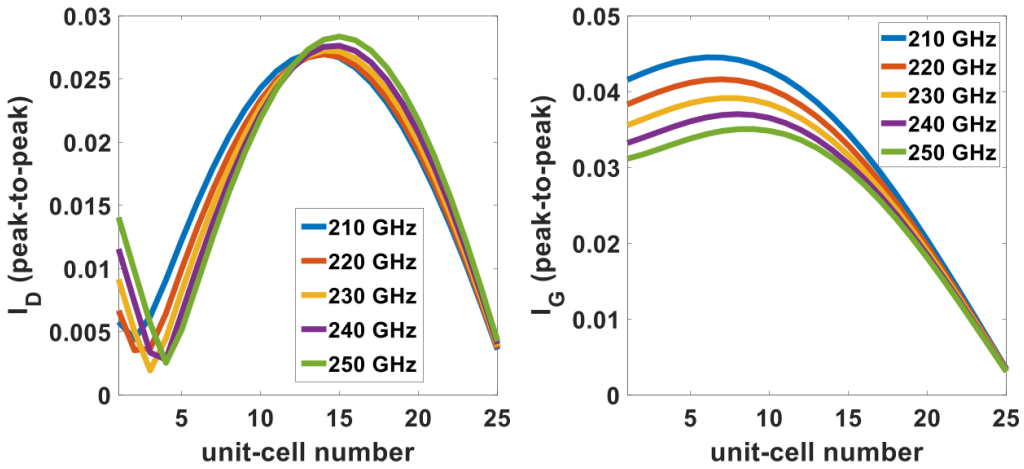

Fig. 5.7 Gate and drain currents along the device width for five different operating frequencies (partial standing wave behavior).

This compensation is performed based on the configuration of the device model. C_{GSi} (intrinsic gate-source capacitance) is the limiting element which suppresses the phase velocity of the gate electrode. As the intrinsic section of the device is a representative of the semiconductor

layer structure of the device, the overall behavior of the device may change by altering this section. Therefore, the solution lies in the values for extrinsic section, where the inductance and/or capacitance of the drain electrode (C_{DSe} and L_{De}) can be increased and adjusted in a way that the phase velocity on the drain line becomes almost equal to that of the gate line [23]. In other words, the mismatch is imposed by the intrinsic features of the device and optimized electrode design alleviates this limitation.

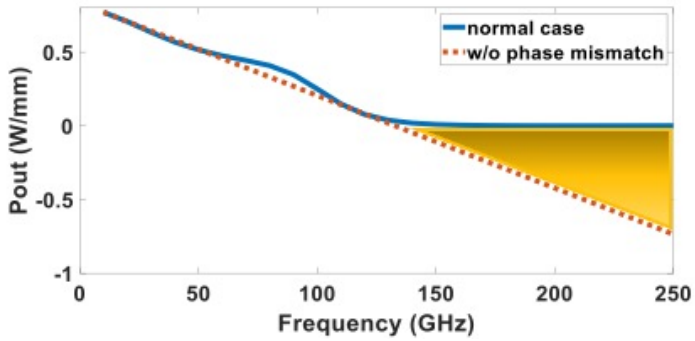

Fig. 5.8 Output power of the HEMT device over 10-250 GHz frequency band.

Fig. 5.9 shows a schematic of how the drain electrode is configured to compensate for the phase velocity mismatch. This layout arrangement suggests a defined repeating pattern in order to steer the electromagnetic signals inside the device. The air gaps in the structure of the drain conductor force an extra capacitance to the overall value, which serves as the velocity adjustment tool on the drain electrode. The modified configuration is implemented in the configuration of a HEMT device. The typical device demonstrates a 43% phase velocity mismatch between the input and output electrodes, with a current gain of 3.85 dB at 60 GHz. However, the modified HEMT configuration, where the phase velocity mismatch is eliminated, provides a current gain of 8.86 dB at the same operating frequency. Clearly, the proposed configuration results in a 130% increase in the gain of the device.

5.7 Conclusion

In millimeter-wave devices, the electromagnetic-wave propagation effect is a phenomenon that must be taken into account in the device design. The simplest definition for this effect is the interaction of the signals on the input and output electrodes. This happens mainly due to the phase velocity mismatch between the gate and drain electrodes, which becomes prominent when the operating frequency increases beyond a certain point, where the wavelength of the propagating signal inside the device and the device physical width become comparable. Hence, the device width is kept at very small values for high-frequency operations to avoid any degradations of the device output. However, a narrower device results in a reduced gain. A solution for making today's devices to be capable of operating at higher frequency bands must compensate for the phase mismatch between the input and output conductors. This is mainly performed by focusing on the extrinsic device parameters to maintain equal phase velocities on the input and output electrodes.

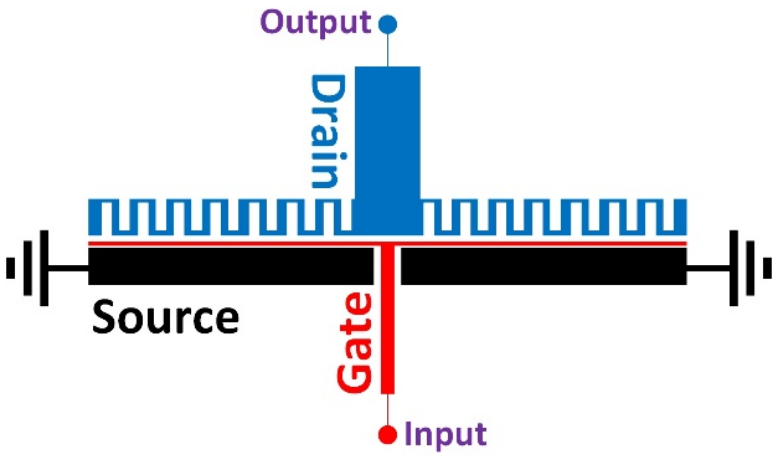

Fig. 5.9 Redesigned drain for removing the phase mismatch between the input and output.

5.8 References

[1] B. Romanczyk *et al*., "N-polar GaN-on-Sapphire deep recess HEMTs with high W-band power density," *IEEE Electron Device Lett.*, vol. 41, no. 11, pp. 1633-1636, Nov. 2020.

[2] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764-1783, June 2012.

[3] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "3–3.6-GHz wideband GaN doherty power amplifier exploiting output compensation stages," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2543-2548, Aug. 2012.

[4] P. Shrestha *et al*., "High linearity and high gain performance of N-polar GaN MIS-HEMT at 30 GHz," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 681-684, May 2020.

[5] K. J. Chen *et al*., "GaN-on-Si power technology: devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779-795, Mar. 2017.

[6] A. G. Avval, E. Larique and S. M. El-Ghazaly, "Heterojunction field effect transistors," *Reference Module in Materials Science and Materials Engineering*, 2018.

[7] G. Crupi and D. Schreurs, *Microwave De-Embedding: From Theory to Applications*, New York, NY, USA:Academic, 2013.

[8] R. J. Trew, "A zone-based approach for physics-based FET compact models," *2016 21st Int. Conf. on Microw. Radar and Wireless Commun. (MIKON)*, pp. 1-4, 2016.

[9] S. Nouri and S. M. El-Ghazaly, "Comprehensive physics-based model for millimeter-wave transistors," *IEEE Radio and Wireless Symp. (RWS)*, San Diego, CA, USA, 2021, pp. 29-31.

[10] S. Nouri, A. G. Avval and S. M. El-Ghazaly, "Effects of pad layout variations on the cut-off frequency of millimeter-wave transistors," *2021 IEEE Texas Symp. on Wireless and Microwave Circuits and Systems (WMCS)*, 2021.

[11] H. Hamada *et al*., "300-GHz 120-Gb/s wireless transceiver with high-output-power and high-gain power amplifier based on 80-nm InP-HEMT technology," *2019 IEEE BiCMOS Compound semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nashville, TN, USA, 2019, pp. 1-4.

[12] J. M. Schellenberg, "A 2-W W-band GaN traveling-wave amplifier with 25-GHz bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2833-2840, Sept. 2015.

[13] S. Nouri, A. G. Avval, and S. M. El-Ghazaly, "Impact of wave propagations on figures of merit in millimeter-wave transistors," *IEEE MTT-S International Microwave Symp. (IMS)*, Atlanta, GA, USA, 2021. (to be published)

[14] M. Ćwikliński *et al*., "D-band and G-band high-performance GaN power amplifier MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5080-5089, Dec. 2019.

[15] Fung et al., "Gallium nitride amplifiers beyond W-band," *IEEE Radio and Wireless Symp. (RWS)*, pp. 150-153, Jan. 2018.

[16] W. Heinrich, "Distributed equivalent-circuit model for traveling-wave FET design," *IEEE Trans. Microw. Theory Techn*, vol. 35, no. 5, pp. 487-491, May 1987.

[17] A. G. Avval and S. M. El-Ghazaly, "A new small-signal modelling approach for analyzing HEMTs over a broad frequency range," *2019 IEEE 62nd Int. Midwest Symp. on Circuits and Syst. (MWSCAS)*, pp. 706-709, 2019.

[18] X. Zheng et al., "N-polar GaN MIS-HEMTs on sapphire with high combination of power gain cutoff frequency and three-terminal breakdown voltage," *IEEE Electron Device Lett*, vol. 37, no. 1, pp. 77-80, Jan. 2016.

[19] M. Guidry et al., "Small-signal model extraction of mm-wave N-polar GaN MISHEMT exhibiting record performance: analysis of gain and validation by 94 GHz loadpull," *2016 IEEE MTT-S Int. Microw. Symp. (IMS)*, pp. 1-4, 2016.

[20] A. G. Avval and S. M. El-Ghazaly, "Distributed-model-based approach for electrical and thermal analysis of high-frequency GaN HEMTs," *IEEE Access*, vol. 8, pp. 152333-152341, 2020.

[21] S. B. Cohn, "Thickness corrections for capacitive obstacles and strip conductors," *IRE Trans. Microw. Theory Techn*, vol. 8, no. 6, pp. 638-644, Nov. 1960.

[22] X. Zheng et al., "High frequency N-polar GaN planar MIS-HEMTs on sapphire with high breakdown and low dispersion," *2016 Lester Eastman Conf. (LEC)*, pp. 42-45, 2016.

[23] A. G. Avval and S. M. El-Ghazaly, "Distributed-model-based design approach for achieving matched phase velocities in high-frequency GaN HEMTs," *2020 IEEE 63rd Int. Midwest Symp. on Circuits and Syst. (MWSCAS)*, Springfield, MA, USA, 2020, pp. 545-548.

Chapter 6

Conclusion and future work

6.1 Conclusion

A novel modeling approach was developed in this research which is mainly utilized for transistors operating in mm-wave range frequency bands. Chapter 2 started with presenting some background information about transistors, in general, and different types of these devices utilized in various applications. It was also explained how the physical structure of devices determines their operating modes. Also, different semiconductor materials employed in fabricating these transistors were introduced along with their electrical and thermal properties. From this point, the dissertation was mainly focused on GaN HEMT devices as the favorable components for high-frequency and high-power applications. The characteristics of HEMT devices were then discussed and the regions of the device structure that were associated with the passive and active sections were explained. Additionally, the energy band diagram of a typical HEMT structure before and after contact formation was described.

Different contact types were also discussed in this chapter, and it was explained how and why the gate is a Schottky contact, but the two other conductors, namely drain and source, have an ohmic contact with the semiconductor layer. Next, the general fabrication procedure of these devices was elaborated, recent HEMT designs were introduced, and the N-polar and Ga-polar devices were demonstrated. After providing some introductory materials related to the device structure, different modeling approaches utilized for analyzing these devices were presented and the small-signal and large-signal schemes were introduced. The main limitations of these modeling approaches were also discussed in this section, and it was explained how the current solutions for addressing these limitations are computationally expensive. Finally, the motivations for this research along with the objectives to be achieved were discussed.

Chapter 3 discussed the modeling approach proposed for analyzing the thermal behavior of transistors, and, more specifically, transistor substrates. First, different types of semiconductor materials utilized in transistor substrates were introduced and limitations of these platforms were discussed. A simulation was conducted on a sapphire substrate in COSMOL Multiphysics and the temperature distribution inside this substrate was presented while operating. Thinning the substrate was the initial step in developing the technique for improving the heat dissipation capabilities of the platforms. The simulation was conducted on the thinner substrate and the mathematical analysis for finding the thermal resistance of the substrates under test proved the claims. The actual proposed approach started with defining the conductive heat flow in a solid and the truncated cone etched into the back of the substrate was identified as the solution for increasing the thermal conductivity of the substrate.

Rigorous simulations were then conducted on the normal substrate configuration and the proposed new design in order to ensure the validity and efficiency of the technique. Different substrate thicknesses, cone heights, and applied power values were tested on silicon, sapphire, and silicon carbide as the three main platforms utilized in high-frequency devices and circuits. The proposed method yielded promising results for all the cases, where the improvement for the sapphire substrate was 288% and for the silicon carbide was 101%. Also, cone height was introduced as one of the main factors in determining the efficiency of the method. Different applications of the novel approach along with fabrication procedures were also discussed in this chapter.

The small-signal modeling approach and the device analysis in the linear region was discussed in Chapter 4. First, a thorough literature review of the available methods was presented and the limitations with these approaches were explicitly discussed. Wave propagation effects as

one of the main phenomena in high-frequency regions were discussed and it was explained how important it is to incorporate it in both device fabrication and modeling. The details of the device configuration, which was used for the analysis and validation purposes, were presented and the equivalent circuit model was described. The extraction procedure for the capacitance, inductance, conductance, and resistance of the extrinsic and intrinsic sections in the developed model was explained, which was solely based on the physical structure of the device and simulation results.

Next, the distributed approach was introduced as one of the main contributions of the conducted research on this topic. It was also mentioned how the distributed model can take into account the effects of wave propagation in the analysis. The governing equations for analyzing the device were described and the finite-difference scheme in time-domain was utilized. Current gain and maximum available gain parameters were obtained for the presented device and the simulation results were compared with the measurements for validation purposes, where the excellent agreement proved the claims. The S-parameter values over a wide frequency range were also obtained. Additionally, to demonstrate why it is important to incorporate the distributed effects in the modeling process, the model was applied to a hypothetical wider device over a higher frequency band and the results were compared.

The heat distribution effects were presented in this chapter as well. A power was applied to the active region representing the different phenomena in the vicinity of the gate electrode that causes the generation of internal heat. Then, the temperature distribution was analyzed inside the semiconductor layers, along the device width, and the transistor substrate by looking into multiple cutlines. The obtained results clearly demonstrated that the heat distribution studies must be considered when a circuit model is developed for a transistor device operating at the

mentioned frequency bands and how the distributed model is capable of taking these effects into account.

All the technical materials related to the nonlinear device modeling and a new transistor configuration compensating for the phase cancellations was presented in Chapter 5. This chapter started with further elaborating on the wave propagation effects and phase mismatch in higher frequency bands. Next, another device structure was introduced and its structural details along with the developed circuit model and the obtained parameter values were presented. Before going into the nonlinear regions, the small-signal model, developed in Chapter 4, was applied to this device and promising results were achieved. The output power and gain of the device associated with the large-signal analysis were also demonstrated to show the validity of the nonlinear model. The high-frequency operability limitations were discussed in the last section and a solution pertaining to equalizing the phase velocity of the signals on the gate and drain electrodes was proposed.

6.2 Future work

The research conducted here can be extended by integrating the introduced modeling approaches. The developed distributed modeling approach, as explained in Chapter 5, is capable of analyzing the device in the linear and nonlinear regions and the large-signal scheme has the small-signal tool included. The developed tool for analyzing the thermal behavior of the transistor can also be merged with the electrical model to provide a more comprehensive tool. Moreover, despite the fact that the distributed model and the proposed extraction techniques are independent of the device configuration and structure, the main focus of the present research was on the GaN HEMT devices. Hence, some minor tuning and optimization may be required when

utilizing the technique for analyzing other transistor types. The obtained model including the mentioned information can then be utilized as a software platform capable of analyzing different transistor types operating at higher frequency bands.