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Analysis of Multi Resonant Switched Capacitive Converter with Imbedded PCB Elements

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ANALYSIS OF MULTI RESONANT SWITCHED CAPACITIVE CONVERTER WITH IMBEDDED PCB ELEMENTS

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ABSTRACT

ANALYSIS OF MULTI RESONANT SWITCHED CAPACITIVE CONVERTER WITH IMBEDDED PCB ELEMENTS

by Adel Lahham

The data center industry is headed towards a lower point of load voltages with increased load demands contributing to higher I^2R losses in power busses. Raising the bus voltage from 12V to 48V is a popular area investigated today for reducing power delivery losses. Switched capacitive converters (SCCs) are a popular topology used for this purpose. However, SCCs suffer from low tolerance for operating conditions and are unregulated. The proposed multi resonant switched capacitor buck converter (MRSCBC) can resolve these challenges while also providing output regulation. Switch mode power supplies exhibit high electromagnetic noise and with an increased number of switches in an MRSCBC, controlling EMI noise and compatibility is essential. This thesis will focus on the use of PCB design and software simulations to optimize electromagnetic interference (EMI) and parasitic elements in the traces to improve the robustness of an MRSCBC.

ACKNOWLEDGMENTS

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This thesis was completed during the coronavirus pandemic and the economic collapse of my home country of Lebanon. Acknowledgements go to the family and friends whose support allowed me to complete my degree and graduate. My success in completing my graduate degree is the success of their efforts.

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List of Abbreviations

POL – Point of Load
VR – Voltage Regulator
PSU – Power Supply Unit
IBC – Intermediate Bus Converter
COMPDA – Composite Modular Power Delivery Architecture
ZVS – Zero Voltage Switching
ZCS – Zero Current Switching
MRSCBC – Multi Resonant Switched Capacitive Buck Converter
MRSCC – Multi Resonant Switched Capacitive Converter
EMI – Electromagnetic Interference
SMPS – Switch Mode Power Supply
GaN – Gallium Nitride

1 INTRODUCTION

1.1 Switch Mode Power Supplies

DC-DC converters are a type of power electronic circuits which are used as power supplies. The converters achieve voltage transformation using electrical elements such as mosfets and often inductors. Buck converters are a popular and simple example for step-down voltage transformation using an inductor. In boost converters, however, the inductor is charged during off time and then discharged with the supply to produce a higher voltage on its output. Fig. 1 showcases an example of the DC-DC converter. Inside Fig.1 is the schematic of a boost converter where L is the inductor, Q is the switching element, D is the diode, and C is the output capacitor.

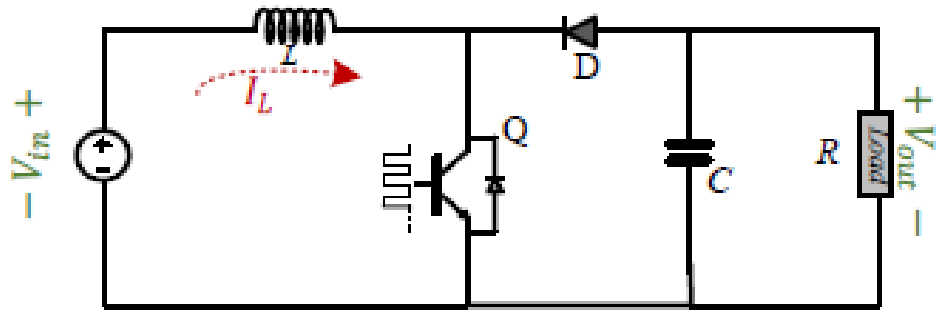

Fig. 1. Boost converter schematic.

When operating as power supplies, DC-DC converters are called switch-mode power supplies (SMPS) often used to power consumer electronics. The switching elements have typically been Mosfets using silicon technology. The popularity of silicon is due to the mature technology process and cheaper cost compared to other technologies such as gallium nitride. Power adapters are a popular example of SMPS which usually utilize flyback converters.

When operating, switch-mode power supplies have multiple parameters surrounding their operation. The switching element, usually a mosfet, is primarily responsible for the transformation ratio of the voltage between its input and output. The duty cycle of the switching controls energy flow duration and direction in a SMPS. The inductor has a complex role that differs depending on the converter topology. Some topologies do not use a discrete inductor. Flyback, forward, and push-pull converters rely on leakage inductances inside their isolation transformers. Commonly, the inductance value is responsible for the ripple current value across it which can change a converter's mode of operation between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Finally, the output capacitance maintains a constant output voltage. The capacitance value is responsible for the voltage ripple on its output. Parasitic capacitances and inductances exist; however, their scope remains outside this thesis. Eqns. 1 and 2 are the equations for current ripple proportionality to inductance and voltage ripple proportionality to capacitance, respectively.

Equation 1. Inductance to current ripple proportionality

$$L = V \times \frac{di}{dt} \qquad (1)$$

Equation 2. Capacitance to voltage change proportionality

$$I = C\frac{dv}{dt} \qquad (2)$$

Two important design considerations for a SMPS are the addition of multi-phase operation and output voltage regulations. The multi-phase design offers advantages in the form of smaller inductors for resonant circuits as in Fig. 2, and improved voltage

overshoot during transients as in Fig. 3 [1]. Multi-phase designs, however, do suffer from susceptibility to circulating current as shown in Fig. 4 [1].

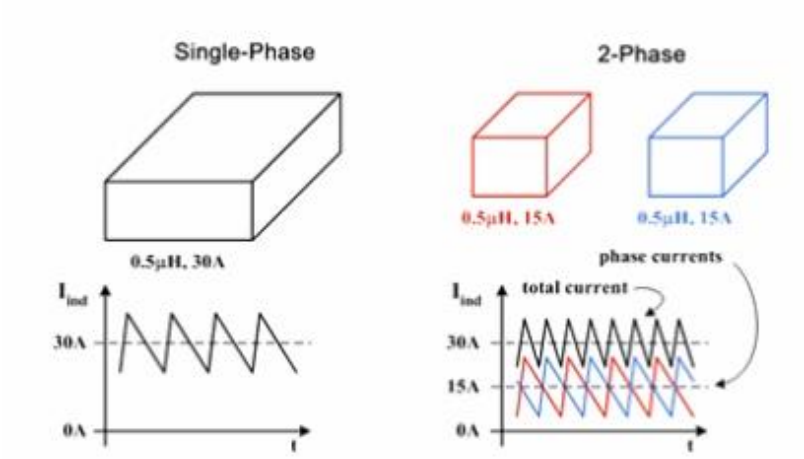

Fig. 2. Comparison of inductor size and current for single and two-phase systems [1].

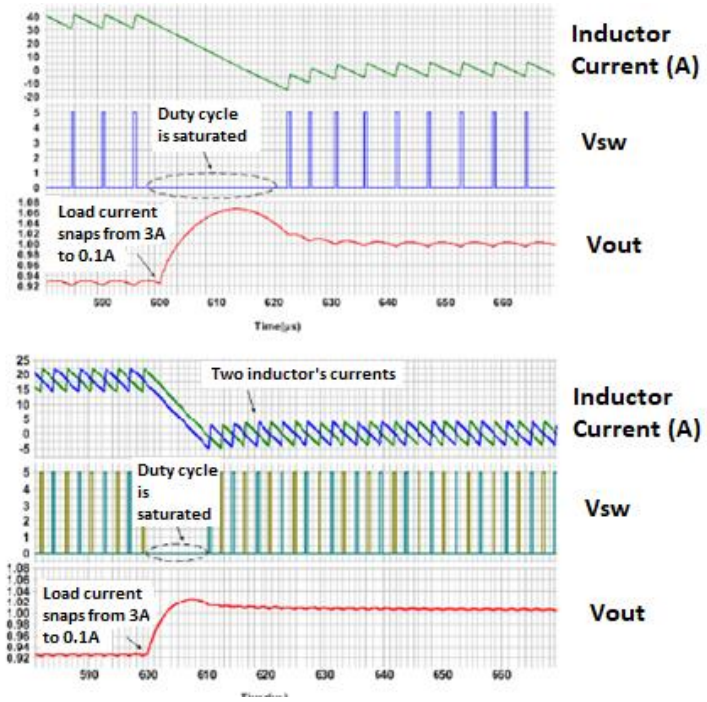

Fig. 3. Voltage overshoot comparison of single and multi-phase systems [1].

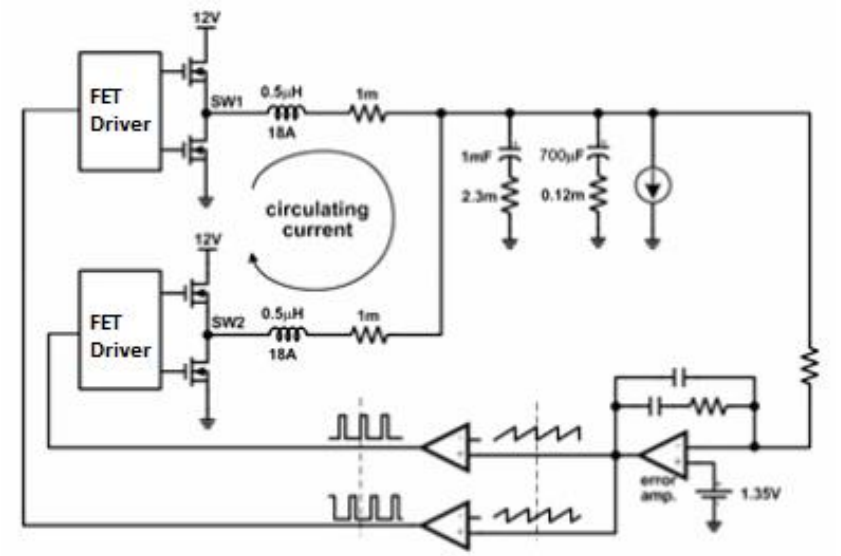

Fig. 4. Example of circulating current in multi-phase systems [1].

There are three types of voltage regulation schemes that exist which are fixed ratio, semi-regulated, and fully regulated converter outputs [2]. In a fixed ratio SMPS, the output voltage is not regulated and changes with any input voltage perturbation. This type of converter operates with a wide output voltage range and a small input voltage range [2]. The semi-regulated SMPS offers partial regulation which is an improvement over nonregulated outputs. The output voltage is regulated based on perturbation to the input voltage. The input voltage of the semi-regulated converter can maintain a wide range, while output voltage maintains a smaller range relative to the input [2]. The last regulation scheme is the fully regulated converter. The output voltage is regulated into a fixed value regardless of perturbations on the input while output perturbations are canceled. The fully regulated converter can handle a large input voltage range [2]. Fig. 5 depicts the three regulation schemes as well as the input and output voltage range of each.

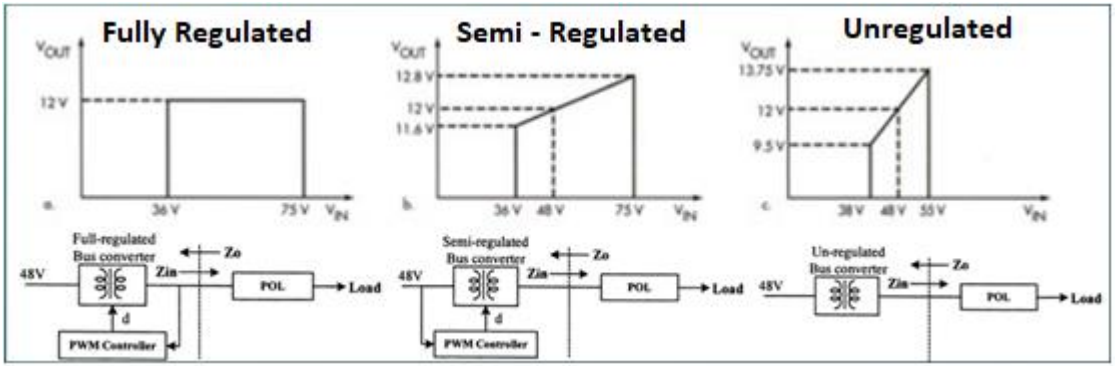

Fig. 5. Visual comparison of three voltage regulation techniques [2].

Another concert affecting regulation choice is stability. Regulation instability refers to the presence of voltage oscillations during operation [2]. A regulator which is designed to be stable in standalone operation may show oscillatory and unstable behavior once connected to a load [2]. Instability in operation is due to overlap in the converter output impedance and load input impedance [2]. The presence of impedance overlap, shown in Fig. 6, triggers instability for output voltage [2].

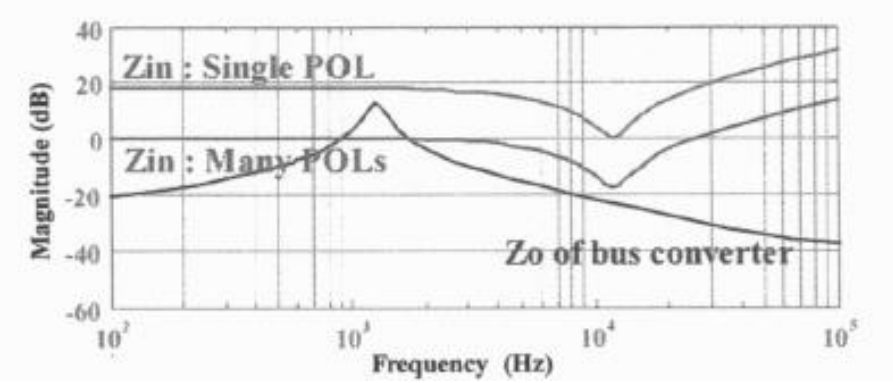

Fig. 6. Condition for instability [2].

If the number of parallel loads connected to the converter is high, then their input impedance could become lower than the converter's output impedance. Both non-regulated and semi-regulated control topologies suffer from this issue while fully regulated converters do not [2]. Due to the higher bandwidth in fully regulated control,

the peak impedance is lowered and no overlap between the output and input impedance occurs. Fig. 7 displays a comparison between stable converter output voltage and unstable converter voltage oscillations.

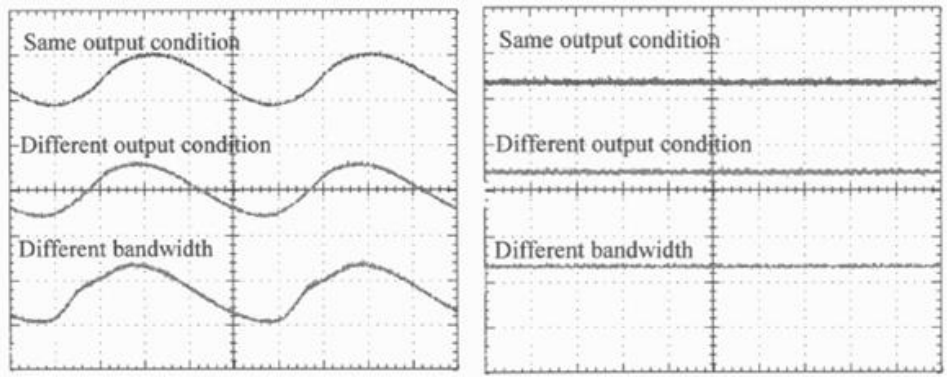

Fig. 7. Comparison of unstable (left) and stable (right) output voltages [2].

Further analysis of the bode plots shows that when the output impedance of the converter exceeds the low-frequency input impedance of its load then operation slides into unstable regions [3]. This behavior is observed through a nyquist plot. Stable operation observers no clockwise encirclements of the (-1,0) point which is the critical point for stability [3]. Since the nyquist plot flows in a clockwise direction, if it does encircle the critical point then the system becomes unstable. When the output impedance of the converter is equal to the low-frequency input impedance of the load connected, we observe marginal stability as in Fig. 8 [3].

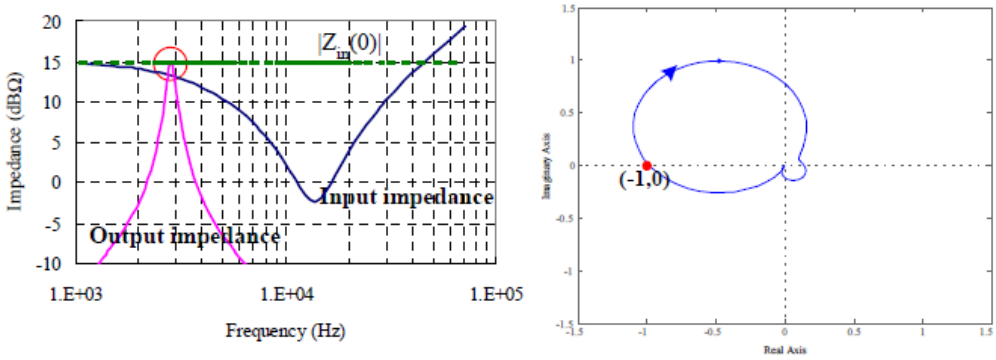

Fig. 8. Depiction of critical condition on bode plot (left) and nyquist plot (right) [3].

There exist solutions to maintain a stable output for each regulation mode. In fixed-ratio converters the output capacitance can be increased [3]. In high power and energy dense application this is impractical due to the large number of capacitors required. Reducing the inductor size and increasing the duty cycle is another solution which improves system stability. For semi-regulated operation, however, the duty cycle is variant, and as a result, the only way to improve output stability is by utilizing larger output capacitances [3].

1.2 Resonant Converters

A variation of DC-DC converters is resonant converters. Resonant converters are favorable for high-power applications. One popular topology is the LLC resonant converters. LLC converters hold a multitude of benefits that are advantageous in high-power applications. LLC converters benefit from high power density and high efficiency which are important for high power [4]. Zero voltage switching (ZVS) and zero current switching (ZCS) is another benefit to the LLC topology which allows to reduce switching losses [5]. Fig. 9 presents the schematic of an LLC converter and highlights the LLC tank.

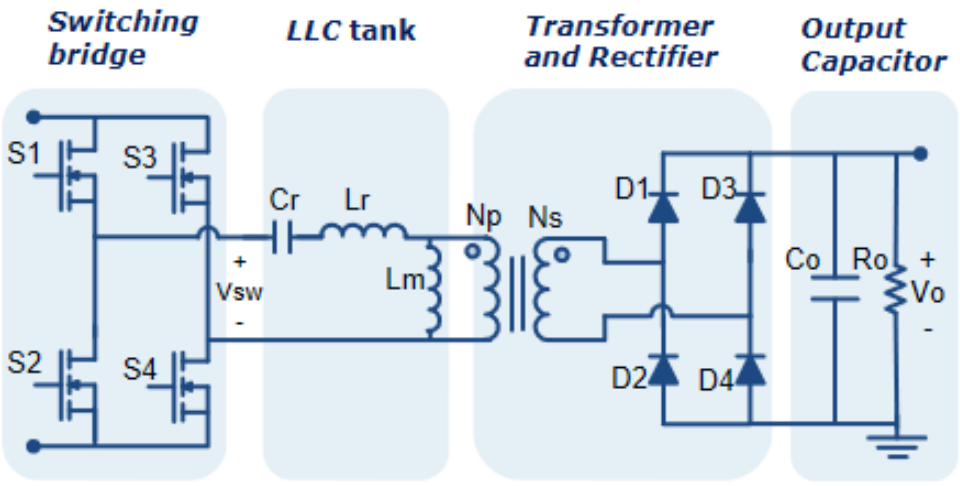

Fig. 9. LLC converter schematic [5].

1.3 Gallium Nitride

A new technology popularizing in the power electronics and SMPS industry is gallium nitride (GaN). GaN is used for wide-bandgap semiconductors that are implemented in transistors and integrated analog circuits. GaN offers improved efficiency, improved switching speeds, and higher breakdown voltages [6]. When implemented, GaN can reduce the size footprint of a package while maintaining the same power and voltage breakdown capabilities or allow for higher capabilities using the same size package. GaN technology does suffer from some drawbacks. Parasitic inductance inside traces leading to a GaN transistor can cause issues such as ringing and increased EMI. As a result, strong efforts are needed when designing a layout for a GaN switching circuit [7]. The improvements and popularity of GaN are a cause to include it in any analysis of a new DC-DC converter topology. The industry is currently shifting towards GaN and companies such as Power Integrations are designing their own GaN implementations called “PowiGaN” [8]. Fig. 10 presents the improved switching and power capabilities of GaN compared to traditional silicon transistors. Fig 11. showcases the voltage and on-

resistance (Rdson) improvements of GaN transistor over traditional silicon-based transistors.

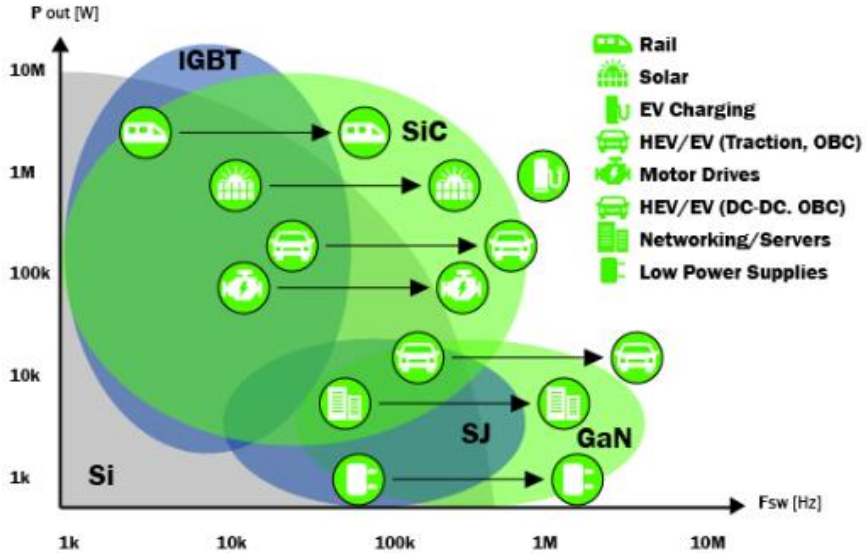

Fig. 10. Silicon to GaN transition with capabilities improvements [9].

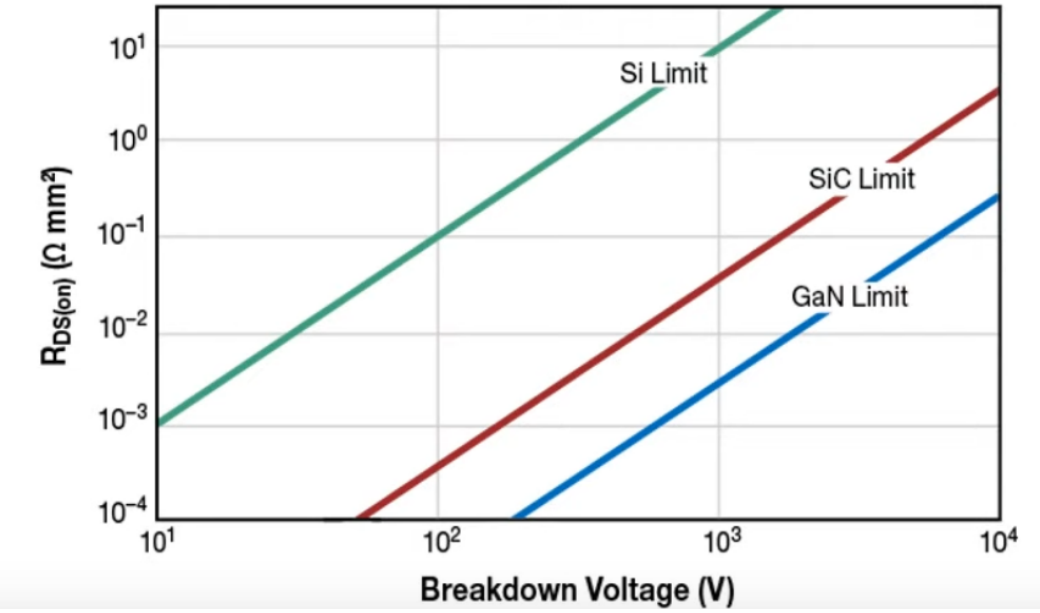

Fig. 11. Voltage and Rdson improvements of GaN compared to silicon (Si) [10].

2 LITERATURE REVIEW

2.1 Data Centers

Data centers, which consume 2% of total power usage in the US, can improve their energy consumption by reducing their conduction losses [11]. Data center racks can be rated up to 15kW where each rack contains up to 220A rated current at point of load voltages of 1.85kW [12]. Raising the DC bus voltage of data centers to 48V diminishes distribution losses and is a popular area of industry research [13]. A 48V bus converter is located between the power supply unit (PSU) and the 12V servers in two-staged architectures as illustrated in Fig. 12 [14]

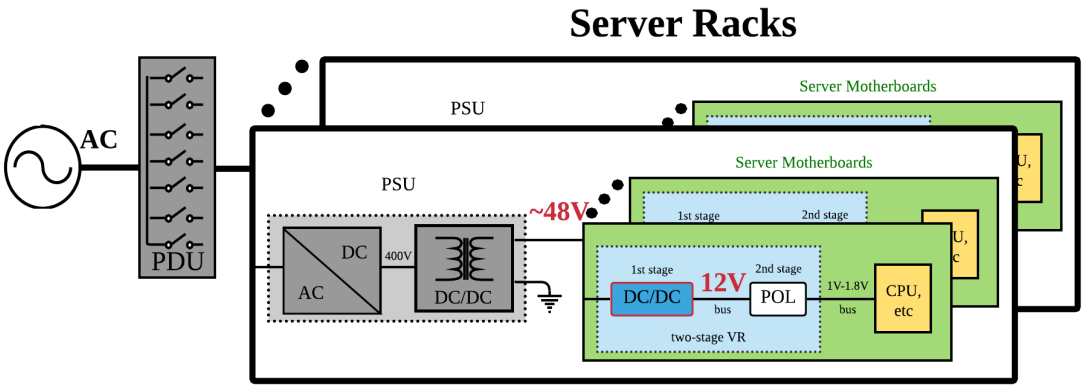

Fig. 12. Google's two staged architecture [13].

2.2 Intermediate Bus Converter

The design of intermediate bus converters (IBC) has high demands and limitations for two-staged regulator structures. The data center market is competitive where power density and efficiency are a design priority [15]. The market for 48V to 12V IBC contains a variety of power converter topologies. A non-isolated fixed-ratio DC/DC converter by Vicor Power steps down a 48V input voltage to 12V through a high-frequency LC tank

converter with an efficiency up to 97.9% and power density reaching 4.5kW/in^3 [16]. Another different topology is a composite modular power delivery architecture (COMPDA) based switched-tank converter (STC) which was presented by the State University of North Dakota [14]. Fig. 13 showcases the COMPDA architecture.

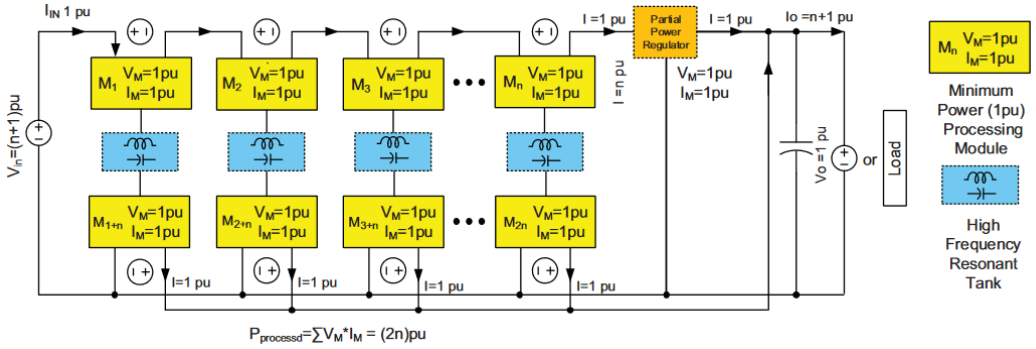

Fig. 13. Composite modular power delivery architecture (COMPDA) [14].

The COMPDA achieves zero voltage switching (ZVS) and zero current switching (ZCS) which maintains low voltage stress for all the components and utilizes a smaller power delivery module. The efficiency reaches 98.55% peak efficiency and a 750W/inch^3 power density. These converter topologies, however, lack voltage regulation on their 12V output.

2.3 Proposed Converter

Resonant converters are a popular area of research [15]. A regulated two-staged multi-resonant multi-phased switched-capacitor-buck converter (MRSCBC) is in the research phase at San Jose State University, and it achieves high efficiency and power density for the two-staged VR structure while regulating the 12V output. Research simulation results suggested efficiency numbers up to 98% at 1.5kW, as depicted in Table 1. The MRSCBC is made up of two cascaded converters. The first is a multi-resonant switched-capacitor

converter (MRSCC) which halves the input voltage by a fixed ratio. The second cascaded stage of the converter is a synchronous buck converter that can step down the input voltage to a regulated 12V output using peak current-mode control for equal current sharing of the multi-phases used in the design. There is potential for the MRSCBC converter to be competitive in the data center market.

Table 1. Efficiency of Converter for Four Phased Interleaved MRSCBC.

Input Power	Output Power	Efficiency	Dissipated Power
1.5224kW	1.49813kW	98.41%	24.266W

3 MULTI RESONANT SWITCH CAPACITIVE BUCK CONVERTER (MRSCBC)

3.1 MRSCBC Operation

The MRSCBC consists of an MRSCC which is cascaded by a buck converter on its output to provide regulation. Fig. 14 showcases the MRSCBC schematic.

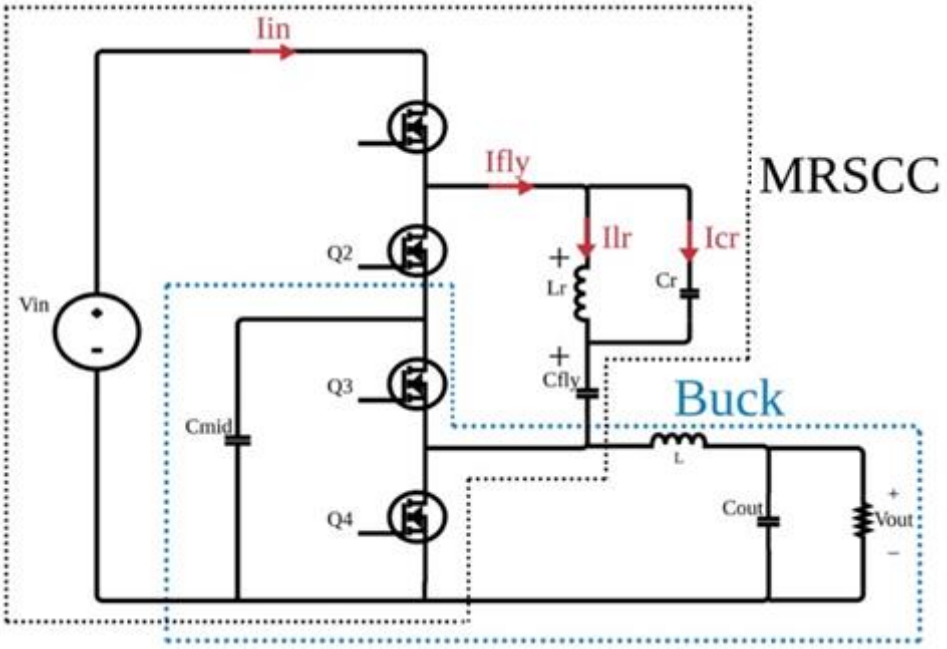

Fig. 14. Schematic of MRSCBC in research.

The MRSCC is characterized by high efficiency and power density but remains unable to regulate its output due to fixed ratio conversion [16]. A small inductor L_r placed in series with the fly capacitor C_{fly} prevents hard charging and eliminates high conduction losses. The inductor L_r with capacitor C_{fly} function as a resonant tank to control the charging current at a resonant frequency f_o. However, it is difficult to match the resonant tank frequency to the switching frequency due to components values' variations. Class I capacitors, recommended for resonant capacitors, keep resonant frequencies fixed with

respect to bias voltages. Class I capacitors have, however, part to part variation of 20% at worst case [17]. To prevent negative inductor current turn-off in the resonant tank and increase immunity to component variation due to resonant and switching frequency mismatch, the switching frequency f_{sw} is selected higher than the nominal resonant frequency f_o [17]. To handle inductor discharging, a capacitor C_r much smaller than C_{fly} forms a second high frequency resonant tank with the inductor to discharge the current in a controlled manner during the deadtime t_d [17]. With higher switching frequency which increases immunity to component variation, the use of class II capacitors is allowed for C_{fly} [17]. C_{fly} needs to be larger than C_r as depicted in Eqn. 3.

Equation 3. Capacitance comparison for stability.

$$C_r < C_{fly} \tag{3}$$

Equation 4. Switching frequency.

$$f_{sw} > f_o = \frac{1}{2\pi\sqrt{L_r C_{fly}}} \tag{4}$$

Equation 5. Deadtime calculation for secondary resonant circuit.

$$t_d = \pi\sqrt{L_r C_r} \tag{5}$$

Eqn. 4 presents the calculation for the resonant frequency f_o and illustrates the switching frequency f_{sw} being higher. Eqn. 5 can be used to size the secondary resonant capacitor C_r.

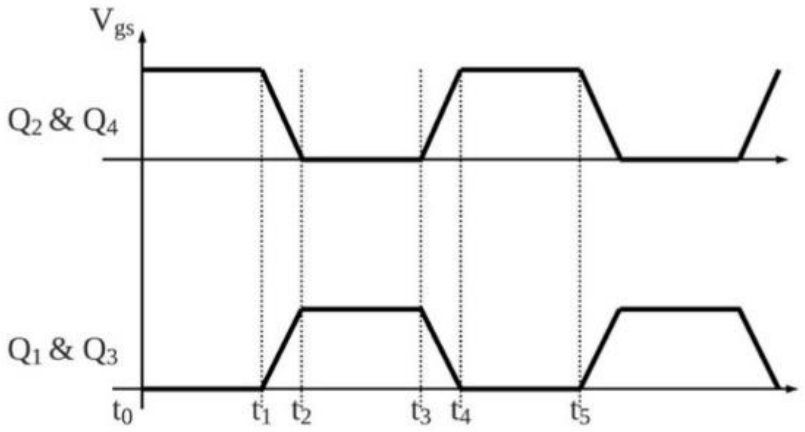

Fig. 15. MRSCBC gate signals.

The MRSCBC operates with two conduction cycles and one dead-time for a total of three switching phases. Fig. 15 depicts these switching phases. The secondary resonant tank L_r and C_r is isolated during the deadtime periods t_1-t_2 and t_3-t_4. During the deadtime, the resonant tank rings, and the current changes to the opposite direction by the time the dead time is over which eliminates voltage spikes from the main switching circuit. Gates Q_2 and Q_4 switch on while Q_1 and Q_3 switch off in periods t_0-t_1. During the mentioned period, the primary resonant tank is parallel with the output, and the flying capacitor C_{fly} transfers its stored energy to the middle capacitor C_{mid} and the output loads. Eqn. 6 calculates the output voltage.

Equation 6. Output voltage equation.

$$V_{out} = V_{Cfly} + V_{Lr} \qquad (6)$$

Gates Q_2 and Q_4 switch off, and Q_1 and Q_3 switch on during the period t_3-t_4. During t_3-t_4 the primary resonant tank and output are in series with the input supply and energy is transferred directly between the input and the output. Eqn. 7 presents the series

KVL equation. The combination of Eqn. 6 and 7 produces Eqn. 8. Observation of the analysis shows how the first stage of the MRSCBC operates as a simple voltage divider that halves the input voltage.

Equation 7. KVL equation during t_3-t_4.

$$-V_{in} + V_{cfly} + V_{Lr} + V_{out} = 0 \quad (7)$$

Equation 8. Voltage transformation ratio.

$$V_{out} \approx \frac{1}{2} V_{in} \quad (8)$$

Equation 9. Minimum buck inductance calculation equation.

$$L_{min} \geq \frac{(1-D)R}{2f_{SW}} \quad (9)$$

Equation 10. Output capacitance calculation equation.

$$C_{out} = \frac{(1-D)}{8L\frac{\Delta V_o}{V_o}{f_{SW}}^2} \quad (10)$$

The buck converter which cascades the MRSCBC runs in continuous conduction mode and minimum buck inductor inductance L_{min} is calculated through Eqn. 9. The parameters of Eqn. 9 are D, R, and f_{sw} which are the duty ratio, load resistance, and switching frequency respectively. Eqn. 10 uses the desired output ripple voltage ΔV_O to calculate the output capacitor's capacitance C_{out} similar to a traditional buck circuit output.

3.2 Four Phase Design

The buck converter stage provides voltage regulation which improves the converter stability. Converter stability can be determined by the overlap between the converter

output impedance and load input impedances [2]. If enough loads are connected in parallel to a converter their input impedance could lower to a value below the output impedance of the converter. In such a situation the converter output voltage begins to oscillate and exits stable operation. [3]. A fully regulated converter benefits from its ability to lower its output impedance through voltage regulation and reduces the chances of falling into unstable operation [2]. Full regulation is achieved through peak current mode control. Peak current-mode control is chosen for its large duty cycle range aiding in regulation stability, and popular use.

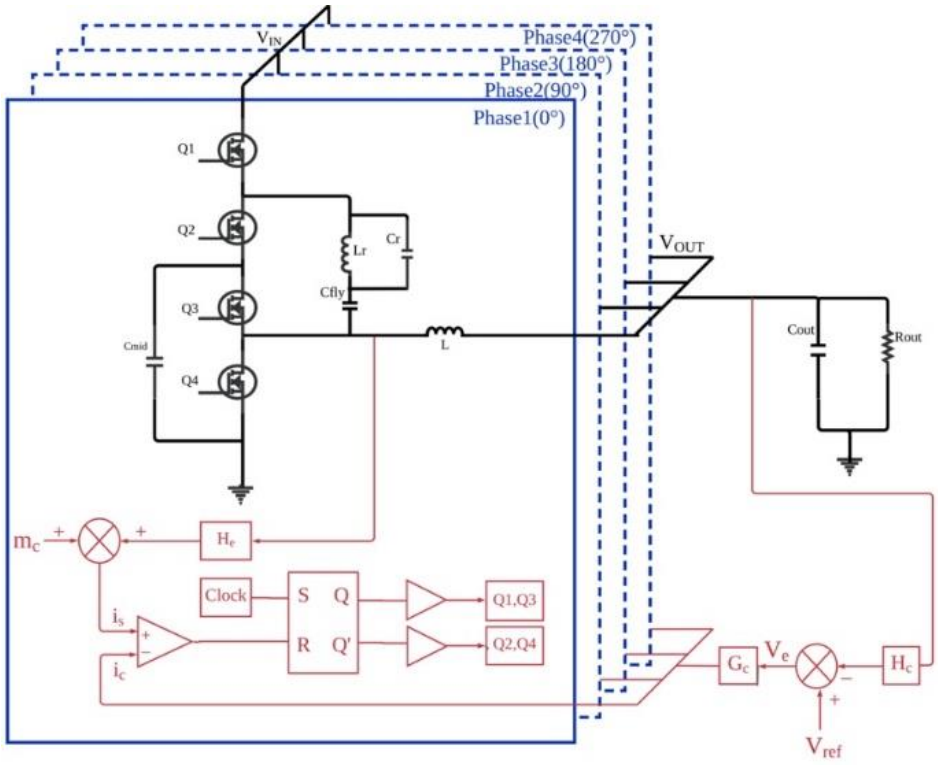

Fig. 16. Four-phased MRSCBC with peak current-mode control.

For large loads, the multi-phase operation is preferred as it keeps inductor sizes small due to current sharing. Balanced current sharing between phases can be achieved through

peak current-mode control. Fig. 16 presents a simplified diagram of four-phased MRSCBC regulated through peak current mode control. Lowering the per-phase current reduces the ripple-current-rating requirement and reduces conduction losses and heat stress for capacitors, mosfets, and inductors in the design which also increases efficiency. Furthermore, the multi-phased design allows for interleaved current on the output which cancels high current ripple values [18]. The main drawback of multi-phased design as expected is the large number of components required as the power and gate drive elements are paralleled for each phase. Table 2 illustrates how many components are used per phase and the current reduction achieved through multi-phased design.

Table 2. Comparison of Phase Numbers for MRSCBC.

Multi-Phased MRSCCB Converter at 1.5kW Output Power				
	Single Phase	Two-Phase	Three Phase	Four Phase
Total # of Inductors	2	4	6	8
Total # of Capacitors	>4	>8	>12	>16
Total # of MOSFETS	4	8	12	16
Current per Phase (A)	125	62.5	41.7	31.25

For the converter design starting with the output and middle capacitors C_o and C_{mid} respectively, Würth Electroniks (WE) X7R ceramic capacitors are chosen with low ESR and ESL which helps control conduction losses and the high-frequency resonance. Ten ceramic capacitors are paralleled for each capacitor. Similar X7R ceramic capacitors are

chosen for the fly capacitor C_{fly} where twelve are paralleled. Infineon BSC032N04LS switches with low on-resistance mosfets are used to also to maintain low conduction losses. The buck converter utilizes an SER2011-202 rated 2µH inductor from Coilcraft which is rated for high peak and RMS current suitable for prototyping. UCC21520 isolated gate drivers safely switch two of the high-voltage power transistors without damaging the control logic circuit in each phase. Table 3. summarizes and continues the power stage's component selection for the design.

Table 3. Component Values for Design.

Components Parameters	Item	Values
Input DC Voltage	V_{in}	48V
Output DC Voltage	V_o	12V
Switching Frequency	f_s	500kHz
Output Current	I_O	125A
Output Power	p_o	1.5kW
Flying Capacitor	C_{fly}	12µF
Middle Capacitor	C_{mid}	100µF
Output Capacitor	C_{out}	100µF
Resonant Capacitor	C_r	1nF
Resonant Inductor	L_r	10nH
Output Inductor	L	22nH
Resistor Load	R_{out}	96mΩ
Deadtime	t_d	10ns

For four phases, each phase's inductor current will be shifted by a 90° phase angle. Interleaving four currents will reduce output ripple as larger ripples get canceled as Fig. 17 illustrates. Peak mode current control as mentioned earlier maintains a balanced current load of $31.2A_{RMS}$ across the four phases. Early simulations show the output current ripple reducing from 200mA to 593µA, and the output voltage ripple from 15mV to 57µV due to interleaving function. While the results are not final, they do illustrate

large gains to be benefited from interleaving. The transient response shows a stable change in voltage in Fig. 18 for a step-change in the output load. Fig. 19 highlights the flying capacitor's sinusoidal current, which suggests soft capacitor charging. As a result, switching losses are reduced in each phase. The efficiency increases when the phase of the MRSCBC converter increases which is shown in Fig. 20.

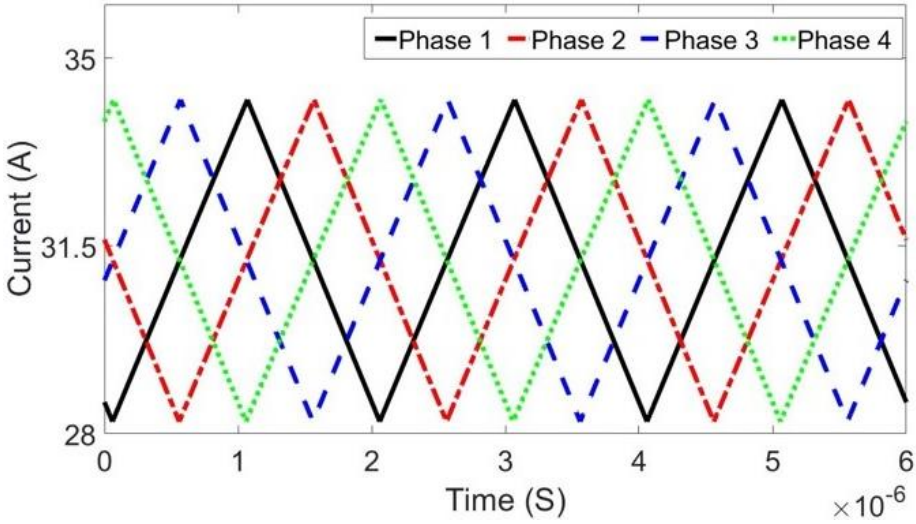

Fig. 17. MRSCBC four phases' interleaving currents.

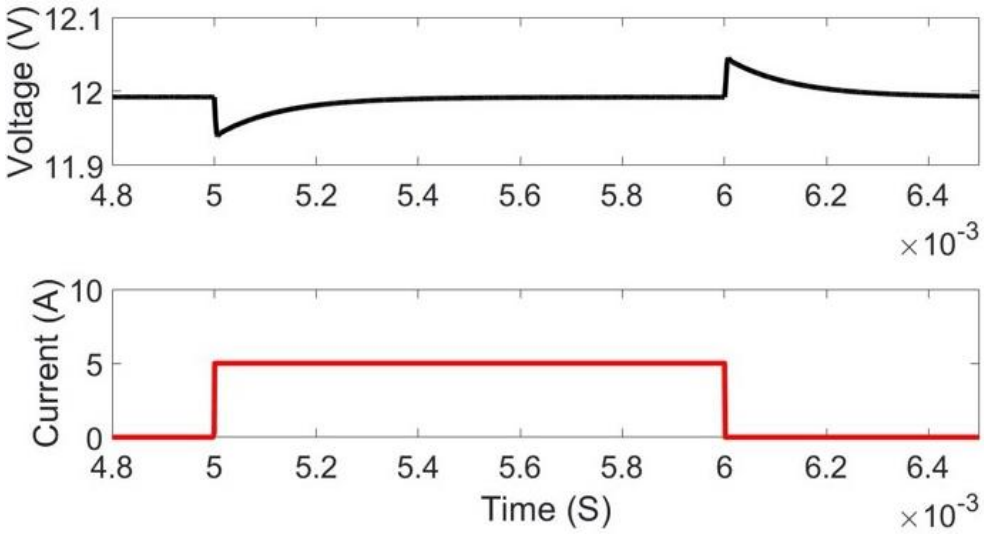

Fig. 18. MRSCBC transient response showing output voltage and output current.

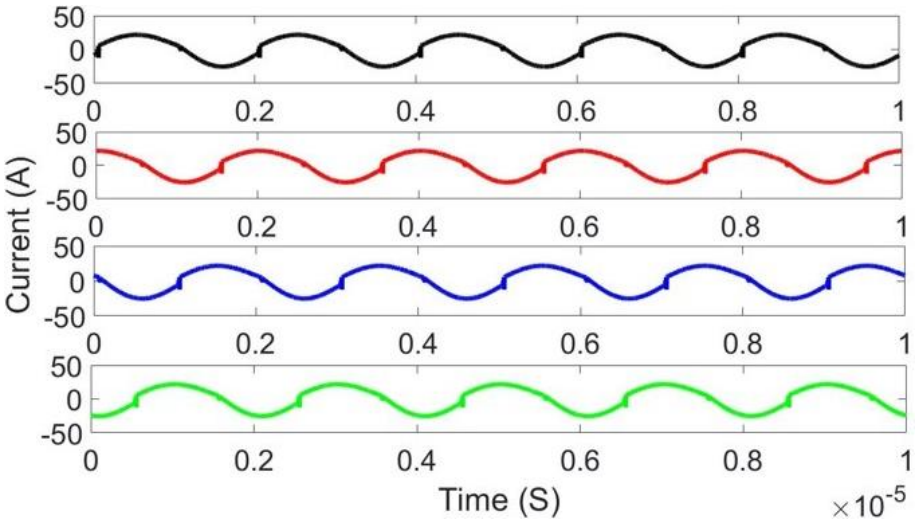

Fig. 19. MRSCBC flying capacitors' currents at full load of 1.5kW.

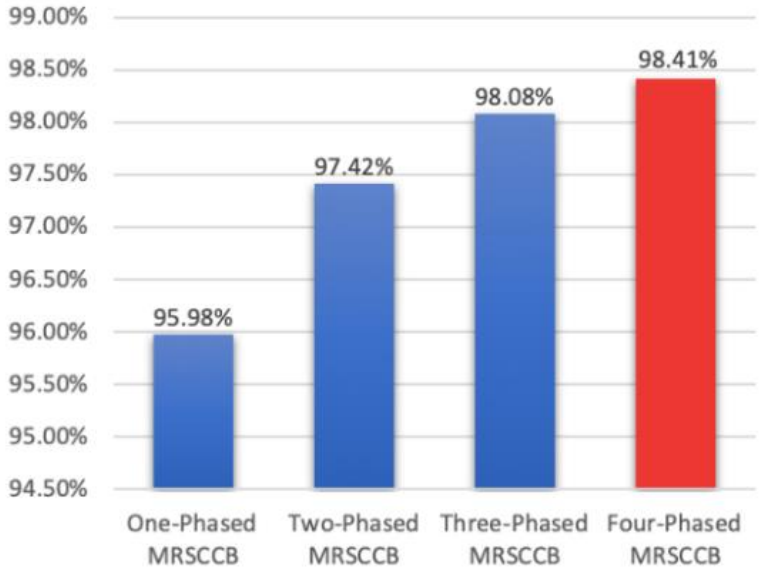

Fig. 20. Efficiency comparison of multi-phased MRSCBC at 1.5kW output power.

3.3 300 kHz Design

It is worthwhile to investigate how the switching frequency affects the MRSCBC. Switching losses and components values change with the switching frequency. The four-phase MRSCBC is recreated in Cadence Capture with 300kHz. Fig. 21 highlights experimental results that study immunity towards components variation. When the fly

capacitor current is higher, then the capacitor charging, and resonant operation of the power circuit is less ideal. Compared to the RSCC, the MRSCC has high immunity towards the flying capacitor's variation when the switching frequency of the MRSCC is higher than its main resonant frequency at k=1.3. By decreasing the switching frequency of MRSCC from 500kHz to 300kHz, the RMS current of the flying capacitor reduces significantly at k=1.3. Therefore, by selecting k to be around 1.3, the MRSCC shows the immunity towards ± 20 % flying capacitor's variation and better efficiency. Fig. 22 compares the efficiency improvement between 300kHz and 500kHz. The startup voltage and interleaved current profiles of the built four-phase MRSCBC converter are shown in Fig. 23. For fast PCB parasitic analysis, a single-phase MRSCBC is created in Cadence Capture. Fig. 24 shows the steady-state output voltage profile of the converter.

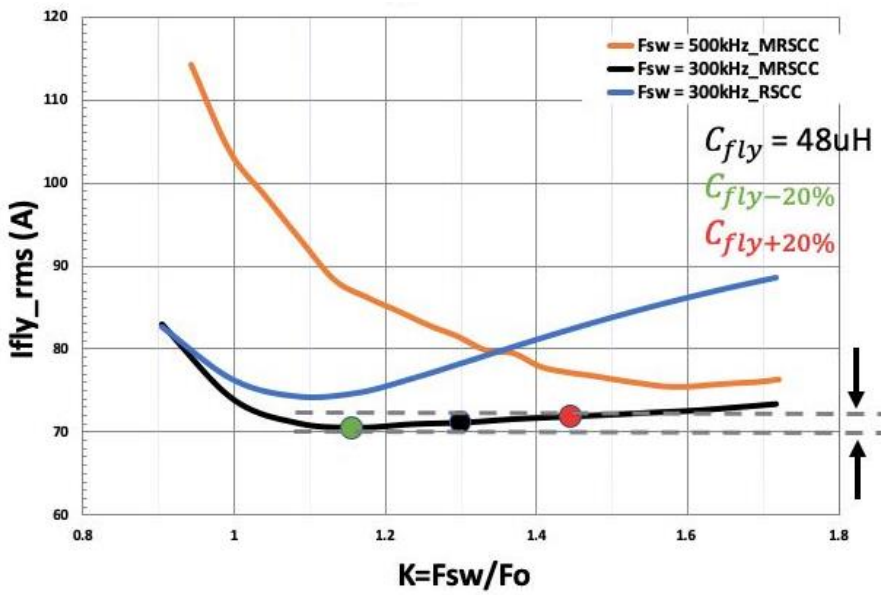

Fig. 21. Fly capacitor current change with respect to resonant and switching frequency mismatch.

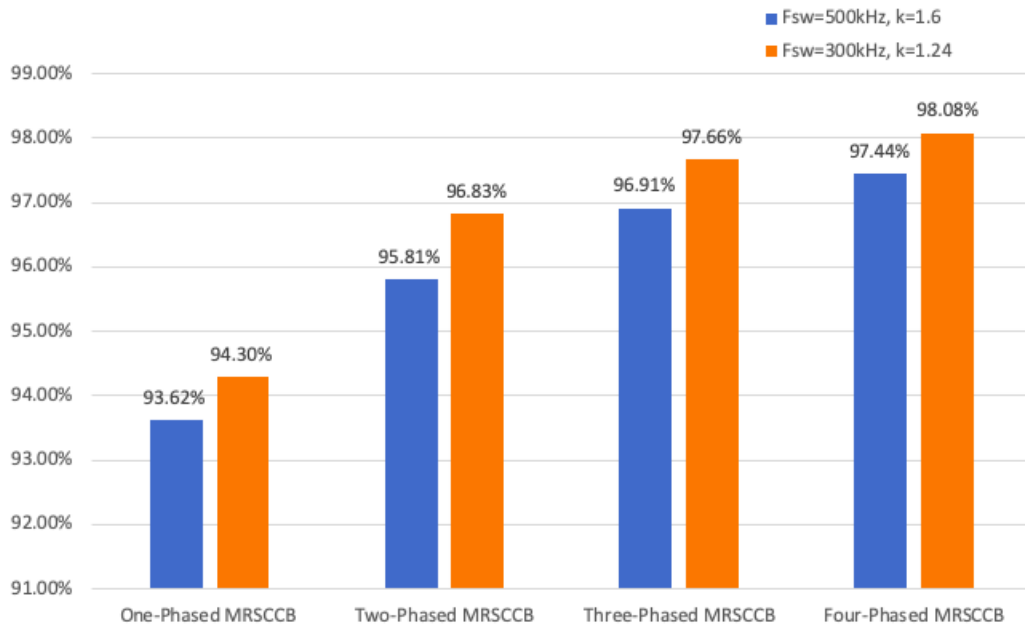

Fig. 22. Efficiency comparison of 300kHz and 500kHz design.

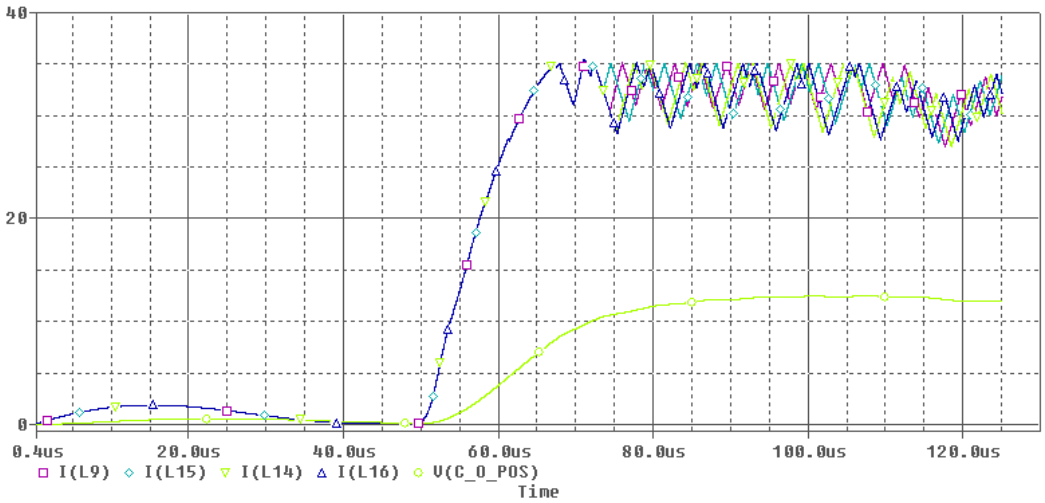

Fig. 23. Output voltage and inductor interleaved current during startup; (Y-axis shared between current and voltage signals).

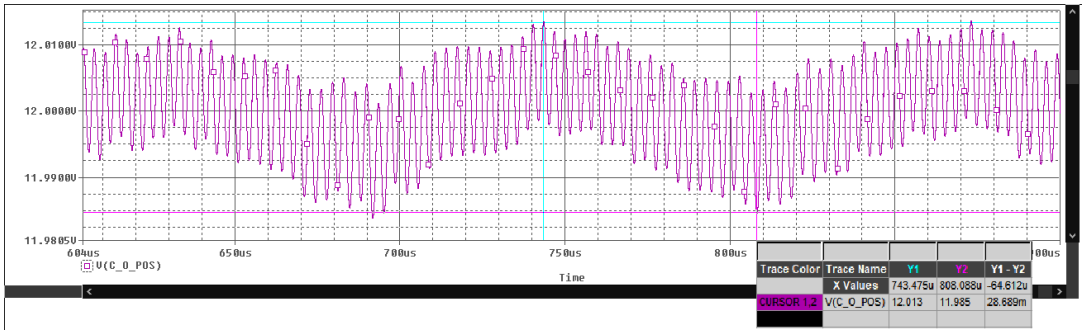

Fig. 24. Output voltage of designed MRSCBC.

4 SPICE AND PHYSICAL DESIGN

The full design process of the proposed converter, shown in Fig. 25, starts with behavioral simulation design in SIMPLIS and moves to SPICE simulations in Cadence Capture. An initial PCB design is then created in OrCAD PCB Editor. Ansys Q3D imports the design and exports a PSpice model of the self and mutual parasitic elements in each net. The model is fed back into Cadence Capture to study the performance of the converter with the simulated parasitic elements.

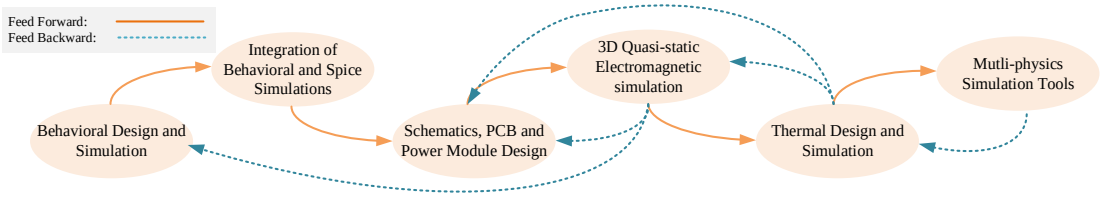

Fig. 25. Workflow diagram of the technical design approach used in this paper.

Texas Instrument's LM5141 synchronous buck controller featuring peak current mode control provides feedback closed-loop control signals to two UCC21520 isolated gate drivers per phase. Featuring a buck converter on the output of the multi-resonant switched capacitive converters allows the use of traditional synchronous buck controllers. Traditional control ICs simplify the design of the feedback control and allow for flexibility in choosing controllers as the synchronous buck controller with peak current mode control is common. The isolated gate drivers help reduce switching losses while each drives two gates.

OrCAD PCB editor is used to create a single-phase PCB design. The first design performed does not have to be final and contains all the thermal considerations. The initial PCB design is for parasitic analysis and as a result, the design is chosen such that it is focused on a realistic layout for the converter. To start the design an 8-layer board is

chosen to provide flexibility in routing and EMI control with multiple ground planes. Fig. 26 shows the layer cross-section of the board with 4oz copper in each layer. Two ground planes on layers 2 and 7 ensure that any internal high-speed signal routing is shielded from EMI.

Objects		Types		Thickness	Physical		Embedded	Signal Integrity		
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore
		Surface							1	
1	TOP	Conductor	Conductor	5.6	1	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
2	GND	Conductor	Conductor	5.6	2	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
3	INNER_SIGNAL	Conductor	Conductor	5.6	3	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
4	POW	Conductor	Conductor	5.6	4	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
5	POW-	Conductor	Conductor	5.6	5	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
6	INNER_SIGNAL2	Conductor	Conductor	5.6	6	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
7	GND2	Conductor	Conductor	5.6	7	Copper	Not embedded	596000	1	
		Dielectric	Dielectric	14		Fr-4		0	4.5	
8	BOTTOM	Conductor	Conductor	5.6	8	Copper	Not embedded	596000	1	
		Surface							1	

Fig. 26. Eight-layer cross section.

The first traces routed shown in green in Fig. 27 are the power traces as they are the least flexible to reroute and require the largest footprint. The remaining elements such as controllers, gate drivers, and voltage regulators are centered around the power circuit with their footprints catering to the need of the power circuit. The controller LM5141-Q1 is highlighted with a blue square and placed around the output and benefits from short trace length for feedback signals such as voltage and current sensing. The gate drivers highlighted with an orange square are placed physically close to the mosfets. The designed PCB imported into ANSYS Electronic Desktop is shown in Fig. 28.

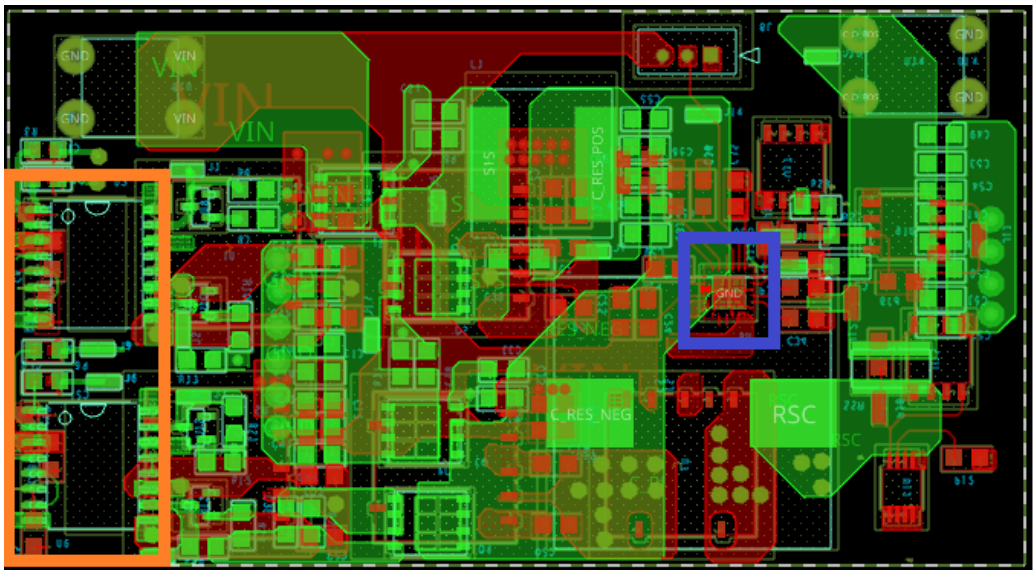

Fig. 27. First and final layer of the initial design highlighting component placement.

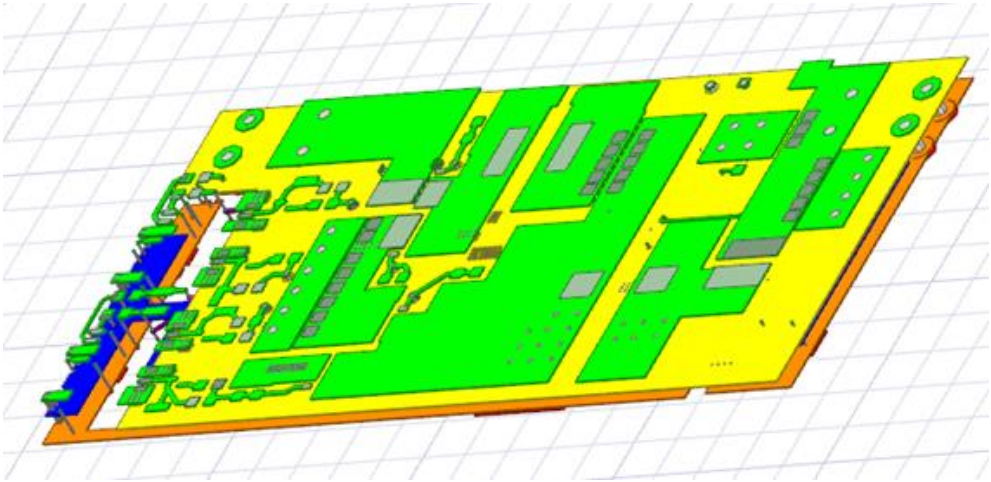

Fig. 28. PCB design in Q3D.

5 SIMULATION AND RESULT

Q3D extracts a model for the self and mutual parasitic capacitance, inductance, and resistance and exports it as a PSpice file. The PCB model is imported into Ansys Q3D extractor which provides the values of the parasitic components at the switching frequency, 300kHz in this case. The self and mutual inductance and capacitance matrix are then imported into Cadence Capture as a square model. Fig. 29 displays the parasitic models connected to the circuit in Cadence Capture. Analysis of the performance of the converter with a parasitic model finds that the inductance is the most sensitive variable in design. Acceptable maximum inductance values range from $L\times10^{-11}$ to $L\times10^{-12}$. Higher inductance values in the nH range in the control and gate drive traces produce voltage spikes during rising and falling edges high enough to block the MRSCBC from starting or reaching 12V output. Fig. 30 shows the startup response with original and reduced inductance values. The parasitic model highlights the importance of reducing the inductance in the control and gate drive traces in the PCB design. The multi-resonant power converter circuit, however, is tolerant to the forementioned inductance values.

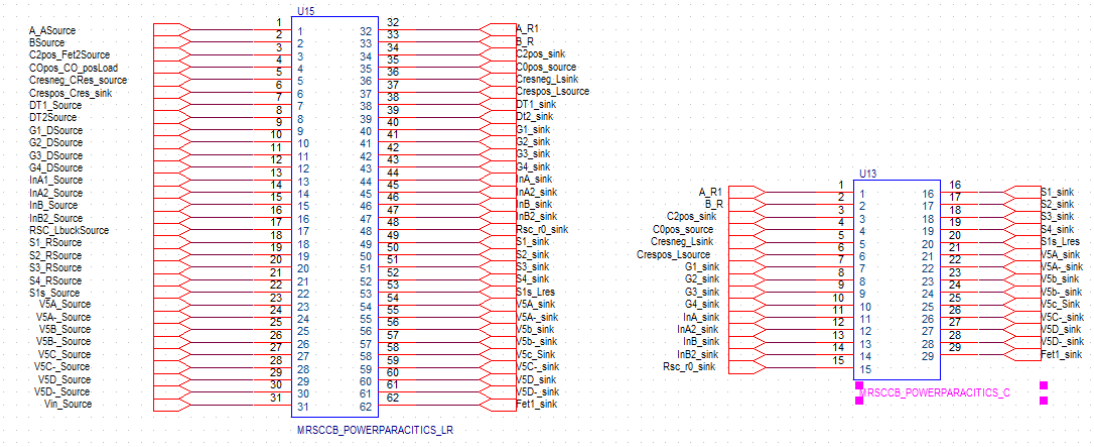

Fig. 29. Spice model of the parasitic elements in the designed PCB.

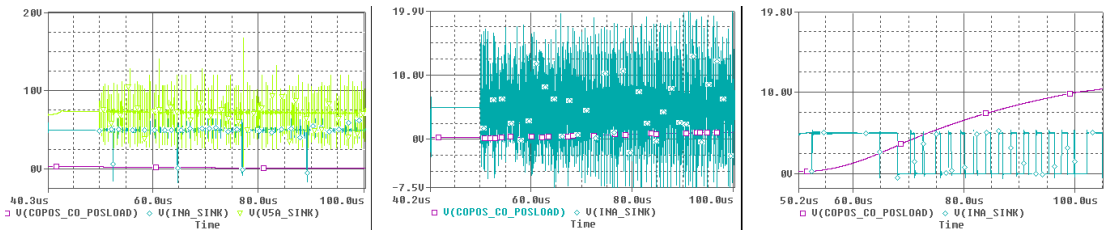

Fig. 30. Left to right: 1. circuit failure to start with high parasitic inductance; 2. circuit startup with lowered inductance in gate drive traces. 3. circuit Startup with lowered inductance in control and gate drive traces.

6 PCB REDESIGN AND EMI

6.1 PCB Redesign

The information obtained from the Q3D analysis supports the need for a new PCB design. The original design aimed to provide feedback on the circuit's operation with parasitic elements. The redesign initially would focus on reducing the inductances of the traces between the gate driver and the switches. Due to the presence of many capacitors and inductors next to the switches in the MRSCBC, it is difficult to route the gate drive traces without utilizing vias. As a result, the gate drivers are moved underneath the Mosfets to reduce the length of the traces as possible. Fig. 31 compares the two trace paths.

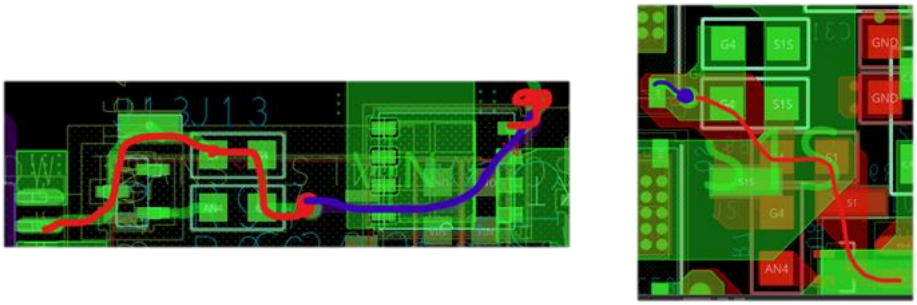

Fig. 31. Routing comparison of gate driver output with the old design on the left and new design on the right.

The redesign also focuses on other elements such as maximizing power density and including some heat management. Thermal vias are used underneath the switching mosfets as shown in Fig. 32. The inductor choice is changed to a shorter inductor, and the design overall is brought closer together as depicted in Fig. 33. Capacitors with 1206 size used in the place of the power capacitors C_{fly} and C_2 to help with heat dissipation of the current as shown in Fig. 34. The number of layers is reduced from 8 layers to 6 to help

reduce current loop sizes. A chassis ground added is shown in Fig. 35 and Fig. 36 highlights the overall compact improvements of the design. Analysis of the parasitic inductances is performed again the results are displayed in Fig. 37. A bill of material is prepared and shown in Table 4.

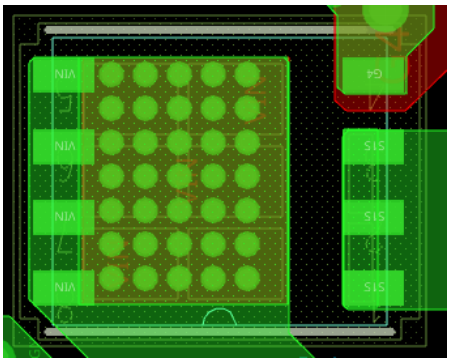

Fig. 32. Thermal vias underneath the mosfets.

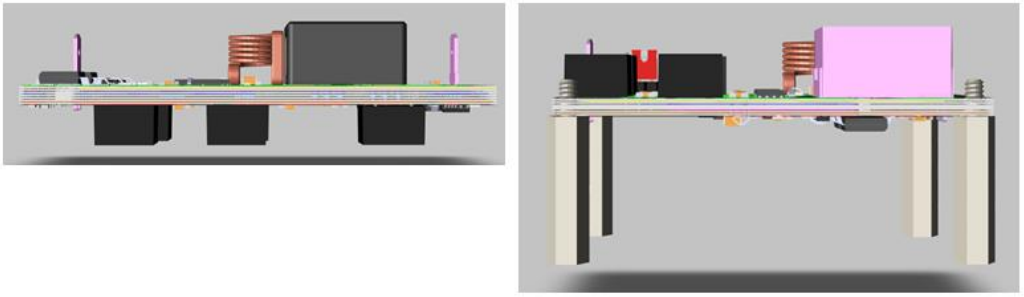

Fig. 33. Height comparison of original design (left) and redesign (right).

Fig. 34. Power capacitor size comparison between original (left) and redesign (right).

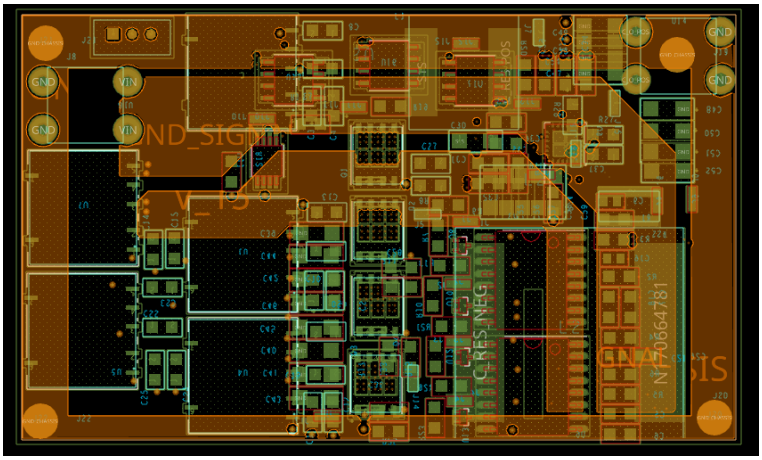

Fig. 35. Routing of chassis ground.

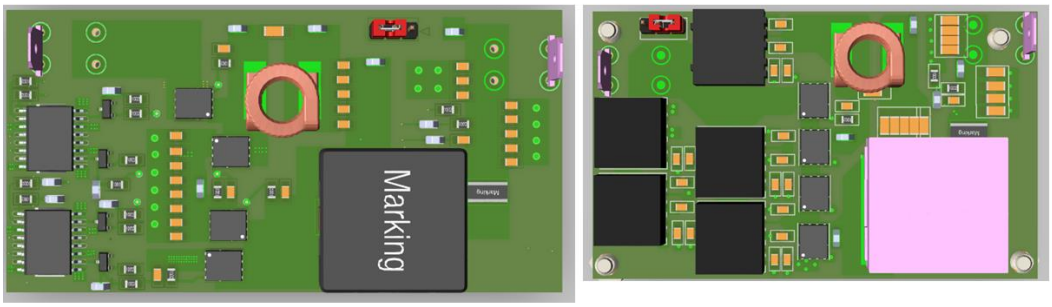

Fig. 36. Overall design comparison highlighting compactness between original (left) and redesign (right).

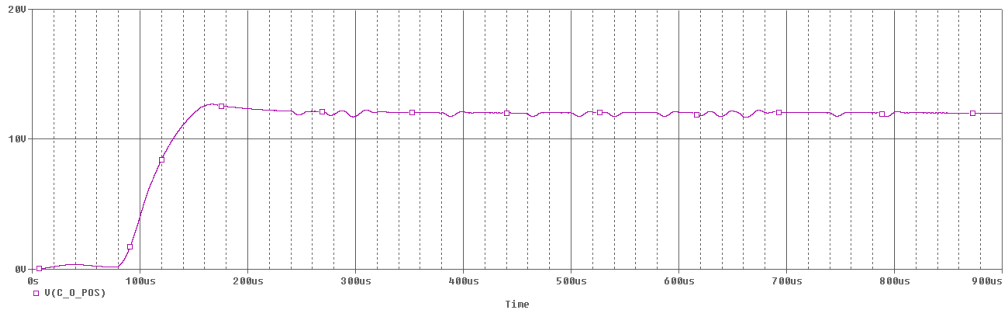

Fig. 37. Output of PSpice simulations with redesign parasitics.

Table 4. Bill of Materials.

Item #	Value	Manufacture	Manufacture #	Qty 4phs
1	10n	Würth Elektronik	885012207122	36
2	0.1u	Würth Elektronik	885012207128	32
3	10p	Würth Elektronik	885012006073	16
4	1n	Würth Elektronik	885012207116	56
5	46n	KEMET	C0805C473J1RAC 7800	4
6	5p	Würth Elektronik	885012007101	4
7	5n	Würth Elektronik	885012007092	4
8	120n	KEMET	C0805C124K1RA CTU	4
9	0.33u	Würth Elektronik	885012207101	4
10	4.7uF (2 x 2.2uF stacked)	Samsung Electro-Mechanics	CL31B225KCHSN NE	80
11	10uF	Würth Elektronik	885012208041	40
12	Pin	Keystone Electronics	5015	60
13	CON_532530370	Molex	532530370	4
14	22nH	Würth Elektronik	7449152022	4
15	4.7u	Pulse Electronics Power	PA4349.472ANLT	4
16	BSC032N04LS	Infineon Technologies	BSC032N04LSAT MA1	16
17	50	Vishay Dale	RCS080549R9FK EA	16
18	10k	Panasonic Electronic Components	ERA-6AEB103V	32
19	8	Panasonic Electronic Components	ERJ-6BQF1R0V	4

20	76k	Panasonic Electronic Components	ERJ-6ENF7682V	4
21	73.7674k	Panasonic Electronic Components	ERA-6AEB7322V	4
22	0	Vishay Dale	CRCW08050000Z 0EBC	12
23	0	Wurth Electronics	581070763001	4
24	9.1K	Panasonic Electronic Components	ERA-6ARB912V	4
25	94.1k	TE Connectivity Passive Product	RQ73C2A93K1BT D	4
26	TRS2-4823	Traco Power	TRS 2-4823	16
27	UCC21520DW_T RANS	Texas Instruments	UCC21520DW	8
28	TRS2-4813	Traco Power	TRS 2-4813	4
29	BAT54	ON Semiconductor	BAT54	16
30	LM5141-Q1RGE	Texas Instruments	LM5141-Q1	4
31	ds1090u-16	Maxim Integrated	DS1090U-16+	4
32	2 Tab	TE Connectivity AMP Connectors	63986-1	16
33	DS1100Z-500	Maxim Integrated	**DS1100Z-500+**	8
34	DS1100Z-40	Maxim Integrated	DS1100Z-40+	4
35	Test Point	Keystone Electronics	4820	100

6.2 EMI Analysis

PSIM is used to run EMI simulation on conducted noise. The MRSCBC is recreated in PSIM with the parasitic values found during ANSYS Q3D Simulations. Fig. 38 shows the MRSCBC with parasitic inductances in the power traces. An EMI line filter with part number 810911010 is chosen from Würth Elektronik and is shown in Fig. 38. The line

filter is shown in Fig. 39 for reference. The EMI of the circuit is shown in Fig. 40 passing CISPR 22 standards.

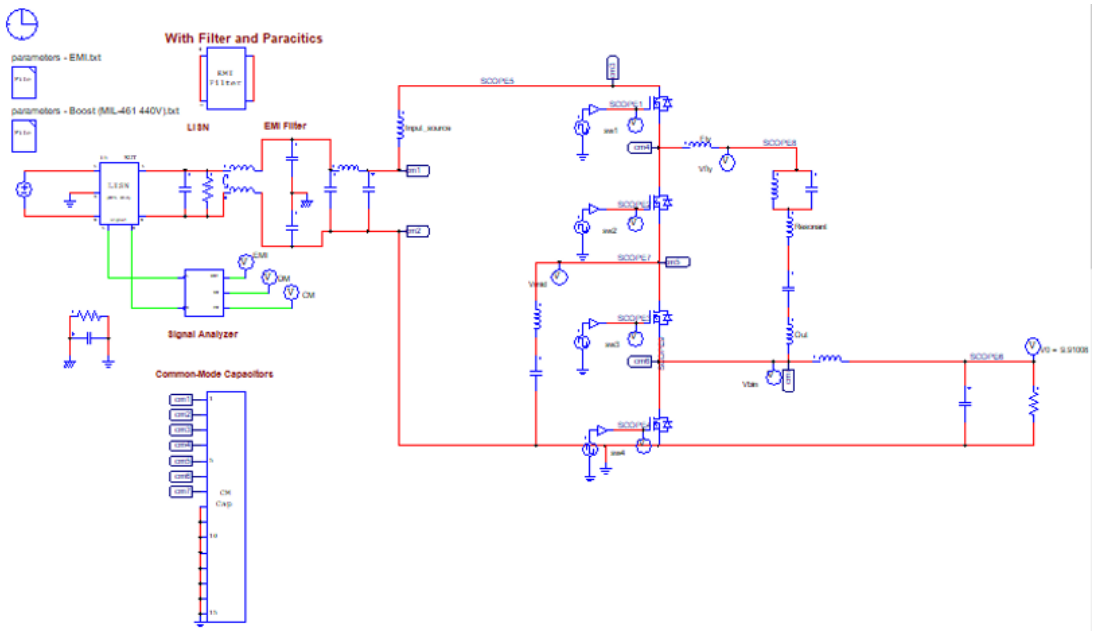

Fig. 38. PSIM model with parasitic inductances in the power traces.

Fig. 39. 810911010 Line filter from Würth Elektronik.

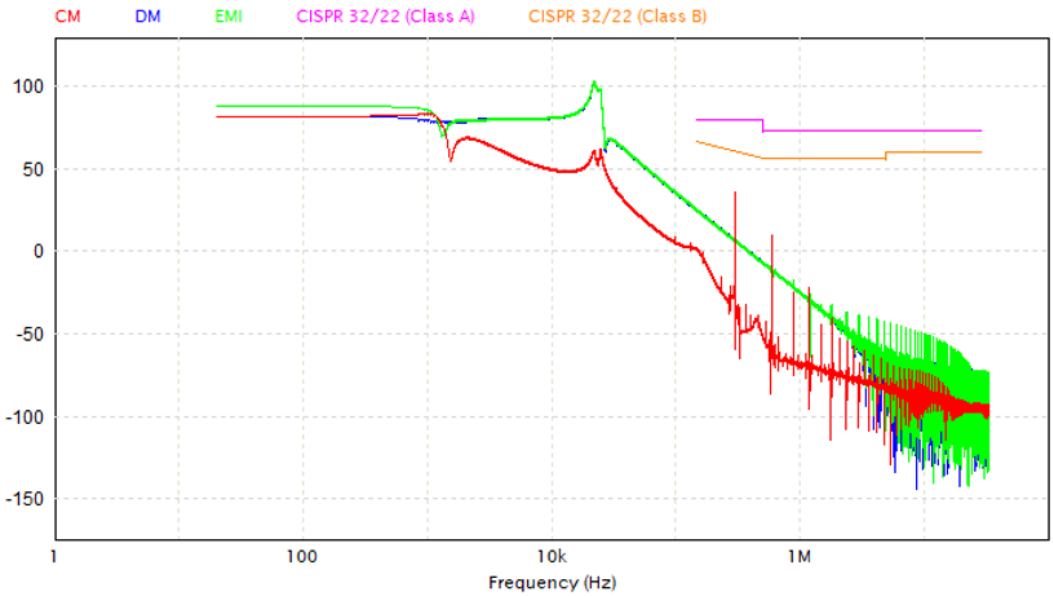

Fig. 40. EMI results of simulation shown passing CISPR 22 standards.

7 CONCLUSION

Analysis through ANSYS Electronic Desktop allows for the simulation of the operation of the design close to experimental data and provides feedback on improvements before the design is completed. An acceptable inductance range value in the gate drive and switching traces are presented for the operation of the MRSCBC. Future work constitutes an experimental prototype of the proposed converter to validate the system's effectiveness and highly efficient characteristics.

Gallium nitride's application is worth considering due to its rising popularity. Designing short gate drive traces is challenging as shown in previous attempts to design a PCB for the MRSCBC. The presence of two inductors and two arrays of power capacitors around the switches cause a blockage around the switched for routing non-power signals. Gallium nitride technology's high switching speed cause higher susceptibility to parasitic inductances in the traces than silicon mosfets. As a result, gallium nitride application for the MRSCBC is discouraged until better routing techniques are available for the MRSCBC which ensures tight gate drive loops.

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