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Araştırma Makalesi / Research Article

DVCC Based Current-Mode First Order All-Pass Filter and Quadrature Oscillator

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Abstract: A current mode first-order all-pass filter configuration is proposed. The presented circuit uses a single differential voltage current conveyor (DVCC), a capacitor and resistors. High output impedance of the proposed filter enables the circuit to be cascaded without additional buffers. To demonstrate the performance of the proposed filter a new current mode quadrature oscillator is given as an application example. Oscillator is implemented through the proposed first order all-pass filter and integrator as the building blocks. Furthemore the effects of tracking errors of the DVCC on oscillation condition and frequency are investigated. The theoretical results are verified with PSPICE simulations using a new CMOS realization of DVCC.

Key-words*: All-pass filter, differential voltage current conveyor, quadrature oscillator, analog integrated circuits.*

Introduction

Current mode circuits have been receiving considerable attention due to their potential advanteges such as inherently wide band width, higher slow-rate, geater linearity, wider dynamic range, simply circuiting and low power consumption [1-5] . The active devices that have been used for the realization of current mode circuits include current conveyor, current feedback operational amplifier, operational transconductance amplifier and differential voltage current conveyor. The use of current mode active filter is being attractive in high frequency signal processing applications.

All-pass filters are one of the most commonly used filter types of all. They are generally used for introducing a frequency dependent delay while keeping the amplitude of the input signal constant over the desired frequency range. Other types of active circuits such as oscillators and high-Q band-pass filters are also realized by using all-pass filters [6]. Current-mode filters reported in literature either do not offer all-pass configuration at all, or are excess in the number of components and require component matching constraints[7-11]. Recently, a current differencing buffered amplifier (CDBA) and current operational amplifier (COA) based first order current-mode all-pass filter configurations are proposed [12-13]. In this paper , DVCC based current-mode first order all-pass filter configuration is proposed. The proposed circuit uses single DVCC, a capacitor and resistors. A sinusoidal quadrature oscillator is implemented to show usefulness of the proposed configuration as an illustrating example. PSPICE simulations are given which confirms the theoretical analysis.

The Proposed Circuit

The DVCC was proposed first by Pal a modified current conveyor [14] and then developed and realized in CMOS tecnology by Elwan and Soliman [15]. The DVCC has the advantages of both of the second generation current conveyor (CCII) (such as large signal bandwith, great linearty, wide dynamic range) and differential difference amplifier (DDA) (Such as high input impedance and arithmetic operational capability) [15]. This element is a versalite building block for applications demanding floating inputs.

The electrical symbol of the DVCC is shown in Fig.1 and its terminal relations are given by

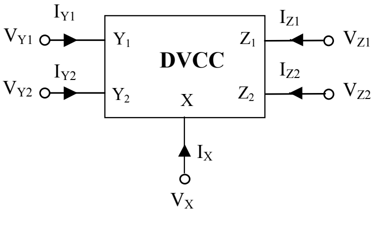

Figure.1 Electrical symbol of the DVCC

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \quad (1)$$

The proposed current-mode first order all-pass configuration is shown in Fig.2.

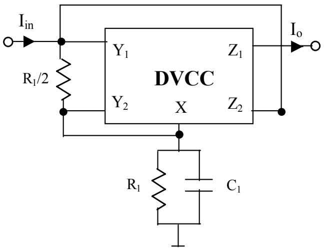

Figure.2 The proposed current-mode first order all-pass filter configuration

Routine analysis yields the current transfer function as follows;

$$\frac{I_z}{I_{in}} = \frac{1 - RCs}{1 + RCs} \quad (2)$$

The proposed all-pass filter has the following phase response.

$$\varphi(\omega) = -2\arctan(\omega RC) \quad (3)$$

Quadrature Oscillator as an All-pass Filter Application

It is well known fact that a sinusoidal quadrature oscillator can be realized using an all-pass section and an integrator [16] as shown in Fig.3. Using this block diagram, DVCC-based current-mode quadrature oscillator can be implemented as shown in Fig. 4. In this circuit, the proposed all-pass filter and current-mode integrator employing a DVCC with two matched resistors and capacitors are used. For providing a sinusoidal oscillation the loop gain of the circuit is set to unity at $s = j\omega$, i.e.

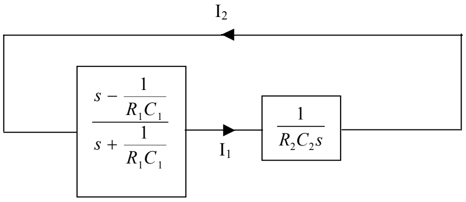

Figure.3 Realization block diagram for quadrature oscillator

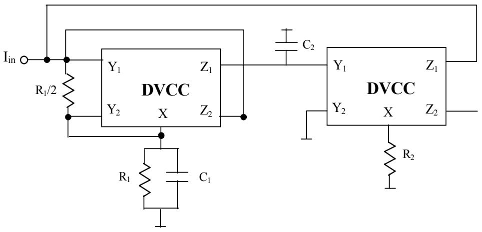

Figure.4 DVCC-based quadrature oscillator circuit

$$\left(\frac{s - \frac{1}{R_1C_1}}{s + \frac{1}{R_1C_1}} \right) \left(\frac{1}{sR_2C_2} \right)_{s=j\omega} = 1 \quad (4)$$

From Equation (4) oscillation condition and frequency can be found respectively as

$$R_1C_1 = R_2C_2 \quad (5)$$

$$\omega_0 = \sqrt{\frac{1}{R_1C_1R_2C_2}} \quad (6)$$

From equations (5) and (6) one concludes that w_0 is given by

$$\omega_0 = \frac{1}{R_1 C_1} \tag{7}$$

For simplicity, if we choose $R_1 = R$ and $C_1 = C$, oscillation condition is satisfied and oscillation frequency becomes:

$$\omega_0 = \frac{1}{RC} \tag{7}$$

Tracking Error Analysis

Tracking into consideration the DVCC non-idealities, terminal relations in (1) can be expressed as

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2}$$

$$I_{Z1} = \alpha_1 I_X \text{ and } I_{Z2} = -\alpha_2 I_X \tag{8}$$

where $\beta_j = 1 - \varepsilon_{VJ}$ and $\alpha_j = 1 - \varepsilon_{IJ}$ for $j = 1,2$. Here ε_{VJ} and ε_{IJ} $\left(|\varepsilon_{VJ}| - |\varepsilon_{IJ}| << 1\right)$ represent voltage and current tracking errors of the DVCC respectively. Reanalysis of the allpass filter circuit shown in Figure-2 yields the modified transfer function as follow

$$\frac{I_O}{I_I} = \alpha_1 \frac{1 + 2\beta_2 - 3\beta_1 - \beta_1 R_1 C_1 s}{2(1 + \beta_2 + -\beta_1 - \alpha_2 - \alpha_2\beta_2 + \alpha_2\beta_1) + \alpha_2\beta_1 + \alpha_2\beta_1 C_1 R_1 s} \tag{9}$$

It can be seen that allpass filter condition, gain and phase functions of the allpass filter may be altered slightly by the effect of the DVCC voltage and current tracking errors. Tracking into account the non-ideal DVCC, characteristic equation of the oscillator circuit shown in Figure-4 becomes

$$\alpha_2\beta_1 C_1 R_1 C_2 R_2 s^2 + \left[\left[2(1 + \beta_2 - \beta_1 - \alpha_2 - \alpha_2\beta_2 + \alpha_2\beta_1) + \alpha_2\beta_1\right] R_2 C_2 - \alpha_1\beta_1\alpha'_1\,\beta'_1\, R_1 C_1\right] s \tag{10}$$

$$+ \alpha_1\alpha'_1\,\beta'_1\,(2 + 2\beta_2 - 3\beta_1) = 0$$

The modified oscillation condition and oscillation frequency are, respectively

$$\left[2(1 + \beta_2 - \beta_1 - \alpha_2 - \alpha_2\beta_2 + \alpha_2\beta_1) + \alpha_2\beta_1\right] R_2 C_2 = \alpha_1\beta_1\alpha'_1\,\beta'_1\, R_1 C_1 \tag{11}$$

$$\omega_o = \sqrt{\frac{\alpha_1\alpha'_1\,\beta'_1\,(2 + 2\beta_2 - 3\beta_1)}{\alpha_2\beta_1 R_1 C_1 R_2 C_2}} \tag{12}$$

Here α'_1 and β'_1 denotes tracking errors of the DVCC used in integrator. From (11) and (12) the oscillatoion frequency is given by

$$\omega_0 = \frac{1}{\beta_1 R_1 C_1}\sqrt{(2 + 2\beta_2 - 3\beta_1)\left[\frac{2(1 + \beta_2 - \beta_1 - \alpha_2)}{\alpha_2} - 2\beta_2 + 3\beta_1\right]} \tag{13}$$

If all $\alpha_i = \beta_i = 1$, $i = 1,2$ (7) is obtained as a special case for ideal DVCC. From Equatoins (11), (12) and (13), the tracking errors slightly change the oscillation conditions and oscillation frequencies. However, the oscillation conditions and oscillation frequencies of the circuit shown in Figure-3 still can be independently controlable. It is noticed that tracking errors of the integrator have no effect on the oscillation frequency.

Simulation Results

The proposed the first order all-pass filter and quadrature oscillator circuits have been simulated using SPICE program to verify the given theoretical analysis. The DVCCs have been simulated using CMOS stucture and MIETEC 0.5µm CMOS process model parameters given in [15]. The supply voltages were taken as $V_{DD} = 2.5V$ and $V_{SS} = -2.5V$. For this purpose, passive components were chosen as R=1k, and C=0.1nF, which results in a 360kHz center frequency. The PSPICE simulations were performed using a CMOS realization of DVCC. Simulation results of the filter response with CMOS DVCC is given Fig.5, which are in good agreement with the predicted theory. Fig.6 shows the time domain response of the filter. A sinusoidal input at the frequency of 159kHz was applied to the all-pass network constructed with above mentioned passive element values.Actually, the parasitic resistances and capacitances, and tracking error parameters of the CMOS- DVCC, that is not mentioned in the limited space available here, cause the deviations in the frequency and phase response of the filter from theoretical values.Quadrature oscillator employing the proposed all-pass filter has also been simulated using PSPICE. In this simulation all resistances and capacitances were taken as 1kΩ and 0.1nF respectively which results in a 159kHz oscillation frequency. The output waveforms of the oscillator are shown in Fig.7. Actually, the parasitic resistances and capacitances, and tracking error parameters of the CMOS- DVCC also cause the deviations in the output waveforms of the filter and oscillator from the theoretical values.For either discrete or integrated implementation of the filter and oscillator circuits, the designers should pay attention to reduce the parasitics of DVCC.

Conclusion

A Current-mode first order all-pass filter configuration is presented. The proposed circuit uses only a single DVCC, a capacitor and resistors. The output of the filter exhibits high impedance so that the synthesized current-mode filters can be cascaded without additional buffers.The proposed allpass filter were employed to implement the quadrature oscillator As an application of the filter, a new quadrature oscillator was realized. Moreover tracking error analysis of the proposed allpass filter and oscillator circuits were made for non-ideal DVCC. PSPICE simulations of the proposed circuits were performed by using a CMOS realization of DVCC. The proposed circuits are designed for operation at high frequency and tested using SPICE simulation program. Simulation results agree quite well with the theoretical analysis.

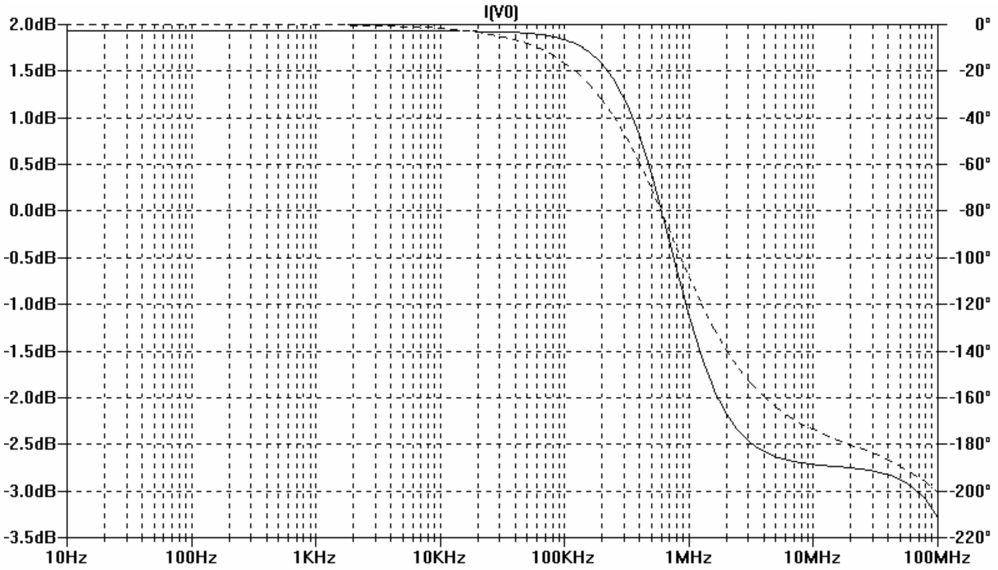

Figure.5 PSPICE simulation result of the proposed current-mode first order all-pass filter (amplitude —, phase ---)

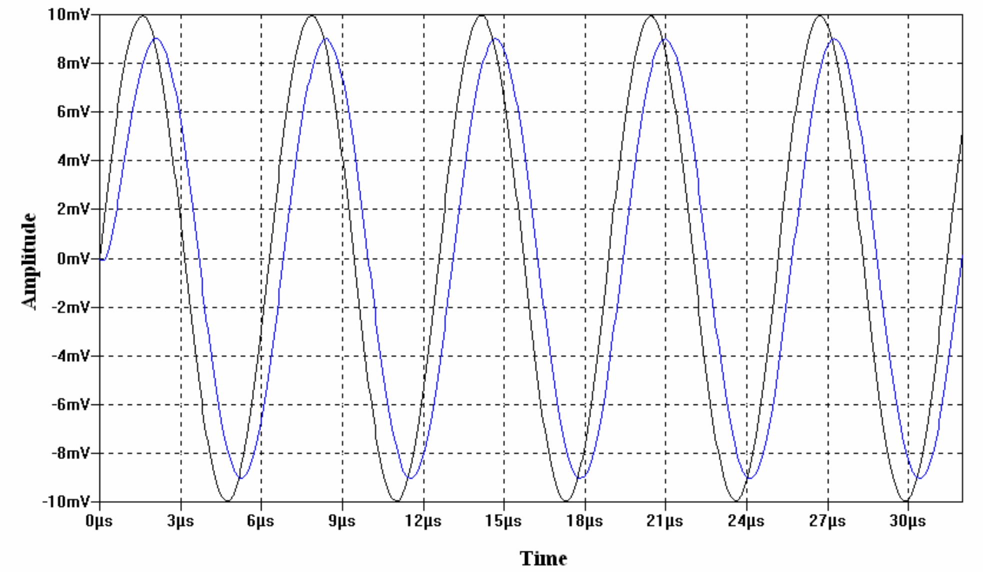

Figure.6 Simulated time-domain response of the proposed all-pass filter (input: ▲, output: ■)

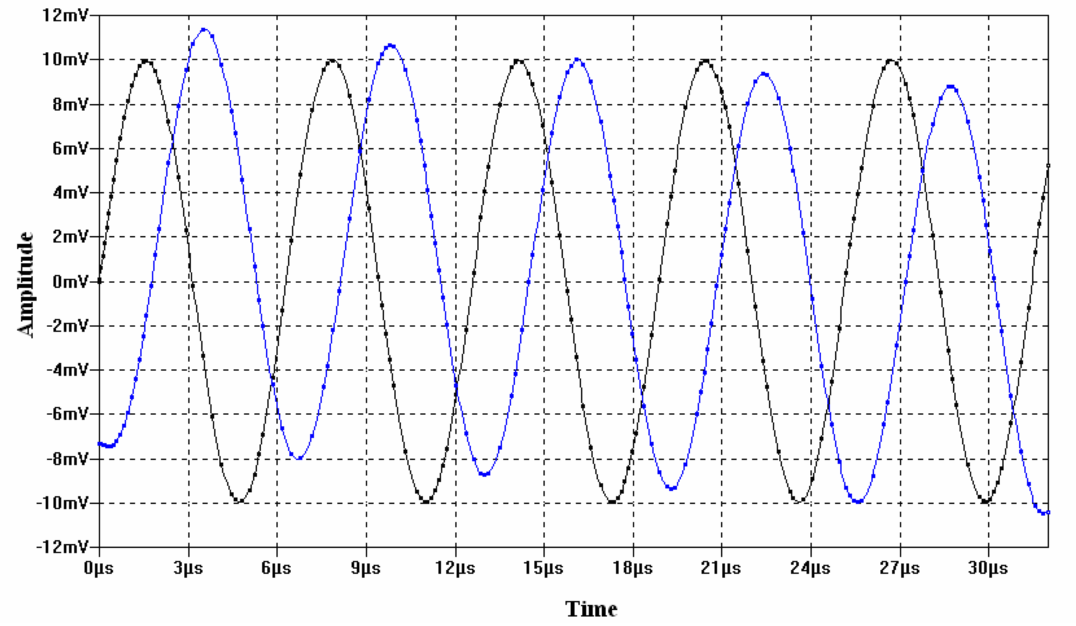

Figure.7 Sinusoidal output waveforms of the quadrature oscillator (input: ▲, output: ■)

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