INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

PERANCANGAN DAN PEMBUATAN SISTEM ABONEMEN PEMBAYARAN PADA WARNET DENGAN MENGGUNAKAN MEMBER CARD RFID BERBASIS MIKROKONTROLER RENESAS R8C/13

SKRIPSI

Disusun Oleh :

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SEPTEMBER 2006

LEMBAR PERSETUJUAN

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Disusun Untuk Melengkapi Dan Memenuhi Syarat
Guna Mencapai Gelar Sarjana Teknik

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ABSTRAKSI

Denny Prasetya, 01.17.082 "Perancangan dan Pembuatan Sistem Abonemen Pembayaran Pasa Warnet dengan Menggunakan Member Card RFID Berbasis Mikrokontroller Renesas R8C/13", Skripsi Jurusan Teknik Elektro S1, Konsentrasi Teknik Elektronika S1 Institut Teknologi Nasional Malang, Dosen Pembimbing : Joseph Dedy Irawan, ST, MT

Kata Kunci : Sistem Abonemen (Prabayar), dengan Tag RFID, RFID Reader, Buzzer, Keypad, Mikrokontroler R8C/13, LCD, PC

Sistem abonemen atau prabayar merupakan system yang digunakan sebagai pembayaran tanpa harus mengeluarkan uang tunai dengan cara pembayaran yang dilakukan dahulu untuk mendapatkan saldo.

Dengan adanya sistem pembayaran abonemen menggunakan fasilitas membercard RFID, maka akan mempermudah bagi pemilik maupun pengguna warnet untuk mempercepat proses pembayaran tanpa harus mengeleuarkan uang tunai oleh pelanggan secara tepat serta fasilitas member yang bersifat personal.

Skripsi ini menjelaskan tentang sistem abonemen yang menggunakan Tag untuk memancarkan gelombang radio. Pada saat gelombang radio melalui medan yang dihasilkan oleh RFID Reader, tag akan terdeteksi dan mentransmisikan informasi yang ada pada tag kepada reader. Informasi tersebut akan diterjemahkan oleh mikrokontroler R8C/13 sehingga data yang ada pada PC dapat ditampilkan pada display untuk dibaca.

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Seiring dengan perkembangan pembangunan, teknologi elektronika mengalami kemajuan yang sangat pesat, menyebabkan manusia tidak akan lepas dari penggunaan berbagai macam peralatan elektronika yang ada, baik itu penggunaan peralatan yang berupa perangkat keras maupun perangkat lunak elektronika.

Dalam perkembangannya warung internet atau warnet kini bersaing untuk memberikan pelayanan yang maksimal, tetapi sering kali pelayanan yang diberikan warnet tersebut banyak menyebabkan komplain bagi para pelanggannya. Antara lain komplain pada penghitugan waktu pemakaian jasa internet yang sering tidak cocok dengan pembayarannya.

Teknologi elektronika menuntut manusia untuk merekayasa suatu peralatan elektronika yang praktis. Dari uraian di atasalah satu peralatan elektronika yang berkembang dewasa ini banyak menggunakan suatu perangkat lunak yang akan menjalankan suatu peralatan elektronika. Dengan adanya sistem pembayaran abonemen menggunakan fasilitas membercard RFID, maka akan mempermudah bagi pemilik maupun pengguna warnet untuk mempercepat proses pembayaran tanpa harus mengeleuarkan uang tunai oleh pelanggan secara tepat serta fasilitas member yang bersifat personal.

1.2. Rumusan Masalah

Mengacu pada latar belakang masalah di atas, maka rumusan masalah dapat dijabarkan sebagai berikut:

1. Bagaimana mendesain suatu sistem berbasis mikrokontroler Renesas R8C/13 yang dapat mendeteksi kartu RF ID tersebut.
2. Bagaimana membuat simulasi dari alat tersebut
3. Bagaimana merancang program pengaktifan waktu pemakaian jasa internet yang dapat menghitung berapa biaya pemekaian jasa internet tersebut agar dapat dideteksi oleh mikrokontroler.

1.3. Tujuan

Tujuan dari penulisan tugas akhir ini adalah untuk merencanakan dan membuat suatu sistem pembayaran pada pemakaian jasa internet di warung internet, dan membuat perngakat lunak sebagai pengendali utama dari peralatan yang akan dibuat.

1.4. Batasan Masalah

Mengingat begitu luasnya bahan kajian mengenai sistem pembayaran menggunakan member card, maka pokok bahasan dibatasi sebagai berikut:

1. Pengendali utama sistem menggunakan mikrokontroler Renesas R8C/13.
2. Untuk sistem abonemen pembayaran menggunakan membercard RFID.
3. Pembacaan kartu RF ID dilakukan dengan menembakkan sensor ke kartu.

4. Bila ada peralatan yang mempunyai fungsi sama tetapi berbeda dalam metode, model fisik, dan rangkaiannya tidak dibahas dalam skripsi ini.
5. Tidak membahas catu daya.
6. Tidak membahas internet.
7. Pembuatan program data base untuk sistem pembayaran menggunakan PC (*Personal Computer*).

1.5. Metodologi

Metodologi yang digunakan dalam penyusunan tugas akhir ini adalah sebagai berikut:

1. Study literature, meliputi:

   Melakukan kajian buku, majalah atau hasil penelitian di laboraturium.

2. Perencanaan tiap blok diagram

   Perencaan yang dilakukan berhubungan dengan prinsip kerja alat yang akan digunakan, kemudian komponen yang dipakai dilakukan penggabungan masing-masing blok yang telah disusun.

3. Pengujian alat

   Penngujian alat dilakukan perbloksystem dan keseluruhan system yang telah disusun sehngga disimpulkan suatu efektifitas penggunaan suatu alat.

4. Analisa.

1.6. Sistematika Penulisan

Pembahasan laporan skripsi ini akan diuraiakan dan dijabarkan dalam setiap bab, dengan pembagian sebagai berikut:

BAB I : PENDAHULUAN

Terdiri dari latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi, dan sistematika penulisan.

BAB II : LANDASAN TEORI

Membahas teori-teori yang mendukung dan menunjang perencanaan dan membuat alat yang digunakan.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Berisi tentang proses perencanaan dan pembuatan sistem pembayaran pemakaian jasa internet di warnet.

BAB IV : PENGUJIAN ALAT

Berisi tentang pengujian terhadap alat yang dibuat.

BAB V : PENUTUP

Memuat tentang kesimpulan-kesimpulan yang diperoleh dari hasil pembuatan laporan skripsi ini serta saran untuk pengembangan lebih lanjut.

BAB II

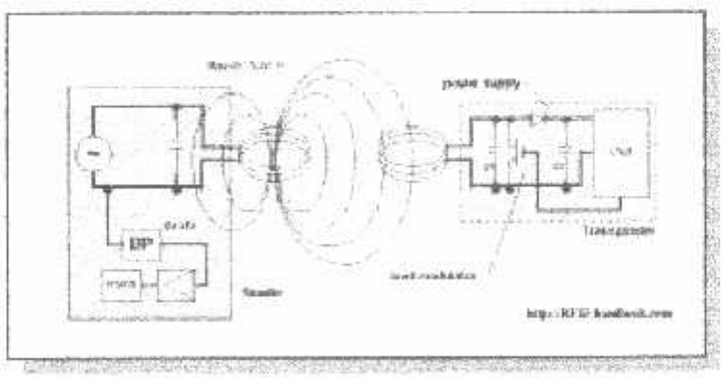
LANDASAN TEORI

2.1. Umum

Pada bagian ini akan dibahas teori penunjang untuk peralatan yang akan dirancang yaitu teori dasar RFID dengan ID-10 RFID Reader, mikrokontroler AT89S51, tombol masukan (*keypad*), dan tampilan (*display*).

2.2. RFID

RFID adalah proses identifikasi seseorang atau objek dengan menggunakan frekuensi transmisi radio. RFID menggunakan frekuensi radio untuk membaca informasi dari sebuah devais kecil yang disebut tag atau *transponder* (*Transmitter* + *Responder*). Tag RFID akan mengenali diri sendiri ketika mendeteksi sinyal dari devais yang kompatibel, yaitu pembaca RFID (RFID *Reader*) dengan range kisaran pembacaan 8cm serta bekerja pada frekuensi 125 KHz.



Gambar 2.1 Komunikasi Antara Reader dan Transmiter (Tag)
Sumber: www.digiware.com, RFID

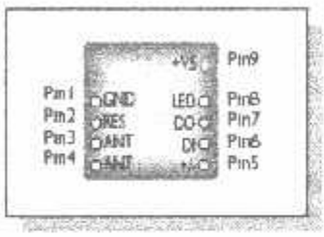
RFID dapat disediakan dalam devais yang hanya dapat dibaca saja (*Read Only*) atau dapat dibaca dan ditulis (*Read/Write*), tidak memerlukan kontak langsung maupun jalur cahaya untuk dapat beroperasi, dapat berfungsi pada berbagai variasi kondisi lingkungan, dan menyediakan tingkat integritas data yang tinggi. Sebagai tambahan, karena teknologi ini sulit untuk dipalsukan, maka RFID dapat menyediakan tingkat keamanan yang tinggi.

Pada sistem RFID umumnya, tag atau *transponder* ditempelkan pada suatu objek. Setiap tag membawa dapat membawa informasi yang unik, di antaranya: serial number, model, warna, tempat perakitan, dan data lain dari objek tersebut. Ketika tag ini melalui medan yang dihasilkan oleh pembaca RFID yang kompatibel, tag akan mentransmisikan informasi yang ada pada tag kepada pembaca RFID, sehingga proses identifikasi objek dapat dilakukan.

Sistem RFID terdiri dari empat komponen, di antaranya seperti dapat dilihat pada gambar 1:

- Tag: Ini adalah devais yang menyimpan informasi untuk identifikasi objek. Tag RFID sering juga disebut sebagai *transponder*. Format dari tag pada perancangan ini adalah EM4001 atau tag kompatibel lainnya.
- Antena: untuk mentransmisikan sinyal frekuensi radio antara pembaca RFID dengan tag RFID.
- Pembaca RFID: adalah devais yang kompatibel dengan tag RFID yang akan berkomunikasi secara *wireless* dengan tag. Digunakan Tipe ID-10 sebagai RFID reader pada perancangan ini.

- Software Aplikasi: adalah aplikasi pada sebuah workstation atau PC yang dapat membaca data dari tag melalui pembaca RFID. Baik tag dan pembaca RFID diperlengkapi dengan antena sehingga dapat menerima dan memancarkan gelombang elektromagnetik.



Gambar 2.2 Konfigurasi Pin ID-10 (RFID Reader)
Sumber: www.digiware.com, RFID

Format Pembacaan ASCII

Salah satu tipe dari RFID reader ini yang digunakan pada alat ini adalah ID-10. RFID reader ini memiliki dua bentuk output serial yaitu: ASCII dan Wiegand 26-bit. Pada perancangan alat ini digunakan output dengan format ASCII, karena output ini sangat mudah untuk dihubungkan pada mikrokontroler.

Tabel 2.1 Fungsi Pin dan Format Data

Pin No.	Description	ASCII	Wiegand26
Pin 1	Zero Volts and Tuning Capacitor Ground	GND 0V	GND 0V
Pin 2	Strap to −5V	Reset Bar	Reset Bar
Pin 3	To External Antenna and Tuning Capacitor	Antenna	Antenna
Pin 4	To External Antenna	Antenna	Antenna
Pin 5	Format Selector (+/-)	Strap to GND	Strap to +5V
Pin 6	Data 1	CMOS	One Output
Pin 7	Data 0	TTL Data (inverted)	Zero Output
Pin 8	3.1 kHz Logic	Beeper / LED	Beeper / LED
Pin 9	DC Voltage Supply	5V (+)	5V (-)

Sumber: www.digiware.com, RFID

Output yang memiliki format ASCII memiliki struktur sebagai berikut:

0 2	10 data karakter ASCII	checksum	CR	LF	0 3

Checksum merupakan hasil EXOR (Exclusive OR) dari 5 biner data byte. Misalnya data output serial (dalam hexadesimal) yang kita tangkap adalah sebagai berikut:

02	30	34	36	32	30	31	44	37	36	43	44	43	0D	0A	03

Langkah pertama adalah merubah semua nilai data diatas menjadi karakter ASCII. Misalnya 30H menjadi karakter "0", 34H menjadi karakter "4", dst. Langkah kedua adalah menyusun data – data tersebut ke dalam Format Data ASCII seperti tabel 1. Kemudian ambil 10 data karakter ASCII. Dalam contoh ini berarti data tersebut adalah:

30	34	36	32	30	31	44	37	36	43	Data Heksa
		6	2	0	1	D	7	6	C	Data ASCII

Untuk data dengan angka 30 dan 34 merupakan data untuk jenis-jenis kartu dan tidak digunakan dalam proses konversi, yang akan dipakai disini adalah data yang ke 3 s/d 10. Hasil konversi dari data heksa ke dalam data ASCII adalah "6201D76C". Gabungkan karakter data ASCII menjadi bilangan Hexadesimal, kemudian konversikan bilangan hexadesimal tsb ke dalam desimal. Hasilnya sebagai berikut: 6201D76C H menjadi 1644287852. angka-angka ini merupakan nomor kartu sebenarnya yang tertera pada badan kartu yang biasa disebut tag RFID.

2.3. Mikrokontroler R8C/13 Tiny Series (R5F21134FP)

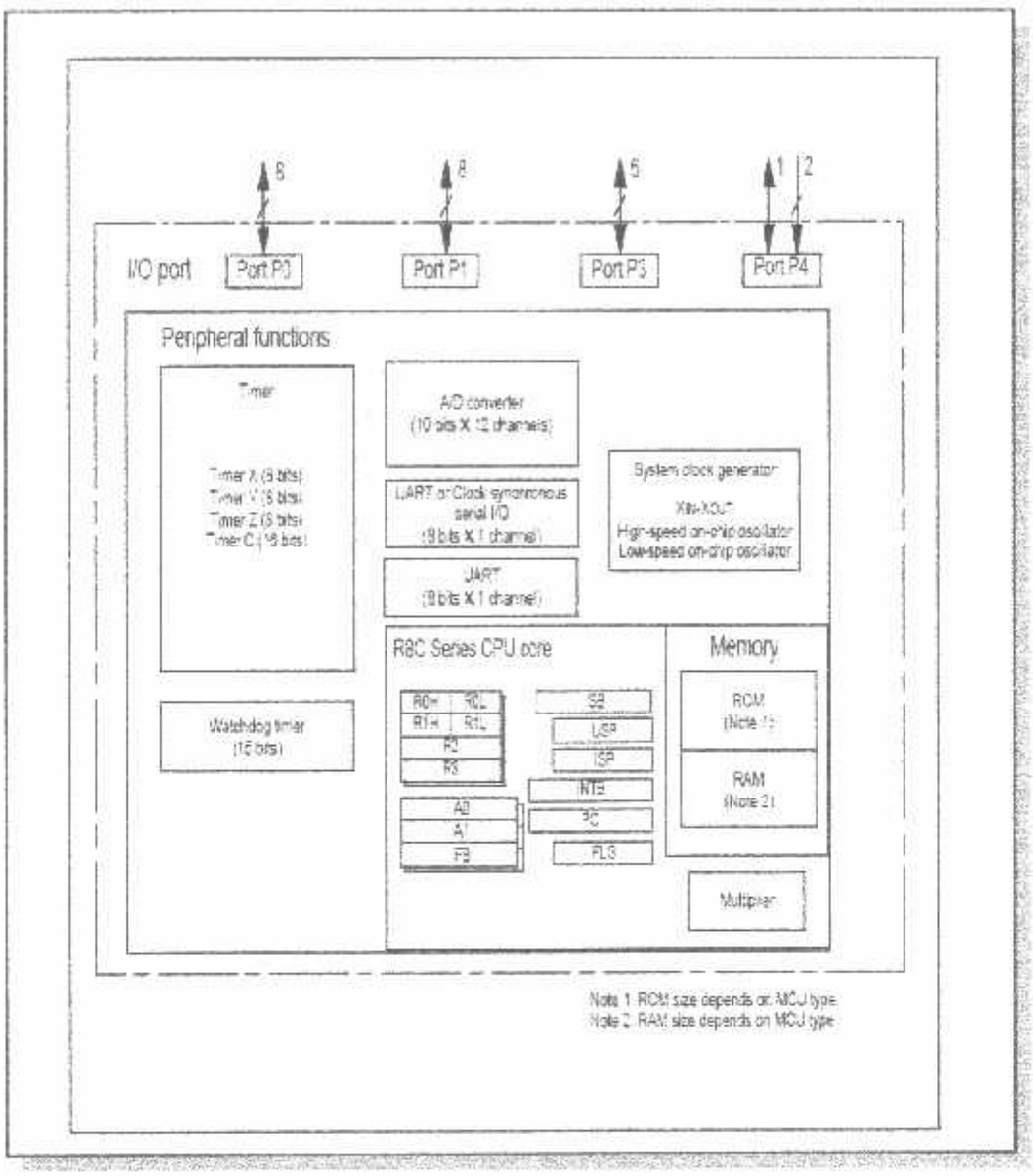
R8C/13 merupakan salah satu mikrokontroler dari buatan RENESAS keluarga M16C yang mempunyai 16 kbyte Flash ROM (*Flash Read Only Memory*) dan 1 kbytes SRAM serta 2x2 kbytes Data Flash, RAM sampai 1 kbyte, 22 bit port I/O (4 buah *port* I/O bit) yang mana tiap pin tersebut dapat diprogram secara paralel dan tersendiri, mempunyai ADC (Analog To Digital Converter) mempunyai tiga buah Timer/Counter 8 bit (Timer X, Y, Z) dan satu buah Timer/Counter 16 bit (Timer C), mempunyai Watchdog Timer, mempunyai power on reset, mempunyai serial I/F (A/Sync), mempunyai On-Chip Debug, serta Oscillator Circuit.

Pada dasarnya mikrokontroler adalah terdiri atas prosesor (CPU), memory (ROM, RAM), perangkat I/O dan peripheral. Mikrokontroler termasuk perangkat yang sudah didesain dalam bentuk *chip* tunggal. Mikrokontroler dikemas dalam satu *chip* (*single chip*). Mikrokontroler didesain dengan instruksi-instruksi lebih luas dan 16 bit instruksi yang digunakan membaca data instruksi dari internal memori ke ALU.

Sebagai suatu sistem kontrol mikrokontroler R8C/13 bila dibandingkan dengan mikroprosesor memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam mikrokontroler sudah terdapat RAM dan ROM sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Secara umum konfigurasi yang dimiliki mikrokontroler R8C/13 adalah sebagai berikut : (Renesas, 2005).

- Sebuah CPU 16 bit dengan menggunakan teknologi dari Renesas.
- Memiliki memory (ROM) 16 Kbyte (2x2 Kbyte data Flash).
- Memiliki memori baca-tulis (RAM) 1 Kbyte.
- Jalur dua arah (*bidirectional*) yang digunakan sebagai saluran masukan atau keluaran.
- Interface Komunikasi Serial UART (*Universal Asynchronous Receiver Transmitter*), UART 0 (Sync/Async) dan UART 1 (hanya Async).
- Empat buah *timer/counter* (3 buah Timer X, Y, Z 8 bit dan Timer C 16 bit).
- Memiliki ADC (Analog To Digital Converter).
- Osilator internal dan rangkaian pewaktu.
- Flash ROM yang besarnya 16 kbyte untuk memori program
- Kemampuan melaksanakan operasi perkalian, pembagian, dan operasi *Boolean*.
- Mampu beroperasi sampai 20 MHz..

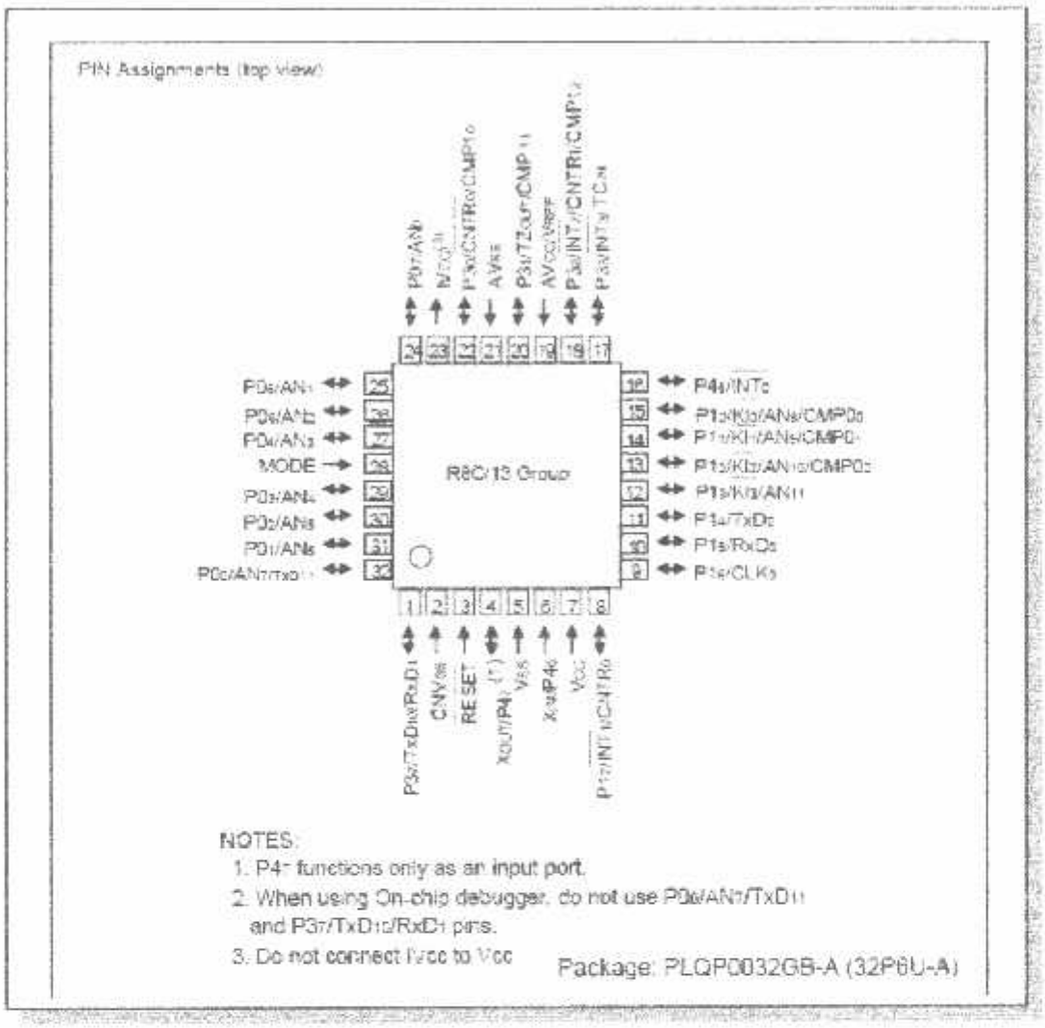
Sedangkan untuk blok diagram diperlihatkan dalam Gambar 2.1



Gambar 2.3 Blok Diagram R8C/13
Sumber: www.renesas.com

2.3.1. Penjelasan Fungsi Pin R8C/13

Mikrokontroler 8C/13 mempunyai 32 pin seperti yang ditunjukkan dalam Gambar 2.2. Fungsi-fungsi pin dijelaskan sebagai berikut:



Gambar 2.4 Konfigurasi Pin R8C/13
Sumber: www.renesas.com

Fungsi kaki-kaki R8C/13 adalah:

- Vcc dan Vss (Pin 5, 7) merupakan power supply input.
- Ivcc (Pin 23) pin ini digunakan untuk menstabilkan internal power supply (dihubungkan kapasitor 0,1uF).
- Avcc, Avss (Pin 19, 21) merupakan power supply input untuk ADC (Analog To Digital Converter).
- $\overline{RESET}$ (Pin 3) merupakan input reset dari MCU.

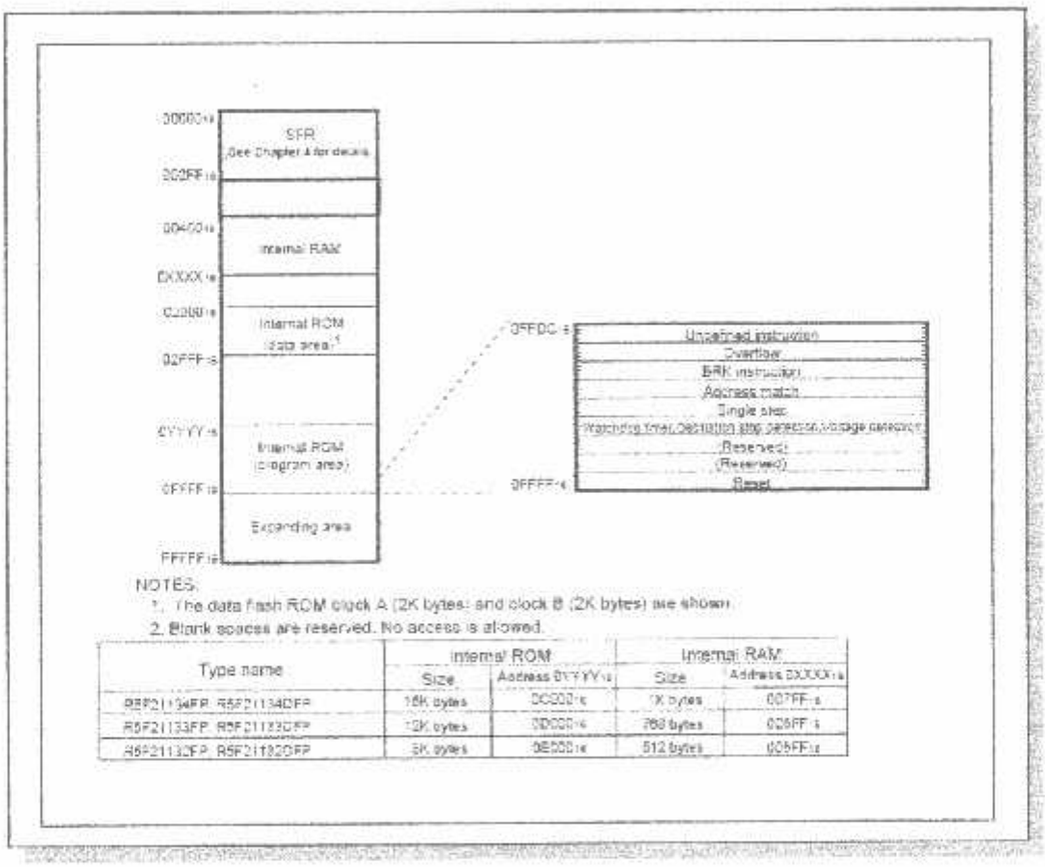
- CNVss (Pin 2) merupakan input untuk dihubungkan ke Vss Melalui resistor[1].
- MODE (Pin 28) merupakan input untuk dihubungkan ke Vcc melalui resistor.
- X_{IN}, X_{OUT} (Pin 6, 4) merupakan main clock input dan output.
- $\overline{INT_0} - \overline{INT_3}$ (Pin 16, 8, 17, 18) merupakan INT interrupt input.
- $\overline{KI_0} - \overline{KI_3}$ (Pin 12..15) merupakan key interrupt input.
- Timer X (Pin $CNTR_0$) merupakan pin timer x I/O.
- Timer X (Pin $\overline{CNTR_0}$) merupakan pin timer x output.
- Timer Y (Pin $CNTR_1$) merupakan pin Timer Y I/O.
- Timer Z (Pin TZ_{OUT}) merupakan pin timer Z output.
- Timer C (Pin TC_{IN}) merupakan pin timer C input.
- Timer C (Pin $CMP0_0$-$CMP0_3$ dan $CMP1_0$-$CMP1_3$) merupakan pin timer C output.
- A/D Converter (Pin AN_0..AN_{11}) merupakan pin input analog untuk A/D konverter.
- *Port* $P0_0..0_7$, $P1_0..1_7$, $P3_0..3_3$, $P3_7$, $P4_5$ (Pin 24..32, Pin 8..15, Pin 17..22, Pin 1, Pin 16), merupakan port yang dapat diset sebagai input atau output *Port Direction Register* (PD).

2.3.2. Organisasi Memori Mikrokontroler R8C/13

Organisasi memori mikrokontroler R8C/13 dapat dibagi menjadi 2 bagian yang berbeda, yaitu ROM/Read Only Memory (Flash) dan RAM.. Lebar jalur

alamat yang dapat diakses adalah 1 Mbytes mulai alamat 00000_{16} sampai dengan $FFFFF_{16}$.

Untuk ROM internal (Program area) ditempatkan pada lower addresss dimulai dari $0FFFF_{16}$. Sedangkan untuk ROM internal (data area) ditempatkan mulai dari address 02000_{16} sampai $02FFF_{16}$. Dan internal RAM ditempatkan pada upper address mulai dari 00400_{16} sampai $007FF_{16}$.



Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R8F21134FP, R8F21134DFP	16K bytes	0C000h	1K bytes	007FFh
R8F21133FP, R8F21133DFP	12K bytes	0D000h	768 bytes	005FFh
R8F21132FP, R8F21132DFP	8K bytes	0E000h	512 bytes	003FFh

Gambar 2.5. Memory Map R8C/13
Sumber: *www.renesas.com*

Special function register (SFR) ditempatkan pada address mulai dari 00000_{16} sampai $002FF_{16}$. Fungsi control register peripheral juga dialokasikan pada address ini.

Tabel 2.2. Spesial Function Register R8C/13

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 [1]	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00₁₆
0006₁₆	System clock control register 0	CM0	01101000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆	High-speed on-chip oscillator control register 0	HRO	00₁₆
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	00XX0000₂
000B₁₆	High-speed on-chip oscillator control register 1	HR1	40₁₆
000C₁₆	Oscillation stop detection register	OCD	00000100₂
000D₁₆	Watchdog timer reset register	WDTR	XX₁₆
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00011111₂
0010₁₆ 0011₁₆ 0012₁₆	Address match interrupt register 0	RMAD0	00₁₆ 00₁₆ X0₁₆
0013₁₆			
0014₁₆ 0015₁₆ 0016₁₆	Address match interrupt register 1	RMAD1	00₁₆ 00₁₆ X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [2]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [2]	VCR2	00₁₆ [3] 10000000₂ [4]
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	INT3 input filter select register	INTCF	XXXXXX00₂
001F₁₆	Voltage detection interrupt register 2	D4INT	00₁₆ [3] 01000012 [4]
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined

Address	Register	Symbol	After reset
0040H			
0041H			
0042H			
0043H			
0044H			
0045H			
0046H			
0047H			
0048H			
0049H			
004AH			
004BH			
004CH			
004DH	Key input interrupt control register	KUPIC	XXXXX000B
004EH	AD conversion interrupt control register	ADIC	XXXXX000B
004FH			
0050H	Compare 1 interrupt control register	CMP1IC	XXXXX000B
0051H	UART0 transmit interrupt control register	S0TIC	XXXXX000B
0052H	UART0 receive interrupt control register	S0RIC	XXXXX000B
0053H	UART1 transmit interrupt control register	S1TIC	XXXXX000B
0054H	UART1 receive interrupt control register	S1RIC	XXXXX000B
0055H	INT2 interrupt control register	INT2IC	XXXXX000B
0056H	Timer X interrupt control register	TXIC	XXXXX000B
0057H	Timer Y interrupt control register	TYIC	XXXXX000B
0058H	Timer Z interrupt control register	TZIC	XXXXX000B
0059H	INT1 interrupt control register	INT1IC	XXXXX000B
005AH	INT3 interrupt control register	INT3IC	XXXXX000B
005BH	Timer C interrupt control register	TCIC	XXXXX000B
005CH	Compare 0 interrupt control register	CMP0IC	XXXXX000B
005DH	INT0 interrupt control register	INT0IC	XX00X000B
005EH			
005FH			
0060H			
0061H			
0062H			
0063H			
0064H			
0065H			
0066H			
0067H			
0068H			
0069H			
006AH			
006BH			
006CH			
006DH			
006EH			
006FH			
0070H			
0071H			
0072H			
0073H			
0074H			
0075H			
0076H			
0077H			
0078H			
0079H			
007AH			
007BH			
007CH			
007DH			
007EH			
007FH			

X : Undefined

NOTES

1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0050H	Timer Y, Z mode register	TYZMR	00H
0051H	Prescaler Y	PREY	FFH
0052H	Timer Y secondary	TYSC	FFH
0053H	Timer Y primary	TYPR	FFH
0054H	Timer Y, Z waveform output control register	PUM	00H
0055H	Prescaler Z	PREZ	FFH
0056H	Timer Z secondary	TZSC	FFH
0057H	Timer Z primary	TZPR	FFH
0058H			
0059H			
005AH	Timer Y, Z output control register	TYZOC	00H
005BH	Timer X mode register	TXMR	00H
005CH	Prescaler X	PREX	FFH
005DH	Timer X register	TX	FFH
005EH	Count source set register	TCSS	00H
005FH			
0060H	Timer C register	TC	00H
0061H			00H
0062H			
0063H			
0064H			
0065H			
0066H	External input enable register	INTEN	00H
0067H			
0068H	Key input enable register	KIEN	00H
0069H			
006AH	Timer C control register 0	TCC0	00H
006BH	Timer C control register 1	TCC1	00H
006CH	Capture, compare 0 register	TM0	00H
006DH			00H
006EH	Compare 1 register	TM1	FFH
006FH			FFH
00A0H	UART0 transmit/receive mode register	U0MR	00H
00A1H	UART0 bit rate register	U0BRG	XXH
00A2H	UART0 transmit buffer register	U0TB	XXH
00A3H			XXH
00A4H	UART0 transmit/receive control register 0	U0C0	00001000B
00A5H	UART0 transmit/receive control register 1	U0C1	00000010B
00A6H	UART0 receive buffer register	U0RB	XXH
00A7H			XXH
00A8H	UART1 transmit/receive mode register	U1MR	00H
00A9H	UART1 bit rate register	U1BRG	XXH
00AAH	UART1 transmit buffer register	U1TB	XXH
00ABH			XXH
00ACH	UART1 transmit/receive control register 0	U1C0	00001000B
00ADH	UART1 transmit/receive control register 1	U1C1	00000010B
00AEH	UART1 receive buffer register	U1RB	XXH
00AFH			XXH
00B0H	UART transmit/receive control register 2	UCON	00H
00B1H			
00B2H			
00B3H			
00B4H			
00B5H			
00B6H			
00B7H			
00B8H			
00B9H			
00BAH			
00BBH			
00BCH			
00BDH			
00BEH			
00BFH			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFFH.

Address	Register	Symbol	After reset
00C0H	AD register	AD	XXH
00C1H			XXH
00C2H			
00C3H			
00C4H			
00C5H			
00C6H			
00C7H			
00C8H			
00C9H			
00CAH			
00CBH			
00CCH			
00CDH			
00CEH			
00CFH			
00D0H			
00D1H			
00D2H			
00D3H			
00D4H	AD control register 2	ADCON2	00H
00D5H			
00D6H	AD control register 0	ADCON0	0000 0XXXB
00D7H	AD control register 1	ADCON1	00H
00D8H			
00D9H			
00DAH			
00DBH			
00DCH			
00DDH			
00DEH			
00DFH			
00E0H	Port P0 register	P0	XXH
00E1H	Port P1 register	P1	XXH
00E2H	Port P0 direction register	PD0	00H
00E3H	Port P1 direction register	PD1	00H
00E4H			
00E5H	Port P3 register	P3	XXH
00E6H			
00E7H	Port P3 direction register	PD3	00H
00E8H	Port P4 register	P4	XXH
00E9H			
00EAH	Port P4 direction register	PD4	00H
00EBH			
00ECH			
00EDH			
00EEH			
00EFH			
00F0H			
00F1H			
00F2H			
00F3H			
00F4H			
00F5H			
00F6H			
00F7H			
00F8H			
00F9H			
00FAH			
00FBH			
00FCH	Pull-up control register 0	PUR0	00XX0000B
00FDH	Pull-up control register 1	PUR1	XXXXXX00B
00FEH	Port P1 drive capacity control register	DRR	00H
00FFH	Timer C output control register	TCOUT	00H

0182H	Flash memory control register 4	FMR4	01000000B
0183H			
0184H	Flash memory control register 1	FMR1	1000000XB
0185H			
0186H	Flash memory control register 0	FMR0	00000001B
0187H			
02FFH	Option function select register (2)	OFS	Note 2

X : undefined

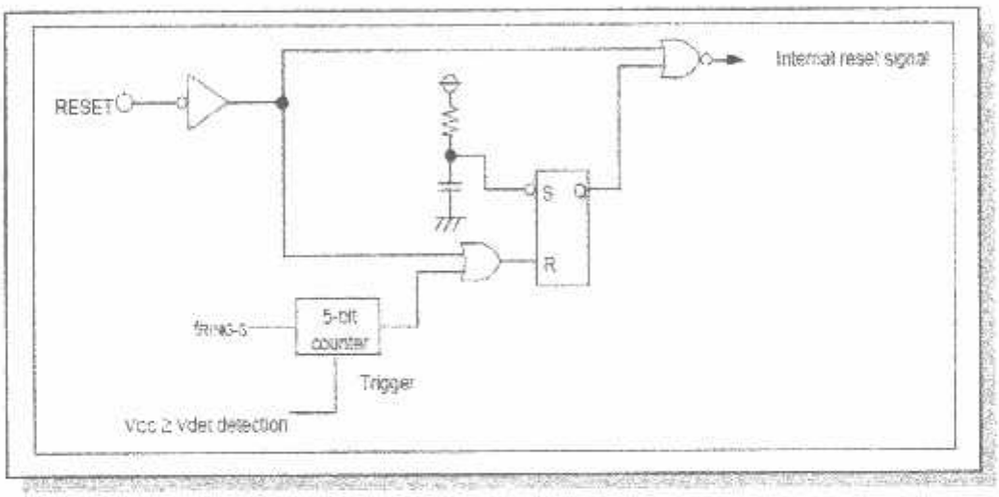
NOTES:

1. The blank areas, 0100H to 0182H and 0188H to 02FFH are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details.

Sumber: www.renesas.com

2.3.3. Reset

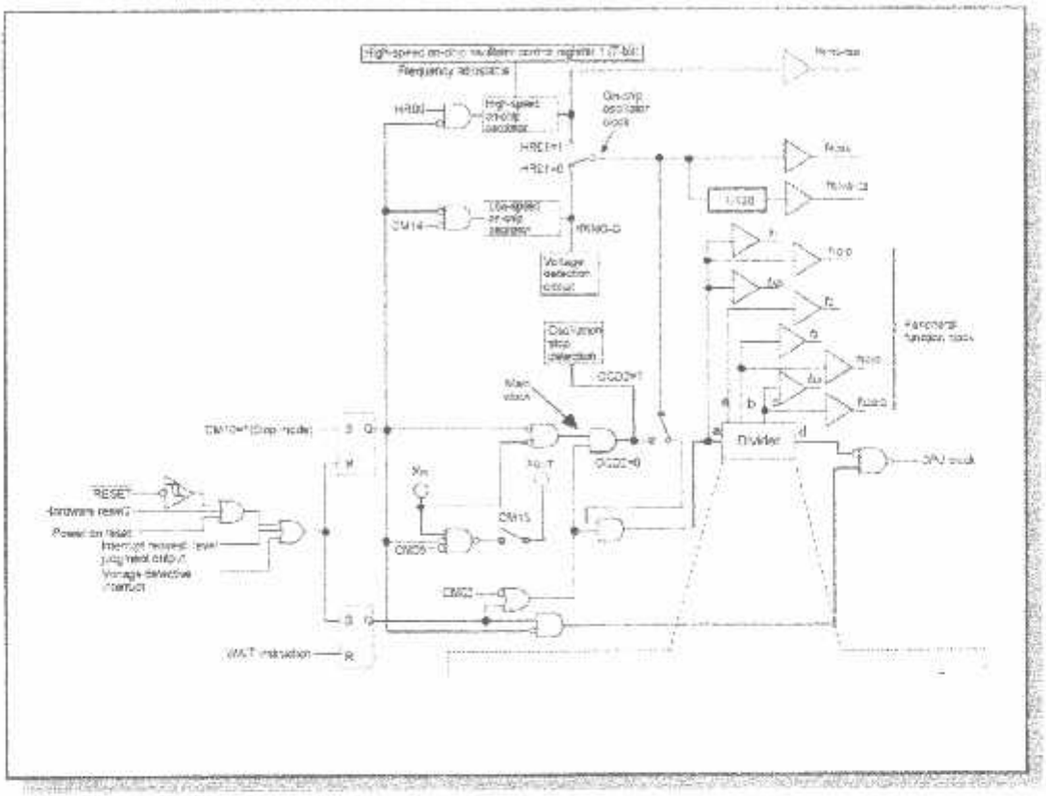
Rangkaian *Power On Reset* diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya dinyalakan. ketika catu daya diaktifkan, rangkaian reset akan menahan logika tinggi pada penyemat RST dengan jangka waktu yang ditentukan oleh lamanya pengosongan muatan kapasitor. Untuk keabsahan reset, logika tinggi harus bertahan lebih lama dari dua siklus mesin ditambah waktu hidup *(start on)* oscilator . Gambar 2.4. menunjukkan rangkaian *Power On Reset.*



Gambar 2.7. Rangkaian Power On Reset
Sumber: www.renesas.com

2.3.4. Pewaktuan

Mikrokontroler R8C/13 memiliki rangkaian osilator internal yang terdiri dari Main Clock Oscillator dan On-Chip Oscillator. Main clock oscillator menggunakan kristal eksternal sampai 20 MHz dan memiliki fitur Clock Stop Detect. Rangkain oscillator ditunjukkan pada Gambar 2.5.



Gambar 2.8. Rangkaian Pewaktuan dengan Osilator Internal

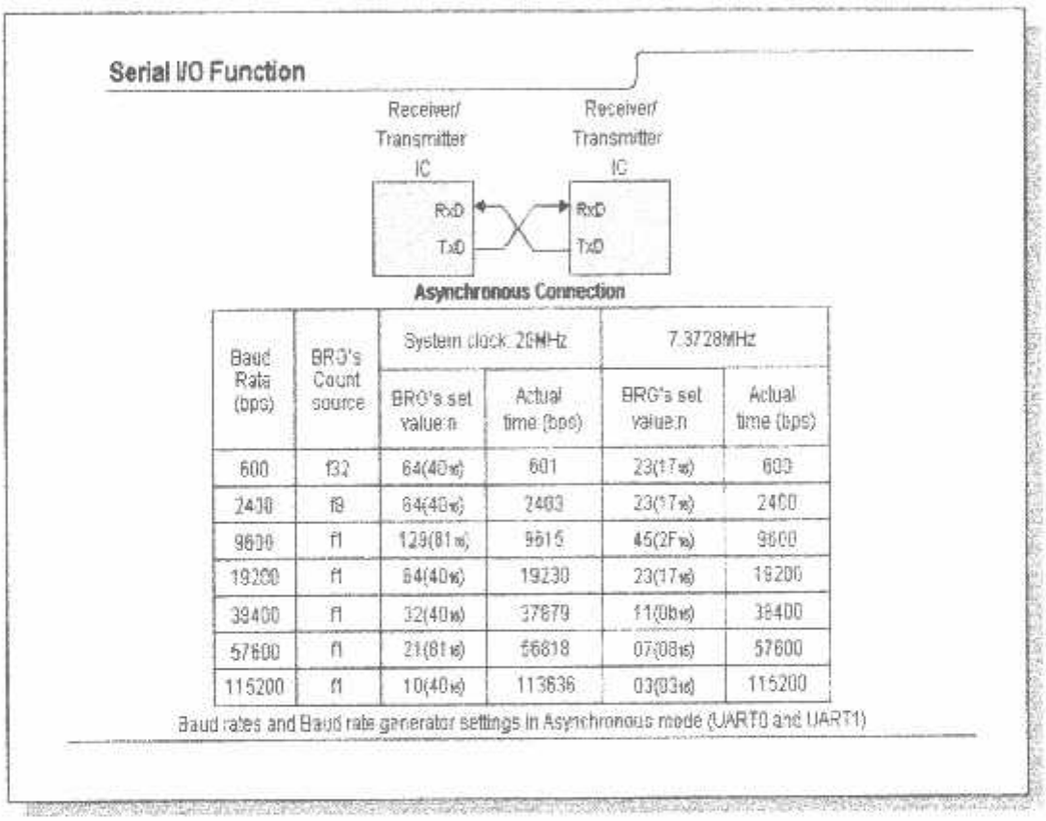
Sumber: *www.renesas.com*

2.3.5. Komunikasi Data Serial

Pengiriman data serial biasanya digunakan untuk jarak yang relatif jauh. Pada port serial R8C/13 dapat digunakan untuk komunikasi data secara sinkron maupun asinkron. Komunikasi data serial sinkron merupakan bentuk komunikasi data serial yang memerlukan sinyal clock untuk sinkronisasi. Sinyal clock tersebut akan tersulut pada setiap bit pengiriman data, sedangkan komunikasi data serial asinkron tidak memerlukan sinyal clock sebagai sinkronisasi. Pengirimannya akan dimulai dari LSB (Least Significant Bit) dan diakhiri oleh MSB (Most Significant Bit).

2.4. *Interface* Komunikasi Serial

R8C/13 mempunyai Serial Interface yang terdiri dari dua channel yaitu UART0 sampai UART1. UART0 mempunyai dua mode yaitu mode pewaktu synchron serial I/O dan mode pewaktu asynchron serial I/O. Sedangkan untuk UART1 hanya mempunyai satu mode yaitu mode pewaktu asynchron serial I/O.



Baud Rate (bps)	BRG's Count source	System clock: 20MHz		7.3728MHz	
		BRG's set value:n	Actual time (bps)	BRG's set value:n	Actual time (bps)
600	f32	64(40H)	601	23(17H)	600
2400	f8	64(40H)	2403	23(17H)	2400
9600	f1	129(81H)	9615	45(2FH)	9600
19200	f1	64(40H)	19230	23(17H)	19200
38400	f1	32(20H)	37879	11(0BH)	38400
57600	f1	21(15H)	56818	07(08H)	57600
115200	f1	10(0AH)	113636	03(03H)	115200

Baud rates and Baud rate generator settings in Asynchronous mode (UART0 and UART1)

Gambar 2.9. Koneksi Asinkron

Sumber: *www.renesas.com*

2.4.1. Komunikasi Serial Antara PC dengan MCU

IC digital, termasuk mikrokontroler, umumnya bekerja pada level tegangan TTL, yang dibuat atas dasar tegangan catu daya +5 Volt. Rangkaian input TTL menganggap tegangan kurang dari 0,8 Volt sebagai level tegangan '0'

dan tegangan lebih dari 2.0 Volt dianggap sebagai level tegangan '1'. Level tegangan ini sering dikatakan sebagai level tegangan TTL. Sedangkan pada PC / *Serial Port* tegangan antara +3 sampai +15 Volt dianggap sebagai level tegangan '0', dan tegangan antara –3 sampai –15 Volt dianggap sebagai level tegangan '1'. Dari perbedaan acuan tegangan tersebut diperlikan RS232 sebagai jembatan untuk menghubungkan antara MCU dengan PC, sehingga *transfer* data dapat dilakukan.

2.4.2. *Interface Unit RS-232*

Dalam komunikasi data komputer terdapat dua terminal (port) komunikasi yaitu *port paralel* (LPT standart) dan port serial (RS – 232 standart) yang masing-masing memiliki spesifikasi yang berbeda. Biasanya standar serial RS – 232 memiliki dua buah terminal yang sering disebut COM 1 dan COM 2.

DTE (*Data Terminal Equipment)* atau terminal data yang melakukan pertukaran data seri dan menggunakan data biner, dapat menggunakan terminal komun ikasi seri RS- 232 yang dibuat oleh EIA (*Electrical industry Association)* dan dikenal dengan standar CCITT V 24. Sebuah DTE adalah perangkat prosesor yang dilengkapi data pararel menjadi serial dan sebaliknya.

Sedang yang dimaksud dengan DCE (*Data Communication Equipment)* adalah perangkat yang mengubah data serial menjadi salah satu bentuk sinyal analog yang dapat ditransformasikan pada saluran transmisi seperti telepon atau radio. Standar RS – 232 ini berisikan karakteristik sinyal listrik, karakteristik mekanik dan cara rangkaian fungsionalnya. Beberapa karakteristik sinyal listrik RS – 232 adalah sebagai berikut :

- Tegangan rangkaian terbuka (*open loop*) tidak boleh lebih dari 25 Volt.

- Keadaan logika "1" (Mark) pada driver ditandai dengan tegangan antara –5 sampai –25 Volt.
- Keadaan logika "0"(Space) pada driver ditandai dengan tegangan antara +5 sampai +25 Volt.
- Slew Rate (perubahan tegangan keluaran perancangan satuan waktu) < 30 V/s. Waktu untuk melewati daerah invalid –3 V hingga +3 V ≤ 1 ms.

Karakteristik mekanik interface ditentukan dengan konektor DB – 25 pin atau DB – 9 pin, dimana tiap-tiap kontak konektor memiliki fungsi tertentu seperti tabel 2-3

Tabel 2-3 Nama Pin dan Keterangan dari Port RS – 232

No pin U/9 pin	**No pin U/25 pin**	**Nama Pin**	**Nama RS-232**	**Keterangan**	**Hub Ke DCE**
	1		AA	Protective Ground	-
3	2	TXD	BA	Transmitted Data	IN
2	3	RXD	BB	Received Data	OUT
7	4	RTS	CA	Request to Send	IN
8	5	CTS	CB	Clear to Send	OUT
6	6	DSR	CC	Data Set Ready	OUT
5	7	GND	AB	Sinyal Ground (Common Return)	-
1	8	CD	CF	Received Line Signal Detector	OUT
	9		-	Received for data testing	-
	10		-	Received for data	-

				testing	
	11		-	Unssigned	-
	12		SCF	Secondary Received Line Signal Detector	OUT
	13		SCB	Secondary Clear to send	OUT
	14		SBA	Secondary Transmitted Data	IN
	15		DB	Transmision Signal Element Timing	OUT
	16		SBB	Secondary Received Data	OUT
	17		DD	Receiver Signal Element Timing	OUT
	18			Unssigned	-
	19	TXD	SCA	Secondary request to send	IN
	20	DTR	CD	Data Terminal Ready	IN
	21		CG	Signal Quality Detector	OUT
9	22		CE	Ring Indicator	OUT
	23		CH/CI	Data Signal Rate Selector	I/O
	24		DA	Transmit Signal Element Timing	IN
	25			Unssigned	-

Fungsi pin DB – 9 RS – 232 adalah :

1. **Data Carrier Detect (DCD)**

   Berguna pada DTE untuk tidak memperbolehkan penerimaan data.

2. **Transmitted Data (TXD)**

Berguna untuk jalur pengiriman data dari DTE ke DCE

3. **Received Data (RXD)**

   Berguna sebagai jalur pengiriman data dari DCE ke DTE

4. **Data Terminal Ready (DTR)**

   Berguna untuk memberitahu DCE bahwa DTE telah aktif dan siap untuk bekerja.

5. **Signal Ground (DSR)**

   Berguna sebagai referensi semua tegangan interface

6. **Data Set Ready (DSR)**

   Bekerja untuk memberitahu DTE bahwa DCE telah aktif dan siap untuk bekerja.

7. **Request to Send (RTS)**

   Bertugas untuk memberitahu DCE bahwa DTE akan mengirimkan data. RTS merupakan sebuah *protokol hardware* yang mendahului pengiriman data DTE ke DCE.

8. **Clear to Send (CTS)**

   Berguna untuk memberitahu DTE bahwa DCE siap untuk menerima data. CTS merupakan sebuah *protokol hardware* yang mendahului pengiriman dari DTE ke DCE.

9. **No Conection (NC)**

   Ditinjau dari proses jabatan (*handshaking)* standar RS-232 yaitu pin-pin DTR, DSR, RTS, CTS, dan CD maka perangkat lunak akan mengaktifkan DTR yang menandakan bahwa komputer siap melakukan transmisi atau

menerima data dan apabila terminal lain juga dihidupkan serta siap menerima/mengirim data, maka terminal tersebut akan mengirimkan sinyal DSR.

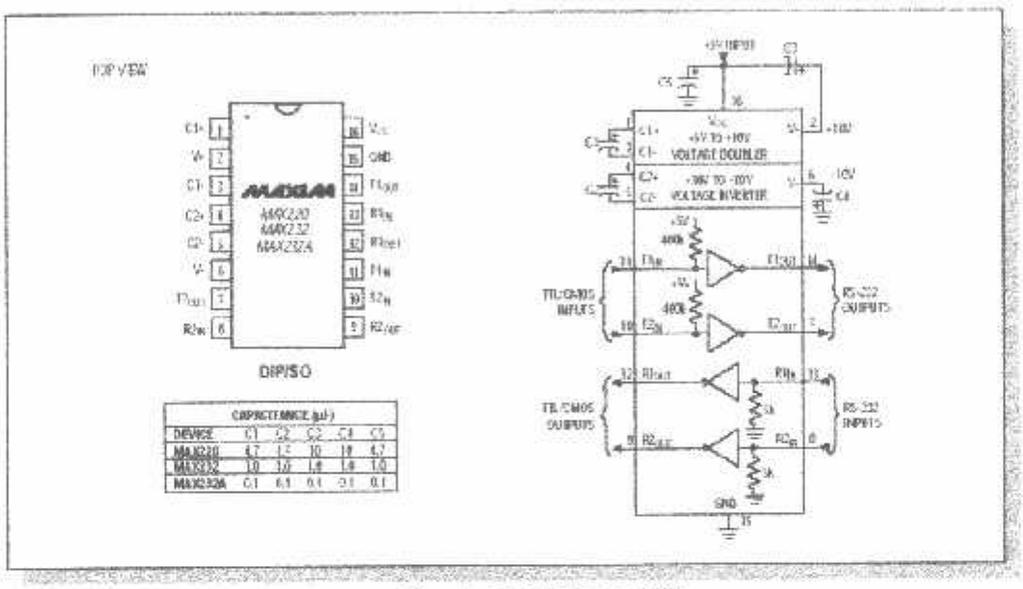
2.4.3. MAX 232 Sebagai Pengubah Tegangan TTL

MAX 232 merupakan pengubah TTL ke level tegangan RS 232. MAX 232 memiliki dua driver mengkonversikan RS 232 ke level TTL, dan dua penerima yang merubah TTL ke RS 232. MAX 232 memiliki kemampuan mengakses data lebih dari 120 Kbps. MAX 232 memiliki 16 pin dan dioperasikan dengan empat buah kapasitor yang memiliki nilai 0,1µF.

RS 232 merupakan salah satu jenis antar muka (interface) dalam proses transfer data antar komputer dalam bentuk serial transfer. RS 232 merupakan singkatan dari Recommbeded Standard number 232. Alat ini dibuat oleh Elektronik Industri Assosiation, untuk interface antara peralatan terminal data dan peralatan komunikasi data, dengan menggunakan data biner serial sebagai data yang ditransmisikan. IC MAX 232 ini mempunyai empat buah bagian konverter yaitu dua buah driver receiver dan dua buah driver transmitter.

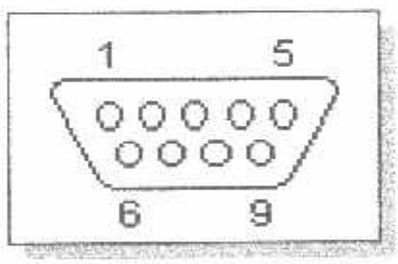
Saluran data pada port seri PC menggunakan standard RS 232, dimana logic 0 (low) dinyatakan sebagai tegangan antara +3 volt sampai +10 volt, dan logic 1 (high) dinyatakan sebagai tegangan antara -3 volt sampai -10 volt. Level tegangan ini tidak sesuai dengan level tegangan yang dipakai pada port seri R8C/13 yang menggunakan standard TTL (Tranastor Transistor Logic), yaitu level tegangan baku dalam rangkaian – rangkaian digital.

Dalam standard TTL, logic 0 (low) dinyatakan sbagai tegangan antara 0 volt sampai 0.8 volt, dan logic 1 (high) dinyatakan sebagai tegangan antara 3.5 volt sampai 5 volt. Untuk dua MCU yang dihubungkan secara serial pada jarak tertentu maka dibutuhkan IC MAX 232 karena level tegangan TTL terlalu kecil untuk ditrasfer.



Gambar 2.10. IC Max 232

Sumber : *Data Sheet, http://www.lookrs232.com*



Gambar 2.11. Konektor DB 9

(Sumber : *http://fly.hiwaay.net/~jfrohwei/tech/null-mod.html*)

Fungsi dari pin-pin yang ada untuk konektor DB 9 adalah sebagai berikut :

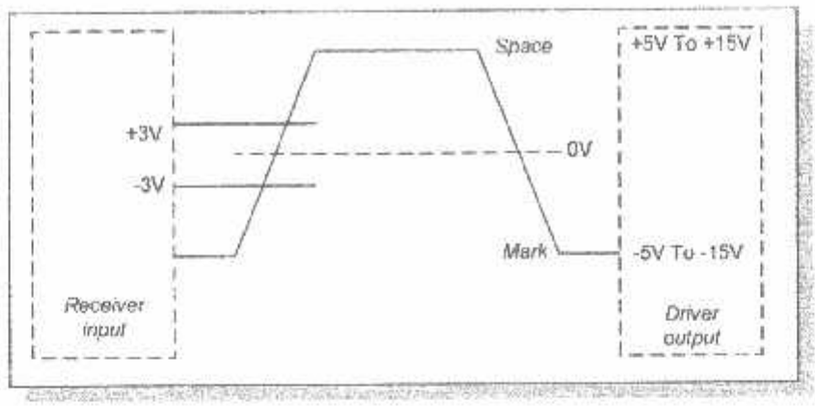
Tabel 2.4. Konfigurasi pin DB 9

EIA 232 (RS 232) Function	PIN
Data Carrier Detect (DCD)	1
Received Data (RxD)	2
Transmitted Data (TxD)	3
Data Terminal Ready (DTR)	4
Sinyal Ground (GND)	5
Data Set Ready (DSR)	6
Request To Send (RTS)	7
Clear To Send (CTS)	8
Ring Indicator (RI)	9

(**Sumber** : B & B Electronics Mfg Co, USA, 2001, halaman 5)

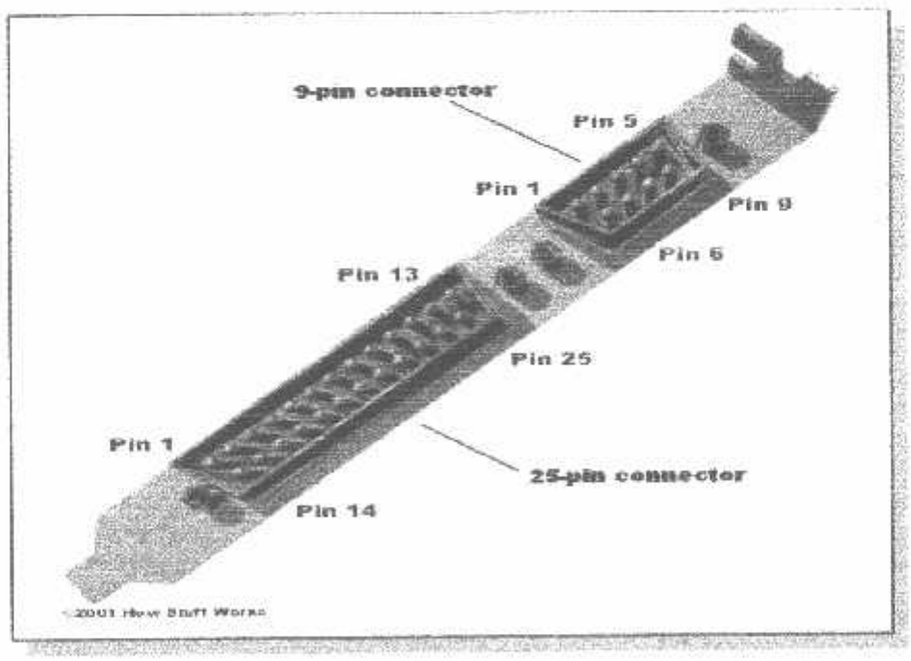
RS-232 merupakan seperangkat alat yang berfungsi sebagai *interface* dalam proses transfer data secara serial. Metode pengiriman secara serial RS-232 adalah asinkron. Pengiriman asinkron berarti tidak membutuhkan pewaktu sebagai sinkronisasi. Dalam pengiriman serial *asinkron*, *clock* tidak dikirimkan, tetapi dikondisikan oleh *timing start bit* yang merupakan isyarat dari sumber ke tujuan untuk mengkodekan adanya pengiriman karakter sudah selesai dikirim.

Karakteristik elektris dari sistem RS-232 adalah mempunyai tegangan keluaran antara –15 Volt sampai dengan +15 Volt. Teganan +5 sampai +15 volt untuk mewakili level rendah (logika '0'/ *spacing*) dan tegangan -5 sampai -15 volt untuk mewakili level tinggi (logika '1'/ *marking*). Hal tersebut seperti ditunjukkan dalam Gambar 2.8.



Gambar 2.12. Level Logika Standar RS-232
Sumber : Dallas Semiconductor, 1998: 2.

Di dalam komputer terdapat fasilitas komunikasi serial yang menggunakan standar RS-232, yaitu terletak pada COM1 dan COM2. Kedua fasilitas ini menggunakan konektor DB9 atau DB25 sebagai penghubung dengan piranti luar. Gambar konektor DB9 seperti terdapat dalam Gambar 2.9.



Gambar 2.13. Konektor DB-9 dan DB-25
Sumber: *www.howstuffworks.com*

Fungsi masing-masing pin pada DB-9 seperti terdapat dalam Tabel 2.3.

Tabel 2.5. Fungsi Pin RS-232 dalam DB-9

Pin	Nama	Fungsi
1	DCD (*Data Carrier Detect*)	Mendeteksi sinyal *carrier* dari modem lain
2	RD (*Receive Data Line*)/ (R_XD)	Pengiriman data serial dari DCE ke DTE
3	TD (*Transmit Data Line*)/(T_XD)	Pengiriman data serial dari DTE ke DCE
4	DTR (*Data Terminal Ready*)	Memberitahu DCE bahwa DTE telah aktif dan siap untuk bekerja
5	*Ground*	Referensi semua tegangan antarmuka
6	DSR (*Data Set Ready*)	Memberitahu DTE bahwa DCE telah aktif dan siap untuk bekerja
7	RTS (*Request To Send*)	Memberitahu DCE bahwa DTE akan mengirim data
8	CTS (*Clear To Send*)	Memberitahu DTE bahwa DCE siap menerima data
9	RI (*Ring Indikator*)	Aktif jika modem menerima sinyal ring pada jalur telepon

Sumber : Ganiadi Gunawan, 1991: 4.

Jalur data (TxD dan RxD) untuk transport data, TxD adalah jalur output pada komputer, data dikirim dari pin ini. Sedangkan RxD adalah penerima untuk komputer, data yang datang akan diterima oleh pin ini. Pin ke empat adalah output (RTS) di mana sebuah sinyal akan diberikan pada alat yang dihubungkan dengan maksud meminta kiriman data. CTS adalah sinyal masukan yang menunggu sinyal dari alat yang terhubung. Ketika alat tersebut menerima sinyal RTS dan bisa menerima data maka ia akan mengirimkan sinyal balik yang merupakan CTS. DTR adalah sinyal keluaran yang memberi tanda bahwa ada alat yang terhubung dan akan mengirimkan data. DSR merupakan sinyal input yang mana jika alat yang terhubung manerima sinyal DTR ia akan memberi sinyal balikkemudian diterima sebagai sinyal DSR.

Spesifikasi RS-232 dapat dilihat dalam Tabel 2.4.

Tabel 2.6. Spesifikasi RS-232

Keistimewaan	Karakteristik
Jenis operasi	*Single ended* (tak seimbang)
Jenis penggerak dan Penerima per jalur	1 *driver* 1 *receiver*
Data *rate* maksimum	20 kbps
Panjang saluran maksimum	50 ft (15 m)
Tegangan keluaran penggerak	±5 - ±15 volt
Sensitivitas penerima	±3 volt

Sumber : ARC Electronics, 2000

2.5. Keypad 4 x 4

Untuk mempermudah pengunaan mikrokontroller sebagai alat proses, maka diperlukan sarana yang dapat menjadi penghubung penggunaan dengan alat kontrol, yaitu sebagai sarana input data yang nantinya akan diolah oleh mikrokontroller.

Peralatan input data yang dapat menunjang mikrokontroller adalah beberapa saklar tekan yang menyatakan angka dan karakter yang disusun berbentuk matrik 4 kolom dan 4 baris dengan total tombol 16 buah. Keypad ini berfungsi untuk memberi masukan nilai derajat langsung ke minimum sistem. kemudian data ditampilkan pada LCD.

Rangkaian ini dapat dianalogikan dengan empat buah kabel terbuka yang disilang dengan empat buah kabel yang lain (diletakan diatasnya). Perlakuan ini akan menyebabkan perolehan 16 titik persilangan. Bila pada suatu titik kabel persilangan itu bersentuhan (salah satu ditekan hingga menyentuh kabel yang lain dibawahnya), maka diasumsikan bahwa tombol keypad pada posisi bersilangan tersebut ditekan. Berikut ini adalah gambar konfigurasi tombol Keypad :

1	2	3	COR
4	5	6	MEN
7	8	9	UP
CAN	0	ENT	DOWN

Gambar 2.14. Konfigurasi Tombol Keypad

2.6. LCD (*Liquid Crystal Display*)

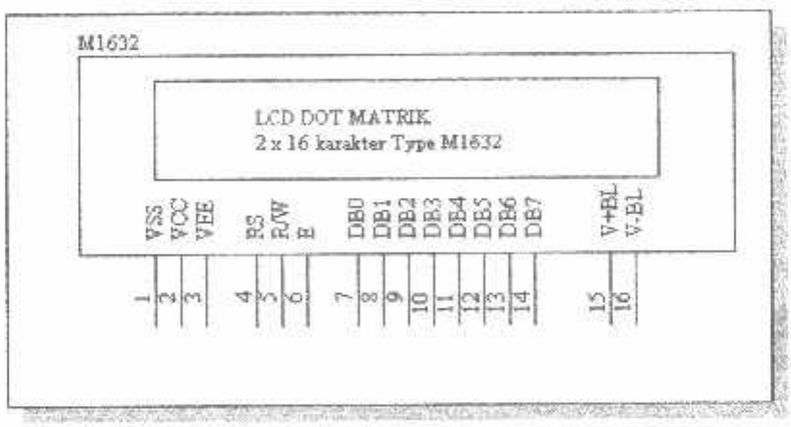
Liquid Crystal Display atau LCD merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistrik), komponen pembangkit cahaya (light emiting) dan komponen-komponen yang akan mengubah sinar. LCD terbuat dari bahan kristal cair yang merupakan suatu komponen organik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

Sel kristal cair terdiri dari selapis bahan kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan kristal cair (*liquid crystal)* yang tembus cahaya. Permukaan luar dari masing-masing keping kaca mempunyai lapisan penghantar tembus cahaya seperti oxida timah (*tin oxide)* atau oxida indium (*indium oxide)*. Sel mempunyai ketebalan sekitar 1 x 10^{-5} meter dan diisi dengan kristal cair.

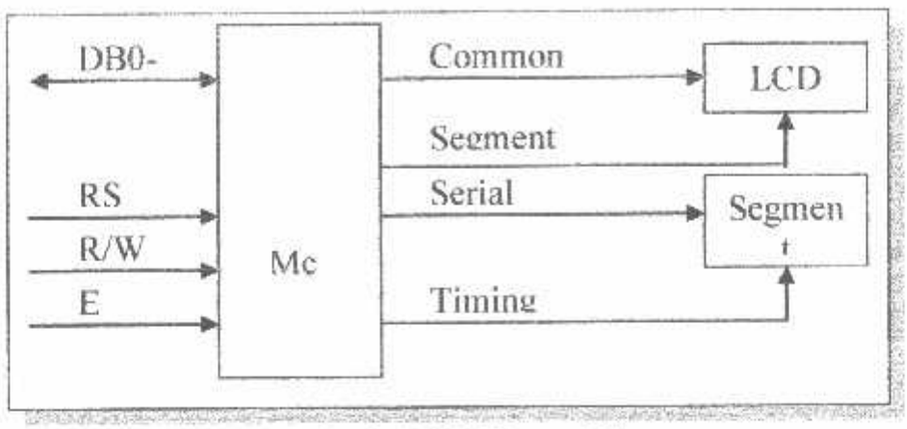
Karena sel-sel kristal cair merefleksikan cahaya dan bukan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah.

Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (3 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 - 300 μA). LCD seringkali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain, yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632, suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCII jika padanya diberikan input ASCII. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisasi yang telah ditentukan oleh pabrik pembuatnya. Timing penganalisasian sangat dipertimbangkan, karena jika meleset sampai ordo *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.



Gambar 2.15. Konfigurasi Kaki LCD
Sumber: *Liquid Crystal Display Module M1632 User Manual*



Gambar 2.16. Blok Diagram LCD

Sumber: *Liquid Crystal Display Module M1632 User Manual*

Adapun karakteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkitan karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 bit
- Dapat dirangkai dengan MPU 8 bit/4 bit
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi instruksi antara lain *display on/off, Cursor on/off, display* karakter *blink, cursor shift* dan *display shift*
- Memiliki rangkaian osilator sendiri
- Catu tegangan tunggal yaitu ± 5 V
- Memiliki rangkaian reset otomatis pada catu daya yang dihidupkan
- Temperatur operasi 0^0 - 50^0

LCD memiliki 16 pin yang masing-masing mempunyai fungsi sebagai berikut :

Tabel 2.7. Fungsi Tiap Pin LCD

No. Pin	Simbol	Level	Fungsi	
1	V_{SS}	-	Power Supply	0 V (GND)
2	V_{CC}	-		5 V ± 10%
3	V_{DD}	-		For LCD Drive
4	RS	H/L	Sinyal seleksi register H ; Data Input [register data (write/read)] L ; Instruction Input [register instruksi (write), busy flag dan address counter (read)]	
5	R/W	H/L	H ; Read L ; Write	
6	E	H	Enable Signal [sinyal penanda mulai operasi, aktif saat operasi write atau read]	
7	DB0	H/L	4 bit bus data lower 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 bit bus data upper 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai busy flag	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 - 4,2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

Sumber: Liquid Crystal Display Module M1632 User Manual

2.6.1. Instruksi Operasi

Tabel 2.8. Instruksi Pada LCD

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	1	*	*	*
CG RAM Address Set	0	0	0	1	A_{CG}					
DD RAM Address Set	0	0	1	A_{DD}						
BF/Address Read	0	1	BF	AC						
Data Write to CG RAM	1	0	Write Data							
Data Read from CG RAM	1	1	Read Data							

*Invalid Bit
A_{CG} ; CG RAM Address
A_{DD} ; DD RAM Address

Sumber: Liquid Crystal Display Module M1632 User Manual

2.6.2. Operasi Dasar

- Register

  Kontrol dari LCD memiliki 2 buah register 8 bit yaitu register instruksi (IR) dan register data (DR). IR memiliki instruksi seperti display, clear, cursor shift dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM dan CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Tabel 2.9. Pemilihan Register Pada LCD

RS	RW	Operasi
0	0	Seleksi IR, IR Write Display Clear
0	1	Busy Flag (DB7), @ Counter (DB0-DB7) Read
1	0	Seleksi DR, DR Write
1	1	Seleksi DR, DR Read

Sumber: Liquid Crystal Display Module M1632 User Manual

- Busy Flag

  Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. Register seleksi sinyal akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja internal dan instruksi tidak akan dapat diterima, oleh karena itu status dari flag harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- Address Counter (AC)

  AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat Ac diberikan lewat register instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari Entry Mode Set.

- Display Data RAM

  Pada LCD, masing-masing line memiliki range alamat tersendiri. Alamat itu diekspresikan dengan bilangan hexadesimal. Untuk line 1 range alamat berkisar antara 40_H-$4F_H$.

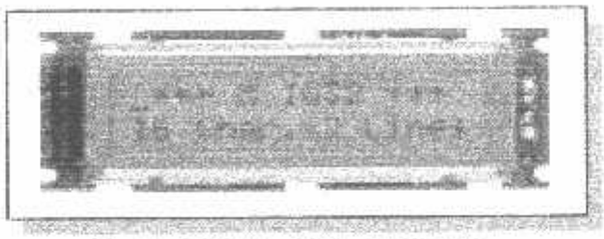
- Character Generator ROM (CG ROM)

CG ROM memiliki tipe dot matrik 5x7, dimana pada LCD telah tersedian ROM sebagai pembangkit karakter dalam kode ASCII.

- Character Generator RAM (CG RAM)

  CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

Adapun bentuk fsik dari LCD M1632 adalah pada gambar berikut :

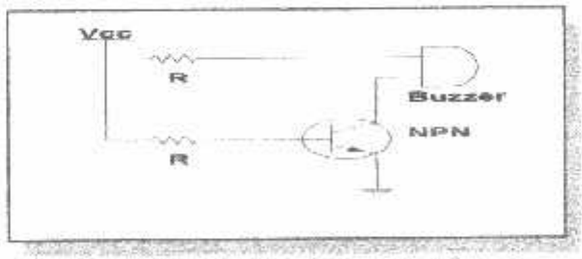


Gambar 2.17. Liquid Crystal Display

Sumber: *Liquid Crystal Display Module M1632 User Manual*

2.7 Buzzer

Perangkat *Buzzer* digunakan untuk menghasilkan bunyi, merupakan komponen resonator *piezoelectric* yang digunakan untuk mengadakan isyarat terdengar sebagai indikator. Buzzer akan aktif dengan cara mengeluarkan sinyal suara (berbunyi) dengan lama waktu sesuai dengan perencanaan nanti.



Gambar 2.18. Rangkaian Driver Buzzer

Sumber : 303 Rangkaian Elektronika, 1997 : 278

2.8. Bahasa Pemrograman Borland Delphi

Delphi adalah perangkat lunak untuk menyusun program aplikasi yang berdasarkan pada bahasa pemrograman bahasa *pascal* dan bekerja dalam lingkungan sistem operasi *Windows*. Dengan Delphi diperoleh kemudahan dalm menyusun program aplikasi, karena Delphi menggunakan komponen-komponen yang akan menghemat penulisan program dengan fasilitas *VCL (Visual Component Library)*.

Dalam pembuatan sebuah program, *Delphi* menggunakan sistem yang disebut *RAD (Rapid Aplication Development)*. Sistem ini memanfaatkan bahasa pemrograman visual yang membuat seorang programmer lebih mudah mendesain tampilan program (*User Interface*. Cara ini bermanfaat untuk membuat program yang bekerja pada sistem *Windows* yang memang tampilan layarnya lebih rumit (sekaligus dapat dilihat dengan indah) dibanding dengan sistem DOS.

Aplikasi dalam tatanan *GUI (Graphical User Interface)* yaitu karakter program aplikasi yang menggunakan sarana perantara grafis dapat dibentuk dengan Delphi. Seperti kotak dialog (*dialog box*), tombol (*button. menu*) dan lain sebagainya. Contoh program GUI adalah program-program *Windows*. Dengan *Delphi* sebuah *Windows* yang mengandung tombol-tombol, kotak cek, tombol pilihan panel dan komponen lainnya dapat dengan mudah diciptakan.

2.8.1. IDE (*Integrated Development Environment*) Delphi

IDE adalah suatu lingkungan dimana sebuah tools yang diperlukan untuk desain, menjalankan dan mengetes sebuah aplikasi disajikan dan terhubung

dengan baik sehimgga memudahkan pengembangan program. Pada *Delphi* terdiri dari *main Windows, Component Palette, Toolbar, Form designer, Code Editor, Code Explorer.* Intergrasi ini memberikan kemudahan dalam mengembangkan aplikasi yang kompleks.

- **Main Windows (jendela utama)**

  Main Widows adalah bagian utama dari IDE. *Main Windows* mempunyai semua fungsi utama dari program-program Windows lainnya. Main Windows dibagi tiga yaitu menu utama, toolbar, dan component palette.

  Menu utama. Seperti program *Windows* lainnya, menu utama dipakai untuk membuat dan menyimpan file memanggil *wziard*, menampilkan jendela lain, mengubah option dan lain sebagainya setiap pilihan pada menu juga dapat dipanggil dengan sebuah tombol pada *toolbar*.

  Toolbar. Beberapa operasi pada menu utama dapat dilakukan melalui *toolbar*. Setiap tombol pada toolbar mempunyai sebuah *tooltip* yang berisi informasi mengenai fungsi dari tombol tersebut. Selain *component palette*, ada 5 *toolbar* terpisah yaitu *debug, desktop, standart, view, dan custom.*

  Component Palette adalah toolbar dengan ketinggian ganda, yaitu berisi page kontrol dengan semua komponennnya. Urutan dan

tampilan dari page dan komponen pada komponen palette dapat diatur dengan klik kanan atau dengan memilih menu component configure component dari menu utama.

- **Form designer**

Diawali dengan jendela kosong yang memungkinkan untuk merancang aplikasi *Windows*. Dari sini dapat ditentukan tampilan aplikasi sesuai dengan yang diingnkan. Berinteraksi dengan *form designer* dengan cara memilih komponen *palette* dan meletakkannya ke dalam *form*, posisi dan ukuran dapat diubah-ubah dengan menggunakan *mouse*. Untuk mengubah tampilan dan perilaku komponen maka digunakan *object inspector* dan *code editor*.

- **Object Editor**

Object Editor terdiri dari dua tab yaitu *tab properties* dan *tab events*. *Tab properties* memberi fasilitas untuk melihat dan mengubah property dari setiap item. Klik pada sebuah form kosong, dan perhatikan atribut-atribut yang ada. Jika terdapat tanda + disamping property maka property tersebut berarti mempunyai *sub property*. Contohnya *property font*, jika diklik ganda pada *property font* maka akan ditampilkan *sub property*nya seperti color, height,name dan lain-lain. *Tab Event* berisi event-event yang dapat direspon oleh sebuah obyek. Klik tab event disebelah kanan tab properties. Misalnya ingin

sesuatu dikerjakan pada saat form ditutup, maka tindakan tersebut (berupa sebuah procedure) pada *Onclose*.

- **Struktur Menu Delphi**

Struktur menu Delphi memberikan tools untuk mengakses lingkungan Delphi.

➢ **File**

Menu file adalah menu paling penting dan akan dijabarkan pada bagian berikut:

New. Digunakan untuk memulai obyek baru.

New Application. Dengan memilih menu ini, berarti akan membuat project baru. Jika belum membuka sebuah *project* atau *object* yang dibuka sudah disimpan ke disk. *Delphi* akan menutup *project* tersebut dan akan membuat *project* baru, termasuk membuat jendela *editor* baru dengan nama file UNIT.PAS, *form baru* (form 1) dan menampilkan *object inspector*.

New Form. Menu ini dipakai untuk membuat form baru.

New frame. Untuk membuat frame kosong dan menambahkannya ke dalam project.

Open. Menyatakan pada *Delphi* bahwa akan dibuka sebuah object dapat berupa sebuah program atau seluruh *project*.

Open Project. Untuk membuka sebuah *project*.

Reopen. Menu ini dipakai untuk membuka *object favorit* yang sudah pernah dibuka.

Save. Menu ini dipakai untuk menyimpan *module* yang sedang aktif.

Save as. Dipakai untuk menyimpan *module* dengan nama lain.

Save project as. Menu ini dipakai untuk menyimpan project dengan nama baru.

Save all. Menyimpan sebuah object yang dibuka.

Close. Untuk menutup module program dengan formnya. Jika module tersebut belum disimpan, saat menutup maka Delphi akan menanyakan apakah modul tersebut akan disimpan.

Close all. Menutup project.

Use Unit. Delphi akan menambahkan *klauda uses* pada program yang dibuat. Artinya sebuah unit akan dipakai dalam project.

Print. Mencetak item Delphi yang telah dipilih.

Exit. Keluar dari aplikasi Delphi.

- **Edit**

Dipakai untuk menyuting program.

- **Search**

  Dipakai untuk mencari dan mengganti kata-kata pada saat menyuting program.

- **View**

  Dipakai untuk menampilkan atau menyembunyikan jendela-jendela tertentu, misalnya object inspector, code explorer, debug dan lain-lain.

- **Project**

  Dipakai untuk mengelola project. Form dapay ditambah dan sibuang dari object, mengkompilasi project dan lain-lain.

- **Run**

  Menu ini dipakai untuk menjalankan program dan memantau jalannya program. Pada saat di run, apabila terjadi salah tulis akan dapat diketahui.

- **Component**

  Dengan menu ini komponen baru dapat ditambah atau diinstal.

BAB III

PERENCANAN DAN PEMBUATAN ALAT

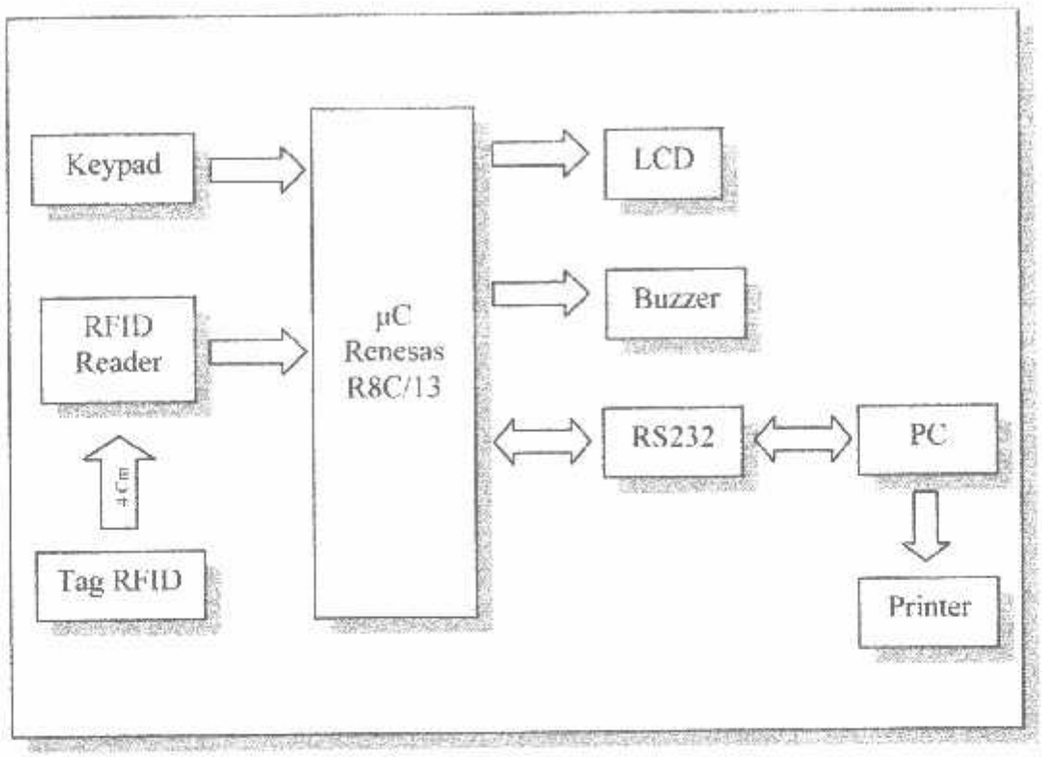
Dalam perancangan alat ini dapat dibagi menjadi dua bagian yang terdiri atas perancangan perangkat keras dan perancangan perangkat lunak yang mendukung sistem kerja alat ini.

Pada perancangan perangkat keras meliputi perancangan diagram blok sistem, perancangan rangkaian *RFID*, mikrokontroler R8C/13, keypad, buzzer, RS232 sebagai penghubung ke PC serta display LCD. Sedangkan perancangan perangkat lunaknya, menjelaskan perangkat lunak yang digunakan untuk menjalankan sistem.

Dalam perencanaan ini dilakukan secara bertahap untuk memudahkan dalam menganalisis setiap bagiannya maupun dalam sistem keseluruhan. Perencanaan dan pembuatan sistem ini terdiri atas dua perencanaan utama, yaitu perencanaan perangkat keras dan perencanaan perangkat lunak, disamping itu aspek lainnya yang juga perlu dijelaskan dalam pembahasan bab ini seperti penentuan spesifikasi atas sistem yang dirancang dalam blok diagram dan prinsip kerja sistem.

3.1. Blok Diagram

Adapun diagram blok dari perancangan alat ini adalah sebagai berikut:



Gambar 3.1 Blok Diagram Sistem

Sumber: Perancangan

3.2. Cara Kerja Rangkaian

Pada dasarnya prinsip kerja dari alat ini adalah mendeteksi identitas pelanggan warnet, yang meliputi nama pelanggan, nomor ID pelanggan, pin atau password dari pelanggan, dan informasi lain yang memungkinkan perlu sebagai informasi tentang identitas lain yang ada.

Cara kerja alat ini diawali dari tag RFID yang memancarkan gelombang radio. Pada saat gelombang radio melalui medan yang dihasilkan oleh RFID Reader, tag akan terdeteksi dan mentransmisikan informasi yang ada pada tag kepada reader. Informasi tersebut akan diterjemahkan oleh mikrokontroler

R8C/13 sehingga data yang ada pada PC dapat ditampilkan pada display untuk dibaca.

Pada alat ini keypad atau tombol masukan berfungsi untuk memasukkan kata kunci yang telah disediakan untuk mengidentifikasi member. Misalkan masukan yang diberikan pada keypad angka 12345, maka pendeteksian hanya berlaku untuk member yang mempunyai ID atau pin 12345. Dan apabila saldo dari member yang mempunyai ID atau pin 12345 tidak mencukupi atau dibawah saldo minimal maka buzzer akan berbunyi.

3.3. Spesifikasi Alat

Perancangan alat ini mempunyai beberapa spesifikasi sebagai berikut:

1. Menggunakan RFID sebagai komponen yang digunakan untuk mengidentifikasi obyek dengan frekuensi transmisi radio.
2. Menggunakan mikrokontroler sebagai pengolah data dan pengontrol keseluruhan kinerja system.
3. Menggunakan PC yang digunaan untuk menyimpan data base pelanggan serta pengolahan data berupa laporan bulanan.
4. *Keypad* yang digunakan sebagai masukan perintah pencarian pin atau password yang dikehendaki oleh pemakai alat.
5. LCD yang digunakan untuk melihat secara *visual* tentang informasi identitas pelanggan yang terdeteksi.
6. Rangkaian RS-232 sebagai penjembatan antara mikrokontroler dengan PC.

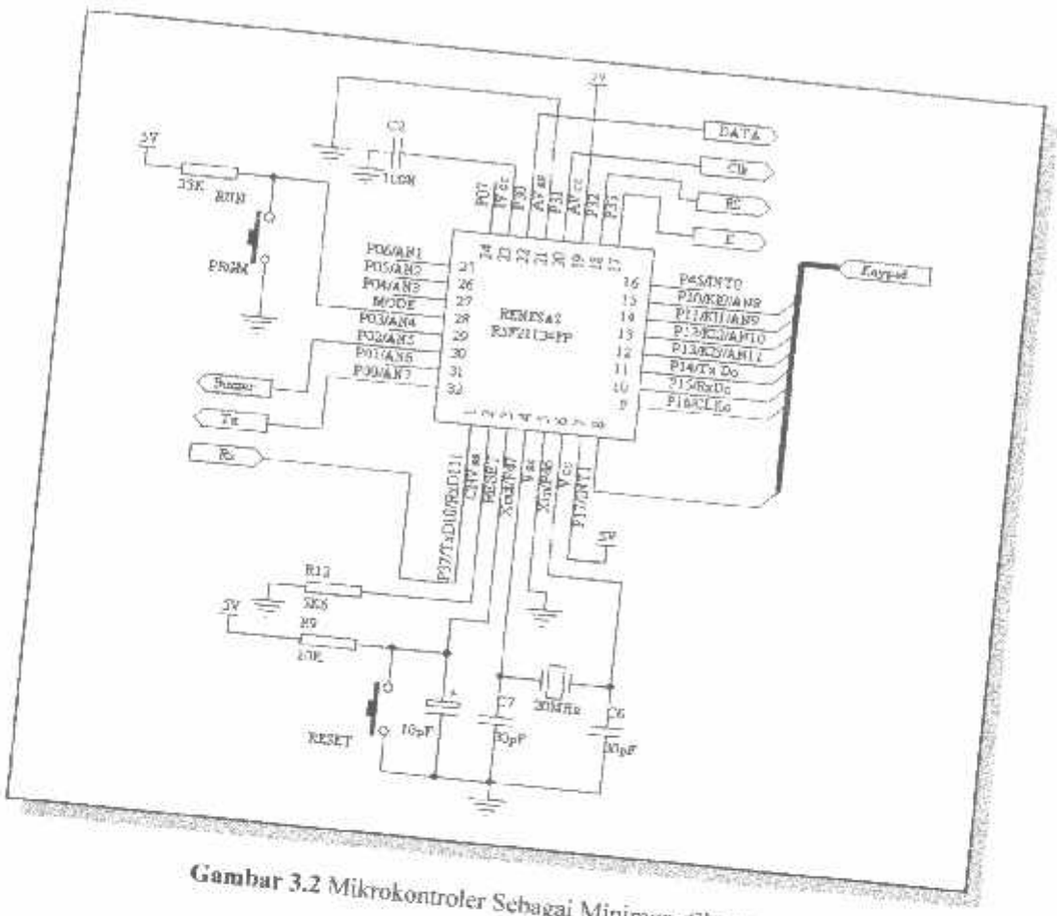
7. Perangkat lunak *(software)* berupa bahasa pemrograman Delphi.

3.4. Perangkat Keras

Perangkat keras yang digunakan dalam sistem ini terdiri atas beberapa bagian yaitu:

3.4.1. Mikrokontroler R8C/13 Sebagai Minimum Sistem

Rangkaian minimum dari mikrokontroler R8C/13 terdiri dari 3 kapasitor, 1 IC mikrokontroler, 1 resistor, dan 1 kristal. Dengan rangkaian yang sederhana ini penulis membuat mikrokontroler sebagai sistem minimum menjadi pengontrol alat, disamping itu rangkaian ini dapat dibuat bermacam-macam alat dengan menambah sedikit komponen tambahan lainnya. Dari rangkaian tersebut yang berpengaruh terhadap kecepatan proses menjalankan program adalah kristal. Adapun rangkaiannya ditunjukkan seperti gambar berikut ini:



Gambar 3.2 Mikrokontroler Sebagai Minimum Sistem

Sumber: Perancangan

Agar sebuah mikrokontroler dapat bekerja sebagai pengontrol, maka kaki-kaki/*port* mikrokontroler dihubungkan dalam rangkaian-rangkaian eksternal. Dalam perancangan ini, *port* yang digunakan adalah sebagai berikut:

1. *Port* 1 sebagai *port* input, yaitu digunakan oleh mirokontroler untuk menerima data dari keypad.
2. *Port* 3 sebagai input serta output dari dua jalur yang berbeda, yaitu:
   a. *Port* $3_{.0}$ - $3_{.3}$ mikrokontroler yang dihubungkan sebagai output ke LCD untuk menampilkan data berupa informasi.

b. *Port* 3_7 (RxD) digunakan sebagai *port* Rx serial *input*, *port* ini digunakan oleh mikrokontroler untuk menerima data dari RFID *reader* dan komputer

3. Port 0 sebagai input dan output dari dua jalur yang berbeda yaitu:

a. *Port* 0_2 sebagai output dari mikrokontroler yang dihubungkan ke Buzzer

b. *Port* 0_0 (TxD) digunakan untuk *port* Tx serial *output*, *port* ini digunakan oleh mikrokontroler untuk mengirim data serial pada komputer.

4. X_{IN} dan X_{OUT} digunakan sebagai input dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri dari kristal osilator 20 MHz, kapasitor C1 dan C2 yang masing-masing bernilai 30 pF, akan membangkitkan pulsa *clock* yang menjadi penggerak bagi seluruh operasi internal MCU (aplication Note R8C/13 In-Circuit programing).

5. V_{CC} dihubungkan dengan tegangan sebesar +5V sesuai dengan tegangan operasi *chip* tunggal yang diizinkan dalam *data sheet*.

6. GND dihubungkan ke *ground* catu daya.

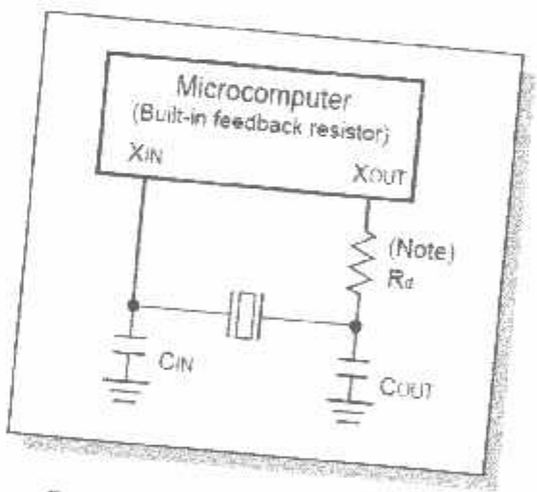
7. Reset digunakan untuk mereset program kontrol MCU, dimana MCU memiliki masukan aktif *high*.

Sebagai pewaktuan R8C/13 menggunakan pin X_{IN} dan X_{OUT} sebagai masukan dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri atas osilator 20 MHz, kapasitor C_1 dan C_2 yang masing-masing bernilai 30 pF yang

akan membangkitkan pulsa *clock* yang digunakan sebagai penggerak bagi sejumlah operasi internal CPU.

Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini menggunakan osilator internal yang telah tersedia dalam *chip* R8C/13. Untuk menentukan frekuensi osilatornya cukup dengan menghubungkan kristal dalam *port* 4_6 (X_{IN}) dan *port* 4_7 (X_{OUT}) serta dua buah kapasitor ke *ground*.

Besarnya kapasitansinya disesuaikan dengan spesifikasi dalam lembar data R8C/13 yaitu 30 pF. Kristal yang digunakan adalah 20 MHz. Dalam Gambar 4.5 memperlihatkan rangkaian *clock* yang direncanakan.



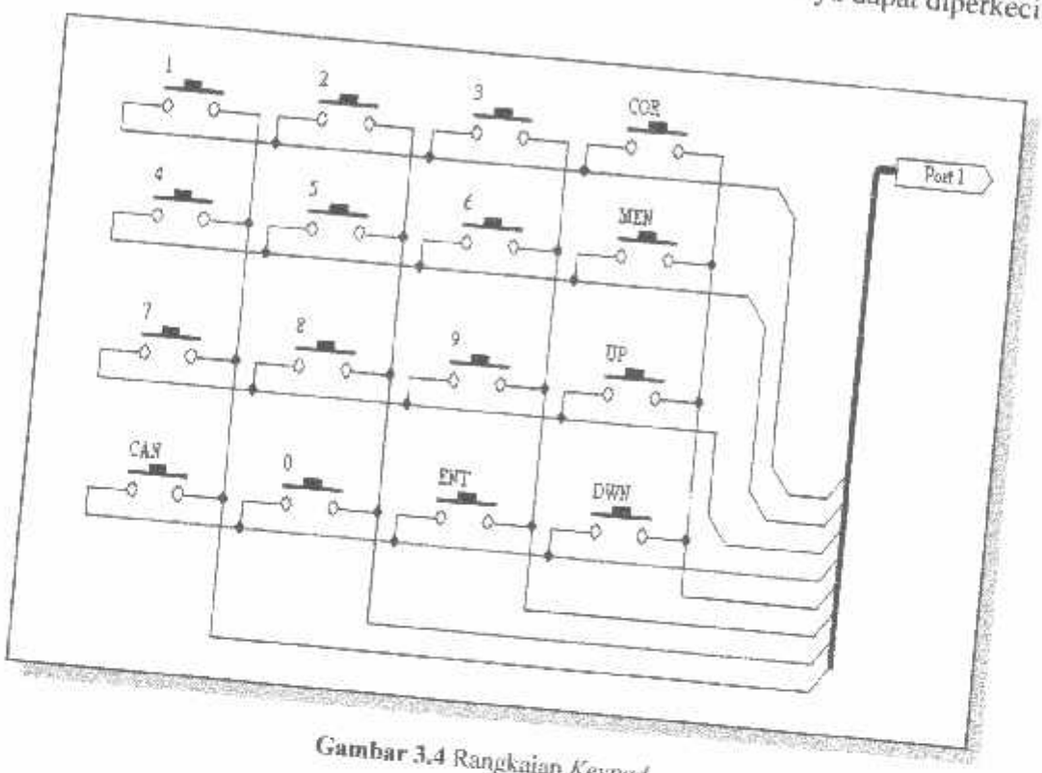
Gambar 3.3 Rangkaian *Clock*

Sumber: Perancangan

3.4.2. Tombol Masukan (Keypad)

Tombol masukan biasa disebut juga dengan *keypad*, pada alat ini *keypad* tersebut difungsikan untuk memberikan masukan data melalui tombol-tombol yang terdapat pada papan *keypad* tersebut. *Keypad* ini berfungsi untuk

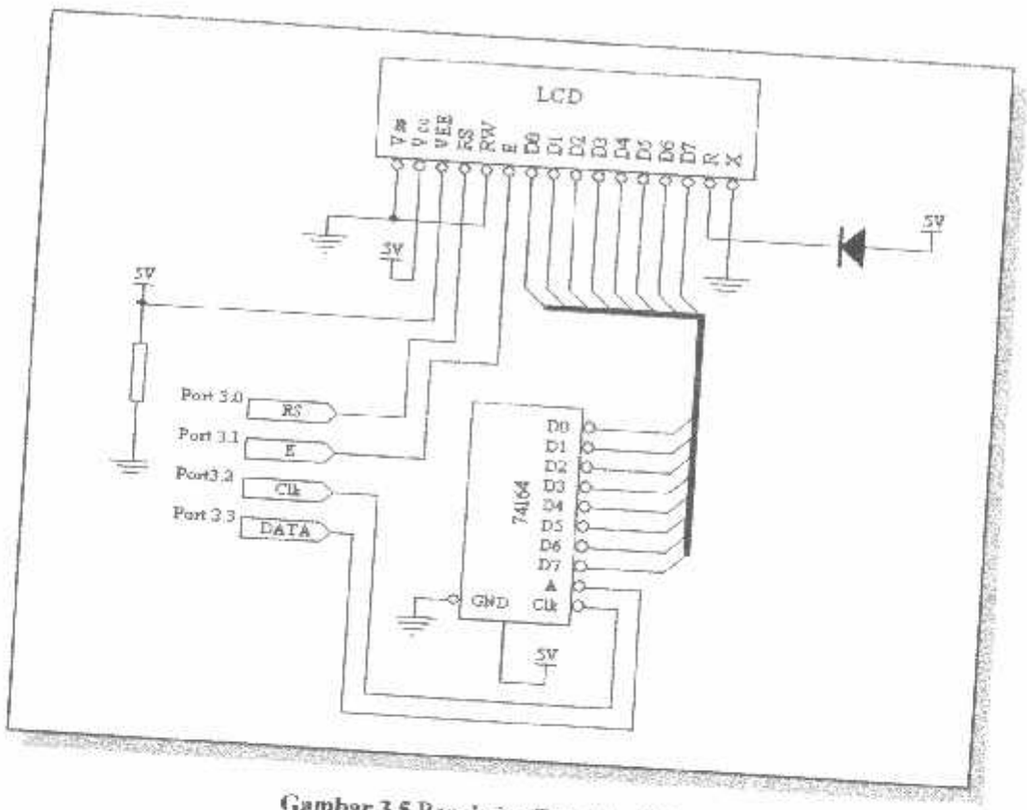
menterjemahkan penekanan pada salah satu tombol kedalam bentuk biner. Sehingga jumlah jalur yang akan masuk ke rangkaian berikutnya dapat diperkecil.



Gambar 3.4 Rangkaian *Keypad*
Sumber: Perancangan

3.4.3. Perancangan Tampilan (LCD)

Pada perancangan ini digunakan suatu tampilan yaitu LCD (*Liquid Crystal Display*), yang mana LCD ini memudahkan untuk melihat informasi atau data yang berhubungan dengan pendeteksian barang inventaris yang dilakukan yang terdapat pada memori eksternal yang ada.

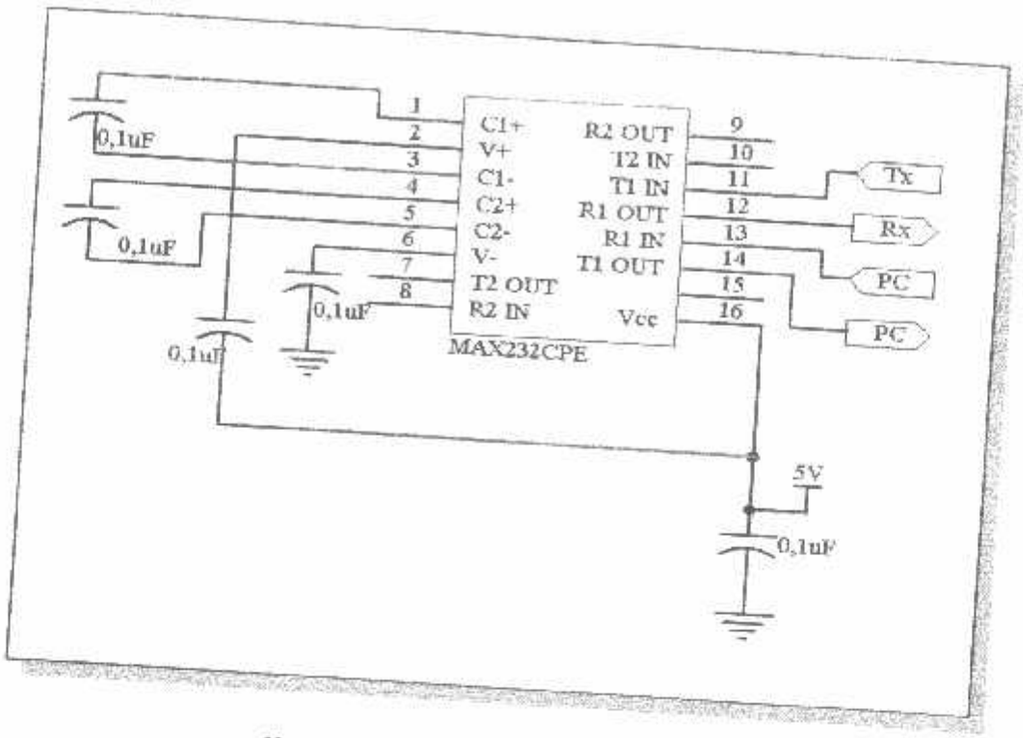


Gambar 3.5 Rangkaian Tampilan *LCD*

Sumber: Perancangan

3.4.4. Rangkaian Antarmuka Saluran RS-232

Perangkat ini digunakan sebagai alat untuk menghubungkan mikrokontroler dengan PC. Dalam jaringan yang direncanakan terdapat lima buah titik yaitu empat buah titik berupa mikrokontroler dan satu titik berupa PC. Pada titik mikrokontroler,port komunikasi serial yang digunakan bekerja padalevel tegangan RS-232 sehingga dapat langsung dihubungkan ke PC.



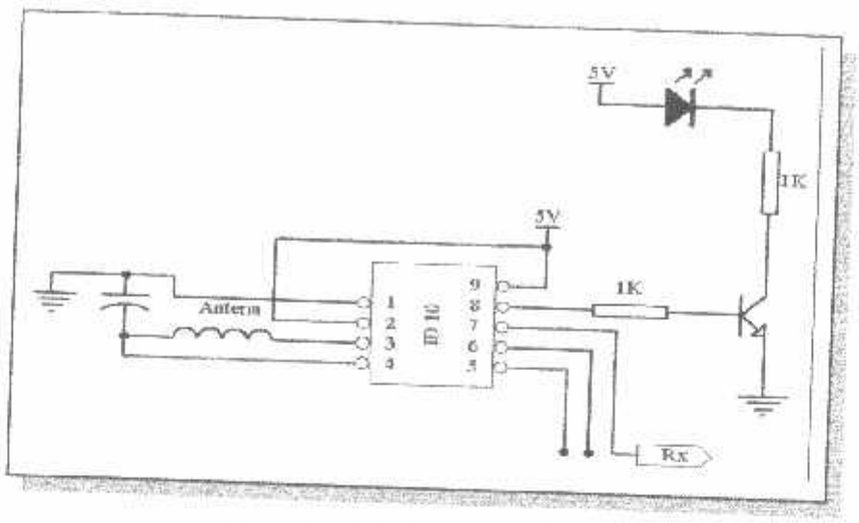
Gambar 3.6 Rangkaian Antarmuka RS-232

Sumber: Perancangan

Sebagai saluran penerima data,keluaran TTL dari mikrokontroler dihubungkan ke masukan TTL (T_{1in}) dari MAX 232 yang kemudian keluaran RS-232-nya dihubungkan ke terminal R_XD dari port serial komputer. Sedangkan sebagai saluran pengiriman data dari komputer, terminal T_XD dari port serial komputer dihubungkan ke masukan RS-232 dari MAX 232.

3.4.5. Rangkaian Antarmuka RFID

Kartu ini digunakan sebagai ID yang digunakan member untuk pembayaran warnet dengan sistem abonemen. Kartu ini harus ditempelkan atau dilewatkan di ID tag sebelum member memulai pemakaian internet. Gambar rangkaian antarmuka RFID ditunjukkan pada gambar 3.7:

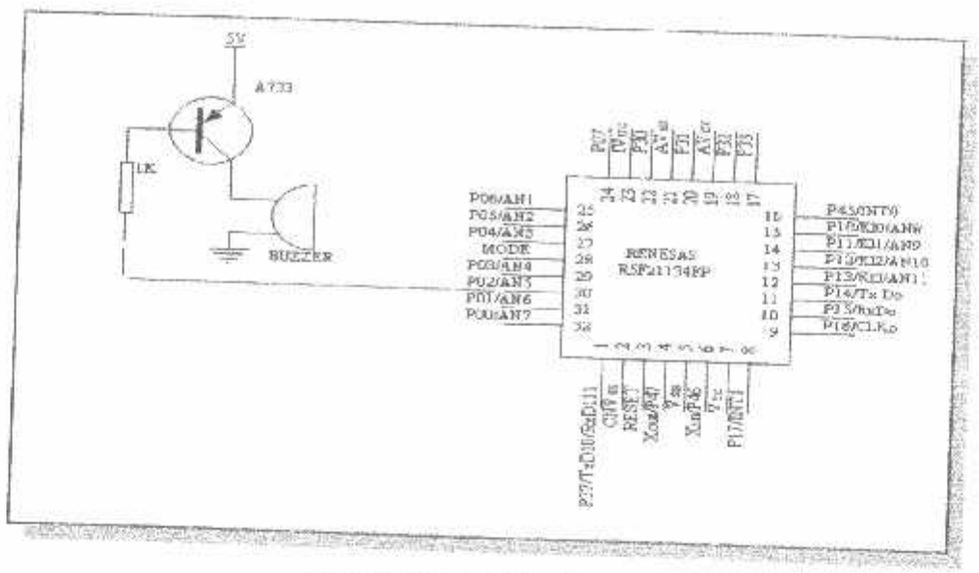


Gambar 3.7 Rangkaian Antarmuka RFID

Sumber: Perancangan

3.4.6. Rangkaian Buzzer

Rangkaian ini digunakan untuk mengetahui apakah jumlah saldo yang akan digunakan member mencukupi atau tidak. Jika saldo minimal tidak mencukupi makarangkaian ini akan bkerja dan mengeluarkan bunyi. Rangkaian buzzer ini dihubungkan dengan port0.2 pada mikrokontroler R8C/13. Gambar rangkaian buzzer ditunjukkan pada gambar 3.8:

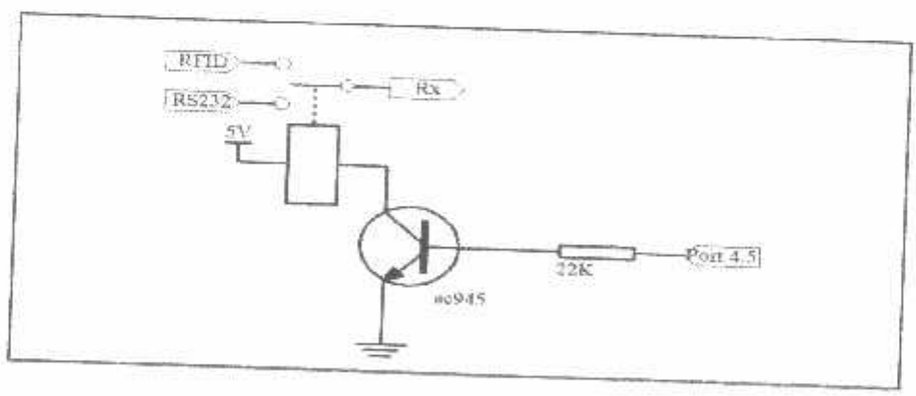


Gambar 3.8 Rangkaian Buzzer

Sumber: Perancangan

3.4.7. Rangkaian Switch Data

Rangakaian switch data ini menggunakan relay yang dipakai untuk memilih jalur data dari RFID ke mikrokontoler atau dari PC ke mikrokontroler yang melalui RS-232. Dalam rangkaian relay ini memakai transistor sc945 yang dipakai sebagai saklar penghubung relay dengan mikrokontroler.



Gambar 3.9 Rangkaian Switch Data

Sumber: Perancangan

3.5. Perancangan Perangkat Lunak

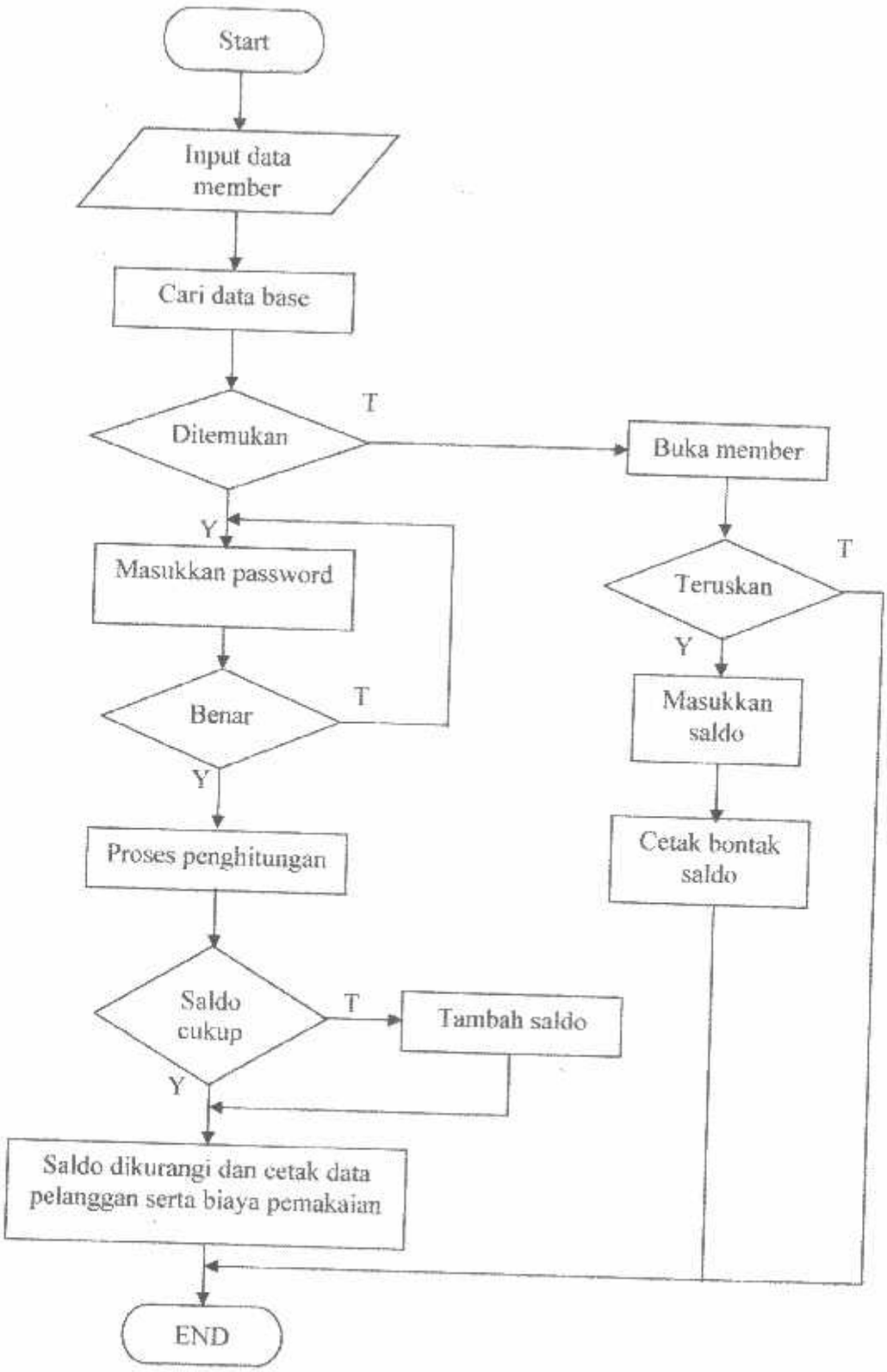
Perangkat lunak dibagi atas dua macam, yaitu program komputer yang menggunakan delphi dan program mikrokontroler yang menggunakan bahasa *C*.

3.5.1. Program Utama pada PC

Pada dasarnya program komputer ini bertujuan untuk mengorganisasi komunikasi antara komputer sebagai pengolah data dengan mikrokontroler sebagai saluran masukkan dan keluaran, sehingga untuk perangkat lunak dalam program komputer perlu diketahui terlebih dahulu aturan-aturan atau protokol komunikasi yang digunakan untuk mengatur jalannya komunikasi antara komputer dengan mikrokontroler. Diagram alir program komputer di dalam proses komunikasi dengan mikrokontroler.

3.5.2. Mikrokontroler

Program mikrokontroler bertujuan untuk mengontrol masukkan dan keluaran. Hal-hal yang dikontrol oleh mikrokontroler adalah proses komunikasi secara serial dengan RFID dan komputer, proses pengambilan data base dari PC kemudian ditampilkan ke LCD, keypad serta penyaklaran komunikasi serial antara RFID dengan komputer



Gambar 3.10 Flowchart Program

BAB IV

PENGUJIAN ALAT

4.1. Umum

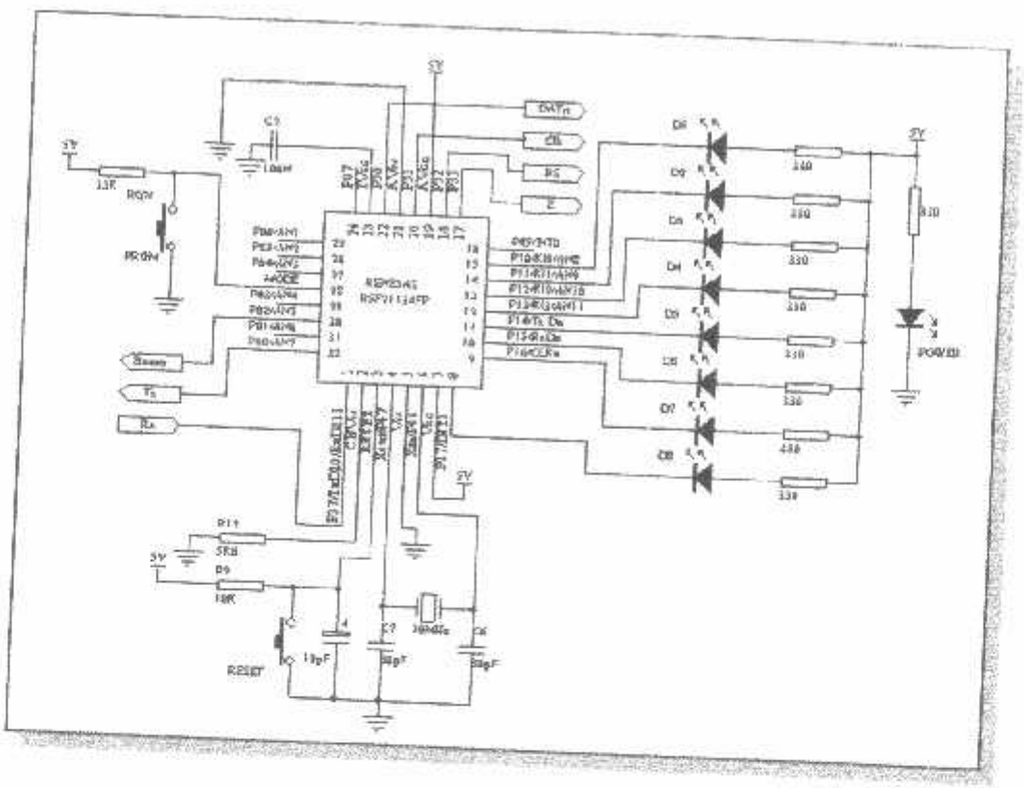
Setelah merancang keseluruhan sub-sistem selanjutnya dilakukan pengujian untuk mengetahui kerja masing-masing sub-sistem yang telah direncanakan. Setelah dilakukan pengujian terhadap masing-masing sub-sistem, selanjutnya seluruh sub-sistem tersebut digabungkan membentuk suatu sistem yang kemudian dilakukan pengujian sistem secara keseluruhan.

Pengujian sub-sistem meliputi pengujian sub-sistem mikrokontroler, sub-sistem keypad, sub-sistem LCD, sub-sistem komunikasi serial RS-232 dengan R8C/13 serta RFID dengan menggunakan program bahasa C, pengujian software Delphi sebagai pembacaan memori eksternal.

4.2. Pengujian Sub Sistem

4.2.1. Pengujian Sistem Mikrokontroler

Pengujian ini bertujuan untuk mengetahui apakah port-port paralel pada mikrokontroler yang digunakan dapat berjalan dengan baik.



Gambar 5.1. Rangkaian Pengujian Mikrokontroler Sebagai Output

Sumber: Pengujian Alat

Listing Program:

```
#include   <stdio.h>
#include        "sfr_r813.h"            /* Definition of the R8C/13 SFR */


/*****************************************
*   proto-type declaration
*****************************************/
void Delay();


/*************************************************************************
*********
*       Function : main()
*       program section
*************************************************************************
********/
void main()
{
        asm("FCLR I");          /* Interrupt disable */
```

```
        prcr = 1;               /* Protect off */
        cm13 = 1;               /* X-in X-out */
        cm15 = 1;               /* XCIN-XCOUT drive capacity select bit : HIGH*/
        cm05 = 0;               /* X-in on */
        cm16 = 0;               /* Main clock = No division mode */
        cm17 = 0;
        cm06 = 0;               /* CM16 and CM17 enable */
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        ocd2 = 0;               /* Main clock change */
        prcr = 0;               /* Protect on */

            p1 = 0x00;
    pd1 = 0xff;

    while(1)
            {
            p1 = 0x00;          // Port 1 = 00000000
            Delay();            // panggil rutin delay
            p1 = 0xFf;          // Port 1 = 11111111
            Delay();            // panggil rutin delay
            }
}

void Delay()
{
int lama = 0xFFFF;          // definisi variable lama dg nilai awal=20000
while (lama > 0, lama--);   // lama=lama-1, ulangi terus sampai lama = 0
}
```

Data Hasil Pengujian:

Tabel 4.1. Hasil Pengujian Mikrokontroler Sebagai Output

Waktu	Logika Pada P1	L7	L6	L5	L4	L3	L2	L1	L0
1	00000000B	H	H	H	H	H	H	H	H
2	11111111B	M	M	M	M	M	M	M	M

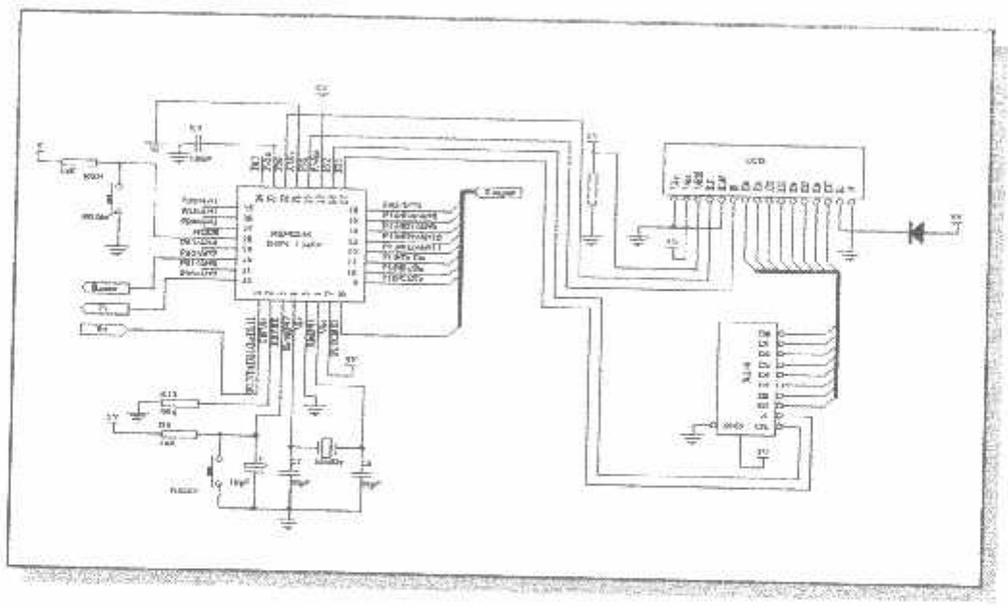
Sumber: Pengujian Alat

Keterangan:

- H : Hidup
- M : Mati

4.2.2. Pengujian Sistem Keypad dan LCD

Pengujian keypad ini bertujuan untuk mengetahui apakah keypad yang digunakan dapat berjalan dengan baik, yaitu sebagai masukan pada mikrokontroler.



Gambar 4.2 Rangkaian Pengujian Keypad

Sumber: Pengujian Alat

Listing program:

```
#include   <stdio.h>
#include   "sfr_r813.h"                /* Definition of the R8C/13 SFR */
#include   "keypad.h"
#include   "lcd.h"

void main(void)
```

```
{
    asm("FCLR I");          /* Interrupt disable */
    prcr = 1;               /* Protect off */
    cm13 = 1;               /* X-in X-out */
    cm15 = 1;               /* XCIN-XCOUT drive capacity select bit : HIGH*/
    cm05 = 0;               /* X-in on */
    cm16 = 0;               /* Main clock = No division mode */
    cm17 = 0;
    cm06 = 0;               /* CM16 and CM17 enable */
    asm("nop");
    asm("nop");
    asm("nop");
    asm("nop");
    ocd2 = 0;               /* Main clock change (x-tal)*/
    prcr = 0;               /* Protect on */

    initLCD();
    init_keypad();
    while(1)
    {
        while(Tombolnya() == ' '){;}
        kirimLCD_data(Tombolnya());
    }
}

   /*file header untuk keypad.c
   berisi deklarasi fungsi dan variabel*/

   #define keyport          p1
   #define keypad_arah pd1
```

```
#define MatrikX1 p1_7
#define MatrikX2 p1_6
#define MatrikX3 p1_5
#define MatrikX4 p1_4
#define MatrikY1 p1_3
#define MatrikY2 p1_2
#define MatrikY3 p1_1
#define MatrikY4 p1_0
void init_keypad(void);
//char Tombolnya(void);
char Tombolnya1(void);

void Delay_key(char lama);
```

Data Hasil Pengujian:

Tabel 4.2 Hasil Pengujian Keypad

Kondisi	LCD
Tekan 1	1
Tekan 2	2
Tekan 3	3
Tekan 4	4
Tekan 5	5
Tekan 6	6
Tekan 7	7
Tekan 8	8
Tekan 9	9
Tekan *	*
Tekan 0	0
Tekan #	#

Sumber: Pengujian Alat

4.2.3. Pengujian Tag RFID dan Reader RFID

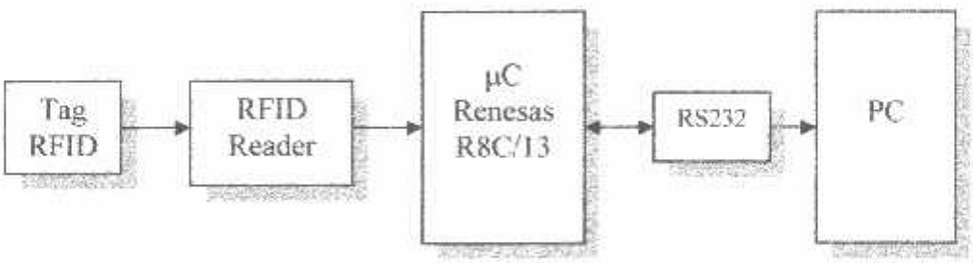
Pengujian tag RFID dan reader RFID bertujuan untuk mengetahui apakah RFID reader dapat membaca tag (kartu) RFID atau tidak.

a. Peralatan Yang Dibutuhkan

1. Tag (kartu) RFID
2. RFID reader
3. Mikrokontroler Renesas R8C/13
4. RS232 sebagai penghubung Mikrokontroler dengan PC
5. PC

b. Prosedur Pengujian

1. Menyusun rangkaian seperti gambar 4.1
2. Menempelkan tag pada RFID reader
3. Mengamati reader



Gambar 4.4 Diagram Blok Pengujian tag terhadap reader RFID

c. Hasil Pengujian dan Analisis

Hasil Pengujian menunjukkan bahwa RFID reader dapat membaca tag (kartu) RFID atau tag dapat diakses oleh reader sampai sejauh kurang lebih 3cm.

Dengan demikian RFID untuk digunakan sebagai kartu absensi karyawan karena telah bekerja dengan baik.

Tabel 4.3 Pengujian RFID

Jarak jangkauan	Tingkat pengujian	Kepekaan reader
1 cm	10 kali	10 kali sangat peka
2 cm	10 kali	10 kali peka
3 cm	10 kali	10 kali peka
4 cm	10 kali	5 kali peka, 2 kali kurang peka, 3 kali tidak peka
5 cm	10 kali	10 kali Tidak Peka
6 cm	10 kali	10 kali Tidak Peka
7 cm	10 kali	10 kali Tidak Peka
8 cm	10 kali	10 kali Tidak Peka

4.2.4. Pengujian Sistem Secara Keseluruhan

Pengujian sistem secara keseluruhan bertujuan untuk mengetahui apakah sistem dapat bekerja dengan baik sesuai dengan yang perencanaan.

a. Peralatan dan perlengkapan yang digunakan

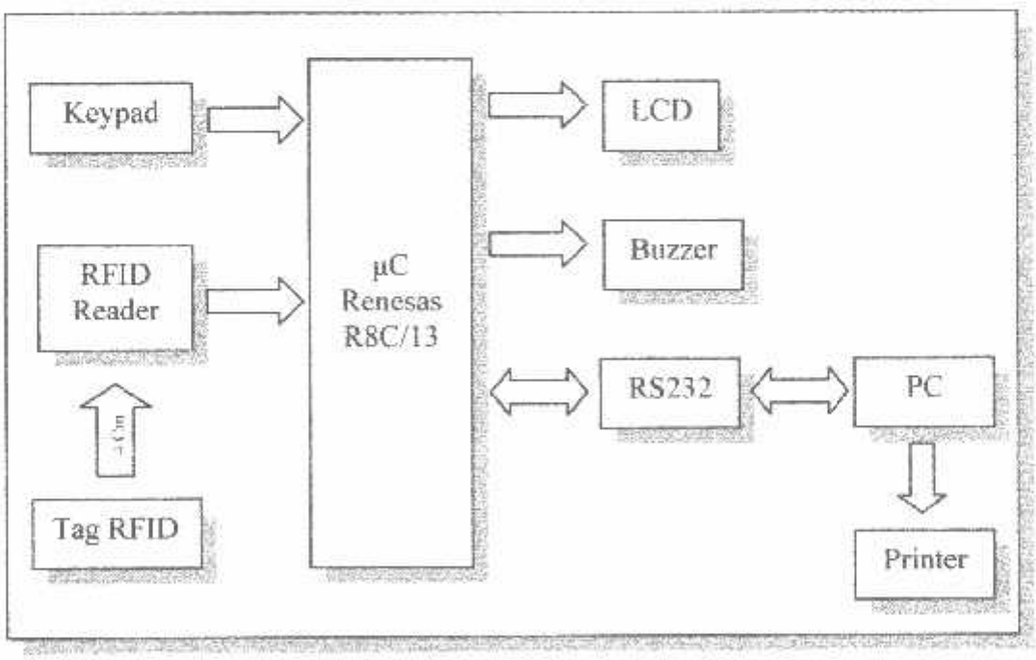
- PC (Personal Komputer).
- Keseluruhan sistem pada client:
  - Tag RFID
  - Reader RFID
  - Buzzer
  - Keypad
  - LCD

- Mikrokontroller AT89S51
- RS232
- PC (Personal Computer

- Kabel serial
- Software Komputer
- Database yang terkoneksi dengan software yang digunakan

b. Prosedure Pengujian

- Menyusun Rangkaian seperti Gambar 4.4
- Mendekatkan Tag ke Reader RFID
- Memberi masukan dengan keypad
- Mengamati respon Buzzer
- Mengamati tampilan LCD



Gambar 4.5 Blok Diagram Pengujian Keseluruhan Sistem

Sumber: Perancangan

Rangkaian akan berjalan sesuai dengan yang diinginkan apabila tag dapat diterima oleh reader dan data diolah oleh mikrokontroller kemudian diminta mengetikkan password sebagai masukannya adalah keypad setelah itu data disesuaikan dengan data base yang ada pada PC jika data telah cocok maka akan tampil dalam LCD berupa yang meliputi nama pelanggan, nomor ID pelanggan, pin atau password dari pelanggan saldo yang dimiliki pelanggan dan informasi lain yang memungkinkan perlu sebagai informasi tentang identitas lain yang ada.

Tabel 4.4. Data pengujian system abonemen pada warnet

No	System pengoperasian	Hasil Pengujian
1	Operasi Tag ke reder RFID	Dapat diterima oleh reader RFID
2	Masukan Keypad	Password sesuai
3	Pengolahan mikrokontroller Dan Kesesuaian dengan Data Base	Sesuai dengan data base
4	Sistem Buzzer	Aktif
5	Output LCD	Dapat menampilkan nama pelanggan, nomor ID pelanggan, pin atau password dari pelanggan saldo yang dimiliki pelanggan dan informasi lain

Berdasarkan pengujian didapatkan hasil bahwa setelah Tag didekatkan dengan Reader RFID maka reader dapat menerimasinyal masukan dari tag, setelah data diolah oleh mikrokontroller dan sesuai dengan data base, LCD sebagai outputannya. Sehingga dapat dikatakan bahwa system absensi telah bekerja terbukti dengan mampu bekerja sesuai dengan yang diinginkan.

BAB V

KESIMPULAN

5.1. Kesimpulan

Berdasarkan dari hasil pembuatan dan perancangan alat ini, maka dapat diperoleh beberapa kesimpulan sebagai berikut :

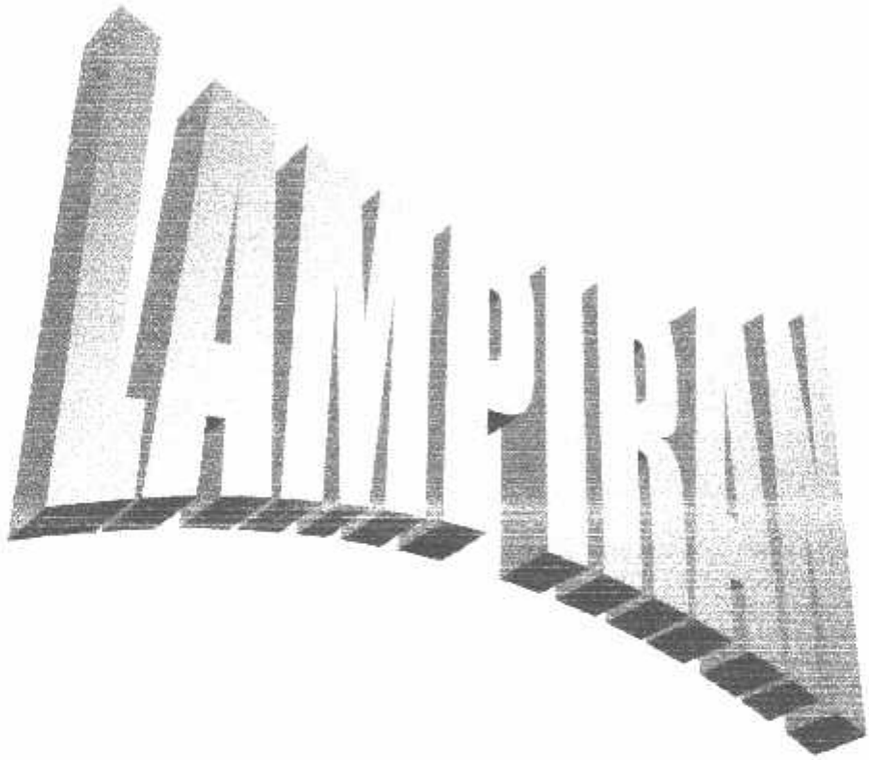
- Komunikasi antar tag dengan pembaca RFID sangat bergantung pada daya yang diterima tag dari antena yang terhubung dengan pembaca RFID.
- Intensitas medan magnet yang diemisikan oleh antena berkurang terhadap jarak, maka akan terdapat jarak dimana tag tidak aktif.
- Komunikasi anatar tag dengan reader berkurang jika medan magnet harus menembus material yang mengurangi daya elektromagnetik
- Faktor penghalang dari luar seperti logam sangat mempengaruhi pengiriman data ke penerima karena logam secara signifikan mengurangi fluks dari medan magnet.

5.2. Saran-saran

- Jarak antara tag RFID dengan RFID Reader sebaiknya tidak lebih dari 4 Centimeter.
- Saat melewatkan tag RFID ke RFID Reader sebaiknya yang tidak terhalang sesuatu terutama benda-benda yang mengandung logam atau material yang dapat mengurangi daya elektromagnetik.

DAFTAR PUSTAKA

1. www.renesas.com, ***R8C/13 Group***, Single-Chip 16-bit microcomputer, Rev.1.10
2. Albert Paul Malvino, Ph.D.(1994). ***Prinsip-prinsip Elektronika Jilid I dan II.*** Alih Bahasa M.Barnawi,Ph.D. Jakarta : Penerbit Erlangga
3. Robert F. Coughlin. Frederick F. Driscoll. (1994). ***Penguat Operasional dan Rangkaian Terpadu Linier***. Penerbit Erlangga. Jakarta
4. www.digiware.com, RF ID product data sheets archieves
5. www.maxim_ic.com, Maxim ± 15 kV ESD-Protected, +5 V RS-232 Transceivers
6. Albert Paul Malvino, Ph.D and Donald P. Leagh, Ph.D, ***Prinsip-prinsip dan Penerapan Digital***. Alih Bahasa Ir. Irawan Wijaya, UKI, 1994, Penerbit Erlangga


LAMPUR

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ENERGI LISTRIK

LEMBAR BIMBINGAN SKRIPSI

Nama Mahasiswa	: DENNY PRASETYA
N.I.M.	: 01.17.082
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: PERANCANGAN DAN PEMBUATAN SISTEM ABONEMEN PEMBAYARAN PADA WARNET DENGAN MENGGUNAKAN MEMBER CARD RFID BERBASIS MIKROKONTROLER RENESAS R8C/13

Tanggal Mengajukan Skripsi	: 25 Agustus 2006
Tanggal Menyelesaikan Skripsi	: 20 September 2006
Dosen Pembimbing	: Joseph Dedy Irawan, ST,MT
Telah dievaluasi dengan nilai	: 86 (Delapan Puluh Enam)

Malang, September 2006

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JURUSAN TEKNIK ELEKTRO S-1
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BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

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Judul Skripsi	**: PERANCANGAN DAN PEMBUATAN SISTEM ABONEMEN PEMBAYARAN PADA WARNET DENGAN MENGGUNAKAN MEMBER CARD RFID BERBASIS MIKROKONTROLER RENESAS R8C/13**

Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1)

Hari	**: Kamis**
Tanggal	**: 21 September 2006**
Dengan Nilai	**: 79,1 (B+)**

Panitia Ujian

(Ir. Mochtar Asroni, MSME)
Ketua

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Sekretaris

Anggota Penguji

(Ir.Usman Djuanda, MM)
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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

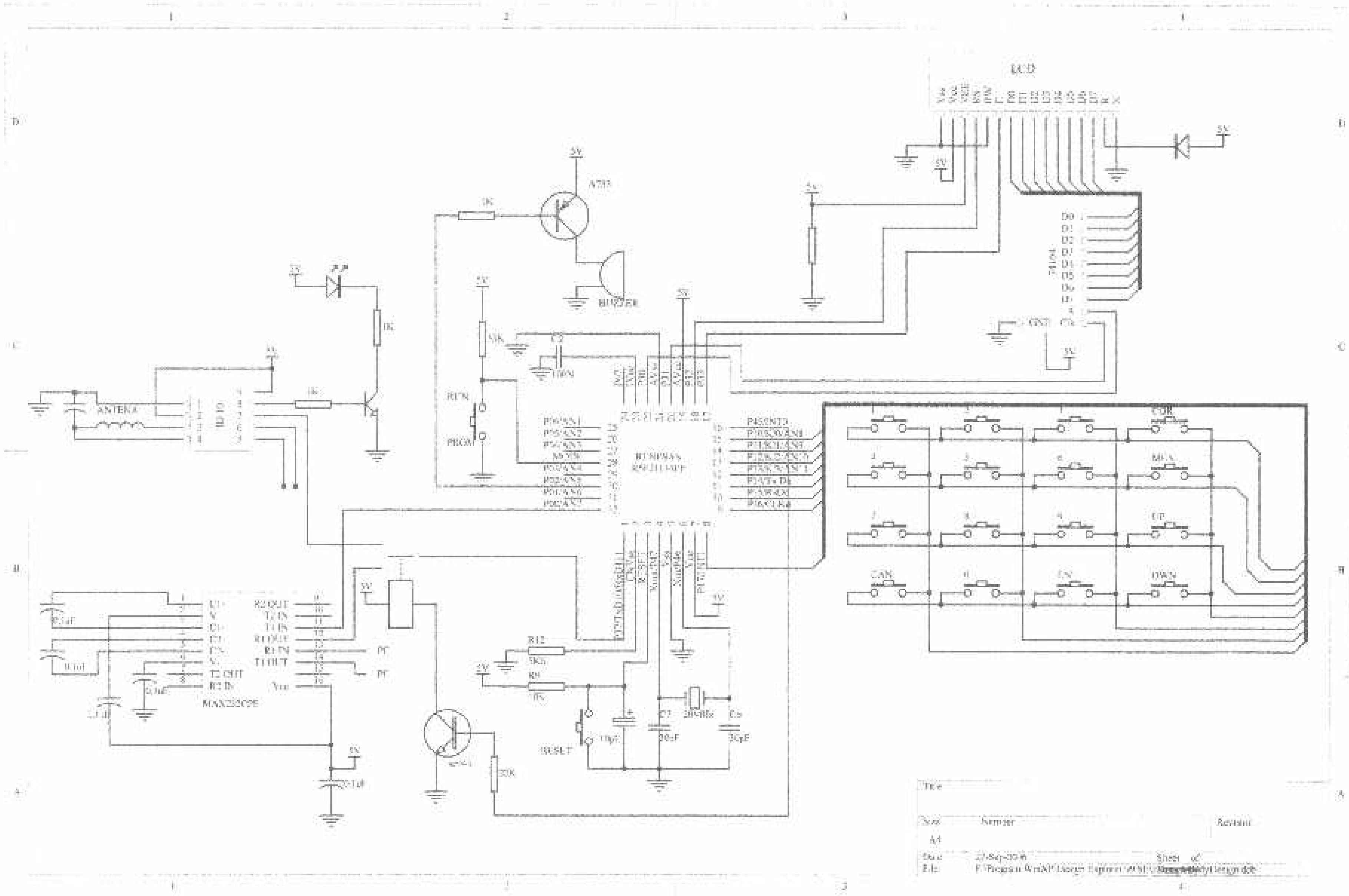
Formulir Bimbingan Skripsi

Nama : Denny Prasetya
Nim : 01.17.082
Masa Bimbingan : 10Agustus 2006 s/d 10 Februari 2007
Judul Skripsi : " Perancangan dan Pembuatan Sistem Abonemen Pembayaran Pasa Warnet dengan Menggunakan Member Card RF ID Berbasis Mikrokontroller Renesas R8C/13 "

No	Tanggal	Uraian	Paraf Bimbingan
1	02 - 9 - 2006	Bab I , revisi latar belakang	
2	03 - 9 - 2006	ACC BAB I	
3	06 - 9 - 2006	BAB II , revisi gambar , ket. gambar dan sumber gambar	
4	07 - 9 - 2006	ACC BAB II , revisi BAB III gambar	
5	09 - 9 - 2006	ACC BAB III , revisi BAB IV tabel pengujian	
6	14 - 9 - 2006	ACC BAB IV	
7	19 - 9 - 2006	ACC KOMPRE	
8			
9			
10			

Malang.....
Dosen Pembimbing

Joseph Dedy Irawan, ST, MT
NIP: 132315178



LCD
74164
BUZZER
A733
ANTENA
MAX232C05
RESET
PROM
R12
5K6
R8
10K
22K
20MHz
C7
C6
C2
100N
30pF
CAN
DWN
UP
MCA
COR
Title
Size
Number
Revision
A4
Sheet of

```
/************************************************************************
******/
/*                                                                      */
/*  FILE        :aban.c                                                 */
/*  DATE        :Wed, Aug 09, 2006                                      */
/*  DESCRIPTION :Main Program                                           */
/*  CPU TYPE    :Other                                                  */
/*                                                                      */
/*  This file is generated by Renesas Project Generator (Ver.4.0).      */
/*                                                                      */
/************************************************************************
******/
#include <sfr_r813.h>
#include "lcd.h"
#include "keypad.h"
#include "usart.h"

#define max_list 6   //list maximum = max_list - 2
#define control p0_2
#define buzzer  p0_3

char mode, status;
char rf_data[16];
char pass_data[6];
char rx_buff;
unsigned char counter, counter_p, pointer;

#pragma INTERRUPT rx_int
void rx_int(void)
{
        /*if(u0rb == 0x02)
        {
                mode = 1;       //rfid mode
                counter = 0;
        }else if(u0rb == 0x05)
        {
                mode = 0;       //comp mode
        }*/
        if(mode == 1)
        {
                rf_data[counter] = u1rb;
                counter++;
        }else if(mode == 0)
        {
                rx_buff = u1rb;
                status = 1;
        }
}
void Delay(char lama);
void baca_pwd(void);
void baca_sisa(void);
//void pilih_kota(void);
void kirim_pwd(void);
```

```
void main(void)
{
        asm("FCLR I");                                  /* Interrupt
disable */
        prcr = 1;                                               /* Protect
off */
        cm13 = 1;                                               /* X-in
X-out */
        cm15 = 1;       /* XCIN-XCOUT drivecapacity select bit :
HIGH */
        cm05 = 0;                                               /* X-in on
*/
        cm16 = 0;                                       /* Main clock = No
division mode */
        cm17 = 0;
        cm06 = 0;                                               /* CM16
and CM17 enable*/
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        ocd2 = 0;                                       /* Main clock
change (x-tal)*/
        prcr = 0;                                               /* Protect
on */
        prc2 = 1;
        pd0_2 = 1;
        prc2 = 1;
        pd0_3 = 1;
        pd3_7 = 0;

        control = 0;
        buzzer = 1;
        initLCD();
        initSerial();
        init_keypad();

        mode = 1;
        status = 0;
        rx_buff = 0;
        counter = 0;
        asm("FSET I");
        kirimLCD_perintah(0x01);
        kirimLCD_perintah(0x80);
        kirimLCD_string("    Selamat    ");
        kirimLCD_perintah(0xC0);
        kirimLCD_string("    Datang     ");
        while(1)
        {
                //kirimLCD_string("Maskkan pssword");
                if(mode == 1)
                {
                        while(counter < 16){;}
                        asm("FCLR I"); //disable int

                        //convert id
                        kirimLCD_perintah(0x01);
                        kirimLCD_perintah(0x81);
                        kirimLCD_string("Maskkan pssword");
                        kirimLCD_perintah(0xC1);
                        baca_pwd();
                        counter = 3;
```

```
                counter_p = 0;
                control = 1;
                Delay(0xFFFF);
                kirimSeri('I');
                Delay(0xFFFF);
                while(counter < 11)
                {
                        kirimSeri(rf_data[counter]);
                        Delay(0xFFFF);
                        counter++;
                }
                kirimSeri('P');
                Delay(0xFFFF);
                kirim_pwd();
                kirimLCD_perintah(0x01);
                counter = 0;
                mode = 0;
                asm("FSET I");
        }else if(mode == 0)
        {
                switch(rx_buff)
                {
                        case 'A' :
kirimLCD_perintah(0x01);
kirimLCD_string("Paswd diterima");
Delay(0xFFFF);
                                                        while
(status == 0){;}
                                                        status =
0;
                                                        rx_buff =
0;
                                                        break;
                        case 'B' :
kirimLCD_perintah(0x01);
                                                        mode = 1;
Delay(0xFFFF);
                                                        control =
0;
kirimLCD_string("Paswd ditolak");
                                                        pm03 = 1;
                                                        rx_buff =
0;
                                                        break;
                        case 'C' :
kirimLCD_perintah(0x01);
kirimLCD_string("Sisa saldo");
kirimLCD_perintah(0xC1);
kirimLCD_string("Rp  ");
baca_sisa();
                                                        rx_buff =
0;
                                                        break;
                        case 'D' :      buzzer = 0;
```

```
//active low
                                                    break;
                                case 'E' :      control = 0;
                                                buzzer =
1;
                                                mode = 1;
                                                rx_buff =
0;
kirimLCD_perintah(0x80);
kirimLCD_string("    Selamat    ");
kirimLCD_perintah(0xC0);
kirimLCD_string("    Datang     ");
                                                break;
                                case 'F' :
kirimLCD_perintah(0x01);
                                                rx_buff =
0;
                                                break;
                        }
                }
        }
}
void Delay(char lama)
{
        while (lama > 0)
        {
                lama--;         // lama=lama-1, ulangi terus
sampai lama = 0
        }
}
void baca_pwd(void)
{
        counter_p = 0;
        while(counter_p < 6)
        {
                while(Tombolnya1() != ' ')
                {
                        if((Tombolnya1() >= '0') && (Tombolnya1()
<= '9'))
                        {
                            pass_data[counter_p] = Tombolnya1();
                                kirimLCD_data('*');
                                counter_p++;
                        }
                        while(Tombolnya1() != ' '){;}
                }
        }
        while(Tombolnya1() != 'E');
}
void kirim_pwd(void)
{
        counter_p = 0;
        while(counter_p < 6)
        {
                kirimSeri(pass_data[counter_p]);
                Delay(0xFFFF);
                counter_p++;
```

```
        }
}
void baca_sisa(void)
{
//      u1c1 |= 0x04;
//      while((u1c1 & 0x08) == 0x00 ){;}
//      rx_buff = u1rb; //pindahkan data

        while(rx_buff != 'Z')
        {
                status = 0;
                if((rx_buff >= 0x30) && (rx_buff <= 0x39))
                {
                        kirimLCD_data(rx_buff);
                }
                Delay(0xFFFF);
        //      u1c1 |= 0x04;
        //      while((u1c1 & 0x08) == 0x00 ){;}
                while (status == 0){;}
        //      rx_buff = u1rb; //pindahkan data

        }

}
/*void pilih_kota(void)
{
        kirimLCD_perintah(0x81);
        kirimLCD_string("  Kota Tujuan :");
//      kirimLCD_perintah(0xC1);
        pointer = 1;
        while(Tombolnya1() != 'E')
        {
                if(Tombolnya1() == 'U')
                        pointer++;
                if(Tombolnya1() == 'D')
                        pointer--;
                while(Tombolnya1() != ' '){;}
                if(pointer == 0)
                        pointer = max_list - 1;
                if(pointer == max_list)
                        pointer = 1;
                kirimLCD_perintah(0xC1);
                switch(pointer)
                {
                        case 1 : //kirimLCD_perintah(0x01);
                                                kirimLCD_string("Surabaya
        ");
                                                break;
                        case 2 : //kirimLCD_perintah(0x01);

 //kirimLCD_perintah(0xC1);
                                                kirimLCD_string("Jember
        ");
                                                break;
                        case 3 : //kirimLCD_perintah(0x01);

 //kirimLCD_perintah(0xC1);

 kirimLCD_string("Banyuwangi      ");
                                                break;
                        case 4 : //kirimLCD_perintah(0x01);
```

```
//kirimLCD_perintah(0xC1);
        ");
                                        kirimLCD_string("Bangil
                                        break;
                        case 5 : //kirimLCD_perintah(0x01);
//kirimLCD_perintah(0xC1);
                                        kirimLCD_string("Jakarta
        ");
                                        break;
                }

         }
         kirimSeri(pointer);;
}*/
```

Everywhere you imagine.

R8C/13 Group

Hardware Manual

RENESAS 16-BIT SINGLE-CHIP MICROCOMPUTER

M16C FAMILY/R8C/Tiny SERIES

Rev. 1.10
Revision date: Apr 27, 2005

Renesas Technology
www.renesas.com

I. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8)
Electrical characteristics	Power supply voltage	VCC = 3.0 to 5.5V (f(XIN) = 20MHz) VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
	Power consumption	Typ.9 mA (VCC = 5.0V, (f(XIN) = 20MHz,High-speed mode) Typ.5 mA (VCC = 3.0V, (f(XIN) = 10MHz,High-speed mode) Typ.35 µA (VCC = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 µA (VCC = 3.0V, Stop mode)
Flash memory	Program/erase voltage	VCC = 2.7 to 5.5 V
	Number of program/erase	10,000 times (Data area) 1,000 times (Program area)
Operating ambient temperature		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

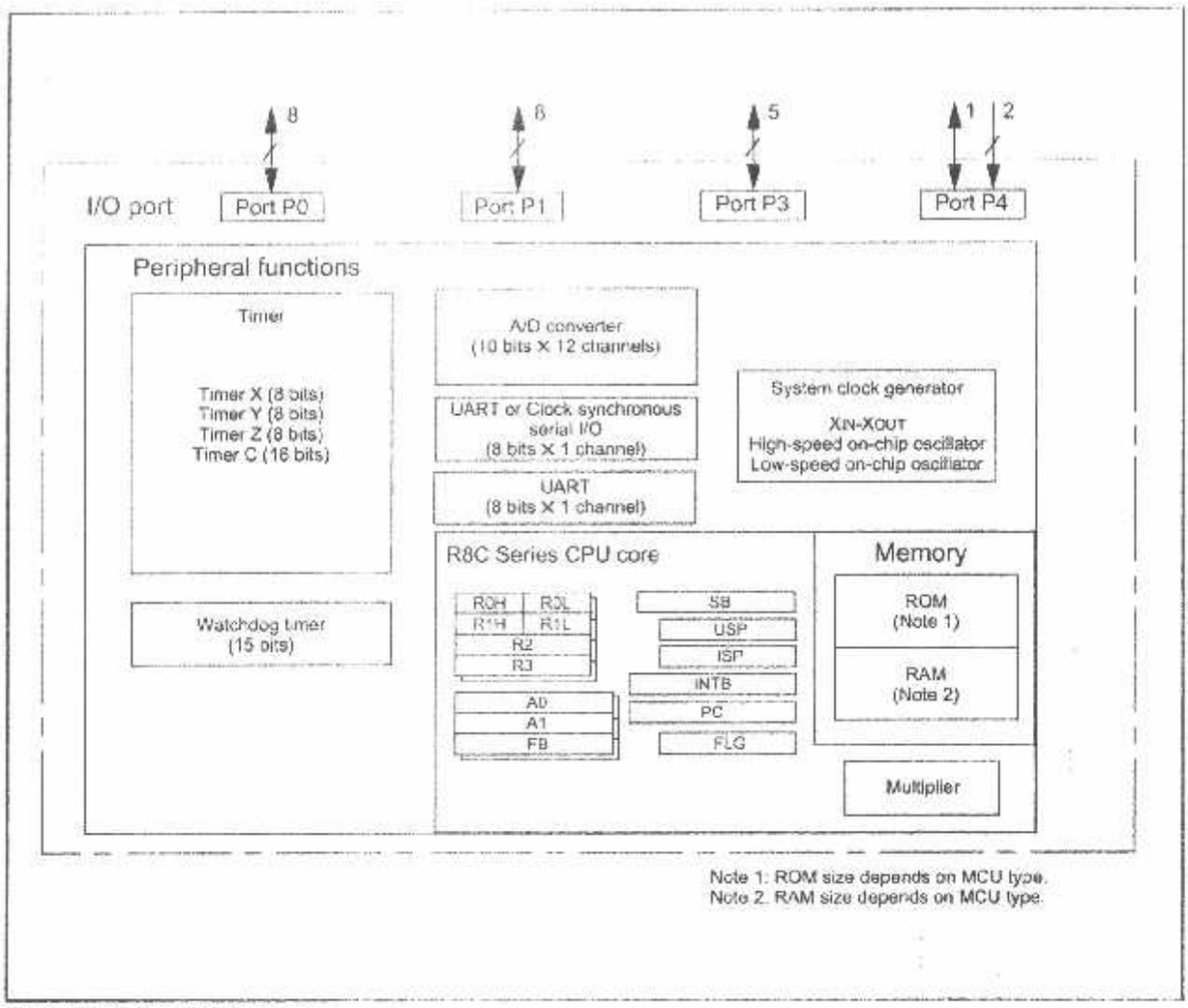


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of April 2005

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

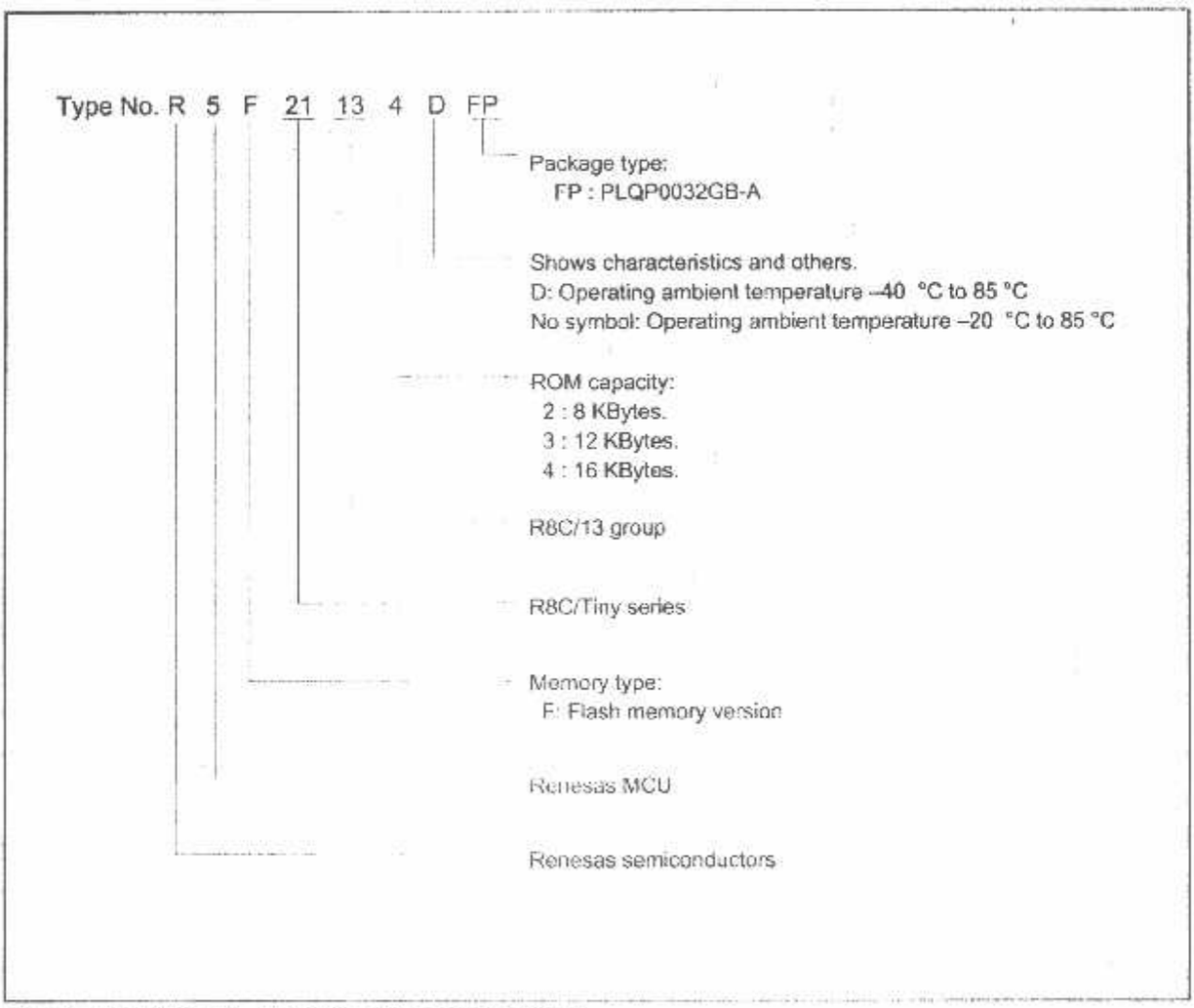


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

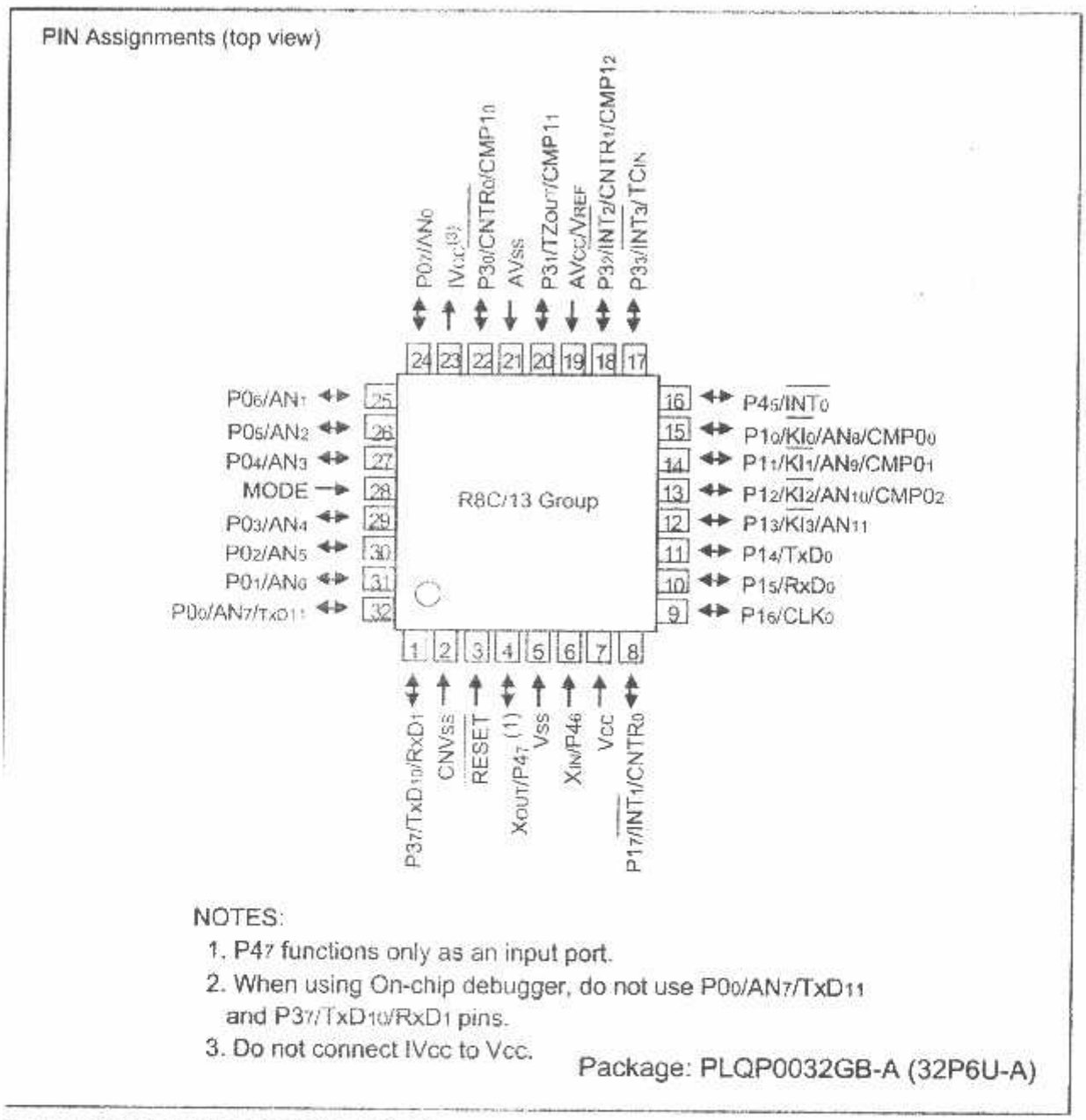


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply Connect this pin to Vss via a capacitor (0.1 µF) Do not connect to Vcc
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor(1)
MODE	MODE	I	Connect this pin to Vcc via a resistor
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	These are INT interrupt input pins.
Key input interrupt input	KI0 to KI3	I	These are key input interrupt pins.
Timer X	CNTR0	I/O	This is the timer X I/O pin.
	CNTR0	O	This is the timer X output pin.
Timer Y	CNTR1	I/O	This is the timer Y I/O pin.
Timer Z	TZOUT	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP00 to CMP03, CMP10 to CMP13	O	These are the timer C output pins.
Serial interface	CLK0	I/O	This is a transfer clock I/O pin.
	RxD0, RxD1	I	These are serial data input pins.
	TxD0, TxD10, TxD11	O	These are serial data output pins.
Reference voltage input	VREF	I	This is a reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	These are analog input pins for A/D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	These are input only pins.

NOTES :

1. Refer to "19.8 Noise" for the connecting reference resistor value.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

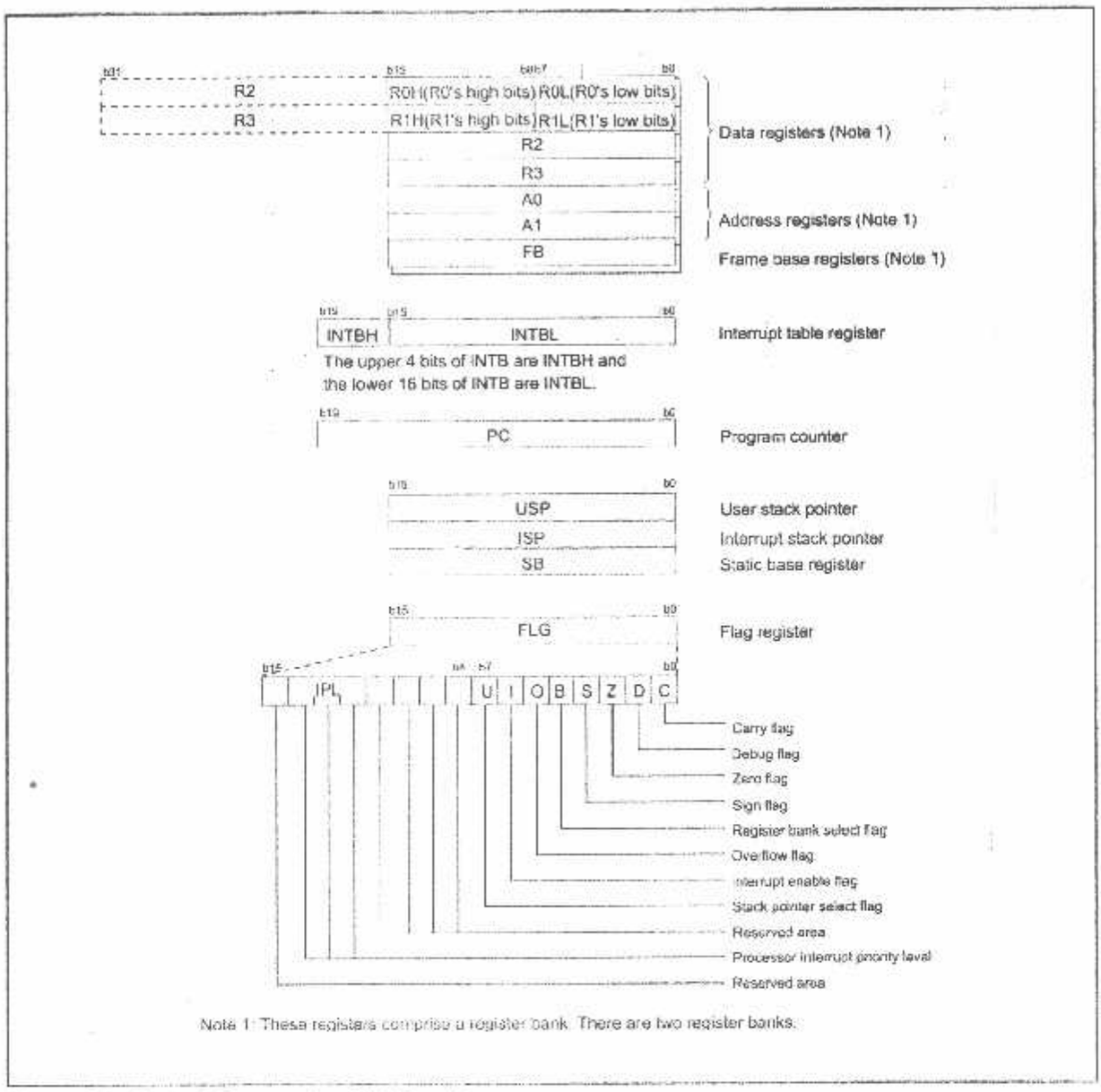


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 0000016 to FFFFF16.

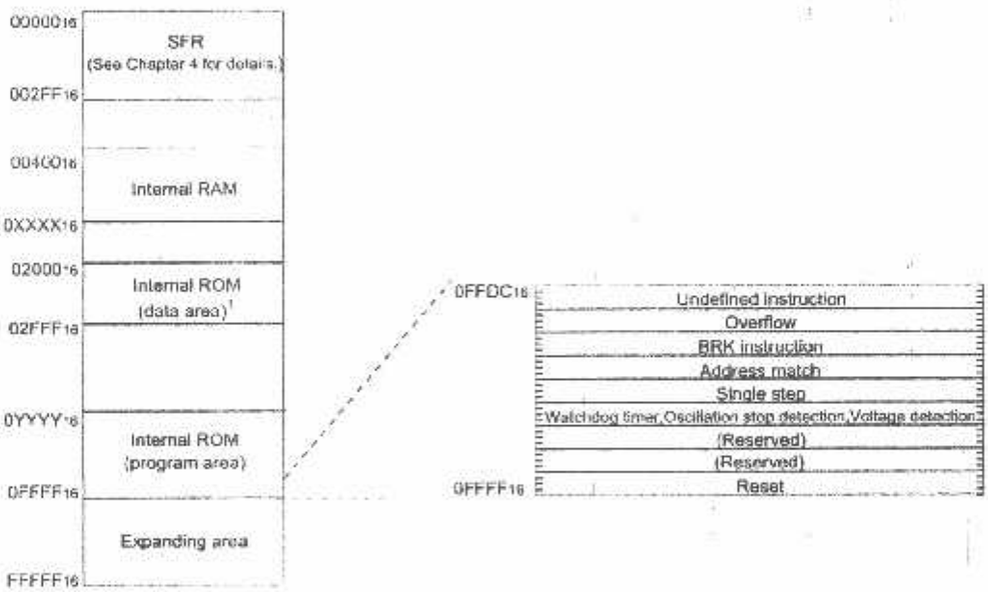
The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFF16. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C00016 to 0FFFF16.

The fixed interrupt vector table is allocated to the addresses from 0FFDC16 to 0FFFF16. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 0200016 to 02FFF16.

The internal RAM is allocated in an upper address direction beginning with address 0040016. For example, a 1-Kbyte internal RAM is allocated to the addresses from 0040016 to 007FF16. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 0000016 to 002FF16. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



NOTES:
1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY16	Size	Address 0XXXX16
R5F21134FP, R5F21134DFP	16K bytes	0C00016	1K bytes	007FF16
R5F21133FP, R5F21133DFP	12K bytes	0D00016	768 bytes	006FF16
R5F21132FP, R5F21132DFP	8K bytes	0E00016	512 bytes	005FF16

igure 3.1 Memory Map

I. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 [1]	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00₁₆
0006₁₆	System clock control register 0	CM0	01101000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆	High-speed on-chip oscillator control register 0	HR0	00₁₆
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	00XXX000₂
000B₁₆	High-speed on-chip oscillator control register 1	HR1	40₁₆
000C₁₆	Oscillation stop detection register	OCD	00000100₂
000D₁₆	Watchdog timer reset register	WDTR	XX₁₆
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00011111₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [2]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [2]	VCR2	00₁₆ [3] 10000000₂ [4]
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	INT0 input filter select register	INT0F	XXXXX000₂
001F₁₆	Voltage detection interrupt register [2]	D4INT	00₁₆ [3] 01000001₂ [4]
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined

NOTES:
1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = H retaining

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	AD conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX000₂
0056₁₆	Timer X interrupt control register	TXIC	XXXXX000₂
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX000₂
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX000₂
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX000₂
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX000₂
005B₁₆	Timer C interrupt control register	TCIC	XXXXX000₂
005C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y	PREY	FF₁₆
0082₁₆	Timer Y secondary	TYSC	FF₁₆
0083₁₆	Timer Y primary	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z	PREZ	FF₁₆
0086₁₆	Timer Z secondary	TZSC	FF₁₆
0087₁₆	Timer Z primary	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆	Timer C register	TC	00₁₆
0091₁₆			00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆	Capture, compare 0 register	TM0	00₁₆
009D₁₆			00₁₆[2]
009E₁₆	Compare 1 register	TM1	FF₁₆
009F₁₆			FF₁₆
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate register	U0BRG	XX₁₆
00A2₁₆	UART0 transmit buffer register	U0TB	XX₁₆
00A3₁₆			XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
00A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
00A6₁₆	UART0 receive buffer register	U0RB	XX₁₆
00A7₁₆			XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
00AA₁₆	UART1 transmit buffer register	U1TB	XX₁₆
00AB₁₆			XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
00AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
00AE₁₆	UART1 receive buffer register	U1RB	XX₁₆
00AF₁₆			XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF₁₆.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0₁₆	AD register	AD	XX16
00C1₁₆			XX16
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆	AD control register 2	ADCON2	0016
00D5₁₆			
00D6₁₆	AD control register 0	ADCON0	00000XXX2
00D7₁₆	AD control register 1	ADCON1	0016
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆	Port P0 register	P0	XX16
00E1₁₆	Port P1 register	P1	XX16
00E2₁₆	Port P0 direction register	PD0	0016
00E3₁₆	Port P1 direction register	PD1	0016
00E4₁₆			
00E5₁₆	Port P3 register	P3	XX16
00E6₁₆			
00E7₁₆	Port P3 direction register	PD3	0016
00E8₁₆	Port P4 register	P4	XX16
00E9₁₆			
00EA₁₆	Port P4 direction register	PD4	0016
00EB₁₆			
00EC₁₆			
00ED₁₆			
00EE₁₆			
00EF₁₆			
00F0₁₆			
00F1₁₆			
00F2₁₆			
00F3₁₆			
00F4₁₆			
00F5₁₆			
00F6₁₆			
00F7₁₆			
00F8₁₆			
00F9₁₆			
00FA₁₆			
00FB₁₆			
00FC₁₆	Pull-up control register 0	PUR0	00XX00002
00FD₁₆	Pull-up control register 1	PUR1	XXXXXX0X2
00FE₁₆	Port P1 drive capacity control register	DRR	0016
00FF₁₆	Timer C output control register	TCOUT	0016
01B3₁₆	Flash memory control register 4	FMR4	010000002
01B4₁₆			
01B5₁₆	Flash memory control register 1	FMR1	1000000X2
01B6₁₆			
01B7₁₆	Flash memory control register 0	FMR0	000000012
0FFFF₁₆	Option function select register(2)	OFS	Note 2

X : Undefined

NOTES:

1. The blank areas, 0100₁₆ to 01B2₁₆ and 01B8₁₆ to 02FF₁₆ are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

5. Reset

There are three types of resets: a hardware reset, a software reset, and an watchdog timer reset.

5.1 Hardware Reset

There are three kinds of hardware reset: hardware reset 1, hardware reset 2, and power-on reset. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected for the CPU.

5.1.1 Hardware Reset 1

A reset is applied using the RESET pin. When an "L" signal is applied to the $\overline{\text{RESET}}$ pin while the power supply voltage is within the recommended operating condition, the pins are initialized (see Table 5.1 "Pin Status When $\overline{\text{RESET}}$ Pin Level is 'L'"). When the input level at the $\overline{\text{RESET}}$ pin is released from "L" to "H", the CPU and SFR are initialized, and the program is executed starting from the address indicated by the reset vector. Figure 5.1 shows the CPU register status after reset and figure 5.2 shows the reset sequence. The internal RAM is not initialized. If the $\overline{\text{RESET}}$ pin is pulled "L" while writing to the internal RAM, the internal RAM becomes indeterminate.
Figures 5.3 to 5.4 show the reset circuit example using the hardware reset 1. Refer to Chapter 4, "Special Function Register (SFR)" for the status of SFR after reset.

• When the power supply is stable
(1) Apply an "L" signal to the RESET pin.
(2) Wait for 500 µs (1/f_{RING-S} × 20).
(3) Apply an "H" signal to the RESET pin.

• Power on
(1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin.
(2) Let the power supply voltage increase until it meets the recommended operating condition.
(3) Wait td(P-R) or more until the internal power supply stabilizes.
(4) Wait for 500 µs (1/f_{RING-S} × 20).
(5) Apply an "H" signal to the $\overline{\text{RESET}}$ pin.

Table 5.1 Pin Status When $\overline{\text{RESET}}$ Pin Level is "L"

Pin name	Pin status
P0	Input port
P1	Input port
$P3_0$ to $P3_3$, $P3_7$	Input port
$P4_5$ to $P4_7$	Input port

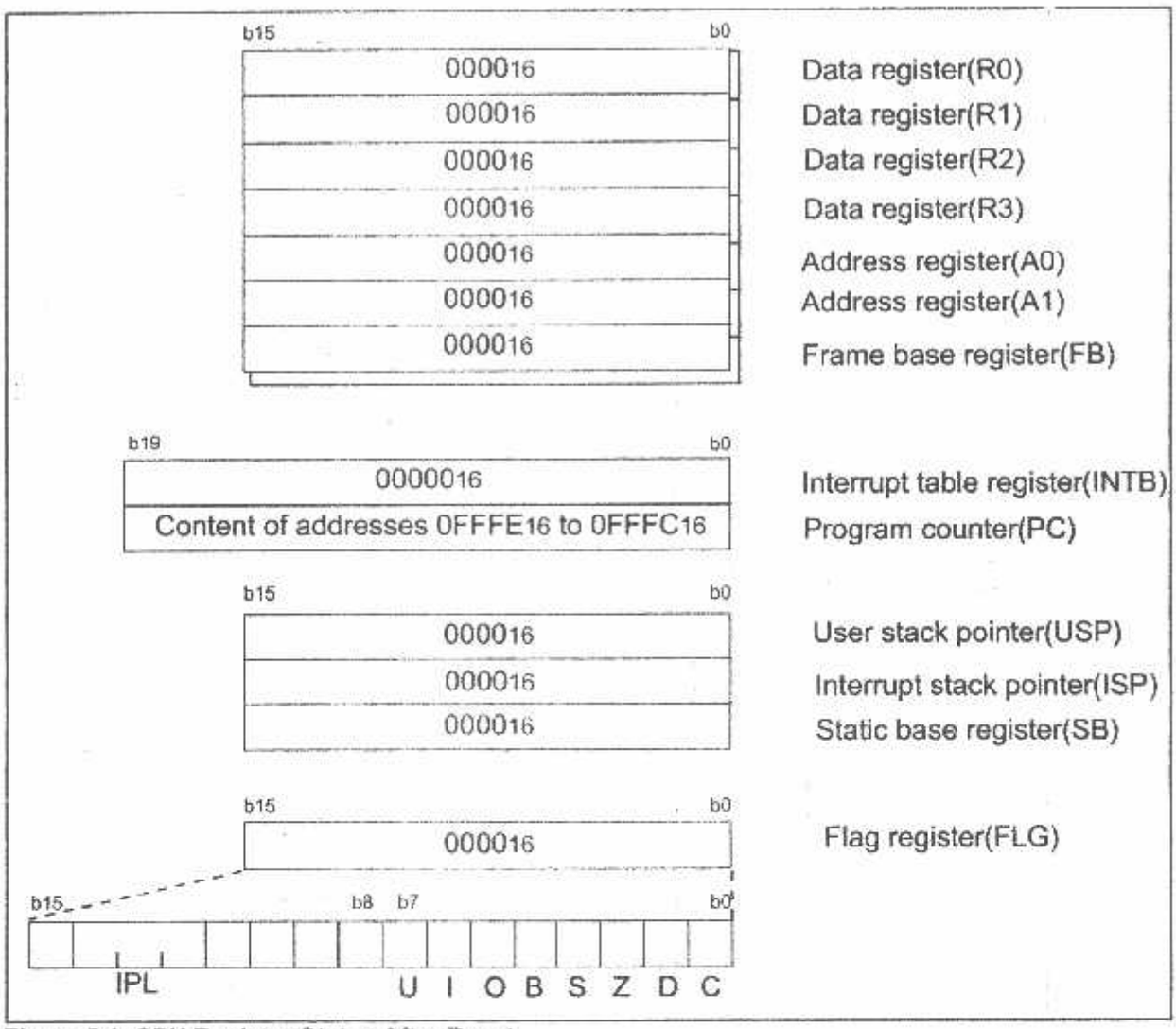


Figure 5.1 CPU Register Status After Reset

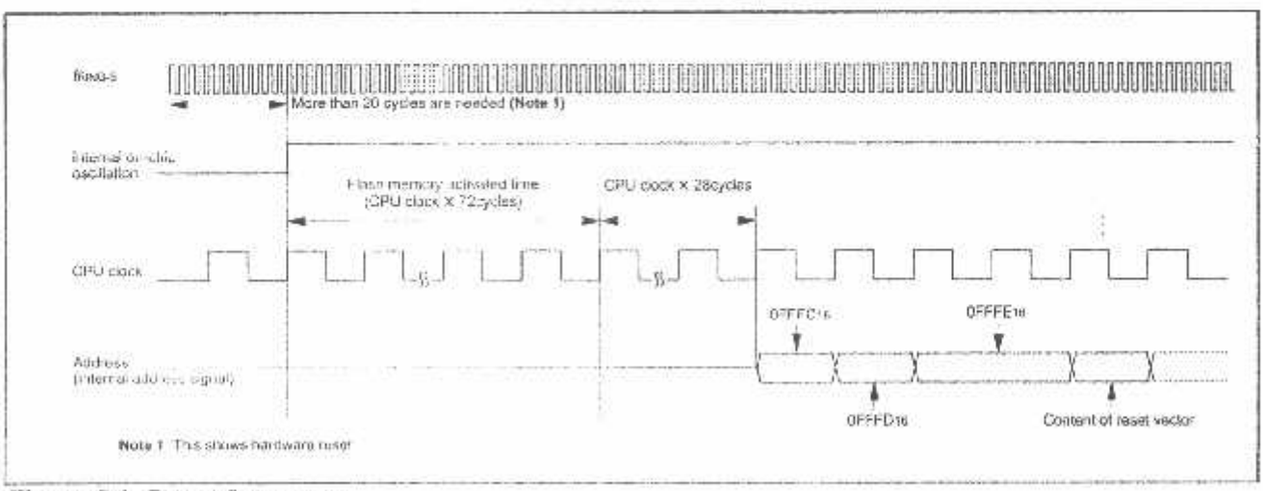


Figure 5.2 Reset Sequence

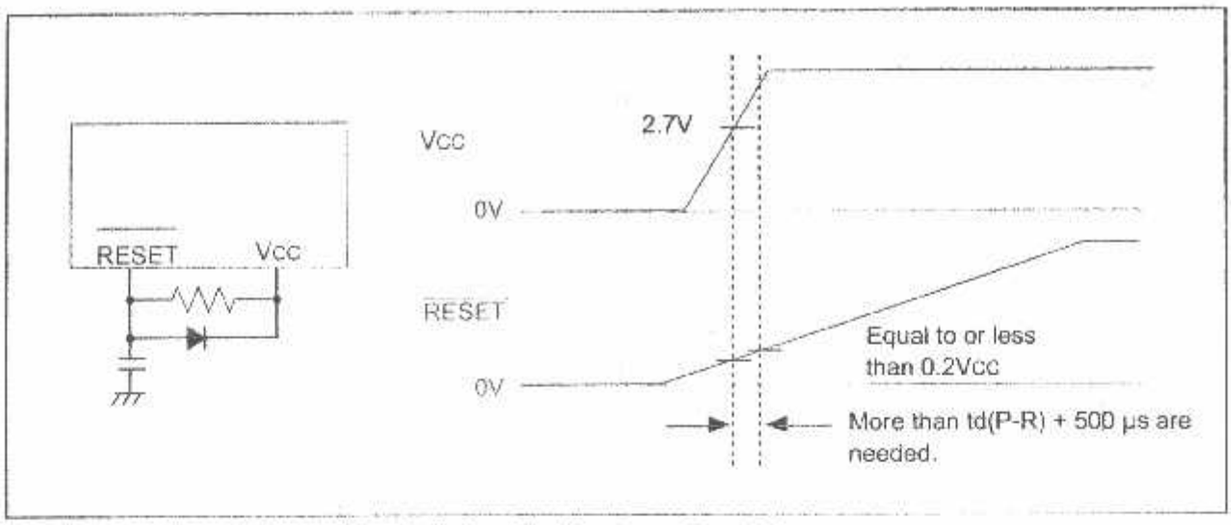


Figure 5.3 Example Reset Circuit Using The Hardware Reset 1

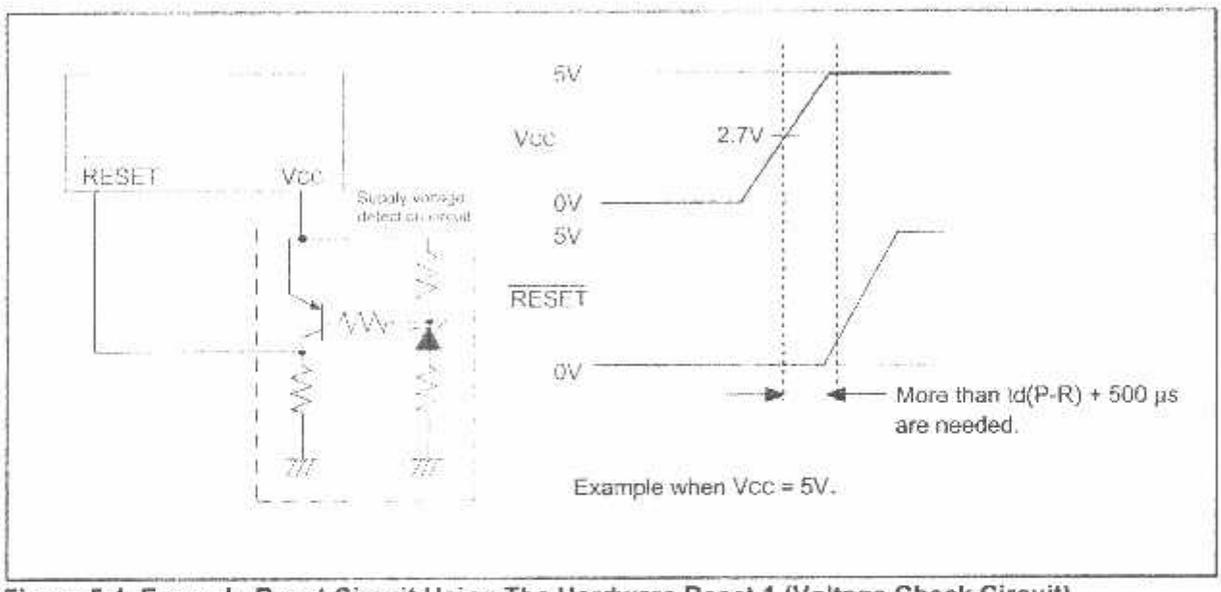


Figure 5.4 Example Reset Circuit Using The Hardware Reset 1 (Voltage Check Circuit)

5.1.2 Hardware Reset 2

This is the reset generated by the voltage detection circuit which is built-in to the microcomputer. The voltage detection circuit monitors the input voltage at Vcc input pin. The microcomputer is reset when the voltage at the VCC input pin drops below Vdet if all of the following conditions hold true.

- The VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled)
- The D40 bit in the D4INT register is set to "1" (voltage detection interrupt enabled)
- The D46 bit in the D4INT register is set to "1" (hardware reset 2 when going through Vdet)

When using a digital filter (D41 bit in the D4INT register is set to "1"), set the CM14 bit in the CM1 register to "0"(low-speed on-chip oscillator oscillates).

Conversely, when the input voltage at the Vcc pin rises to Vdet or more, the pins, CPU, and SFR are initialized and counting the low-speed on-chip oscillator starts. When counting the low-speed on-chip oscillator clock 32 times, the internal reset is exited and the program is executed beginning with the address indicated by the reset vector. The initialized pins and registers and the status thereof are the same as in hardware reset 1. Refer to Section 5.4 "Voltage Detection Circuit."

5.1.3 Power-on Reset Function

The power-on reset is the function which can reset the microcomputer without the external reset circuit. The $\overline{\text{RESET}}$ pin should be connected to the Vcc pin via about 5 kΩ pull-up resistance using the power-on reset function, the function turns to active and the microcomputer has its pins, CPU, and SFR initialized.

When the input voltage at the Vcc pin reaches to the Vdet level, count operation of the low-speed on-chip oscillator clock starts. When the operation counts the low-speed on-chip oscillator clock for 32 times, the internal reset is released. Then the program is executed starting from the address indicated by the reset vector. The initialized pins and registers and the status thereof are the same as in hardware reset 1 excluding the following bits.

- The D40 bit in the D4INT register turns to "1" automatically (voltage detection interrupt enabled)
- The D46 bit in the D4INT register turns to "1" automatically (hardware reset 2 when going through Vdet)

Additionally, the hardware reset 2 turns to active after the power-on reset. This is because the VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled) after the power-on reset same as the hardware reset 1, so that hardware reset 2 active conditions are all satisfied including above D40 and D46 bit conditions.

Figure 5.5 shows the power-on reset circuit. Figure 5.6 shows the power-on reset operation.

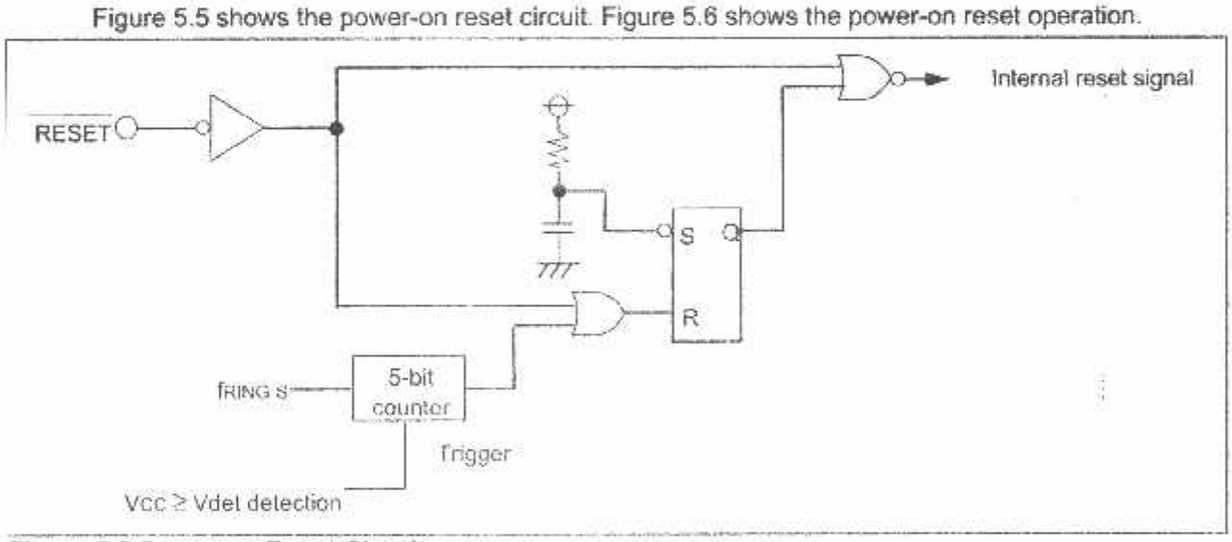
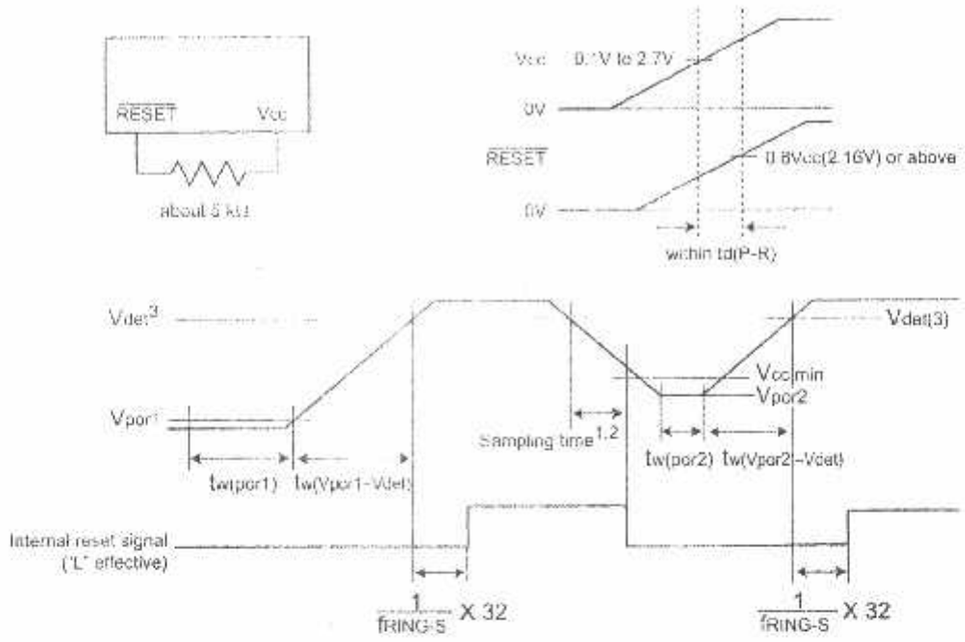


Figure 5.5 Power-on Reset Circuit



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Detection Circuit" for details.
4. Refer to Table 16.7, 16.8 for electrical characteristics.

Figure 5.6 Power-on Reset Operation

5.2 Software Reset

When the PM03 bit in the PM0 register is set to "1" (microcomputer reset), the microcomputer has its pins, CPU, and SFR initialized. Then the program is executed starting from the address indicated by the reset vector.

After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected for the CPU.

Some SFRs are not initialized by the software reset. Refer to Chapter 4, "SFR."

5.3 Watchdog Timer Reset

Where the PM12 bit in the PM1 register is "1" (reset when watchdog timer underflows), the microcomputer initializes its pins, CPU and SFR if the watchdog timer underflows. Then the program is executed starting from the address indicated by the reset vector.

After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected for the CPU.

Some SFRs are not initialized by the watchdog timer reset. Refer to Chapter 4, "SFR."

5.4 Voltage Detection Circuit

The voltage detection circuit monitors the input voltage at the Vcc pin with respect to Vdet. The user program can check for voltage detection using the VC13 bit or set up the voltage detection interrupt register to generate a hardware reset 2 or voltage detection interrupt.

Figure 5.7 shows the voltage detection circuit. Figure 5.8 shows VCR1 and VCR2 registers. Figure 5.9 shows the D4INT register. Figure 5.10 shows an operation example of the voltage detection circuit. Figure 5.11 to 5.12 show the operation example of the voltage detection circuit to get out of stop mode.

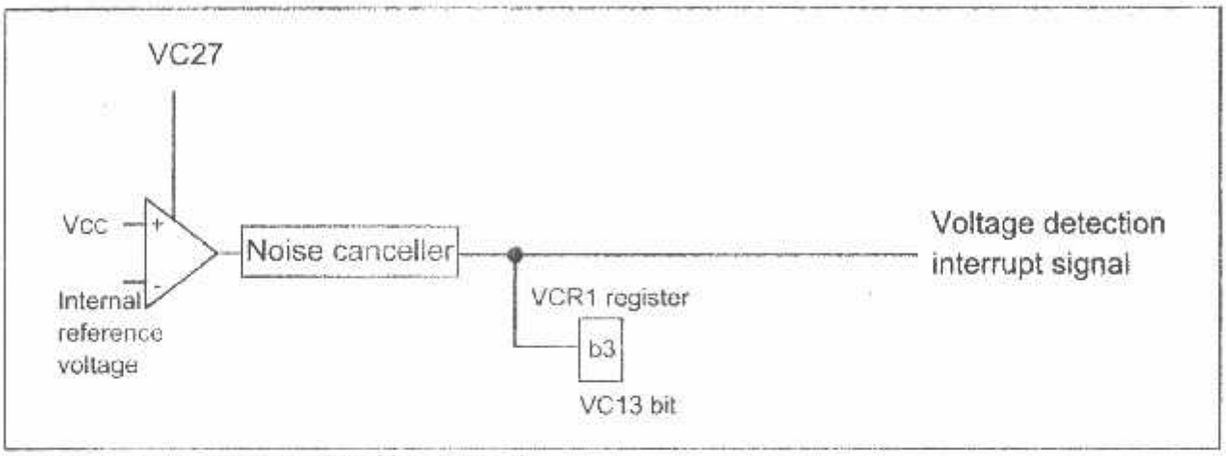


Figure 5.7 Voltage Detection Circuit Block

Voltage detection register 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0	0	0

Symbol: VCR1 Address: 001916 After reset(2): 000010002

Bit symbol	Bit name	Function	RW
(b2 b0)	Reserved bit	Should set to "0"	RW
VC13	Voltage monitor flag(1)	0:Vcc < Vdet 1:Vcc ≥ Vdet or voltage detection circuit disabled	RO
(b7-b4)	Reserved bit	Should set to "0"	RW

Notes:
1. The VC13 bit is valid when the VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled). The VC13 bit is set to "1" (Vcc≥Vdet or voltage detection circuit disabled) when the VC27 bit in the VCR2 register is set to "0" (voltage detection circuit disabled).
2. Software reset or the watchdog timer reset does not affect this register.

Voltage detection register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0

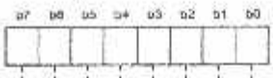
Symbol: VCR2 Address: 001A16 After reset(3): Reset input : 00162 RESET pin = "H" retaining : 100000002

Bit symbol	Bit name	Function	RW
(b6-b0)	Reserved bit	Should set to "0"	RW
VC27	Voltage monitor enable bit(2)	0: Voltage detection circuit disabled 1: Voltage detection circuit enabled	RW

Notes:
1. Set the PRC3 bit in the PRCR register to "1" (write enabled) before writing to this register.
2. Set the VC27 bit to "1" (voltage detect circuit enabled) when hardware reset 2 is used. After the VC27 bit is set to "1", the voltage detection circuit elapses for td(E-A) before starting operation.
3. Software reset or the watchdog timer reset does not affect this register.

Figure 5.8 VCR1 Register and VCR2 Register

Voltage detection interrupt register[1]



Symbol D4INT | Address 001F16 | After reset[10] Reset input : 0016 RESET pin = H retaining : 010000012

Bit symbol	Bit name	Function	RW
D40	Voltage detection interrupt enable bit[7]	0 : Disable 1 : Enable	RW
D41	Voltage detection digital filter disable mode select bit	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	RW
D42	Voltage change detection flag[3, 4, 5]	0: Not detected 1: Vdet passing detection	RW
D43	WDT overflow detect flag[3, 4]	0: Not detected (flag clear) 1: Detected	RW
DF0	Sampling clock select bit	b5b4 00 : fRING-S divided by 1 01 : fRING-S divided by 2 10 : fRING-S divided by 4 11 : fRING-S divided by 8	RW
DF1			RW
D46	Voltage monitor mode select bit[6]	0: Voltage detection interrupt request is generated when passing through Vdet 1: Hardware reset 2 when passing through Vdet	RW
D47	Voltage detection condition select bit[11]	Voltage detection interrupt request is generated or hardware reset 2 when Vcc passes Vdet[9] 0: Over Vdet 1: Below Vdet	RW

Notes:
1. Set the PRC3 bit in the PRCR register to "1" (write enable) before writing to this register.
2. If the voltage detection interrupt needs to be used to get out of stop mode again after once used for that purpose, reset the D41 bit by writing a "0" and then a "1".
3. Valid when the VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled).
4. If the VC27 bit is set to "0" (voltage detection circuit disabled), the D42 and D43 bits are set to "0" (not detected).
5. This bit is set to "0" by writing a "0" in a program. (writing a "1" has no effect.)
6. Valid when the D40 bit is set to "1" (voltage detection interrupt enabled).
7. The D40 bit is valid when the VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled). When setting the D40 bit to "1", the following setting is required.
   (1) Set the VC27 bit "1".
   (2) Wait for td(E-A) until the detecter circuit operates.
   (3) Wait for the sampling time (the sampling clock which is selected in the DF0 bit to DF1 bit times 4 cycles.)
   (4) Set the D40 bit to "1".
   (5) Set the CM14 bit in the CM1 register to "0" (low-speed on-chip oscillator on).
8. Valid when the D41 bit is set to "1" (digital filter disabled mode).
9. The D46 bit can be selected.
10. The software reset or the watchdog timer reset do not affect this register.
11. When the D46 bit is set to "1" (hardware reset 2 when Vdet passes), set the D47 bit to "1" (below Vdet). (Do not set to "0").

Figure 5.9 D4INT Register

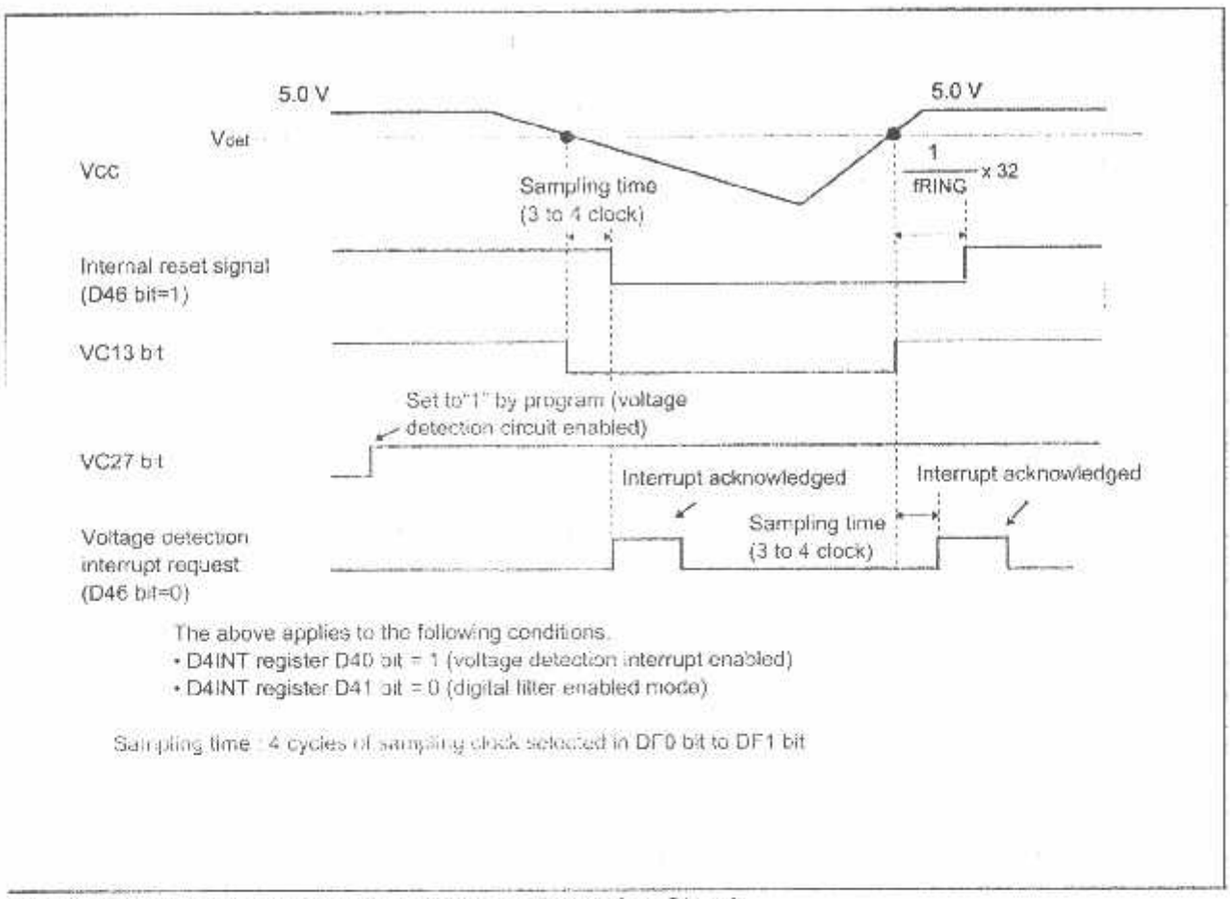


Figure 5.10 Operation Example of Voltage Detection Circuit

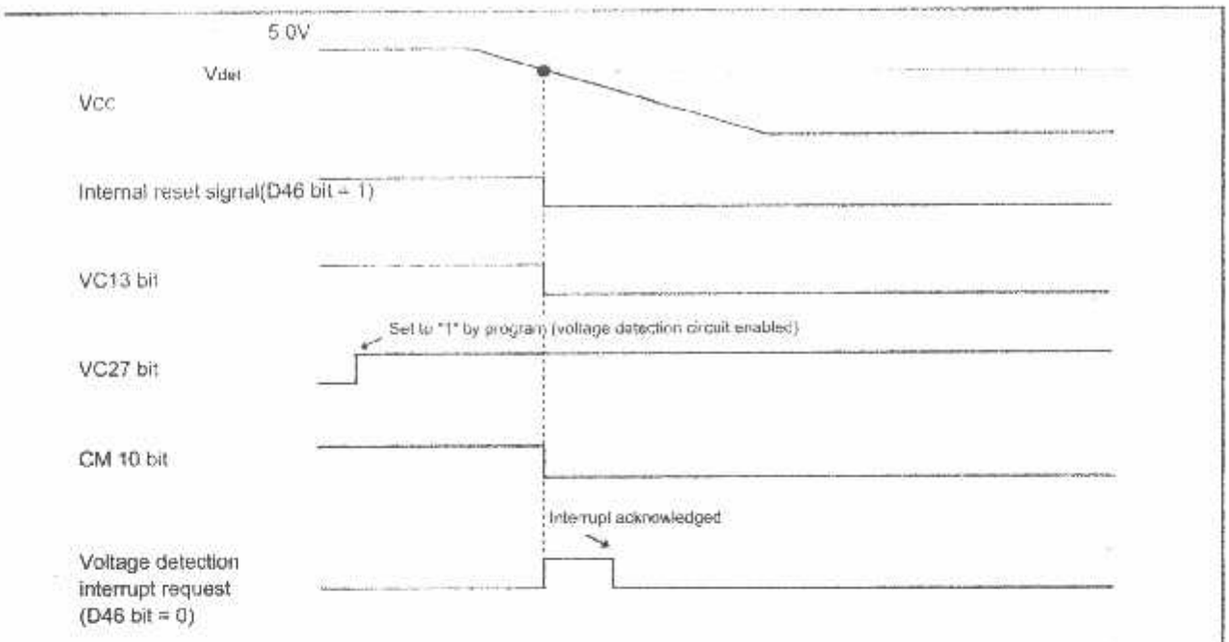


Figure 5.11 Operation Example of Voltage Detection Circuit to get out of Stop mode (1)

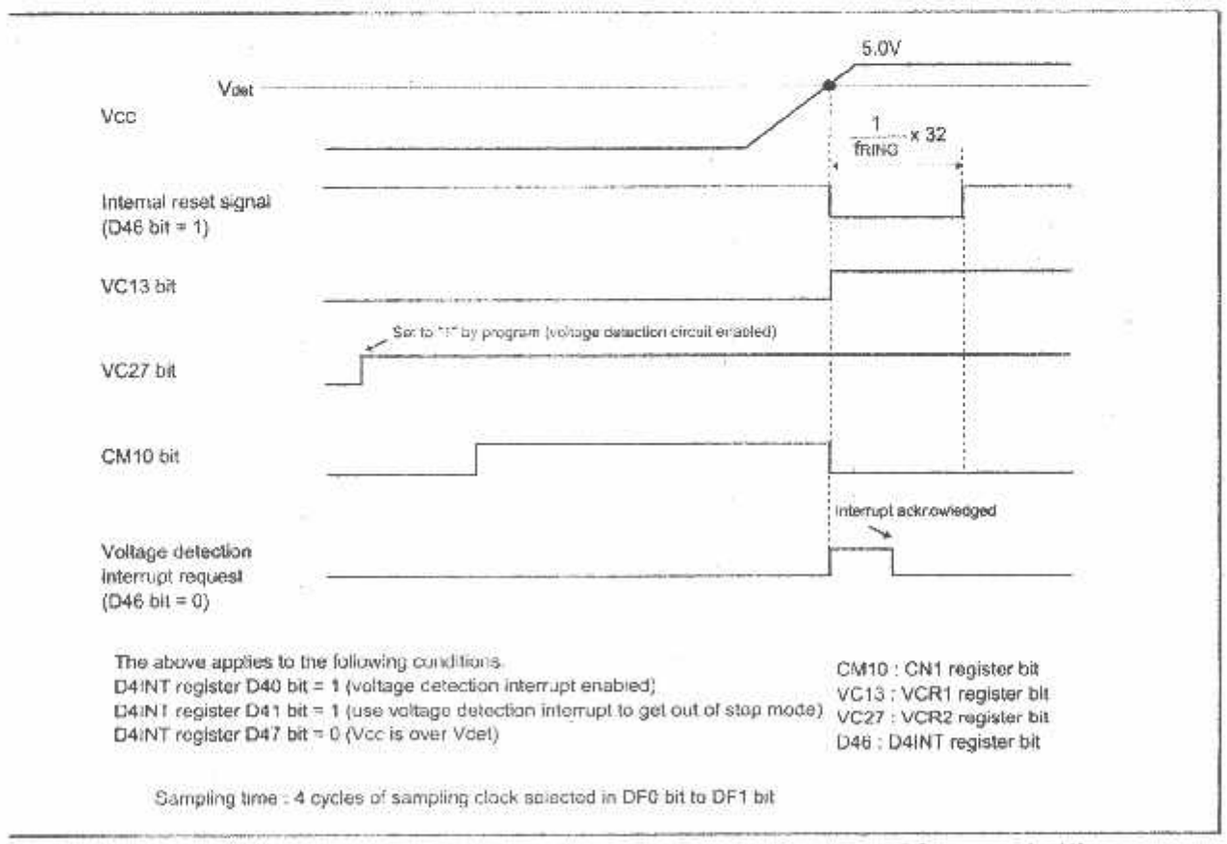


Figure 5.12 Operation Example of Voltage Detection Circuit to get out of Stop mode (2)

5.4.1 Voltage Detection Interrupt

Figure 5.13 shows the block diagram of voltage detection interrupt generation circuit.
Refer to 5.4.2. "Exiting Stop Mode on a Voltage Detection Circuit" for Getting out of stop mode due to the voltage detection interrupt.

A voltage detection interrupt is generated when the input voltage at the Vcc pin rises to Vdet or more or drops below Vdet if all of the following conditions hold true in normal operation mode and wait mode.

- The VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled)
- The D40 bit in the D4INT register is set to "1" (voltage detection interrupt enabled)
- The D46 bit in the D4INT register is set "0" (voltage detection interrupt selected)

To use the digital filter (D41 bit in the D4INT register is set to "0"), set the CM14 bit in the CM1 register to "0" (low-speed on-chip oscillator on). Figure 5.14 shows an operation example of voltage detection interrupt generation circuit.
The voltage detection interrupt shares the interrupt vector with the watchdog timer interrupt and oscillation stop detection interrupt.
The D42 bit in the D4INT register becomes "1" when passing through Vdet is detected after the voltage inputted to the Vcc pin is up or down.
A voltage detection interrupt request is generated when the D42 bit changes state from "0" to "1". The D42 bit needs to be set to "0" in a program.
Table 5.2 lists the voltage detection interrupt request generation conditions.
It takes 4 cycles of sampling clock until the D42 bit is set to "1" since the voltage which inputs to Vcc pin passes Vdet.
It is possible to set the sampling clock detecting that the voltage applied to the Vcc pin has passed through Vdet with the DF0 to DF1 bits in the D4INT register.

Table 5.2 Voltage Detection Interrupt Request Generation Conditions

Operation mode	VC27 bit	D40 bit	D41 bit	D42 bit	D46 bit	VC13 bit	CM14 bit
Normal operation mode[1]	1	1	0 or 1	0	0	From 0 to 1[2]	0
						From 1 to 0[2]	
Wait mode	1	1	0 or 1	0	0	From 0 to 1[2]	0
						From 1 to 0[2]	

Notes:
1. The status except the wait mode and stop mode is handled as the normal mode. (Refer to Chapter 6, "Clock Generation Circuit.")
2. Refer to Figure 5.14, "Operation Example of Voltage Detection Interrupt Generation Circuit" for interrupt generation timing.

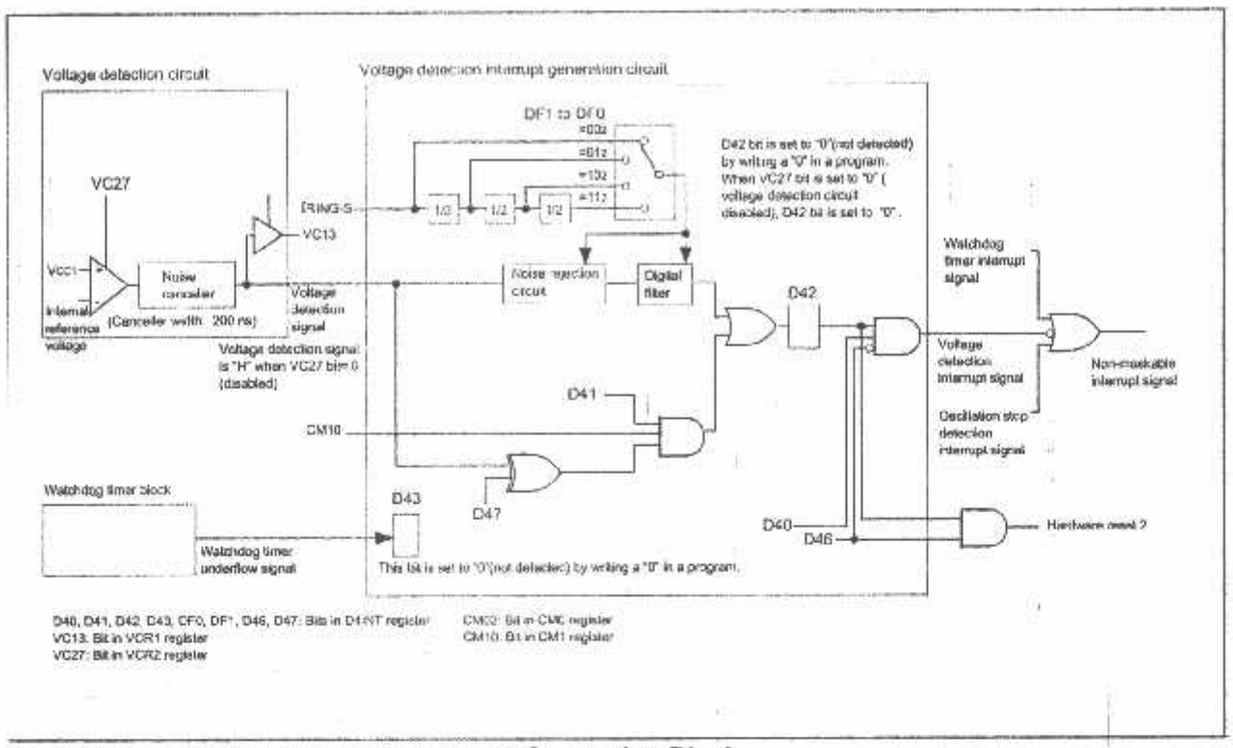


Figure 5.13 Operation Detection Interrupt Generation Block

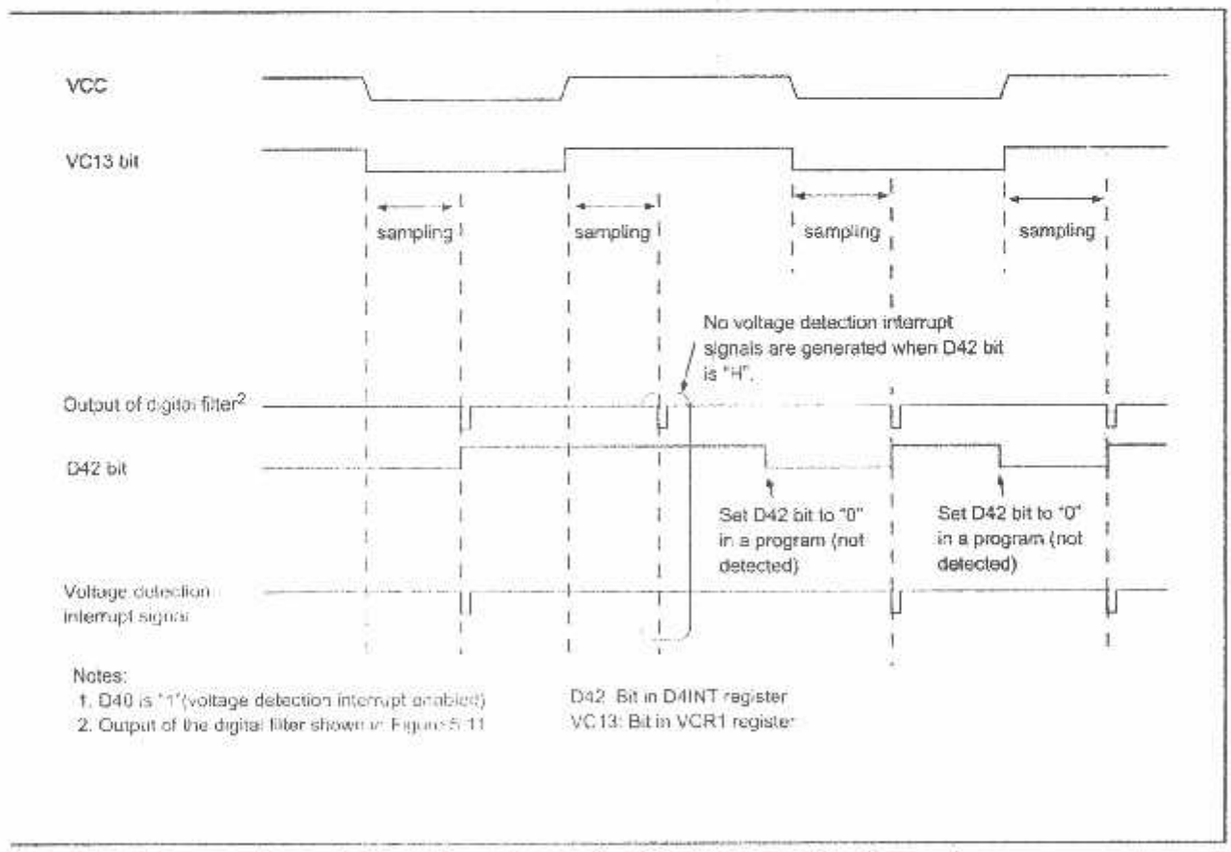


Figure 5.14 Voltage Detection Interrupt Generation Circuit Operation Example

5.4.2 Exiting Stop Mode on a Voltage Detection Interrupt

A voltage detection interrupt is generated when the input voltage at the Vcc pin rises to Vdet or more or drops below Vdet if all of the following conditions hold true in stop mode.

- The VC27 bit in the VCR2 register is set to "1" (voltage detection circuit enabled)
- The D40 bit in the D4INT register is set to "1" (voltage detection interrupt enabled)
- The D41 bit in the D4INT register is set "1" (digital filter disabled mode)
- The D46 bit in the D4INT register is set "0" (voltage detection interrupt selected)

The voltage detection interrupt shares the interrupt vector with the watchdog timer interrupt and oscillation stop detection interrupt.
The D42 bit in the D4INT register becomes "1" when passing through Vdet is detected after the voltage inputted to the Vcc pin is up or down.
A voltage detection interrupt request is generated when the D42 bit changes state from "0" to "1". The D42 bit needs to be set to "0" in a program.
Table 5.3 lists the voltage detection interrupt request generation conditions to get out of stop mode.

Table 5.3 Voltage Detection Interrupt Request Generation Conditions to get out of Stop mode

Operation mode	VC27 bit	D40 bit	D41 bit	D42 bit	D46 bit	D47 bit	VC13 bit
Stop mode	1	1	1	0	0	0 or 1	From 0 to 1
							From 1 to 0

Notes:
1. The status except the wait mode and stop mode is handled as the normal mode. (Refer to Chapter 6, "Clock Generation Circuit.")
2. Refer to Figure 5.14, "Operation Example of Voltage Detection Interrupt Generation Circuit" for interrupt generation timing.

. Clock Generation Circuit

The clock generation circuit contains two oscillator circuits as follows:

- Main clock oscillation circuit
- On-chip oscillator (oscillation stop detect function)

Table 6.1 lists the clock generation circuit specifications. Figure 6.1 shows the clock generation circuit. Figures 6.2 to 6.4 show the clock-related registers.

Table 6.1 Clock Generation Circuit Specifications

Item	Main clock oscillation circuit	On-chip oscillator	
		High-speed on-chip oscillator	Low-speed on-chip oscillator
Use of clock	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating
Clock frequency	0 to 20 MHz	Approx. 8 MHz	Approx. 125 kHz
Usable oscillator	• Ceramic resonator • Crystal oscillator	———	———
Pins to connect oscillator	XIN, XOUT[1]	Note[1]	Note[1]
Oscillation starts and stops	Present	Present	Present
Oscillator status after reset	Stopped	Stopped	Oscillating
Other	Externally derived clock can be input[2]	———	———

Notes:
1. Can be used as P46 and P47 when the on-chip oscillator clock is used for CPU clock while the main clock oscillation circuit is not used.
2. Set the CM05 bit in the CM0 register to "1" (main clock stops) and the CM13 bit in the CM1 register to "1" (XIN-XOUT pin) when the external clock is input.

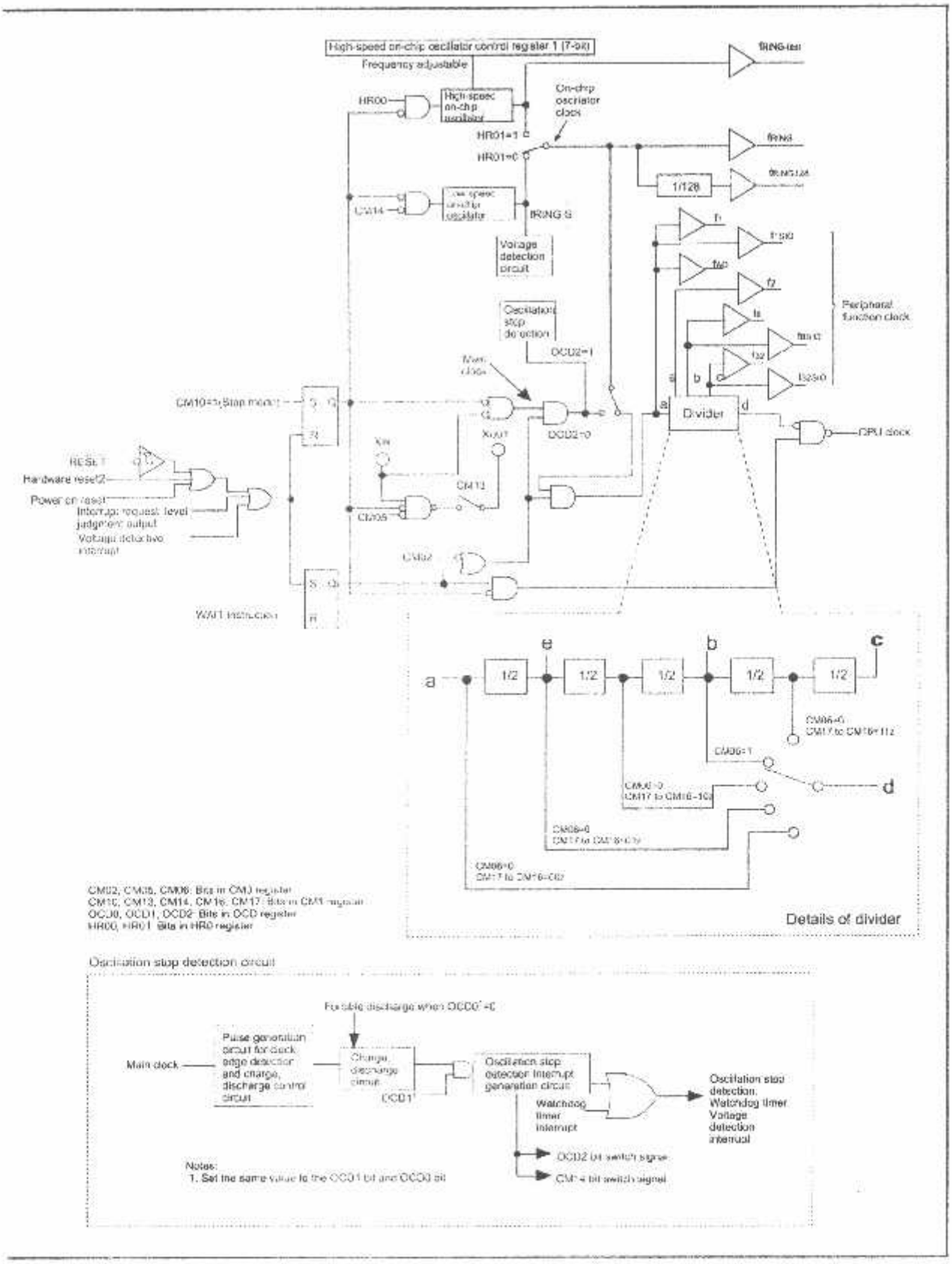


Figure 6.1 Clock Generation Circuit

System clock control register 0[1]

b7	b6	b5	b4	b3	b2	b1	b0
0			0	1		0	0

Symbol: CM0 Address: 000616 After reset: 6816

Bit symbol	Bit name	Function	RW
(b1-b0)	Reserved bit	Set to "0"	RW
CM02	WAIT peripheral function clock stop bit	0 : Do not stop peripheral function clock in wait mode 1 : Stop peripheral function clock in wait mode	RW
(b3)	Reserved bit	Set to "1"	RW
(b4)	Reserved bit	Set to "0"	RW
CM05	Main clock (XIN-XOUT) stop bit[2, 4]	0 : On 1 : Off[3]	RW
CM06	CPU clock division select bit 0[5]	0 : CM16 and CM17 valid 1 : Divide-by-8 mode	RW
(b7)	Reserved bit	Set to "0"	RW

Notes
1: Set the PRC0 bit of PRCR register to "1" (write enable) before writing to this register.
2: The CM05 bit is provided to stop the main clock when the on-chip oscillator mode is selected. This bit cannot be used for detection as to whether the main clock stopped or not. To stop the main clock, the following setting is required:
(1) Set the OCD0 and OCD1 bits in the OCD register to "002" (disable oscillation stop detection function).
(2) Set the OCD2 bit to "1" (on-chip oscillator clock selection).
3: Set the CM05 bit to "1" (main clock stops) and the CM13 bit in the CM1 register to "1" (XIN-XOUT pin) when the external clock is input.
4: When the CM05 bit is set to "1" (main clock stop), P46 and P47 can be used as input ports.
5: When entering stop mode from high or middle speed mode, the CM06 bit is set to "1" (divide-by-8 mode).

System clock control register 1[1]

b7	b6	b5	b4	b3	b2	b1	b0
					0	0	

Symbol: CM1 Address: 000716 After reset: 2016

Bit symbol	Bit name	Function	RW
CM10	All clock stop control bit[4, 7]	0 : Clock on 1 : All clocks off (stop mode)	RW
(b1)	Reserved bit	Set to "0"	RW
(b2)	Reserved bit	Set to "0"	RW
CM13	Port XIN-XOUT switch bit[7]	0 : Input port P46, P47 1 : XIN-XOUT pin	RW
CM14	Low-speed on-chip oscillation stop bit[5, 6]	0 : Low-speed on-chip oscillator on 1 : Low-speed on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit[2]	0 : LOW 1 : HIGH	RW
CM16	CPU clock division select bit 1[3]	b7 b6 0 0 : No division mode 0 1 : Division by 2 mode 1 0 : Division by 4 mode 1 1 : Division by 16 mode	RW
CM17			RW

Notes:
1: Write to this register after setting the PRC0 bit of PRCR register to "1" (write enable).
2: When entering stop mode from high or middle speed mode, the CM15 bit is set to "1" (drive capacity high).
3: Effective when the CM06 bit is "0" (CM16 and CM17 bits enable).
4: If the CM10 bit is "1" (stop mode), the internal feedback resistor becomes ineffective.
5: The CM14 bit can be set to "1" (low-speed on-chip oscillator off) if the OCD2 bit=0 (main clock selected). When the OCD2 bit is set to "1" (selecting on-chip oscillator clock), the CM14 bit is set to "0" (low-speed on-chip oscillator on). This bit remains unchanged when "1" is written.
6: When using voltage detection interrupt circuit, CM14 bit is set to "0".
7: When the CM10 bit is set to "1" (stop mode) or the CM05 bit in the CM0 register to "1" (main clock stops) and the CM13 bit is set to "1" (XIN-XOUT pin), the XOUT (P47) pin becomes "H".
When the CM13 bit is set to "0" (input ports P46, P47), the P47 (XOUT) enters input mode.

Figure 6.2 CM0 Register and CM1 Register

Oscillation stop detection register[1]

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol: OCD | Address: 000C16 | After reset: 0416

Bit symbol	Bit name	Function	RW
OCD0	Oscillation stop detection enable bit	b1 b0 0 0: The function is disabled[4] 0 1: Do not set 1 0: Do not set 1 1: The function is enabled[7]	RW
OCD1			
OCD2	System clock select bit[6]	0: Select main clock[7] 1: Select on-chip oscillator clock[2]	RW
OCD3	Clock monitor bit[3, 5]	0: Main clock on 1: Main clock off	RO
(b7-b4)	Reserved bit	Set to "0"	RW

Notes:
1. Set the PRC0 bit in the PRCR register to "1" (write enable) before rewriting this register.
2. The OCD2 bit is set to "1" (selecting on-chip oscillator clock) automatically if a main clock oscillation stop is detected while the OCD1 to OCD0 bits are set to "11₂" (oscillation stop detection function enabled). If the OCD3 bit is set to "1" (main clock stops), the OCD2 bit remains unchanged when trying to write "0" (main clock selected).
3. The OCD3 bit is enabled when the OCD1 to OCD0 bits are set to "11₂" (oscillation stop detection function enabled). Read the OCD3 bit several times with the oscillation stop detection interrupt processing program to determine the main clock state.
4. The OCD1 to OCD0 bits should be set to "00₂" (oscillation stop detection function disabled) before entering stop mode or on-chip oscillator (main clock stops).
5. The OCD3 bit remains set to "0" (main clock on) if the OCD1 to OCD0 bits are set to "00₂".
6. The CM14 bit goes to "0" (low-speed on-chip oscillator on) if the OCD2 bit is set to "1" (on-chip oscillator clock selected).
7. Refer to Figure 6.7 "switching clock source from low-speed on-chip oscillator to main clock" for the switching procedure when the main clock re-oscillates after detecting an oscillation stop.

Figure 6.3 OCD Register

High-speed on-chip oscillator control register 0[3]

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	

Symbol: HR0 Address: 0008₁₆ After reset: 00₁₆

Bit symbol	Bit name	Function	RW
HR00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	RW
HR01	High-speed on-chip oscillator select bit	0: Low-speed on-chip oscillator selected[2] 1: High-speed on-chip oscillator selected	RW
(b7-b2)	Reserved bit	Set to "0"	RW

Notes:
1. The HR01 bit should be changed under the following conditions.
   - HR00 = 1 (high-speed on-chip oscillator on)
   - CM1 register CM14 bit = 0 (low-speed on-chip oscillator on)
2. When writing "0"(low-speed on-chip oscillator selected) to the HR01 bit, do not write "0"(high-speed on-chip oscillator stops) to the HR00 bit simultaneously. Set the HR00 bit to "0" after setting the HR01 bit to "0".
3. Set the PRC0 bit in the PRCR register to "1" (write enable) before rewriting this register.

High-speed on-chip oscillator control register 1[1]

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol: HR1 Address: 000B₁₆ After reset: 40₁₆

Function	RW
The frequency of high-speed on-chip oscillator is adjusted with bits 0 to bits 6. Period of high-speed on-chip oscillator = fd(HR offset) + (64 × b6 + 32 × b5 + 16 × b4 + 8 × b3 + 4 × b2 + 2 × b1 + b0) × fd(HR) Bit 7 should be set to "0".	RW

Note:
1. Set the PRC0 bit in the PRCR register to "1" (write enable) before rewriting this register.

Figure 6.4 HR0 Register and HR1 Register

The following describes the clocks generated by the clock generation circuit.

6.1 Main Clock

This clock is supplied by a main clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The main clock oscillator circuit is configured by connecting a resonator between the XIN and XOUT pins. The main clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The main clock oscillator circuit may also be configured by feeding an externally generated clock to the XIN pin. Figure 6.5 shows examples of main clock connection circuit.

During reset and after reset, the main clock is turned off.

The main clock starts oscillating when the CM05 bit in the CM0 register is set to "0" (main clock on) after setting the CM13 bit in the CM1 register to "1" (XIN- XOUT pin).

To use the main clock for the CPU clock, set the OCD2 bit in the OCD register to "0" (selecting main clock) after the main clock becomes oscillating stably.

The power consumption can be reduced by setting the CM05 bit in the CM0 register to "1" (main clock off) if the OCD2 bit is set to "1" (on-chip oscillator clock selected).

Note that if an externally generated clock is fed into the XIN pin, the main clock cannot be turned off by setting the CM05 bit to "1". If necessary, use an external circuit to turn off the clock.

During stop mode, all clocks including the main clock are turned off. Refer to Section 6.4, "Power Control."

Note: Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the maker of the oscillator.
When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip, insert a feedback resistor between XIN and XOUT following the instruction.

Figure 6.5 Examples of Main Clock Connection Circuit

6.2 On-Chip Oscillator Clock

This clock is supplied by a on-chip oscillator. There are two kinds of on-chip oscillator: high-speed on-chip oscillator and low-speed on-chip oscillator. These oscillators are selected by the bit HR01 bit in the HR0 register.

6.2.1 Low-Speed On-Chip Oscillator Clock

The clock derived from the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, f_{RING}, $f_{RING128}$ and f_{RING-S}.

After reset, the on-chip oscillator clock derived from low-speed on-chip oscillator by divided by 8 is selected for the CPU clock.

If the main clock stops oscillating when the OCD1 to OCD0 bits in the OCD register are "11$_2$" (oscillation stop detection function enabled), the low-speed on-chip oscillator automatically starts operating, supplying the necessary clock for the microcomputer.

The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operation ambient temperature. The application products must be designed with sufficient margin to accommodate the frequency range.

6.2.2 High-Speed On-Chip Oscillator Clock

The clock derived from high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, f_{RING}, $f_{RING128}$, and $f_{RING1\text{-}fast}$.

After reset, the on-chip oscillator clock derived from high-speed on-chip oscillator is halted. The oscillation is started by setting the HR00 bit in the HR0 register to "1" (high-speed on-chip oscillator on). The frequency can be adjusted by the HR1 register.

The relationship between the value of HR1 register and the period of high-speed on-chip oscillator is shown below. It is noted that the difference in delay between the bits should be adjusted by changing each bit. Bit 7 should be set be "0".

Period of high-speed on-chip oscillator = td(HR offset) + (64 × b6 + 32 × b5 + 16 × b4 + 8 × b3 + 4 × b2 + 2 × b1 + b0) × td(HR)

b0 to b6 : Bits in HR1 register

6.3 CPU Clock and Peripheral Function Clock

There are two types of clocks: CPU clock to operate the CPU and peripheral function clock to operate the peripheral functions. Also refer to "Figure 6.1 Clock Generating Circuit".

6.3.1 CPU Clock

This is an operating clock for the CPU and watchdog timer.

The clock source for the CPU clock can be chosen to be the main clock or on-chip oscillator clock.

The selected clock source can be divided by 1 (undivided), 2, 4, 8 or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register and the CM17 to CM16 bits in the CM1 register to select the divide-by-n value.

After reset, the low-speed on-chip oscillator clock divided by 8 provides the CPU clock.

Note that when entering stop mode from high or middle speed mode, the CM06 bit is set to "1" (divide-by-8 mode).

6.3.2 Peripheral Function Clock (f_1, f_2, f_8, f_{32}, f_{AD}, f_{1SIO}, f_{8SIO}, f_{32SIO}, f_{RING}, $f_{RING128}$)

These are operating clocks for the peripheral functions.

Of these, fi (i=1, 2, 8, 32) is derived from the main clock or on-chip oscillator clock by dividing them by i. The clock fi is used for timers X, Y, Z and C.

The clock f_{jSIO} (j=1, 8, 32) is derived from the main clock or on-chip oscillator clock by dividing them by j. The clock f_{jSIO} is used for serial interface.

The f_{AD} clock is produced from the main clock or the on-chip oscillator clock and is used for the A/D converter.

When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to "1" (peripheral function clock turned off during wait mode), the clocks fi, f_{jSIO}, and f_{AD} are turned off.

6.3.3 f_{RING} and $f_{RING128}$

These are operating clocks for the peripheral functions.

The f_{RING} runs at the same frequency as the on-chip oscillator, and can be used as the souce for the timer Y. The $f_{RING128}$ is derived from the f_{RING} by dividing it by 128, and can be used for Timer C.

When the WAIT instruction is executed, the clocks f_{RING} and $f_{RING128}$ are not turned off.

6.3.4 f_{RING}-fast

This is used as the count source for the timer C. The f_{RING}-fast is derived from the high-speed on-chip oscillator and provided by setting the HR00 bit to "1" (high-speed on-chip oscillator on).

When the WAIT instruction is executed, the clock f_{RING}-fast is not turned off.

6.4 Power Control

There are three power control modes. All modes other than wait and stop modes are referred to as normal operation mode.

6.4.1 Normal Operation Mode

Normal operation mode is further classified into four modes.

In normal operation mode, because the CPU clock and the peripheral function clocks both are on, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the greater the processing capability. The lower the CPU clock frequency, the smaller the power consumption in the chip. If the unnecessary oscillator circuits are turned off, the power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source to which switched must be oscillating stably. If the new clock source is the main clock, allow a sufficient wait time in a program until it becomes oscillating stably.

- **High-speed Mode**

  The main clock divided by 1 (undivided) provides the CPU clock. If the CM14 bit is set to "0" (low-speed on-chip oscillator on) or the HR00 bit in the HR0 register is set to "1" (high-speed on-chip oscillator on), the f_{RING} and $f_{RING128}$ can be used for timers Y and C. When the HR00 bit is set to "1", f_{RING}-fast can be used for timer C.

- **Medium-speed Mode**

  The main clock divided by 2, 4, 8 or 16 provides the CPU clock. If the CM14 bit is set to "0" (low-speed on-chip oscillator on) or the HR00 bit in the HR0 register is set to "1" (high-speed on-chip oscillator on), the f_{RING} and $f_{RING128}$ can be used for timers Y and C. When the HR00 bit is set to "1", f_{RING}-fast can be used for timer C.

- **High-speed, Low-speed, On-Chip Oscillator Mode**

  The on-chip oscillator clock divided by 1 (undivided), 2, 4, 8 or 16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. When the HR00 bit is set to "1", f_{RING}-fast can be used for timer C.

Table 6.2 Setting Clock Related Bit and Modes

Modes		OCD register	CM1 register	CM0 register	
		OCD2	CM17, CM16	CM06	CM05
High-speed mode		0	00$_2$	0	0
Medium-speed mode	divided by 2	0	01$_2$	0	0
	divided by 4	0	10$_2$	0	0
	divided by 8	0	—	1	0
	divided by 16	0	11$_2$	0	0
High-speed, low-speed on-chip oscillator mode[1]	no division	1	00$_2$	0	0 or 1
	divided by 2	1	01$_2$	0	0 or 1
	divided by 4	1	10$_2$	0	0 or 1
	divided by 8	1	—	1	0 or 1
	divided by 16	1	11$_2$	0	0 or 1

Notes:
1. The low-speed on-chip oscillator is used as the on-chip oscillator clock when the CM1 register CM14 bit=0 (low-speed on-chip oscillator on) and HR0 register HR01 bit=0 (low-speed on-chip oscillator selected).
The high-speed on-chip oscillator is used as the on-chip oscillator clock when the HR0 register HR00 bit=1 (high-speed on-chip oscillator on) and HR01 bit=1 (high-speed on-chip oscillator selected).

6.4.2 Wait Mode

In wait mode, the CPU clock is turned off, so are the CPU and the watchdog timer because both are operated by the CPU clock. Because the main clock and on-chip oscillator clock both are on, the peripheral functions using these clocks keep operating.

- **Peripheral Function Clock Stop Function**

If the CM02 bit is "1" (peripheral function clocks turned off during wait mode), the f_1, f_2, f_8, f_{32}, f_{1SIO}, f_{8SIO}, f_{32SIO}, and f_{AD} clocks are turned off when in wait mode, with the power consumption reduced that much.

- **Entering Wait Mode**

The microcomputer is placed into wait mode by executing the WAIT instruction.

- **Pin Status During Wait Mode**

The status before wait mode is retained.

- **Exiting Wait Mode**

The microcomputer is moved out of wait mode by a hardware reset or peripheral function interrupt.

When using a hardware reset to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "000$_2$" (interrupts disabled) before executing the WAIT instruction.

The peripheral function interrupts are affected by the CM02 bit. If CM02 bit is "0" (peripheral function clocks not turned off during wait mode), all peripheral function interrupts can be used to exit wait mode. If CM02 bit is "1" (peripheral function clocks turned off during wait mode), the peripheral functions using the peripheral function clocks stop operating, so that only the peripheral functions clocked by external signals can be used to exit from wait mode.

Table 6. 3 lists the interrupts to exit wait mode and the usage conditions.

When using a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

1. In the ILVL2 to ILVL0 bits in the interrupt control register, set the interrupt priority level of the peripheral function interrupt to be used to exit wait mode.
   Also, for all of the peripheral function interrupts not used to exit wait mode, set the ILVL2 to ILVL0 bits to "000$_2$" (interrupt disable).
2. Set the I flag to "1".
3. Enable the peripheral function whose interrupt is to be used to exit wait mode.

In this case, when an interrupt request is generated and the CPU clock is thereby turned on, an interrupt sequence is executed.

The CPU clock turned on when exiting wait mode by a peripheral function interrupt is the same CPU clock that was on when the WAIT instruction was executed.

Table 6.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02=0	CM02=1
Serial interface interrupt	Can be used when operating with internal or external clock	Can be used when operating with external clock
Key input interrupt	Can be used	Can be used
A/D conversion interrupt	Can be used in one-shot mode	— (Do not use)
Timer X interrupt	Can be used in all modes	Can be used in event counter mode
Timer Y interrupt	Can be used in all modes	Can be used when counting inputs from CNTR1 pin in timer mode
Timer Z interrupt	Can be used in all modes	— (Do not use)
Timer C interrupt	Can be used in all modes	— (Do not use)
INT interrupt	Can be used	Can be used (INT0 and INT3 can be used if there is no filter.
Voltage detection interrupt	Can be used	Can be used
Oscillation stop detection interrupt	Can be used	— (Do not use)

6.4.3 Stop Mode

In stop mode, all oscillator circuits are turned off, so are the CPU clock and the peripheral function clocks. Therefore, the CPU and the peripheral functions clocked by these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to Vcc pin is VRAM or more, the internal RAM is retained.

However, the peripheral functions clocked by external signals keep operating. The following interrupts can be used to exit stop mode.

- Key interrupt
- $\overline{INT0}$ to $\overline{INT2}$ interrupts (INT0 can be used only when there is no filter.)
- INT3 interrupt (INT3 can be used when there is no filter and Timer C output compare mode (the TCC13 bit in the TCC1 register is set to "1")
- Timer X interrupt (when counting external pulses in event counter mode)
- Timer Y interrupt (when counting inputs from CNTR1 pin in timer mode)
- Serial interfaces interrupt (when external clock is selected)
- Voltage detection interrupt

• Entering Stop Mode

The microcomputer is placed into stop mode by setting the CM10 bit of CM1 register to "1" (all clocks turned off). At the same time, the CM06 bit of CM0 register is set to "1" (main clock oscillator circuit drive capability high). CM15 bit of CM10 register is set to "1" (main clock oscillator circuit drive capability high).

Before entering stop mode, set the OCD1 to OCD0 bits to "002" (oscillation stop detection function disable).

• Pin Status in Stop Mode

The status before wait mode is retained.

However, the XOUT(P47) pin is held "H" when the CM13 bit in the CM1 register is set to "1" (XIN-XOUT pin). The P47(XOUT) is in input state when the CM13 bit is set to "0" (input port P46, P47).

• Exiting Stop Mode

The microcomputer is moved out of stop mode by a hardware reset or peripheral function interrupt.

When using a hardware reset to exit stop mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "0002" (interrupts disabled) before setting the CM10 bit to "1".

When using a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to "1".

1. In the ILVL2 to ILVL0 bits in the interrupt control register, set the interrupt priority level of the peripheral function interrupt to be used to exit stop mode.
   Also, for all of the peripheral function interrupts not used to exit stop mode, set the ILVL2 to ILVL0 bits to "0002".
2. Set the I flag to "1".
3. Enable the peripheral function whose interrupt is to be used to exit stop mode.
   In this case, when an interrupt request is generated and the CPU clock is thereby turned on, an interrupt sequence is executed.

The main clock divided by 8 of the clock which is used right before stop mode is used for the CPU clock when exiting stop mode by a peripheral function interrupt.

6.5 Oscillation Stop Detection Function

The oscillation stop detection function is such that main clock oscillation circuit stop is detected. The oscillation stop detection function can be enabled and disabled by the OCD1 to OCD0 bits in the OCD register.

Table 6.4 lists the specifications of the oscillation stop detection function.

Where the main clock corresponds to the CPU clock source and the OCD1 to OCD0 bits are "11$_2$" (oscillation stop detection function enabled), the system is placed in the following state if the main clock comes to a halt:

- OCD register OCD2 bit = 1 (selecting on-chip oscillator clock)
- OCD register OCD3 bit = 1 (main clock stopped)
- CM1 register CM14 bit = 0 (low-speed on-chip oscillator oscillating)
- Oscillation stop detection interrupt request occurs

Table 6.4 Oscillation Stop Detection Function Specifications

Item	Specification
Oscillation stop detectable clock and frequency bandwidth	$f(X_{IN}) \geq 2$ MHz
Enabling condition for oscillation stop detection function	Set OCD1 to OCD0 bits to "11$_2$" (oscillation stop detection function enabled)
Operation at oscillation stop detection	Oscillation stop detection interrupt occurs

6.5.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares the vector with the watchdog timer interrupt. If the oscillation stop detection and watchdog timer interrupts both are used, the interrupt factor must be determined. Table 6.5 shows how to determine the interrupt factor with the oscillation stop detection interrupt, watchdog timer interrupt and voltage detection interrupt.
- Where the main clock re-oscillated after oscillation stop, the clock source for the CPU clock and peripheral functions must be switched to the main clock in the program.
  Figure 6.7 shows the procedure for switching the clock source from the low-speed on-chip oscillator to the main clock.
- To enter wait mode while using the oscillation stop detection function, set the CM02 bit to "0" (peripheral function clocks not turned off during wait mode).
- Since the oscillation stop detection function is provided in preparation for main clock stop due to external factors, set the OCD1 to OCD0 bits to "00$_2$" (oscillation stop detection function disabled) where the main clock is stopped or oscillated in the program, that is where the stop mode is selected or the CM05 bit is altered.
- When using the low-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the HR01 bit in the HR0 register to "0" (low-speed on-chip oscillator selected) and the OCD1 to OCD0 bits to "11$_2$" (oscillation stop detection function enabled). When using the high-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the HR01 bit to "1" (high-speed on-chip oscillator selected) and the OCD1 to OCD0 bits to "11$_2$" (oscillation stop detection function enabled).

Table 6.5 Interrupt Factor Determination of Oscillation Stop Detection, Watchdog Timer Interrupt or Voltage Detection Interrupt

Generated Interrupt Factor	Bit showing interrupt source
Oscillation stop detection ((a) or (b))	(a) The OCD3 bit in the OCD register = 1
	(b) The OCD1 to OCD0 bits in the OCD register = 112 and the OCD2 bit = 1
Watchdog timer	The D43 bit in the D4INT register = 1
Voltage detection	The D42 bit in the D4INT register = 1

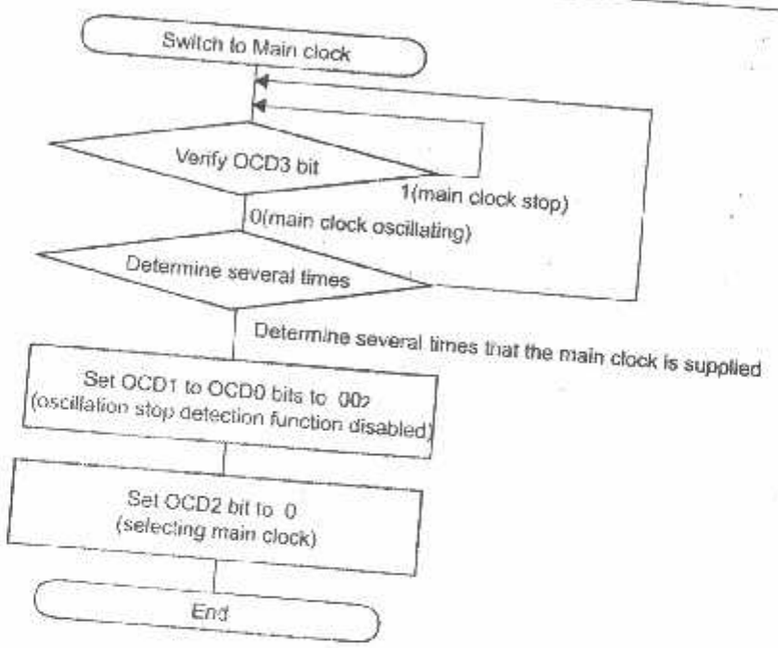


Figure 6.7 Switching Clock Source From Low-speed On-Chip Oscillator to Main Clock

Protection

In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily. Figure 7.1 shows the PRCR register. The following lists the registers protected by the PRCR register.

- Registers protected by PRC0 bit: CM0, CM1, and OCD, HR0, HR1 registers
- Registers protected by PRC1 bit: PM0 and PM1 registers
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: VCR2 and D4INT registers

Set the PRC2 bit to "1" (write enabled) and then write to any address, and the PRC2 bit will be set to "0" (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to "1". Make sure no interrupts will occur between the instruction in which the PRC2 bit is set to "1" and the next instruction. The PRC0,PRC1 and PRC3 bsits are not automatically set to "0" by writing to any address. They can only be set to "0" in a program.

Protect register

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol: PRCR | Address: 000A16 | After reset: 00XXX0002

Bit symbol	Bit name	Function	RW
PRC0	Protect bit 0	Enable write to CM0, CM1, OCD, HR0, HR1 registers 0 : Write protected 1 : Write enabled	RW
PRC1	Protect bit 1	Enable write to PM0, PM1 registers 0 : Write protected 1 : Write enabled	RW
PRC2	Protect bit 2	Enable write to PD0 register 0 : Write protected 1 : Write enabled[1]	RW
PRC3	Protect bit 3	Enable write to VCR2, D4INT registers 0 : Write protected 1 : Write enabled	RW
(b5-b4)	Reserved bit	When write, should set to "0"	RW
(b7-b6)	Reserved bit	When read, its content is "0".	RO

Notes:
1. The PRC2 bit is set to "0" by writing to any address after setting it to "1". Other bits are not set to "0" by writing to any address, and must therefore be set to "0" in a program.

Figure 7.1 PRCR Register

8. Processor Mode

8.1 Types of Processor Mode

The processor mode is single-chip mode. Table 8.1 shows the features of the processor mode. Figure 8.1 shows the PM0 and PM1 register.

Table 8.1 Features of Processor Mode

Processor mode	Access space	Pins which are assigned I/O ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

Processor mode register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	0	

Symbol: PM0 — Address: 000416 — After reset: 0016

Bit symbol	Bit name	Function	RW
(b2-b0)	Reserved bit	Set to "0"	RW
PM03	Software reset bit	Setting this bit to "1" resets the microcomputer. When read, its content is "0".	RW
(b7-b4)	Nothing is assigned. When write, set to "0". When read, its content is "0".		—

NOTES:
1. Set the PRC1 bit in the PRCR register to "1" (write enable) before writing to this register.

Processor mode register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X	X	X	X	0	

Symbol: PM1 — Address: 000516 — After reset: 0016

Bit symbol	Bit name	Function	RW
PM10	Data area access enable bit	0 : Disabled 1 : Enabled	RW
(b1)	Reserved bit	Set to "0"	RW
PM12	WDT interrupt/reset switch bit(2)	0 : Watchdog timer interrupt 1 : Watchdog timer reset2	RW
(b6-b3)	Nothing is assigned. When write, set to "0". When read, its content is 0.		—
(b7)	Reserved bit	Set to "0"	RW

Notes:
1. Set the PRC1 bit in the PRCR register to "1" (write enable) before writing to this register.
2. PM12 bit is set to "1" by writing a "1" in a program. (Writing a "0" has no effect.)

Figure 8.1 PM0 Register and PM1 Register

. Bus

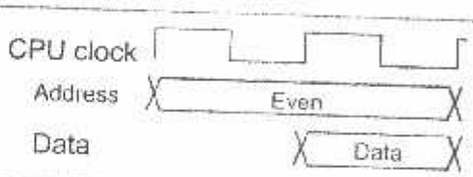
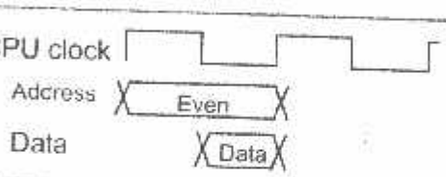
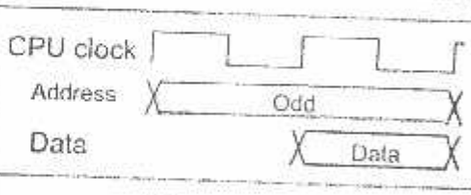
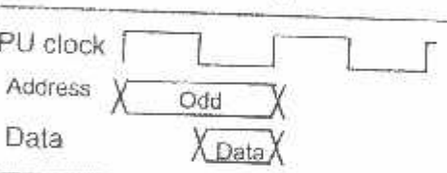
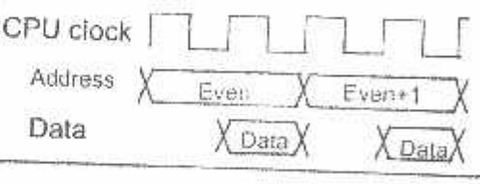
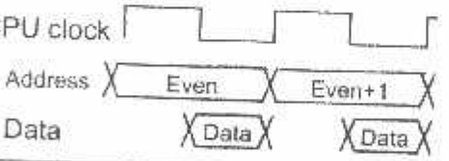
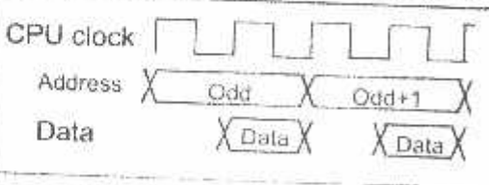
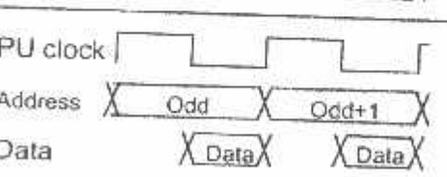
During access, the ROM/RAM and the SFR have different bus cycles. Table 9.1 shows bus cycles for access space.

The ROM/RAM and SFR are connected to the CPU through an 8-bit bus. When accessing in word (16 bits) units, these spaces are accessed twice in 8-bit units. Table 9.2 shows bus cycles in each access space.

Table 9.1 Bus Cycles for Access Space

Access space	Bus cycle
SFR	2 CPU clock cycles
ROM/RAM	1 CPU clock cycles

Table 9.2 Access Unit and Bus Operation

Space	SFR	ROM/RAM
Even address byte access		
Odd address byte access		
Even address word access		
Odd address word access		

1. Watchdog Timer

The watchdog timer is the function of detecting when the program is out of control. Therefore, we recommend using the watchdog timer to improve reliability of a system. Figure 11.1 shows the watchdog timer block diagram.The watchdog timer contains a 15-bit counter which counts down the clock derived by dividing the CPU clock using the prescaler. Whether to generate a watchdog timer interrupt request or apply a watchdog timer reset as an operation to be performed when the watchdog timer underflows after reaching the terminal count can be selected using the PM12 bit in the PM1 register. The PM12 bit can only be set to "1" (reset). Once this bit is set to "1", it cannot be set to "0" (watchdog timer interrupt) in a program. Refer to Section 5.3, "Watchdog Timer Reset" for details.
The divide-by-N value for the prescaler can be chosen to be 16 or 128 with the WDC7 bit in the WDC register. The period of watchdog timer can be calculated as given below. The period of watchdog timer is, however, subject to an error due to the prescaler.

$$\text{Watchdog timer period} = \frac{\text{Prescaler dividing (16 or 128) X Watchdog timer count (32768)}}{\text{CPU clock}}$$

For example, when CPU clock = 16 MHz and the divide-by-N value for the prescaler= 16, the watchdog timer period is approx. 32.8 ms.

Figure 11.2 shows the OFS, the WDC, the WDTR and the WDTS registers. The watchdog timer operation after reset can be selected using the WDTON bit in the option function select register ($0FFFF_{16}$ address).

- When the WDTON bit is "0" (the watchdog timer is started automatically after reset), the watchdog timer and the prescaler both start counting automatically after reset.
- When the WDTON bit is "1" (the watchdog timer is inactive after reset), the watchdog timer and the prescaler both are inactive after reset, so that the watchdog timer is activated to start counting by writing to the WDTS register.

The WDTON bit can not be changed in a program. When setting the WDTON bit, write "0" into bit 0 of $0FFFF_{16}$ address using a flash writer. The watchdog timer is initialized by writing to the WDTR register and the counting continues.

In stop mode and wait mode, the watchdog timer and the prescaler are stopped. Counting is resumed from the held value when the modes or state are released.

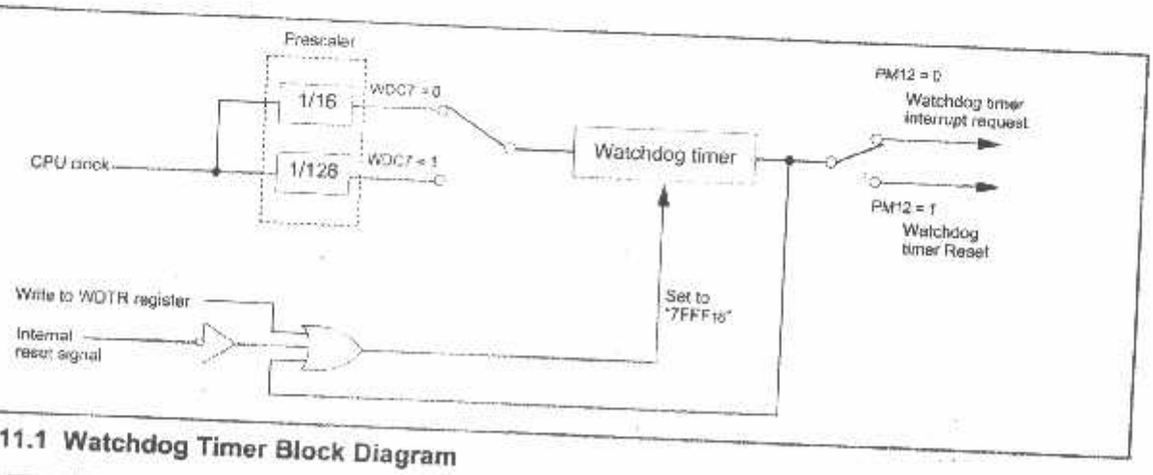


Figure 11.1 Watchdog Timer Block Diagram

2. Timers

The microcomputer has three 8-bit timers and one 16-bit timer. The three 8-bit timers are Timer X, Timer Y, and Timer Z and each one has an 8-bit prescaler. The 16-bit timer is Timer C and has input capture and output compare. All these timers function independently. The count source for each timer is the operating clock that regulates the timing of timer operations such as counting and reloading.
Table 12.1 lists functional comparison.

Table 12.1 Functional Comparison

Item		Timer X	Timer Y	Timer Z	Timer C
Configuration		8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	16-bit free-run timer
Count		Down	Down	Down	Up
Count source		•f_1 •f_2 •f_8 •f_{32}	•f_1 •f_8 •f_{RING} •Input from $CNTR_1$ pin	•f_1 •f_2 •f_8 •Timer Y underflow	•f_1 •f_8 •f_{32} •$f_{RING-fast}$
Function	Timer mode	provided	provided	provided	not provided
	Pulse output mode	provided	not provided	not provided	not provided
	Event counter mode	provided	provided[1]	not provided	not provided
	Pulse width measurement mode	provided	not provided	not provided	not provided
	Pulse period measurement mode	provided	not provided	not provided	not provided
	Programmable waveform generation mode	not provided	provided	provided	not provided
	Programmable one-shot generation mode	not provided	not provided	provided	not provided
	Programmable wait one-shot generation mode	not provided	not provided	provided	not provided
	Input capture mode	not provided	not provided	not provided	provided
	Output compare mode	not provided	not provided	not provided	provided
Input pin		$CNTR_0$	$CNTR_1$	INT_0	TC_{IN}
Output pin		$CNTR_0$ $CNTR_1$	$CNTR_1$	TZ_{OUT}	$CMP0_0$ to $CMP0_2$ $CMP1_0$ to $CMP1_2$
Related interrupt		Timer X int INT1 int	Timer Y int INT2 int	Timer Z int INT0 int	Timer C int INT3 int compare 0 int compare 1 int
Timer stop		provided	provided	provided	provided

Note: Select the input from the $CNTR_1$ pin as a count source of timer mode.

3. Serial Interface

Serial interface is configured with two channels: UART0 to UART1. UART0 and UART1 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 13.1 shows a block diagram of UARTi (i=0, 1). Figure 13.2 shows a block diagram of the UARTi transmit/receive.

UART0 has two modes: clock synchronous serial I/O mode, and clock asynchronous serial I/O mode (UART mode).

UART1 has only one mode, clock asynchronous serial I/O mode (UART mode).

Figures 13.3 to 13.5 show the UARTi-related registers.

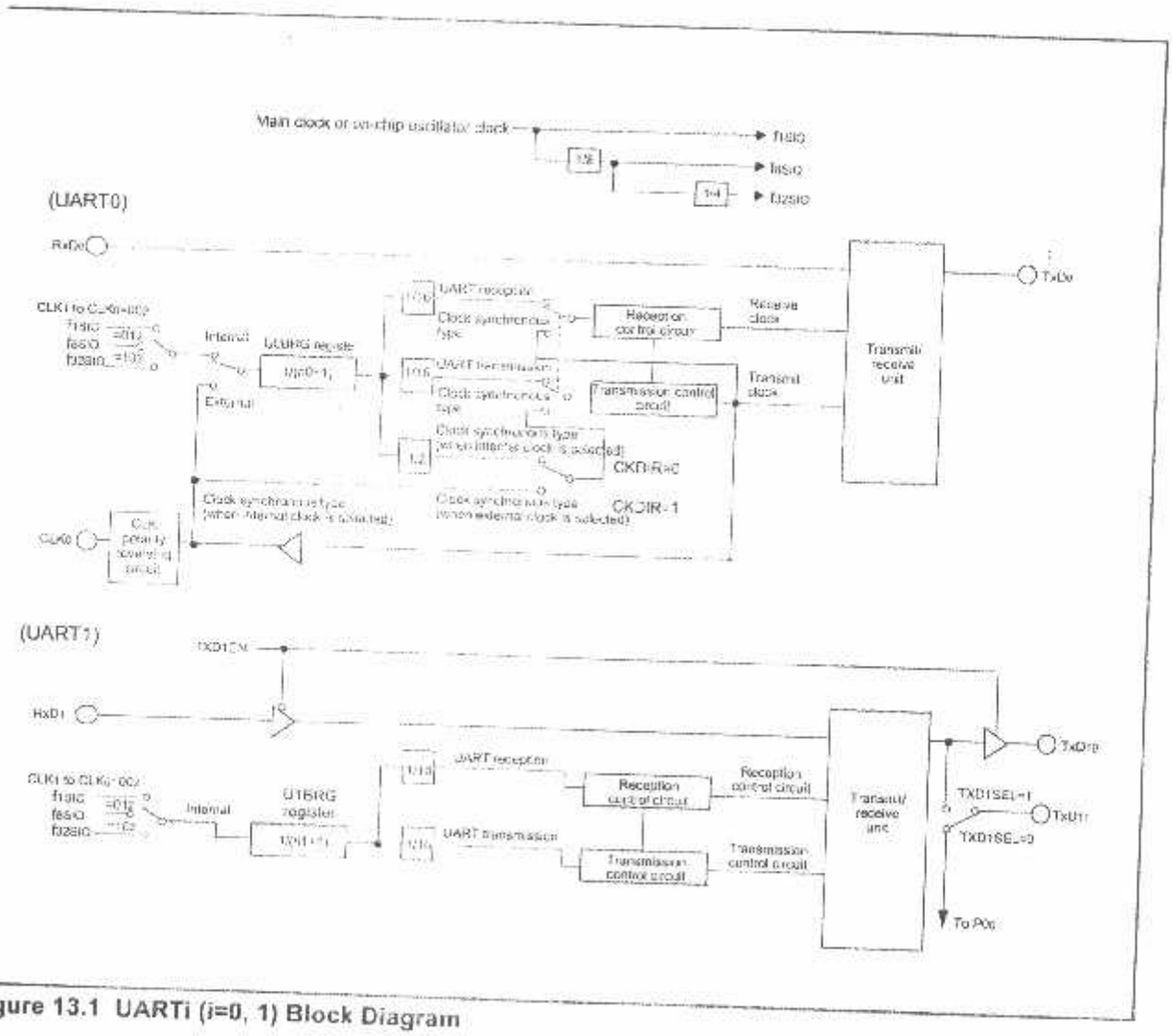


Figure 13.1 UARTi (i=0, 1) Block Diagram

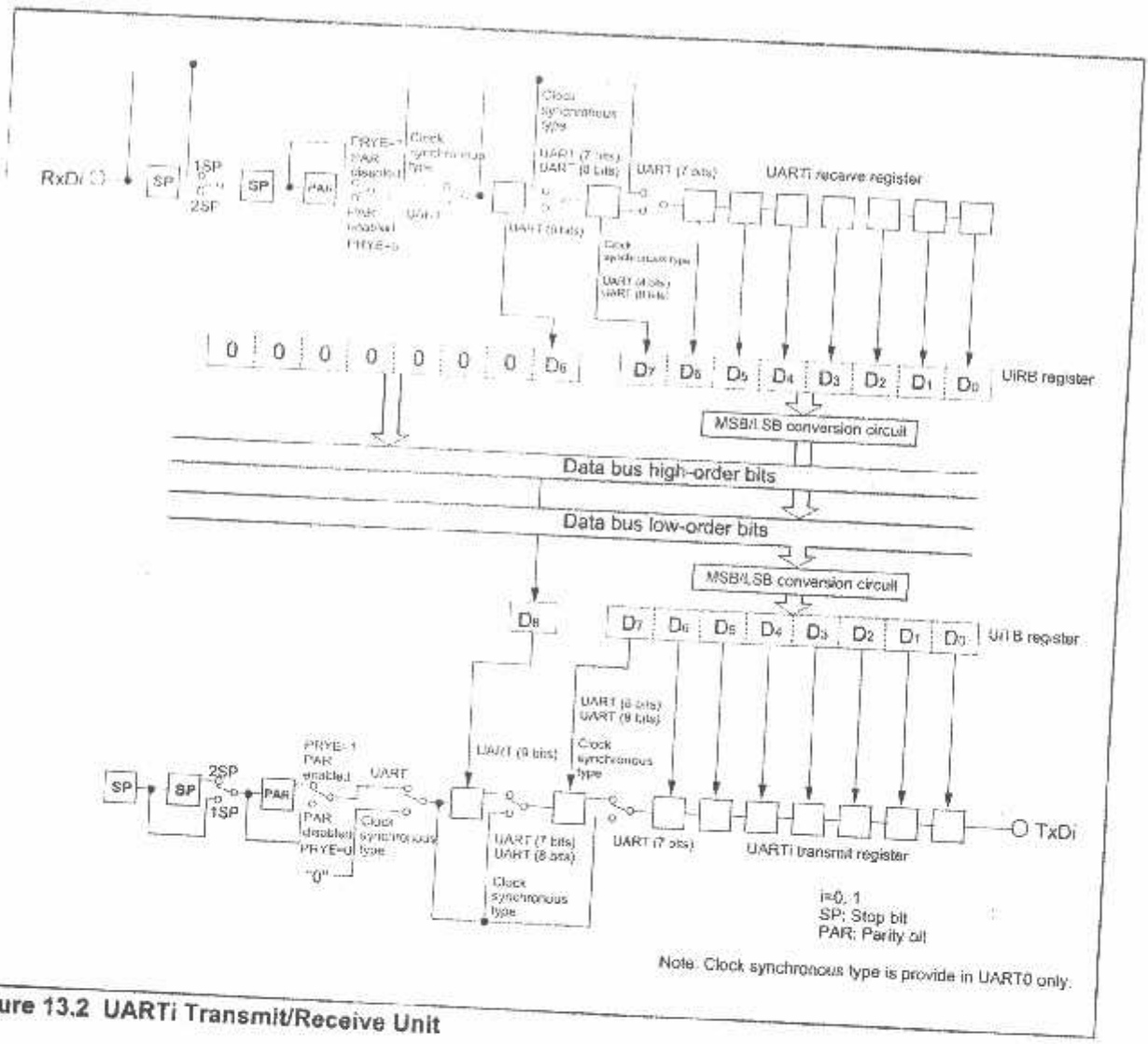
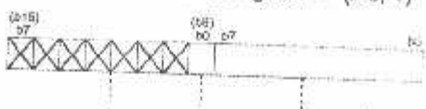


Figure 13.2 UARTi Transmit/Receive Unit

UARTi transmit buffer register[1, 2] (i=0, 1)

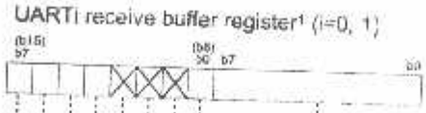


Symbol	Address	After reset
U0TB	00A3₁₆-00A2₁₆	Indeterminate
U1TB	00AB₁₆-00AA₁₆	Indeterminate

Function	RW
Transmit data	WO
Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

Notes
1. When transfer data length is 9-bit long, write high-byte first then low-byte.
2. Use MOV instruction to write to this register.

UARTi receive buffer register[1] (i=0, 1)



Symbol	Address	After reset
U0RB	00A7₁₆-00A6₁₆	Indeterminate
U1RB	00AF₁₆-00AE₁₆	Indeterminate

Bit symbol	Bit name	Function	RW
(b7-b0)	—	Receive data (D7 to D0)	RO
(b8)	—	Receive data (D8)	RO
(b11-b9)	—	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—
OER	Overrun error flag[2]	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag[2]	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag[2]	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag[2]	0 : No error 1 : Error found	RO

Notes:
1. Read the UiRB register in 16-bit unit.
2. All of the SUM, PER, FER and OER bits are set to "0" (no error) when the SMD2 to SMD0 bits in the U0MR register are set to "000₂" (serial I/O disabled) or the RE bit in the U0C1 register is set to "0" (reception disabled). The SUM bit is set to "0" (no error) when all of the PER, FER and OER bits are set to "0" (no error).
The PER and FER bits are set to "0" even when the higher byte of the U0RB register is read.

UARTi bit rate register[1, 2] (i=0, 1)

Symbol	Address	After reset
U0BRG	00A1₁₆	Indeterminate
U1BRG	00A9₁₆	Indeterminate

Function	Setting range	RW
Assuming that set value = n, U0BRG divides the count source by n + 1	00₁₆ to FF₁₆	WO

Notes:
1. Write to this register while serial interface is neither transmitting nor receiving.
2. Use MOV instruction to write to this register.

Figure 13.3 U0TB and U1TB Registers, U0RB and U1RB Registers, and U0BRG and U1BRG Registers

UARTi transmit/receive mode register (i=0, 1)

Symbol	Address	After reset
U0MR	00A0₁₆	00₁₆
U1MR	00A8₁₆	00₁₆

Bit symbol	Bit name	Function	RW
SMD0	Serial interface mode select bit[2]	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Must not be set except above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit[3]	0 : Internal clock 1 : External clock[1]	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
(b7)	Reserved bit	Must set to "0"	RW

Notes:
1. Must set the PD1_6 bit in the PD1 register to "0" (input).
2. For the U1MR register, the SMD2 to SMD0 bits must not be set except the followings: "000₂", "100₂", "101₂", or "110₂".
3. Must set the CKDIR bit to "0" (internal clock) in UART1.

UARTi transmit/receive control register 0 (i=0, 1)

Symbol	Address	After reset
U0C0	00A4₁₆	08₁₆
U1C0	00AC₁₆	08₁₆

Bit symbol	Bit name	Function	RW
CLK0	BRG count source select bit	b1 b0 0 0 : fSIO is selected 0 1 : fSIO is selected 1 0 : fSIO is selected 1 1 : Avoid this setting	RW
CLK1			RW
(b2)	Reserved bit	Set to "0"	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	RO
(b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
NCH	Data output select bit	0 : TxDi pin is a pin of CMOS output 1 : TxDi pin is a pin of N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

Figure 13.4 U0MR and U1MR Registers and U0C0 and U1C0 Registers

UARTi transmit/receive control register 1 (i=0, 1)

Symbol	Address	After reset
U0C1	00A5₁₆	02₁₆
U1C1	00AD₁₆	02₁₆

Bit symbol	Bit name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit[1]	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag[2]	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b7-b4)	Nothing is assigned. When write, set "0". When read, its content is "0".		—

Notes:
1. As for the UART1, set the TXD1EN bit in the UCON register before setting this bit to reception enabled.
2. The RI bit is set to "0" when the higher byte of the UiRB register is read.

UART transmit/receive control register 2

Symbol	Address	After reset
UCON	00B0₁₆	00₁₆

Bit symbol	Bit name	Function	RW
U0IRS	UART0 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U1IRS	UART1 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enable	RW
— (b4-b3)	Reserved bit	Must set to "0"	RW
TXD1SEL	Port TxD1 switching bit	0 : I/O port P0₀ 1 : TxD1	RW
TXD1EN	TxD1/RxD1 select bit	0 : RxD1 1 : TxD1	RW
— (b7)	Nothing is assigned. When write, set "0". When read, its content is "0".		—

Notes
1. For P3₇, select "0" (RxD1) for data receive, and "1" (TxD1) for data transfer.
Set the PD3_7 bit in the PD3 register to "0" (input mode) when receiving.

Figure 13.5 U0C1 and U1C1 Registers and UCON Register

3.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. This mode can be selected with UART0. Table 13.1 lists the specifications of the clock synchronous serial I/O mode. Table 13.2 lists the registers used in clock synchronous serial I/O mode and the register values set.

Table 13.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clock	• CKDIR bit in U0MR register is set to "0" (internal clock): fi/(2(n+1)) fi=f1SIO, fSSIO, f32SIO n=setting value in UiBRG register: 00$_{16}$ to FF$_{16}$ • CKDIR bit is set to "1" (external clock): input from CLK0 pin
Transmission start condition	• Before transmission can start, the following requirements must be met[1] – TE bit in U0C1 register is set to "1" (transmission enabled) – TI bit in U0C1 register is set to "0" (data present in U0TB register)
Reception start condition	• Before reception can start, the following requirements must be met[1] – RE bit in U0C1 register is set to "1" (reception enabled) – TE bit in U0C1 register is set to "1" (transmission enabled) – TI bit in U0C1 register is set to "0" (data present in the U0TB register)
Interrupt request generation timing	• For transmission, one of the following conditions can be selected – U0IRS bit is set to "0" (transmit buffer empty): when transferring data from U0TB register to UART0 transmit register (at start of transmission) – U0IRS bit is set to "1" (transfer completed): when serial interface finished sending data from UARTi transmit register • For reception When transferring data from the UART0 receive register to the U0RB register (at completion of reception)
Error detection	• Overrun error[2] This error occurs if serial interface started receiving the next data before reading the U0RB register and received the 7th bit of the next data
Select function	• CLK polarity selection Transfer data I/O can be chosen to occur synchronously with the rising or the falling edge of the transfer clock • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the U0RB register

Notes:

1. When an external clock is selected, the conditions must be met while if the U0C0 register0 CKPOL bit = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the U0C0 register is set to "1" (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.
2. If an overrun error occurs, the value of U0RB register will be indeterminate. The IR bit of S0RIC register does not change.

Table 13. 2 Registers to Be Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U0TB	0 to 7	Set transmission data
U0RB	0 to 7	Reception data can be read
	OER	Overrun error flag
U0BRG	0 to 7	Set a bit rate
U0MR	SMD2 to SMD0	Set to "001"
	CKDIR	Select the internal clock or external clock
U0C0	CLK1 to CLK0	Select the count source for the U0BRG register
	TXEPT	Transmit register empty flag
	NCH	Select TxD0 pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
U0C1	TE	Set this bit to "1" to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set this bit to "1" to enable reception
	RI	Reception complete flag
UCON	U0IRS	Select the source of UART0 transmit interrupt
	U0RRM	Set this bit to "1" to use continuous receive mode
	TXDISEL	Set to "0"
	TXDIEN	Set to "0"

Notes:

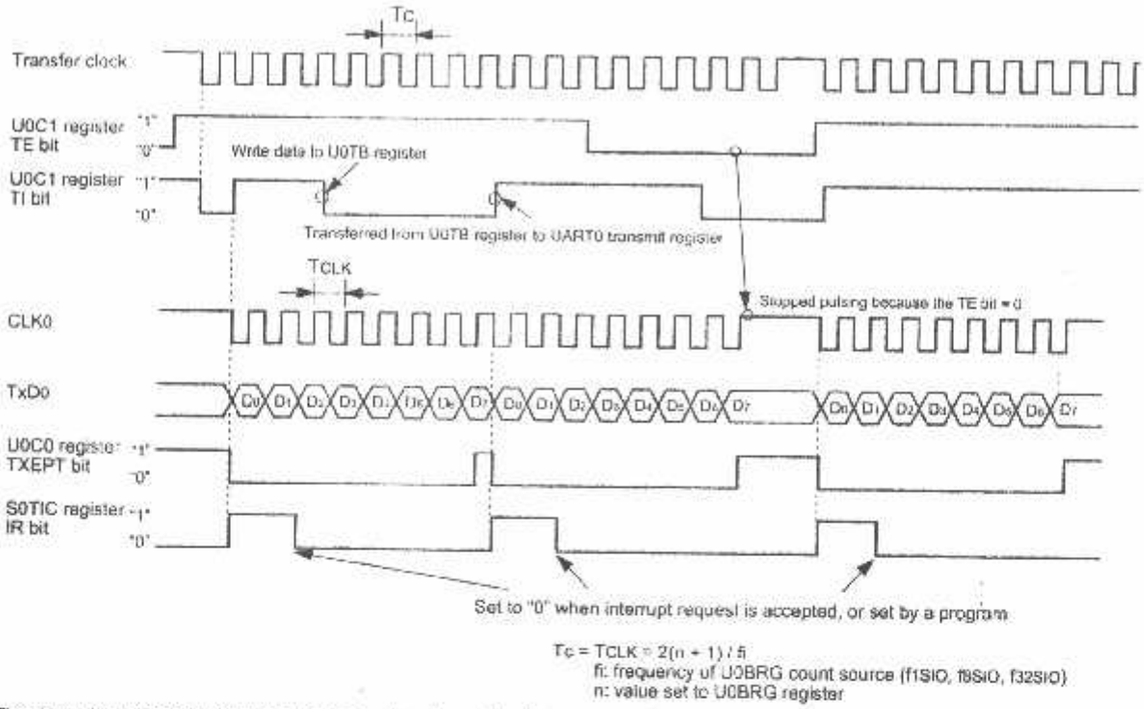
1. Not all register bits are described above. Set those bits to "0" when writing to the registers in clock synchronous serial I/O mode.

Table 13.3 lists the functions of the I/O pins during clock synchronous serial I/O mode. Note that for a period from when the UART0 operation mode is selected to when transfer starts, the TxD0 pin outputs an "H". (If the NCH bit is set to "1"(N-channel open-drain output), this pin is in high-impedance state.)

Table 13.3 Pin Functions

Pin name	Function	Method of selection
TxD0 (P14)	Serial data output	(Outputs dummy data when performing reception only)
RxD0 (P15)	Serial data input	PD1 register PD1_5 bit=0 (P15 can be used as an input port when performing transmission only)
CLK0 (P16)	Transfer clock output	U0MR register CKDIR bit=0
	Transfer clock input	U0MR register CKDIR bit=1 PD1 register PD1_6 bit=0

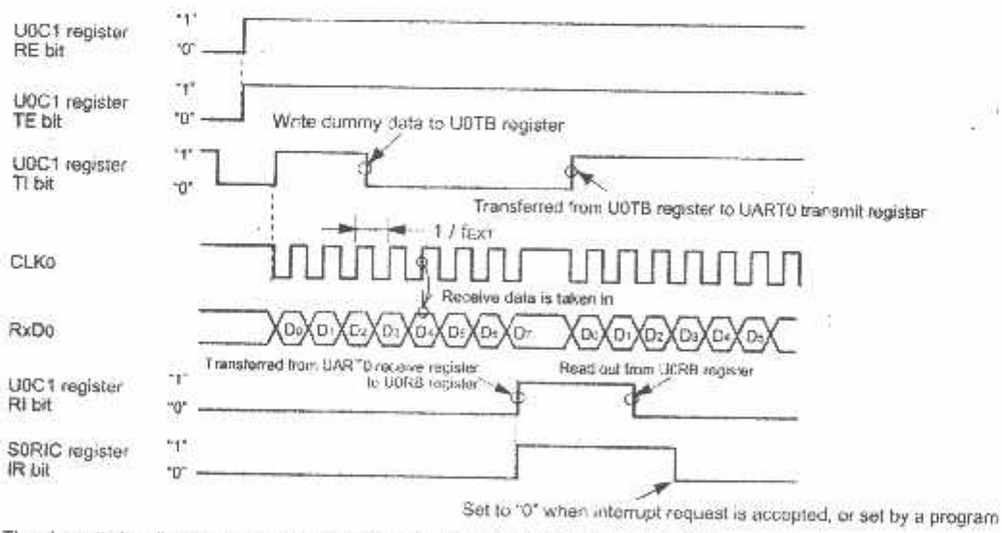
• Example of transmit timing (when internal clock is selected)



Tc = TCLK = 2(n + 1) / fi
fi: frequency of U0BRG count source (f1SIO, f8SIO, f32SIO)
n: value set to U0BRG register

The above timing diagram applies to the case where the register bits are set as follows:
- U0MR register CKDIR bit = 0 (internal clock)
- U0C0 register CKPOL bit = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)
- U0IRS bit = 0 (an interrupt request occurs when the transmit buffer becomes empty)

• Example of receive timing (when external clock is selected)



The above timing diagram applies to the case where the register bits are set as follows:
- U0MR register CKDIR bit = 1 (external clock)
- U0C0 register CKPOL bit = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)

Make sure the following conditions are met when input to the CLK0 pin before receiving data is high:
- U0C1 register TE bit = 1 (transmit enabled)
- U0C1 register RE bit = 1 (receive enabled)
- Write dummy data to the U0TB register

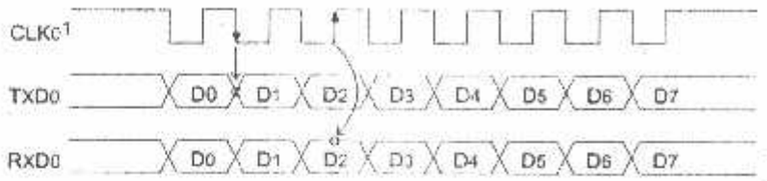
fEXT: frequency of external clock

Figure 13.6 Transmit and Receive Operation

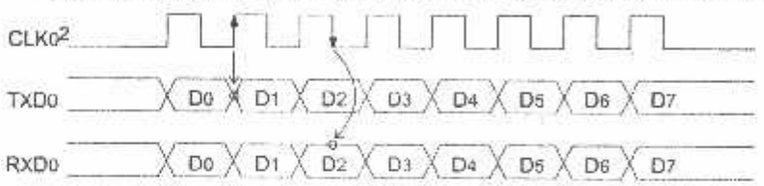
13.1.1 Polarity Select Function

Figure 13.7 shows the polarity of the transfer clock. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

(1) When the U0C0 register CKPOL bit = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock)



(2) When the U0C0 register CKPOL bit = 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock)



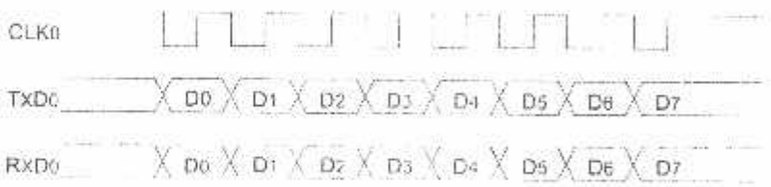
Notes:
1. When not transferring, the CLK0 pin outputs a high signal.
2. When not transferring, the CLK0 pin outputs a low signal.

Figure 13.7 Transfer Clock Polarity

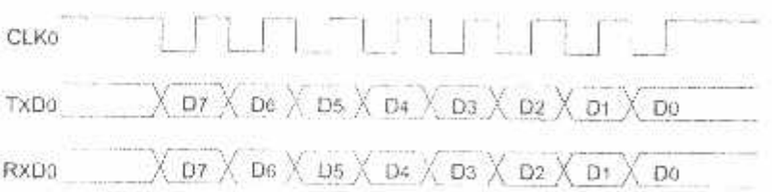
13.1.2 LSB First/MSB First Select Function

Figure 13.8 shows the transfer format. Use the UFORM bit in the U0C0 register to select the transfer format.

(1) When U0C0 register UFORM bit = 0 (LSB first)



(2) When U0C0 register UFORM bit = 1 (MSB first)



Note: This applies to the case where the CKPOL bit in the U0C0 register is set to "0" (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock).

Figure 13.8 Transfer Format

13.1.3 Continuous Receive Mode

Continuous receive mode is held by setting setting the U0RRM bit in the UCON register to "1" (enables continuous receive mode). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to "0"(data in the U0TB register). When the U0RRM bit is set to "1", do not write dummy data to tge U0TB register in a program.

13.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmitting and receiving data after setting the desired bit rate and transfer data format. Tables 13.4 lists the specifications of the UART mode. Table 13.5 lists the registers and settings for UART mode.

Table 13.4 UART Mode Specifications

Item	Specification
Transfer data format	• Character bit (transfer data): selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: selectable from odd, even, or none • Stop bit: selectable from 1 or 2 bits
Transfer clock	• UiMR(i=0, 1) register CKDIR bit = 0 (internal clock) : fj/(16(n+1)) fj=f1SIO, f8SIO, f32SIO n=setting value in UiBRG register: 0016 to FF16 • CKDIR bit = "1" (external clock) : fEXT/(16(n+1)) fEXT: input from CLKi pin n=setting value in UiBRG register: 0016 to FF16
Transmission start condition	• Before transmission can start, the following requirements must be met – TE bit in UiC1 register= 1 (transmission enabled) – TI bit in UiC1 register = 0 (data present in UiTB register)
Reception start condition	• Before reception can start, the following requirements must be met – RE bit in UiC1 register= 1 (reception enabled) – Start bit detection
Interrupt request generation timing	• For transmission, one of the following conditions can be selected – UiIRS bit = 0 (transmit buffer empty): when transferring data from UiTB register to UARTi transmit register (at start of transmission) – UiIRS bit =1 (transfer completed): when serial interface finished sending data from UARTi transmit register • For reception When transferring data from UARTi receive register to UiRB register (at completion of reception)
Error detection	• Overrun error[1] This error occurs if serial interface started receiving the next data before reading UiRB register and received the bit one before the last stop bit of the next data • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when if parity is enabled, the number of 1's in parity and character bits does not match the number of 1's set • Error sum flag This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered
Select function	• TxD10, RxD1 selection (UART) P37 pin can be used as RxD1 pin or TxD10 pin in UART1. Select by a program. • TxD11 pin selection (UART1) P00 pin can be used as TxD11 pin in UART1 or port P00. Select by a program.

Notes:

1. If an overrun error occurs, the value of U0RB register will be indeterminate. The IR bit in the S0RIC register does not change.

Table 13.5 Registers to Be Used and Settings in UART Mode

Register	Bit	Function
UiTB	0 to 8	Set transmission data[1]
UiRB	0 to 8	Reception data can be read[1]
	OER,FER,PER,SUM	Error flag
UiBRG	---	Set a bit rate
UiMR	SMD2 to SMD0	Set these bits to '100₂' when transfer data is 7 bits long Set these bits to '101₂' when transfer data is 8 bits long Set these bits to '110₂' when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock[2]
	STPS	Select the stop bit
	PRY, PRYE	Select whether parity is included and whether odd or even
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TxDi pin output mode
	CKPOL	Set to "0"
	UFORM	LSB first or MSB first can be selected when transfer data is 8 bits long. Set this bit to "0" when transfer data is 7 or 9 bits long.
UiC1	TE	Set this bit to "1" to enable transmission
	TI	Transmit buffer empty flag
	RE	Set this bit to "1" to enable reception
	RI	Reception complete flag
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt
	U0RRM	Set to "0"
	TXD1SEL	Select output pin for UART1 transfer data
	TXD1EN	Select TxD1 or RxD1 to be used

Notes:

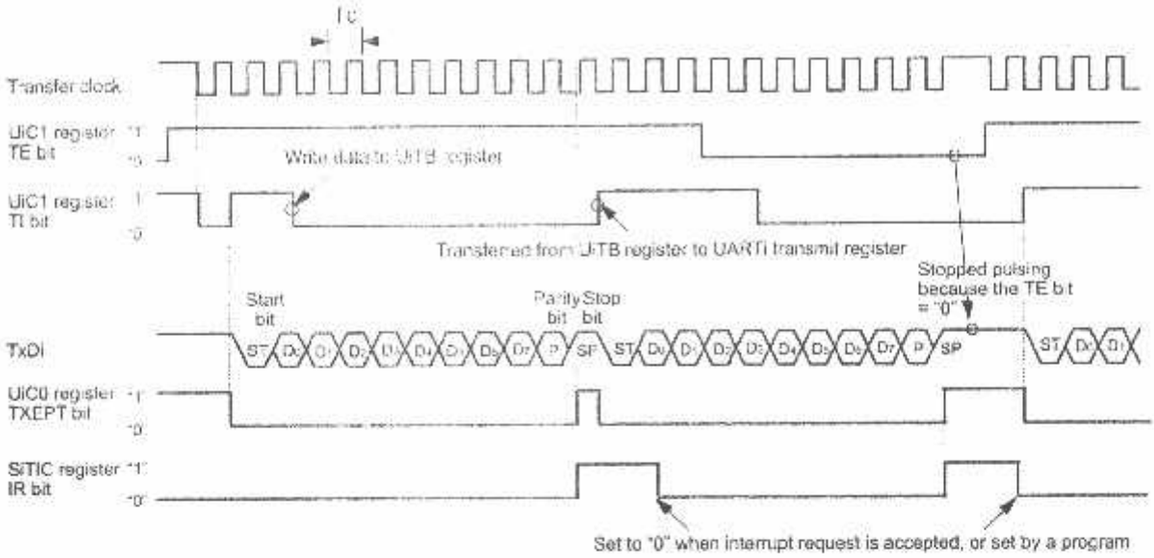
1. The bits used for transmit/receive data are as follows: Bit 0 to bit 6 when transfer data is 7 bits long, bit 0 to bit 7 when transfer data is 8 bits long; bit 0 to bit 8 when transfer data is 9 bits long.
2. An external clock can be selected in UART0 only.

Table 13.6 lists the functions of the I/O pins during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an "H". (If the NCH bit is set to "1"(N-channel open-drain output), this pin is in high-impedance state.)

Table 13.6 I/O Pin Functions

Pin name	Function	Method of selection
TxD0 (P14)	Serial data output	(Cannot be used as a port when performing reception only)
RxD0 (P15)	Serial data input	PD1 register PD1_5 bit=0 (Can be used as an input port when performing transmission only)
CLK0 (P16)	Programmable I/O port	U0MR register CKDIR bit=0
	Transfer clock input	U0MR register CKDIR bit=1 PD1 register PD1_6 bit=0
TxD1/RxD1 (P37)	Serial data output	TXD1EN=1
	Serial data input	TXD1EN=0, PD3 register PD3_7 bit=0
TxD1 (P00)	Serial data output	Serial data output, TXD1SEL=1

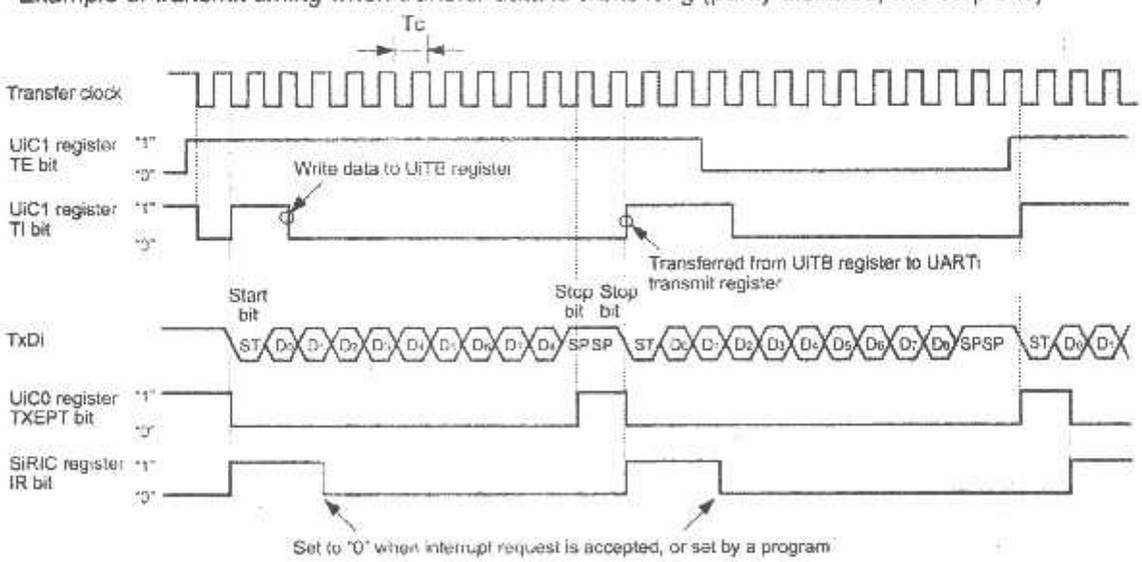
• Example of transmit timing when transfer data is 8 bits long (parity enabled, one stop bit)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 1 (parity enabled)
- UiMR register STPS bit = 0 (1 stop bit)
- UiIRS bit = 1 (an interrupt request occurs when transmit completed)

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i: 0, 1

• Example of transmit timing when transfer data is 9 bits long (parity disabled, two stop bits)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 0 (parity disabled)
- UiMR register STPS bit = 1 (2 stop bits)
- UiIRS bit = 0 (an interrupt request occurs when transmit buffer becomes empty)

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i: 0, 1

Figure 13.9 Transmit Operation

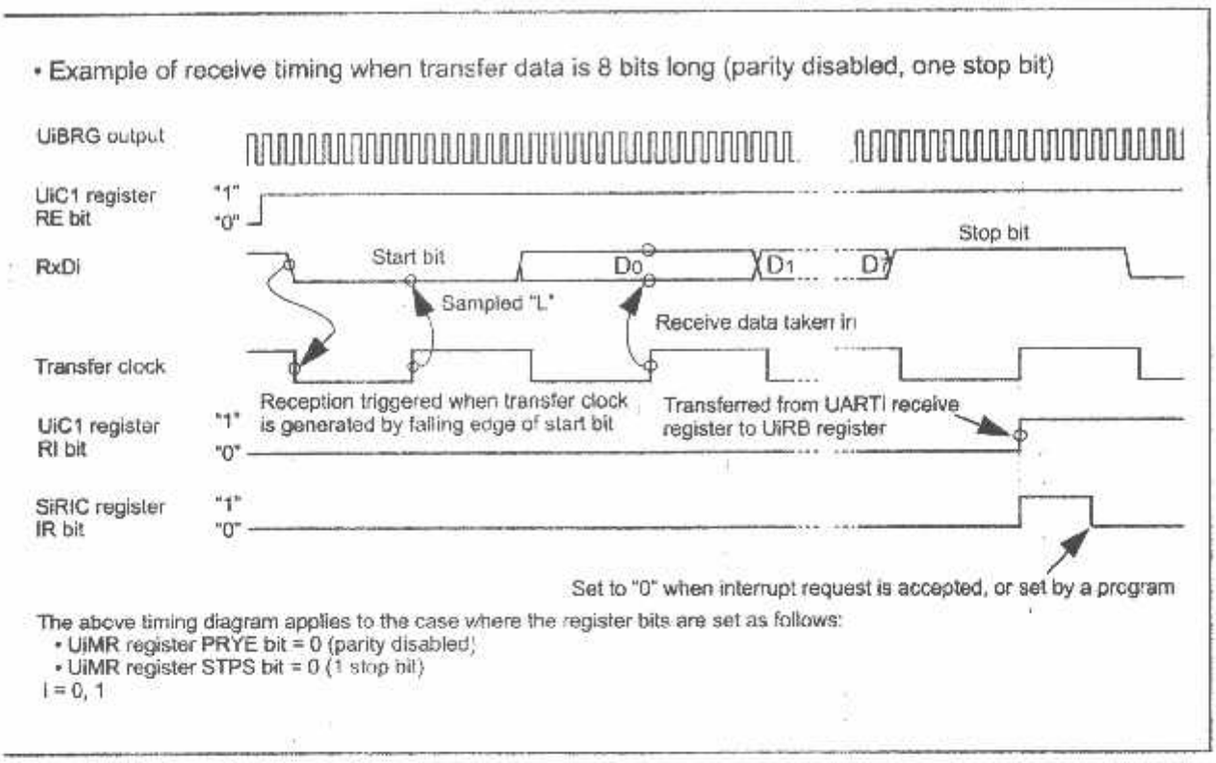


Figure 13.10 Receive Operation

13.2.1 TxD10/RxD1 Select Function (UART1)

P37 can be used as TxD10 output pin or RxD1 input pin by selecting with the TXD1EN bit in the UCON register. P37 is used as TxD10 output pin if the TXD1EN bit is set to "1" (TxD10) and used as RxD1 input pin if set to "0" (RxD1).

13.2.2 TxD11 Select Function (UART1)

P00 can be used as TxD11 output pin or a port by selecting with the TXD1SEL bit in the UCON register. P00 is used as TxD11 output pin if the TXD1SEL bit is set to "1" (TxD11) and used as an I/O port if set to "0" (P00).

13.2.3 Bit Rate

Divided-by-16 of frequency by the UiBRG (i=0 to 1) register in UART mode is a bit rate.

<UART Mode>

• When selecting internal clock

$$\text{Setting value to the UiBRG register} = \frac{\text{fj}}{\text{Bit Rate} \times 16} - 1$$

fj : Count source frequency of the UiBRG register (f1SIO, f8SIO and f32SIO)

• When selecting external clock

$$\text{Setting value to the UiBRG register} = \frac{\text{fEXT}}{\text{Bit Rate} \times 16} - 1$$

fEXT : Count source frequency of the UiBRG register (external clock)

Figure 13.11 Calculation Formula of UiBRG (i=0 to 1) Register Setting Value

Table 13.7 Bit Rate Setting Example in UART Mode

Bit Rate	BRG	System Clock = 20MHz			System Clock = 8MHz		
(bps)	Count Source	BRG Setting Value	Actual Time(bps)	Error(%)	BRG Setting Value	Actual Time(bps)	Error(%)
1200	f8	129 (81_{16})	1201.92	0.16	51 (33_{16})	1201.92	0.16
2400	f8	64 (40_{16})	2403.85	0.16	25 (19_{16})	2403.85	0.16
4800	f8	32 (20_{16})	4734.85	−1.36	12 ($0C_{16}$)	4807.69	0.16
9600	f1	129 (81_{16})	9615.38	0.16	51 (33_{16})	9615.38	0.16
14400	f1	86 (56_{16})	14367.82	−0.22	34 (22_{16})	14285.71	−0.79
19200	f1	64 (40_{16})	19230.77	0.16	25 (19_{16})	19230.77	0.16
28800	f1	42 ($2A_{16}$)	29069.77	0.94	16 (10_{16})	29411.76	2.12
31250	f1	39 (27_{16})	31250.00	0.00	15 ($0F_{16}$)	31250.00	0.00
38400	f1	32 (20_{16})	37878.79	−1.36	12 ($0C_{16}$)	38461.54	0.16
51200	f1	23 (17_{16})	52083.33	1.73	9 (09_{16})	50000.00	−2.34

4. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog inputs share the pins with P00 to P07 and P10 to P13. Therefore, when using these pins, make sure the corresponding port direction bits are set to "0" (input mode).

When not using the A/D converter, set the VCUT bit to "0" (Vref unconnected), so that no current will flow from the VREF pin into the resistor ladder, helping to reduce the power consumption of the chip.

The result of A/D conversion is stored in the AD register.

Table 14.1 shows the performance of the A/D converter. Figure 14.1 shows a block diagram of the A/D converter, and Figures 14.2 and 14.3 show the A/D converter-related registers.

Table 14.1 Performance of A/D converter

Item	Performance
Method of A/D conversion	Successive approximation (capacitive coupling amplifier)
Analog input voltage[1]	0V to Vref
Operating clock ϕ_{AD}[2]	AVcc = 5V fAD, divide-by-2 of fAD, divide-by-4 of fAD AVcc = 3V divide-by-2 of fAD, divide-by-4 of fAD
Resolution	8-bit or 10-bit (selectable)
Integral nonlinearity error	AVcc = Vref = 5V • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVcc = Vref = 3.3 V • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating modes	One-shot mode and repeat mode[3]
Analog input pins	12 pins (AN0 to AN11)
A/D conversion start condition	ADST bit in ADCON0 register is set to "1" (A/D conversion starts)
Conversion speed per pin	• Without sample and hold function 8-bit resolution: 49 ϕ_{AD} cycles, 10-bit resolution: 59 ϕ_{AD} cycles • With sample and hold function 8-bit resolution: 28 ϕ_{AD} cycles, 10-bit resolution: 33 ϕ_{AD} cycles

Notes:

1. Does not depend on use of sample and hold function.
2. The frequency of ϕ_{AD} must be 10 MHz or less.
   When AVcc is less than 4.2V, ϕ_{AD} must be fAD/2 or less by dividing fAD.
   Without sample and hold function, the ϕ_{AD} frequency should be 250 kHz or more.
   With the sample and hold function, the ϕ_{AD} frequency should be 1 MHz or more.
3. In repeat mode, only 8-bit mode can be used.

ID-10 SERIES
LOW COST PROXIMITY READER

BOOTTOM VIEW

Power Requirement : 5V@13mA nominal
Card Format : EM4001 or compatible
Frequency : 125KHz
Encoding : Manchester 62bit,modulus 64

I/O Output Current : 20mA sink/source
Drive Current : 300mA
Antenna Volt : 100 Volt PKPK

OUTPUT FORMAT-ASCII

02 10 ASCII Data Characters Checksum CR LF 03

The checksum is the result of the 'exclusive or' of the 5 Binary Data bytes (the 10 ASCII data characters)

DATA STRUCTURE WIEGAND 26 BIT

P=Parity Start Bit and Stop Bit

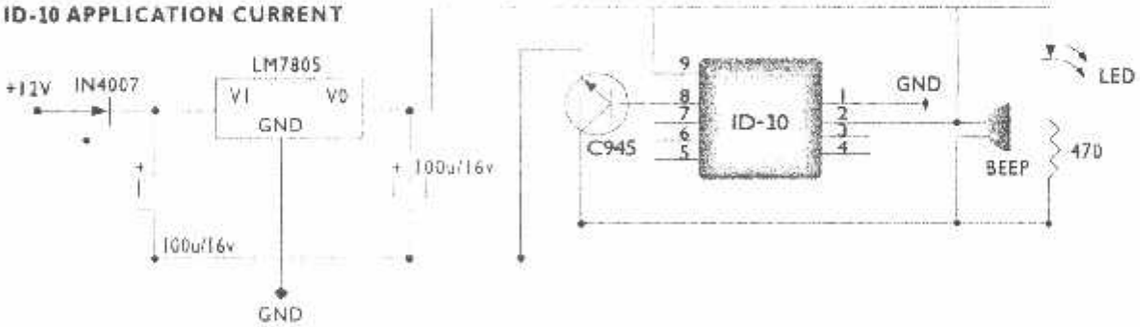
ASCII (RS232)

Pin1	Ground 0V	Zero volts and Tuning Capacitor Ground
Pin2	Reset Bar	Strap to +5V
Pin3	Antenna	NC
Pin4	Antenna	NC
Pin5	Strap to Ground	
Pin6	CMOS	Serial ASCII
Pin7	TTL Data	Serial ASCII inverted
Pin8	BEEP/LED	2.7KHz Logic
Pin9	+4.6 through +5.5V	Supply DC volts

WIEGAND 26

Pin1	Ground 0V	Zero volts and Tuning Capacitor Ground
Pin2	Reset Bar	Strap to +5V
Pin3	Antenna	NC
Pin4	Antenna	NC
Pin5	Strap to Pin +5V	
Pin6	One Output	
Pin7	Zero Output	
Pin8	BEEP/LED	2.7KHz Logic
Pin9	+4.6 through+5.5V	Supply DC volts

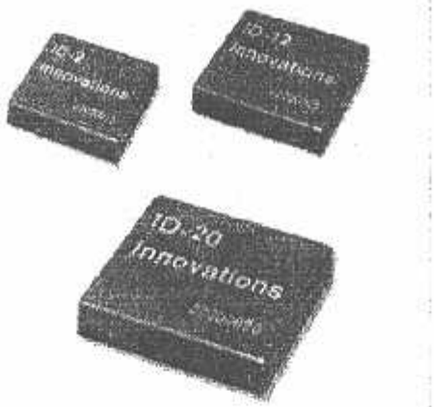
ID-10 APPLICATION CURRENT



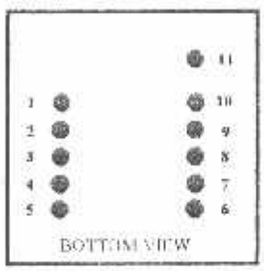
D SERIES DATASHEET Feb 10 , 2004

ID-2 / ID-12 / ID-20

he ID2, ID12 and ID20 are similar to the ID0, ID10 and ID15 IK(ii) series devices, but they have extra pins which allow Magnetic mulation output to be included in the functionality. The ID-12 and)-20 come with internal antennas, and have read ranges of 12+ cm id 16+ cm, respectively. With an external antenna, the ID-2 can eliver read ranges of up to 25 cm. All three readers support ASCII, 'iegand26 and Magnetic ABA Track2 data formats.



ID2 / ID12 / ID20 PIN-OUT



1. GND
2. RES (Reset Bar)
3. ANT (Antenna)
4. ANT (Antenna)
5. CP
6. Future
7. +/- (Format Selector)
8. D1 (Data Pin 1)
9. D0 (Data Pin 0)
10. LED (LED / Beeper)
11. +5V

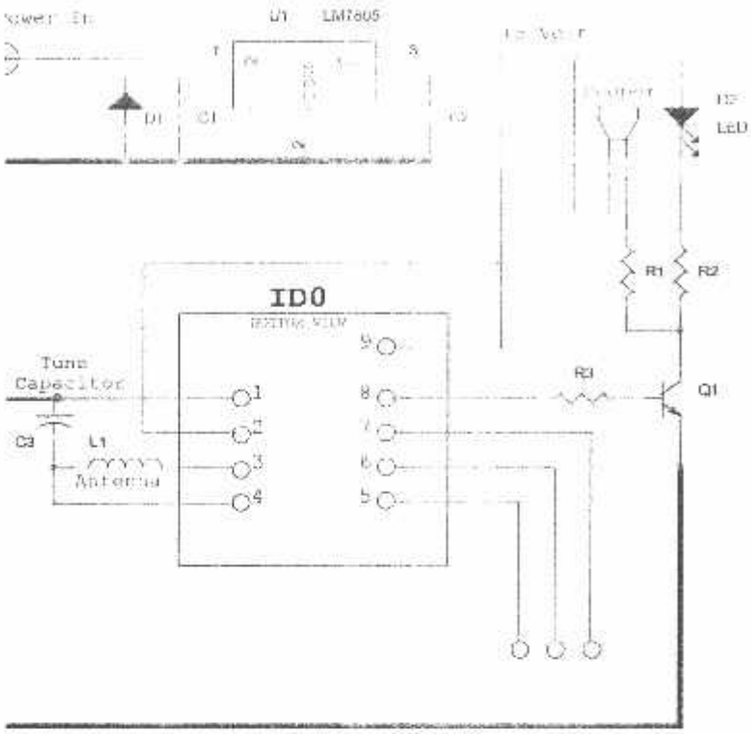
'perational and Physical Characteristics

Parameters	ID-2	ID-12	ID-20
Read Range	N/A (no internal antenna)	12+ cm	16+ cm
Dimensions	21 mm x 19 mm x 6 mm	26 mm x 25 mm x 7 mm	40 mm x 40 mm x 9 mm
Frequency	125 kHz	125 kHz	125 kHz
Card Format	EM 4001 or compatible	EM 4001 or compatible	EM 4001 or compatible
Encoding	Manchester 64-bit modulus 64	Manchester 64-bit modulus 64	Manchester 64-bit, modulus 64
Power Requirement	5 VDC @ 13mA nominal	5 VDC @ 30mA nominal	5 VDC @ 65mA nominal
I/O Output Current	+/-200mA PK	-	-
Voltage Supply Range	+4.6V through +5.4V	+4.6V through +5.4V	+4.6V through +5.4V

in Description & Output Data Formats

Pin No.	Description	ASCII	Magnet Emulation	Wiegand26
Pin 1	Zero Volts and Tuning Capacitor Ground	GND 0V	GND 0V	GND 0V
Pin 2	Strap to +5V	Reset Bar	Reset Bar	Reset Bar
Pin 3	To External Antenna and Tuning Capacitor	Antenna	Antenna	Antenna
Pin 4	To External Antenna	Antenna	Antenna	Antenna
Pin 5	Card Present	No function	Card Present	No function
Pin 6	Future	Future	Future	Future
Pin 7	Format Selector (+/-)	Strap to GND	Strap to Pin 10	Strap to +5V
Pin 8	Data 1	CMOS	Clock	One Output
Pin 9	Data 0	TTL Data (inverted)	Data	Zero Output
Pin 10	3.1 kHz Logic	Beeper / LED	Beeper / LED	Beeper / LED
Pin 11	DC Voltage Supply	+5V	+5V	+5V

ircuit Diagram for the ID0



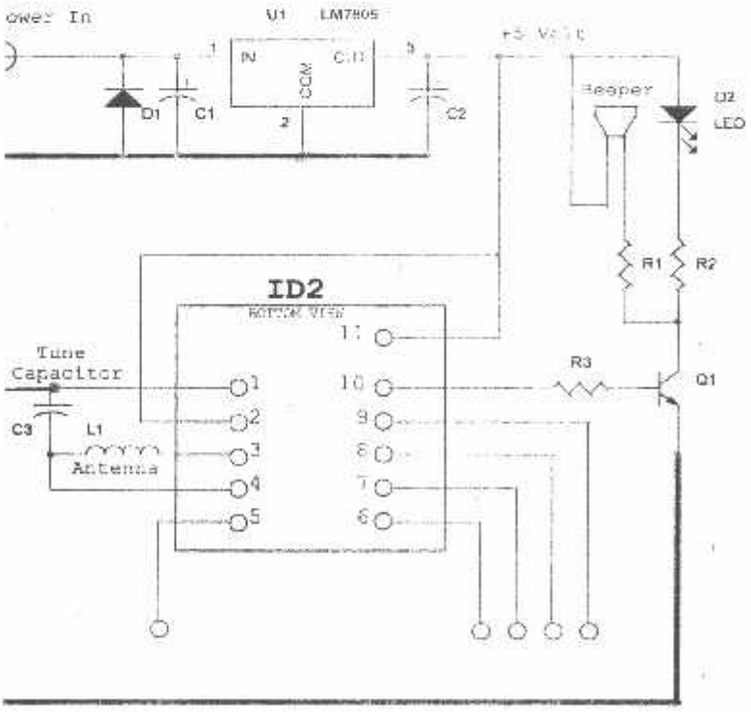
COMPONENT LIST
R1 = 100R
R2 = 1K
R3 = 1K
C1 = 100uF 16V
C2 = 100uF 10V
C3 = 1nF COG 100V *
Beeper = 2.7-3.5KHz 100R
D1 = 1N4001
D2 = GREEN LED
U1 = LM7805
Q1 = UTC8050 (NPN)
L1 = 640Uh

ID0 = ID Innovations ID0

* Please Note the ID0 has an internal tuning capacitor of 1.5nF and this makes the total tuning capacity = 2.5nF

The 3.1Khz Beeper Logic is centered for most Beepers in range 2.7-3.5Khz

ircuit Diagram for the ID2



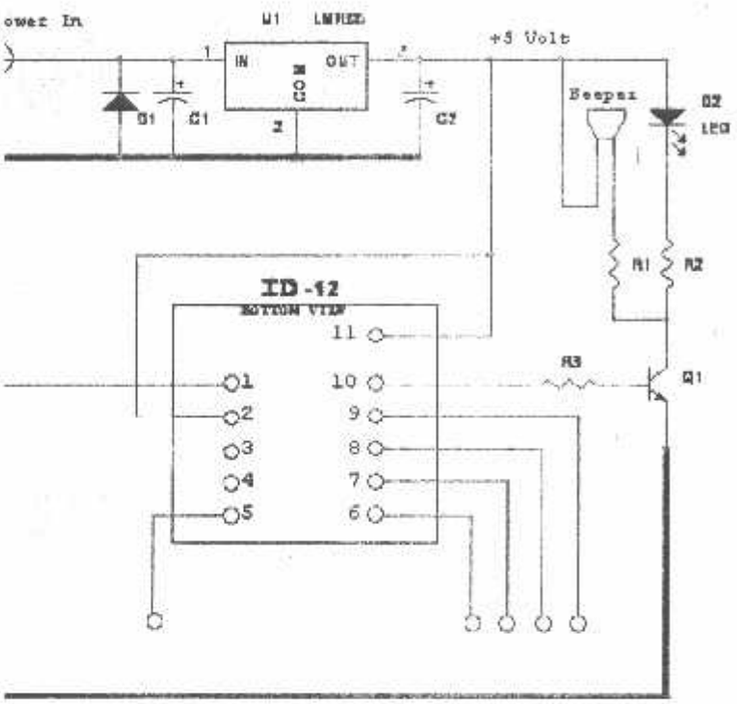
COMPONENT LIST
R1 = 100R
R2 = 1K
R3 = 1K
C1 = 100uF 16V
C2 = 100uF 10V
C3 = 1nF COG 100V *
Beeper = 2.7-3.5KHz 100R
D1 = 1N4001
D2 = GREEN LED
U1 = LM7805
Q1 = UTC8050 (NPN)
L1 = 640Uh

ID2 = ID Innovations ID2

* Please Note the ID2 has an internal tuning capacitor of 1.5nF and this makes the total tuning capacity = 2.5nF

The 3.1Khz Beeper Logic is centered for most Beepers in range 2.7-3.5Khz

Circuit Diagram for the ID-12



COMPONENT LIST

R1 = 100R
R2 = 1K
R3 = 1K
C1 = 100uF 16V
C2 = 100uF 10V
Beeper = 2.7-3.5KHz 100R
D1 = 1N4001
D2 = GREEN LED
U1 = LM7805
Q1 = UTC8050 (NPN)
ID2 = ID Innovations ID2

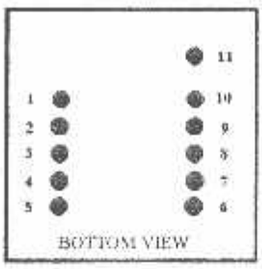
* Please Note the ID2 has an internal tuning capacitor of 1.5nF and this makes the total tuning capacity = 2.5nF

The 3.1Khz Beeper Logic is centered for most Beepers in range 2.7-3.5Khz

ID-2RW. ID-12RW Brief Data

ıe ID2-RW, ID12-RW and ID15-RW are a new series of ead/Write modules for the Temec Q5 tag. It has full functionality cluding password. They contain built-in algorithms to assist ıstomers programming the popular Sokymat Unique type tag. ıssword protection is allowed. Control is via a host computer using simple terminal program such as hyper terminal or Qmodem.

ID2 / ID12 / ID20 PIN-OUT



1 GND
2 RES (Reset Bar)
3 ANT (Antenna)
4 ANT (Antenna)
5 Future
6 Program LED
7 ASCII in
8 Future
9 ASCII Out
10 Read (LED / Beeper)
11 +5V

perational and Physical Characteristics

Parameters	ID-2RW	ID-12RW	ID-20RW
ead Range	N/A (no internal antenna)	12+ cm (Unique Format)	15+ cm (Unique Format)
imensions	21 mm x 19 mm x 6 mm	26 mm x 25 mm x 7 mm	40 mm x 40 mm x 9 mm
requency	125 kHz	125 kHz	125 kHz
ard Format	Temec Q5555	Temec Q5555	Temec Q5555
ead Encoding	Manchester modulus 64	Manchester modulus 64	Manchester modulus 64
ower Requirement	5 VDC @ 13mA nominal	5 VDC @ 30mA nominal	5 VDC @ 50mA nominal
O Output Current	+/-200mA PK	-	-
oltage Supply Range	+4.6V through +5.4V	+4.6V through +5.4V	+4.6V through +5.4V
oil Detail	L = 0.6mH - 1.5mH, Q = 15-30	-	-

escription

host computer is required to send the commands to the module. A simple terminal program such as Qmodem or per-terminal can be used to send commands to the module. The blocks are individually programmable. If you have er found that the Q5 can be a bit 'Twitchy' to program this programmer module is your solution. The command erface is simple to use and easily understood. The programmer also has two types of internal reader. One of these is ovided to read Sokymat 'Unique' type tag configuration.

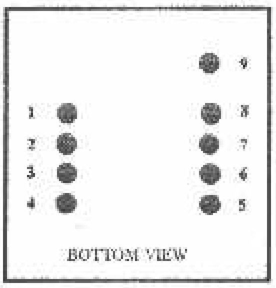
Low Cost Short-Range Proximity Readers

ID-0 / ID-10 / ID-15 MK(ii) Series

aintenance [illegible] Consider using [illegible] ID-2 [illegible] and the ID-20 that ve improved performance.

ne ID Series short-range readers come in three different sizes and ad ranges. Both the ID-10 and ID-15 come with internal antennas id have read ranges of 12+ cm and 16+ cm, respectively. With an ternal antenna, the ID-0 MK(ii) can deliver read ranges of up to 25 n. All three readers support ASCII and Wiegand26 data formats.

ID0 / ID10 / ID15 PIN-OUT



1. GND
2. RES (Reset Bar)
3. ANT (Antenna)
4. ANT (Antenna)
5. +/- (Format Selector)
6. D1 (Data Pin 1)
7. D0 (Data Pin 0)
8. LED (LED / Beeper)
9. +5V

perational and Physical Characteristics

Parameters	ID-0	ID-10	ID-15
Read Range	N/A (no internal antenna)	12+ cm	15+ cm
Dimensions	21 mm x 19 mm x 6 mm	26 mm x 25 mm x 7 mm	40 mm x 40 mm x 9 mm
Frequency	125 kHz	125 kHz	125 kHz
Card Format	EM 4001 or compatible	EM 4001 or compatible	EM 4001 or compatible
Encoding	Manchester 64-bit, modulus 64	Manchester 64-bit, modulus 64	Manchester 64-bit, modulus 64
Power Requirement	5 VDC @ 13mA nominal	5 VDC @ 30mA nominal	5 VDC @ 50mA nominal
IO Output Current	+/-200mA PK	-	-
Voltage Supply Range	+4.6V through +5.4V	+4.6V through +5.4V	+4.6V through +5.4V

'n Description & Output Data Formats

Pin No.	Description	ASCII	Wiegand26
Pin 1	Zero Volts and Tuning Capacitor Ground	GND 0V	GND 0V
Pin 2	Strap to +5V	Reset Bar	Reset Bar
Pin 3	To External Antenna and Tuning Capacitor	Antenna	Antenna
Pin 4	To External Antenna	Antenna	Antenna
Pin 5	Format Selector (+/-)	Strap to GND	Strap to +5V
Pin 6	Data 1	CMOS	One Output
Pin 7	Data 0	TTL Data (inverted)	Zero Output
Pin 8	3.1 kHz Logic	Beeper / LED	Beeper / LED
Pin 9	DC Voltage Supply	+5V	+5V

ATA FORMATS

utput Data Structure – ASCII

STX (02h)	DATA (10 ASCII)	CHECK SUM (2 ASCII)	CR	LF	ETX (03h)

he 1byte (2 ASCII characters) Check sum is the "Exclusive OR" of the 5 hex bytes (10 ASCII) Data characters.]

utput Data Structure – Wiegand26

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	E	E	E	E	E	E	E	E	E	E	E	E	O	O	O	O	O	O	O	O	O	O	O	O	P
	Even parity (E)												Odd parity (O)												

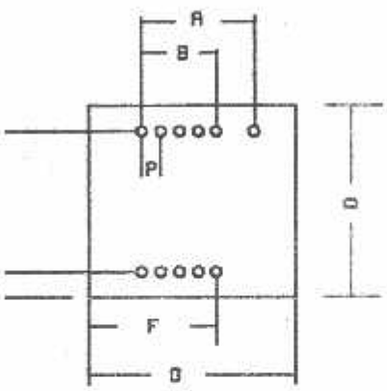
Parity start bit and stop bit

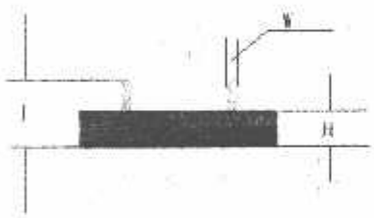
utput Data Magnetic ABA Track2

10 Leading Zeros	SS	Data	ES	LCR	10 Ending Zeros

5 is the Start Character of 11010, ES is the end character of 11111, LRC is the Longitudinal Redundancy Check.]

imensions (Top View) (mm)





ID-0/ID-2			ID-10/ID-12			ID-15/ID-20		
Nom.	Min.	Max.	Nom.	Min.	Max.	Nom.	Min.	Max
12.0	11.6	12.4	12.0	11.6	12.4	12.0	11.6	12.4
8.0	7.6	8.4	8.0	7.6	8.4	8.0	7.6	8.4
15.0	14.6	15.4	15.0	14.6	15.4	15.0	14.6	15.4
20.5	20.0	21.5	25.3	24.9	25.9	40.3	40.0	41.0
18.5	18.0	19.2	20.3	19.8	20.9	27.8	27.5	28.5
14.0	13.0	14.8	16.3	15.8	16.9	22.2	21.9	23.1
22.0	21.6	22.4	26.4	26.1	27.1	38.5	38.2	39.2
2.0	1.8	2.2	2.0	1.8	2.2	2.0	1.8	2.2
5.92	5.85	6.6	6.0	5.8	6.6	6.8	6.7	7.0
9.85	9.0	10.5	9.9	9.40	10.5	9.85	9.4	10.6
0.66	0.62	0.67	0.66	0.62	0.67	0.66	0.62	0.67

ote – measurements do not include any burring of edges.

DTCE - Innovated Devices reserve the right to change these specifications without prior notice.

19-0175; Rev 3; 1/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

Hand-Held Equipment

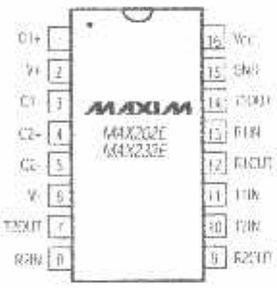
Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

LapLink is a registered trademark of Traveling Software, Inc.

ABSOLUTE MAXIMUM RATINGS

VCC ..... -0.3V to +6V
V+ ..... (VCC - 0.3V) to +14V
V- ..... -14V to +0.3V
Input Voltages
T_IN ..... -0.3V to (V+ + 0.3V)
R_IN ..... ±30V
Output Voltages
T_OUT ..... (V- - 0.3V) to (V+ + 0.3V)
R_OUT ..... -0.3V to (VCC + 0.3V)
Short-Circuit Duration, T_OUT ..... Continuous
Continuous Power Dissipation (TA = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ... 889mW
20-Pin SO (derate 10.00mW/°C above +70°C) ... 800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) ... 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C) ... 1.14W
24-Pin SO (derate 11.75mW/°C above +70°C) ... 941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) ... 640mW
28-Pin SO (derate 12.50mW/°C above +70°C) ... 1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) ... 762mW
Operating Temperature Ranges
MAX2__EC_ _ ... 0°C to +70°C
MAX2__EE_ _ ... -40°C to +85°C
Storage Temperature Range ... -65°C to +165°C
Lead Temperature (soldering, 10sec) ... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
VCC Supply Current	ICC	No load, TA = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		TA = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to VCC (MAX202E/203E/232E)				±10	µA
Input Threshold Low	VIL	T_IN, EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	VIH	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	VOL	R_OUT; IOUT = 3.2mA (MAX202E/203E/232E) or IOUT = 1.6mA (MAX205E/206E/211E/213E/241E)				0.4	V
Output Voltage High	VOH	R_OUT; IOUT = -1.0mA		3.5	VCC - 0.4		V
Output Leakage Current		$\overline{EN}$ = VCC; T_IN = 0V, 0V ≤ ROUT ≤ VCC; MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

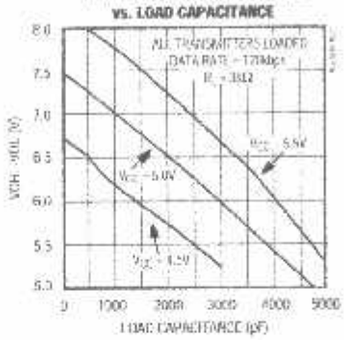
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, $\overline{EN}$ = V_{CC}	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, $\overline{EN}$ = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		V_{CC} = V_+ = V_- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PHL}, t_{PLH}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, $\overline{EN}$ = V_{CC}		4	40	
Receiver Output Enable Time		MAX205E/208E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLH}, t_{PHL}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, measured from 3V to -3V or -3V to 3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211E_ _ tested with V_{CC} = +5V ±5%.

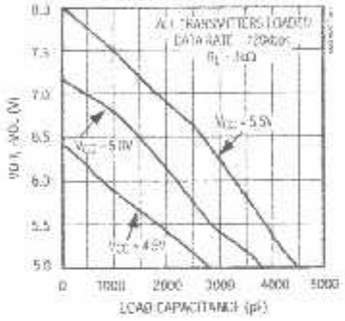
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

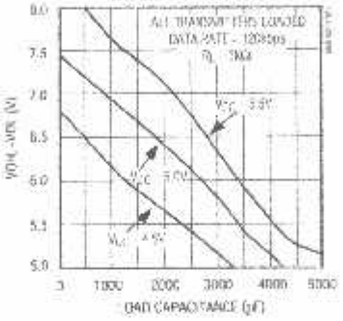
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



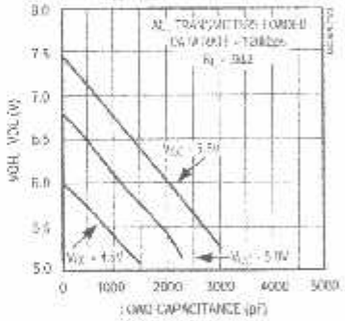
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



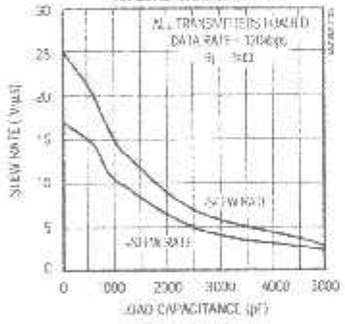
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



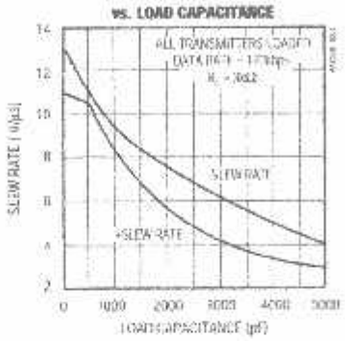
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



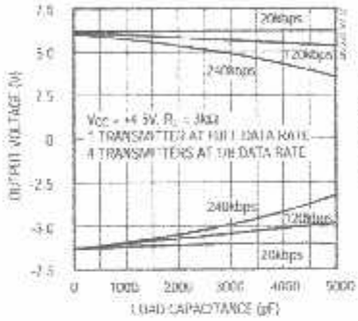
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

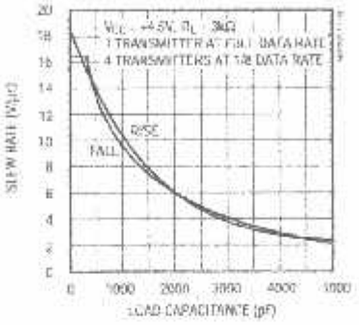
MAX202E/MAX203E/MAX232E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



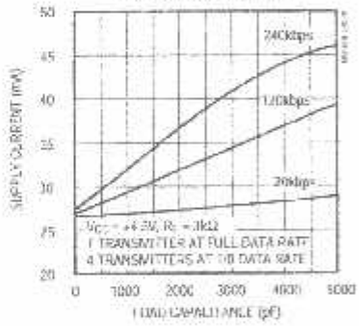
MAX205E–MAX208E TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



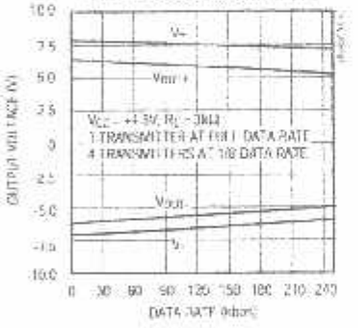
MAX205E–MAX208E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



MAX205E–MAX208E SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX205E–MAX208E OUTPUT VOLTAGE vs. DATA RATE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2Vcc voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge pump capacitor
6	8	V-	-2Vcc voltage generated by the charge pump
7, 14	9, 10	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	Vcc	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	Vcc	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2Vcc voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2Vcc voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together

MAX205E

PIN	NAME	FUNCTION
1, 4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to Vcc.
11	GND	Ground
12	Vcc	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

Pin Descriptions (continued)

MAX206E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V-	-2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V+	+2V_{CC} generated by the charge pump
20	EN	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V_+	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V_-	-2V_{CC} generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V-	+2V_{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V_{CC} generated by the charge pump

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 16, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to Vcc.
10	GND	Ground
11	Vcc	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	+2Vcc voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2Vcc voltage generated by the charge pump
24	EN	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	SHDN	Shutdown Control—active low (MAX213E)

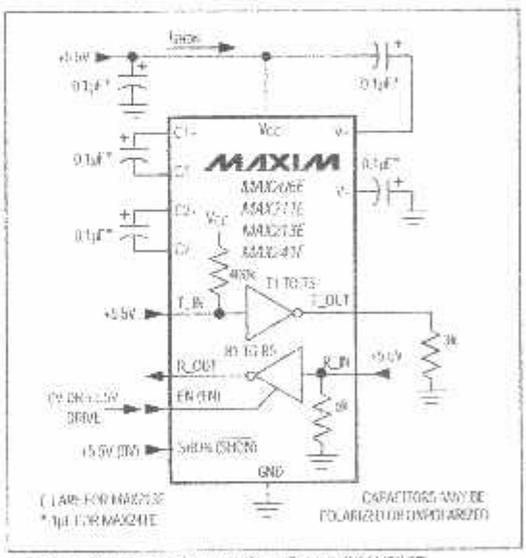


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX241E)

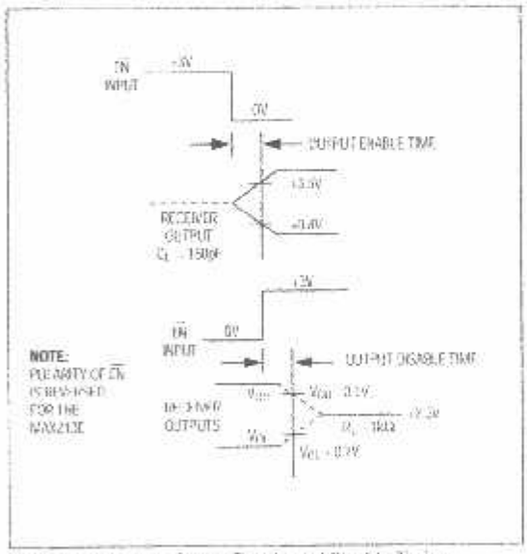


Figure 2. Receiver Output Enable and Disable Timing (MAX205/MAX206E/MAX211E/MAX213E/MAX241E)

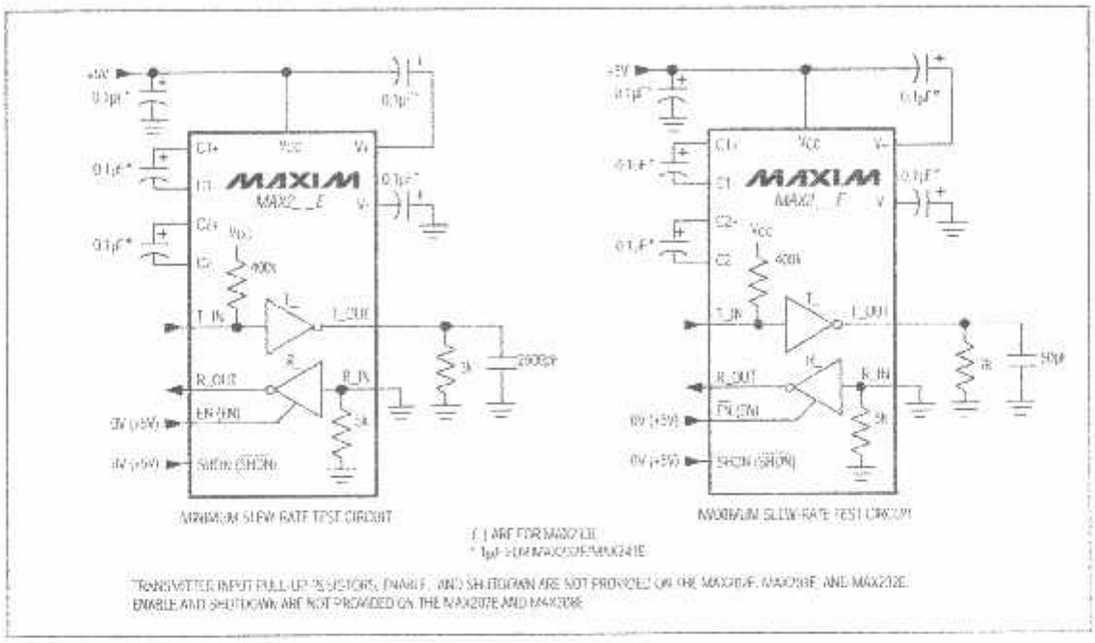


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non "E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V input to +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to Vcc by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With Vcc = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum Vcc, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to Vcc are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA 232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

In shutdown mode, the charge pumps are turned off, V- is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E ($\overline{EN}$), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E ($\overline{SHDN}$).

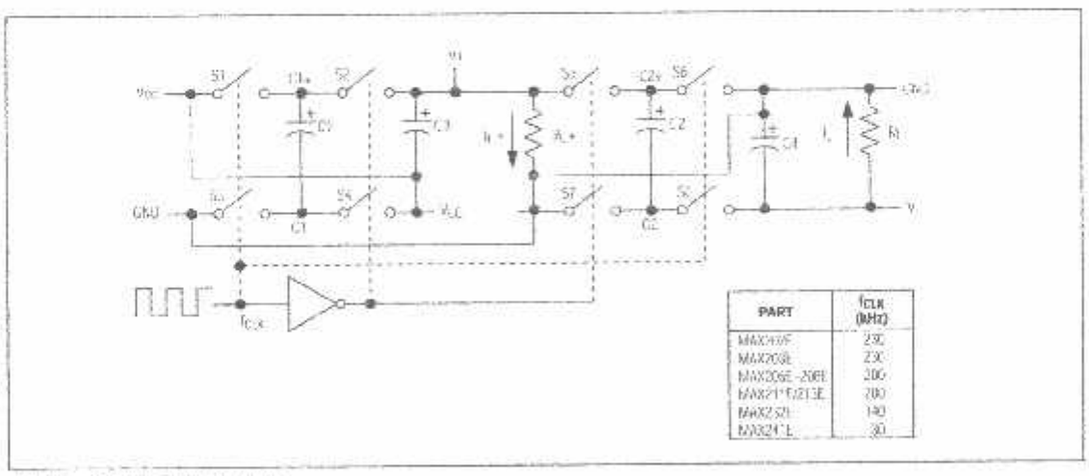


Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after SHDN is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

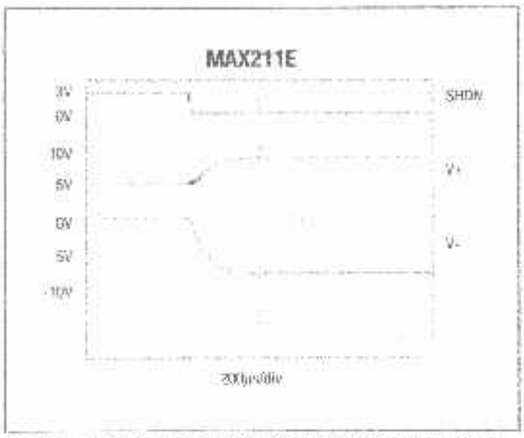


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

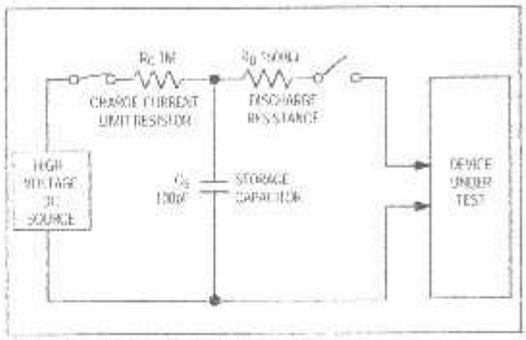


Figure 6a. Human Body ESD Test Model

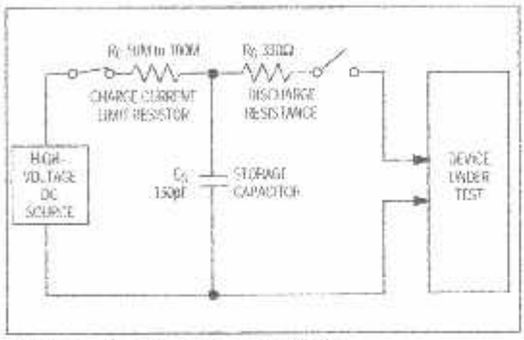


Figure 7a. IEC1000-4-2 ESD Test Model

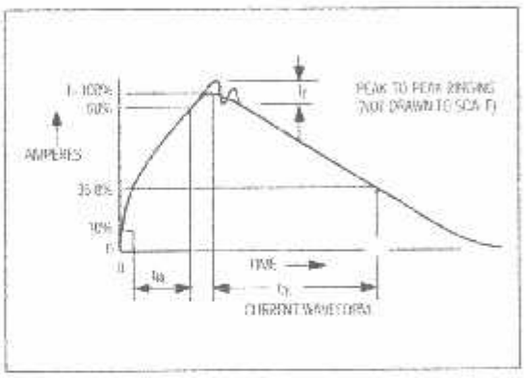


Figure 6b. Human Body Model Current Waveform

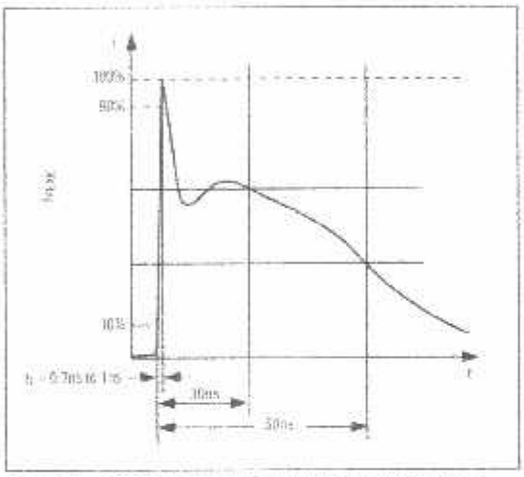


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level four ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205F have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

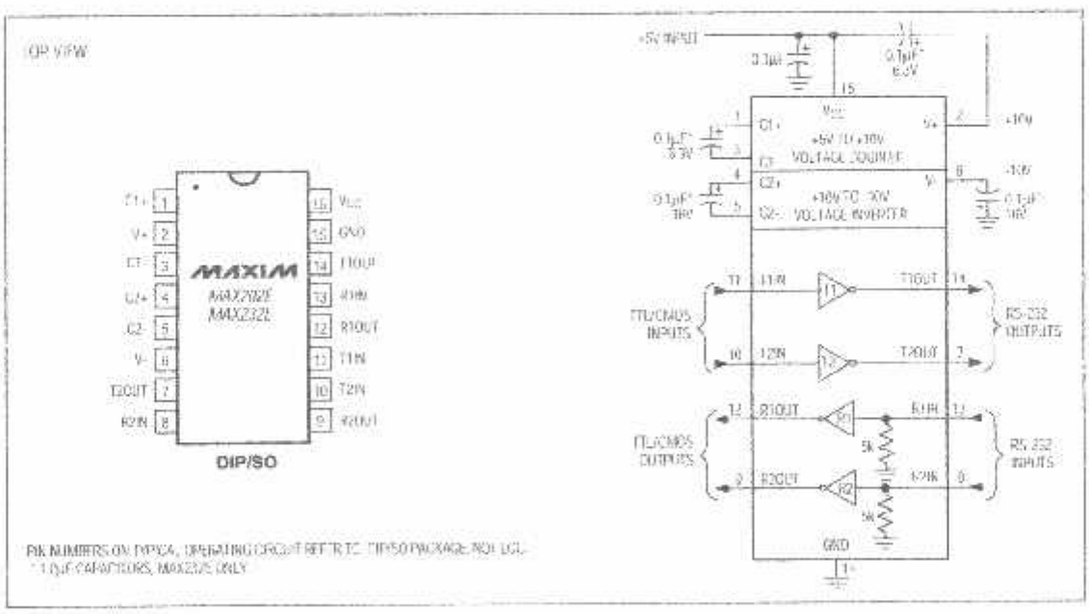
Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	S Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		$-2V < V_{OUT} < +2V$	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

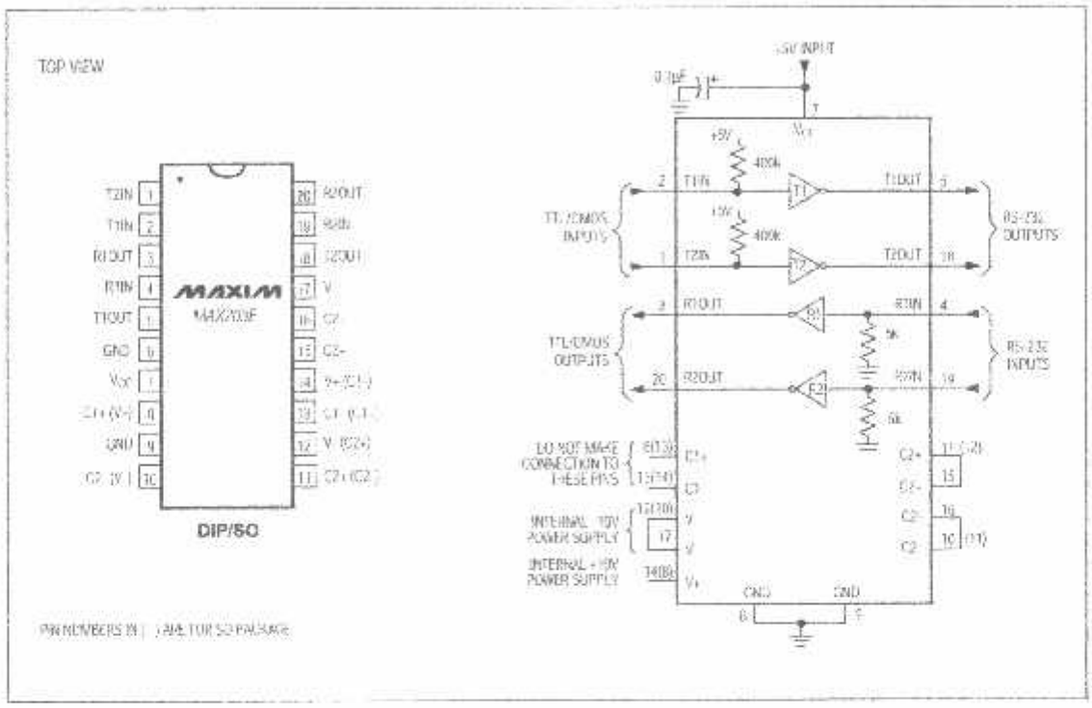
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)

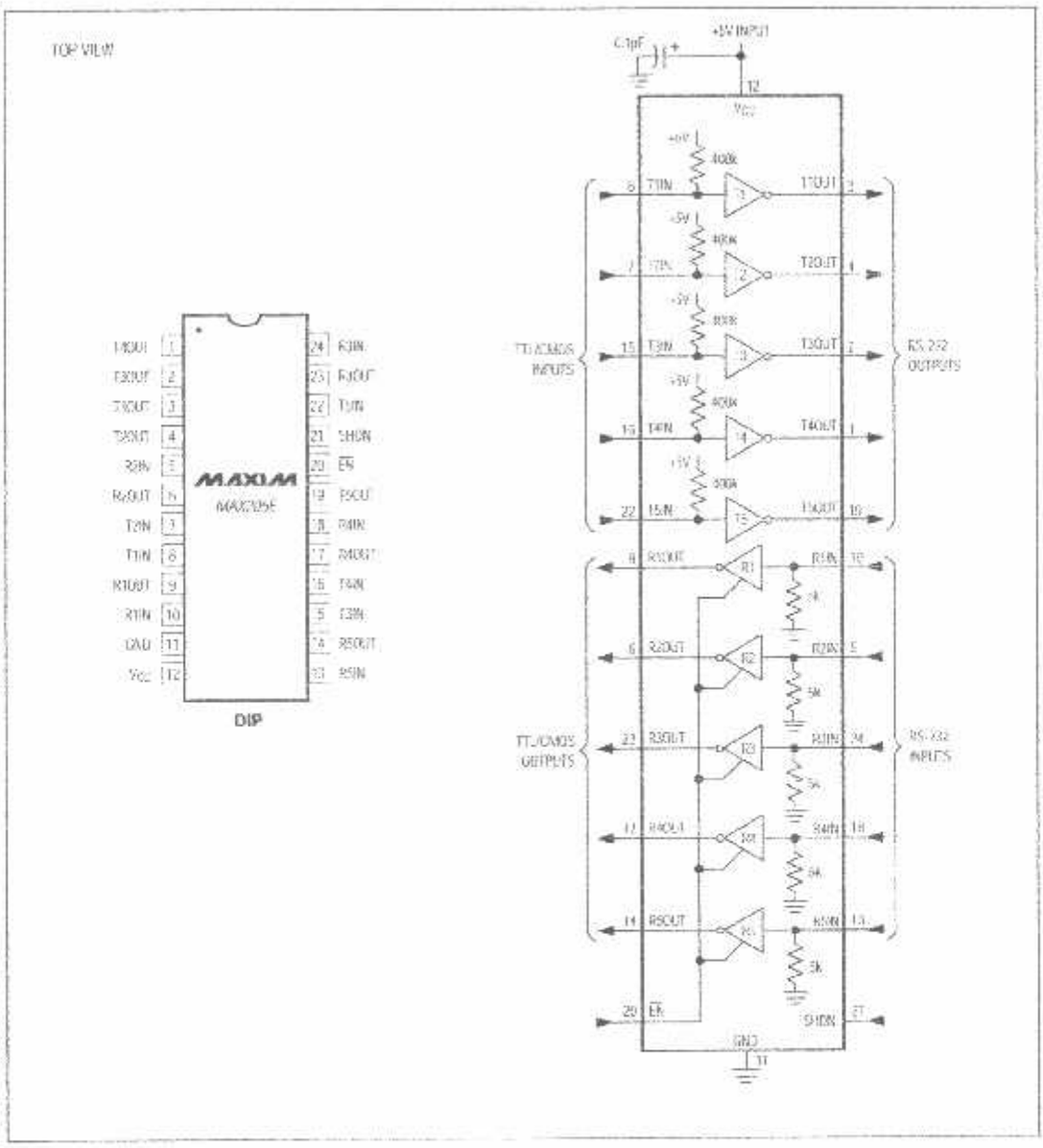


PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE. NOTE: ALL 0.1µF CAPACITORS, MAX232/E ONLY.

Pin Configurations and Typical Operating Circuits (continued)

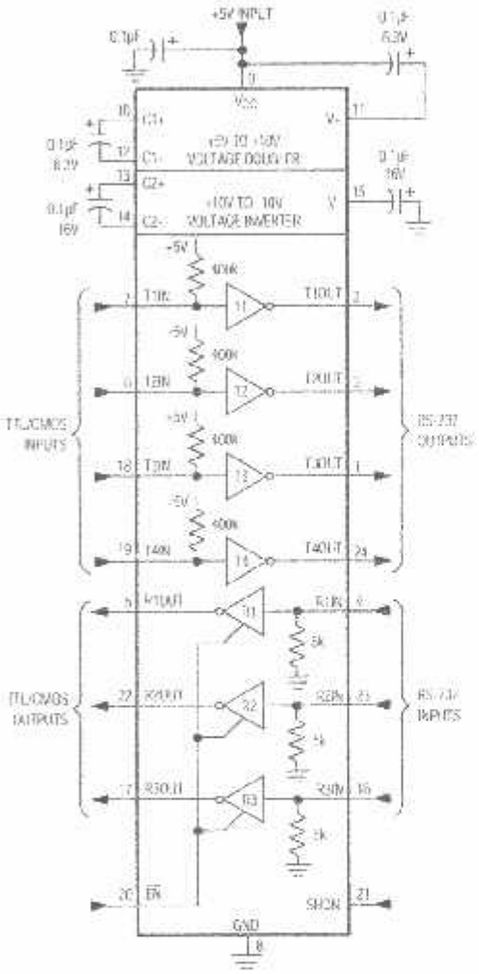


Pin Configurations and Typical Operating Circuits (continued)

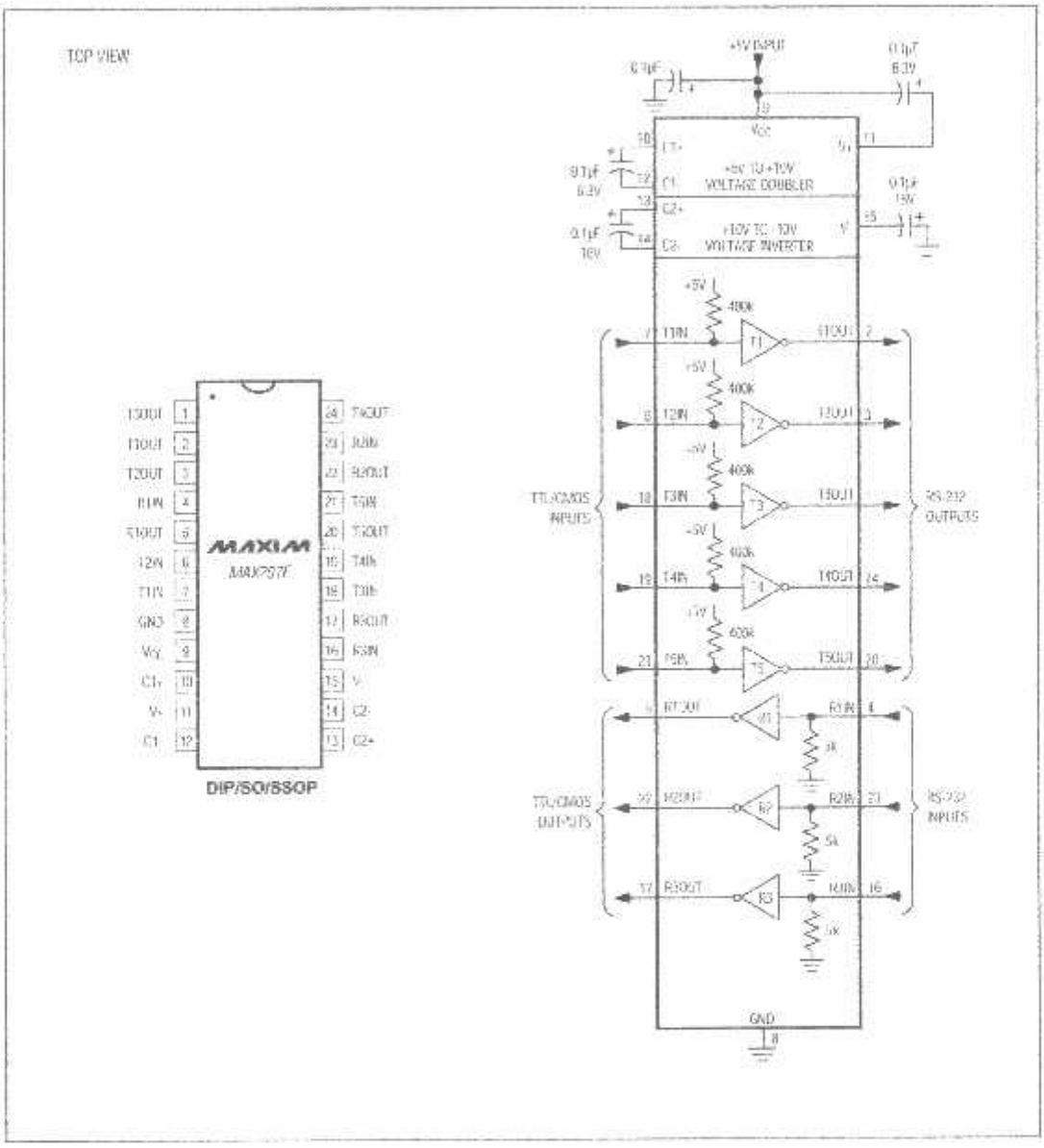


Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

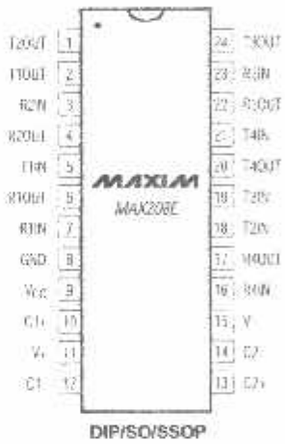


Pin Configurations and Typical Operating Circuits (continued)

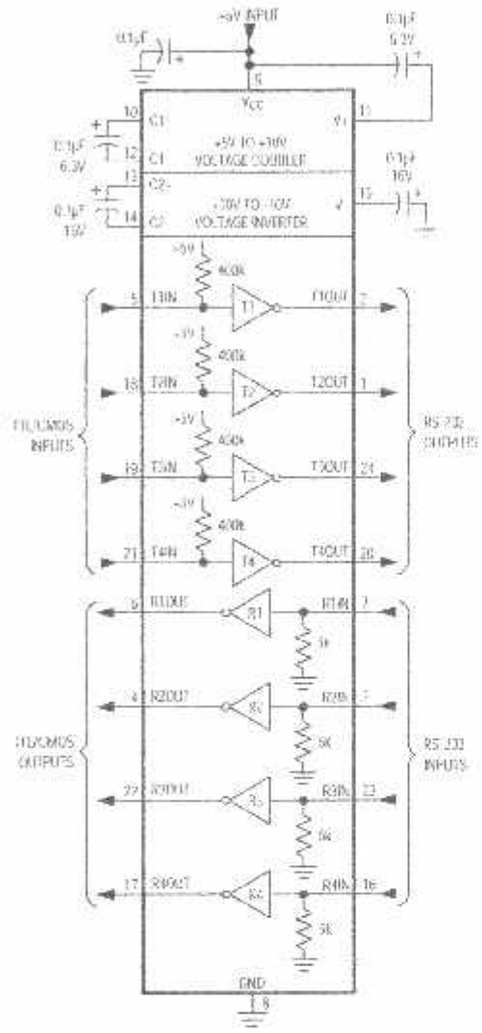


Pin Configurations and Typical Operating Circuits (continued)

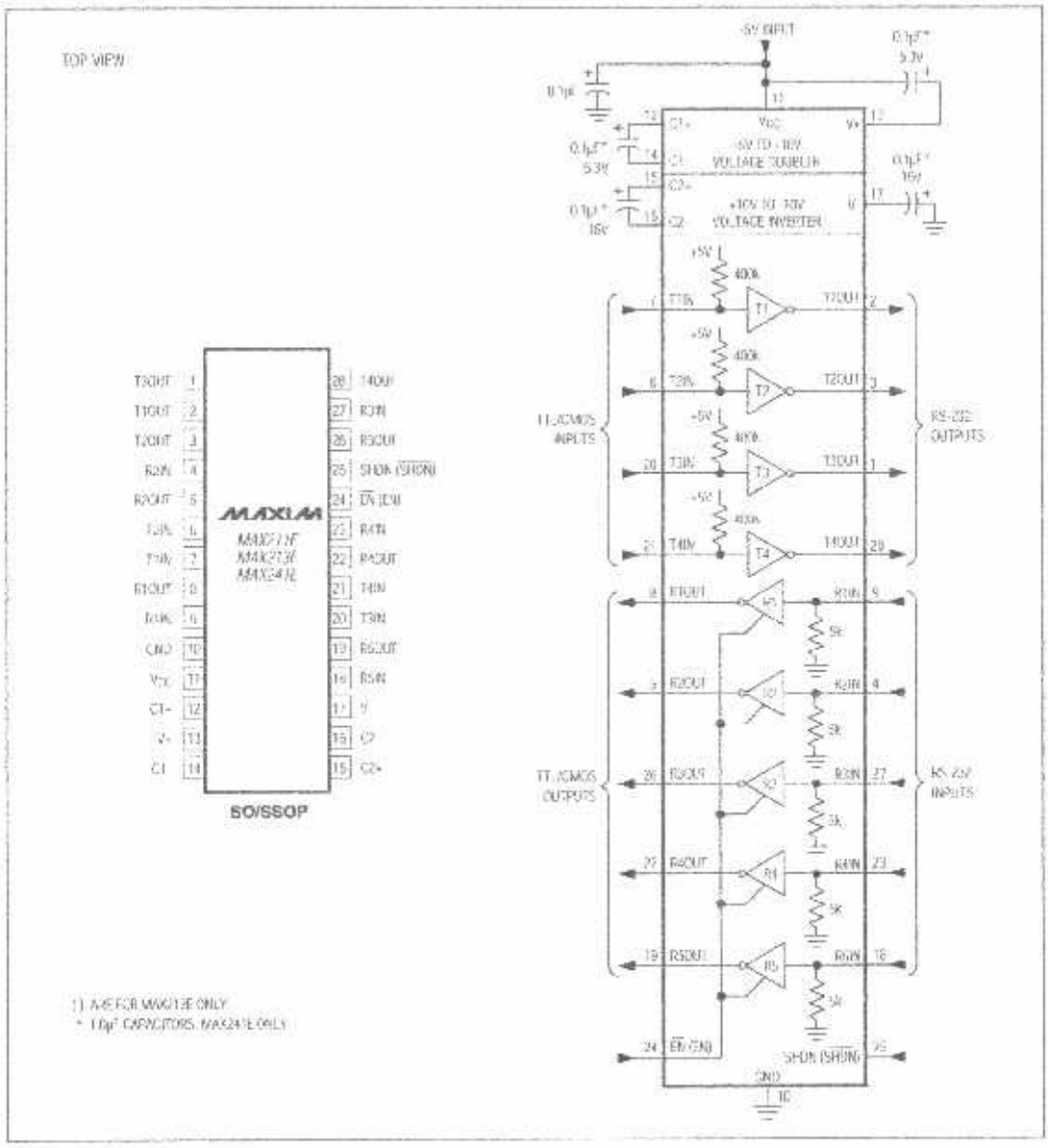
TOP VIEW



DIP/SO/SSOP



Pin Configurations and Typical Operating Circuits (continued)



Ordering Information

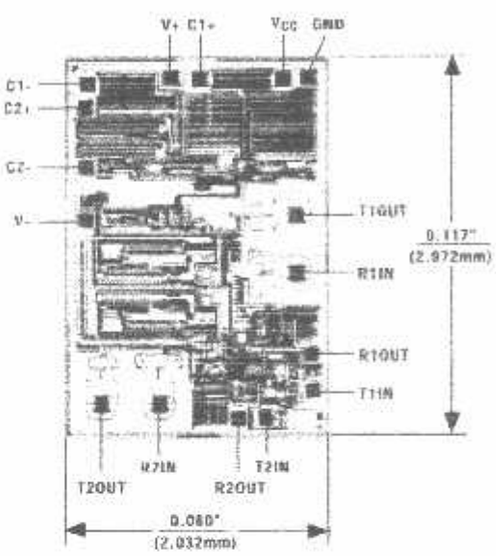
PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO
MAX203ECPP	0°C to +70°C	20 Plastic DIP
MAX203ECWP	0°C to +70°C	20 SO
MAX203EEPP	-40°C to +85°C	20 Plastic DIP
MAX203EEWP	-40°C to +85°C	20 SO
MAX205ECPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206ECWG	0°C to +70°C	24 SO
MAX206ECAG	0°C to +70°C	24 SSOP
MAX206EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EEWG	-40°C to +85°C	24 SO
MAX206EEAG	-40°C to +85°C	24 SSOP
MAX207ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207ECWG	0°C to +70°C	24 SO
MAX207ECAG	0°C to +70°C	24 SSOP
MAX207EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EEWG	-40°C to +85°C	24 SO
MAX207EEAG	-40°C to +85°C	24 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX208ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208ECWG	0°C to +70°C	24 SO
MAX208ECAG	0°C to +70°C	24 SSOP
MAX208EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EEWG	-40°C to +85°C	24 SO
MAX208EEAG	-40°C to +85°C	24 SSOP
MAX211ECWI	0°C to +70°C	28 SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EEWI	-40°C to +85°C	28 SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EEWI	-40°C to +85°C	28 SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EEPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX241ECWI	0°C to +70°C	28 SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EEWI	-40°C to +85°C	28 SO
MAX241EEAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

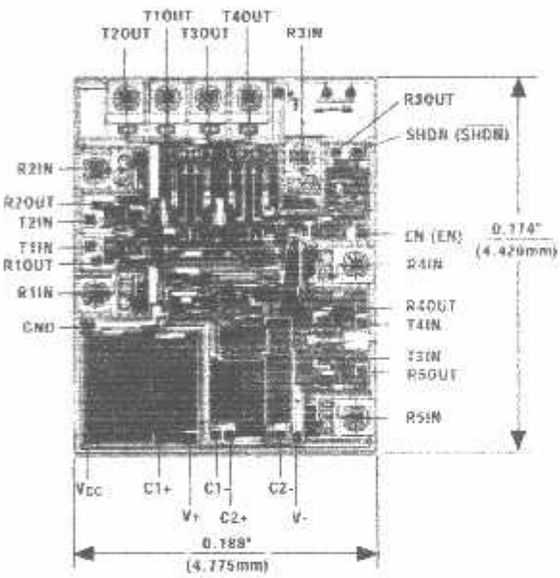
Chip Topographies

MAX202E/MAX232E



TRANSISTOR COUNT: 123
SUBSTRATE CONNECTED TO GND

MAX211E/MAX213E/MAX241E



( ) ARE FOR MAX213E ONLY

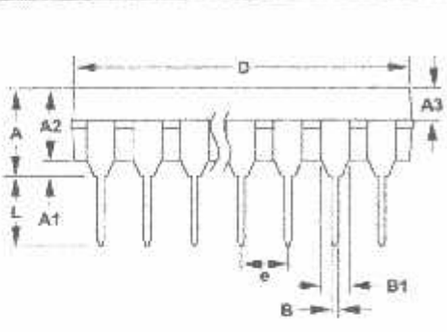
TRANSISTOR COUNT: 542
SUBSTRATE CONNECTED TO GND

Chip Information

MAX205E/MAX206E/MAX207E/MAX208E

TRANSISTOR COUNT: 328
SUBSTRATE CONNECTED TO GND

Package Information

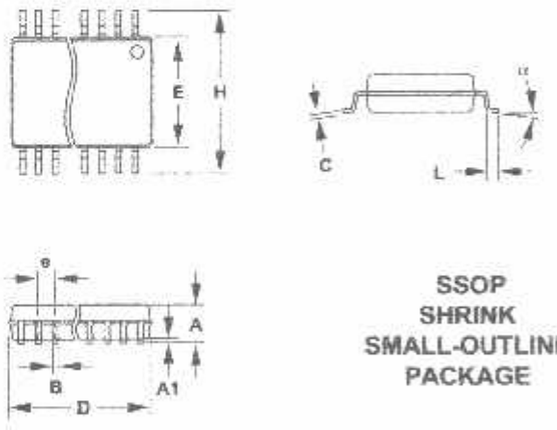


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043B



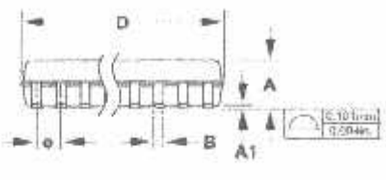
SSOP
SHRINK
SMALL-OUTLINE
PACKAGE

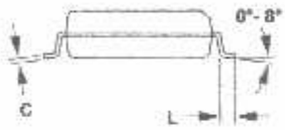
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.37	8.33
D	28	0.397	0.407	10.07	10.33

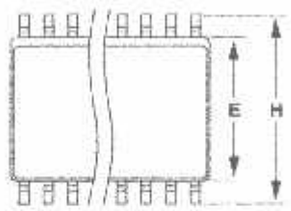
21-0056A

Package Information (continued)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

LCM

Liquid Crystal Display Modules

Seiko Instruments GmbH

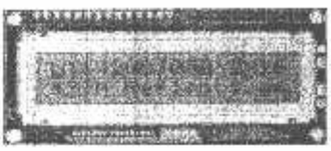
ıt Matrix Liquid Crystal Display Modules

ıRACTER TYPE

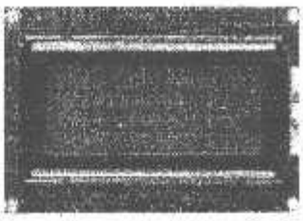
FEATURES :

- Slim, light weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interfacing
- LCD modules with built-in EL or LED backlight

M1641



L1642



L1614

M1632

L1652

L2012

• SPECIFICATIONS :

[ ]: Standard products [ ]: Products of optional specification

Format (character x line)		16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
		M1641	M1632	L1642	L1652	L1614	L2012
		M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
ht		M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
ight		M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
(wide temp)		M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
ight (wide temp)		M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
	Reflective	80.0 x 36.0 x 11.3	85.0 x 36.0 x 10.7	80.0 x 36.0 x 11.3	122.0 x 44.0 x 11.3	87.0 x 60.0 x 11.6	116.0 x 37.0 x 11.3
	EL backlight	80.0 x 36.0 x 11.3	85.0 x 36.0 x 10.7	80.0 x 36.0 x 11.3	122.0 x 44.0 x 11.3	87.0 x 60.0 x 11.6	116.0 x 37.0 x 11.3
nm	LED backlight	80.0 x 36.0 x 15.8	85.0 x 36.0 x 15.8	80.0 x 36.0 x 15.8	122.0 x 44.0 x 15.8	87.0 x 60.0 x 15.8	116.0 x 37.0 x 15.8
rea (HxV) mm		64.5 x 15.8	62.0 x 16.0	64.5 x 13.8	99.0 x 24.0	61.6 x 25.2	83.0 x 18.6
size (HxV) mm	*1	3.87 x 5.73	2.75 x 4.27	2.95 x 3.60	4.84 x 8.06	2.95 x 4.15	3.20 x 4.85
dxV) mm		0.55 x 0.75	0.50 x 0.55	0.50 x 0.55	0.92 x 1.10	0.55 x 0.55	0.60 x 0.65
ply voltage (VDD-VSS) V		+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
nsumption	IDD	1.5	2.0	1.6	2.0	2.7	2.0
	ILC *4	0.2	0.2	0.3	0.4	1.1	0.4
ethod (duty)		1/16	1/16	1/16	1/16	1/16	1/16
		KS0066 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent
temperature (°C)	normal temp.	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
mperature (°C)	normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
	Reflective	25	25	25	50	50	40
	EL backlight	30	30	30	55	55	45
	LED backlight	35	40	35	65	65	60
	Model	5S	5S	5S	5C	5A	5A
	Power supply (V)	+5.0	+5.0	+5.0	+5.0	+5.0	+5.0
	current consumption (mA) *3	10	10	10	35	45	45
	Forward current consumption (mA)	103	112	103	240	200	154
	Forward input voltage (V,typ.)	+4.1	+4.1	+4.1	+4.1	+4.1	+4.1

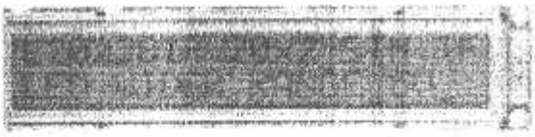
ing cursor H : Horizontal V : Vertical T : Thickness (max)

dernal temperature compensation

ng EL backlight

on normal temperature range

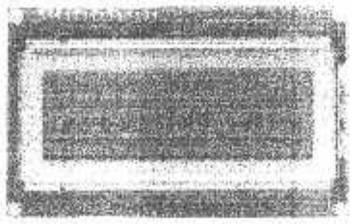
olicy is one of continues improvements we reserve the right to change the specifications for the products in the catalogue without notice.



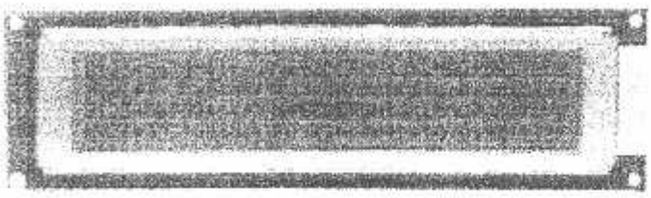
L2022

L2432

L4042



L2014



M4024

• SPECIFICATIONS :

[ ] : Standard products [ ] : Products of optional specification

aracter Format (character x line)		20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
odel		L2022	L2014	L2432	L4042	M4024
flective			L201400J000S	L243200J000S	L404200J000S	M40240AS
backlight			L201421J000S	L243221J000S	L404221J000S	M40249DWS
D backlight			L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
flective (wide temp)		L202203F000S	L201400L000S	L243200L000S	L404200L000S	M40240CS
D backlight (wide temp)		L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
aracter font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
odule	Reflective	180,0 x 40,0 x 10,5	98.0 x 60.0 x 11.6	118,0 x 36,0 x 11.3	182.0 x 33,5 x 11.3	190.0 x 54.0 x 10.1
e	EL backlight	180,0 x 40,0 x 10,5	98.0 x 60.0 x 11.6	118,0 x 36,0 x 11.3	182.0 x 33,5 x 11.3	190.0 x 54.0 x 10.1
(VxT) mm	LED backlight	180,0 x 40,0 x 14,8	98.0 x 60.0 x 15.8	118,0 x 36,0 x 15.8	182.0 x 33,5 x 15.3	190.0 x 54.0 x 16.3
ewing area (HxV) mm		149.0 x 23,0	76.0 x 25,2	94.5 x 17.8	154.4 x 15.8	147.0 x 29,5
aracter size (HxV) mm *1		5,00 x 5.66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,70 x 4,27
t size (HxV) mm		1,12 x 1.12	0,55 x 0,55	0,60 x 0,65	0,60 x 0 65	0,50 x 0,55
wer supply voltage (VDD-VSS) V		+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
rrent consumption	IDD	4,2	2,9	2,5	3,0	8,0
A typ)	ILC *4	2,6	1,2	0,5	1,0	3,0
ving method (duty)		1/16	1/16	1/16	1/16	1/16
ilt-in LSI		KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent
erating temperature (°C)	normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	- 20 to + 70	- 20 to - 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
rage temperature (°C)	normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
ight	Reflective	80	55	40	70	90
typ.)	EL backlight	-	60	45	75	105
	LED backlight	110	70	60	95	140
	Model		5A	5A	5C	5D
erters	Power supply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
EL	current consumption (mA) *3	-	45	45	25	60
D	Forward current consumption (mA)	320	240	150	260	480
klight	Forward input voltage (V typ.)	+ 4.1	+ 4.1	+ 4.1	+ 4,1	+ 4,1

: Excluding cursor H : Horizontal V : Vertical T : Thickness (max)

: With external temperature compensation

: Including EL backlight

. Based on normal temperature range

ot Matrix Liquid Crystal Display Modules

:APHIC TYPE

FEATURES :

- •Wide viewing angle and high contrast
- •Full dot configuration fits any application
- •Slim, light weight and low power consumption
- •Available in STN and FSTN

• SPECIFICATIONS :

(HxV dot)			97 x 32	128 x 32	128 x 64	128 x 64
			Y97031	G1233	G1216	G1226
le)	Reflective	built-in RAM	-	-	-	-
	Reflective wide temp.	built-in RAM		G121300N000S	G121600N000S	-
	LED backlight	built-in RAM		-	-	G12268N000S
	LED backlight wide temp.	built-in RAM		G12138N000S	G12168N000S	-
	Transmissive	-	-	-	-	-
le)	with CFL backlight	built-in controller	-	-	-	-
	Transflective	built-in RAM	Y97031LF60W	-	-	-
e	Reflective (no backlight)		47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
)	LED backlight			75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,8	93,0 x 70,0 x 11,4
	CFL backlight		-	-	-	-
ea (HxV) mm			43,5 x 23,3	60,0 x 21,3	60,0 x 32,5	70,7 x 38,8
(x V) mm			0,35 x 0,49	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
H x V) mm			0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
ply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	-	- 8,0	- 8,1	-8,2
nsumption		IDD	0,10	2,0	2,0	3,0
		IDD (built-in controller)	-	-	-	-
		ILC	-	1,8	1,8	2,0
	Driving method (duty)		1/33	1/64	1/64	1/64
		Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
		Controller	-	-	-	-
emperature range (°C)			- 20 to + 70	- 20 to + 70	- 20 to + 70	0 to + 50
mperature range (°C)			- 30 to + 80	- 30 to + 80	- 30 to + 80	- 20 to + 60
	Reflective (Transflective no backlight)		10	23	35	-
	LED backlight		-	35	45	72
	CFL backlight		-	-	-	-
ght	Forward current consumption (mA)		-	40	90	125
	Forward input voltage (V, typ.)		-	3,8	4,1	4,1
	Mode		-	-	-	-
r CFL	Power supply voltage (V)		-	-	-	-
	Current consumption (mA, typ.)		-	-	-	-

DC/DC converter (single power source)

th external temperature compensation circuit

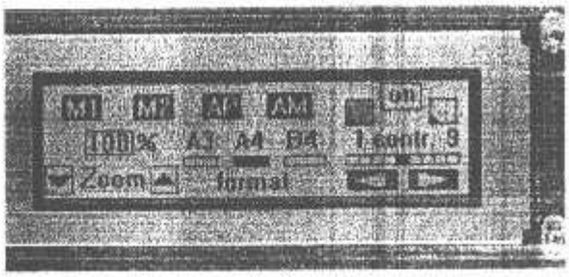
olicy is one of continues improvements we reserve the right to change the specifications of the products in the catalogue without notice.

			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
			G2446	G242C	G321D	G324E	G6490
	Reflective	built-in RAM	-	-	-	-	-
	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp.	built-in RAM	-	-	-	-	-
	Transmissive	-	G2446X5R1A0S	G242CX5R1ACS	G321DX5R1A0S	G324EX5R1ACS	G6490X5R0188
	with CFL backlight	built-in controller	G2446X5R1ACS	G242CX5R1A0S	G321DX5R1ACS	G324EX5R1ACS	-
	Transflective	built-in RAM	-	-	-	-	-
	Reflective (no backlight)		-	-	-	-	-
	LED backlight		-	-	-	-	-
	CFL backlight		91,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	280,0 x 122,0 x 15,7
	area (HxV) mm		134,0 x 41,0	134,0 x 76,0	128,0 x 113,0	128,0 x 110,0	216,0 x 83,0
	(H x V) mm		0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,36
	(H x V) mm		0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,36 x 0,43	0,33 x 0,39
	supply voltage (V)	(VDD - VSS)	+ 5,0	+ 5,0	+ 5,0	+ 5,0	+ 5,0
		(VLC - VSS)	*1	*1	-24,0	-24,0	-24,0
	consumption	IDD	12	30	8	7,5	11
		IDD (built-in controller)	15	40	23	23	-
		ILC	-	-	6	6,5	9
	Driving method (duty)		1/64	1/128	1/200	1/240	1/200
	LSI	Driver	MSM5298 MSM5299 or equivalent	KS0108 KS0104 or equivalent	MSM5298 MSM5299 or equivalent	HD66204 HD66205 or equivalent	MSM5298 MSM5299 or equivalent
		Controller	SED1330F8	SED1330F8	SED1330F8	SED1330F8	-
	ng temperature range (°C)		0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	e temperature range (°C)		- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
		Reflective (Transflective no backlight)	-	-	-	-	-
		LED backlight	-	-	-	-	-
		CFL backlight	200	280	250	360	420
	cklight	Forward current consumption (mA)	-	-	-	-	-
		Forward input voltage (V, typ.)	-	-	-	-	-
		Mode	4800210	4800210	4800210	4800210	4800120
	r for CFL	Power supply voltage (V)	+ 5,0	+ 5,0	+ 5,0	+ 5,0	+ 12,0
		Current consumption (mA, typ.)	250	350	265	365	390

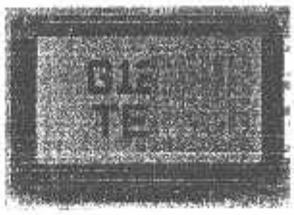
*1 in DC/DC converter (single power source)

*2 with external temperature compensation

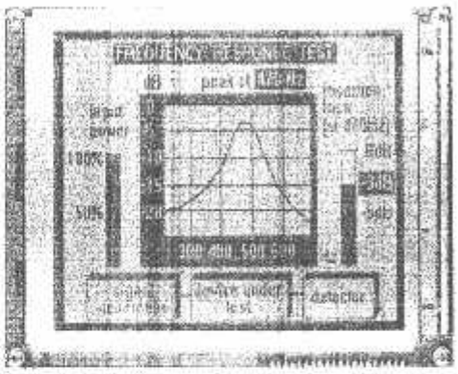
Our policy is one of continuous improvements, we reserve the right to change the specifications of the products in the catalogue without notice



G2446

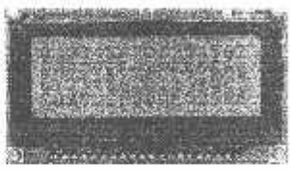


G1226

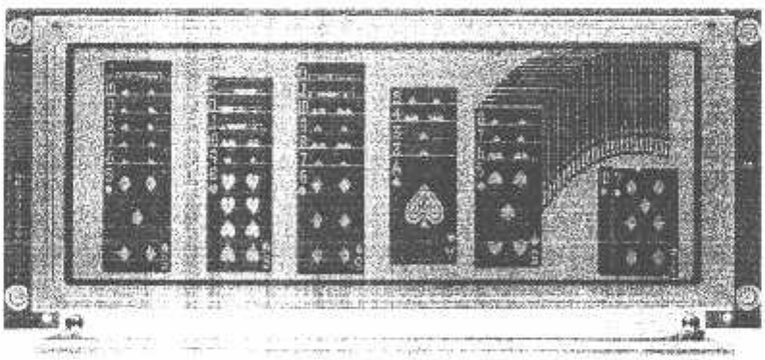


G321D

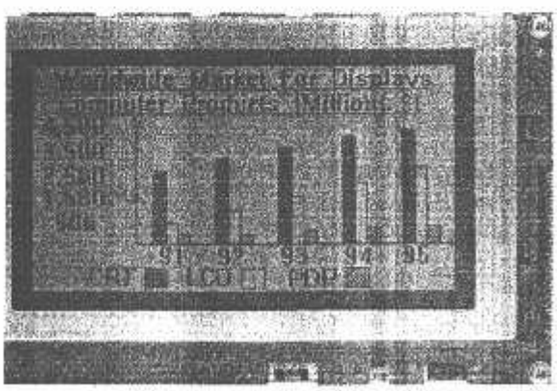
G1216



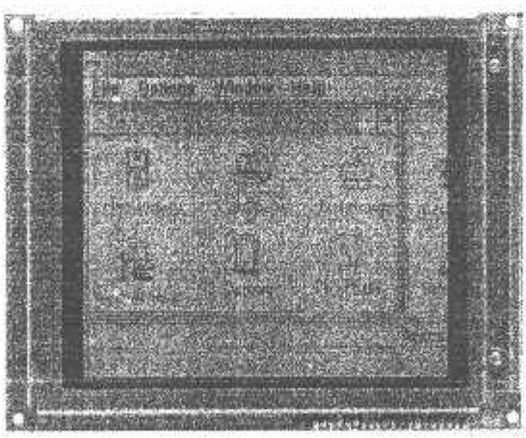
G1213



G649D



G242C



G324E

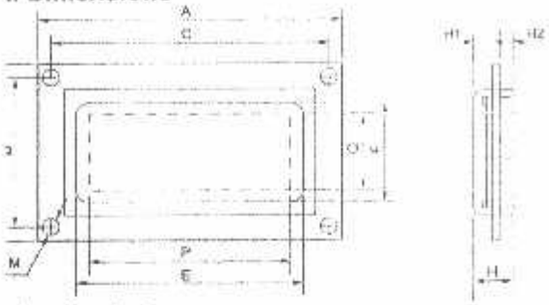
:CK LIST FOR CUSTOM DESIGNED LCD MODULE

npany_____ **2. Application**_____ **3. Customer Specified Part No.**_____

ıign

ew ☐Modified : Manufacturer_____, Part No._____, Remarks _____
quivalent: Manufacturer_____, Part No._____, Remarks _____

ıl Dimensions



A x B : Module size _____ x _____ mm
E x F : Viewing area _____ x _____ mm
P x Q : Active display area _____ x _____ mm
C : Length between mounting holes _____ mm
D : Length between mounting holes _____ mm
M : Diameter of mounting hole _____ mm
H : Total thickness _____ mm
H1 : Upper thickness _____ mm
H2 : Lower thickness _____ mm

play Contents

haracter type:_____characters_____lines
haracter font_____x_____dots + cursor
haracter pitch_____x_____mm
ot pitch_____x_____mm
ot size_____x_____mm
raphics (Full dot) type:_____x_____dots
ot pitch_____x_____mm
ot size_____x_____mm
egment type:_____digits_____lines
thers_____

) Panel

ing angle: ☐6 o'clock ☐12 o'clock☐____o'clock
: ☐TN ☐FSTN (Black and white)
STN (☐Yellow green ☐Gray ☐Blue)
Chromaticity coordinates
(_____ ≦ x ≦ _____ , _____ ≦ y ≦ _____)
Positive type ☐Negative type
Reflective ☐Transflective ☐Transmissive
Others_____
scale: ☐Yes_____gray scale ☐No
erential specifications:
Response time t_{on} ____ms (____°C) t_{off} ____ms (____°C)
Viewing angle____deg. (____°C) ☐Contrast____(____°C)
Others_____
surface finishing:
Normal ☐Anti-glare☐_____
rizer color: ☐Normal (neutral gray) ☐Red
Green ☐Blue ☐_____

ving Method

plexing: 1/_____duty, 1/_____bias
e frequency:_____Hz

driver: ☐Specified ☐Unspecified
egment driver_____(Manufacturer_____)
ommon driver_____(Manufacturer_____)
roller: ☐Internal ☐External
pe No._____(Manufacturer_____)
: ☐Internal ☐External
pe No._____(Manufacturer_____)
: ☐Internal ☐External
pe No. /Memory size_____(Kbit) (Manufacturer_____)

ower Supply

ngle power supply: ☐5V ☐_____V
power supplies
or logic: (V_{DD}-V_{SS}) : ☐5V ☐_____V
or LC drive: (V_{EE}-V_{SS}) : ☐_____V

11. Temperature Compensation Circuit

☐Internal ☐External ☐Unnecessary
Compensation range: ☐0°C to 50°C ☐___°C to ___°C

12. Current Consumption

For logic: typ._____mA, max._____mA
For LC drive: typ._____mA, max._____mA
Others ( ) : typ._____mA, max._____mA

13. Contrast Adjustment

☐Internal ☐External ☐Unnecessary
Method: ☐Temp. compensation circuit ☐Volume ☐____

14. Temperature Range

Operating temperature range: ☐0°C to 50°C☐____°C to____°C
Storage temperature range:☐-20°C to 60°C☐____°C to____°C

15. Input/Output Terminals

Specifying allocation: ☐Yes ☐No
Specifying position: ☐Yes ☐No

16. Weight

typ._____g, max._____g

17. Connector

☐Internal ☐External ☐Unnecessary
Type No._____(Manufacturer_____)

18. Backlight

☐Internal ☐External ☐Unnecessary
☐EL: ☐Green ☐White ☐_____
☐LED: ☐Yellow green ☐Amber ☐_____
☐CFL: ☐White ☐_____
☐Incandescent lamp ☐Others_____
☐Backlight type ☐Edge backlight type
Brightness:_____cd/m²
Inverter:☐Internal ☐External ☐Unnecessary
Power supply voltage_____V
Current consumption (backlight included)_____mA
Brightness control: ☐Yes ☐No

19. Others

_____
_____
_____

20. Schedule

Estimate:_____
Sample: Delivery_____, Quantity:_____pcs
Mass production: Target price:_____
Delivery_____, Total quantity:_____pcs
Quantity per month_____pcs

iid Crystal Displays

CK LIST FOR CUSTOM DESIGNED LCD

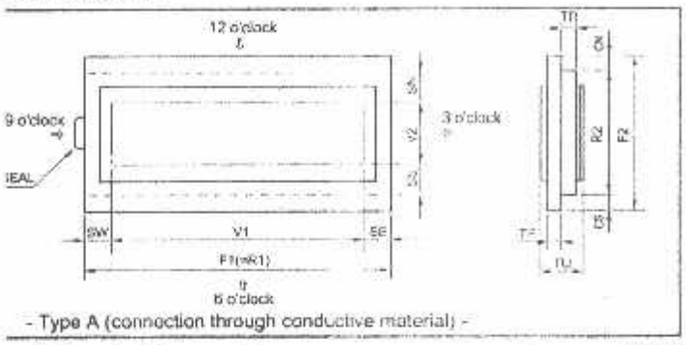
pany_____ **2. Application**_____ **3. Customer Specified Part No.**_____

gn

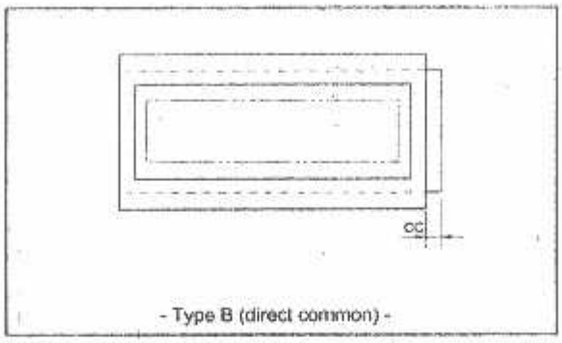
v ☐ Modified: Manufacturer _____ , Part No. _____ , Remarks _____

iivalent: Manufacturer _____ , Part No. _____ , Remarks _____

l Dimensions



- Type A (connection through conductive material) -



- Type B (direct common) -

zontal length of upper glass _____ mm
cal length of upper glass _____ mm
zontal length of lower glass _____ the same as F1
tical length of lower glass _____ mm
generally longer than F2 when terminals are with pin.
*: Thickness of glass _____ mm
dard type: 1.1 mm or 0.7 mm
kness of LCD _____ mm
: ☐ Right ☐ Left ☐ Right or Left

V1 :Horizontal length of viewing area _____ mm
V2 :Vertical length of viewing area _____ mm
CN**: Terminal length _____ mm
CS**:Terminal length _____ mm
**CN or CS=0 in case of one side terminal type.
CC: Terminal length _____ mm
SE,SW,SN,SS : Seal width
(According to design or manufacturing condition:
about 2.0 mm to 4.0 mm)

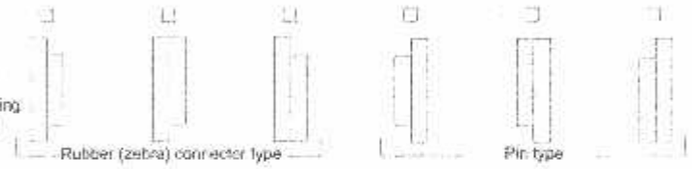
l Form

inal ☐

- Type A - - Type B -

nfering • Drilling

☐ Yes ☐ No ☐ Yes ☐ No



ay Mode

g angle : ☐ 6 o'clock ☐ 12 o'clock ☐ _____ o'clock
☐ TN ☐ FSTN (Black and white)
TN: (☐ Yellow green ☐ Gray ☐ Blue)
romaticity coordinates (____ ≤ x ≤ ____ , ____ ≤ y ≤ ____)
ositive type ☐ Negative type
eflective ☐ Transflective ☐ Transmissive
ential specifications:
esponse time (at ____ °C) ____ ms (at ____ °C)
iewing angle ____ deg. (at ____ °C) ☐ Contrast ____ (at ____ °C)
thers _____

rizer

e finishing: ☐ Normal ☐ Anti-glare ☐ _____
☐ Normal (neutral gray) ☐ Red ☐ Green
☐ Blue ☐ _____
olarizer : ☐ Attached type ☐ Separate type
olarizer : ☐ Attached type ☐ Separate type

ng Method

c ☐ Multiplexing: (1/_____ duty, 1/_____ bias)
ting voltage (V_{OP}) : _____ V
frequency: _____ Hz
g IC: _____ (Manufacturer _____)
nt consumption: _____ μA

10. Temperature Range

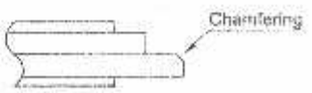
Operating temperature range
☐ With temperature compensation circuit (or volume)
(☐ 0°C to 50°C ☐ _____ °C to _____ °C)
☐ Without temperature compensation circuit
(☐ 0°C to 50°C ☐ _____ °C to _____ °C)
Storage temperature range
(☐ - 20°C to 60°C ☐ _____ °C to _____ °C)

11. Terminal Connecting Method

☐ Rubber connector (Zebra rubber)
☐ Pin: ☐ DIL ☐ SIL ☐ _____
Pitch (☐ 2.54 ☐ _____ mm) Length (_____ mm)
☐ Heat seal: ☐ Equipped ☐ Unnecessary

12. Others

Print (Characters, lines, masks etc.) : ☐ Yes ☐ No
Protective film:
☐ Yes (Color: ☐ Red ☐ Translucent ☐ Transparent) ☐ No
Chamfering (for heat-seal connector) :
☐ Yes (Position: _____)
(Quantity: _____)
☐ No



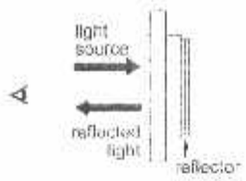
13. Schedule

Estimate : _____
Sample : Delivery _____ , Quantity : _____ pcs
Mass production : Target price : _____
Delivery _____ , Total quantity: _____ pcs
Quantity per month: _____ pcs

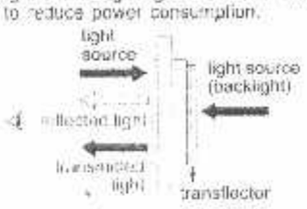
iid Crystal Display Modules

LECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

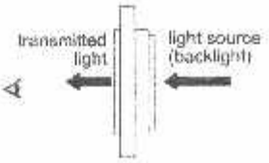
lective LCD
or bonded to the rear polarizer
the incoming ambient light. Low power
nption because no backlight is required.



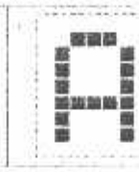
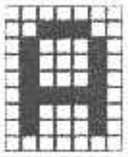
❷ Transflective LCD
Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.



❸ Transmissive LCD
Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image



ITIVE/NEGATIVE MODE

sitive type		Negative type	
		Negative type (inverse image) (when data is inverted)	

YPE/STN TYPE/FSTN TYPE

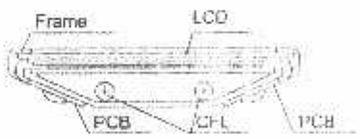
(Background/dot color) Gray/Black	TN (Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch,calculator, etc.)
Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

JCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

(Cold Cathode Fluorescent Lamp) backlight
tures: high brightness, long service life, inverter required

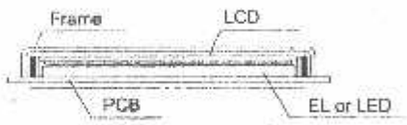
ge backlight type
G2446,G242C)
G321D,G649D)

cklight type



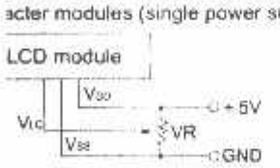
EL (Electroluminescent Lamp) backlight
LED (Light Emitting Diode) backlight

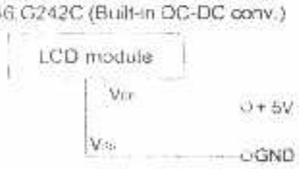
Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

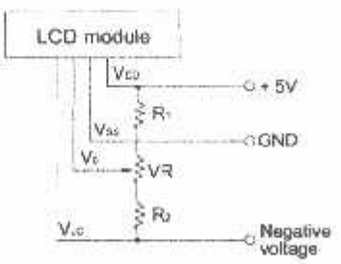


VER SUPPLY

acter modules (single power supply) • G2446,G242C (Built-in DC-DC conv.) • G321D, G324E and G649D

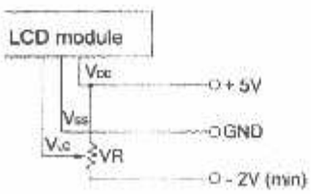


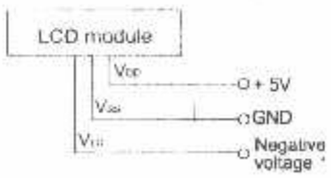




Note 1:Contrast can be adjusted by VR.
Note 2:For module with backlight, power supply for backlight is necessary.

racter Modules(Dual power supply) • Y1206 and G1226





Negative voltage should be variable for contrast adjustment.

cautions

/ Instructions

ɜ LCD panel is damaged, be careful not to get the ɨ crystal in your mouth and not to be injured by hed glasses.

ɹ should swallow the liquid crystal, first, wash your th thoroughly with water, then, drink a lot of water induce vomiting, and then, consult a physician.

ɜ liquid crystal should get in your eye, flush your with running water for at least fifteen minutes.

ɜ liquid crystal touches your skin or clothes, re- e it and wash the affected part of your skin or ıes with soap and running water.

r CFL backlight is driven by a high voltage with an ter. Do not touch the connection part or the wir- ıattern of the inverter.

ıot use inverters without a load or in the short-cir- node.

the LCD module within the rated voltage to pre- overheating and/or damage. Also, take steps to ıre that the connector does not come off.

ing Precautions

e the LCD panel has glass substrate, avoid apply- nechanical shock or pressure on the module. Do lrop, bend, twist or press the module.

ıot soil or damage LCD panel terminals.

e the polarizer is made of easily-scratched mate- ɔe careful not to touch or place objects on the dis- surface.

ɔ the display surface clean. Do not touch it with skin.

)S LSI is used in the LCD module. Be careful of ɔ electricity.

ıot disassemble the module or remove the liquid al panel or the panel frame.

ot damage the film surface of the EL lamp; other- the lamp will be damaged by humidity.

et an EL lamp in an LCD module, push the EL ı with its emitting side up, without pushing the rub- ɔonnectors too hard. If you damage them, the LCD ule may not work properly.

ing and Designing

rotect the polarizer and the LCD panel, cover the ay surface with a transparent plate (e.g., acrylic ass) with a small gap between the transparent plate the display surface.

ɔ the module dry. Avoid condensation to prevent ransparent electrodes from being damaged.

ɜ LCD panel with AC waveform in which DC ele- t is not included to prevent deterioration in the LCD ɜl.

ɹrast of LCD varies depending on the ambient tem- ture. To offer the optimum contrast, LC drive volt- should be adjusted. LCD driven in a high duty must be provided with drive voltage adjustment ıod.

nt a LCD module with the specified mounting part/ s.

- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone)or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is 25°C±10°C and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

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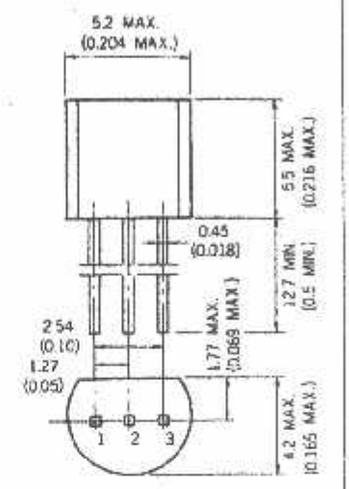
NEC

NPN SILICON TRANSISTOR
2SC945

SCRIPTION The 2SC945 is designed for use in driver stage of AF amplifier and low speed switching.

ATURES
- High Voltage — LV_{CEO} : 50 V MIN.
- Excellent h_{FE} Linearity
  h_{FE1} (0.1 mA)/h_{FE2} (1.0 mA) : 0.92 TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC 43B
JEDEC : TO 92
IEC : PA33

SOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +125 °C
Junction Temperature	+125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation	250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60 V
V_{CEO}	Collector to Emitter Voltage	50 V
V_{EBO}	Emitter to Base Voltage	5.0 V
I_C	Collector Current	100 mA
I_B	Base Current	20 mA

ECTRICAL CHARACTERISTICS (Ta = 25 °C)

YMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
FE1	DC Current Gain	50	135			V_{CE}=6.0 V, I_C=0.1 mA
FE2	DC Current Gain	90	200	600		V_{CE}=6.0 V, I_C=1.0 mA
IF	Noise Figure		0.8	15	dB	V_{CE}=6.0 V, I_C=0.1 mA, R_G=2.0 kΩ, f=1.0 kHz
T	Gain Bandwidth Product	150	250	450	MHz	V_{CE}=6.0 V, I_E=−10 mA
ob	Collector to Base Capacitance		3.0	4.0	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
CBC	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
EBO	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
BE	Base to Emitter Voltage	0.55	0.62	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
CEsat)	Collector Saturation Voltage		0.15	0.3	V	I_C=100 mA, I_B=10 mA
BEsat)	Base Saturation Voltage		0.86	1.0	V	I_C=100 mA, I_B=10 mA

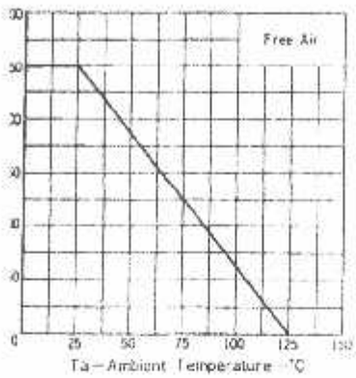
assification of h_{FE2}

Rank	R	O	P	K
Range	90 − 180	135 − 270	200 − 400	300 − 600

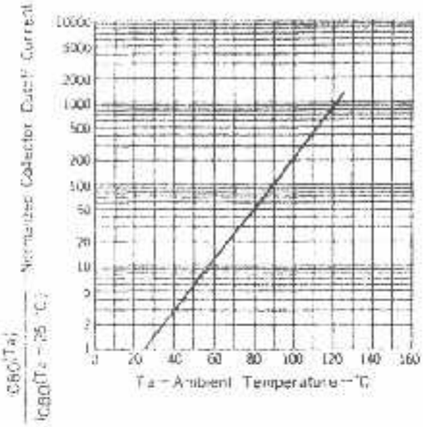
h_{FE2} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

PICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

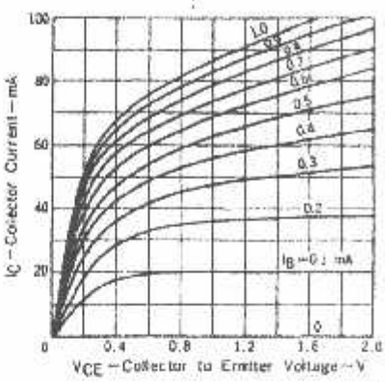
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE

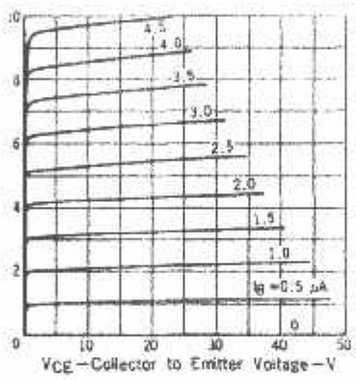


COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE

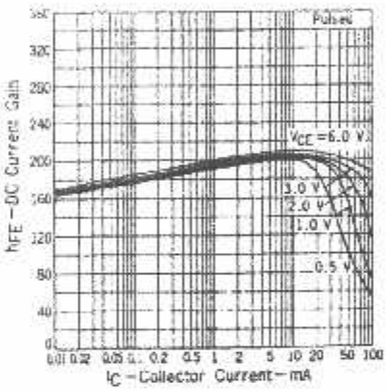


4-3

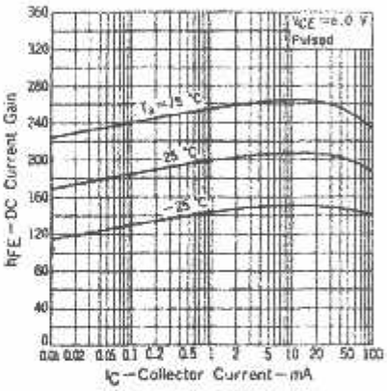
LECTOR CURRENT OLLECTOR TO EMITTER VOLTAGE



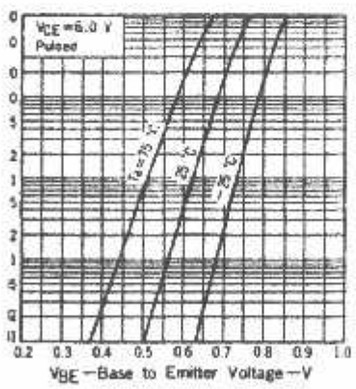
DC CURRENT GAIN vs. COLLECTOR CURRENT



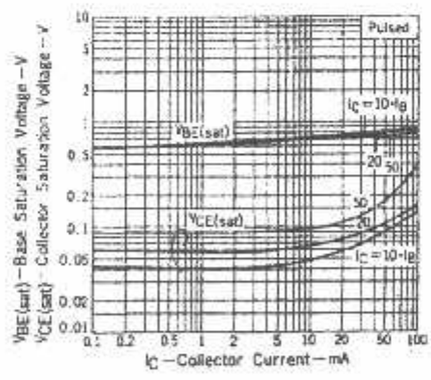
DC CURRENT GAIN vs. COLLECTOR CURRENT



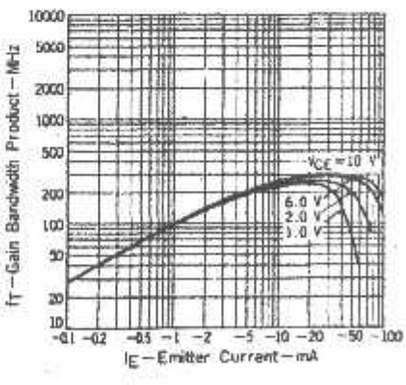
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



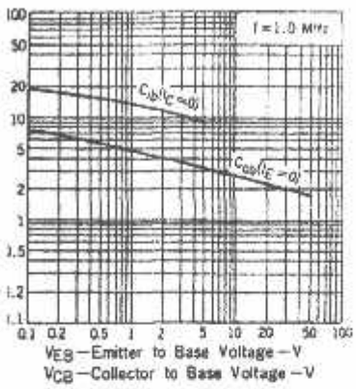
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



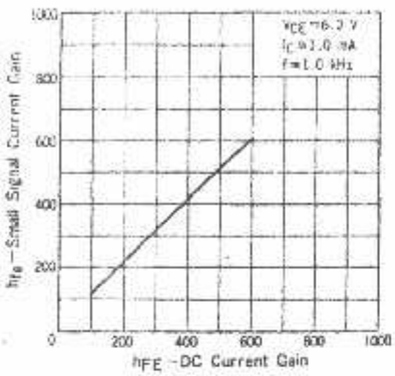
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



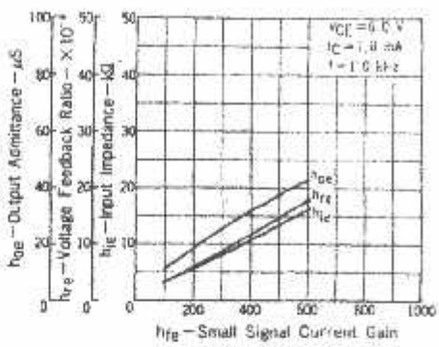
TER TO BASE AND COLLECTOR TO CAPACITANCE vs. REVERSE VOLTAGE



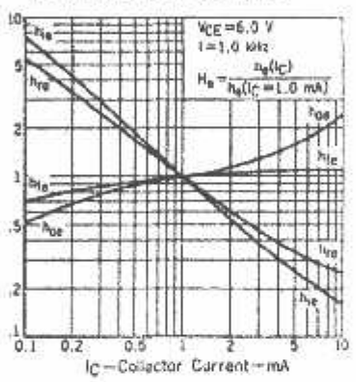
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



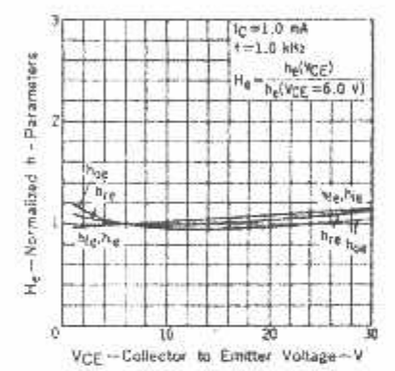
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



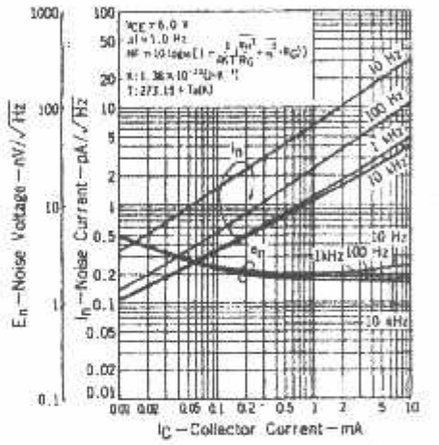
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



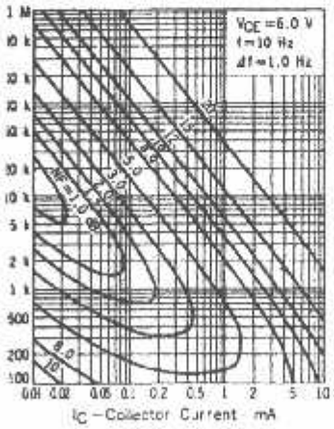
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



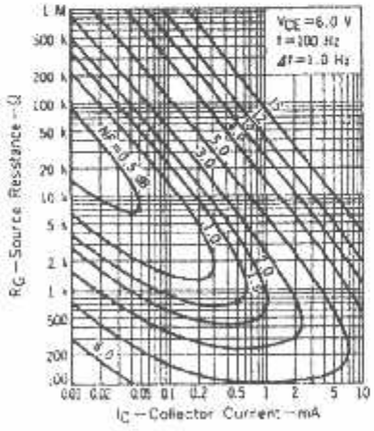
E$_n$ AND I$_n$ vs. COLLECTOR CURRENT



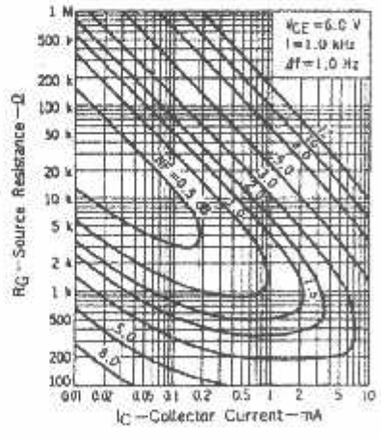
NOISE FIGURE MAP 1



NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



National Semiconductor

June 1989

54LS164/DM54LS164/DM74LS164
8-Bit Serial In/Parallel Out Shift Registers

General Description

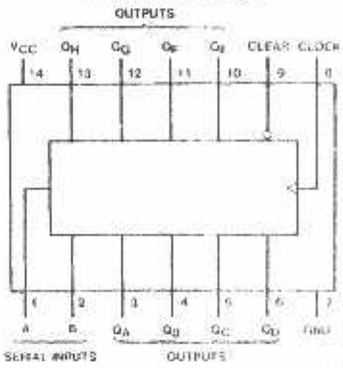
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW
- Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6390–1

Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

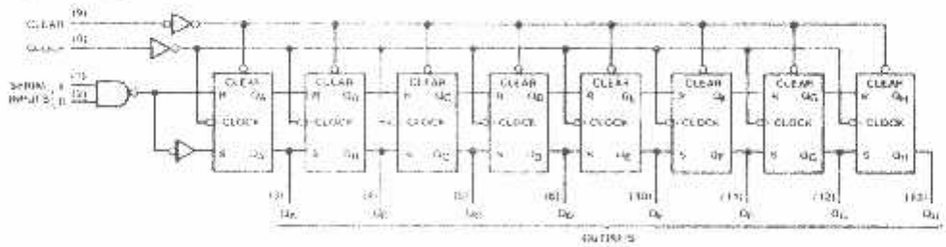
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6390–2

RRD-B30M105/Printed in U.S.A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		17			17			ns
t_H	Data Hold Time (Note 4)		5			5			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

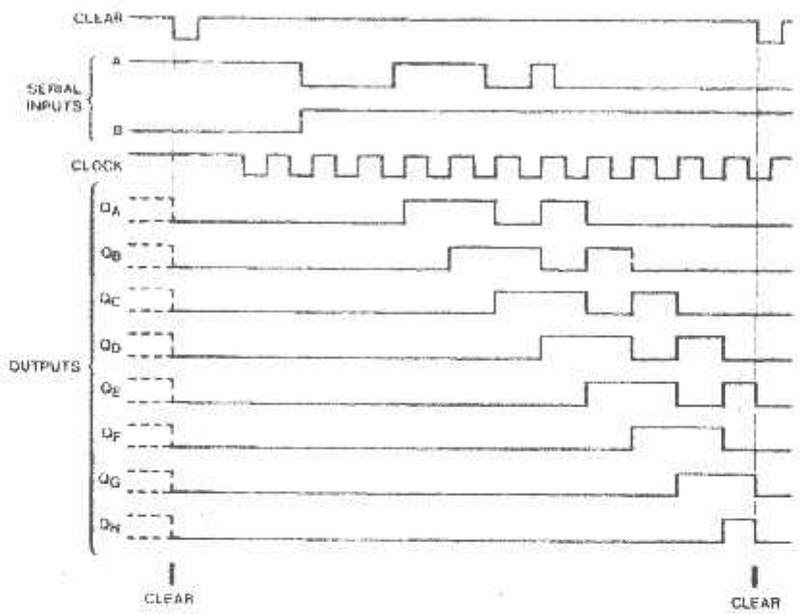
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

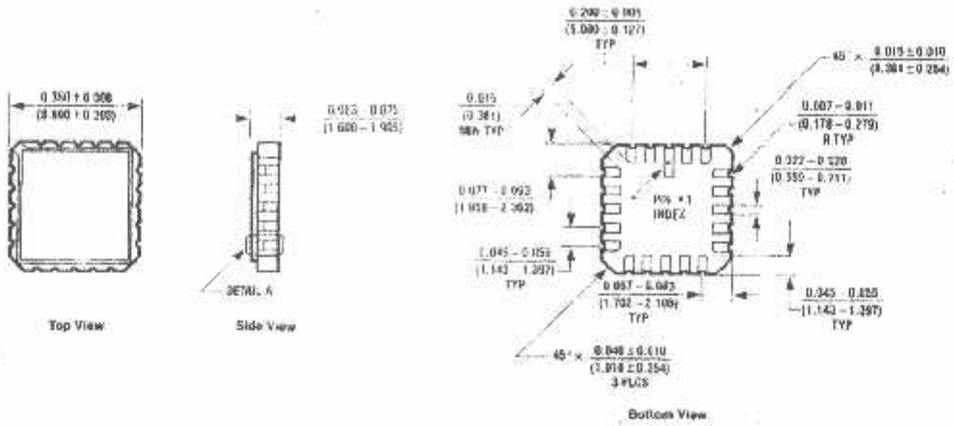
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

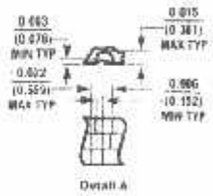
Timing Diagram



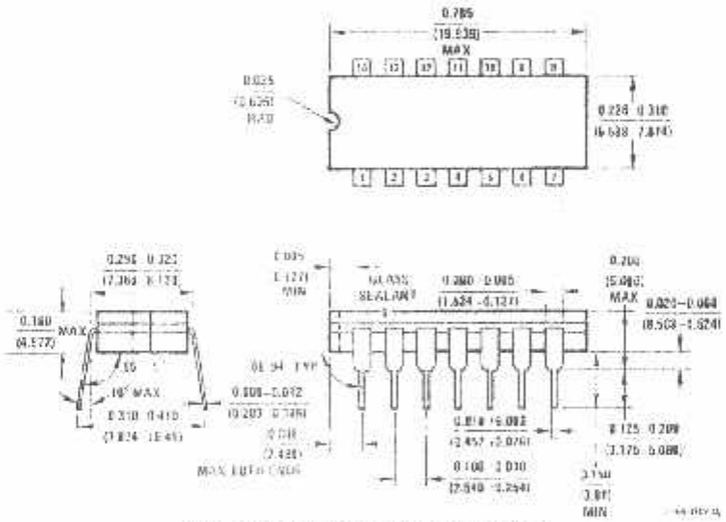
TL/F/6086-9

Physical Dimensions inches (millimeters)



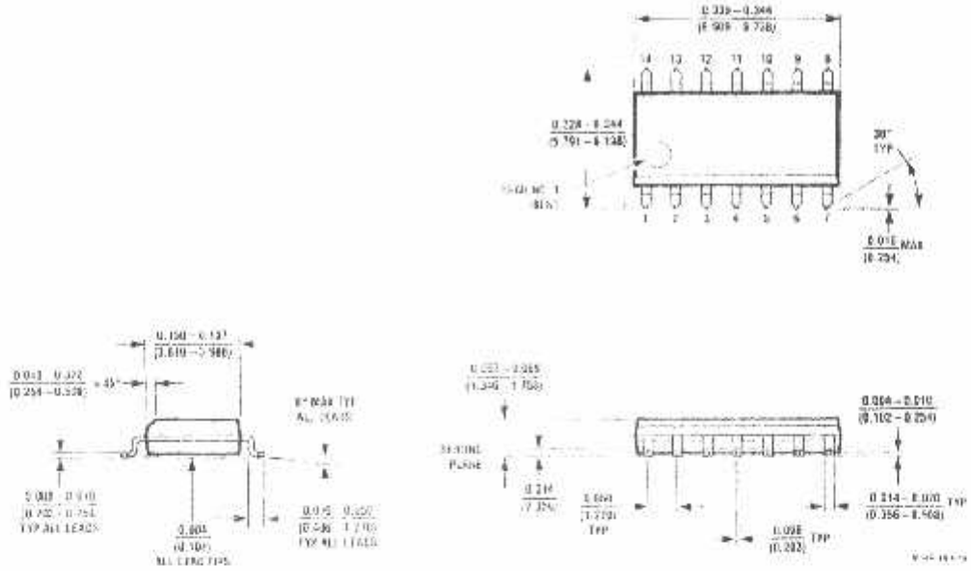


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS164LMQB
NS Package Number E20A

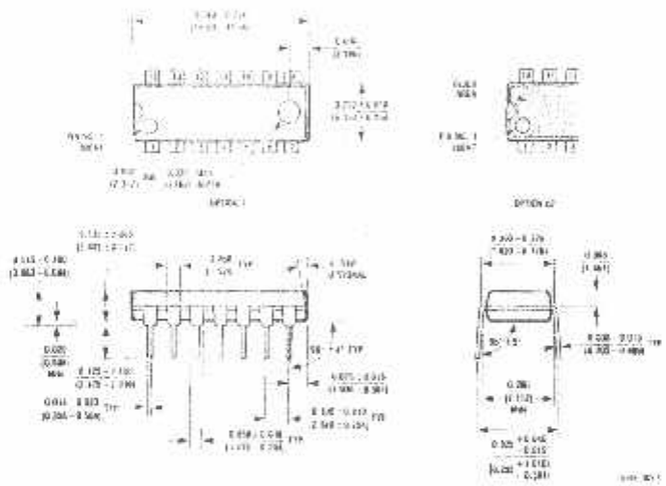


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS164DMQB or DM54LS164J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

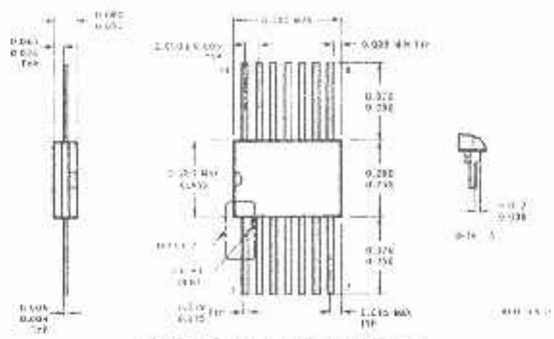


14-Lead Small Outline Molded Package (M)
Order Number DM74LS164M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS164N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS164FMQB or DM54LS164W
NS Package Number W14B

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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