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Real-Time Hardware-In-the-Loop Testing of IEC 61850 GOOSE based Logically Selective Adaptive Protection of AC Microgrid

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ABSTRACT The real-time (RT) hardware-in-the-loop (HIL) simulation-based testing is getting popular for power systems and power electronics applications. The HIL testing provides the interactive environment between the actual power system components like control and protection devices and simulated power system networks including different communication protocols. Therefore, the results of the RT simulation and HIL testing before the actual implementation in the field are generally more acceptable than offline simulations. This paper reviews the HIL testing methods and applications in the recent literature and presents a step-by-step documentation of a new HIL testing setup for a specific case study. The case study evaluates improved version of previously proposed communication-dependent logically selective adaptive protection algorithm of AC microgrids using the real-time HIL testing of IEC 61850 generic object-oriented substation event (GOOSE) protocol. The RT model of AC microgrid including the converter-based distributed energy resources and battery storage along with IEC 61850 GOOSE protocol implementation is created in MATLAB/Simulink and RT-LAB software using OPAL-RT simulator platform. The Ethernet switch acts as IEC 61850 station bus for exchanging GOOSE Boolean signals between the RT target and the actual digital relay. The evaluation of the round-trip delay using the RT simulation has been performed. It is found that the whole process of fault detection, isolation and adaptive setting using Ethernet communication is possible within the standard low voltage ride through curve maintaining the seamless transition to the islanded mode. The signal monitoring inside the relay is suggested to avoid false tripping of the relay.

INDEX TERMS Adaptive Protection, AC Microgrid, Logic Selectivity, IEC 61850 GOOSE, Real-time Simulation, HIL Testing, Converter-based DERs, Battery Storage.

I. INTRODUCTION

Microgrids are the local distribution systems connected with many local distributed energy resources (DERs) and controllable/non-controllable loads with the capability of operating in both the grid-connected and intentional or unintentional islanding modes. The DERs or generators in microgrids include the small-scale variable or non-dispatchable renewable energy sources (VRES) like the wind turbine generators (WTGs) and solar photovoltaic (PV) systems and non-variable or dispatchable RES (NVRES) like mini-hydropower, biomass, geothermal and other combined heat and power (CHP) generators. The VRES usually require some form of energy storage systems (ESS) like battery energy storage systems (BESS), superconducting magnetic energy storage (SMES), supercapacitors (SC), flywheel energy storage systems (FESS) and pumped hydroelectric energy storage (PHES) to smooth out the short, medium and long term operational and weather-related power fluctuations. The ESS including BESS, FESS, and electric vehicles (EVs) may behave like controllable loads when working in the charging mode and as controllable generators when working in the discharging mode. So, depending on the availability of power generation resources measured in terms of the active power generation capability of DERs, the state of charge (SOC) of BESS and EVs and their mode of operation (charging or discharging), the microgrid will behave as a net producer or consumer to the main distribution network in the

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grid-connected operation. However, ideally in the islanded mode of operation the availability of power generation resources including the active and reactive power should be equal to the demand of the local load plus microgrid losses and thus the microgrid should behave as a self-sufficient system [1]-[2]. Microgrids can be AC microgrids, DC microgrids or hybrid AC/DC microgrids but in this paper only utility-scale AC microgrids are considered due to their potential for the large-scale adoption in distribution systems.

The AC microgrid is essentially an aggregated system comprised of many parallel operating complex systems like dispatchable and non-dispatchable DERs, ESSs, controllable and uncontrollable loads, hence its operation, management, control, and protection are equally complex in nature [3]. One of the complexities involved in the AC microgrid is its operation also in the islanded mode with the extensive share of the converter-based DERs. In this paper the term "extensive share" refers to the 100% share of the converter-based DERs. The operation of microgrid in the islanded mode enhances the reliability of the distribution system but requires different adaptive approaches in terms of operation, management, control and protection compared with the grid-connected mode, particularly, when a large number of converter-based DERs are connected in the islanded microgrid. The converter-based DERs on the one hand offer the quick response times and the possibility of controlling system variables like voltage, current, active power and reactive power smoothly, but on the other hand they lack the inertial response and provide the limited fault contribution. This creates challenges for the traditional control and protection equipment to keep the system intact during different operational and contingency events. Therefore, the need is increased to revise the traditional control and protection schemes, adapt them according to new evolving scenarios or put forward the new control and protection schemes to tackle these challenges [4]. For example, the hybrid centralized and decentralized [5] or distributed hierarchical control systems [6]-[7] and adaptive protection schemes using high speed communication links [8]-[11] could be the options to meet new challenges if these schemes are well-designed, prototyped and validated through reliable tests before the actual deployment in the field.

The digital real-time simulations (DRTS) offer the interactive platforms for different complex components of smart grids and microgrids including control, protection and communication devices for testing, validation and prototyping different microgrid design concepts and operations with much reduced costs and risks compared with the fully physical experiments. The real-time (RT) interaction of simulations with individual physical components is not possible with the traditional computer-based offline simulation platforms. Therefore, the popularity of RT simulations has increased in the new era of power system evolution with the increasing penetration levels of DERs connected to transmission and distribution systems. Many designing, testing, prototyping and training studies based on RT simulations are being conducted in the fields of power systems, power electronics, control and communication systems in the broad context of smart grid developments [12]. An overview of RT simulation and testing methods along with the related literature review of the latest studies using RT simulations is presented separately in the next section of this paper.

From the protection point of view, all types of faults inside the microgrid both in the grid-connected and islanded modes should be detected, located, and selectively isolated to prevent the possible damage to the property and equipment without causing supply interruption to the healthy parts of the microgrid [2]. From the control point of view in the grid-connected mode, DERs in microgrid should be operated in a manner to utilize as much renewable energy as locally available and surplus energy should be exported to other parts of the local distribution networks through market participation for net profitability. In the islanded mode of operation, the surplus energy should be stored and the loss of any load or generator due to faults should be equally compensated by generation control/curtailment or load shedding respectively to maintain the voltage and frequency stability of the remaining healthy system inside the microgrid. The microgrid management system (MMS) can achieve power balance through ESS in the primary control level, provide unit commitment and economic dispatch functions through an energy management system (EMS) implemented in the secondary control level and ancillary services to the main grid like voltage and frequency support by tertiary control [3]. A survey of the microgrid EMS is presented in [13] which is based on four categories including non-renewables, ESS, demand side management (DSM) and hybrid systems. The latest literature reviews on microgrid protection and related challenges can be found in [14]-[19].

To ensure the uninterrupted power to the healthy parts of the microgrid, the ESS resources inside the microgrid should be allocated according to the reliability demand of the priority and non-priority load categories and located near the non-dispatchable VRES to avoid the load flow complexities. The larger capacities of ESS equal in capacities to the peak demand of the microgrid loads should, however, be located at the point of common coupling (PCC) so that these could be used as local centralized grid-forming DERs during the islanded mode. For example, in [20] a grid-forming centralized BESS of a minimum 12 MW capacity is selected for a peak load of 31 MW to meet N-1 criterion and replace one diesel generator operation in an islanded power system operating in parallel with another diesel generator of 12 MW and two WTGs of 9 MW and 5.5 MW. The results show that the selected 12 MW capacity of BESS also successfully maintained the stability of the islanded power system. The connection of the peak load capacities of ESS at PCC will provide significant help for the seamless transition of microgrid to the islanded mode. In case of the faults or accidental opening of the main grid breaker, the rest of the microgrid will be able to operate in the islanded mode by the quick connection of the grid-forming converter

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of the centralized ESS or changing its control mode from the normal grid-following mode to the grid-forming mode [21]-[22]. This way a single stronger source compared with the individual DERs in the microgrid although weaker than the main grid, will still provide enough frequency and voltage stability in the islanded mode. Moreover, the fault detection in the islanded mode will be easier with a stronger centralized ESS providing an additional fault current contribution compared with the case when all the individual fault-current-limiting converter-based DERs are operating in the grid-forming mode with no centralized ESS. However, the individual converter-based DERs should also be capable of operating in both the grid-forming and grid-following modes so that the loss of the centralized ESS due to faults, the accidental opening of the breaker or the cyberattack etc. should not result in a complete blackout of the islanded microgrid. Even if the blackout occurs inside the islanded AC microgrid, then with a centralized BESS available, the black start or the transient-free resynchronization to the main grid could easily be facilitated [23]-[26].

TABLE I
CONTROL MODES OF DERS ACCORDING TO SIZE/LOCATION AND OPERATIONAL MODES OF MICROGRID

DER location/size	**DERs control in different operational modes of microgrid**			
	Grid-connected Mode	Transition Mode	Islanded Mode	Isolated Mode
Centralized[1] *ESS/DER*	Grid-following control	Grid-forming control	Grid-forming control	-
Decentralized[2] *DERs*	Grid-following control	Grid-following control	Grid-following control	Grid-forming control

[1]The DER and/or ESS capacity installed at microgrid PCC equal to combined peak load of microgrid.[2]The capacity of individual DER and/or ESS at downstream of microgrid PCC equal to peak load of the vicinity.

The grid-following or grid-forming control modes of the converter-based DERs in the grid-connected mode, transition mode, islanded mode and isolated mode (facility island) should therefore in principle be according to the division shown in Table I. This will ensure the smooth transition from one mode to the other without the loss of voltage and frequency stability as it is evident from the results of this paper. The change of the control mode from the grid-following mode to the grid-forming mode for some or all DERs of the microgrid during the islanded mode operation is recommended in IEEE 1547.4-2011 [27].

In Table I, the grid-connected mode indicates the operation of the microgrid when DERs, ESS and the loads of the microgrid are completely connected to the main grid synchronously and the microgrid is behaving like a net consumer or producer of the active and reactive power at the PCC. In the grid-connected mode, all the centralized as well as the decentralized DERs/ESS should operate with the grid-following control (Table I, column 2).

The transition mode indicates the operation of the microgrid when it is partly connected to the main grid or network during the faults or other events which have resulted in the opening of the grid-side breaker but the breaker at PCC is still closed. In the transition mode, the main grid voltage is not available due to the open circuit condition. Therefore, the centralized DER(s)/ESS at PCC of the microgrid should immediately change to the grid-forming control to provide the reference rotating frequency signal (ωt) for the decentralized DERs/ESS during the transition mode (Table I, column 3). This way the decentralized DER(s)/ESS would not need change their control and keep operating smoothly with the same grid-following control even during the transition mode.

The islanded mode (Table I, column 4) indicates the situation when the breaker at PCC is also opened and the microgrid is completely isolated from the main grid. In the islanded mode, the centralized DER(s)/ESS should continue operation with the grid-forming control and the decentralized DERs/ESS should continue operation with the grid-following control unless the centralized DER(s)/ESS are also disconnected due to faults or other events. In case the centralized DER(s)/ESS are disconnected, then all the decentralized DERs/ESS should immediately change to the grid-forming control to provide the uninterrupted power for the loads in the islanded mode. It is obvious that the loss the centralized DER(s)/ESS would require other control actions like load shedding or power curtailment for maintaining the voltage and frequency stability of the microgrid in the islanded mode.

The isolated mode or facility island according to IEEE 1547.4-2011 (Table I, column 5) refers to the operation of any individual DER/ESS of the declared microgrid facility which is disconnected from the microgrid during the grid-connected or the islanded mode but can fully or partially supply the local load in its immediate vicinity. In the isolated mode, the individual DER/ESS should only operate with the grid-forming control unless it is possible to operate the isolated individual DER and its related ESS with the combined grid-forming and grid-following control. In the combined grid-forming and grid-following control in the isolated mode, the ESS should operate with the grid-forming control while the individual DER should operate in grid-following mode.

The grid-following control mode of DERs is the usual control method in the grid-connected mode operation of the AC microgrids. In the grid-following control mode the voltage (V) and the frequency (f) of the AC microgrid is only controlled by the main grid and the reference rotating frequency signal (ωt) is derived from the measured three-phase grid-side voltage to generate the power of the same frequency as the main grid. A phase-locked loop (PLL) is usually used to extract the rotating frequency signal (ωt) from the measured three-phase grid-side voltage. However, in the islanded, isolated, or even the transition mode after the loss of

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the grid connection, the measured three-phase grid-side voltage is not available. Therefore, DERs need to change their control mode from the normal grid-following mode to the local independent voltage and frequency control mode called the grid-forming control of DERs. The grid-forming and the grid-following control of the BESS inverter for AC microgrid is presented in [28]. An overview of the different methods of the grid-forming inverter control is given in [29]. The droop-free distributed secondary control of the grid-forming and grid-following converters in AC microgrids is proposed in [30].

The grid-following or the grid-forming controls of the converter-based DERs can be changed using the trip signal of the circuit breakers (CBs) and/or the local voltage measurements during the fault. When the operation of microgrid is stabilized after the transition mode, the settings of digital relays or the intelligent electronic devices (IEDs) should also be changed adaptively according to the new operational mode (grid-connected, islanded, or isolated mode) to detect and isolate the possible faults in the future. In this paper, the IEC 61850 generic object-oriented substation event (GOOSE) message containing the data of a Boolean signal representing the fault detection/pickup signal of an overcurrent (OC) relay is used for the estimation of the round-trip communication delay and the tripping status of circuit breaker (CB) at PCC is used both for changing the control mode or activation of the centralized BESS and for changing the active setting group of IEDs for an adaptive protection in AC microgrid. However, the magnitude of the local voltage at the connection points of DERs is used to provide the fault ride through (FRT)/low voltage ride through (LVRT) behavior and fault current contribution during the fault.

This paper provides a comprehensive review of the hardware-in-the-loop (HIL) testing methods and applications in the recent literature and presents a step-by-step documentation of a new HIL testing setup for a specific case study. The presented case study evaluates improved version of the previously proposed communication-dependent logically selective adaptive protection algorithm of AC microgrids [11] using the real-time HIL testing of IEC 61850 GOOSE protocol. It is found that the whole process of fault detection, isolation and adaptive setting using Ethernet communication is possible within the standard 150 ms/250 ms LVRT curve. The results look promising for the dynamic voltage and frequency stability and the seamless transition of the AC microgrid to the islanded mode. The real-time HIL testing also detects the intermittent loss of the Boolean signal data using the GOOSE protocol which could result in false tripping of the protection relay. Therefore, the monitoring of the status 0 of the subscribed Boolean signal inside the protection relay is suggested to improve the security of the relay.

The rest of the paper is organized in a way that Section II presents a comprehensive review on the RT simulation and testing methods, and Section III explains the adaptive protection schemes in the AC microgrids. Section IV presents the methodology and results of the real-time HIL testing of the communication-dependent logically selective adaptive protection using IEC 61850 GOOSE protocol. Section V gives a short discussion on the proposed RT testing and its applications and Section VI gives conclusions.

II. REAL-TIME SIMULATION AND TESTING METHODS

The RT simulators for the electrical networks have evolved from the earlier analog simulators or the transient network analyzers using the physical hardwired components (pi-sections, operational amplifiers etc.) of reduced sizes to the hybrid analog and digital simulators and then to the complete digital simulators using the digital signal processor (DSP) and microprocessor technologies. The first commercially available real-time digital simulator (RTDS) was developed and demonstrated by RTDS Technologies using DSP-based proprietary technology. The development of low-cost readily available multi-core processors and related commercial off-the-shelf (COTS) computer components from Intel Corporation and Advanced Micro Devices (AMD) paved the way for the development of low-cost and easily scalable fully digital standard computer-based RT simulators. The fully digital computer-based RT simulators have been in use since the end of the 1990s for power system analysis, design, testing, planning and operations such as ARENE developed by Electricite de France, NETOMAC developed by Siemens, the general-purpose processor-based RT simulator developed by OPAL-RT Technologies and the dSPACE RT simulation and control. Both the OPAL-RT and the dSPACE RT simulators use MATLAB/Simulink as the main modelling tool for the simulation [31]-[34].

The main difference between the non-RT or offline simulation platforms and the RT simulation platforms is the time required to solve a system of complex equations and produce the output result, called “the execution time” of the simulation. The RT simulators use a fixed-time step, T_s (for example, 50 microsecond (μs)) for the execution of the simulation within the same time frame as in the real-world clock. This means the RT simulator solves the system of equations and gives output after a fixed-time interval, also called step-size of RT simulation and continues to do so at regular equal time intervals. Therefore, the instantaneous continuous output voltage and current waveforms are produced at discrete time intervals. Hence, RT simulators are inherently the discrete time electromagnetic transient (EMT) simulators using only the fixed-step solvers. The resolution of the voltage and current waveforms, the accuracy of the results and the speed of RT simulation is greatly dependent on the selection of step-size. The smaller the step-size, the better the resolution and accuracy, however slower the simulation speed if the number of processors is small and the number of components is large in the RT simulation model. The simulation speed at the small step-size can only be increased with the additional number of processors. If the execution time of the RT simulation is shorter or equal to the selected step-

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size, the simulation is considered as the real-time and if the execution time is greater than the step-size for one or more time-steps then overruns will occur, and simulation is considered as the non-RT or offline. In case of overruns during RT simulation, either step-size should be increased, or the system model should be simplified to run the simulation in real-time without overruns. The typical step-size in RT simulators is in the range of 20-100 µs, however by using dedicated field-programmable gate array (FPGA) a step-size of as low as 1 µs can be achieved [32][35].

A. CLASSIFICATION OF THE DIGITAL REAL-TIME SIMULATION

The DRTS can be classified into main two categories based on the simulation setup and field specific applications: 1) fully digital real-time simulation, and 2) hardware-in-the-loop or HIL simulation. A fully DRTS is the category of simulation in which the entire system including control, protection and other auxiliary devices are modelled inside the simulator and no external devices or inputs/outputs (I/Os) are involved in any case. The model-in-the-loop (MIL), software-in-the-loop (SIL) or processor-in-the-loop (PIL) are considered as the fully digital RT simulation types. The HIL simulation is the type of DRTS in which a part or some parts of the fully DRTS are replaced with physical components like protection relays, converters, controllers etc. In the HIL simulation the device or the hardware-under-test (HUT) is connected to the RT simulator via input/output interfaces like filters, digital-to-analog (DA) and analog-to-digital (AD) converters, signal conditioning devices (power amplifiers and sensors etc.) or communication links. The limited RT simulation controls can be executed with HIL simulations with user-defined inputs like closing and opening of the switches for the connection and disconnection of the components inside the simulated power system [31].

If the HIL simulation employs the external control hardware that interacts with the virtual simulated power system, then the simulation is called the controller hardware-in-the-loop (CHIL) simulation. The CHIL simulation is usually used for rapid controller prototyping (RCP) or testing of a newly developed or designed controllers. In the CHIL simulation, the external controller gets the feedback signals from the RT simulator, processes these feedback signals to generate the required outputs and then sends back these outputs to the simulated system inside the RT simulator. In the CHIL simulation no real power exchange happens to or from the HUT but only the control signals are exchanged. However, if the HUT in the HIL simulation is an actual power source or a sink that can generate or absorb electric power and it is interfaced to the RT simulator using the power amplifiers, then this type of HIL setup is called power hardware-in-the-loop (PHIL) simulation. In the PHIL simulation, the reference signals are generated based on the solution of the virtual simulated system, scaled down inside the model and sent to the power amplifier which produces the appropriate voltages and currents to be applied to the power HUT. In the same way, the feedback signals of the measured voltages and currents from the power HUT are appropriately scaled and sent back to the RT simulator via power amplifiers or sensors for a complete simulation loop [31].

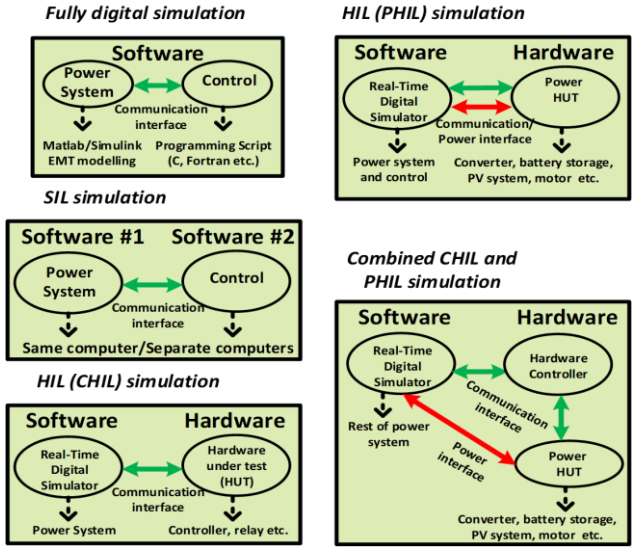

FIGURE 1. The generalized categories of digital real-time simulations for power system testing [36].

The HIL testing of protection relays does not fall under the category of the PHIL simulation even if the voltage and current amplifiers are used for sensing the actual voltages and currents in relay testing because the protection relays as the HUT do not generate or consume power. The HIL testing of electrical machines, DERs, power electronics converters (EVs and charging equipment etc.), fault current limiters (FCLs) etc. fall under the PHIL simulation category [31]. Whereas the HIL testing of the DER controllers, power electronic converter controllers, phasor measurement units (PMUs), protection relays etc. is considered as the CHIL simulation [36].

In the SIL testing, the basic concern is the compatibility of the power and control simulation software platforms with different communication interface protocols used between them in addition to the synchronization and initial condition mismatch problem. In the CHIL testing, the operating voltage mismatches of analog and digital ports, the noise and delay in the transmitted signal as well as packet loss of the data are the potential challenges. In the PHIL testing, the basic challenge is the use of power amplifiers between the RT simulator and the HUT for voltage scaling and feeding back current to the simulator via an analog port thus forming a closed-loop system. In the PHIL testing, the loss of stability may damage the equipment and in order to achieve stability the accuracy of testing may be compromised. Therefore, fine-tuning is necessary in the PHIL testing to achieve the acceptable level of accuracy without the loss of stability [37]. Fig. 1 presents the generalized categories of the real-time digital simulation used for power system testing.

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More recently, the idea of the PHIL simulation which is limited for testing only single devices has been extended for testing the whole microgrids or distribution systems and a new term of Power System-in-the-loop (PSIL) is introduced. The PSIL testing offers the future perspective of hybrid experiments involving power hardware, power network configurations and control hardware and software (combined CHIL and PHIL simulations) but with the increased level of complexity and challenges. These challenges include the complexity of implementing RT compliant interfaces between different components and domains like RT simulations, controllers, electrical components, SCADA (supervisory control and data acquisition) system, etc. Additionally, the issues like communication latency and interface stability need to be assessed properly for ensuring the safety of equipment and the users. The PSIL testing concept can also be adopted for the remote connections of laboratories for the research, development and training purposes [36]. The details of the cyber-physical energy system (CPES) level testing and the validation approach of the European research infrastructure ERIGrid project for a holistic approach of the smart grid can be found in [38]. The fundamentals of joint PHIL and co-simulation experiments for the holistic validation of CPES, related architecture, main challenges and potential solutions are discussed in [39].

B. REVIEW OF TESTING APPLICATIONS OF RT SIMULATIONS

The applications of RT simulators can be classified into four high-level categories: functional applications, field specific applications, simulation fidelity-based applications and Multiphysics applications. The functional applications of RT simulators include designing, RCP, testing, teaching and training etc. The field specific applications of RT simulators may include but not limited to power systems, power electronics and control systems. The simulation fidelity-based applications of RT simulators include EMT simulations, phasor simulations and hybrid phasor and EMT simulations. Whereas the Multiphysics applications of RT simulators include thermoelectric, electromechanical, power systems with integrated communication and gas networks etc. [32].

Mainly, there are two types of power disturbances or transients which need to be simulated in power systems: electromagnetic transients or EMTs and electromechanical transients. The EMTs are very fast occurring disturbances in the time range of µs to milliseconds (ms). The EMTs may happen due to sudden modifications in power system configurations like the opening and closing of the CBs or power electronics switches during the faults or equipment failures. The study and analysis of EMT phenomena require the accurate modelling of power system components such as lines, transformers, protection devices and power electronic converters. However, some components of power systems like turbines and generators etc. may have comparatively slower response time and hence longer time constants than the aforementioned components. Hence, it is usually preferred to use the simplified models of the power plant equipment in EMT simulations if the effect of slower disturbances is not relevant to the study.

The electromechanical transients are comparatively slower than the EMTs happening in the time range of milliseconds to seconds. Usually, the oscillations of rotating machines produced by the mismatch of power generation and consumption are related to electromechanical transients. The electromechanical simulations, also called the stability simulations, utilize the quasi-steady-state phasor technique for modelling the power system components, however, the phasors are allowed to vary in order to produce the dynamic response related with rotating machines. In phasor type of simulations, the EMTs are filtered out, hence the mathematical models in phasor simulations are simplified or averaged versions of EMT models. Due to the simplified models, large time-steps in the range of 10-20 ms can be used in phasor simulations and therefore large power system networks can be simulated with normal single-processor computers at relatively higher speed than in the EMT simulations. However, the phasor simulation produces solutions at one particular frequency, usually the fundamental frequency of the common power system (50 or 60 Hz) and only computes RMS (root-mean-square) values of voltages and currents. Some of the commercially available offline EMT simulation software include EMTP (EMT Program), EMTP-RV, PSCAD (Power System Computer Aided Design), MATLAB/Simulink (discrete) etc. and real-time EMT simulation software include eMEGASIM and HYPERSIM by OPAL-RT etc. Some of the popular commercially available software for offline phasor simulations include EUROSTAG, PSS/E (Power System Simulation for Engineering), CYME (Industrial and Transmission Network Analysis), ETAP (Electrical Transient and Analysis Program), MATLAB/Simulink (phasor) etc., and for real-time interactive phasor simulations ePHASORSIM software offered by OPAL-RT [35][40].

The use of RT simulations for the analysis of electromechanical transients in phasor domain is not common in scientific research except in dispatcher training simulators [41]. The hybrid or co-simulation of EMT and phasor type RT simulations may be of interest for large transmission and distribution system operators with many DERs for the interactive and interdependent type of studies. Due to the lack of computational ability to perform RT simulations of large-scale power systems in the pure EMT domain only a small part of interest can be modelled in EMT for the HIL testing and the remainder of the power system is modelled in phasor domain. However, the hybrid simulations have the main challenges of using the EMT-to-phasor and phasor-to-EMT converters between two different types of simulations for updating the equivalent circuits in both domains of the hybrid simulation and exchanging the data that should be error-free. Due to the operation of EMT and phasor simulations with different simulation time-steps such as 50 µs and 10 milliseconds,

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respectively, large errors may happen in case of fast transients in EMT domain. The accuracy of hybrid EMT and phasor type of RT simulations can be at acceptable level in most cases of only AC systems but not for the hybrid AC/DC power systems. For those, additional techniques are required for accuracy improvement [32][35]. Various case studies of co-simulation of EMT and phasor models are presented in [42]. In this paper, only the fixed-step EMT type of RT simulations are used and discussed for performing the HIL testing of protection relays in the following sections. A brief literature review of recent microgrid and smart grid studies conducted with the help of RT simulations is presented in this section to present the big picture and latest trends in this regard.

A combined CHIL and PHIL simulation for the testing of smart grid control algorithms has been proposed in [37]. In this regard, a four-stage testing chain of the smart grid control algorithm (SGCA) is suggested before the field implementation. These four stages include pure software simulation (offline simulation), SIL testing, CHIL testing and the combined CHIL and PHIL testing. The interface options and the challenges of SIL, CHIL, PHIL and combined CHIL and PHIL tests are also discussed. The combined CHIL and PHIL simulation is applied to a case study of an optimal centralized coordinated voltage control (CVC). The CVC control algorithm manages all direct voltage control devices including on-load tap changer (OLTC), as well as power injection sources like BESS and PV. The CVC algorithm includes two SOC based BESS management techniques. One technique ensures that the BESS is not discharged beyond the minimum 40 % SOC and not charged beyond the maximum 100 % SOC limit by setting active power constraint to zero depending on the estimated bus voltage limit in a scenario without voltage control. The BESS is only allowed to charge when the estimated maximum voltage is higher than 1.05 per unit (p.u.) and only allowed to discharge when the estimated minimum voltage is less than 0.95 p.u. The second technique is used to restore the SOC to the predefined level during the night-time when the demand is low and PV generation is zero. The testing is done using a modified benchmark low-voltage (LV) microgrid presented in [43] assuming a three-phase balanced network.

The CHIL simulation for peak shaving and optimized voltage control using a centralized control scheme and BESS has been presented in [44]. In the same paper PHIL simulation is also presented using a single-phase hardware PV inverter along with PV simulator as HUT. The hardware PV system is connected through a linear power amplifier, current sensor and AD/DA converters to one bus of the simulated single-phase version of CIGRE LV benchmark network with four PV systems modelled as active power-reactive power (P-Q) sources and a BESS. The modelled PV systems and the hardware PV system use the standard f/P and V/Q droops to provide the voltage and frequency support. The results for the voltage control during the high solar irradiation and reduced load with and without using V/Q droops of PV systems and P-Q production/consumption behavior of the hardware PV inverter have been produced for the grid-connected operation. For the islanded mode, the active power curtailment and f/P droops of hardware and simulated PV systems along with the use of BESS as active power storage are used to control the frequency within acceptable limits.

The development and validation case study of a system-integrated smart PV inverter has been presented in [45]. The case study demonstrated comprises three stages of testing including SIL and CHIL testing, PHIL testing and the cyber-physical PHIL testing with communication network co-simulation. The SIL testing is performed using MATLAB/Simulink models of the power system, the power electronics converter and its two-level controller, while the high-level controller and its communication interface is implemented using IEC 61499 and the framework for industrial automation and control (4DIAC) based simulation model. For the CHIL testing the real-time models of the power system and PV inverter have been simulated using the Typhoon HIL RT simulator and the smart inverter controller is embedded onto a physical DSP. The PHIL testing is performed using physical hardware comprised of a three-phase PV inverter of 500 kVA rating as HUT which is interfaced to 194 kW PV emulator via the DC bus and to the grid emulator of 1 MVA via the AC bus. The physical hardware is interfaced to the OPAL-RT simulator using AD and DA converters interface. More than a hundred intentional islanding test runs were performed at different operational parameters using the PHIL setup. The cyber-physical PHIL testing with communication network co-simulation architecture consists of three parts: 1) the residential scale microgrid power hardware including BESS with a 4-kVA inverter, PV emulator with 6-kVA inverter, 45-kVA power amplifier, two power meters, microgrid controller and AC loads, 2) the grid model simulated on OPAL-RT simulator interfaced with microgrid setup via AD/DA converter and power amplifier, and 3) the RT communication network model simulated on OMNET++ software package interfaced to the microgrid controller, the PV inverter and meters via a standard Ethernet connection. Several tests for different load profiles and microgrid configurations have been performed for the observation of the effects of channel and router delays on the controller and the PHIL distribution network model.

The CHIL testing framework for the validation of microgrid ancillary services is presented in [46] for the verification of the control algorithm and its further improvement. The issues of real-time simulation related to modelling, circuit partitioning and multi-rate design are also discussed in this paper. The advantages of the CHIL testing particularly for the grid-compliance testing of generators and network voltage stability studies have been discussed in [47]. This paper indicates that the accuracy of the CHIL testing results is very high and it can be further increased by in-depth modelling of power electronics circuitry to get results identical to the hardware laboratory test results. In this way, the CHIL testing has the

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potential to be considered as a requirement for future standardization procedures.

The HIL co-simulation setup for the RT simulation of the smart grid including the communication network is presented in [48] for testing the coordination between the breakers during a three-phase line fault and the resulting behavior of microgrid after the fault clearance. The test setup consists of two RT simulator platforms, one of these platforms consists of software add on called Simulink desktop real-time (SLDRT) kernel running externally in the Intel processor of the computer out of Simulink to generate C-code. The other platform consists of National Instruments NI cRIO FPGA hardware which includes a real-time processor and a reconfigurable FPGA. These two simulator platforms are connected and synchronized with each other over Ethernet network using UDP (User Datagram Protocol) protocol. The microgrid model used for RT simulation is divided into DC and AC systems. The DC system consisting of 100 kW PV array and a boost converter is simulated on cRIO FPGA platform. The AC system consisting of 250 kVA, 400 V hydraulic turbine-based synchronous generator, transformer, voltage source inverter, CBs, loads, controllers for voltage, current and frequency regulation, and the communication between CBs for the coordination is simulated on SLDRT platform. The test setup also includes physical low voltage CB trip units coordinated using IEC 61850 communication protocols and driven by the voltage and current signals of the AC system via the FPGA interface. The setup is able to measure the delays of 31-36 ms due to communication and internal processing of the real devices (relays and CBs). The similar co-simulation setup is also used in [49] for a case study of frequency control of a synchronous generator and PV system microgrid during the reduction in irradiation level of PV system and a load increase at the connection point.

The HIL testing for the control of a battery-less microgrid consisting of a diesel-driven synchronous generator and PV system is presented in [50]. The primary control of the microgrid related to the PV curtailment of the active power based on droop control for the frequency control and meeting the minimum load ratio of the diesel generator is tested using pure digital RT simulation with RTDS simulator. For testing the secondary control algorithm of the microgrid, a combined CHIL and PHIL setup has been used. The combined CHIL and PHIL simulations have been used to validate two different control approaches, one approach uses hardware controllable loads for the demand response and the other approach uses the active power curtailment of a hardware PV inverter. The combination of these two approaches gives promising results for the control of a diesel generator and PV based microgrid.

The HIL testing platform consisting of three voltage source converters (VSCs), one dSPACE control card, one DC network cabinet, three grid simulators and two RTDS cubicles is presented in [51] for the hybrid AC and DC systems interaction studies. The testing setup can be used for the small and large disturbance studies, testing and validation of ancillary services, grid synchronization, power quality assessment and power system protection. Two case studies one for the subsynchronous resonance damping and the other for the fast frequency support have been demonstrated using the HIL setup.

The details about the application of HIL simulation for the upgradation of the protective relays or IEDs in a large industrial facility are discussed in [52]. The investment of the cost and time in HIL testing technology provided the net saving and increased overall value in terms of many benefits in the development, testing, training and execution of the IEDs upgradation project. The use of RT simulations not only reduced the number of electrical tests and functional operations during the field commissioning but also alleviated the need of hiring the external consultants for the completion of other plant engineering. The HIL simulation of a hybrid smart inverter consisting of two unidirectional boost converters (one for each of two PV inputs), a bidirectional interleaved DC-DC boost converter for BESS input and a bidirectional H-bridge inverter interfacing controllable load and the utility grid is presented in [53]. The proposed HIL test setup consists of three parts: 1) Typhoon HIL 602+ for modelling sources, loads and hybrid power hardware, 2) the self-made interface board consisting of the signal conditioning circuit, power buses and communication transceivers, 3) the digital signal controller development kit from Texas Instruments consisting of processors, firmware and auxiliary hardware. With this setup of power electronics implemented in Typhoon HIL both the hardware topology and microcontroller unit including the firmware have been tested and improved at different operating scenarios. The HIL testing setup is suggested to make the development process faster than the offline simulations.

The CHIL simulation of a multi-functional inverter operating in AC microgrid has been presented in [54] using RTDS simulator for the inverter and the AC microgrid modelling and dSPACE hardware for the control implementation. The RTDS simulator and the dSPACE hardware are communicating through optically isolated I/O interface cards. The current and voltage measurements are taken from the RTDS simulator by the Giga-Transceiver Analog Output (GTAO) card of RTDS Technologies and sent to the dSPACE hardware for the realization of the control logic. The generated control signals from the dSPACE hardware are then taken by the Giga-Transceiver Analog Input (GTAI) card of RTDS Technologies for feedback to the RTDS simulator. The AC microgrid test model implemented in RTDS simulator includes the PV system with a DC-DC boost converter and BESS with a bidirectional DC-DC converter both connected at a common DC-link capacitor at input of a multi-functional DC-AC converter (inverter) that is connected to the main electric grid through an RLC-filter. The CHIL simulation based validation of the ancillary functionalities of the inverter included the active filtration of harmonic currents generated from the non-linear loads in the grid-connected

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mode without using PV and BESS, the control of voltage and frequency at the point of connection during the time of islanding (transition mode) acting as a virtual synchronous machine with PV and BESS in operation and the power management of AC microgrid by the power flow control of BESS according to the demand and power generation of the PV system.

The PHIL test-bench has been developed in [55] to simulate a LV distribution grid to test the dynamic behavior of the power components and find the inaccuracies affecting the smooth operation. The hybrid EMT and phasor co-simulation method has been used for the PHIL setup. The hybrid co-simulation model is developed using MATLAB/Simulink software platform. The model is executed in real-time using a Speedgoat RT target machine with multi-core processors. The power HUT used for the PHIL test-bench consists of a 30 kVA switched-mode current-controlled power amplifier with 5 kHz bandwidth that can be used either as a load or a source depending on its settings. The problems associated with the use of the power amplifier as a power HUT are highlighted including a small phase difference between the reference and actual generated voltage signals due to RT computation and power amplifier time delays, the noise in the reference signal generated by RT simulator due to higher EMT simulation time-step (100 μs) and the distortion of the connection point voltage in the simulated grid due to reactive power export from the power amplifier because of its parasitic capacitance.

The applications of PHIL simulation for laboratory education and understanding the important topics of power system operations including the increased integration of DERs, power sharing between synchronous generators and DERs, voltage control with OLTC and DERs, short circuits with inverter-based DERs and microgrid operation have been discussed in [56]. The positive feedback from students about the use the PHIL simulation for hands-on laboratory exercises and diploma dissertations is also discussed.

The multi-site framework for the RT co-simulation of transmission and distribution systems and the architecture of virtual integration of digital RT simulator laboratories located at four sites in three different countries across Europe connected via pan-European data networks (public Internet) is presented in [57]. The presented framework includes an interface based on a web browser which allows third parties access to the joint experiments. The interface algorithm (IA) used for the study represents the interface quantities in the form of dynamic phasors (DPs) and the time delay compensation between RT simulators is done via phase shift enabling the satisfactory simulation fidelity for the slow transients (voltage and frequency variations). Two kinds of interfaces are required for the presented virtual interconnected laboratories for large systems simulation/emulation (VILLAS) architecture: lab-to-lab interface and lab-to-cloud interface. The lab-to-lab interface at each laboratory manages data exchange between the local and remote simulators and acts as a gateway of communication. The lab-to-lab interfaces exchange time-sensitive simulation data between simulation subsystems, hence a reliable and deterministic communication between lab-to-lab interfaces is the basic requirement for RT co-simulation. The lab-to-lab interface performs the functions such as dropping reordered and duplicated packets, the buffering of packets for the elimination of delay variation, the adjustment of the sent and the received data rates of simulators, the collection of communication statistics and the addition of time stamps to data packets etc. The data exchange between the lab-to-lab interfaces is done using the UDP protocol due to its lower delay variation compared with the TCP (Transmission Control Protocol), hence preferred for the RT applications. The lab-to-cloud interface manages the data exchange between the laboratory and the cloud platform for the on-demand services including the remote access, user interactions during experiments, post processing of simulation results or setting tunable simulation parameters. The most commonly used IA for the PHIL simulations called the ideal transformer model is used for the co-simulation. The setup uses the time-domain (TD) inside the simulators for EMT simulations and the dynamic phasor (DP) domain for the co-simulation algorithm and data exchange.

The idea presented in [36] is further advanced to establish a global RT Superlab across Europe and the United States (U.S.) by connecting eight laboratories with ten digital RT simulators from three major vendors (OPAL-RT, RTDS and Typhoon HIL) [58]. Another setup of the remote connections of RT simulators located in the laboratories of the U.S. and Australia for performing the geographically-dispersed PHIL co-simulation studies is presented in [59]. The connection of the remote labs is done using a centralized entity in the form of a web application called the simulation whiteboard which can be accessed using web protocols on the standard web ports from anywhere on the internet. In addition to providing the remote interconnections and acting as a watchdog, the simulation whiteboard also performs other functions like simulation coordination, time synchronization and data logging. The communication between each laboratory and the simulation whiteboard is done using the hypertext transfer protocol over secure socket level (SSL) (HTTPS) on standard web port 443. A case study of smoothing the combined output of PV/battery inverter and PV-only inverter under intermittent solar irradiation is investigated using coordinated control. The co-simulation setup is such that the PV/battery inverter, the PV controller and the co-simulated network are physically located in the U.S. meanwhile the PV-only inverter is located in Australia. The power network models are implemented using the GRIDLAB-D software and the PV controller algorithm is implemented in Simulink for this case study.

An analytical approach for the mitigation of communication delays in multiple remotely connected HIL testing experiments has been proposed in [60]. The proposed method includes the procedure of the observer delay compensation approach for the communication delay compensation along with the required computational and communication

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architecture. The suggested method is validated using the HIL testing between two remotely connected laboratories each having an OPAL-RT simulator separated by a distance of 115 km with a sample mean communication delay of 30 ms per round trip. The digital and analog I/O channels are used for the exchange of measurements and observer values between OPAL-RT simulators and Arduino microcontrollers at each location. The exchange of state information between the two remote locations is done through EtherDUE boards using the TCP/IP (Internet Protocol) communication protocol and synchronization is implemented using the master/slave hand-shaking configuration algorithms on Arduino boards. However, the results are based on perfect knowledge of the model systems and further studies are required for the imperfect and variable knowledge of systems.

The detailed reviews on RT testing and simulation methods for microgrids in different areas of application presented in [61] and [62] are recommended for further in-depth study. For the detailed review on the RT modelling and the simulation methods of power electronics and related challenges, the references [63] and [64] are suggested. The application of RT simulations using FPGA based accurate solutions particularly for different power electronics applications have recently been reported in many references. Related to this the references [65]-[79] are suggested for further reading.

III. ADAPTIVE PROTECTION WITH IEC 61850

The adaptivity of the protection schemes is the new requirement for the detection and isolation of faults in both the grid-connected and islanded mode operation of AC microgrids. The main reason behind the requirement of the adaptivity is the variation in magnitude of fault current in the grid-connected and the islanded mode. Due to the absence of the main grid in the islanded mode the magnitude of fault current is expected to be lower than the pickup current value of the grid-connected mode particularly if the large number of the converter-based DERs are connected in AC microgrid. This may cause the blinding of the OC relays which are usually used for fault detection in medium voltage (MV) and LV networks. The adaptivity of protection scheme can be implemented either using the same principle of fault detection and isolation for example, OC relays with different settings in the grid-connected and the islanded mode or using the separate principles of fault detection and isolation in both modes of operation for example, OC relays in the grid-connected mode and differential current, directional OC or symmetrical components in the islanded mode. Moreover, the adaptive protection can be implemented using either the centralized or decentralized control and communication architecture. The IEC 61850 communication standard including GOOSE and SV (sampled values) protocols using Ethernet network could facilitate the implementation of successful adaptive protection schemes. Several adaptive protection schemes have been suggested in the scientific literature as previously reviewed and reported in [2] [4] [11] [80]. The most practical and latest adaptive protection schemes are reviewed in this section.

An adaptive protection using the centralized control and communication architecture has been demonstrated and practically installed at a 20 kV feeder pilot of the largest geographical island in Finland called the Hailuoto island. The islanded mode operation on the Hailuoto island is supported by a 0.5 MW WTG and a 1.5 MW diesel generator for a peak load of 1144 kW. The centralized adaptive protection is applied using IEC 61850 communication standard for changing the directional OC relays settings [10].

The centralized communication-assisted protection for MV microgrids with the converter-based DERs proposed in [81] uses symmetrical current components based directional module and OC relays in the grid-connected mode and the under-voltage, the symmetrical current components based high-impedance fault detection and the directional module for the islanded mode of operation. The scheme uses the definite time coordination in combination with fault detection modules as a backup if the communication fails. The proposed scheme does not use the adaptive settings, however the separate methods for fault detection in the grid-connected and islanded modes. To activate and deactivate different methods of the variable sensitivities in the grid-connected and islanded modes, the scheme necessarily requires the communication signal which makes the scheme fall under the category of adaptive protection schemes. The adaptive protection schemes using the centralized communication architecture have also been suggested previously in [82]-[84].

An adaptive protection for a campus microgrid presented in [85] uses the directional OC relays with adaptive settings for the detection of load-side faults and for the implementation of the localized differential protection to detect faults in the loop sections. The islanding mode operation is supported by a gas turbine synchronous generator operating in parallel to the WTGs, PVs and BESS to service a load of 8 MW. The adaptive scheme uses the transfer trip or the permissive overreaching transfer trip (POTT) as the backup for the primary protection failures and the non-directional substation OC relay as the backup of the transfer trip failures in the grid-connected mode. A high speed (2 ms) optical fiber communication link with highly reliable communication capability is used for the adaptive protection. The scheme prefers the localized differential protection over the centralized differential protection due to the fact that the centralized scheme results in unacceptable computational time delays by the central controller [85].

The other adaptive and IEC 61850 communication-based protection schemes have been suggested recently for microgrids and distribution networks with DERs in [86]-[93]. Our previous paper [11] proposed an adaptive protection algorithm using IEC 61850 GOOSE communication for a radial AC microgrid to operate within the standard LVRT time period of DERs.

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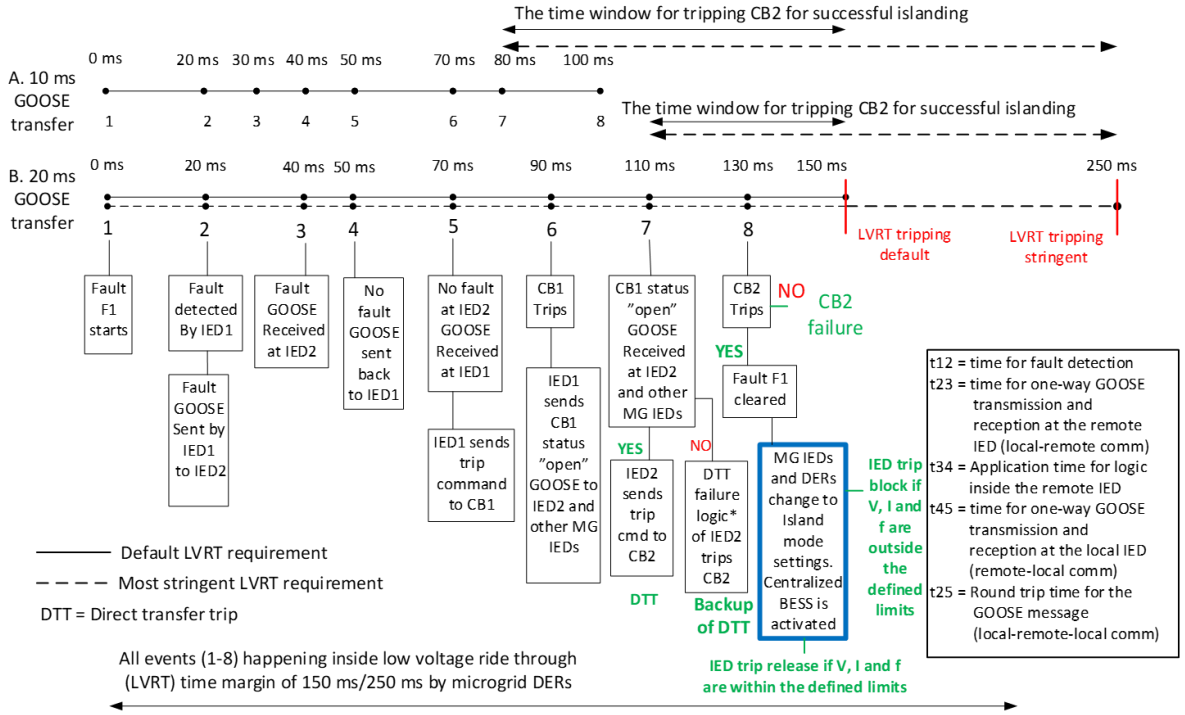

FIGURE 2. **The communication-dependent logically selective protection algorithm for the detection and isolation of fault F1 using the centralized control architecture and aligned with EN 50549-1-2019 and EN 50549-2-2019 LVRT standards.**

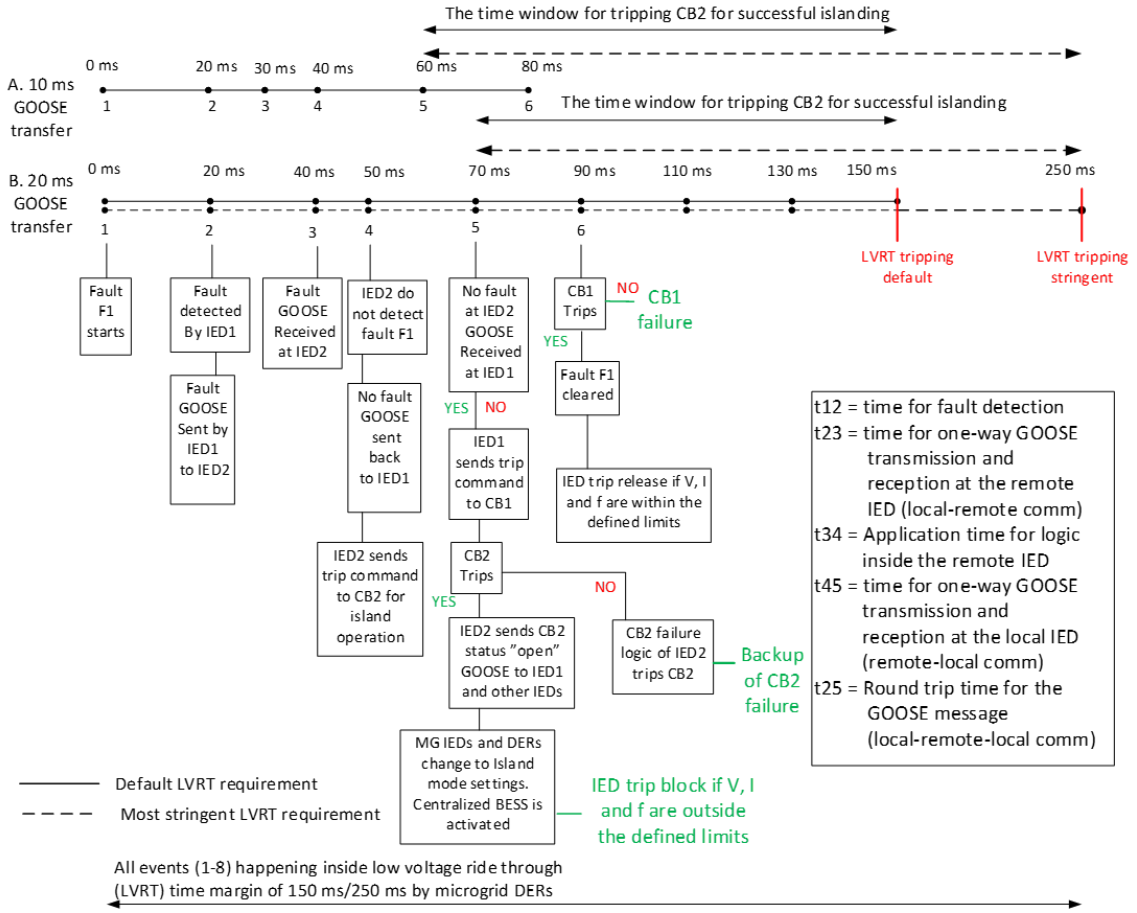

FIGURE 3. **The communication-dependent logically selective protection algorithm for the detection and isolation of fault F1 using the decentralized control architecture and aligned with EN 50549-1-2019 and EN 50549-2-2019 LVRT standards.**

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The proposed method provides the natural coordination in terms of the standard time delays of 10 ms or 20 ms between the publication and the subscription of a Boolean GOOSE signal. Thus, the process of fault detection and isolation is accomplished within the standard LVRT curve of DERs after the fault if the communication is reasonably reliable. In this paper, the reliability of the proposed method is practically checked using the real-time HIL simulation of IEC 61850 GOOSE protocol implemented in the RT target and the actual digital relay. However, the previously proposed algorithm for the detection and isolation of a three-phase (3Ph) close-in short-circuit fault F1 near the microgrid PCC (Fig. 4) is modified in this paper as explained in the following section. Further improvements have been suggested to increase the reliability of the proposed communication-dependent logically selective adaptive protection. The scheme is capable of being extended also to the looped microgrids and can be implemented with the centralized or the decentralized communication architecture.

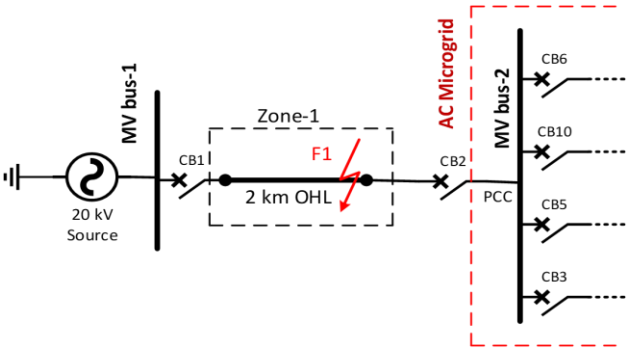

FIGURE 4. The 3Ph close-in short-circuit faut F1 near microgrid PCC.

IV. HIL TESTING METHODOLOGY AND RESULTS

Fig. 2 presents the modified versions of the previously proposed communication-dependent adaptive and logically selective fault detection and isolation algorithm for the grid-side fault F1 in [11].The main modification is that in the modified algorithm the control of DERs and the setting groups of IEDs are changed after the opening of the CB2 at the PCC of the microgrid which was done previously after the opening of the grid-side circuit breaker CB1. The algorithm assumes that the fault F1 happens in the grid-connected mode between the CB1 and CB2 locations and only the grid-side relay at CB1 location detects the fault F1. Additionally, the modified algorithm also includes the most stringent LVRT requirement for the converter-based DERs according to the new European grid code standards EN 50549-1:2019 and EN 50549-2:2019.

Fig. 2 and Fig. 3 show the implementation of the proposed algorithm with the centralized and the decentralized control architecture, respectively. With the centralized control architecture, if the fault F1 happens then the central relay at CB1 collects the fault information and then decides to open the circuit breaker CB1 and sends transfer trip command to the remote circuit breaker CB2. With the decentralized control architecture, if the fault happens then each relay at CB1 and CB2 locations collects the fault information and decides to open the corresponding circuit breaker independently. In this paper, only the protection algorithm using the centralized control architecture (Fig. 2) is evaluated.

The main objective behind the HIL testing is to estimate the round-trip time of a fault detection Boolean signal using the real-time simulation. It means the estimation of time delay from the event 2 to event 5 (t_{25}) of the protection algorithm of Fig. 2 which is actually the round-trip time between relays at CB1 and CB2 locations. The other objective is to check if the "10 ms GOOSE transfer" timeline is more practical than the "20 ms GOOSE transfer" timeline (Fig. 2). In the HIL testing CB1 is opened instantaneously after collecting "No fault" information of the IED at CB2 using the IEC 61850 GOOSE protocol and CB2 is opened using the transfer trip command from the IED at CB1 location.

This section explains the steps taken to carry out the IEC 61850 GOOSE communication-based HIL testing of VAMP digital relay using the RTDS of OPAL-RT and Ethernet link communication. Both the VAMP digital relay and the OPAL-RT simulator were capable of publishing and subscribing at least one Boolean signal using IEC 61850 GOOSE protocol. The testing of VAMP digital relay not only involved the successful publication and subscription, but it also included the recording of the real-time Boolean signal (fault detection signal) during the publication and the subscription by both the real-time digital simulator and the VAMP relay. The real-time GOOSE signal data was recorded using OpWriteFile block of the OPAL-RT simulator which saves the real-time data in a MATLAB file (.mat) format. The subscription of the real-time GOOSE signal by the VAMP relay, however, involved only the time stamp-based subscription of GOOSE message visible from the "Event Buffer" memory of the VAMP relay. In other words, it was not possible to record the subscribed GOOSE signal of the VAMP relay by the OPAL-RT simulator at the receiving-end Ethernet link adapter of the VAMP relay. This means the OPAL-RT simulator could only record the Boolean signal in real-time at three instances: 1. When the GOOSE signal is published by the OPAL-RT simulator, 2. When the GOOSE signal is subscribed by the OPAL-RT simulator, and 3. When the GOOSE signal is published by the VAMP relay and subscribed by the OPAL-RT simulator. Fig. 5 presents the IEC 61850 GOOSE HIL testing setup at the FREESI (Future Reliable Electrical and Energy Systems Integration) laboratory of the University of Vaasa, Finland.

The HIL testing setup hardware in Fig. 5 includes the OPAL-RT simulator platform, VAMP relay, the laptop computer for the graphical user interface for commands and the visualization of the results, the Ethernet switch and the Ethernet cables for connections. The software involved in this HIL testing includes the RT-LAB of OPAL-RT, MATLAB/Simulink toolbox Simscape (the previous SimPowerSystems), VAMPSET relay configuration software, the Wireshark network protocol analyzer to capture the published GOOSE message packets from the local Ethernet

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and Windows 7 operating system of the laptop. The description of the hardware involved in the IEC 61850 GOOSE protocol testing is given in the following subsections.

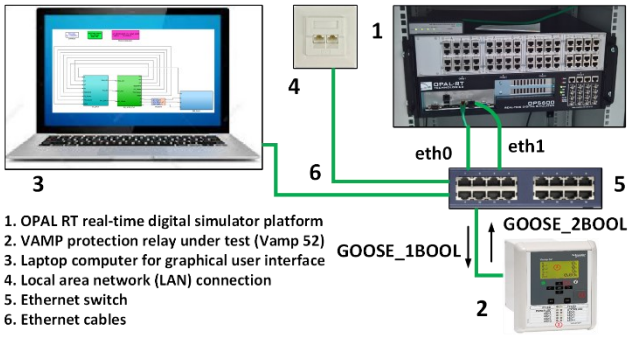

FIGURE 5. **The HIL testing setup at the FREESI Lab.**

A. REAL-TIME HIL TESTING HARDWARE

1) OPAL-RT SIMULATOR PLATFORM

The OPAL-RT simulator platform used for the HIL testing case study is OP5600 HIL Box (Fig. 5, number 1) with four 3.2 GHz INTEL processor cores with Redhat Linux operating system and six Ethernet network ports. Two Ethernet network ports are available at the front while the rest of the Ethernet network ports are located at the back of the chassis. The OP5600 simulator is available in different configurations operating with either Spartan 3 or Virtex 6 FPGA platforms with the target computer having minimum four to maximum thirty-two 2.4 or 3.3 GHz cores or without any target computer. In general, the front of the OP5600 HIL Box chassis consists of the monitoring interfaces and connectors whereas the back of the chassis consists of all I/O connectors, power cable, main power switch and the FPGA monitoring connections. The main housing architecture of the OP5600 HIL Box is divided into two sections: The upper section and the lower section. Both the upper and the lower sections are connected by a DC power cable and a PCIe (Peripheral Component Interconnect Express) cable, a high-speed serial computer expansion bus. The lower section consists of a powerful target computer including ATX (Advance Technology eXtended) motherboard with up to 12 (or maximum 32 cores), six dynamic random-access memory (DRAM) connectors, 250 MB (megabyte) hard disk, 600 W power supply and PCIe boards up to eight slots depending on the configuration. The upper section consists of signal conditioning modules (AD and DA converters), a flexible high-speed front-end processor and DC supplies for analog and digital signals. The front-end processor processes the conditioning signals and executes fast models previously downloaded via the PCIe link between the target and the front-end processor [94][95]. The signal conditioning modules in the used platform include the OP5330 DA converter module with 16 single-ended output channels [96], the OP5340 AD converter module with up to 16 differential channels [97], the OP5353 digital input signal conditioning module with 32 opto-isolated digital inputs (4-50 Vdc input voltage) [98] and the OP5360 digital output module with 32 digital output channels (5-30 Vdc output voltage) [99].

2) THE VAMP RELAY UNDER TEST

The device or the hardware-under-test called HUT used in the HIL testing is VAMP 52 feeder and motor protection relay of the Schneider Electric (Fig. 5, number 2). The Vamp 52 is a numerical protection relay or IED with signal filtering, protection and control functions fully implemented through digital processing. The VAMP 52 protection relay uses an adapted Fast Fourier Transformation (FFT) numerical technique. By using the synchronized sampling of the measured signal (voltage or current) with 32 samples per cycle, the FFT solution is realized with just a 16-bit micro controller without the help of a separate DSP. The main hardware components of the VAMP relay include the energizing inputs, digital input elements, output relays (trip and alarm relays), AD converters, the micro controller with a memory circuit, a power supply unit and a human-machine interface (HMI).

The protection functions of the VAMP 52 relay include a three-stage OC protection (IEC: I>, I>>, I>>> or IEEE: 50/51), thermal overload protection (IEC: T> or IEEE: 49), current unbalance protection (IEC: I_2/I_1> or IEEE: 46), CB failure protection (IEC: CBFP or IEEE: 50BF) and several other feeder and motor specific functions. The VAMP 52 relay also have eight independent programmable stages (IEC: Prg1-8 or IEEE: 99) for special applications. The user can select the supervised signal and the comparison mode to build custom programmable protection stages. The VAMP 52 relay has four setting groups available and the switching between setting groups can be controlled manually or by using the digital and virtual inputs including mimic display, communication and logic inputs [100].

The VAMP 52 relay is capable of communicating with other systems using the most common protocols including Modbus RTU (Remote Terminal Unit), Modbus TCP, Profibus DP (Decentralized Periphery), IEC 60870-5-101, IEC 60870-5-103, IEC 61850, SPA (Strömberg Protection Acquisition) bus, Ethernet/IP and DNP (Distributed Network Protocol) 3.0. [100].

3) THE LAPTOP COMPUTER

The laptop computer used for the HIL testing is HP EliteBook 840 G3 with Intel(R) Core (TM) i7-6600U CPU (central processing unit) @ 2.60GHz, 2.81 GHz processor and 16 GB (gigabyte) of installed RAM. The computer uses Windows 7 operating system. All the required software for the HIL testing compatible with Windows 7 operating system is installed on the laptop computer. The laptop computer with all the required software installed is capable of performing offline/real-time modelling and simulation, configuring the relay, capturing the published GOOSE message and providing the graphical user interface (GUI) for real-time simulation testing. The laptop computer is connected to the same Ethernet network switch where the OPAL-RT simulator and the VAMP relay are previously connected via an Ethernet cable (Fig. 5, number 3).

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4) THE ETHERNET NETWORK AND SWITCHES

The Ethernet connection of the HIL testing setup in the FREESI lab to the local area network (LAN) router of the University of Vaasa is provided through a surface-mounted two-port white wall box/plate (Fig. 5, number 4). One port of the Ethernet switch at the lab (Fig. 5, number 5) is connected to a port of the Ethernet wall box/plate using a twisted pair high speed data cable to access the University of Vaasa LAN network. The rest of the devices including the laptop computer, the OPAL-RT simulator and the VAMP relay are connected to the same Ethernet network using data cables connected to the other ports of the Ethernet switch at the lab that is acting as an IEC 61850 station bus.

5) THE ETHERNET CABLES

Five pairs of the twisted pair high speed data cables with RJ45 Ethernet plugs/connectors (Fig. 5, number 6) are required for the HIL testing setup, the connection arrangement of the devices is presented in Fig. 5.

B. THE CREATION OF RT SIMULATION MODEL

In this section the description about the general benchmark model of a radial AC microgrid used for the HIL simulation is given along with the modelling steps to create the MATLAB/Simulink Simscape and RT-LAB real-time versions of the described AC microgrid model. Additionally, the implementation of IEC 61850 communication inside the RT model of the AC microgrid is also described in this section.

1) THE RADIAL AC MICROGRID MODEL IN SIMULINK/SIMSCAPE

The schematic diagram of a general benchmark model of a radial AC microgrid used for the HIL testing is shown in Fig. 6. The AC microgrid is connected to the 20 kV main grid MV bus-1 at CB2 location via a 2 km overhead line. CB2 location is therefore the PCC for the main grid and the AC microgrid. The normal downstream connections at MV bus-2 in the AC microgrid consist of a WTG of 2 MW capacity, a load of 2 MW and a 1 km MV cable feeder connecting MV bus -2 with LV bus through a 0.5 MVA, 20/0.4 kV transformer. Additionally, a BESS of 2.1 MW capacity is also connected at MV bus-2. The BESS is assumed as a charging load in the grid-connected mode, while it can be used as a grid-forming source only during the islanded mode of operation when CB2 is open due to fault F1. The LV bus of the AC microgrid consists of a PV system of 400 kW capacity and a load of 400 kW.

The radial AC microgrid model presented in Fig. 6 was previously modelled and analyzed using offline simulations in PSCAD software for the development of an adaptive protection algorithm using the IEC 61850 communication standard but without the connection of a BESS (Zone 10 in Fig. 6). The details about the developed adaptive protection algorithm and the fault analysis with the earlier PSCAD model can be found in [11]. The AC microgrid model has been further developed using MATLAB/Simulink modelling environment with an additional BESS of 2.1 MW_{peak} connected at MV bus-2 to be used as grid-forming source for the islanded mode of operation.

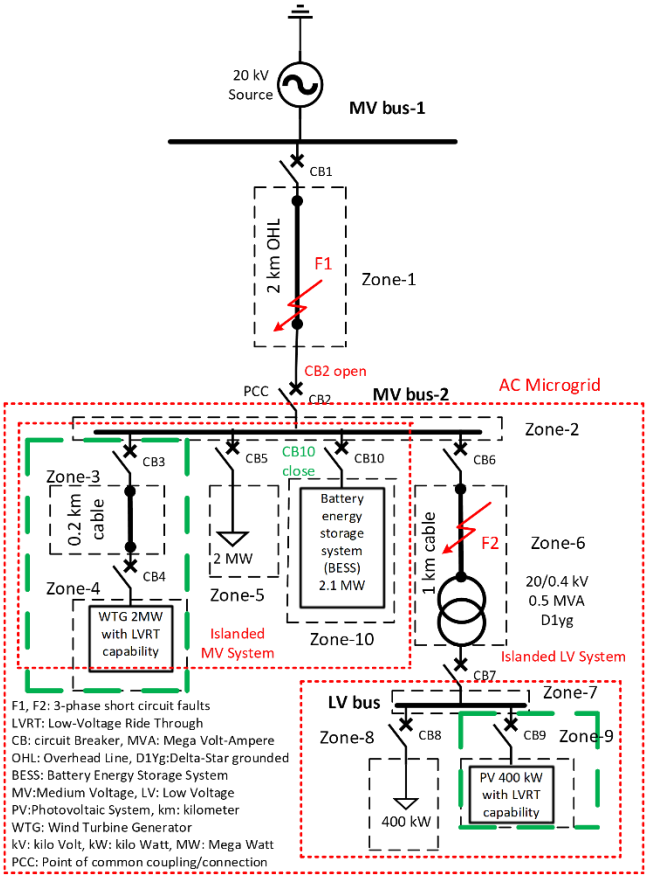

FIGURE 6. The general benchmark model of a radial AC microgrid used for HIL testing.

The WTG, PV and BESS models are the average type models developed in MATLAB/Simulink; their details are given in the next subsection. The overhead line and cables are represented by 3Ph pi-section lines, the transformers are 3Ph two-winding transformers, and the main grid is represented by a 3Ph 20 kV 50 Hz programmable voltage source. The results of the protection coordination of the definite-time and the inverse-definite minimum time (IDMT) OC relays in the grid-connected mode without and with DERs and in the islanded mode with DERs and the central grid-forming BESS have already been presented in the previous paper [4] using MATLAB/Simulink and RT-LAB version of the model.

In this paper, the HIL simulation testing of the actual VAMP relay is performed after the real-time implementation of the IEC 61850 publisher and subscriber blocks in the RT-LAB model using the Ethernet communication link. The main objectives are to find the expected round-trip communication delays of a Boolean signal exchanged between two relays at different substations (the centralized and distributed relays), the seamless transition from the grid-connected to the islanded mode with the exchange of Boolean logical signals and the implementation of an adaptive protection during the grid-

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connected and the islanded mode. In this way, the realization extent of the earlier proposed adaptive protection algorithm [11] can be found with HIL simulation testing for its practical implementation. Additionally, the dynamic behavior of DER models in real-time simulation is also compared.

2) THE RT COUNTERPART OF THE RADIAL AC MICROGRID MODEL

After the complete offline modelling and simulation of the AC microgrid model (Fig. 6), the model was converted to the real-time version using the RT-LAB software of OPAL-RT. The topmost level of the AC microgrid model developed in Simulink and RT-LAB is presented in Fig. 7.

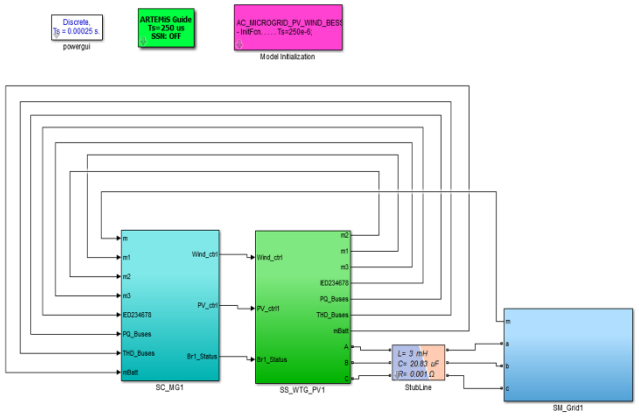

FIGURE 7. The topmost level of the radial AC microgrid model developed in Simulink/RT-LAB.

The developed RT-LAB model (Fig. 7) consists of total three subsystems, two of them are computational subsystems named as SM_Grid1 and SS_WTG_PV1 and one is a console subsystem named as SC_MG1. The data between two computation subsystems (SM_Grid1 and SS_WTG_PV1) is exchanged synchronously through shared memory. The data between any computational subsystems (SM_Grid1 or SS_WTG_PV1) and the console subsystem (SC_MG1) is exchanged asynchronously through TCP/IP link.

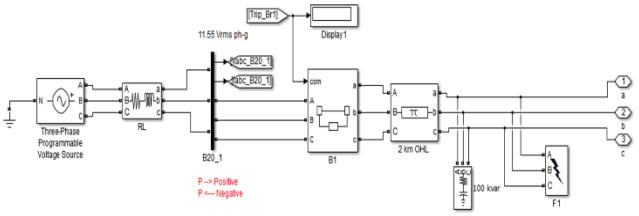

FIGURE 8. The details of the SM_Grid1 subsystem of the developed Simulink/RT-LAB model.

The SM_Grid1 and SS_WTG_PV1 subsystems are connected with each other using an ARTEMiS stubline which provides the decoupling of the state space matrices of two subsystems thus reducing the memory overflow and increasing the simulation speed. The details of the SM_Grid1 subsystem are shown in Fig. 8.

The SM_Grid1 subsystem consists of the main grid components up to zone-1 of Fig. 6 including 20-kV 3Ph programmable voltage source, MV-bus1, CB1 and overhead line of 2 km. Additionally, a 3Ph capacitor bank of 100 kvar is also connected in this subsystem for the proper voltage regulation. A 3Ph short-circuit fault F1 with R_f = 5.001 Ohm at the end of 2 km overhead line is also located in SM_Grid1 subsystem. The rest of the components of AC microgrid of Fig. 6 including the components in protection zones 2-10 and circuit breakers CB2-CB10 along with 3Ph short circuit fault F2 with R_f = 0.001 Ohm are located in SS_WTG_PV1 subsystem. The details of SS_WTG_PV1 subsystem are given in Fig. 9. The details of the PV_system1 and the BESS inside the SS_WTG_PV1 subsystem are given in Fig. 10 and Fig. 11, respectively.

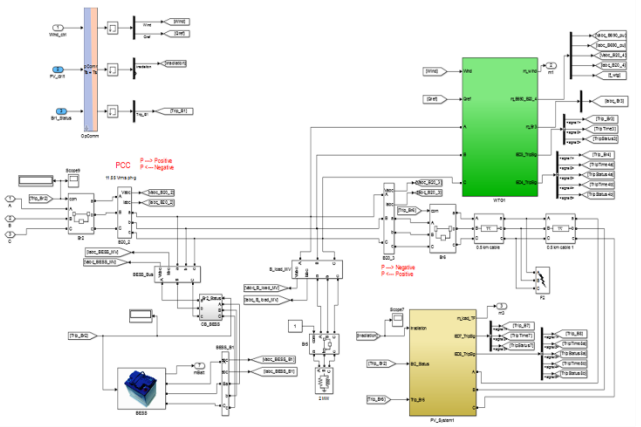

FIGURE 9. The details of the SS_WTG_PV1 subsystem of the developed Simulink/RT-LAB model.

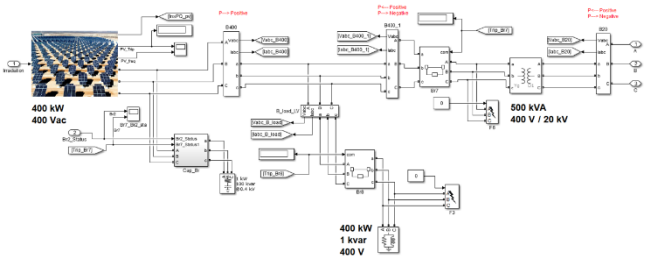

FIGURE 10. The details of the PV_System1 of the SS_WTG_PV1 subsystem of the developed RT-LAB model.

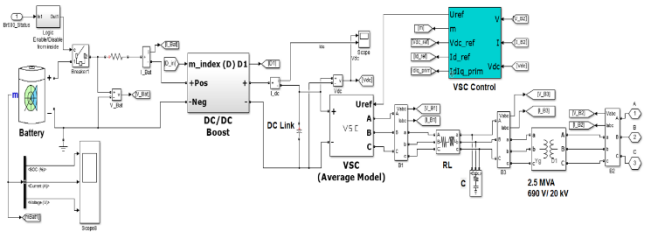

FIGURE 11. The details of the BESS of the SS_WTG_PV1 subsystem of the developed RT-LAB model.

The WTG model (Fig. 9, green) is adopted from the example model [101]. However, the parameters of the WTG model like voltage, power capacity, frequency etc. have been changed according to the AC microgrid model of Fig. 6. The WTG average model is able to run correctly with fixed time-

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step discrete solver suitable for RT simulation. The time-step of 250 µs is used to avoid overruns during RT simulation. The WTG model is also capable of providing the LVRT during the faults with an optional fault current contribution of 1.2-2 times the full rated current during the short circuit fault by setting the maximum output current limit of its full-scale converter.

The PV model (Fig. 10) is adopted from the "Active Distribution Grid" model developed in [102][103]. However, the parameters (voltage, power capacity etc.), the control and the protection of the PV model have been modified according to the AC microgrid model (Fig. 6). The LVRT behavior is also added to the PV model to provide 1.2-2 times the full rated current during the short circuit faults when the grid-side voltage drops below 50%.

The BESS model (Fig. 11) has been developed on the basis of the PV model given in [104]. The 2.1 MW_{peak}, (600 V_{dc} (nominal), 698 V_{dc} (fully charged), 3000 AH (nominal)) battery is connected at the input of DC-DC boost converter to raise its voltage to 1100 V_{dc} at the DC-link. The 1100 V_{dc} at the DC-link was used as input to a 3Ph inverter for getting 690 V_{ac} at the output RLC-filter which is then step up to 20 kV by a 2.5 MVA, 0.69/20 kV 3Ph transformer for the connection to the MV bus-2.

After the creation of subsystems, the next step is to take measurement signals out from the computation subsystems to the console subsystem for the real-time observation of the model behavior. The measurements from the output ports (Outports) of one subsystem to the input ports (Inports) of the other subsystem have to be transferred through OpComm blocks of the RT-LAB/ARTEMiS. Fig. 9 shows three input ports with different control signals transferred from SC_MG1 subsystem to the SS_WTG_PV1 subsystem through OpComm block located in SS_WTG_PV1 subsystem. In the same way, different measurements have been transferred from the SM_Grid1 subsystem and SS_WTG_PV1 subsystem to the SC_MG1 (Fig. 7) using the individual OpComm blocks with unique "Acquisition Group" numbers for each measurement inside the SC_MG1 subsystem. If everything is correctly connected and the settings of the model are saved using Simulink, the model (Fig. 7) is ready for the real-time software-in-the-loop or fully digital RT simulation using the RT-LAB software.

With the addition of the RT target in RT-LAB and the availability of the RT-LAB model in the project explorer, the model can be opened in RT-LAB editor for the compilation or code generation. The C code can be generated and transferred to the target using the "Build the model" command. Any errors generated during "Build the model" process have to be removed first before proceeding to the next step of "Load the model". The process of "Build the model" should be repeated after each new subsystem component/control addition or replacement.

After the successful completion of the "Build the model" process without any error messages, the next step is to "Load the model." After "Load the model" command from the RT-LAB editor, the model will be loaded on the target and a message will appear in the "view" section of the RT-LAB under the "Display" tab indicating a pause mode with "zero (0)" overruns.

The final step is the real-time running of the RT-LAB model by "Execute the model" command from the model editor. This will open the console subsystem "SC_MG1" replica created automatically by RT-LAB. From this console, the real-time measurements can be seen and controlled by changing the controller inputs on-the-fly. The display view of the model will show the new message indicating the run mode along with synchronized time step of the simulation.

From the monitoring view of the RT-LAB model, it can be seen if the model is running with any overruns or not and how much is the minimum, maximum and average jitter (dt) of the signal in each subsystem of the model. A jitter (dt) around 7 µs is considered as a good jitter. As mentioned in the earlier chapters, too little time-step of simulation may give overruns and too large a time-step will give erroneous results. If the jitter is too close to the time-step of simulation, it will cause overruns. In most cases, the overruns will vanish after increasing the time-step of simulation. The accuracy of the results should be carefully checked by saving the results in MAT-file format using the OpWriteFile block of ARTEMiS by carefully setting its mask parameters.

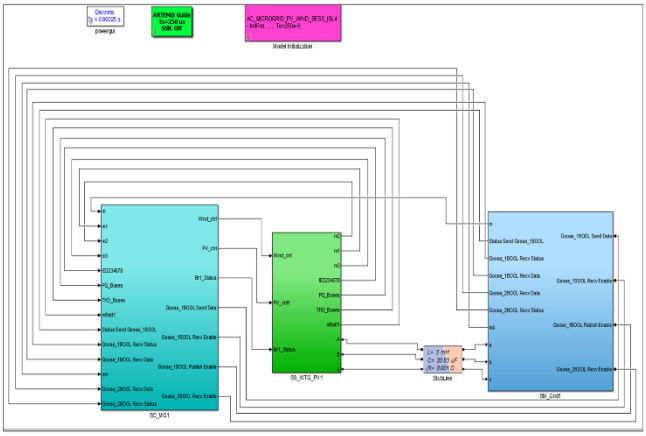

FIGURE 12. The topmost view of the RT model with IEC 61850 GOOSE protocol implemented.

3) THE IMPLEMENTATION OF IEC 61850 GOOSE PROTOCOL IN THE RT MODEL FOR HIL TESTING

For the Ethernet network transmission of the Boolean signals represented by logical states of 0 and 1 for the YES/NO fault detection or open/close states of the CBs of the model, the IEC 61850 GOOSE protocol needs to be implemented inside the error free RT-LAB model of the radial AC microgrid. The implementation of the IEC 61850 GOOSE protocol in RT-LAB model can be done through "Opal IEC 61850 GOOSE Publisher" and "Opal IEC 61850 GOOSE Subscriber" blocks of IEC 61850 library of the RT-LAB. Although, the GOOSE publisher and subscriber blocks can be located in any computation subsystems like SM_Grid1 or SS_WTG_PV1,

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but these have been placed only in SM_Grid1 subsystem of the RT-LAB model. The topmost view of the RT-LAB model of radial AC microgrid after the implementation of IEC 61850 GOOSE protocol is shown in Fig. 12.

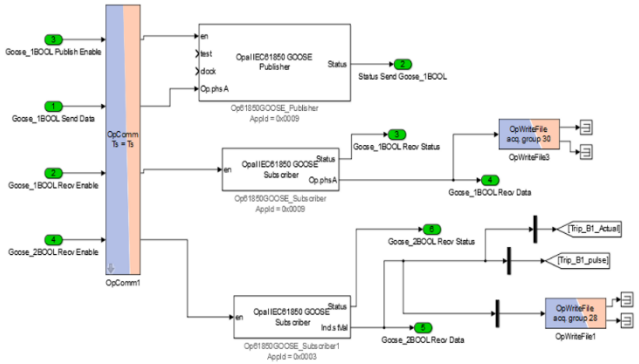

FIGURE 13. The Opal IEC 61850 GOOSE Publisher and Subscriber blocks placed inside SM_Grid1 subsystem.

The Opal IEC 61850 GOOSE Publisher and Subscriber blocks inside the SM_Grid1 subsystem and their inputs and outputs are shown in Fig. 13 and described in Table II. There is only one GOOSE publisher block with application ID AppId = 0x0009 used for sending the fault detection Boolean signal represented by GOOSE message name "Goose_1BOOL" from the OC relay inside the SM_Grid1 subsystem to the station bus/Ethernet switch (Fig. 5, number 5) for the IED under test (VAMP relay) to subscribe.

TABLE II
INPUTS AND OUTPUTS OF GOOSE PUBLISHER AND SUBSCRIBER BLOCKS

Input/ Output	Description (signal name)	From/To subsystem
GOOSE PUBLISHER BLOCK (AppId = 0x0009)		
en	Enable or disable GOOSE publication (Goose-1BOOL Publish Enable)	From SC-MG1
test	-	-
clock	-	-
Op phsA	Data of the signal to be published (Goose-1BOOL Send Data)	From SC-MG1
Status	True/False status of published signal (Status Send Goose-1BOOL)	To SC-MG1
GOOSE SUBSCRIBER BLOCK (AppId = 0x0009)		
en	Enable or disable GOOSE subscription (Goose-1BOOL Recv Enable)	From SC-MG1
Status	True/False status of subscribed signal (Goose-1BOOL Recv Status)	To SC-MG1
Op phsA	Data of the subscribed signal (Goose-1BOOL Recv Data)	To SC-MG1
GOOSE SUBSCRIBER BLOCK (AppId = 0x0003)		
en	Enable or disable GOOSE subscription (Goose-2BOOL Recv Enable)	From SC-MG1
Status	True/False status of subscribed signal (Goose-2BOOL Recv Status)	To SC-MG1
Ind stVal	Data of the subscribed signal (Goose-2BOOL Recv Data)	To SC-MG1

The GOOSE publisher block (Fig. 13, Table II) receives two input signals from the console subsystem SC_MG1 namely "Goose_1BOOL Publish Enable" and "Goose_1BOOL Send Data" and sends one output signal "Status Send Goose_1BOOL" to the console subsystem SC_MG1. The output of the GOOSE publisher block named as "Status Send Goose_1BOOL" is sent to the console subsystem SC_MG1 for the real-time monitoring. A simple two-way control switch with input 1 to enable and input 0 to disable the publishing of the GOOSE message is used inside the SC_MG1 subsystem for controlling the "Status" output of the published signal in real-time. The output of the two-way control switch is directed back to the SM_Grid1 subsystem as the signal "Goose_1BOOL Publish Enable" connected to the input "en" of the GOOSE publisher block. The GOOSE publisher block will publish the GOOSE_1BOOL signal to the station bus/Ethernet switch only if the status of its input "en" is logical "TRUE". The second input signal to the GOOSE publisher block is the actual GOOSE data signal named as "Goose_1BOOL Send Data", here it is the fault detection signal of OC relay inside SM_Grid1. The fault detection data signal is already transferred to the console system SC_MG1 from the SM_Grid1 subsystem for the real-time monitoring. Now the fault detection signal is directed back from the console subsystem SC_MG1 back to the SM_Grid1 as input "Goose_1BOOL Send Data" to the GOOSE publisher block connected to its input "*Op phsA*" for publishing to the Ethernet switch.

The first GOOSE subscriber block with AppId = 0x0009 (Fig. 13, Table II) receives the only input control signal "en" from the console subsystem SC_MG1. A simple two-way switch with input 1 to enable and input 0 to disable the subscription of the GOOSE message is used inside the console subsystem SC_MG1 for the real-time control of input "en". The GOOSE subscriber block will subscribe to the GOOSE signal from the station bus/Ethernet switch only if the status of its input "en" is logical "TRUE". The real-time status of the subscribed signal can be monitored from the first output "Status" of the GOOSE subscriber block. The second output "*Op phsA*" of the GOOSE subscriber block contains the actual data of the Goose_1BOOL signal subscribed from the Ethernet switch that is sent to the console subsystem SC_MG1 for the real-time monitoring. The real-time subscribed signal "Goose_1BOOL Recv Data" can also be saved in MAT-file using the OpWriteFile block (Fig. 13) for offline data analysis later to check the quality/performance of the subscribed data signal.

The second GOOSE subscriber block with AppId = 0x0003 (Fig. 13, Table II) also receives the only input signal "en" from the console subsystem SC_MG1. This GOOSE subscriber block is used to subscribe to the Goose_2BOOL signal published by the VAMP relay to the Ethernet switch. The real-time subscribed signal "Goose_2BOOL Recv Data" is sent to the console subsystem SC_MG1 for the real-time monitoring. This signal can also be saved in MAT-file using the OpWriteFile block (Fig. 13) for offline data analysis later to check the quality of the subscribed signal. The real-time monitoring and saving of the data of the published and subscribed GOOSE messages establishes a closed-loop two-

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way communication link between the OPAL-RT target and the actual VAMP relay through the Ethernet switch.

The real-time subscribed signal "Goose_2BOOL Recv Data" published by the VAMP relay has been used to trip CB1 in real-time inside the SM_Grid1 subsystem. The same data signal sent from the SM_Grid1 subsystem to SS_WTG_PV1 subsystem via the console subsystem SC_MG1 is also used for tripping CB2. The results are explained in the following sections. The control and data inputs connected to the GOOSE publisher and subscriber blocks have to pass through the OpComm block first as it is done in Fig. 13.

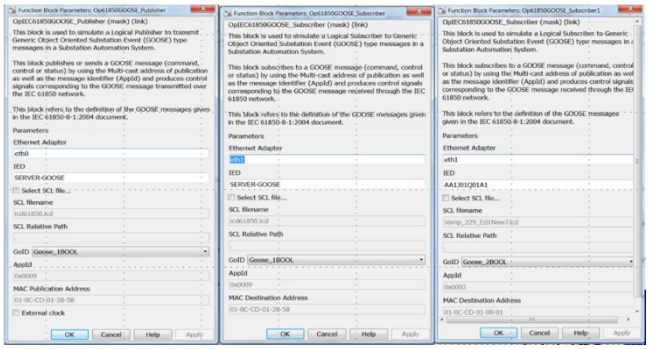

FIGURE 14. The parameter settings of the GOOSE publisher and subscriber blocks of Fig. 11.

The mask parameter settings of the Opal IEC 61850 GOOSE publisher and GOOSE subscriber blocks of Fig. 13 are described in Fig. 14. The names of the Ethernet Adapter and IED have to be written manually in the related masks of the publisher and subscriber blocks. The rest of the parameters are automatically read from the SCL (Substation Configuration description Language) file which is actually an ICD (IED capability description) file of the protection relay or OPAL-RT target. The OPAL-RT target may have many Ethernet adapters named as eth0, eth1, eth2 and so on. It is recommended to publish the GOOSE message via the one Ethernet adapter and subscribed the same GOOSE message via the other Ethernet adapter. It means both the GOOSE publisher and the GOOSE subscriber blocks should have different Ethernet adapters. Therefore, the Ethernet adapter eth0 is used for the GOOSE publisher block and the Ethernet adapter eth1 is used for the GOOSE subscriber blocks (Fig. 14). The IED names manually entered in the GOOSE publisher and GOOSE subscriber masks should match the IED names written in the ICD files. The IED name "SERVER-GOOSE" is the name of the virtual IED of OPAL-RT target which is written in the ICD file named "iec61850.icd" provided in the IEC 61850 demo of OPAL-RT. The IED name "AA1J01Q01A1" is the name of the actual VAMP relay which is written in the ICD file named "Vamp_229_Ed1New7.icd" created after the final configuration of IEC 61850 GOOSE protocol of the VAMP relay using the VAMPSET relay configuration software.

The GOOSE publisher and the GOOSE subscriber blocks should use the same ICD file in order to communicate with each other successfully. The same GOOSE message "Goose_1BOOL" should be selected from the GoID (GOOSE ID) drop-down boxes of the masks of the GOOSE publisher and the subscriber blocks. The OPAL-RT subscriber block accepts the ICD file of the external test device with the same GoID messages as included the ICD file "iec61850.icd" provided by OPAL-RT even with the different IED name, AppId and MAC (media access control) destination address. Therefore, during the configuration of the external relay the same GoIDs should be used as in the ICD file "iec61850.icd" but with different AppId and MAC destination address to distinguish between the two different IEDs. Fig. 15 shows how GOOSE message inputs received from the SM_Grid1 are used for the real-time monitoring and control of the published and subscribed GOOSE messages inside SC_MG1 console subsystem.

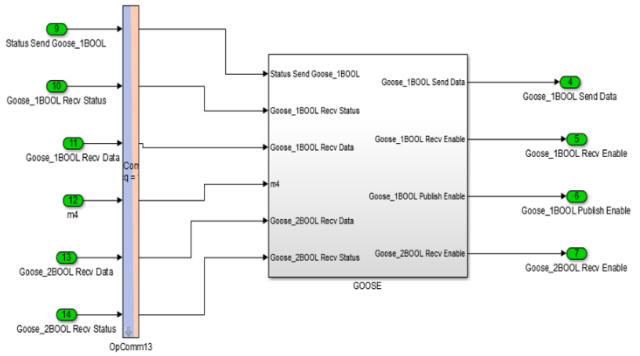

FIGURE 15. The real-time monitoring and control of the GOOSE messages in SC_MG1 subsystem.

C. THE CONFIGURATION OF THE IEC 61850 GOOSE PROTOCOL IN VAMP RELAY

After the opening of the VAMPSET relay configuration software and after the proper communication settings and establishment of the communication link with the VAMP relay, the IEC 61850 protocol can be configured. The detailed guide about the configuration of IEC 61850 protocol of VAMP relays can be found in [105]. Only the main points of the configuration of IEC 61850 protocol are discussed here based on the application note AN61850.EN005 [105].

Starting from the protocol configuration, the IP address 193.166.118.229 of the VAMP relay and the network mask "NetMask" 255.255.255.0 are entered into the "ETHERNET PORT" settings. Then from the first instance of TCP port titled "TCP PORT 1st INST," the IEC 61850 is selected from the many available protocols which activates the IEC 61850 as the Ethernet port protocol. The other settings are kept the same as the default settings. In order to verify the working of the LAN connection and to check the physical connection of the computer and the VAMP relay, the ping command can be used. The ping commands of the VAMP relay and the OPAL-RT target are shown in Fig. 16. The ping command of the VAMP relay proves the acceptance of the TCP/IP address and the network mask setting. The ping statistics indicate the

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round-trip times of the VAMP relay without any loss of packets which are although slower in comparison with the OPAL-RT target round-trip times but yet acceptable and realistic, near to the round-trip times mentioned in [105].

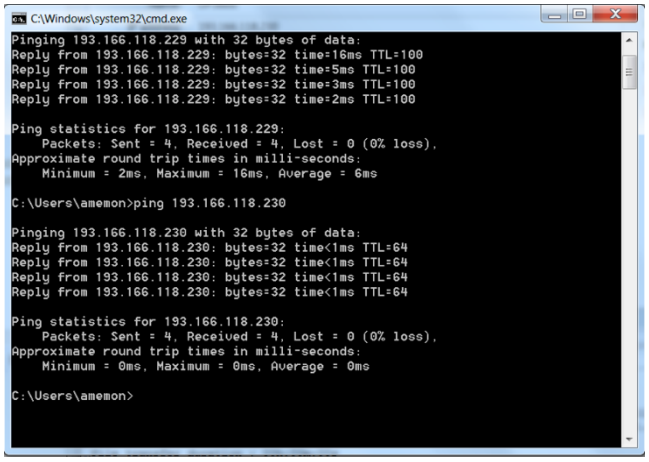

FIGURE 16. The ping command responses of the VAMP relay and the OPAL-RT target.

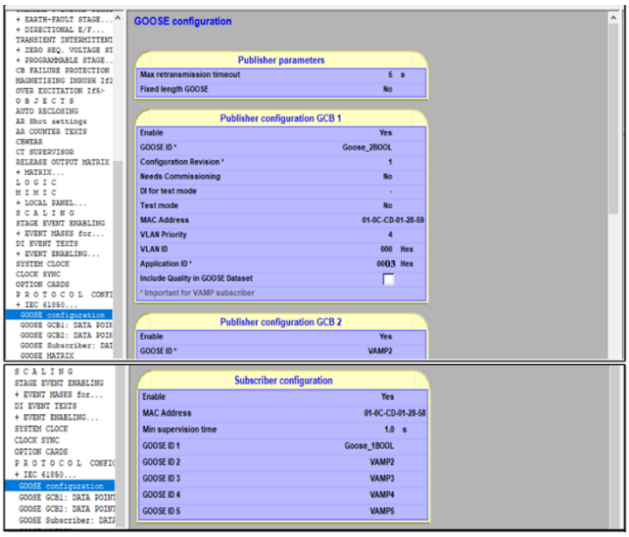

FIGURE 17. The GOOSE configuration menu of the VAMPSET software.

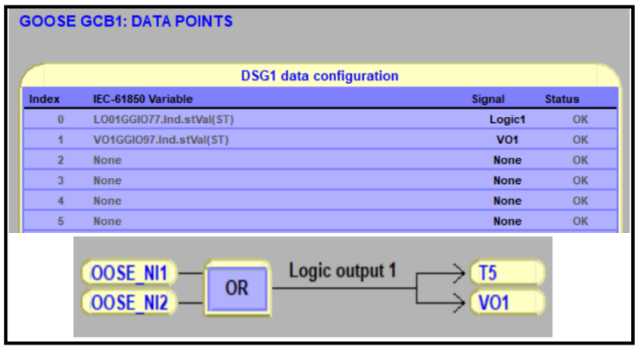

FIGURE 18. The GOOSE publisher data in "GOOSE GCB1: DATA POINTS" and related OR Logic output 1.

The activation of the IEC 61850 protocol will enable the "IEC 61850 main config" to be selectable in the group list to the left side of the VAMPSET window. In the "IEC 61850 main config" menu only the IED name should be set differently for each device connected to the same network. This IED name will appear in the final ICD file to be used in GOOSE subscriber block of the OPAL-RT. Additionally, "Dataset 1" is selected in the "LLN0 and LPHD DOs in datasets" section of the "IEC 61850 main config," where LLN0 stands for the logical node device, LPHD stands for the logical physical device and DOs stands for the data objects. Then IEC 61850 data maps (1) to IEC 61850 data maps (12) can be used to select the logical nodes (LN) which will be visible via the IEC 61850 interface. The IEC 61850 logical nodes for the functions of the device are available in the data maps which can be selected/activated by choosing "Yes" in the particular pre-defined dataset (Dataset1). For example, all digital inputs, logical output 1, all virtual inputs and virtual outputs, GOOSE network inputs 1 to 16 (GOOSE NI 1-16), GOOSE Validity Groups and GOOSE Publisher Properties etc. are selected "Yes" in data maps. The VAMP relay has three predefined datasets DS1 to DS3 which can be assigned to one or more buffered report control blocks (BRCB) and unbuffered report control blocks (URCB) using "IEC 61850 BRCB configuration" and "IEC 61850 URCB configuration" menus.

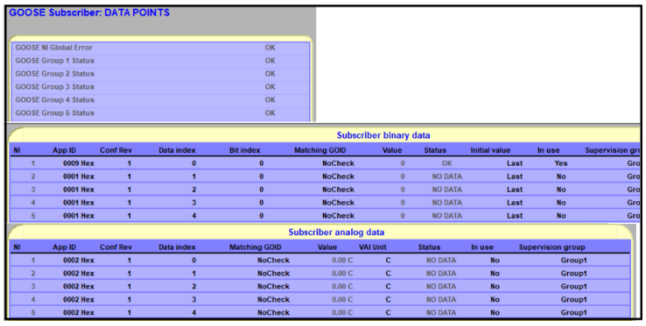

FIGURE 19. The GOOSE subscriber data in "GOOSE Subscriber: DATA POINTS" menu.

The most important part in this study is the configuration of the GOOSE messages to be published and subscribed by the VAMP relay. The GOOSE configuration menu (Fig. 17) can be opened from the VAMPSET left side group list where the GOOSE messages published and subscribed by the VAMP relay under test can be configured. The maximum retransmission timeout and fixed length GOOSE (Yes/No) can be defined in publisher parameters. The fixed GOOSE message feature is only defined by Edition 2 of IEC 61850, hence "No" should be selected for testing Edition 1 of IEC 61850. The VAMP relay under test is capable of publishing only two GOOSE messages each containing 8 bits of data packets, one GOOSE message is configured in "Publisher configuration GCB1" section and other configured in "Publisher configuration GCB2" section. The GCB1 and GCB2 stand for GOOSE control block 1 and 2, respectively. In addition to enabling the GOOSE message publication by selecting "Yes" in the "Publisher configuration GCB1"

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section, the other important parameters marked with * include the GOOSE ID, configuration revision and the application ID along with the multi-cast MAC address.

The GCB1 and GCB2 are used to control the sending of data packets of two GOOSE messages. The data to be sent is defined/selected in the "GOOSE GCB1: Data Points" and "GOOSE GCB2: Data Points" configuration menus for data points in group 1 and group 2, respectively. For example, the GOOSE message to be published by the VAMP relay is defined with GOOSE ID of "Goose_2BOOL," MAC address of 01-0C-CD-01-28-59 and AppId of 0003 Hex (Hexadecimal). The data to be sent by Goose_2BOOL message is defined in "GOOSE GCB1: Data Points" as the "Logic1" signal which is the "Logic output 1" of the "OR" logic defined in the LOGIC configuration section (Fig. 18). The status of all signals in the list of GOOSE GCB Data Points should indicate OK, otherwise the data is not sent.

In the "Subscriber configuration" sections, the incoming GOOSE messages subscribed by the VAMP relay are configured. As can be seen from Fig. 17, VAMP relay can subscribe to multiple GOOSE messages (maximum five) but all from one defined MAC Destination Address. The subscribed GOOSE message in this study is the first GOOSE message in the list which has the Goose ID of "Goose_1BOOL" and it is coming from the MAC Adress "01-0C-CD-01-28-58" of the RT target. The "Enable" should be changed to "Yes" in order to subscribe to the GOOSE message by the VAMP relay. The GOOSE data bits to be received by VAMP relay are defined in the "GOOSE Subscriber: DATA POINTS" menu. The binary/Boolean signals in the "Subscriber binary data" and analog signals in the "Subscriber analog data" sections of the "GOOSE Subscriber: DATA POINTS" menu (Fig. 19). The most important setting in the GOOSE Subscriber: DATA POINTS menu is the entry of the "App ID" of the incoming GOOSE message in Hexadecimal format. The App ID of each GOOSE message sent to the VAMP relay should be different because it is the main criteria of receiving GOOSE message in the VAMP relay. The other important settings in the "GOOSE Subscriber: DATA POINTS" menu include the "In use" and "Supervision Group" settings.

For the to be subscribed GOOSE message Goose_1BOOL which is a binary signal coming from RT target, the App ID of "0009 Hex," "In use" selection of "Yes" and "Group Supervision" of "Group1" have been entered into the "Subscriber binary data" section in row 1, with the network input index (NI) 1 in column 1 of row 1 (Fig. 19). The GOOSE_NI1 is connected to the NI in the GOOSE matrix so that the subscribed Goose_1BOOL message from the RT target can be used as binary input to the OR logic presented in Fig. 18. Additionally, this GOOSE_NI1 representing the subscribed Goose_1BOOL message from the RT target can be used in the output matrix for the control of different LEDs (Light Emitting Diodes) or virtual outputs (VOs) with the solid dot connection. For example, Fig. 20 shows the connection of GOOSE_NI1 with the LED number E (LE) and VO1 of the VAMP relay in the output matrix. So, when the status of GOOSE_NI1 changes, the LED number E will illuminate. In the same way, Logic output 1 can be connected to perform different functions (T5).

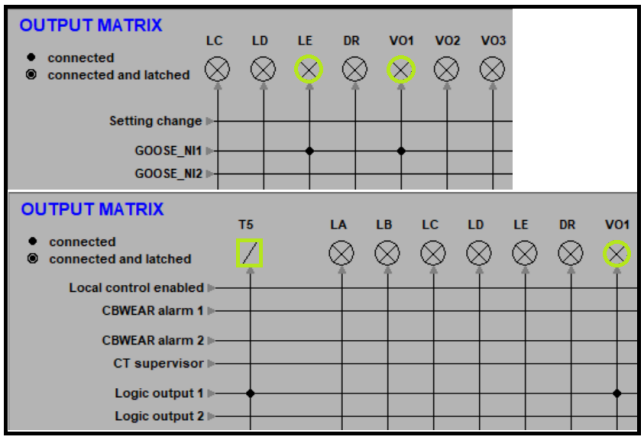

FIGURE 20. The connection of the subscribed GOOSE_NI1 and logical output 1 in the "Output Matrix."

After completing the configuration of the IEC 61850 GOOSE protocol with the VAMPSET software, all new configured settings can be written to the VAMP relay using the "Communication > Write All Settings to Device" command. The configuration settings can be saved in "AnyName.vf2" file for future use. Moreover, ICD file can be created for use inside the GOOSE Subscriber block of the RT-LAB as discussed earlier. Using the VAMPSET interface, the real-time Goose_1BOOL subscription by the VAMP relay can also be monitored from the "GOOSE Subscriber: Data Points," "Logic" and the "Output Matrix" menus with a successful Ethernet link connection. For real-time monitoring "Enable continuous updating" and "Sync time and date from computer" should be activated. The time stamp information about the subscribed GOOSE messages can be observed in the "Event Buffer" menu of the VAMPSET interface.

D. THE REAL-TIME HIL TESTING OF THE IEC 61850 GOOSE PROTOCOL

In this subsection, the testing of the VAMP relay performed using a Boolean signal representing the actual fault detection/pickup signal "Yes" (signal status = 0) of the OC relay at CB1 location (Fig. 6) is described. During this test, the VAMP relay was time synchronized with the computer time and date using VAMPSET interface. The fault detection signal "status = 0" is published by the OPAL-RT target as GOOSE_1BOOL message from its Ethernet port eth0 which is subscribed by the VAMP relay and used for OR logic (Fig. 18) created inside the VAMP relay. The logic output 1 of the OR logic is published back as GOOSE_2BOOL message by the VAMP relay which is then subscribed by the OPAL-RT target through its Ethernet port eth1 and saved in OpWriteFile. It means the testing procedure of Fig. 21 is followed assuming

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OPAL-RT located at CB1, and the VAMP relay located at CB2.

The round-trip time delay ($t_{RTT} = t_{25}$) for the status change consists of seven individual delays according to (1) [106]:

$$t_{RTT} = t_{25} = t_{23} + t_{34} + t_{45} \quad (1)$$
$$t_{23} = t_{out\ TARGET} + t_{net\ Goose\_1BOOL} + t_{in\ HUT} \quad (2)$$
$$t_{34} = t_{app\ LOGIC} \quad (3)$$
$$t_{45} = t_{out\ HUT} + t_{net\ Goose\_2BOOL} + t_{in\ TARGET} \quad (4)$$

Where, t_{25} is the round-trip time delay between events 2 and 5 (Fig. 2), t_{23} is the time delay between events 2 and 3, t_{34} is the time delay between events 3 and 4 and t_{45} is the time delay between events 4 and 5 in Fig. 2, $t_{out\ TARGET}$ is the delay by RT target to publish Goose_1BOOL on the Ethernet network, $t_{net\ Goose\text{-}1BOOL}$ is the delay of the Ethernet network until Goose_1BOOL message is available at the HUT (VAMP relay), $t_{in\ HUT}$ is the delay by the HUT to subscribe to Goose_1BOOL message as GOOSE_NI1, $t_{app\ LOGIC}$ is the delay of the OR logic to generate Logic output1 using GOOSE_NI1, $t_{out\ HUT}$ is the delay by the HUT to publish the Logic output1 via Goose_2BOOL message, $t_{net\ Goose\text{-}2BOOL}$ is the delay of the Ethernet network until Goose_2BOOL message is available at RT target and $t_{in\ TARGET}$ is the time taken by RT target to subscribe to Goose_2BOOL message, extract the information and write it on OpWriteFile for recording (Fig. 21).

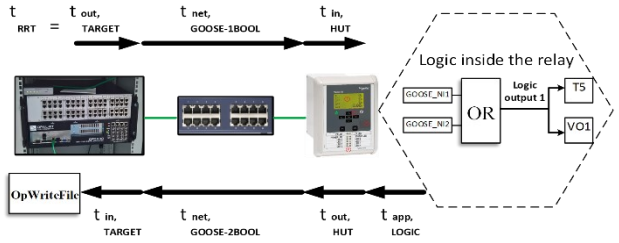

FIGURE 21. The round-trip time delay (t_{RTT}) estimation with real-time testing.

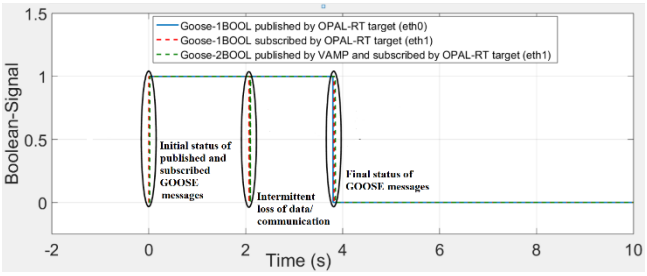

FIGURE 22. The published and subscribed fault detection Boolean GOOSE signals saved in OpWriteFile.

It is a hard task to estimate each of the seven individual non-deterministic time delays mentioned in (1)-(4) because the time stamp information at the individual input and output stage of each device including the RT target, the Ethernet switch, HUT and even at the logic implemented inside the HUT is required for it. However, the time stamp information is only available at the HUT, and it is available during the GOOSE subscription stage just to indicate at which clock time this signal has been updated in the "event buffer." The only exception is the estimation of time delay t_{TARGET} for one way GOOSE publication and subscription by the OPAL-RT target which includes three delays $t_{out,\ TARGET}$, $t_{net\ Goose\text{-}1BOOL}$ and $t_{in\ TARGET}$ and can be estimated by publishing the GOOSE signal from one Ethernet port (eth0) of the target and subscribing to the same GOOSE signal from other Ethernet port (eth1) of the same target. By recording both the published and subscribed GOOSE messages on OpWriteFile and matching the signals will give the estimation of t_{TARGET}. The similar estimation technique has been used for the estimation of t_{RTT} of the GOOSE message as shown in Fig. 21.

The actual fault detection signal at CB1 location does not repeat its status change multiple times but only once from the initial status of "No" (signal status = 1) to the final status of "Yes" (status signal = 0). Here, it should be noted that the "final status = 0" is the output of "NOT" gate implemented at the output of the OC relay at CB1 inside the RT model to trip the circuit breaker CB1 in case the fault is not detected by the OC relay at CB2. The final inverted status 0 of OC relay at CB1 acts as a trip command "Yes" for the CB, since in MATLAB/Simulink the CB trips with a "zero" input signal.

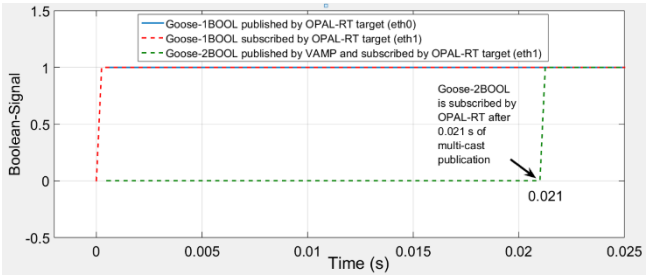

FIGURE 23. The initial status 1 of published and subscribed fault detection Boolean GOOSE signals.

It has been conventionally assumed through "OR Logic" implemented inside VAMP relay that if "No" fault is detected at the CB2 location then the Goose_2BOOL published by the VAMP relay will have the same final status 0 as that of the Goose_1BOOL at CB1 location (OPAL-RT target). Fig. 22 presents the published and subscribed fault detection Boolean GOOSE signals saved in OpWriteFile and plotted with MATLAB commands. In this test, a three-phase short-circuit fault is applied for a duration of 1s from the simulation time of 3 s to 4 s and the OC relay at CB1 is set to detect the fault at 3.8 s. This means the status of fault detection signal changes only at simulation time of 3.8 s. The fault detection status signal is published by OPAL-RT target via Ethernet adapter eth0 as Goose_1BOOL message (blue color) and subscribed by OPAL-RT target via Ethernet adapter eth1 as Goose_1BOOL message (red color) for the estimation of the delay t_{TARGET}. The subscribed Goose_1BOOL message is published back by the VAMP relay and subscribed by the OPAL-RT target as Goose_2BOOL (green color) for the

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estimation of the round-trip time (t_{RTT}). The initial status 1 of the Boolean signal, indicates "No fault detection" and the final status 0 of the Boolean signal indicates "Yes fault detection."

The initial status 1 for the "No fault detection" signal from the start of the RT simulation at Time = 0 s till the round-trip back from the VAMP relay to the OPAL-RT target at Time = 0.021 s is zoomed out as shown in Fig. 23. The time from 0 to 0.021 s is the round-trip time (t_{RTT}) of the initial status 1 of the "No fault detection" signal. The delay $t_{TARGET\ St1}$ of the initial status 1 (red color) is very small and hardly distinguishable from the original published signal (blue color). The OPAL-RT target continuously publishes the current status of the Boolean signal after every time step (Ts) of the simulation and after the publication and subscription the signal is being recorded on OpWriteFile blocks. The status of the Goose_2BOOL signal (green color) from the time 0 to 0.021 s (Fig. 23) does not indicate the status changed to status 0. It, however, means that during the time 0 to 0.021 s, Goose_2BOOL published by VAMP relay is absent (not yet subscribed) at the OPAL-RT target, which by default is recorded as the "0" inside the MAT file of the OpWriteFile block. Therefore, by setting the initial delayed conditions starting after 0.021 s at the input of CBs, the false tripping of CB1 and CB2 during the initial simulation time up to 0.021 s can be avoided during the simulation.

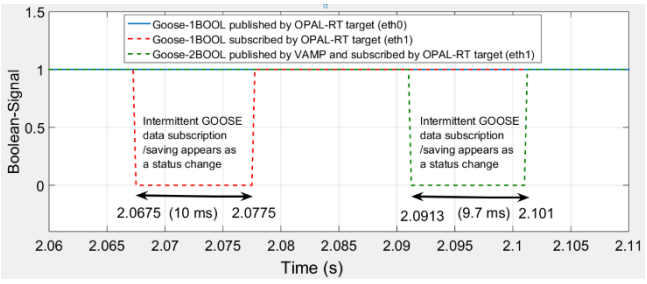

FIGURE 24. The intermittent/missing data recording of the subscribed Boolean GOOSE signals during the initial status 1.

The initial status 1 of the published and subscribed Boolean signals, starting from the simulation time of 0.021 s to onwards, should ideally remain the same till 3.8 s when the fault is detected by the OC relay at CB1. However, it can be seen from the Fig. 22 and more closely from Fig. 24 that there is some intermittency of the subscribed signals for about 10 ms. The data recording of both the subscribed signals Goose_1BOOL (red color) and Goose_2BOOL (green color) is missing and appearing as a changed signal status 0 at 2.0675 s of the simulation time. The intermittency of the initial status 1 of the subscribed Boolean signal happens only once but at different times of simulation during three tests and for different lengths of duration in each case. This has happened most probably due to the software bug in the OPAL-RT target or some loss of data packets but not from the relay model as the published signal in blue color is always continuous. The consequent false tripping of the CBs could be avoided in one way by introducing the monitoring of the continuity of the signal status for 15 ms or 20 ms at the inputs of the CBs inside the model and the signal should be assumed continuous if it is continuous for a duration of 15 ms or 20 ms. However, if the CBs are capable of resetting quickly with the status change during the simulation and the final results of the simulation are not affected then this intermittency can be easily ignored as done in this case.

After ignoring the intermediate discontinuity of the initial fault detection signal with status 1, the most important thing to observe is the behavior of the final status 0 of the signal after 3.8 s which is the actual fault detection event. The continuous behavior of the final status 0 of the Boolean signal, at simulation time 3.8 s onwards, is evident from the results of Fig. 25. The status change inside the model happens at 3.8 s, it is published as Goose_1BOOL message by the OPAL-RT target at 3.8027 s (blue color) and subscribed by the OPAL-RT target at 3.8223 s (red color), resulting in t_{TARGET} = 19.6 ms. The VAMP relay publishes Goose_2BOOL after subscribing to Goose_1BOOL and performing the OR logic which is ultimately subscribed by OPAL-RT target at 3.8510 s resulting in t_{RTT} = 48.3 ms. In this way, many tests were performed for the estimation of the round-trip time, Table III shows three selected best-case scenario testing results. The worst-case maximum round-trip time of t_{RTT} = 90 ms was observed for the same test case at another time of testing. The estimation of the round-trip time using the real-time HIL-testing will help to implement the IEC 61850 communication-dependent logically selective adaptive protection algorithm for AC microgrids proposed in [11].

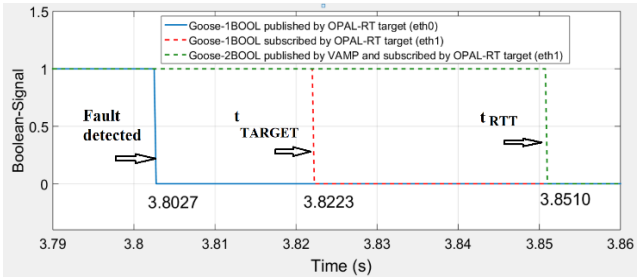

FIGURE 25. The final status 0 of published and subscribed fault detection Boolean GOOSE signals.

TABLE III
THE TIME DELAYS OF THE FINAL STATUS 0 OF THE PUBLISHED AND SUBSCRIBED GOOSE BOOLEAN SIGNALS IN THREE TESTS

Signal (Time delay)	Test-1	Test-2	Test-3	Average
Goose-1BOOL pub[2] by OPAL ($t_{out\ TARGET\ St0}$[4])	2.5 ms[1]	2.7 ms	2.7 ms	2.63 ms
Goose-1BOOL sub[3] by OPAL ($t_{TARGET\ St0}$)	19.5 ms	37.7 ms	17.3 ms	24.83 ms
Goose-2BOOL pub by VAMP sub by OPAL ($t_{RTT\ St0} = t_{25}$)	48.3 ms	52.5 ms	39.5 ms	46.76 ms

[1]ms = millisecond, 1 ms = 0.001 s, [2]pub = published, [3]sub = subscribed, [4]St0 = Status 0.

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E. THE RESULTS FOR IEC 61850 GOOSE PROTOCOL DEPENDENT ADAPTIVE PROTECTION

In this section, the results are presented for the IEC 61850 GOOSE protocol dependent adaptive protection of a radial AC microgrid (Fig. 6) and smooth transition to islanded mode operation using the centralized BESS after the short-circuit fault F1 at 2 km overhead line near the CB2 location. Additionally, the results also include the detection and the isolation of the short-circuit fault F2 at mid-point of a 1 km cable inside the islanded AC microgrid. Due to the inherent limitation of both the VAMP relay and the OPAL-RT target (IEC 61850 ICD file) to publish and/or subscribe to a maximum of two Boolean signals at a time, only the results of fault F1 are dependent IEC 61850 GOOSE communication protocol. However, the test can be repeated, and very similar results can also be obtained for the fault F2. The inclusion of the fault F2 results is particularly important to present the behavior of DERs during the islanded mode with centralized BESS and during the facility island mode of the PV system without BESS.

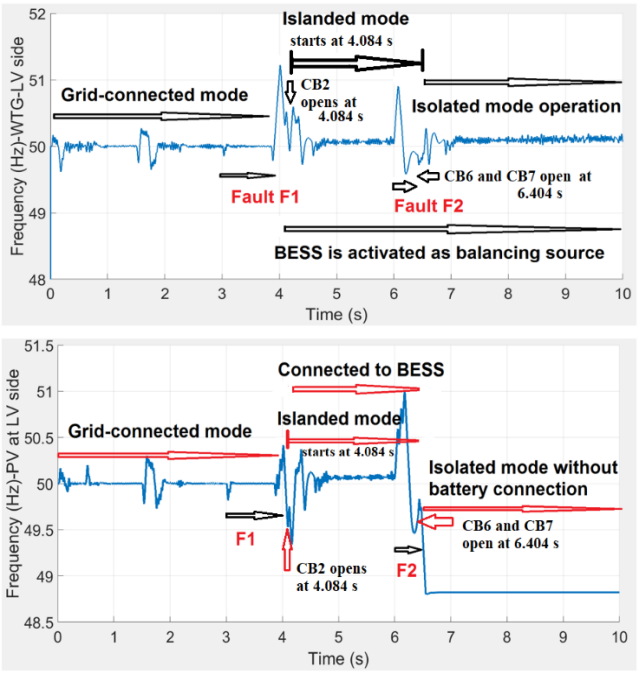

FIGURE 26. **The frequency (Hz) of DERs before and after the fault F1 in grid-connected mode and before and after the fault F2 in the islanded mode: WTG (top), PV system (bottom).**

The estimation of the round-trip time (t_{RTT}) in the previous section was important because using the subscribed Goose_2BOOL signal the centralized BESS is activated as well as CB1 and CB2 are also tripped to isolate the AC microgrid from fault F1 completely and start the islanded mode. The behavior of the frequency at the LV-side of the WTG and the PV system during the faults F1 and F2 and during the different operational modes is presented in Fig. 26. As it is evident that the frequency at DERs is well maintained around 50 Hz during the grid-connected mode and in the islanded mode with the centralized BESS after the fault F1. During the isolated mode of operation after the fault F2 when the islanded MV system and the islanded LV system (Fig. 6) are isolated, the frequency of the WTG remains well maintained around 50 Hz due to the presence of the centralized BESS. However, the frequency of the PV system is dropped below 49 Hz in the isolated mode of operation either due to the absence of any BESS in the islanded LV system or some control problem with the PV model or the PLL block, however, it remains well above 48.5 Hz. The PV system can operate up to 90 minutes for the frequency range of 48.5-49 Hz according to the European grid code EN 50549-1-2019.

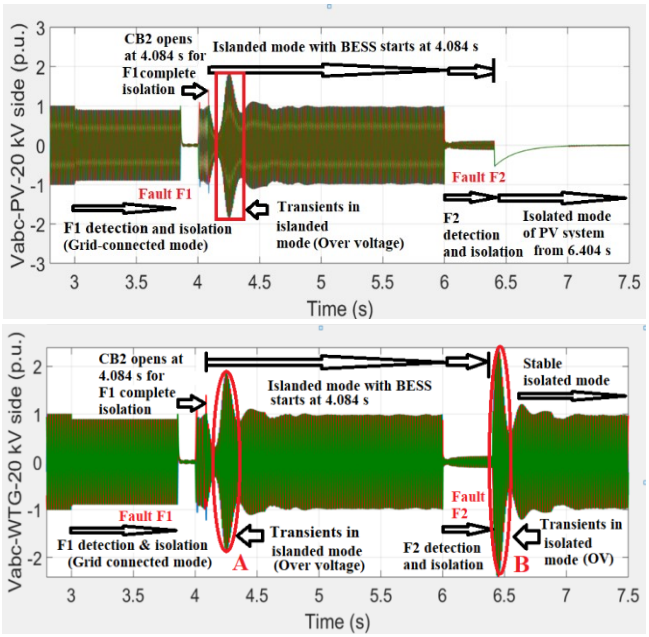

FIGURE 27. **Three-phase voltage (p.u.) of DERs before and after the fault F1 in grid-connected mode and before and after the fault F2 in the islanded mode: 20 kV side of WTG (top) 20 kV side of PV system (bottom).**

The behavior of the voltage on 20 kV side of the WTG and the PV system during the faults F1 and F2 and during the different operational modes is presented in Fig. 27. As it can be seen that during the 3Ph short-circuit fault F1 with R_f = 5.001 Ohm in the grid-connected mode, the voltage at the connection points of DERs is decreased to only 0.9 p.u. until the fault F1 is isolated by CB1 tripping at 3.851 s. From the simulation time of 3.851 s to 4s the voltage at the connection points of DERs is consequently decreased to the minimum (near to zero) value due to the CB1 tripping indicating the loss of the main grid. This minimum voltage for a duration of 149 ms has happened due to the delayed CB2 transfer trip implementation in the RT simulation discussed later in the following paragraph. At the simulation time of 4 s, the fault naturally disappears and the voltage at the connection points of DERs is restored to the normal range of 0.9 p.u. because the active fault duration of only 1 s from the simulation time of 3 s to 4 s is considered for the fault F1. The CB2 trips at simulation time of 4.084 s to completely isolate the fault F1.

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The activation of the centralized BESS is implemented with the opening status signal of the CB2. Therefore, the BESS also starts as the grid-forming source at 4.084 s to support the seamless transition to the islanded mode without the disconnection of DERs.

At the start of the islanded mode with centralized BESS, there is some undervoltage followed by a transient overvoltage region marked as area A (Fig. 27) which may result in the unstability of the islanded mode in case the overvoltage protection of DERs is activated in this region. Therefore, DERs should have high voltage ride through (HVRT) or overvoltage ride through (OVRT) capability to remain stable and not disconnect due to overvoltage during this short transition period of about 5 cycles (100 ms) in the islanded mode. The same HVRT is required during the isolated mode after the fault F2 in the islanded mode marked as area B in Fig. 27 (top). From the simulation time of 4.25 s to onwards, a very stable voltage at the connection points of DERs is achieved in the islanded mode. During the islanded mode, a three-phase short-circuit fault F2 with R_f = 0.001 Ohm is applied at simulation time of 6 s. As can be seen from Fig. 27, that the voltage at the connection points of DERs is decreased to minimum (near to zero) due to the lower fault resistance during F2 compared with the same during F1.

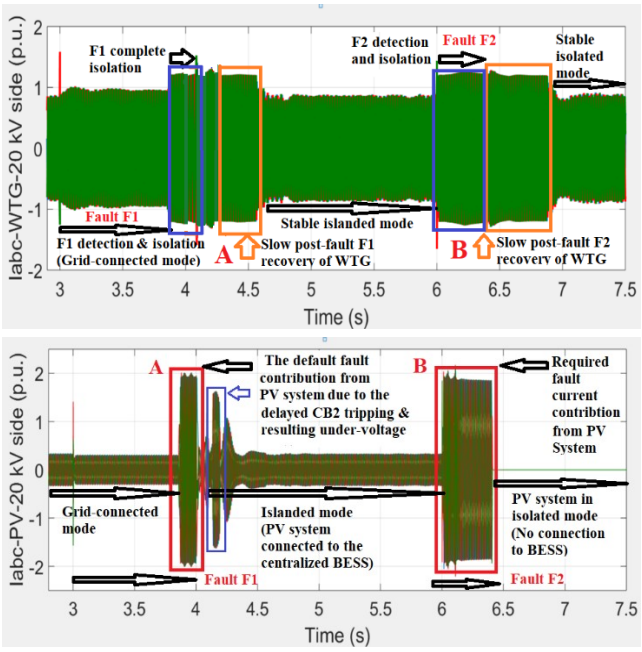

FIGURE 28. **Three-phase current (p.u.) of the DERs before and after the fault F1 in grid-connected mode and before and after the fault F2 in the islanded mode: 20 kV side of WTG (top) 20 kV side of PV system (bottom).**

The fault F2 is detected by OC relay at CB6 and isolated at 6.404 s by tripping CB6 and transfer tripping CB7. This will result in two island systems within the islanded AC microgrid: MV island system with the WTG, the BESS and 2 MW load; LV island system with only the PV system and 0.4 MW load operating without BESS. At the simulation time of 6.5 s, MV island system achieves a stable isolated mode of operation while LV island system lost the voltage of the centralized BESS at its 20 kV connection point (Fig. 27 (bottom)). The PV system in the LV island which is a facility island can only operate with the grid-forming control for the continuity of supply to the LV load. The voltage and current at the LV load before, during and after the faults F1 and F2 can be observed from the figures given in the Appendix.

The behavior of the current on 20 kV side of the WTG and the PV system during the faults F1 and F2 and during different operational modes is presented in Fig. 28. As it is evident from Fig. 27 that during the fault F1, the voltage at the connection point of DERs is only decreased to 0.9 p.u., hence both the WTG and the PV do not provide the fault current contribution of 1.2 p.u. and 2 p.u. respectively until CB1 is opened. This means the grid-side voltage does not decrease to 0.5 p.u. or less in order to trigger the fault current contribution or LVRT of DERs during the fault F1. However, after the communication-dependent detection and isolation of the fault F1 and opening of CB1 at simulation time of 3.851 s, the grid-side voltage is lost at the connection points of DERs. This consequently triggers the fault current contribution from DERs (LVRT capability), and both the WTG and the PV system provide a default maximum fault current contribution until CB2 is also opened at 4.084 s for a complete F1 isolation (area A, Fig. 28).

The default fault current contributions from the WTG (area A in blue color) in Fig. 28 (top) and from the PV system (area A in red color) in Fig. 28 (bottom) for a duration of 233 ms during the time 3.851 s to 4.084 s is the result of the delayed transfer trip of CB2. Actually, the CB2 transfer trip is implemented in a way that the subscribed Goose_2BOOL signal from the SM_Grid1 is first transferred to the console subsystem SC_MG1 and then from the console subsystem SC_MG1 transferred to the SS_WTG_PV1 subsystem where CB2 is connected. Doing this results in a delayed CB2 transfer trip due to the asynchronous connection between the console subsystem SC_MG1 and the computation subsystem SS_WTG_PV1. But, if the transfer trip of CB2 is implemented like CB1 tripping using a separate Goose_2BOOL subscriber block (Fig. 13) also in the SS_WTG_PV1 subsystem of the RT model then the extended CB2 opening delay will not happen and both CB1 and CB2 would trip simultaneously at 3.8510 s in the RT simulation. Consequently, the undervoltage and fault contribution time between 3.851 s and 4 s in Fig. 27 and Fig. 28, respectively could be decreased or avoided.

During the initial voltage dip period from the simulation time 4.084 s and 4.25 s after the successful islanding, both the WTG and the PV system also provide the LVRT and fault contributions (the area between the blue and orange area A rectangles in Fig. 28 (top) and area A in blue color in Fig. 28 (bottom)). By comparing the fault current contribution and dynamics of the WTG and the PV system models during the fault F1 and F2, it can be seen from Fig. 28 (top) that the WTG continues providing fault current for an additional time even after the voltage is restored to the normal value (area A and

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area B in orange color). The PV system, on the other hand, provides the fault current contribution only when it is required (Fig. 28 (bottom) area A, area B in red color) and immediately gives the normal current after the voltage is restored above 50% of the nominal value. The WTG model has a very slow post-fault current recovery compared with the PV system. Therefore, the change of adaptive lower setting group of OC relays will be delayed in the islanded mode by some time after the successful islanding. The generic model of the WTG with good dynamic behavior would, however, avoid the delay to the change of adaptive lower setting group as observed previously in [11].

The three-phase current in p.u. at the CB2 location during the grid-side fault F1 is presented in Fig. 29. This will help understand the complete fault F1 isolation. Fig. 29 shows that after the opening of CB1 at 3.851 s, CB2 will still carry a current fed by the WTG and the PV system and the fault F1 will remain charged by this current until either the fault disappears or CB2 is also opened. After the opening of CB2 at 4.084 s, the fault current disappears from the CB2 location indicating complete fault isolation. The persistence magnitude of current although lower than the fault current after the disappearance of the fault F1 and before the opening of CB2 appearing between simulation time of 4 s and 4.084 s in Fig. 29 is there because of the fault current contribution from DERs which is fed to the 100 kvar capacitor bank (Fig. 8). In the practical situation considering the centralized relay at CB1, if CB1 opens at 3.851 s, then with the one-way GOOSE transfer delay of 10 ms CB2 will open at 3.881 s assuming CB2 as one cycle CB. Thus, the completion of the IEC 61850 GOOSE communication dependent selective fault detection and isolation within 100 ms is possible after adding 20 ms of fault detection which closely matches with the "10 ms GOOSE message algorithm" proposed in [11] and reproduced in Fig. 2.

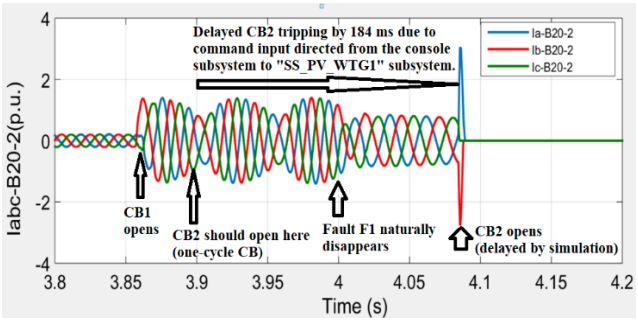

FIGURE 29. **Three-phase current (p.u.) at CB2 location during the grid-side fault F1.**

Considering the relays at CB1 and CB2 as decentralized relays, then CB2 will trip first after receiving "YES" fault detection Goose_1BOOL from the OC relay at CB1 as there is "NO" fault signal readily available at CB2 location because with the higher setting group the OC relay at CB2 does not pickup. So, the OC relay at CB2 will receive Goose_1BOOL, perform the OR logic and send trip command to CB2 meanwhile publish the Goose_2BOOL "NO" fault signal. This procedure will open CB2 completely at 3.851 s which also includes the one cycle duration (20 ms) of CB2 opening (Fig. 3). The OC relay at CB1 will issue trip command to CB1 at 3.851 s after receiving Goose_2BOOL "NO" fault signal and CB1 will open completely within 20 ms at 3.871 s resulting in complete fault detection and isolation in just 91 ms after adding 20 ms of fault detection, which is even faster than the "10 ms GOOSE message algorithm."

However, with a round-trip time (t_{25}) of 90 ms, the worst-case scenario, the "20 ms GOOSE message algorithm" looks more suitable and with the decentralized/centralized architecture, complete detection and isolation of fault F1 will happen around simulation time of 3.92-3.93 s, in just about 120-130 ms after the fault detection at 3.8 s. Again, it confirms the practical implementation of the "20 ms GOOSE message algorithm" which also assumes 130 ms for complete fault detection and isolation. The rest of the results are presented in the Appendix of the paper.

V. DISCUSSION

The communication will be a necessary and integral part of the future smart electric grids and microgrids. The IEC 61850 communication provides the standardized protocol for the exchange of the digital as well as analog type of data among IEDs of different vendors using the Ethernet link as the most reliable and fast medium. The implementation of different control and protection functions through logic selectivity implemented inside IEDs will be a more common trend. To prove the reliability and dependability extent of communication-dependent control and protection functions for example, adaptive protection [11], the HIL simulation testing of actual IEDs in real-time is necessary. The adaptive protection is the new requirement for microgrids which can be implemented with the centralized communication architecture, the distributed communication architecture or even with the hybrid communication architecture using both the centralized and the distributed architecture.

The round-trip testing of communication is generally used for the estimation of the one-way communication delay and can be carried out using different methods for example [106]. However, the dependency on the round-trip delay which involves various inherent delays has rarely been considered for a communication-dependent logically selective adaptive protection. Previously, the estimation of the round-trip delay was done in [106] for the loss of mains detection and transfer trip of DERs using IEC 61850 protocol. However, the method neither considered LVRT of DERs nor provided the complete interactive environment close to the reality in which the consequences of the delayed or missing tripping like the behavior of DERs including the frequency and voltage stability can be found. The HIL simulation testing provides the results close to the actual implementation and therefore can be widely acceptable as a "proof of concept" within its own limitations and additional challenges. This paper provides the

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results for the implementation extent of the communication-dependent logically selective adaptive protection proposed in [11] using the HIL simulation testing. The results reveal that the previously proposed adaptive protection algorithm with the assumed conditions in the offline simulations is also giving the similar results in real-time HIL testing environment. Therefore, it can be implemented in the practical microgrids irrespective of the radial or looped network configuration. The method is capable of being extended to other types of signals like analog signals for other types of protection functions/applications with the similar or comparative results.

It should here be noted that the communication-dependent logically selective adaptive protection algorithms presented in Fig. 2 and Fig. 3 includes both the variable and fixed time delays. In this paper, only the variable time delays for a two-way communication (t_{25}) for the centralized architecture (Fig. 2) are estimated using the real-time HIL testing. The fixed time delays include the delays for the fault detection and opening times of the CBs which greatly depend on the method of fault detection and the type of CB used. In this paper, the instantaneous tripping of CB1 (ideal-case) is used and CB2 tripping is delayed only due to RT simulation model arrangements (worst-case). The fixed time delays of CB tripping can however easily be adjusted according to Fig. 2 by introducing 20 ms time delay at CB1 and 60 ms time delay at CB2 with the subscription of Goose_2BOOL message (event 5) independently in SM_Grid1 and SS_WTG_PV1 subsystems in the RT model as explained previously. This is somewhat confusing due to the fact that only one and the same GOOSE message (Goose_2BOOL) is used for tripping both the CB1 and CB2 in the RT model. In practical situations, the OC relay at CB1 will subscribe to the updated Goose_2BOOL published by the OC relay at CB2 and publish Goose_1BOOL after tripping CB1. In the same way, the OC relay at CB2 will subscribe to the updated Goose_1BOOL published by the OC relay at CB1 and publish Goose_2BOOL after tripping CB2. Each relay may even publish two independent and the unique Boolean GOOSE messages one for the fault detection information and the other for CB tripping. This all depends on the capability of the relays to publish and subscribe to multiple GOOSE messages. Moreover, the fault detection signal (Goose_1BOOL) could be published right after 20 ms of the fault F1 at 3.02 s instead of 3.8 s as done in the HIL testing of this paper to get the results more aligned with the algorithm presented in Fig. 2.

The adaptive lower setting group-based fault detection and isolation although not used in this HIL testing case, but it is an integral part of the algorithm. For example, the algorithm can be repeated for the first fault to be F2 between CB6 and CB7 and the second fault to be F3 at LV load where F3 can only be detected with the lower setting groups assuming the PV provides the fault current contribution of 1.2 p.u. and the grid-connected or BESS-connected islanding pickup setting of the OC relay at LV load (CB8) is 2.25 p.u. In this situation, OC relay at CB8 of LV load (Fig. 6) will change its pickup settings after CB7 tripping (event 8 in Fig. 2). The HIL testing verifies that the seamless transition to the islanded and isolated modes is possible using the reliable, fast and dedicated communication link and the BESS in the islanded sections. However, the Boolean signal integrity should be maintained and the intermittent loss of data for a duration longer than 10-20 ms need to be avoided.

The Boolean signal continuity check of "status 0" (Fig. 30) for a duration longer than 20 ms after the GOOSE subscription will ensure the prevention of wrong tripping by the relays due to intermittent data loss. This signal continuity check delay when added as security delay in the events 3, 5 and 7 of Fig. 2 will obviously extend the overall duration of the proposed algorithm and therefore the stringent LVRT curve of DERs with 250 ms will be required. Due to the use of LAN connection in this HIL testing with a lot of other data traffic in the network, the results produced are close to the realistic substation automation environment with many IEDs and a lot of GOOSE data traffic. This paper will be a good reference for further applications and improvements of the communication-dependent logically selective adaptive protection.

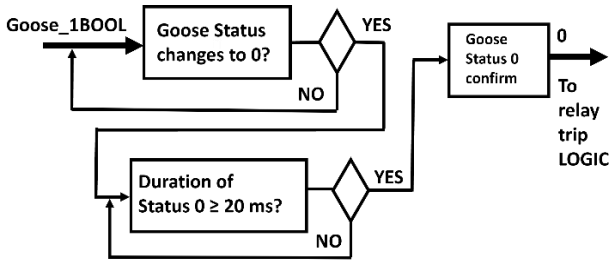

FIGURE 30. Boolean signal continuity check of status 0.

VI. CONCLUSIONS

The real-time HIL testing has been carried out using the actual digital relay and the RT target for the verification of the adaptive protection using the IEC 61850 GOOSE protocol which was previously proposed in [11] using the offline simulations. The results look promising, and the previously assumed conditions are very close to RT simulation results. A dedicated, fast and reliable Ethernet link will ensure the implementation of the proposed adaptive protection and seamless transition to the islanded and isolated mode could be realized with a centralized or distributed control and communication architecture. A centralized BESS will help maintain the voltage and frequency stability for the seamless transition within 150 ms or 250 ms LVRT curve of DERs. The monitoring of status 0 of the Boolean signal will add security to the relay and avoid the unnecessary tripping of the relay during the brief communication discontinuity or loss of data. The similar data handling and monitoring concept inside the relay can also be applied for the analog type of signals. The proposed method can be readily applied to other control and protection applications e.g., in AC microgrids with looped networks.

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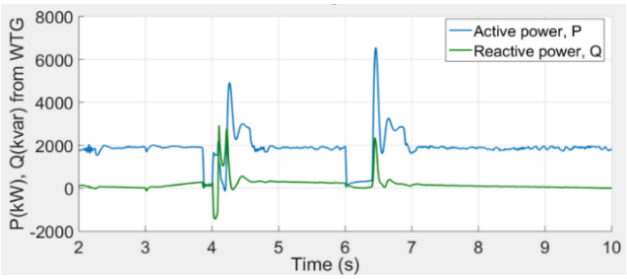
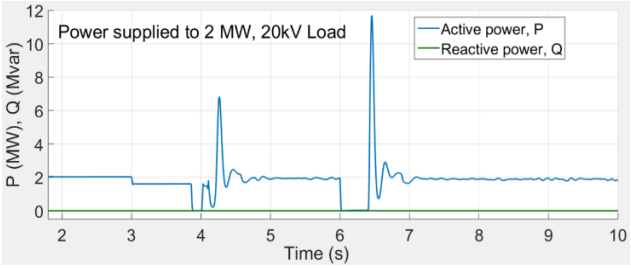
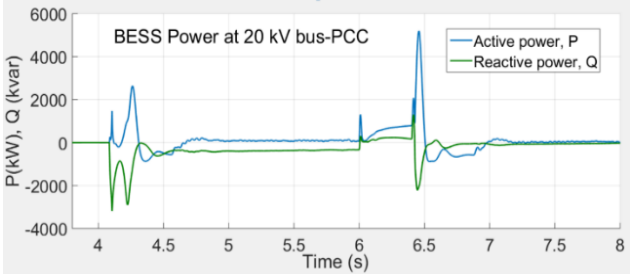
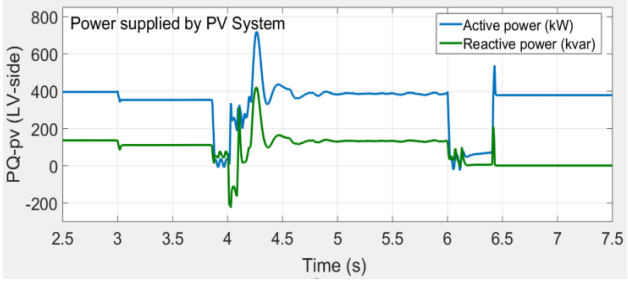
APPENDIX

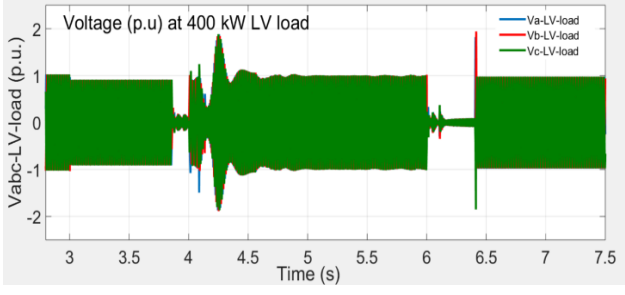
Additional results:

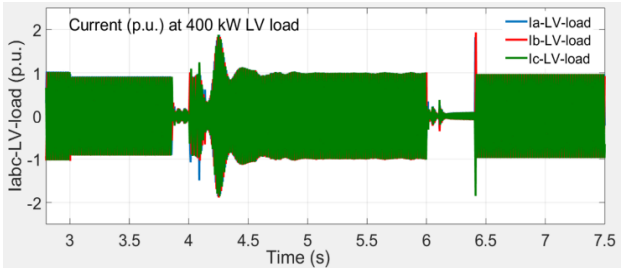












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