Low-Cost DC BIST for Analog Circuits: A Case Study

Pablo Petrashin, Carlos Dualibe, Walter Lancioni, Luis Toledo.

***Abstract*—This paper presents a DC analog testing technique based on a simple voltage comparison of the highest sensitivity node, which is found by simulation. The technique is a structural, fault driven testing approach and can be applied to any analog circuit with very few extra added circuitry. A proof of concept has been implemented in a 65nm low-voltage transconductor, showing good fault coverage for both catastrophic and parametric faults.**

***Index Terms*— DFT, BIST, analog testing.**

I. INTRODUCTION

NOWADAYS and mainly due to the growing presence of analog and mixed signal systems on integrated circuits, the analog test has become an unavoidable part of the whole test procedure. It is because of this fact that research continues to be made in order to make the analog test more efficient.

There are usually two ways of looking at analog testing namely, Fault Driven Test and Specification Driven Test. In the latter, analog and mixed-signal circuits require verification of a large number of specifications, and sometimes, checking all of them lead to prohibitive testing times on high cost automated test equipment [1]. Because of this fact, many efforts are being made in fault driven testing.

One of the most commonly observed physical defects are permanent faults [2], which can be classified into catastrophic faults (open, short or stuck-at) and parametric faults (variations around nominal values due to disturbance in the process parameters).

Several ways of testing structural faults were proposed trough the years. One of the most widely used techniques is IDDq testing [3], because of its inherent simplicity and high reliability. However, this technique seems be strongly limited when used in circuits implemented in deep submicron technologies [4, 5]. Another useful technique called oscillation based test (OBT) was introduced in 1995 [6], and applied later to analog CMOS circuits with considerable success [7, 8]. In the latter, a set of exhaustive simulations was performed showing a good fault coverage rate. The OBT technique is a good example of a Defect-Oriented Testing methodology, which allows to considerably reducing the test time compared to conventional (functional) test approaches. The main idea behind OBT consists in converting the Circuit Under Test (CUT) into an oscillator and using some oscillation parameters (amplitude, frequency, DC level, etc.) as the test deciders. Indeed, this a vectorless BIST technique specially suited for mixed-signal integrated circuits. It is assumed that a fault in the CUT will produce alterations in the oscillation parameters and consequently they can be used as test attributes for determining if a given circuit is faulty or fault-free. Besides the simple idea behind OBT, difficulties associated with oscillation frequency dispersion [7, 12], the inherent circuit complexity and testing time demanded for on chip measurement a of frequency not always results in a convenient OBT BIST implementation.

Several DC testing methods where proposed besides IDDq [9, 10]. Despite the simplicity of those ideas, their implementation are not straightforward, requiring sometimes costly circuitry overhead as well as input stimuli. As stated in the reference, DC testing is inexpensive if compared against other testing methods and it is particularly suitable for detecting catastrophic faults. We propose in this paper a very simple idea, based on a DC voltage comparison of the most sensitive-to-faults node, which is detected by previous simulations. We will show that the proposed vectorless technique is easy to implement and has good fault coverage, rendering it suitable for BIST implementation.

The paper is organized as follows: in section II the technique is explained. In section III and IV, the idea is applied to a low-voltage transconductor designed in a 65nm as a case study. Simulation results are presented in section V. At the conclusions we discuss the presented idea highlighting its pros and cons.

II. THE PROPOSED TESTING TECHNIQUE

The underlying idea of the technique is based on the correlation that should exist between the voltage at a given node of the circuit and a fault present in it. Indeed, this correlation exists in terms of the "Thevenin equivalent" calculated between the chosen node and ground. Assuming this as a fact, the point giving the best fault coverage (FC) can be found by simulation.

The main idea consists in checking all node's voltages with respect to ground, with and without injecting the faults (i.e. shorts and opens). Once the DC simulation of all faults is accomplished, the output file generated by the simulator

Manuscript received October 26, 2012.

Pablo Petrashin, Walter Lancioni and Luis Toledo are with the Microelectronics Laboratory, Catholic University of Cordoba (Universidad Católica de Córdoba - UCC). Camino a Alta Gracia Km 10, (5016) Córdoba, Argentine (phone: +543514938089; fax: +543514938080; e-mail: lancioni, toledo, petra@uccor.edu.ar).

Carlos Dualibe is with the Electronics and Microelectronics Department (SEMi), Faculté Polytechnique - Université de Mons (UMons), 31 Boulevard Dolez, (7000) Mons, Belgium; (e-mail: fortunato.dualibe@umons.ac.be)

can be analyzed by means of a software (i.e. implemented with MATLAB™) in order to look for the node (or nodes) giving the best FC. Once the latter is (are) chosen, the testing circuit shown in figure 1 should be connected to it (them) for implementing the BIST. It should be remarked that the measure should always be done with the input (or inputs) of the CUT passivated.

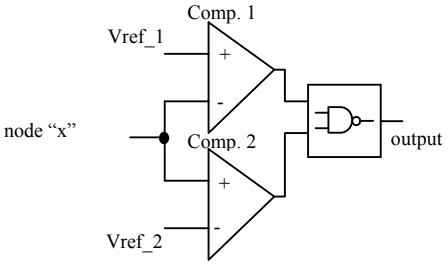

Figure 1. Block diagram of the proposed checker

The input testing node "x" is led to a "window comparator" which detects whether the voltage node under measurement is or is not within the allowed tolerance which can be adjusted through Vref_1 and Vref_2. In the case depicted in figure 1, the output will be at a high level when the voltage is outside the selected window (means the circuit is faulty) or at a low voltage level in the opposite case. A control pin could be easily added in order to deactivate the test mode during normal operation. Since the input of the checker circuit is usually a high DC-impedance MOSFET gate, this method is minimally invasive. If the CUT bandwidth is affected (i.e. because of the MOS gate capacitors connected to the test node) the connection to the checker can be implemented via two pass transistors. In any case, at normal mode the checker circuit should be disconnected from power supply for power consumption reduction.

The implementation shown in figure 1 should not be very area-consuming. This allows the designer to implement one checker for each circuit under test (CUT). However, if the size becomes important, an appropriate multiplexing strategy can be implemented in order to use just one checker for all CUTs.

III. TRANSCONDUCTOR TOPOLOGY

For validating this idea on a real CMOS CUT, a 65nm transconductor is adopted as a case study. The circuit of the proposed transconductor is shown in figure 2. It is a low-voltage topology [11] designed for a nominal 1uS transconductance.

In Figure 2, all schematically redundant nodes adopt the name of the reference node followed by an index starting by one. This redundancy is introduced because of the need of differentiating each redundant node from the others upon open fault injections. Table I shows the names for the reference nodes and their corresponding redundant ones. The whole set of defined nodes make possible to characterize 1258 short circuit faults and 28 open circuit faults.

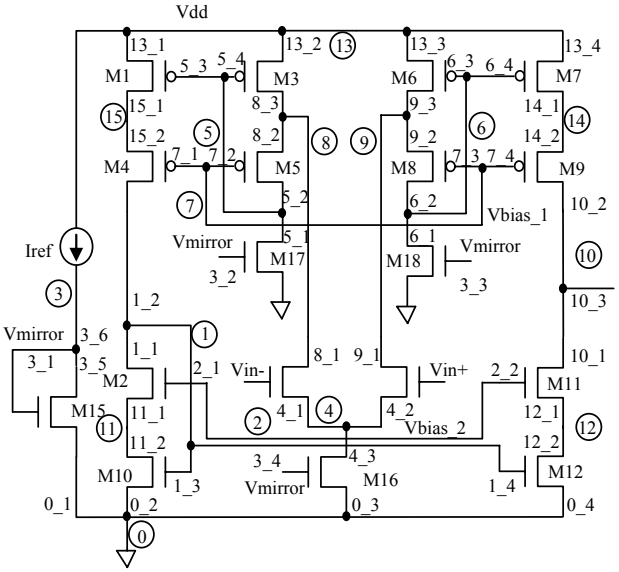

Figure 2. Block diagram of the circuit under study.

IV. FAULT MODELING

Traditionally, the efficiency of an analog testing technique has been evaluated, at structural-level, by using single-catastrophic and single-deviation fault models. In this way, it is possible to use the well-known metric called fault coverage (FC) for qualifying the test. In this work, we focused our attention on catastrophic faults at both, device and circuit level.

Since the layout level of the circuit is not available, an exhaustive faults list is generated from the schematic, considering at first only catastrophic faults. This list includes all possible open and short faults with the sole exception of gate contact open fault because it has no effects on the simulation due to the high impedance of the MOSFET´s gates.

TABLE I. REFERENCES FOR MAIN AND REDUNDANT NODES.

main node	schematically redundant
0	0_1, 0_2, 0_3, 0_4
1	1_1, 1_2, 1_3, 1_4
2	2_1, 2_2
3	3_1, 3_2, 3_3, 3_4, 3_5, 3_6
4	4_1, 4_2, 4_3
5	5_1, 5_2, 5_3, 5_4
6	6_1, 6_2, 6_3, 6_4
7	7_1, 7_2, 7_3, 7_4
8	8_1, 8_2, 8_3
9	9_1, 9_2, 9_3
10	10_1, 10_2, 10_3
11	11_1, 11_2
12	12_1, 12_2
13	13_1, 13_2, 13_3, 13_4
14	14_1, 14_2
15	15_1, 15_2

The reference node and its schematically redundant nodes are connected at the same potential. Obviously, it is impossible to detect a behavioral difference between them at simulation level. Owing to this fact, for the simulations of the shorts, only the reference nodes in Table I have been considered. Certainly, schematically redundant nodes are not necessarily physically redundant if the particularities of the circuit layout are considered; so, different behaviors of the CUT could be obtained if an open fault is located in different schematically redundant nodes. Hence, for open faults all nodes defined in the table are taken into account.

Fault simulations were carried out using SPICE by considering only single fault injection. In order to permit further comparison with other works, opens were modeled with a 10 MΩ resistor whereas the shorts with a 10Ω resistor. The circuit complies with the IBM 65nm CMOS technology.

V. SIMULATION RESULTS

Simulations were carried out over process at five different corners, i.e. Typical-Typical (TT), Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF) and Slow-Slow (SS) models. Like this, a group of five results are shown at all tables.

The OTA was configured as a follower with Vint+ connected to the analog ground. Supported on an automated simulation SPICE setup, the whole set of faults were injected and simulated. Following, a home-made MATLAB script was run in order to find the fault coverage rate related to a specific node for locating the node that gives the best FC. Table II shows the FC for all the nodes for the different technology corners.

TABLE II. SHORT CIRCUIT FAULT COVERAGE FOR DIFFERENT TECHNOLOGY CORNERS AND NODES.

Node	Fault Coverage				
	TT	FS	FF	SF	SS
Node 1	45,79%	64,71%	51,67%	38,16%	46,10%
Node 2	7,31%	5,88%	7,95%	7,47%	5,88%
Node 4	91,89%	95,87%	83,70%	87,60%	94,12%
Node 5	78,14%	73,05%	72,10%	85,61%	77,98%
Node 6	45,55%	45,55%	39,98%	65,42%	56,20%
Node 7	11,76%	11,76%	9,86%	11,13%	11,76%
Node 8	24,64%	24,64%	22,73%	23,69%	23,69%
Node 9	19,40%	17,17%	16,22%	18,12%	18,44%
Node10	86,80%	87,12%	81,24%	86,65%	89,03%
Node11	88,47%	92,45%	87,52%	80,52%	89,43%
Node12	94,28%	94,59%	89,59%	88,47%	95,71%
Node14	15,26%	16,85%	16,38%	14,79%	16,06%
Node15	16,85%	16,85%	16,85%	14,47%	17,01%

Each node voltage is compared against its corresponding non-faulty nominal value for each technology corner, within a margin of +/- 5%. In the case of this example, nodes 4, 11 and 12 are the nodes giving the best FC for all corners. If voltage of node 12 is chosen as a decider, good fault coverage is obtained with a single test. As it can be appreciated, a FC between 88% and 95% was obtained for shorts simulation in all corners.

For the open circuit faults simulation, a similar policy was followed. Table III shows the different fault coverage for each technology corner and node.

TABLE III. OPEN CIRCUIT FAULT COVERAGE FOR DIFFERENT TECHNOLOGY CORNERS AND NODES.

Node	Fault Coverage				
	TT	FS	FF	SF	SS
Node 1	92,86%	89,29%	96,43%	96,43%	92,86%
Node 2	0,00%	0,00%	0,00%	0,00%	0,00%
Node 4	53,57%	60,71%	64,29%	67,86%	64,29%
Node 5	60,71%	50,00%	60,71%	75,00%	67,86%
Node 6	46,43%	53,57%	53,57%	71,43%	64,29%
Node 7	0,00%	0,00%	0,00%	0,00%	0,00%
Node 8	7,14%	14,29%	10,71%	10,71%	10,71%
Node 9	10,71%	14,29%	10,71%	10,71%	10,71%
Node10	92,86%	85,71%	100,00%	100,00%	92,86%
Node11	100,00%	100,00%	100,00%	100,00%	100,00%
Node12	92,86%	89,29%	96,43%	100,00%	92,86%
Node14	3,57%	0,00%	0,00%	0,00%	0,00%
Node15	3,57%	7,14%	7,14%	7,14%	3,57%

In this case, the best FC is obtained when measurements are taken on node 11 (100%). However, node 12 presents also a good FC and, if both fault types were considered, such node gives the best total fault coverage (TFC). Table IV shows the TFC for both shorts and opens looking the output at all tested nodes. If node 12 were taken as decider, the results found are comparable and even better than others reported in the literature [12, 13-22].

TABLE IV. TOTAL FAULT COVERAGE FOR ALL NODES AT EVERY CORNER.

Node	TFC				
	TT	FS	FF	SF	SS
Node 1	46,81%	65,24%	52,64%	39,42%	47,12%
Node 2	7,15%	5,75%	7,78%	7,31%	5,75%
Node 4	91,06%	95,10%	83,28%	87,17%	93,47%
Node 5	77,76%	72,55%	71,85%	85,38%	77,76%
Node 6	45,57%	45,72%	40,28%	65,55%	56,38%
Node 7	11,51%	11,51%	9,64%	10,89%	11,51%
Node 8	24,26%	24,42%	22,47%	23,41%	23,41%
Node 9	19,21%	17,11%	16,10%	17,96%	18,27%
Node10	86,94%	87,09%	81,65%	86,94%	89,11%
Node11	88,72%	92,61%	87,79%	80,95%	89,66%
Node12	94,25%	94,48%	89,74%	88,72%	95,65%
Node14	15,01%	16,49%	16,02%	14,46%	15,71%
Node15	16,56%	16,64%	16,64%	14,31%	16,72%

As a part of the testing campaign, four parametric faults (i.e. variations on the transistors geometry) were injected and detected as well. The results are shown in table V.

Although an exhaustive simulation for parametric faults is almost impossible due to the diversity of this type of faults, good fault coverage for node 12 is obtained for the faults injected.

TABLE V. PARAMETRIC FAULTS INJECTED MEASURING ON NODE 12 WITH TT PARAMETERS.

node 12	fault injected	voltage measured	Relative error	Fault status
	none	42,36mv		
	20%+ on L12	38.07mv	10,13%	detected
	20%+ on W2	45,78mv	-8,07%	detected
	20%- on W17	46,25mv	-9,18%	detected
	30%- on W16	45,41mv	-7,20%	detected

VI. CONCLUSIONS

A simple analog testing technique, based on single DC voltage test was presented. Is a structural fault driven approach that can be applied in principle to any analog circuit. It has been shown that the use of little extra circuitry turns the procedure very suitable for BIST implementation. The idea was proven in a 65nm low-voltage transconductor, showing acceptable fault coverage for both catastrophic and parametric faults.

The discrimination between faulty and non-faulty devices is almost immediate, reducing thus the testing time if compared with other techniques. The checker presents usually high impedance inputs, what minimizes loading the CUT under normal operation. After PSPICE simulation, a MATLAB program was implemented in order to find the node with the highest FC rate.

The application of the proposed technique presents a TFC of 88% - 95%, that is comparable with the results of other more elaborated analog testing techniques.

Future works will focus mainly the implementation of a more sophisticated MATLAB script in order to find the minimum set of nodes to be measured in order to warrant the highest fault coverage near to 100%, if possible.

REFERENCES

[1] [T. M. Souders and G. N. Stenbakken, “Cutting the high cost of testing,” IEEE Spectrum, pp. 48–51, Mar. 1991.

[2] Mouna Karmani, Chiraz Khedhiri and Belgacem Hamdi, “Design and test challenges in Nano-scale analog and mixed CMOS technology”, International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2, June 2011.

[3] R.K. Gulatti and C.F. Hawkins, IDDQ testing of vlsi circuits, Ed. Kluwer Academic Publisher, 1993.

[4] Z. Chen, L. Wei, A. Keshavarzi, and K. Roy, IDDQ testing for deep-submicron ics: Challenges and solutions, IEEE Design & Test of Computers (2002), 24–33.

[5] Chia-Ling Chang et Al., “An intelligent analysis of Iddq data for chip classification in very deep-submicron (VDSM) CMOS technology”, Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific, pp. 163-168.

[6] Arabi, K. & B. Kaminska, "Oscillation-Based 'Test Strategy (OBTS) for Analog and Mixed-Signal Circuits," US Patent, Oct. 1995.

[7] P. Petrashin, G. Peretti, E. Romero “OBT implementation on a Gm-C Pass Band Filter with low gm”, 2010 11th ISQED, San José, CA, US, 22-24 March 2010 pages: 271 – 276.

[8] Pablo Petrashin, Carlos Dualibe, “An improved OBT strategy for untuned continuous-time analog filters”. LATW, Porto de Galinhas, Brazil, march 27-30 of 2011.

[9] Chatterjee, A. , Kim, B. ; Nagi, N., “Low-cost DC built-in self-test of linear analog circuits using checksums”, Proceedings of the Ninth International Conference on VLSI Design, 1996.., pp 230-233.

[10] Matthew Worsman, Mike W. T. Wong, and Y. S. Lee, “Enhancing the Fault Diagnosis of Linear Analog Circuit Steady-State DC Testing Through the Analysis of Equivalent Faults”, IEEE Transactions On Circuits And Systems, Vol. 50, No. 7, July 2003, pp. 932-936.

[11] Behzad Ghanavati, “A 1.5v CMOS Fuzzifier”, International Journal of Multidisciplinary Sciences And Engineering, Vol. 3, No. 6, June 2012 pp. 52-55.

[12] P. Petrashin, C. Dualibe, “An improved OBT strategy for catastrophic faults detection in continuous-time analog filters”, Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA) 2012, pp. 62-65.

[13] Arabi, K.; Kaminska, B. “Parametric and Catastrophic Fault Coverage of Analog Circuits in Oscillation-Test Methodology”; 15th IEEE VLSI Test Symposium, 27 Apr-1 May 1997, USA – pp 166 – 171.

[14] K. P. Parker, “Testability: Barriers to acceptance,” ZEEE Design and Test of Computers, pp. 11-15, Oct. 1986.

[15] S. C. Seth and V. D. Agrawal, “Cutting chip-testing costs,” Spectrum, pp. 38-45, Apr. 1985.

[16] E.R. Atwood, Analog Fault Simulation: Need it? No. It is already done, Proceedings IEEE International Test Conference, 28-30 September 1999, pp. 649–649.

[17] Kenneth M. Butler, The stuck-at fault: it ain’t over ’til it’s over, Proceedings of International Test Conference, 1998, p. 1165.

[18] B. R. Epstein, M. Czigler, and S. R. Miller, Fault detection and classification in linear integrated circuits: An application of discrimination analisys and hypothesis testing, IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems 12 (1993), no. 1, 102 – 113.

[19] C. Guardiani, P. McNamara, L. Daldoss, S. Zanella, S. Saxena, Suli Liu, and Wei Xiang, Prediction of analog performance parameters using fast transient testing, Proceedings of the Design, Automation and Test in Europe Conference, march 2002.

[20] Design of Concurrent Test Hardware for Linear Analog Circuits With Constrained Hardware Overhead. Sule Ozev and Alex Orailoglu - IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, VOL. 12, NO. 7, JULY 2004

[21] Genetic-Algorithm-Based Method for Optimal Analog Test Points Selection - T. Golonek and J. Rutkowski, Member, IEEE- IEEE Transactions On Circuits And Systems—Ii: Express Briefs, Vol. 54, No. 2, February 2007

[22] I. L. Huertas, “Test and design for testability of analog and mixed-signal integrated circuits: Theoretical basis and pragmatical approaches,” in Proc. ECCTD Conf., 1993, pp. 75–156.