Interface Compensation for More Accurate Power Transfer and Signal Synchronization within Power Hardware-in-the-Loop Simulation

Zhiwang Feng, Rafael Peña-Alzola, Paschalis Seisopoulos,
Mazheruddin Syed, Efren Guillo-Sansano, Patrick Norman and Graeme Burt
Department of Electronic and Electrical Engineering
University of Strathclyde, Glasgow, United Kingdom, G1 1RD
Email: {zhiwang.feng, rafael.pena-alzola, paschalis.seisopoulos,
mazheruddin.syed, efren.guillo-sansano, patrick.norman, graeme.burt}@strath.ac.uk

***Abstract*—Power hardware-in-the-loop (PHIL) simulation leverages the real-time emulation of a large-scale complex power system, while also enabling the in-depth investigation of novel actual power components and their interactions with the emulated power grid. The dynamics and non-ideal characteristics (e.g., time delay, non-unity gain, and limited bandwidth) of the power interface result in stability and accuracy issues within the PHIL closed-loop simulations. In this paper, a compensation method is proposed to compensate for the non-ideal power interface by maximizing its bandwidth, maintaining its unity-gain characteristic, and compensating for its phase-shift over the frequencies of interest. The accuracy of power signals synchronization and the transparency of power transfer within the PHIL configuration are assessed by employing the error metrics. In conjunction with the frequency-domain stability analysis and the time-domain simulations, a case study is made to validate the proposed compensation method.**

***Index Terms*—Power hardware-in-the-loop (PHIL), power transfer, signal synchronization, power interface compensation.**

I. INTRODUCTION

The advancement of computation technology facilitates the capability of the power hardware-in-the-loop simulation to carry out non-destructive and in-depth investigation of the large-scale complex power systems, the candidate power apparatus, and the control paradigms under broad-spectrum operation conditions before their final deployments as well as systemic applications [1]–[4]. With the real-time digital simulated system and pure power hardware comprised in a closed-loop testing environment, PHIL has been extensively exploited in the testing and prototyping of power apparatus [3]–[5], laboratory-based power system education [5], validation of novel control strategies [6], geographically distributed real-time co-simulation [7], and the dynamic modelling of renewable energy systems involving variable-speed wind turbines [8], photovoltaic cell [9], etc.

However, as indicated in Fig. 1, PHIL is not a plug-and-play simulation tool that just leverages an off-the-shelf real-time digital simulator and power hardware. As a result of splitting the original operating system into digital real-time simulation (DRTS) and real hardware under test (HUT), a power amplifier and sensor-based power interface (PI) is required to define the power transfer manner and interface the DRTS and HUT into a closed-loop configuration. For medium and high voltage PHIL applications, the switched-mode voltage source converter (VSC)-based power amplifier is widely employed as a power source or sink for the HUT due to its advantages of cost, efficiency, controllability [5]–[8]. The voltage tracking capability of the VSC with closed-loop control is achieved at the expense of a resulting low bandwidth, which limits its capability of replicating the high-frequency reference signal that includes certain harmonics in the PHIL simulation with different testing objectives. As presented in [10], the VSC-based power amplifier with open-loop control is efficient to replicate high-frequency transients within PHIL and introduce less time delay than the VSC with closed-loop control. However, without proper compensation strategies applied to the open-loop controlled VSC-based power amplification stage, the actual PHIL system response presents significant discrepancies if compared with that of the original non-split system due to the following key determinants:

1) Despite a power amplifier with ideal characteristics (i.e., infinite bandwidth and unity gain) being expected in the PHIL system [2], [11], [12], the actual power amplifier, which is modelled as time delay and a low-pass filter in [3], [12]–[15], presents non-ideal characteristics (i.e., limited bandwidth, non-unity gain, and resonance of the passive output filter).
2) The non-zero phase shift introduced by the power amplifier output filter presents the same effects as the loop phase lag that results from the time delay introduced by multiple stages within the PHIL closed-loop [16], on reducing the system stability margin, deteriorating the power signal synchronization, and degrading the transparency of power transfer between the DRTS and the HUT [11], [16], [17].

Many research efforts have been devoted to compensating for the non-ideal characteristics of the power amplifier. In [13], a notch filter is utilized to compensate for the par-

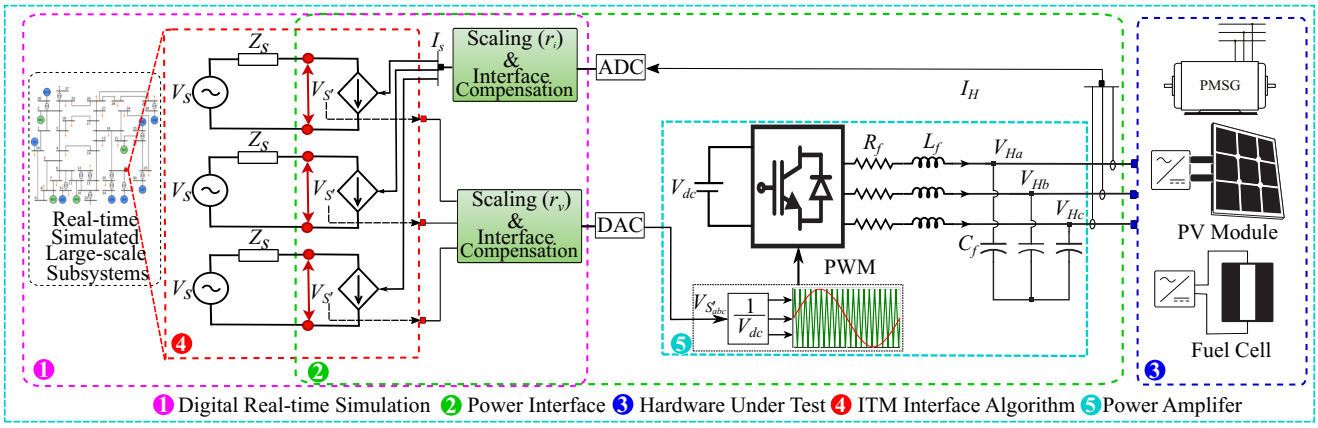


Fig. 1: A typical PHIL setup and a conceptual representation of the topology of the proposed compensation scheme in this paper.

asitic resonance of the passive output filter. However, the cancellation of resonance cannot guarantee the unity-gain of the compensated power interface and introduces additional phase lag to be compensated. A phase-lead compensator is employed to compensate for the magnitude attenuation and the phase lag of the power interface in [12]. While the frequency response of the compensated power interface is much closer to unity, as discussed in section V, the uncompensated phase-lag and amplified magnitude response degrades the stability and accuracy of the PHIL simulation.

To address the limitations of the compensation methods in the literature, we propose a compensation method to maximize the bandwidth of the power interface, preserve unity-gain over a wider frequency range, and compensate for the phase lag in the PHIL closed-loop. Fig. 1 shows a conceptual representation of the proposals stated in this paper. This paper is organized in the following way: Section II provides the details of the PHIL system modelling. Section III presents the analysis of PHIL system regarding its stability, accuracy, and power transfer. In section IV, the details of the proposed compensation method are elaborated. In section V, case studies are carried out to validate the effectiveness of the proposed compensation method. Section VI makes a conclusion and summarizes the scope of the proposed method.

II. Modelling of PHIL System

This section introduces the PHIL system with detailed modelling of its subsystems. Fig. 2 illustrates the PHIL configuration with ideal naturally coupled power system and voltage-type ideal transformer model (ITM) interface algorithm, which is the most widely used for its simpler structure and relatively high stability and accuracy among all the interface algorithms summarised in [11]. The original power system is expressed by a lumped voltage divider topology and is divided into the DRTS platform and the HUT from the splitting point, where the emulated power system and hardware are expressed by their Thévenin equivalent circuits. The power interface consists of a power amplifier, signal conversion cards (i.e., Analog-to-Digital converter (ADC) and Digital-to-Analog converter

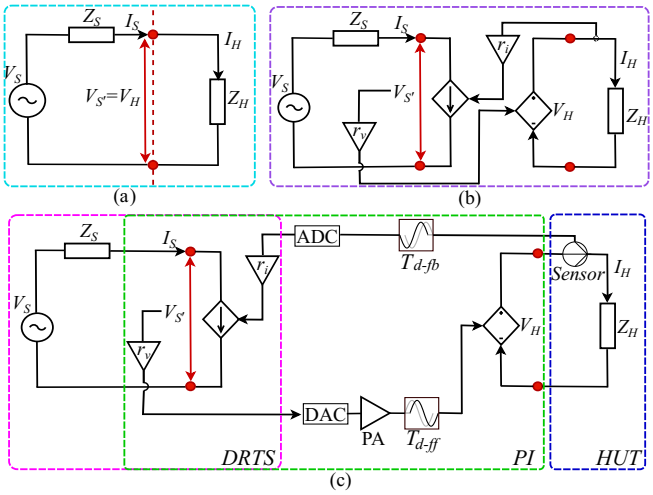


Fig. 2: (a) Natural lumped voltage divider system, (b) scaled voltage divider system, and (c) PHIL system with ITM algorithm.

(DAC)), and current sensors that connect DRTS with HUT. This PHIL configuration will be used throughout the paper.

Fig. 3 presents the equivalent block diagram of the PHIL system presented in Fig. 2(c). The blocks within this diagram are modelled as follows:

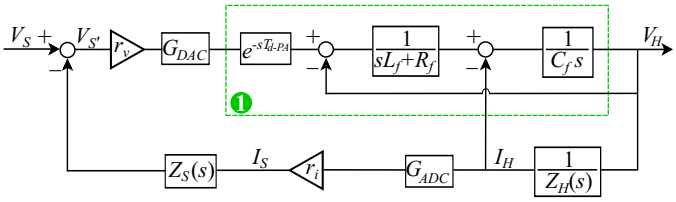
A. Voltage r_v and current r_i scaling ratio.

Due to the limited capacity and voltage levels of the power amplifier, a scaling ratio is introduced to facilitate the capability of a power amplifier. This represents the power components that are emulated in the DRTS with higher power rating and voltage levels than that of the power amplifier.

$$r_v = \frac{V_{Hnom}}{V_{S'nom}} \tag{1a}$$

$$r_i = \frac{I_{S'nom}}{I_{Hnom}} = \frac{S_{S'nom}/V_{S'nom}}{S_{Hnom}/V_{Hnom}} \tag{1b}$$

where V_{Hnom} is the nominal voltage of the physical HUT, $V_{S'nom}$ is the nominal voltage of the emulated HUT at the simulation side, S_{Hnom} is the nominal power rating of the physical HUT, and $S_{S'nom}$ represents the nominal power rating of the emulated component in the simulation side.



1 Equivalent block of power amplifier with *LC* output filter.

Fig. 3: Equivalent block diagram of the PHIL system in a single-phase basis.

B. Analog and digital signal conversion.

The ADC and DAC blocks are modelled as pure time delays (i.e., a full time-step in the DRTS platform) under the assumption that both of these present unity-gain characteristics.

$$\begin{cases} G_{DAC} &= e^{sT_{d-DAC}} \\ G_{ADC} &= e^{sT_{d-ADC}} \end{cases} \tag{2}$$

C. Switched-mode power amplifier with LC output filter.

Cell 5 within Fig. 1 represents the switched-mode VSC-based power amplifier with open-loop control, which is modelled as a voltage source converter with passive output filters and controlled via pulse-width-modulation. The LC output filter is implemented to eliminate high-frequency switching harmonics stemming from high-frequency pulsating modulation and its cut-off frequency should be tuned to be at least a decade lower than the switching frequency. The equivalent block diagram of the switched-mode power amplifier with LC filter is shown in Fig. 3 with its transfer function,

$$G_{PA}(s) = \frac{V_H}{V_{S'}} = e^{sT_{d-PA}} G_f(s) \tag{3a}$$

$$G_f(s) = \frac{1}{L_f C_f s^2 + (R_f C_f + \frac{L_f}{Z_H})s + (1 + \frac{R_f}{Z_H})} \tag{3b}$$

where T_{d-PA} is the equivalent time delay of the PWM modulation and its computation, R_f is the parasitic resistance of the inductor, L_f and C_f are the inductance and capacitance of the output filter respectively, and Z_H is the equivalent impedance of the HUT.

It is evident from (3a) that the output voltage V_H is affected by the filter characteristics and the HUT impedance under different load scenarios as shown in (3b). A compensation strategy as elaborated in the following section is required to ensure high-precision power signal amplification.

D. Total loop time delay.

The time delay T_{dff} in the feed-forward path is the sum of the time delay introduced by the digital computation of the DRTS (i.e., one full time-step T_{DRTS}), DAC (i.e., T_{d-DAC}), and the digital control of power amplifier (i.e.,T_{d-PA}). The time delay T_{dfb} in the feed-back path is the time delay introduced by the ADC (i.e., T_{d-ADC}). The total loop delay T_d is further expressed as the sum of T_{dff} and T_{dfb}, these are:

$$\begin{cases} T_{dff} &= T_{DRTS} + T_{d-DAC} + T_{d-PA} \\ T_{dfb} &= T_{d-ADC} \\ T_d &= T_{dff} + T_{dfb} \end{cases} \tag{4}$$

III. Analysis of PHIL system

This section explains the effects of the power amplifier and the loop time delay on the stability, accuracy, and the transparency of power transfer of the PHIL simulation.

A. PHIL stability and accuracy.

As the scaling factors are introduced in Fig. 2(b), the voltage at both the simulation side and HUT side can be further expressed as:

$$V_{S'} = \frac{1}{1 + r_v r_i \frac{Z_S}{Z_H}} V_S \tag{5a}$$

$$V_H = \frac{r_v}{1 + r_v r_i \frac{Z_S}{Z_H}} V_S = r_v V_{S'} \tag{5b}$$

where Z_S is the equivalent impedance of the emulated power network in the DRTS platform.

Owing to the presence of the power amplifier and the loop time delay, as shown in Fig. 3, the voltage signal to be amplified by the power amplifier at the splitting point in the DRTS side ($V_{S'}$) and the voltage at HUT terminal (V_H) in the ITM-based topology are given by:

$$V_{S'} = \frac{1}{1 + r_v r_i G_{PA}(s) e^{-sT_d} \frac{Z_S}{Z_H}} V_S \tag{6a}$$

$$V_H = \frac{r_v G_{PA}(s) e^{-sT_{dff}}}{1 + r_v r_i G_{PA}(s) e^{-sT_d} \frac{Z_S}{Z_H}} V_S \tag{6b}$$

As shown in (6a) and (6b), the time delay and the non-unity power amplifier $G_{PA}(s)$ are in the closed-loop characteristic polynomial. PHIL system stability can only be guaranteed provided that the gain margin (GM) and phase margin (PM) are positive and that the corresponding phase response of the open-loop transfer function satisfies the following criterion:

$$\left| r_v r_i G_{PA}(jw_{cg}) \frac{Z_S(jw_{cg})}{Z_H(jw_{cg})} e^{-jw_{cg}T_d} \right| = 1 \tag{7a}$$

$$\angle \left[G_{PA}(jw) \frac{Z_S(jw)}{Z_H(jw)} \right] - \angle(wT_d) > -180^\circ, \forall w \leq w_{cg} \tag{7b}$$

where w_{cg} is the gain crossover frequency at which the magnitude of open-loop transfer function is equal to 1 (0 dB).

As the time delay presents unity magnitude, the gain crossover frequency w_{cg} and the gain margin that defines the upper limit of the system magnitude variance before it raises above unity, are determined by the magnitude of power amplifier $|G_{PA}(jw_{cg})|$. As shown in (7b), the phase lag caused by the power amplifier filter and the loop time delay degrades the PHIL system stability margin as a result of the reduced phase margin (PM), a factor that indicates the system stability tolerance to phase lag [18].

Due to the non-unity magnitude and the phase lag of the power amplifier output filter, the phase and magnitude relationship between V_S' and V_H are not aligned with that defined in (5), leading to deteriorated power factor (PF) angle and inaccurate power transfer.

B. PHIL power transfer between the DRTS and the HUT.

Being proportional to the frequency of the input power signal, the phase shift caused by the loop time delay and power amplifier filter, and the non-unity magnitude characteristic of the passive output filter distort the phase relationship between the voltage and current, and change the power transfer between the DRTS platform and the hardware.

If the PHIL system presents unity magnitude and zero phase lag, the apparent power transferred between the simulation side ($S_{S'}$) and hardware (S_H) over a certain frequency w_k are:

$$\begin{cases} S_{S'} = & |V_{S'} I_{S'}| \angle\theta_{S'} & = & P_{S'} + jQ_{S'} \\ S_H = & |V_H I_H| \angle\theta_H & = & P_H + jQ_H \\ & = r_v r_i^{-1} |V_{S'} I_S| \angle\theta_H & = & r_v r_i^{-1} (P_{S'} + jQ_{S'}) \end{cases} \tag{8}$$

where $\theta_{S'}$ is power factor angle at the simulation side (i.e., $\angle V_{S'} - \angle I_{S'}$), θ_H is power factor angle at the hardware side (i.e., $\angle V_H - \angle I_H$), and $\theta_{S'} = \theta_H$.

For the PHIL with an open-loop-VSC-based power amplifier, which presents non-unity magnitude and negative phase characteristics over a certain frequency w_k , the actual voltage $\hat{V}_H$ and current $\hat{I}_H$ at the HUT side are:

$$\begin{cases} \hat{V}_H(w_k) = & r_v G_{PA}(w_k) e^{-jw_k T_{dff}} \hat{V}_{S'}(w_k) \\ & = r_v |G_{PA}(w_k)| \left| \hat{V}_{S'}(w_k) \right| \angle\delta \\ \hat{I}_H(w_k) = & r_i^{-1} e^{jw_k T_{dfb}} \hat{I}_{S'}(w_k) \\ & = r_i^{-1} \left| \hat{I}_{S'}(w_k) \right| \angle(w_k T_{dfb}) \\ \angle\delta = & \angle G_{PA}(w_k) - w_k T_{dff} \\ \angle\varphi = & \angle G_{PA}(w_k) - w_k T_{dff} + (w_k T_{dfb}) \end{cases} \tag{9}$$

where φ represents the phase lag introduced by the non-ideal power amplifier and the loop time delay.

The power factor angles $\hat{\theta}_{S'} = \angle\hat{V}_{S'} - \angle\hat{I}_{S'}$ and $\hat{\theta}_H = \angle\hat{V}_H - \angle\hat{I}_H$ can be further expressed as:

$$\hat{\theta}_H = \hat{\theta}_{S'} + \varphi \tag{10}$$

The apparent power at the simulation side and the HUT side are expressed as:

$$\begin{cases} \hat{S}_{S'} = & \left| \hat{V}_{S'} \hat{I}_{S'} \right| \angle\hat{\theta}_{S'} & = \hat{P}_{S'} + j\hat{Q}_{S'} \\ \hat{S}_H = & r_v r_i^{-1} |G_{PA}(w_k)| \left| \hat{V}_{S'} \hat{I}_{S'} \right| \angle\hat{\theta}_H & = \hat{P}_H + j\hat{Q}_H \end{cases} \tag{11}$$

Substituting (10) into (11), the active and reactive power at the HUT side can be further expressed as:

$$\begin{cases} \hat{P}_H = & r_v r_i^{-1} |G_{PA}(w_k)| (\hat{P}_{S'} cos\varphi - \hat{Q}_{S'} sin\varphi) \\ \hat{Q}_H = & r_v r_i^{-1} |G_{PA}(w_k)| (\hat{Q}_{S'} cos\varphi + \hat{P}_{S'} sin\varphi) \end{cases} \tag{12}$$

It is evident from (12) that the actual power transfer within the PHIL setup is not aligned with the power transfer defined in (8). This difference results from the non-unity magnitude $|G_{PA}(w_k)|$ and the phase lag φ introduced by the power amplifier output filter and the total loop time delay.

IV. PHIL INTERFACE COMPENSATION SCHEME

This section presents the compensation method from the aspects of the power amplifier non-unity characteristic compensation and the loop phase lag compensation.

A. Power amplifier compensator

As discussed in Section III, the non-ideal power amplifier distorts the transparent power transfer between the simulation side and hardware side. The high reconfigurability of the software within PHIL enables the flexibility to implement compensation blocks in the simulation platform. As shown in Fig. 1, compensation blocks are implemented in the software side to process the voltage and current signals before their applications in the feed-forward and feedback paths.

For most scenarios, the passive elements within the power interface and the HUT provide sufficient damping to mitigate the resonance of the output filter. On the contrary, for the passive filter in (3b) whose poles are lightly damped, the notch filter is an option to compensate for the resonance by placing additional zeros near the resonate poles, thus cancelling the associated resonant transient [18], that is:

$$G_{notch} = \frac{s^2 + 2r\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \tag{13}$$

where w_n is the centre notch frequency, ζ is the damping ratio of the notch filter poles that determines the sharpness of notch filter response and its notch width, and r is the filter gain at the notch frequency that determines the notch depth.

The resonant peak in (3b) is compensated by tuning the notch frequency w_n to be equal to the resonant frequency w_r of the output filter, and tuning the filter gain r to be the same as that of the output filter in (3b) at w_r to cancel the resonant peak. As shown in Fig. 4, the compensation for the resonance peak is achieved at the expense of more phase lag in the compensated filter, and the unity-gain of the compensated filter is not maintained over all the frequencies of interest.

$$\begin{cases} G_{lead}(s) = & \frac{\frac{\lambda s}{w_r}+1}{\frac{s}{\lambda w_r}+1}, & \lambda > 1 \\ G_{lag}(s) = & \frac{\frac{\lambda s}{w_r}+1}{\frac{s}{\lambda w_r}+1}, & 0 < \lambda < 1 \end{cases} \tag{14}$$

Lead or lag filters are both candidates to compensate for the non-ideal power interface in (3b). It is obvious from Fig. 4 that the lead filter compensates for the phase lag by introducing a positive phase shift to the power amplifier while resulting in a higher resonant peak that deteriorates the closed-loop stability. The lag filter suppresses the resonant peak by degrading the gain of the passive filter, which is achieved at the expense of a larger phase lag to be compensated and reduced bandwidth. For both scenarios, the unity-gain magnitude response of the compensated filter is achieved only over certain frequencies.

In this paper, the compensator $G_f^{comp}(s)$ is designed to compensate for the non-unity characteristics of the output filter over its bandwidth by inverting the dominator in (3b) to the numerator of $G_f^{comp}(s)$. Because the degree of the dominator is two times higher than that of the numerator

in (3b), a second-order dominator that has two poles is required in $G_f^{comp}(s)$ to cancel the additional two zeros of the numerator in $G_f^{comp}(s)$, and thus making the compensation block physically realizable. So the compensator $G_f^{comp}(s)$ is the inverse of $G_f(s)$ augmented with a second-order low-pass filter to ensure it is a proper transfer function, that is:

$$\begin{aligned} G_f^{comp}(s) &= \frac{G_f^{-1}(s)}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1} \\ &= \frac{L_fC_fs^2+(R_fC_f+\frac{L_f}{Z_H})s+(1+\frac{R_f}{Z_H})}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1} \end{aligned} \tag{15}$$

where k represents the ratio between the resonant frequency in the compensator to that of the transfer function in (3b), ζ_{op} is the optimum damping ratio to be tuned in the compensator.

The transfer function of the equivalent compensated output filter can be further expressed as:

$$G_f^{'}(s) = G_f(s)G_f^{comp}(s) = \frac{1}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1} \tag{16}$$

In order to tune the compensated filter $G_f^{'}(s)$ to behave like a well-known second-order Butterworth filter with maximally flat magnitude response [18], ζ_{op} is set as the optimal value $\frac{\sqrt{2}}{2}$, such that the bandwidth of $G_f^{'}(s)$ is equal to the resonant frequency kw_n. To make the compensated filter $G_f^{'}(s)$ with wider bandwidth than that of the uncompensated filter $G_f(s)$, k is tuned to be 3 in this paper.

Fig. 4 presents the frequency response of the compensator in (15) and the compensated output filter in (16). The compensated filter implemented with the compensator in (15) presents unity magnitude over a wider frequency range than that of the uncompensated filter. The power amplifier compensated by (15) presents a wider bandwidth than that of the power amplifier compensated by a notch filter or lead-lag compensators. Note that, the implementation of the compensator in (15) is under the assumption that the parameters of the LC filter and the HUT impedance are known exactly, which is achievable by employing the system identification techniques in the controlled PHIL environment. However, if system's parameter information is not available or the filter in (3b) has lightly damped complex poles whose locations cannot be estimated precisely, the conventional notch filter in (13) is an option to suppress the resonance and cancel the corresponding resonant transient.

Even though the compensated $G_f^{'}(s)$ presents a unity-magnitude characteristic over a wide range of frequencies, the phase lag introduced by this compensated filter is:

$$\angle G_f^{'}(s=jw) = tan^{-1}\left(\frac{\frac{2\zeta_{op}}{kw_r}w}{1-\frac{w^2}{(kw_r)^2}}\right) \tag{17}$$

The phase lag significantly distorts the power signal and power transfer as discussed in Section III. The compensation of these phase lags and the loop delay on a harmonic-by-harmonic basis is presented in the following section.

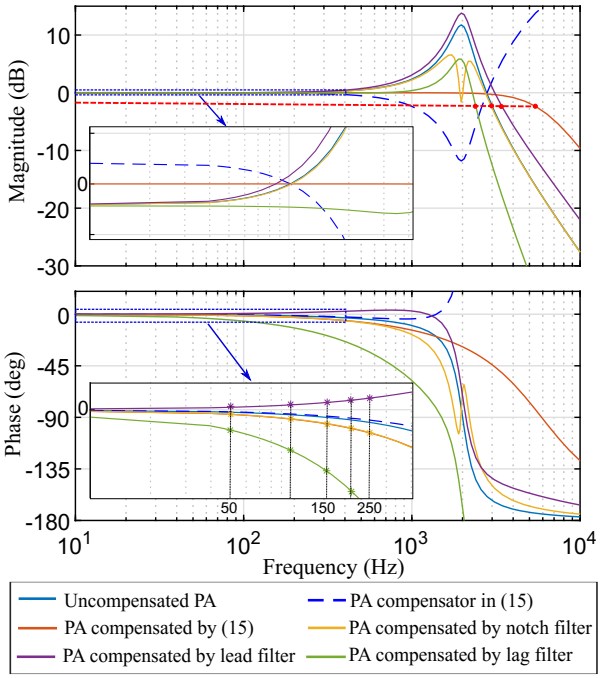


Fig. 4: The frequency response of the uncompensated filter $G_f(s)$, compensator $G_f^{comp}(s)$ in (15), and the compensated filter $G_f^{'}(s)$.

B. Loop phase lag compensation.

As reported in our previous work [17], the phase lag within the PHIL setup is compensated by the frequency sampling filter (FSF)-based compensation scheme on a harmonic-by-harmonic basis. The FSF is implemented as a non-recursive finite impulse response (FIR) filter, of which the linear phase and steep cut-off amplitude characteristics enable the selective update of the signal phase and amplitude characteristics over a wide range of frequencies [19]. As illustrated in Fig. 5, FSF can be represented as a comb filter in series with parallelized complex resonators [19] and be expressed as:

$$H_{FSF}(z) = \underbrace{(1-r^Nz^{-N})}_{\text{Comb filter}}\underbrace{\sum_{k=1}^{N}\frac{e^{j\frac{2\pi k}{N}}}{1-rz^{-1}e^{j\frac{2\pi k}{N}}}}_{\text{Complex resonators}} \tag{18}$$

where $N\,(N=\frac{f_s}{f_0})$ is the window size, f_s is the sampling frequency, f_0 is the fundamental frequency, and $k\,(k=1,2,3,\cdots N)$ represents the order of the resonator. $r\,(r=1-\varepsilon)$ is the damping factor to force the zeros or poles of FSF to be located within the unity circle to guarantee its stability.

According to the frequency response of the FSF in [17], the comb filter presents periodically spaced notches and the complex resonators present periodically spaced sharp peaks at the fundamental and harmonic frequencies. The FSF filter implemented as a comb filter in series with k-th order complex resonator is equivalent to a band-pass filter centred at the resonant frequency kw_0 and the scaling factor $\frac{1}{N}$ is implemented at the output of each single resonator to mitigate the overflow error and maintain the unity gain of the FSF filter. These attributes enable the selective update of the reference signal at any frequencies of interest without magnitude distortion.

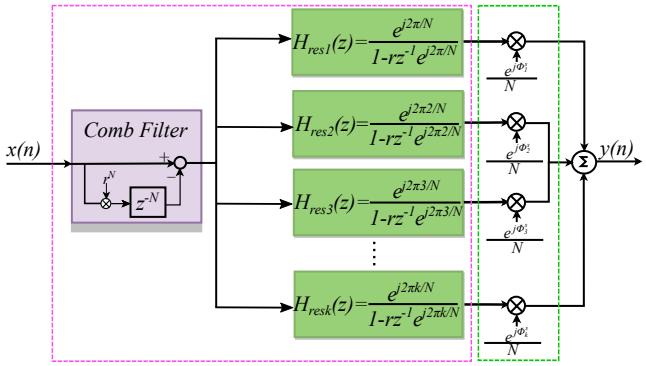


Fig. 5: The block diagram of the FSF with complex resonator banks and harmonic-by-harmonic time delay compensations.

Fig. 5 presents the block diagram of the FSF-based phase lag compensation filters. To compensate for the phase lags of the compensated filter in (17) and the loop time delay, an additional phase shift ϕ_k^s is implemented at the output of the resonator with resonant frequency kw_0. The FSF implemented with additional phase shift can be expressed as:

$$\phi_k^s = kw_0 T_{dff} + \angle G_f^{'}(kw_0) \tag{19}$$

$$H_{FSF}^{comp}(z) = (1 - r^N z^{-N}) \frac{1}{N} \sum_{k=1}^{N} \frac{e^{j\frac{2\pi k}{N}} e^{j\phi_k^s}}{1 - rz^{-1} e^{j\frac{2\pi k}{N}}} \tag{20}$$

V. Case Study and Simulation Results

Matlab/Simulink simulation models are utilized to verify the effectiveness of the proposed compensation method. Table I shows the parameters of the PHIL setup in Fig. 1. A voltage source inverter with ideal semiconductor switches is employed as the power amplifier. The LC parameters are calculated by tuning its cut-off frequency to be equal to $f_{sw}/10$. The voltage divider topology is emulated in the DRTS side and the HUT is emulated as an inductive hardware component.

The scaled voltage signal $r_v \hat{V}_{S'}$ that is to be amplified by the power amplifier, the voltage signal $\hat{V}_H$ at the HUT side, the power factor angle θ, the scaled active power and scaled reactive power at both of the simulation and hardware side are employed to assess the performance of the compensation method. Accuracy metrics are defined by the relative average error η to quantify the accuracy of power signal amplification and the transparency of power transfer between the simulation side and the HUT side at the steady-state.

$$\begin{cases} \text{PF angle tracking error} & \eta_{\theta T} = \frac{\left|\hat{\theta}_H - \hat{\theta}_{S'}\right|}{\left|\hat{\theta}_{S'}\right|} \\ \text{RMS voltage tracking error} & \eta_{VT} = \frac{\left|\hat{V}_H - r_v \hat{V}_{S'}\right|}{\left|r_v \hat{V}_{S'}\right|} \\ \text{Active power tracking error} & \eta_{PT} = \frac{\left|\hat{P}_H - r_v r_i^{-1} \hat{P}_{S'}\right|}{\left|r_v r_i^{-1} \hat{P}_{S'}\right|} \\ \text{Reactive power tracking error} & \eta_{QT} = \frac{\left|\hat{Q}_H - r_v r_i^{-1} \hat{Q}_{S'}\right|}{\left|r_v r_i^{-1} \hat{Q}_{S'}\right|} \\ \text{Measured } x \text{ to reference error} & \eta_x = \frac{|x_{mea} - x_{ref}|}{|x_{ref}|} \end{cases}$$

where x_{mea} is the power signal within the PHIL setup, x_{ref} is the reference power signal in original scaled power system.

TABLE I: PHIL system parameters for analysis and simulations.

Description	*Symbol*	*Value*
PHIL setup		
Nominal HUT resistance	R_H	2 Ω
Nominal HUT inductance	L_H	1 mH
Naturally coupled DRTS resistance	R_S	0.5 Ω
Naturally coupled DRTS equivalent voltage	V_S	4.26 kV
PHIL system fundamental frequency	f_0	50 Hz
PHIL system feed-forward path time delay	T_{dff}	450 µs
PHIL system feed-back path time delay	T_{dfb}	50 µs
Nominal power rating of the emulated HUT	$S_{S'nom}$	62.5MVA
Nominal power rating of the physical HUT	S_{Hnom}	100kVA
Nominal voltage of the emulated HUT	$V_{S'nom}$	15 kV
Nominal voltage of the physical HUT	V_{Hnom}	600 V
Voltage scaling ratio	r_v	0.04
Current scaling ratio	r_i	25
Power amplifier		
DC voltage	V_{DC}	1000 V
PWM switching frequency	f_{sw}	20 kHz
Sampling frequency	f_s	40 kHz
Filter inductance	L_f	0.054 mH
Filter parasitic resistance	R_f	6.8 mΩ
Filter capacitor	C_f	117 µF

TABLE II: Magnitude (in abs), phase (in deg) and bandwidth (in Hz) of the uncompensated output filter and the output filter compensated by the proposed compensator, notch filter, lead filter, and lag filter.

Compensator	Filter in (3b)	Compensator in (15)	Notch filter	Lead filter	Lag filter
Mag at f_0	0.9944	1.0000	0.9943	0.9946	0.9941
Phase at f_0	-0.2744	-0.6707	-0.7687	0.4368	-1.5547
Mag at $5f_0$	1.0030	1.0000	1.0020	1.0088	0.9955
Phase at $5f_0$	-0.2402	-3.3556	-2.7473	3.2852	-6.6068
Bandwidth	3118.2	6033.1	3049.5	3561.3	2729.5

A. Evaluation of different compensation strategies.

This section compares the performances of the compensation schemes presented in Section IV-A from the perspective of their frequency response characteristics and the closed-loop stability of the compensation scheme-based PHIL setup.

Table II presents the frequency responses of the original uncompensated power amplifier filter and that of the power amplifiers that are compensated by different compensators. The non-unity magnitude of the power amplifier output filter in (3b) is compensated to be unity by implementing the proposed compensator (15) in this paper over the fundamental frequency and other harmonics components. This results from the optimal setting of the damping factor in (15) to make the compensated filter present a flat unity magnitude response over a wide range of frequencies. However, the magnitudes of the power amplifier compensated by the notch filter, lead filter, and lag filter are non-unity at the fundamental frequency and other harmonic components, which inevitably distort the reference power signal to be amplified. Note that the phase lags of the power amplifier compensated by the notch filter, lag filter, and the compensator in (15) are much larger than that of the original uncompensated power amplifier. The bandwidth of power amplifier compensated by (15) is higher than that of the uncompensated power amplifier and the power amplifier compensated by notch filter, lead filter, and lag filter. This results from the optimal tuning of the ratio factor k in (15).

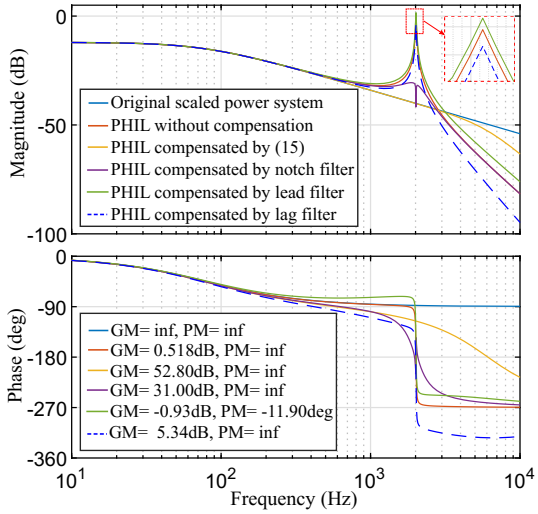


Fig. 6: Bode plot of the open-loop transfer functions of the original scaled power system, uncompensated PHIL system, and the PHIL system compensated by the compensators as shown in the legend.

Fig. 6 presents the frequency responses of the open-loop transfer function of the uncompensated and compensated PHIL systems. The resonance of the uncompensated PHIL system is compensated by implementing the compensator in (15). Notice that the magnitude characteristic of the PHIL system compensated by (15) is aligned with that of the original scaled power system because the compensated power amplifier presents unity gain over a certain frequency range. The notch filter and the lag filter are also effective in suppressing the resonance of the PHIL system, of which the stability margins are lower than that of the PHIL system compensated by (15). Even though the lead filter compensates for phase lag to some extent, it can destabilize the PHIL system, especially the marginally stable PHIL system or the PHIL system with low stability margins. This is because the lead filter causes the magnitude of the compensated PHIL system to exceed unity and the resonance frequency to be greater than the gain-crossover frequency w_{cg} as defined in (7a).

B. Accuracy evaluation of the proposed compensation method.

This section evaluates the performance of the proposed method regarding its capability of improving the power signal synchronization and enhancing the power transfer transparency in the PHIL closed-loop configuration. Accuracy metrics are employed to evaluate the following cases:

1) Original scaled power system in Fig. 2b.
2) PHIL system without compensation.
3) PHIL system with loop time delay compensation only.
4) PHIL system with compensation proposed in this paper.

Table III presents the power signal tracking error metrics. Due to the non-unity gain of the power amplifier as described in Table II, the loop time delay, the phase lag of the power amplifier output filter, and the RMS voltage and power factor angle tracking errors are significant for the PHIL system without proper compensation in case 2) and case 3). Notice that even the loop delay is compensated in case 3), there still

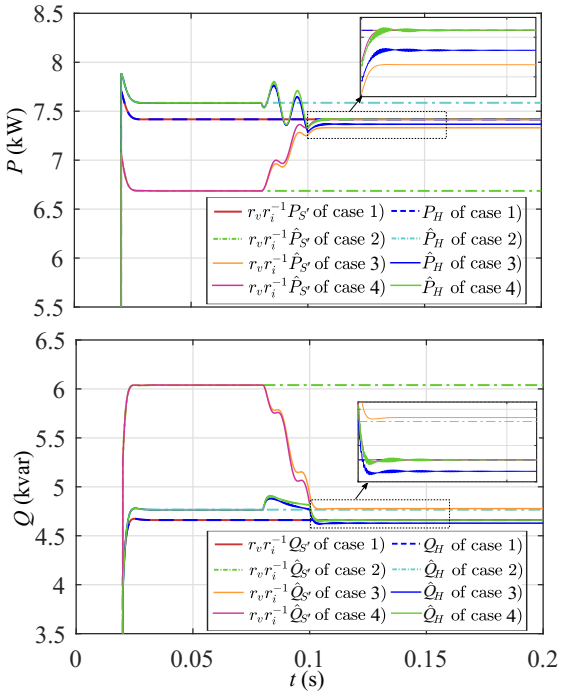


Fig. 7: The active power and reactive power at the simulation and HUT side of the scaled voltage divider system and PHIL system.

exists a power factor angle tracking error due to the phase lag of the power amplifier output filter in (17). Because the compensation method proposed in this paper maintains the unity gain of the power amplifier and takes both the loop time delay and the phase lag of the power amplifier output filter into consideration, as shown in case 4), the PHIL system compensated by the proposed method presents remarkably improved power signal tracking capabilities regarding the RMS voltage, power factor angle, and the active power and reactive power.

Table IV and Fig. 7 present the steady-state PHIL power signal to reference signal error metrics and the $P\&Q$ power behaviours under the pre-defined cases, respectively. The compensation blocks are implemented at $t = 0.08$s in case 3) and case 4). As a result of the non-unity magnitude of power amplifier and the phase lags in the closed-loop, the errors of the voltage and power factor angle between the PHIL system and the original scaled power system are also remarkable in case 2) and case 3). As shown in Fig. 7, there are significant mismatches between the power signal at the simulation and hardware sides (i.e., $\hat{P}_H > r_v r_i^{-1} \hat{P}_{S'}$ and $\hat{Q}_H < r_v r_i^{-1} \hat{Q}_{S'}$) for the PHIL system without compensation. These mismatches result from the loop phase lag and the non-unity magnitude of the power amplifier as explained in (12). Note that the $P\&Q$ differences between the PHIL system in case 3) and the original scaled power system are also remarkable even when the loop time delay is compensated. After implementing the proposed compensation method, the $P\&Q$ of the PHIL system in case 4) are aligned with that of the reference power system and the power transfer within this PHIL system is as transparent as that of the reference power system in Fig. 2b.

TABLE III: The power signal tracking error metrics of different cases at the fundamental frequency f_0.

Case	$\hat{V}_H$ (V_{RMS})	$r_v\hat{V}_{S'}$ (V_{RMS})	η_{VT}	$\hat{\theta}_H$ (deg)	$\hat{\theta}_{S'}$ (deg)	$\eta_{\theta T}$	$\hat{P}_H$ (kW)	$r_v r_i^{-1}\hat{P}_{S'}$ (kW)	η_{PT}	$\hat{Q}_H$ (kvar)	$r_v r_i^{-1}\hat{Q}_{S'}$ (kvar)	η_{QT}
1)	143.84	143.84	0.00%	32.14	32.14	0.00%	7.417	7.417	0.00%	4.660	4.660	0.00%
2)	145.47	146.29	0.56%	32.14	42.09	23.64%	7.586	6.686	13.46%	4.766	6.039	21.08%
3)	143.35	144.17	0.57%	32.14	33.10	2.99%	7.367	7.331	0.49%	4.629	4.777	3.10%
4)	143.84	143.84	0.00%	32.14	32.14	0.00%	7.417	7.417	0.00%	4.660	4.660	0.00%

TABLE IV: The PHIL power signal to the reference power signal error metrics of different cases at the fundamental frequency f_0.

Case	$\hat{V}_H$ (V_{RMS})	η_{V_H}	$r_v\hat{V}_{S'}$ (V_{RMS})	$\eta_{V_{S'}}$	$\hat{\theta}_{S'}$ (deg)	$\eta_{\theta_{S'}}$	$\hat{P}_H$ (kW)	η_{P_H}	$r_v r_i^{-1}\hat{P}_{S'}$ (kW)	$\eta_{P_{S'}}$	$\hat{Q}_H$ (kvar)	η_{Q_H}	$r_v r_i^{-1}\hat{Q}_{S'}$ (kvar)	$\eta_{Q_{S'}}$
1)	143.84	0.00%	143.84	0.00%	32.14	0.00%	7.417	0.00%	7.417	0.00%	4.660	0.00%	4.660	0.00%
2)	145.47	1.13%	146.29	1.70%	42.09	30.96%	7.586	2.28%	6.686	9.86%	4.766	2.27%	6.039	29.59%
3)	143.35	0.34%	144.17	0.23%	33.10	2.99%	7.367	0.67%	7.331	1.16%	4.629	0.67%	4.777	2.51%
4)	143.84	0.00%	143.84	0.00%	32.14	0.00%	7.417	0.00%	7.417	0.00%	4.660	0.00%	4.660	0.00%

VI. Conclusion

This paper presents a compensation scheme for the open-loop controlled VSC-based power amplifier to enable more accurate power signal synchronization and power transfer within the PHIL closed-loop simulation. This compensation method is designed to maintain the unity gain of the power amplifier over a wider range of frequencies via optimal tuning of the proposed compensator. In addition, it compensates for the phase lag on a harmonic-by-harmonic basis. The effectiveness of this compensation method has been evaluated and demonstrated via the accuracy metrics and the simulation results. The advantages of this compensation method over the compensation techniques published in the literature have been demonstrated via frequency-domain analysis. The PHIL simulation that is based on the proposed compensation method presents high power signal tracking capability, which is of great significance for a high-fidelity PHIL simulation.

Acknowledgement

This work was undertaken as part of the Rolls-Royce University Technology Centre program at the University of Strathclyde.

References

[1] M. D. Omar Faruque, T. Strasser, G. Lauss, V. Jalili-Marandi, P. Forsyth, C. Dufour, V. Dinavahi *et al.*, "Real-time simulation technologies for power systems design, testing, and analysis," *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 2, pp. 63–73, 2015.

[2] G. F. Lauss, M. O. Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and design of power hardware-in-the-loop simulations for electrical power systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406–417, Jan 2016.

[3] P. C. Kotsampopoulos, F. Lehfuss, G. F. Lauss, B. Bletterie, and N. D. Hatziargyriou, "The limitations of digital simulation and the advantages of phil testing in studying distributed generation provision of ancillary services," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 9, pp. 5502–5515, 2015.

[4] I. Jayawardana, C. N. M. Ho, and Y. Zhang, "A comprehensive study and validation of a power-hil testbed for evaluating grid-connected ev chargers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.

[5] P. C. Kotsampopoulos, V. A. Kleftakis, and N. D. Hatziargyriou, "Laboratory education of modern power systems using phil simulation," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3992–4001, 2017.

[6] Y. Wang, M. H. Syed, E. Guillo-Sansano, Y. Xu, and G. M. Burt, "Inverter-based voltage control of distribution networks: A three-level coordinated method and power hardware-in-the-loop validation," *IEEE Transactions on Sustainable Energy*, vol. 11, no. 4, pp. 2380–2391, 2020.

[7] M. H. Syed, E. Guillo-Sansano, Y. Wang, S. Vogel, P. Palensky, G. M. Burt, , Y. Xu, A. Monti, and R. Hovsapian, "Real-time coupling of geographically distributed research infrastructures: Taxonomy, overview, and real-world smart grid applications," *IEEE Transactions on Smart Grid*, vol. 12, no. 2, pp. 1747–1760, 2021.

[8] F. Huerta, R. L. Tello, and M. Prodanovic, "Real-time power-hardware-in-the-loop implementation of variable-speed wind turbines," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1893–1904, 2017.

[9] M. Kim, S.-K. Kwak, K. A. Kim, and J.-H. Jung, "Enhanced computation performance of photovoltaic models for power hardware-in-the-loop simulation," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6952–6961, 2021.

[10] K. Upamanyu and G. Narayanan, "Improved accuracy, modeling, and stability analysis of power-hardware-in-loop simulation with open-loop inverter as power amplifier," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 369–378, 2020.

[11] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," *IEEE Transactions on Industry Applications*, vol. 44, no. 4, pp. 1286–1294, 2008.

[12] W. Ren, M. Sloderbeck, M. Steurer, V. Dinavahi, T. Noda, S. Filizadeh *et al.*, "Interfacing issues in real-time digital simulators," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 1221–1230, 2011.

[13] N. Ainsworth, A. Hariri, K. Prabakar, A. Pratt, and M. Baggu, "Modeling and compensation design for a power hardware-in-the-loop simulation of an ac distribution system," in *2016 North American Power Symposium (NAPS)*, 2016, pp. 1–6.

[14] F. Lehfuss, G. Lauss, P. Kotsampopoulos, N. Hatziargyriou, P. Crolla, and A. Roscoe, "Comparison of multiple power amplification types for power hardware-in-the-loop applications," in *2012 Complexity in Engineering (COMPENG). Proceedings*, 2012, pp. 1–6.

[15] G. Lauss and K. Strunz, "Accurate and stable hardware-in-the-loop (hil) real-time simulation of integrated power electronics and power systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 10 920–10 932, 2021.

[16] E. Guillo-Sansano, M. H. Syed, A. J. Roscoe, G. M. Burt, and F. Coffele, "Characterization of time delay in power hardware in the loop setups," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 3, pp. 2703–2713, 2021.

[17] Z. Feng, R. Peña-Alzola, P. Seisopoulos, E. Guillo-Sansano, M. Syed, P. Norman, and G. Burt, "A scheme to improve the stability and accuracy of power hardware-in-the-loop simulation," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 5027–5032.

[18] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 7th ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2014.

[19] R. G. Lyons, *Understanding Digital Signal Processing (2Nd Edition)*. Upper Saddle River, NJ, USA: Prentice Hall PTR, 2004.