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Performance Assessment of Amorphous HfO_2-Based RRAM Devices for Neuromorphic Applications

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The use of thin layers of amorphous hafnium oxide has been shown to be suitable for the manufacture of Resistive Random-Access memories (RRAM). These memories are of great interest because of their simple structure and non-volatile character. They are particularly appealing as they are good candidates for substituting flash memories. In this work, the performance of the MIM structure that takes part of a 4 kbit memory array based on 1-transistor-1-resistance (1T1R) cells was studied in terms of control of intermediate states and cycle durability. DC and small signal experiments were carried out in order to fully characterize the devices, which presented excellent multilevel capabilities and resistive-switching behavior.
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The current trend of non-volatile memories covers a variety of technologies: Ferroelectric RAMs (FRAMs), which include a ferroelectric layer as a dielectric; Magnetoresistive RAMs (MRAMs), based on the magnetization of a ferromagnetic structure; Phase-change RAMs (PRAMs), which depend on crystallization and amorphization processes of a chalcogenide material; Resistive RAMs (RRAMs), which involve electro- and termochemical effects in the resistance change of a metal/oxide/metal system, and some others.[1–6] Focusing on RRAMs, their excellent characteristics (short-operating time, good scalability, good retention, small-operating voltage, multiplicity of intermediate states) make them very relevant in the quest for a consolidated candidate which could suppose a relevant change in the current state-of-the-art.[7–9] The fundamentals of resistive switching (the mechanism on which RRAMs are based on) involve the growth of a conductive filament inside the dielectric film as a result of applying a potential difference between top and bottom electrodes.[10,11] One of the biggest obstacles in the fabrication of RRAMs is related to finding an appropriate combination of materials for the dielectric layer, and thus the materials research has continously progressed.[12] When the filament completely joins both electrodes, the resistance of the RRAM is low, and, thus, this situation is called LRS (low resistance state). When the polarity of the voltage applied is reversed, a rupture on the filament occurs, the resistance is high and this is called HRS (high resistance state). The transitions to reach the mentioned states are called set and reset, respectively.[13] The MIM devices that were tested in this work had an insulator film of HfO_2, which has been extensively studied in the literature and is very appreciated for its usage in resistive memories.[14,15] Interestingly, RRAMs also serve as synaptic elements for neuromorphic networks, attending to the multiple intermediate states which they can reach.[16] Resistive RAMs can even be suitable for both memory and neuromorphic applications, as shown in Ref. 17, 18. There are precedent publications which studied these structures.[19,20] Nevertheless, we provide a complete characterization study of individual devices which were built following the same industrial process.

Experimental

In this work, we evaluated the performance of individual MIM structures which constitute the unit element of a 4 kbit memory array based on 1T1R (1-transistor-1-resistor) cells, as displayed in Fig. 1. The process node to fabricate the devices in the array was 250 nm. In each cell of the memory, an NMOS transistor in series with the MIM resistor was placed so as to be able to select a specific cell and to limit the current that flows through the memory element, preventing an eventual hard breakdown.[19] The MIM stacks presented a TiN/a-HfO_2/Ti/TiN structure, with the Ti layer below the top electrode. The hafnia layer is amorphous and has a thickness of 8 nm. On the other hand, each TiN electrode features 150 nm thickness and the Ti interface layer spanned 7 nm. In Fig. 2 there are included the XRD results that confirm the amorphous state in HfO_2. Moreover, the TEM cross-sectional images that confirm the layer thickness information and also the amorphous state of the HfO_2 film were previously published and can be seen at Ref. 21 and Ref. 19 Each device occupies an area of $75 \times 75\ \mu m^2$. The dielectric was deposited by Atomic Layer Deposition (ALD), while the metal films were deposited by magnetron sputtering. The electrical characteristics were acquired by using a Keithley SCS-4200A and comprised DC and small-signal experiments. The latter were run by applying an AC voltage of 30 mV superimposed to the DC signal, with a fixed frequency of 100 kHz. The bias voltage was supplied to the top electrode, while the bottom electrode was grounded.

Results and Discussion

An exhaustive electrical characterization was performed on a moderately large set of devices, including current-voltage, small-signal cycles, memory maps and endurance tests. The forming process is shown in Fig. 3a: the current progressively increases until it reaches a current limit set to 1.4 mA. At that moment, a conductive filament is formed. It was necessary to restrict the maximum current because otherwise the devices break down irreversibly. Figure 3b depicts 87 I-V cycles which show 3 different stages during the series. During the first 6 cycles the behavior was quite erratic, probably as a result of the initial instability of the conductive filament.[22] The next 56 cycles were much more repetitive, although it can be seen a progressive displacement of current values. The experiment finished with 25 cycles which presented symptoms of stress, given that the transitions were very abrupt and the HRS/LRS levels fluctuated excessively.

Continuing with I-V characteristics, in Fig. 4a a group of nested cycles is represented. They were obtained by applying voltage sweeps where each one completed a set/reset transition. The state transitions were performed alternately, while the voltage levels increased after each cycle. These cycles prove the excellent properties of the devices, in particular the easy control of the intermediate states. The I-V memory map presented in Fig. 4b shows that the set transition is more abrupt than the reset one. This

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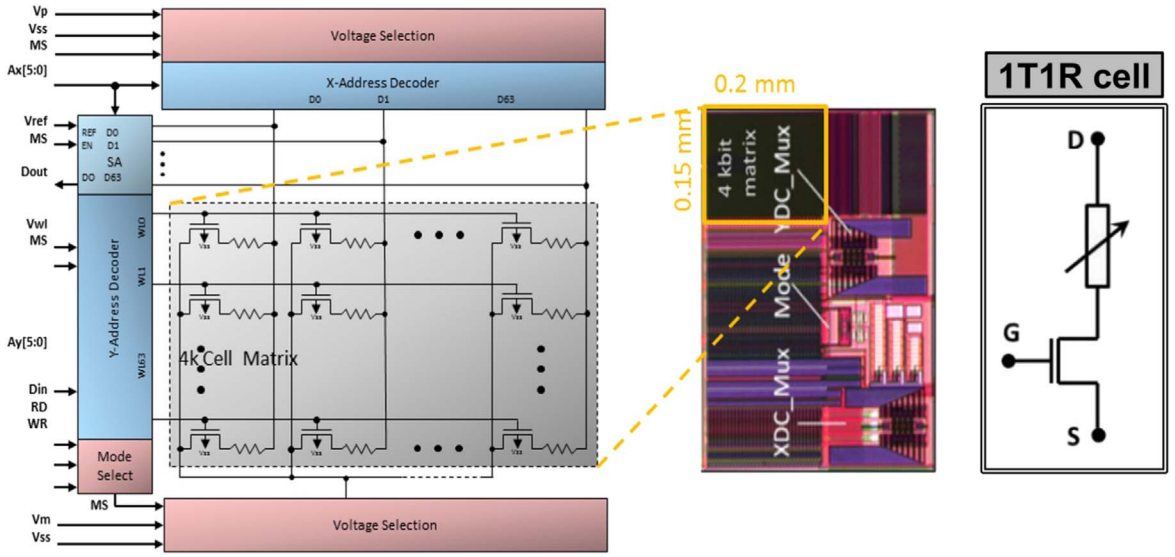

Figure 1. Schematic representation of the 4 kbit array composed by 1T1R cells.

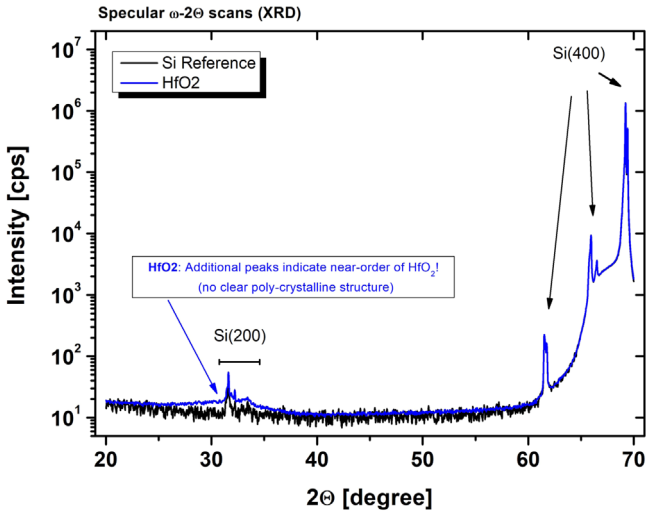

Figure 2. XRD results that confirm the amorphous state of HfO_2.

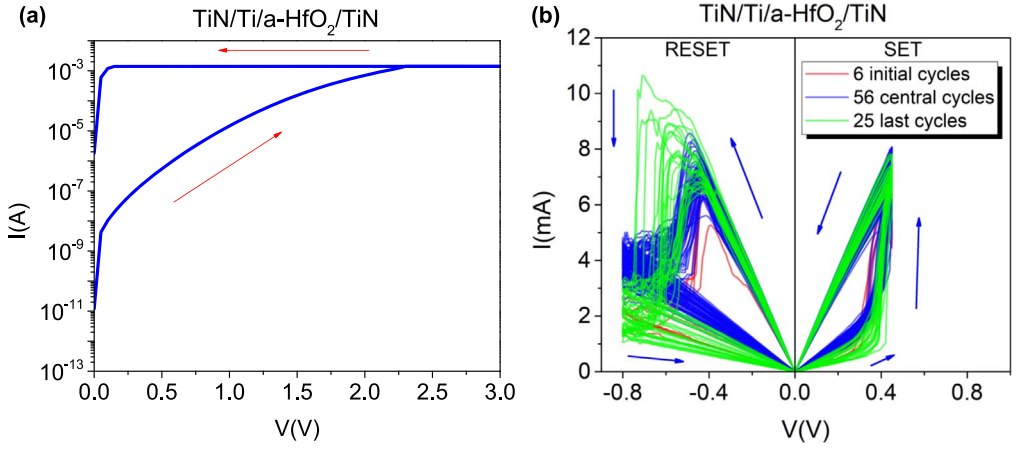

Figure 3. Electroforming process (a). 87 I-V cycles with 3 different switching stages (b). The current (I) is in absolute values.

could be explained by the fact that the rupture of the filament occurs gradually, whilst the formation is abrupt. The procedure to measure I-V memory maps in RRAMs consists of applying a sequence of programming voltage pulses, while alternating a read pulse at a fixed voltage (here it is 0.1 V) between programming pulses.[23] Afterwards, each point in the graph is understood as the current read at 0.1 V vs

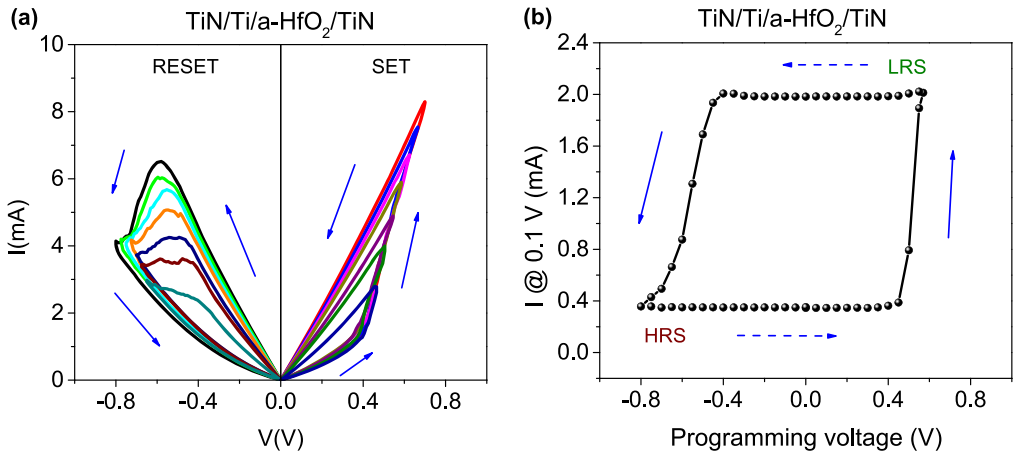

Figure 4. Nested cycles (a), where the voltage level increased for each set/reset cycle. The current (I) is in absolute values. I-V memory map (b).

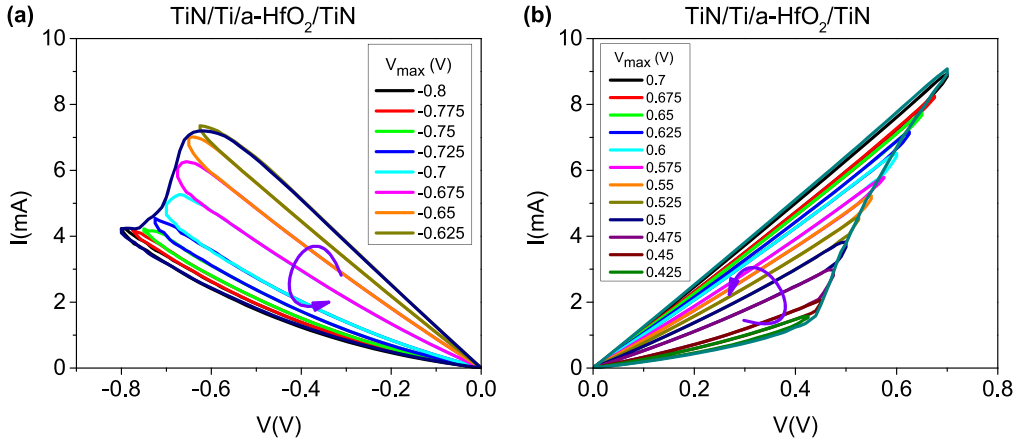

Figure 5. Accumulative I-V cycles. Erasing cycles (a). The current (I) is in absolute values. Writing cycles (b).

the previously applied programming voltage. Memory maps are the RRAM equivalent to ferromagnetic hysteresis cycles, where every state depends on the history of precedent states.

To demonstrate the analogical control of the conductance of RRAMs, we performed some writing/erasing tests. These tests were designed to be either accumulative or incremental. In the former, the first step is to apply the opposite transition from that of the experiment, to assure a start from a full initial state. After that, the corresponding write/erase cycles are run while their effects are accumulated. They are synonymous with set/reset cycles with voltage limits. On the contrary, the incremental cycles add a change to the opposite transition after each cycle, which implies that every write/erase begins at the same level. An example of accumulative I-V cycles is depicted in Fig. 5. It is important to remark that an enveloping cycle was added to demonstrate that a full cycle fits perfectly to the progressive transitions. These tests did not have any current limitation.

As it was proved before,[24] the study in terms of AC parameters, i.e., the admittance behavior of RRAM, provides relevant information about resistive switching phenomena. To do that, a small signal of 30 mV and 100 kHz was overlapped to the DC. For the sake of exemplification, we include some C-V and G-V incremental writing/erasing cycles in Fig. 6. It is remarkable the ease of control of a potential myriad of levels ranging between HRS and LRS. These characteristics strongly enable the already met objective of building neuromorphic systems with these devices.[19] Another interesting characteristic of these devices is the considerably narrow voltage range, not even reaching 1 V in either polarity. Thus, the reduced power consumption is another significant, crucial and desired advantage in this case.

Following the same method as in Fig. 4a, there are illustrated some nested cycles in Fig. 7. The reason for the negative capacitance values was proposed in the literature by relating the properties of the conductive filaments with a theoretical model which states that a device in that situation acts as a capacitance in parallel with a resistance in series with an inductance.[24,25]

In addition to our small-signal study, in a publication in collaboration with Milo et al.,[19] AC pulsed experiments were carried out over devices with the same stack structure as in this work.

Furthermore, the endurance of the devices was evaluated by applying voltage pulses in order to modify alternately the state to HRS and LRS during 2048 cycles. The results of an endurance experiment are shown in Fig. 8a, where the set and reset pulses feature an amplitude of 0.6 V and −0.8 V, respectively. Besides, in Fig. 8b the plotted resistance values exhibited an enlarging HRS vs. LRS ratio as the resistance in HRS was increasing along the iterations.

For the sake of comparison, Table I provides the HfO_2 RRAM main parameters in this work and other reported ones. Although the operating voltages in individual cells are lower than in 1T1R scheme, it must be taken into account the bigger complexity of an array structure. Also, the current did not need to be limited when

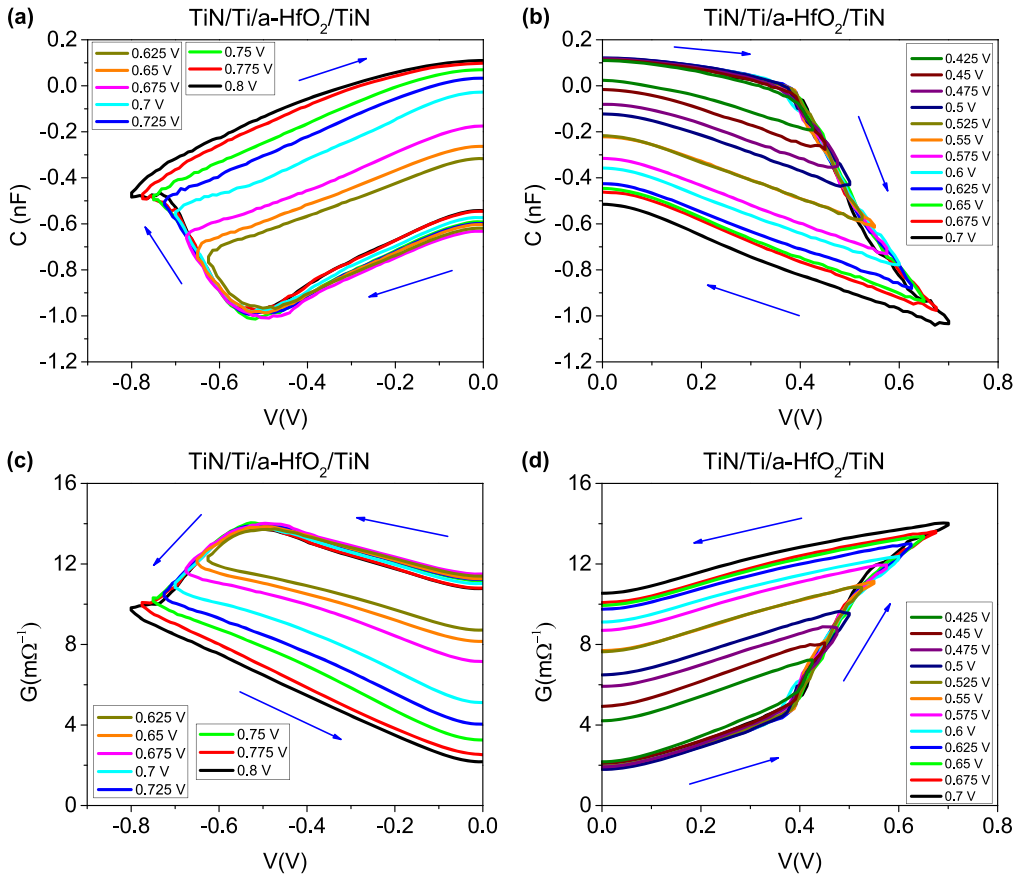

Figure 6. Incremental C-V and G-V cycles. C-V erasing (a). C-V writing (b). G-V erasing (c). G-V writing (d).

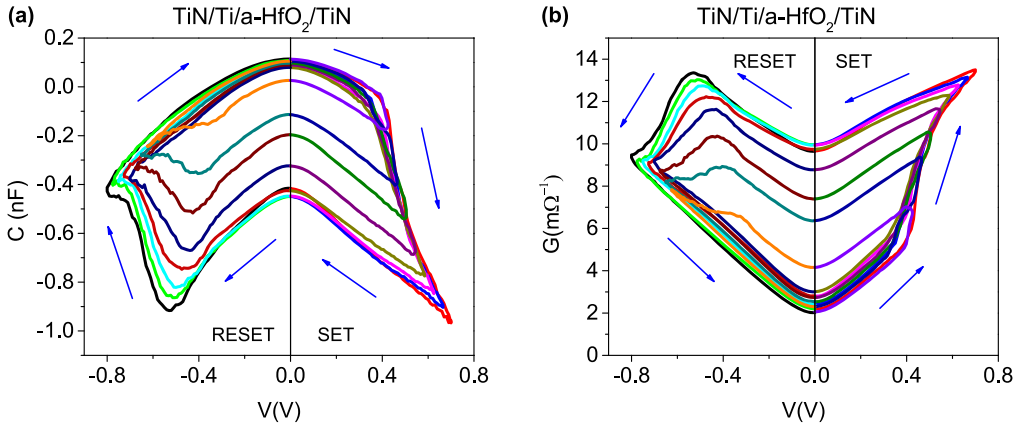

Figure 7. C-V nested cycles (a). G-V nested cycles (b).

working with individual RRAMs, but this is compulsory for controlling a network of several hundreds of memories at the same time.

Finally, with the aim of apporting more characterization results, we refer to the work from Zahari et al.[29] in which there were developed retention tests over 1T1R cells with the same structure as it is described in our study.

Conclusions

An extensive performance study in TiN/a-HfO_2/Ti/TiN devices was carried out. The dielectric composition resulted in a great yield of the resistive memories, which present a wide functional window of approximately an order of magnitude between high and low resistance states when measuring the current values at 0.1 V. Both DC and small-signal experiments showed the ease of control of the multilevel states, thus empowering its suitability for neuromorphic circuits. Additionally, the good endurance results and low power consumption of the samples may indicate a large cycle durability with good behavior, where the resistance window augmented stepwisely across the experiment. These results reinforce the prospects of these thoroughly designed devices. With respect to the comparison with other authors' results, it can be stated that the 1T1R structure is an excellent choice for integrating RRAMs into memory arrays, assuring a good control of the state changes and an improved yield.

Table I. Comparison of resistive switching characteristics among different works.

Ref. Study	Composition TE/ Dielectric/BE	Dielectric Thickness	Structure	Control Mechanism	Ratio LRS/HRS	Forming Voltage	SET/RESET Voltages
This work	TiN/HfO_2/Ti/TiN	8 nm	Individual cell	Voltage (no current limit)	~2	~2.5 V	0.7 V/−0.8 V
26	TiN/Ti/HfO_2/W	10 nm	Individual cell	Voltage (no current limit)	~15	~5 V	0.6 V/−0.8 V
19	TiN/HfO_2/Ti/TiN	8 nm	1T1R	Limited by transistor	~10	[2 V, 5 V] Maximum yield @ 5 V	1.2 V/1.8 V
27	Ti/HfO_2/TiN	10 nm	1T1R	Limited by transistor	~20	Measurements @ 380 K ~1.9 V @ pulse width = 1 s ~2.2 V @ pulse width = 0.01 s ~2.6 V @ pulse width = 100 μs	1.0 V/1.2 V
28	TiN/TaO_x/HfO_2/Al_2O_3/TiN	8 nm	1T1R	Limited by transistor	~30	~2.25 V @ 473 K (200 °C)	1.68 V/2.14 V

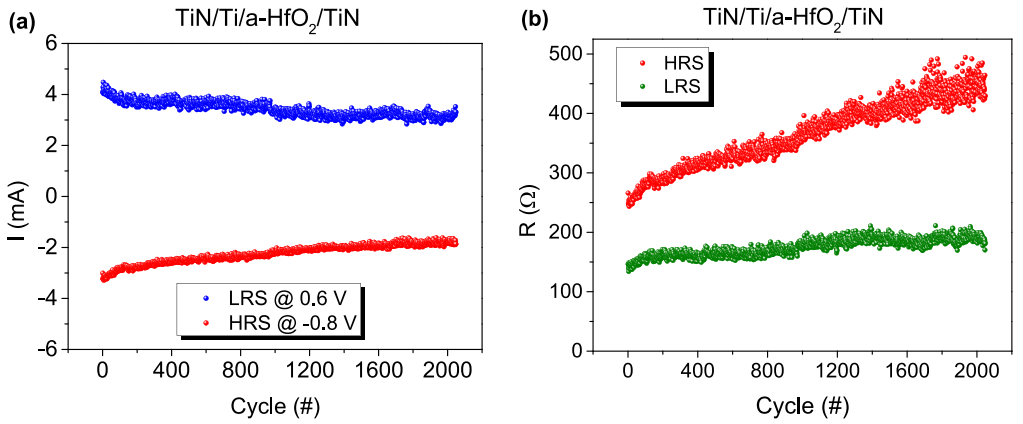

Figure 8. Current variation along an endurance test (a). Resistance variation in the endurance test (b).

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