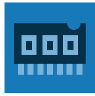 *electronic materials*

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Towards Sustainable Crossbar Artificial Synapses with Zinc-Tin Oxide

Carlos Silva [1], Jorge Martins [2,]*, Jonas Deuermeier [2], Maria Elias Pereira [2], Ana Rovisco [2], Pedro Barquinha [2], João Goes [1], Rodrigo Martins [2], Elvira Fortunato [2] and Asal Kiazadeh [2,]*

[1] Department of Electrical and Computer Engineering, NOVA School of Science and Technology and CTS-UNINOVA, NOVA University Lisbon, Campus de Caparica, 2829-516 Caparica, Portugal; cmd.silva@campus.fct.unl.pt (C.S.); goes@fct.unl.pt (J.G.)

[2] i3N/CENIMAT, Department of Materials Science, NOVA School of Science and Technology and CEMOP/UNINOVA, NOVA University Lisbon, Campus de Caparica, 2829-516 Caparica, Portugal; j.deuermeier@campus.fct.unl.pt (J.D.); mel.pereira@campus.fct.unl.pt (M.E.P.); a.rovisco@fct.unl.pt (A.R.); pmcb@fct.unl.pt (P.B.); rfpm@fct.unl.pt (R.M.); emf@fct.unl.pt (E.F.)

* Correspondence: jds.martins@campus.fct.unl.pt (J.M.); a.kiazadeh@fct.unl.pt (A.K.)

Abstract: In this article, characterization of fully patterned zinc-tin oxide (ZTO)-based memristive devices with feature sizes as small as 25 μm^2 is presented. The devices are patterned via lift-off with a platinum bottom contact and a gold-titanium top contact. An on/off ratio of more than two orders of magnitude is obtained without the need for electroforming processes. Set operation is a current controlled process, whereas the reset is voltage dependent. The temperature dependency of the electrical characteristics reveals a bulk-dominated conduction mechanism for high resistance states. However, the charge transport at low resistance state is consistent with Schottky emission. Synaptic properties such as potentiation and depression cycles, with progressive increases and decreases in the conductance value under 50 successive pulses, are shown. This validates the potential use of ZTO memristive devices for a sustainable and energy-efficient brain-inspired deep neural network computation.

Keywords: memristor; ZTO; amorphous oxide; physical mechanism; resistive switching device

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1. Introduction

With the technological landscape shifting towards big data applications, such as Internet of Things (IoT), the need to analyze and process large amounts of data in a quick and efficient manner has greatly increased in the past decade [1]. The typical Von-Neumann architecture used on most current systems requires that the processing and memory units are independent of each other and connected by a data bus. This means that although the processing power of these systems has been improved over the last few years, it is not possible to take advantage of all its capabilities due to the limited bandwidth of the data bus (Von-Neumann bottleneck). When taking scalability into account, these systems also pose a problem due to the decrease in performance that comes as a consequence of CMOS technology limitations [2]. The increase in operating frequency and device density would involve a higher power consumption and increased operating temperatures. For most neuromorphic applications such as pattern recognition, portable systems do not process their data locally but instead are connect to an external computer server ("cloud") that handles the data processing. This implies not only large power consumption but also a possibly unsafe transfer of data that might be undesirable when handling sensitive information. As an alternative, brain-inspired neuromorphic computation systems have been presented. The human brain consists of computing elements (neurons) and memory elements (synapses) that are connected in a massive parallel architecture. This parallelism allows the brain to outperform modern processors in tasks such as data classification and

pattern recognition while being considerably more power efficient [3]. In order to emulate this highly interconnected network, dense arrays of memristors have been proposed. These two-terminal devices have been shown to emulate a variety of synaptic properties such as potentiation and depression, which are key characteristics of artificial neural networks (ANNs) [4].

Both the industrial and research communities have recently started to take an interest in non-filamentary resistive switching [5,6]. This interest is in great part not only due to the analog switching behavior that is shown in area-dependent mechanisms, but also because filament formation and destruction is not needed for switching to occur, leading to better device reliability [7]. Amorphous oxide semiconductors (AOS) are ideal materials for non-filamentary-based resistive switching [8,9]. These materials allow for an easier and cheaper production process than current market technologies while maintaining compatibility with CMOS processes [10].

When taking neuromorphic applications such as pattern recognition into account, it was shown that a better accuracy is achieved due to a lower random telegraphic noise of area-dependent memristors, compared to filamentary systems [11]. Besides that, by applying AOS-based material as the resistive switching material, flexible and transparent substrates such as plastic or paper can be used due to low processing temperatures and conventional patterning methods [12], which are great advantages for applications such as IoT. The most prominent AOS material in recent literature has been indium-gallium-zinc oxide (IGZO) [12–14]. This material has shown synaptic operations which can be applied for both computing paradigms of deep neural networks (DNNs) and spiking neural networks (SNNs). However, due to indium and gallium both being critical raw materials, the use of zinc-tin oxide (ZTO) has started to be considered as a reliable substitute [15–18]. There are few reports on ZTO memristive devices with synaptic capabilities [19,20], and even fewer using exclusively ZTO as their switching medium [21,22], with all sharing a common bottom electrode configuration. Although patterned ZTO devices have previously been presented [23], synaptic emulation and area dependent switching was never achieved in a crosspoint configuration and the smallest device area has been reported as 100 μm^2. Table 1 sumarizes the current state of the art and relates it to the current work. It is also worth noting that materials with other possible resistive switching mechanisms have been reported such as photo-induced [24], electrolyte gated [25] and second- and third-order effects [26].

Table 1. Benchmark table of amourphous oxide semiconductor-based memristive devices.

Year/Ref.	Switching Material	Structure	BE/TE Interface	Electrical Behavior	Switching Mechanism	Switching Behavior	RON/OFF	Retention (s)	Endurance (Cycles)	Synaptic Functions
2021 [current work]	ZTO	Crosspoint	Pt/Au	Bipolar	Area-dependent	Gradual and Abrupt SET/Gradual RESET	>10^2	-	100	Yes
2021 [21]	ZTO	Common BE	ITO/ITO	Unipolar/ Bipolar	Filamentary	Gradual and Abrupt SET and RESET	≈10^3	10^3	150	Yes
2021 [22]	ZTO	Common BE	TiN/Ta	Bipolar	Filamentary	Gradual SET and RESET	>10	>10^4	2000	Yes
2020 [18]	ZTO	Common BE	Pt/Au	Bipolar	Filamentary	Abrupt SET and RESET	≈10^3	10^5	100	-
2020 [18]	ZTO	Common BE	Pt/Au	Bipolar	Area-dependent	Abrupt SET/ Gradual RESET	>10	-	100	-
2020 [18]	ZTO	Common BE	Pt/Au	Unipolar	Filamentary	Abrupt SET and RESET	>10^3	10^5	50	-
2020 [19]	ZrO_2/ZTO	Common BE	TiN/Ta	Bipolar	Filamentary	Abrupt SET/Gradual RESET	≈10^2	-	100	Yes
2020 [20]	SnO_2/ZTO	Common BE	TiN/W	Bipolar	Filamentary	Gradual SET and RESET	>10	-	300	Yes
2020 [12]	IGZO	Crosspoint	Mo/Mo	Bipolar	Area-dependent	Gradual SET and RESET	≈10^2	-	-	Yes
2017 [14]	IGZO	Common BE	Ti/Ag	Bipolar	Filamentary	Abrupt and Gradual SET and RESET	>10	10^4	100	-
2013 [23]	ZTO	Crosspoint	Pt/Al	Bipolar	Filamentary	Abrupt SET and RESET	>10^3	> 10^3	50	-
2013 [27]	IGZO	Common BE	Pt/TiN	Bipolar	Filamentary	Abrupt SET and RESET	>10^2	10^3	150	-
2012 [28]	IGZO	Common BE	Pt/Pt	Bipolar	Area-dependent	Gradual SET/ Gradual RESET	≈10	-	-	Yes

For real-world applications, device cross bar implementations are necessary. Therefore, the first step is to obtain reliable device characteristics where both electrode contacts are patterned in a cross-point configuration. In the current report, full patterning of the contact layers of the devices was completed by lift-off.

Formerly, we have shown that non-patterned ZTO devices with common bottom Pt electrodes operate in two different modes of resistive switching (RS) [18]: 1D or filamentary (which requires electroforming) and 2D or area-dependent RS. Here in this article, we are focused on the area-dependent resistive switching properties of the device where the electroforming is not required. The characteristic was introduced as 8-wise RS in the literature [29]. However, this implies the application of the voltage to the Schottky contact. In order to use a more universal terminology, the above-mentioned switching mode is referred to as "forward set", since the set operation happens in the diode's forward directions [17].

2. Materials and Methods

The fabrication of the presented ZTO memristive devices started with the patterning of the bottom electrodes via lift-off. E-beam evaporation was used for the deposition of 30 nm of Pt paired with another 30 nm thick layer of Ti that served as an adhesion layer between the substrate and the Pt. For surface cleaning purposes and to ensure a good rectification in the pristine state [18], an O_2 plasma treatment was performed on the bottom electrode in situ moments before the deposition of the active layer. For this treatment, a substrate bias of 10 W was applied with a flow rate of 20 sccm of O_2 for a duration of 10 min. For the active ZTO layer, the radio frequency (RF) magnetron sputtering process was used. The deposition was carried out at room temperature, with a flow rate of 20 sccm of Ar and 20 sccm of O_2, an RF power of 160 W and a deposition pressure of 2.3 mTorr. Using these conditions, an 80 nm layer of ZTO was deposited in 18 min. For the top electrode, both deposition and patterning techniques were the same as the ones used for the bottom electrode. For this electrode, a 60 nm Au layer was deposited on top of a 6 nm Ti layer. After fabrication, the devices went through an annealing process of 120 °C for a period of 24 h.

The devices were measured in a dark environment, under ambient atmosphere, using a Keithley 4200-SCS semiconductor characterization system and a Janis ST-500 cryogenic probe station (Lake Shore Cryotronics, Westerville, OH, USA). The voltage was applied to the top electrode while the bottom electrode was grounded. For these conditions, the ZTO thin film presents an amorphous structure (Figure S1). X-ray diffraction (XRD) measurements were performed in a PANalytical's X'Pert PRO diffractometer (Malvern Panalytical, Malvern, UK) using CuKα radiation with 2θ between 5° and 65° and a step size of 0.033°.

3. Results

All presented measurements were performed in 5 μm × 5 μm devices unless stated otherwise. The current–voltage (I–V) characteristics between −1 V and 1 V (pristine) of the patterned (area: 25 μm^2) and non-patterned (area: 0.2 mm^2) devices are presented in Figure 1a, along with a graphical illustration of the patterned device structure. The electrical characteristics of the patterned and non-patterned devices are similar, besides the different overall current level due to the device area. Additional area dependency of the resistance switching is shown in Figure S2. The polarity of the rectification reveals the presence of a Schottky-like barrier at the ZTO/Pt interface, as expected [18], while the Ti/Au interface is Ohmic. Hence, applying negative voltage (to the top electrode) corresponds to a forward biasing of the device. In Figure 1b, the direct current (DC) resistive switching behavior is shown. The current–voltage characteristics demonstrate the forward set bipolar switching nature of the device, with its set operation occurring under negative voltage bias, and the reset on the opposite polarity. The resistive switching window of the patterned devices is two orders of magnitude.

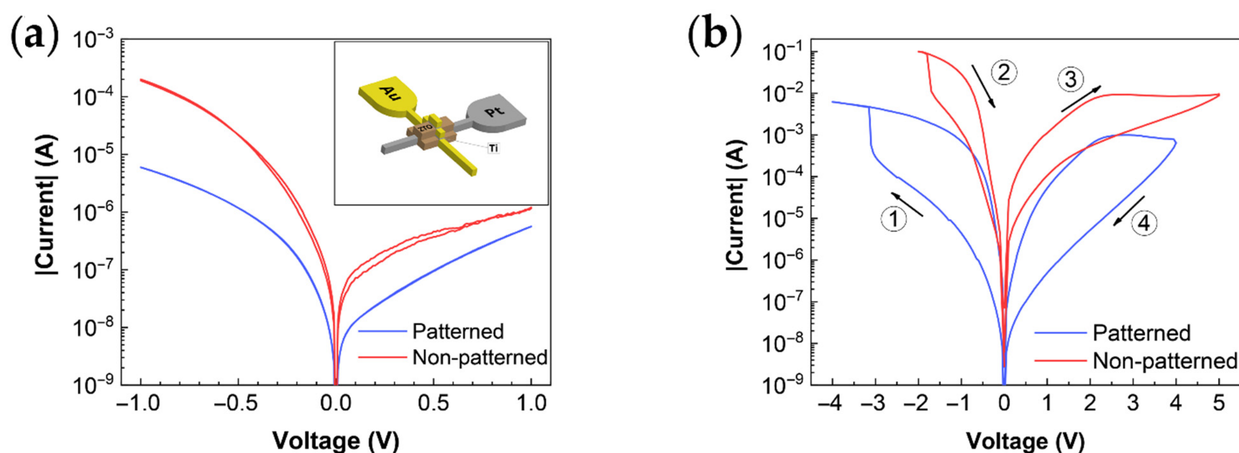

Figure 1. (**a**) Pristine state of patterned (area: 25 μm^2) and non-patterned devices (area: 0.2 mm^2); patterned device structure (inset); (**b**) resistive switching current–voltage characteristics of patterned and non-patterned devices.

The forward set characteristic of ZTO memristive devices reveal retention loss [18]. The dynamic retention data is presented in Figure S3 This characteristic is beneficial for artificial neural networks, especially in sequence-to-sequence models [30].

Device endurance was initially tested by performing voltage sweeps between −4 and 4 V (Figure 2a); however, after the first few cycles, the device remained in the HRS, followed by an uncontrolled breakdown. Figure 2b shows a controllable resistive switching performance by combination of current sweep and voltage sweep for set and reset operations, respectively. This endurance plots are shown in a semi logarithmic scale in Figure S4. As shown in the Supporting Information, Figure S5, a higher maximum current range close to the values measured during voltage sweep does not negatively influence the cycle-to-cycle stability. The current-controlled set was already reported to lead to increased endurance for both valence change memory (VCM) and electrochemical memristor (ECM) cells [31].

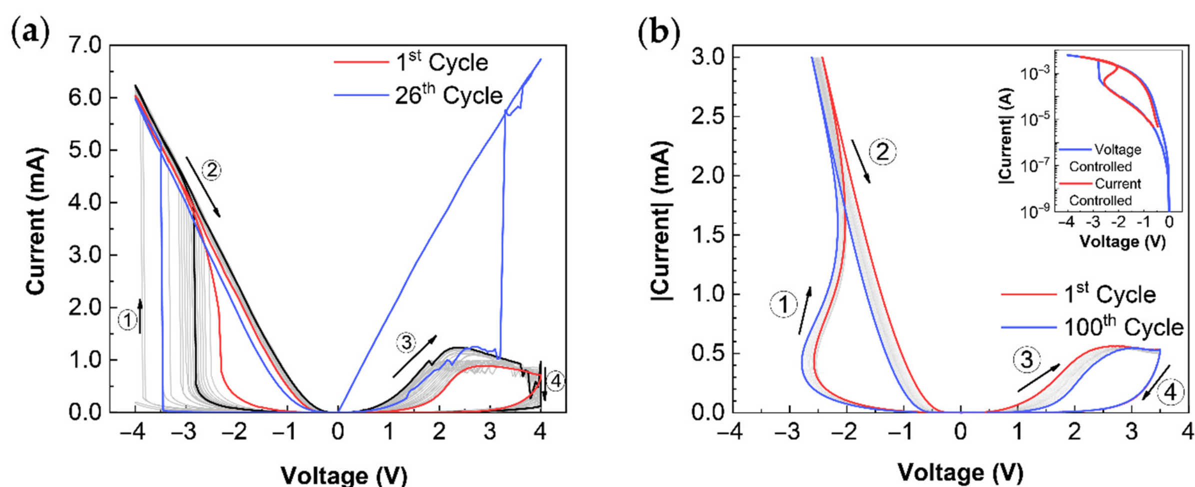

Figure 2. Device endurance testing. (**a**) Voltage-controlled SET and RESET dual-sweep cycling between −4 V and 4 V; (**b**) current-controlled SET dual-sweep cycling between 0 A and −0.003 A and voltage-controlled RESET dual-sweep cycling between 0.0 V and 3.5 V; comparison between current and voltage-controlled SET operations in semi-log scale (inset).

In a biological brain, neurons communicate through synapses. Under stimulation of synapses by neural spikes, they update their strengths or weights, which are realized as potentiation and depression [32]. To replicate this behavior, pulsed signals were applied to the ZTO memristive devices, leading to a change in their conductance value. The gradual set response was analyzed by setting with various pulse amplitudes, with a fixed pulse width of 3 ms, as shown in Figure 3a. Different pulse widths for a fixed pulse amplitude of −2.2 V are presented in Figure 3b. The higher widths and voltage amplitude result in higher on/off ratios within smaller numbers of pulses. Typical potentiation and depression properties, obtained through the progressive increase and decrease in the conductance under the application of 50 successive pulses, are shown in Figure 3c,d, with pulses in ms and µs, respectively.

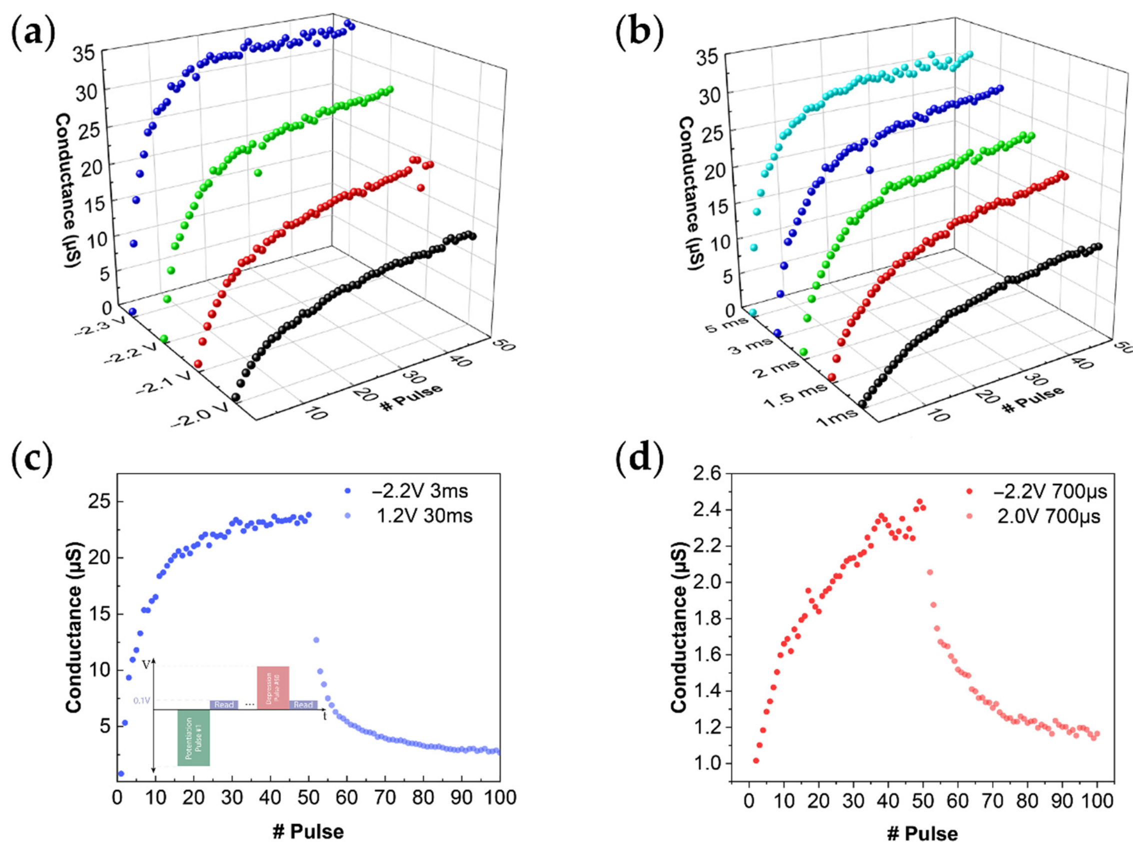

Figure 3. (**a**) Conductance value response to 50 pulses with a fixed 3 ms width with varying amplitudes; (**b**) conductance value response to 50 pulses with a fixed −2.2 V amplitude with varying widths; (**c**) device potentiation and depression response over ms pulsing, pulse scheme used for measuring (inset); (**d**) device potentiation and depression response over µs pulsing.

To investigate the operation of the forward set resistive switching, the temperature dependence of the current–voltage characteristics of the low-resistance state (LRS) and high-resistance state (HRS) was analyzed, respectively. In the temperature range used (between room temperature and 430 K), no thermally induced atomic rearrangement of the materials is expected due to the prolonged annealing used during fabrication. While this analysis was performed for the non-patterned devices, the conduction mechanisms should be the same for the patterned devices, based on the identical I–V characteristics shown in Figure 1b. The I–V characteristics for both HRS and LRS are presented in Figure 4a (by the symbols), in which the voltage is presented in the forward direction of the diode. In the LRS, the conduction is clearly dominated by thermionic emission, which shows that the

Schottky-like barrier at the ZTO-Pt interface is dominantly limiting the conduction. Under the thermionic emission, the current density, j, is defined by:

$$j = A^* T^2 \exp\left(-\frac{\phi_B}{k_B T}\right)\left[\exp\left(q\frac{V - R_S I}{\eta k_B T}\right) - 1\right] \quad (1)$$

in which I is the current, V is the voltage, T is the temperature, ϕ_B is the Schottky barrier heigh, R_S is the series resistance, η is the ideality factor, A^* is the effective Richardson constant, k_B is the Boltzmann constant and q is the elementary charge. The lines in the LRS curves in Figure 4a are the fitted curves described by this model (which followed the procedure described by Werner et al. [33]). The temperature dependence of the Schottky barrier (Figure 4b) describes its inhomogeneity [34], by assuming a Gaussian distribution per $\phi_B^{eff} = \phi_B^m - \frac{\sigma_B^2}{2k_B T}$, where ϕ_B^m is the mean barrier height, σ_B the standard deviation and ϕ_B^{eff} is the effective barrier, which is lower than the mean value as charge carriers will pass preferably through lower barrier regions. The temperature dependency of the ideality factor is given by $\eta = \frac{1}{1-\rho_2+\frac{\rho_3}{2k_B T}}$, in which ρ_2 and ρ_3 describe the linear voltage dependencies of ϕ_B^m and σ_B^2, respectively. The values obtained with this model, summarized in Table 2, are consistent with other reports: while ρ_3 is negative for most Schottky contacts, ρ_2 is positive for Schottky diodes using ZnO [35]. ϕ_B^m is higher than most ZTO Schottky contacts reported by Schlupp et al. (with a similar σ_B) [36].

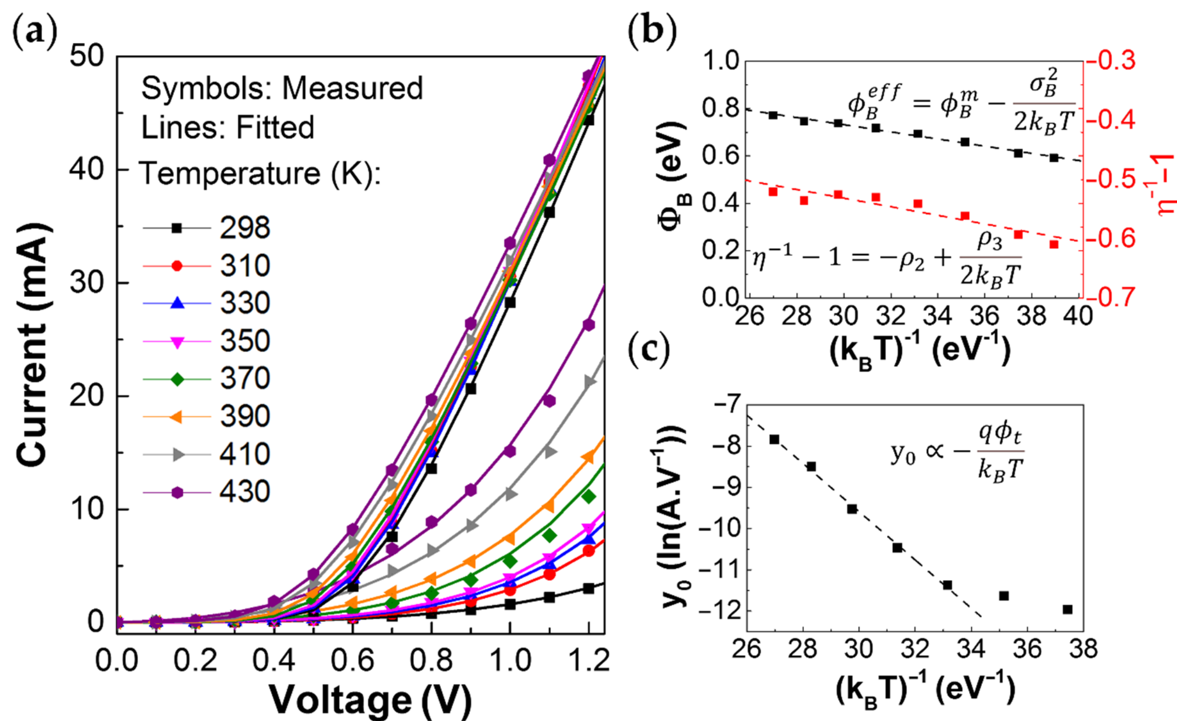

Figure 4. Thermal dependence of the ZTO memristive devices. (**a**) Measured current–voltage characteristics of the LRS and HRS (symbols) and corresponding modeled curves (lines) using the thermionic emission and Poole–Frenkel conduction. (**b**) Temperature dependence of the effective barrier height and the ideality factor. (**c**) Temperature dependence of the $\ln(I/V)-V^{1/2}$ curves y-axis intercept, associated with the energy level of the traps.

Table 2. Mean Schottky barrier height (φ_B^m), standard deviation (σ_B), and their voltage dependencies (ρ_2, ρ_3), for the LRS.

ϕ_B^m (eV)	σ_B (eV)	ρ_2	ρ_3 (meV)
1.186	0.169	0.314	−13.7

The measured current levels in the HRS showed a strong thermal activation as shown in Figure 4a (symbols). This was found to be consistent with Poole–Frenkel emission, and the modeled curves are presented by the lines in Figure 4a, following

$$J = q\mu N_C E \cdot \exp\left[-q\frac{\left(\phi_t - \sqrt{\frac{qE}{\pi\varepsilon_r\varepsilon_0}}\right)}{k_B T}\right] \quad (2)$$

in which μ is the electron mobility, N_C is the effective density of states for electrons in the conduction band, E is the electric field, ε_r is the relative permittivity of ZTO, ε_0 is the vacuum permittivity and $q\phi_t$ is the energy level of the traps [37]. The latter was extracted as 0.59 eV, as shown in Figure 4c, in which y_0 is the y-axis intercept of the $\ln\left(\frac{J}{E}\right) - \sqrt{E}$ curves (see Figure S6), which is proportional to $-\frac{q\phi_t}{k_B T}$. The sub-Arrhenius behavior at low temperature may indicate a transition from the temperature-activated Poole–Frenkel emission to quantum mechanical tunneling through the potential energy barrier between the defect sites.

4. Discussion

It is interesting to note that while the LRS shows an electrode limited mechanism (with a low series resistance), the HRS shows a bulk limited mechanism. This could signify a modulation of at least a significant part of the bulk ZTO region, which could be given, for example, by the redistribution and/or creation of defects or dopants. Analyzing the endurance failure when using voltage sweep for the set operation (see Figure 2a) makes it possible to obtain deeper insight: In conventional reverse set (or counter-eight-wise [29]) VCM-type memristors, it is proven that reset failure within the cycling is related to low energy defect formation of the electrode at the Ohmic side of devices due to the excess of oxygen vacancy generation during cycling, causing the device to remain in the LRS [38]. When using voltage sweeps, the set operation is not self-limited (as opposed to the reset operation), thus presenting the critical factor in reducing the DC endurance. As opposed to the reverse set operation, the endurance-limiting set operation in the devices presented here occurs under negative polarity applied to the Ohmic electrode, which cannot lead to the additional creation of defects in the Ohmic region. Instead, the bulk limited HRS becomes more resistive, and the set voltage increases, indicating a reduction in the bulk dopant concentration. Interestingly, the increase in HRS resistance is accompanied by a decreased LRS resistance. Since the conduction in the LRS is limited by the Schottky barrier, it is concluded that the concentration of dopants at the Schottky interface is increased by the voltage sweep cycling. This conclusion is consistent with the creation of dopants at the Ohmic side in reverse set VCM, differing only in that it happens at the Schottky interface for forward set switching, in line with observations of oxygen exchange at the Pt electrode [39]. The existence of metallic tin near the platinum bottom contact, verified by a previous in-depth XPS analysis [18], corroborates with the hypothesis of defect creation at the Schottky contact. When the current sweep is applied for the set operation, a more stable and uniform device operation is observed, as shown in Figure 2b. The most significant difference to setting the device by voltage sweep is the stabilization of the HRS and, consequently, lower set voltage variation.

5. Conclusions

In this article, fully patterned two-terminal memristive devices with an active ZTO layer were successfully built and tested. Electroforming-free switching behavior was confirmed through I–V testing. Device endurance of 100 cycles is obtained by performing current-controlled SET switching. It is presented that the gradual resistive switching events on both set and reset polarities can be achieved by tuning the pulse parameters of voltage amplitude and pulse width. Neuromorphic capabilities were replicated, showing potentia-

tion and depression responses using pulses in the range of milli and microseconds. The conduction mechanisms of the LRS and HRS in this operation mode were identified as thermionic emission and Poole–Frenkel emission, respectively, suggesting a significant modulation of the ZTO bulk region during resistance switching transition. The uncontrollable set operation by voltage sweep in forward set VCM-type switching is responsible for the creation of excess defects at the Schottky contact and a substantial increase in bulk resistivity. Using current sweeps for the set operation, the defect creation at the Schottky contact can be avoided and the increase in bulk resistance becomes less pronounced, leading to higher device endurance.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/electronicmat2020009/s1, Figure S1: XRD characterization of ZTO thin film. Figure S2: Area-scaling of the patterned device in comparison with the results of a previous study. Figure S3: Typical dynamic retention time of the device after DC sweep set and 10 and 50 voltage pulses with an amplitude of −3 V and a width of 3 ms. Figure S4: Current-controlled (a) and voltage-controlled (b) sweep cycles in semi-log scale. Figure S5: Typical device-to device variation in a row of devices with size of 25 μm^2 testing (a, b, c) under voltage sweeping and (d, e) current sweeping. (f) Cycle-to-cycle variation obtained from typical voltage-sweeping cycles. Figure S6: $\ln\left(\frac{J}{E}\right) - \sqrt{E}$ curves, and linear fitting, under the P-F emission. Table S1: Relaxation time characteristic associated with different SET operations.

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