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Design of a Low Power Transmitter for UWB Applications

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I would like to dedicate this thesis
to those who supported me, my family, Mehrnoush and Diana
and
to those who taught me hardworking, my Parents

Abstract

Emerging technologies, like ubiquitous computing and Internet-of-Things (IoT) create opportunities in the realm of information and communication technology, in which a large number of micro-devices with communication and/or computing capabilities, provide connectivity for anything, by any one at any time and any where. Especially, these devices can be equipped with sensors and actuators that interact with our living environment. Barcode, smart contact-less card, Radio Frequency Identification (RFID) systems, wireless sensor network (WSN), and smart mobile phones are some examples which can be utilized in ubiquitous computing. Ubiquitous sensors are enablers of IoT systems and they need some specific features such as low-cost and small-size implementation, non-line of sight operation, sensing possibilities, data storing ability, and positioning. However, there are several challenges which need to be addressed, such as limited life time for battery powered devices, maintenance cost, higher data rate, and operation in dense multipath and multi-user environment. Bluetooth low-energy (BLE) and ultra wideband (UWB) technologies can be used in the design of wireless sensors. Bluetooth low-energy provides reliability and simpler network infrastructure, however, it is still necessary to put effort on designing sensor nodes that are more efficient, specially for battery-less sensor nodes. On the other hand, although ultra wideband (UWB) has lost most of its initial interest, mainly for not being able to keep-up in the market with competing technologies, it can still be useful in niche applications, as long as it keeps to the promises of lower complexity and higher power efficiency. Impulse-radio ultra wideband (IR-UWB) technique has the possibility of achieving Gb/s data rate, a few meters operation range, pJ energy per bit, centimeter accuracy of positioning, and low cost implementation.

The main contribution of the thesis is to replace conventional A/D Converter by integrate-and-fire modulation and using it in UWB wireless communication. The design mostly focuses on low-cost and low-power implementation, because the amount of power that any IR-UWB transmitter dissipates is directly proportional to the amount of data that it is going to send. In order to decrease the amount of produced data and lowering the power consumption, an integrate-and-fire (IFN) modulation technique and IR-UWB are joined in a system called integrate-and-fire impulse-radio (IRIF) transmitter. The modulator directly converts an analog signal to a bitstream. Then, a logic interface stores the data into memories, compress them in time, makes packets, and applies a command signal to an IR-UWB pulse generator.

Also, in a system-level study, the power efficiency of the IRIF transceiver is attested for a random Gaussian signal, and compared with the conventional A/D based systems.

The results show 12 and 6 times less power consumption in comparison with BPSK and OOK modulations, respectively. This study includes a link budget and it shows that the transmission range of such system will be around 1 m if a bit error rate (BER) of 8×10^{-4} is considered.

Furthermore, a very low power LC-tank based pulse generator is designed. It covers -10dB bandwidth of 4.8 GHz within the range of 3.7 GHz to 8.5 GHzand complient with FCC mask. Its measured peak power equals to -42.8 dBm/MHz. Each UWB impulse dissipate 8.16 pJ energy measured at a pulse repetition frequency (PRF) of 100 MHz.

Last but not the least, the system is silicon proved and fully implemented on a single CMOS chip. A sinusoidal function with frequency of 1 kHz is applied to the system as an input. A printed circuit board (PCB) has been designed for chip-on-board (CoB) measurement approach. Signal reconstruction is performed and the PSD calculation represents ENOB of 5.8 bits while the input signal itself holds that of 6.56 bits. To estimate the transmission range, two horn antennas with the gain of 8 dB over the range of 3.1 GHz to 10.6 GHz are used for transmit and receive. After all, the transmission range of 3 meters is measured while having SNR of 10 dB at the receiver.

Keywords: Impulse-Radio Ultra Wide-band (IR-UWB), Integrate-and-Fire Neuron (IFN), Wireless Sensor Nodes (WSN), Integrate-and-Fire Impulse-Radio (IRIF) Transmitter

Resumo

Tecnologias emergentes, como a computação ubíqua e a Internet das Coisas (IoT) criam oportunidades no campo da tecnologia de informação e comunicação, em que um grande número de micro-dispositivos com recursos de comunicação e/ou computação oferecem conectividade para qualquer coisa, a qualquer momento e em qualquer lugar. Especialmente, esses dispositivos podem ser equipados com sensores e atuadores que interagem com o ambiente. Código de barras, cartão inteligente sem contato, sistemas de identificação por radiofrequência (RFID), rede de sensores sem fio (WSN) e telefones celulares inteligentes são alguns exemplos que podem ser utilizados em computação ubíqua. Os sensores ubíquos são facilitadores dos sistemas de IoT e precisam de alguns recursos específicos, como implementação de baixo custo e pequena dimensão, operação fora da linha de vista, possibilidades de detecção, capacidade de armazenamento de dados e posicionamento. No entanto, há vários desafios que precisam de ser resolvidos, como o tempo de vida útil limitado em dispositivos alimentados por bateria, custo de manutenção, faixa de operação mais longa, maior taxa de dados e operação em ambientes *multipath* e multi-usuário densos. Tecnologias Bluetooth de baixa energia (BLE) e *ultra wideband* (UWB) têm vindo a ser apontadas no projeto de sensores sem fio. O Bluetooth de baixa energia fornece confiabilidade e infra-estrutura de rede mais simples, embora ainda sejam necessários mais esforços para tornar os sensores ubíquos mais eficientes, devido principalmente à arquitetura complexa e aos componentes que consomem muita energia. Por outro lado, embora o UWB tenha perdido a maior parte do seu interesse inicial, principalmente por não conseguir manter-se competitivo no mercado face a tecnologias concorrentes, ela pode ainda ser útil em aplicações de nicho, desde que mantenha a promessa de menor complexidade e maior eficiência energética. A técnica de banda ultra-larga de impulso de rádio (IR-UWB) tem a possibilidade de alcançar taxas de dados de Gb/s, alguns metros de alcance de comunicação, baixa energia por bit, precisão de posicionamento e implementação de baixo custo.

A contribuição deste trabalho é a realização de um transmissor IR-UWB completo para aplicações de IoT, com foco na implementação de baixo custo e baixo consumo de energia. A quantidade de energia que qualquer transmissor IR-UWB dissipa é diretamente proporcional à quantidade de dados que vai enviar. A fim de diminuir a quantidade de dados produzidos e reduzir o consumo de energia, uma técnica de modulação de integração e disparo (IFN) e IR-UWB são unidos num sistema designado transmissor de impulso por rádio integrado (IRIF). O modulador converte diretamente um sinal analógico numa sequência de bits/impulsos. De seguida, uma interface lógica armazena os dados em

memórias, comprime-os, gera pacotes e aplica um sinal de comando a um gerador de impulsos IR-UWB. As características do modulador de IFN são estudadas. O estudo mostra que o transmissor IRIF é capaz de diminuir a necessidade de energia para transmitir uma determinada janela de informação, quando comparado com a transmissão de informação binária equivalente com modulações típicas de UWB. Além disso, o transmissor também relaxará a necessidade de conversores A/D. Um estudo ao nível de sistema, incluindo um *link budget* foi realizado para melhor estimar a funcionalidade do transceptor. Tal estudo mostra que o alcance de transmissão de tal sistema será à volta de 1 m se um BER (*bit error rate*) de 8×10^{-4} for considerado. O gerador de pulsos funciona praticamente na faixa de 3,1 a 8,5 GHz, nomeadamente com 4.8 GHz de banda, definida a -10 dB. Cada impulso UWB dissipa 8.16 pJ, medido a uma razão de repetição de impulsos de 100 MHz. Um sinal sinusoidal com a frequência de 1 kHz é usado como entrada do sistema. O sinal é depois reconstruído e a após a determinação da PSD, o ENOB resultante de 5,8 bits foi alcançado, para um sinal de entrada que apresenta um ENOB de 6,56. Utilizando um par de antenas corneta, com gama de 3.1 GHz to 10.6 GHz e ganho 8 dB, verificou-se o alcance de 3 m para um SNR de 9 dB na receção.

Keywords: Impulse-Radio Ultra Wide-band (IR-UWB). Integrate-and-Fire modulation. Wireless Sensor Nodes (WSN). Ubiquitous Sensor Nodes (USN).

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"It was not about what is covered, it is about what is left uncovered."

Prof. Walter Hendrik Gustav Lewin

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List of Abbreviations

UWB	Ultra Wide-band
WSN	Wireless Sensor Network
SN	Sensor Node
IoT	Internet-of-Things
IR-UWB	Impulse-Radio Ultra Wide-band
IR	Impulse-Radio
IFN	Integrate-and-Fire Neuron
IFM	Integrate-and-Fire Modulator
IRIF	Integrate-and-Fire Impulse-Radio
BAN	Body Area Network
WBAN	Wireless Body Area Network
WPAN	Wireless Personal Area Network
BLE	Bluetooth Low-Energy
ENOB	Effective Number of Bits
SNR	Signal-to-Noise Ratio
SINAD	Signal-to-Noise Distortion Ratio
SER	Signal-to-Error Ratio
erfc	complementary error function
ADC	Analog-to-Digital Converter
EH	Energy Harvester
RFEH	Radio Frequency Energy Harvester
MEMS	Micro-electro Mechanical Systems
FCC	Federal Communication Commission
MB-UWB	Multi-Band Ultra Wide-band
OFDM	Orthogonal Frequency-Division Multiplexing
EIRP	Effective Isotropic Radiated Power
BPSK	Binary Phase Shift Keying
PPM	Pulse Position Modulation
PAM	Pulse Amplitude Modulation
OOK	On-Off Keying

BER	Bit Error Rate
BPF	Band Pass Filter
DWG	Distributed Waveform Generator
TDC	Time-to-Digital Conversion
PWM	Pulse Width Modulation
PDM	Pulse Density Modulation
PCM	Pulse Code Modulation
TEM	Time Encoding Machine
PSD	Power Spectral Density

Chapter 1

Introduction

This chapter presents the problem and motivation behind the solution discussed in this dissertation. It is accompanied by a background to give the necessary research context, and the proposed solution is briefly described. A review of relevant published articles related to the developed work is also carried out. It focuses on low-power data transmission for autonomous sensor nodes and discusses different subjects, namely wireless sensor networks (WSN), the impulse-radio ultra wide-band (IR-UWB) transmitters, in the range of 3.1 GHz-10.6 GHz band, and also discusses data conversion in low-power wireless sensor nodes and the most common modulation techniques for remote monitoring with IR-UWB systems.

1.1 Introduction and Motivation

Sensing can be viewed as the process of getting information from physical phenomena. Such information is vital for decision-making and automation in a variety of situations. Examples are found in environment monitoring for pollution control, wildfire surveillance and prevention, and medical monitoring with body area networks (BAN). Typically, the needed sensing area is bigger than the sensor range, meaning that many of these systems need to be organized in sensing networks, in order to improve information quality about the phenomenon (e.g. medical monitoring with sensors spread on a body area). The internet-of-things is an embodiment of this idea. It is a concept where objects are linked together and self-organized in autonomous communication networks that operate without direct human intervention. By 2020, it is expected that more than $260 billion will be spent on the IoT market [3]. Sensor networks will become important enablers of IoT and has garnered an increasing attention in the last few years, thanks to the enormous growing of potential applications worldwide.

The wireless sensor network (WSN) then becomes the central player in making these concepts a reality. Actually, this is more than a concept in present days, but some fundamental problems still persist. Given that these networks may become massive, cost effectiveness is extremely important and the need for direct human intervention has to be avoided. This means that ideally the WSN elements, the sensor nodes (SN), should be autonomous, thus capable of self-energizing or at least should last a very long time without the need for a battery change. Energy consumption is then a key figure of merit when devising the supporting hardware for the SN. The demand for low-energy systems with communication support is probably the biggest challenge faced when designing WSNs that ought to be autonomous. Its limitation is greatly related to the communication unit that is responsible for a good slice of power consumption in SNs.

A communication system with autonomous features then can realize WSN in the framework of IoT. The SNs in such network are to be produced in large quantity at relatively low-cost per unit, with such a low-power consumption that can potentiate a system capable of operating with energy harvested from the surrounding. Keeping this statement as a guideline, and since it is at the transmitter on the sensor side where the power consumption is more critical, the outcome of this work is an energy efficient, reliable, low-cost transmitter solution for wireless sensor applications.

1.2 Background

With the sprout of modern wireless technologies in 1980s and 1990s, sensors eventually became integrated with wireless platforms. In earlier designs [4], [5], [6], sensors were developed mostly using a single frequency resonator, where the resonant frequency is shifted based on the sensing mechanisms. Such sensors are useful for temperature monitoring and provided low-cost and efficient solutions for different industrial processes. Later, in 1999, due to the improvements in micro-electro mechanical systems (MEMS) technology and large scale integration capabilities, the idea of "smart dust" was introduced [7]. As data networks evolved, also the broader sense of need for networked sensor solutions gained strength. To meet the new challenges, technologies intended for data and voice communication were adopted for WSNs. This resulted in the inclusion of computing power to the sensor node, with a consequent increase in power consumption [8]. In the last few years, due to recent development in cloud computing and data analysis capabilities, various applications for WSNs, like IoT, show a new horizon.

1.2.1 Low-power challenges in WSNs

Numerous and various application scenarios will be supported by IoT. It implies the production and deployment of a large number of sensors, which will produce a huge amount of data that need to be transferred and uploaded to a central collective node, or to the cloud, for further processing. Due to maintenance cost and limited life-time of battery-powered sensors, not surprisingly, a huge effort is being carried out on designing battery-less SNs, specially for applications where the sensors stand in hard-to-reach places. Thus, the designed sensors must be very conservative in terms of power usage, implying, to a large extent, the transference of most of the complexity to the receiver side. For example, by moving the more intensive and demanding processing tasks to a central node that collects data from several SNs.

From the very beginning, in sensor nodes, four basic building blocks were considered for sensing, processing, transmitting and receiving, and power management [8] (Fig. 1.1). After nearly two decades, this architecture is still alive and under improvement. The power unit may contain energy harvester (EH) and a power management unit; EH blocks might use radio frequency or other energy sources such as solar panels, temperature, pizo-electric and so forth [9], [10]. Radio frequency energy harvesters (RFEH) are of two types: those that use different frequency band for data link and the energy harvesting link [11], [12], and those that use a single band for both data and power links [13], [14], [15]. In this technique, for a certain period of time the EH section stores energy and then in the next time slot they send the modulated data.

Constraints on the energy source means that efforts need to be made in order to realize more efficient communication architectures. Typical narrow-band systems employ base-band modulation schemes that improves spectral efficiency, but consequently results in a modulated signal that changes both in amplitude an phase. Keeping the needed signal integrity often demands good linearity from the power amplifier that drives the antenna, at the cost of power efficiency. Furthermore, to minimize the antenna size, up-conversion demands mixers and frequency synthesizers, which amounts in power and complexity. For self-sustainable reasons, the development of short-range technologies, such as Bluetooth, ushered a new era in implementation of WSNs and wireless personal area networks (WPAN) [16]. Bluetooth-based WSNs can provide a reliable data network infrastructure, but the architecture still relies on up and down frequency conversions, which take a toll on power and complexity. Although the impressive ≈ 3 mW that is already achievable during communication [17] still makes this solution difficult to apply in battery-less systems based on energy harvesters. In fact, designing energy harvesting circuits with good efficiencies is a challenge [10], and further taking into consideration that the transducer

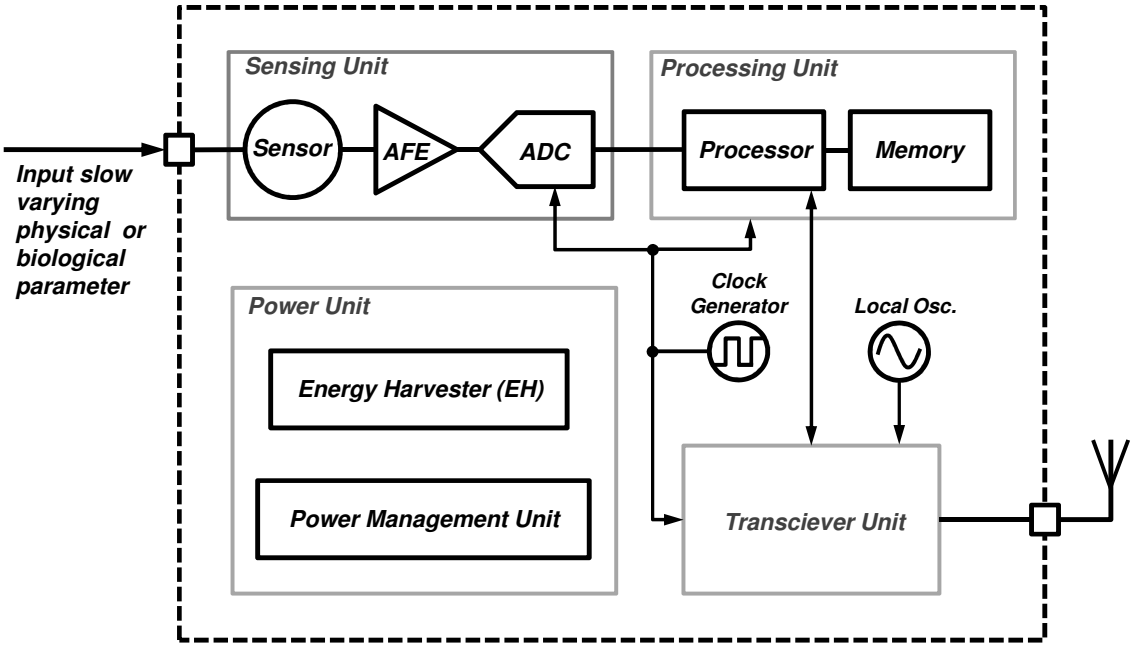


Figure 1.1: Typical architecture of a sensor node [8].

itself has its own efficiency, the size of the system can become considerably large in order to get enough power [9]. Another possible alternative for communication is the ultra wide-band (UWB) [18]. There are two types of UWB communication schemes in the range of 3.1 GHz to 10.6 GHz, as defined by FCC (discussed further in the next section), the multi-band UWB (MB-UWB) and impulse radio-UWB (IR-UWB). In the MB-UWB the spectrum is split into 14 narrow sub-bands, distributed through five channels (all with three bands each, except the last that has two). It implements a multi-band (MB) orthogonal frequency-division multiplexing (OFDM) scheme, where data is divided among the different carrier bands that are transmitted simultaneously. Each sub-band occupies a bandwidth of roughly 528 MHz [19]. Although, the MB-OFDM enjoys high data rate and can be easily adopted to worldwide standards, it uses complex modulator/demodulator in its architecture that requires some processing power that should be implemented in both transmitter (SN) and receiver [16]. Alternatively, the full bandwidth can be utilized with IR-UWB technique, which is based on a low-duty cycle communication. It will be suitable mainly for short range applications due to inherent limitations on its transmit power. Nevertheless, IR-UWB can be implemented without the need of frequency translation, thus avoiding mixers, and the receiver can be greatly simplified by a non-coherent receiver, based on energy detectors, and thus, can be a good alternative for short range WSNs.

Oscillators are also known as power hungry blocks and there is a lot of effort on de-

signing power efficient ones. For example, Bluetooth works at 2.4 GHz and it requires an oscillator with that frequency. Such an oscillator might be a reasonable source of power dissipation. This problem is even worse in MB-OFDM techniques for UWB, because very high frequency oscillators from 3 432 MHz to 10 296 MHz are needed. Some solutions take advantage of the very RF wave used in RFEH units to generate and synthesize a clock signal, by utilizing an analog frequency divider circuit, known as harmonic injection locked divider (HILD). Some other work have used very low-power ring oscillator circuits as the clock generators [21], [22]. However, typically a delay/phase locked loop is introduced to implement a reliable clock [20], [11]. Besides the attempt for relaxing the need for clock generators, others have focused on eliminating the local oscillator and mixers, as in IR-UWB systems referred above and discussed in more detail further ahead. Another one is backscattering technique wherein instead of generating a carrier signal, the SN uses the received RF signal and reflects it by changing the impedance of the antenna. This technique can remarkably reduce the circuit complexity of sensor nodes, decrease the power consumption, and the implementation cost [13], [23]. However, the bit rate is small.

1.2.2 Impulse Radio Ultra-Wide Band

In 2002, the UWB frequency range was release in USA. It was defined by the federal communications commission (FCC) as any wireless transmission scheme that occupies, at least, a fractional bandwidth of 20%, i.e, $(BW/f_C) \geq 20\%$, where f_C is the carrier frequency, or more than 500 MHz of absolute bandwidth [18]. FCC has also defined the UWB radio transmissions from 3.1 GHz to 10.6 GHz as an unlicensed frequency range. But, FCC strongly limits the effective isotropic radiated power (EIRP) to -41.3 dBm/MHz in order to avoid interference with already existent narrowband communication systems [16], [19], [18]. As well stated in [1], this power level is basically the same as that allowed for the noise emissions of an electronic device, so, UWB effectively uses the "noise floor" for communication. As can be seen in Fig. 1.2, the FCC radiation mask coincide for both indoor and outdoor communication contexts, in the frequency range of 3.1 GHz to 10.6 GHz. While for the 1.61 GHz to 3.1 GHz range, and beyond 10.6 GHz, a stronger restriction is imposed on outdoor radiation, limiting it to a 10 dB lower power when compared to the indoor mask [19].

As mentioned above, a UWB signal occupies an extremely wide bandwidth where the RF signal energy can be spread over gigahertz of spectrum. Ideally speaking, if the whole 7.5 GHz band is utilized, the maximum EIRP transmitted through the channel is approximately 0.56 mW, which is quite less than the 500 mW allowed for a 2G cellphone

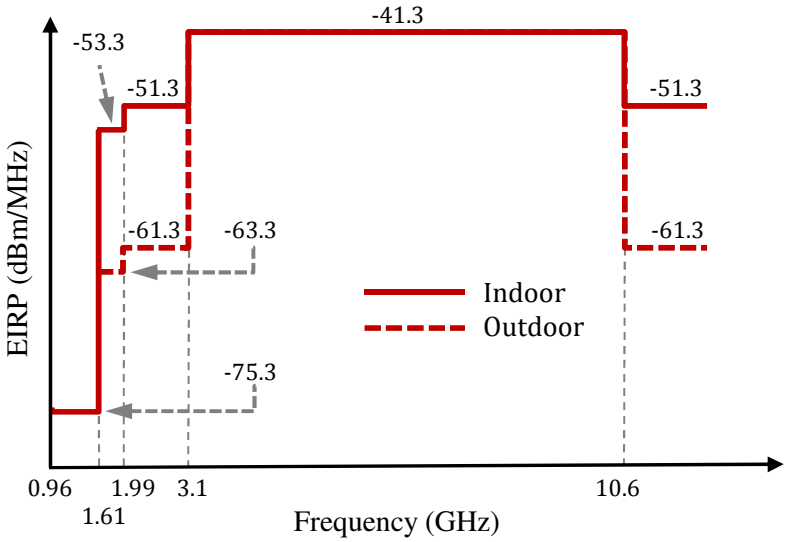


Figure 1.2: UWB spectral mask and FCC part 15 limits [16].

[16], [24]. One should be aware that no unique global spectrum mask rule exists; different countries such as: Australia, Canada, Japan, Korea and Singapore, have their own rules on UWB spectral range [19], and while in Europe and Asia the regulations tend to be more strict, in US and Canada they tend to be more relaxed [1].

All in all, although the new generation of Bluetooth low energy (BLE) overcomes many of the above-mentioned problems, UWB transfers information at higher data-rate while dissipating less power; it also enjoys less complexity in circuit design [16], [25], [26]. Very low energy consumptions of 890 fJ/bit to 250 pJ/bit using UWB were recently reported [1], [27], [28], [29], [30], [31] and evaluated to be constant for a data-rate of 1 Mbps to 10 Gbps [25] when energy detection receivers are considered. These are very attractive features when energy is the biggest constraint in the particular application of a WSN. Moreover, because a very short time windowing is used at the receiver, multi-path and narrow-band interferences in UWB is much more tolerable than other standards such as 802.11b (Wi-Fi) [32].

In a IR-UWB system, there is no restriction on the shape of the signal in the time domain. But in order to occupy the full extent of the UWB spectrum, IR-UWB utilizes short duration pulses with fast rise and fall times. These pulses can directly feed the antennas. There are several possible modulations in UWB systems, depending not only on the application but also on design specifications and constraints, operation range, transmission and reception power consumption, quality-of-service, regularity, hardware complexity, data rate, and capacity [19], [20]. Well-known modulation techniques in IR-UWB are binary phase shift keying (BPSK), pulse amplitude modulation (PAM), on-off-keying (OOK), and pulse position modulation (PPM). The most popular one is the BPSK that

defines zeros and ones by out-of-phase impulses. Although, because of its better bit error rate (BER) and smooth power spectrum, accurate synchronization and channel estimation is required for better pulse detection. Compared with BPSK, the OOK and PPM are just based on the presence or absence of a signal, which relaxes the need for accurate channel modeling, resulting in less complexity, less power dissipation by UWB pulse generator, and higher reliability [13], [20].

1.2.3 IR-UWB pulse generator

As stated, IR-UWB transceiver technology is very promising for short range WSN and RFID technology. Because there is no up- and down-conversion, IR-UWB transceivers are known as a carrier-less communication, resulting in an architecture of low complexity, which leads to less power consumption, less die area and lower production cost. In IR-UWB transmitter, the signal can be formed such that its energy concentrates over the range of UWB frequencies (3.1 GHz-10.6 GHz). In other words, their energy spread over a wide bandwidth in the frequency domain while they have a very short duration in time domain. Also, a band pass filter (BPF) with a 7.5 GHz bandwidth can be used before the antenna to constrain the emissions within the desired frequency band [16], [19], [20].

As a thought experiment, Fig. 1.3-a and -b show the quality that a sine wave in the time domain may have rectangular- or Gaussian-shape envelopes to form the shape of the UWB impulse. The spectrum of the rectangular pulse is a Sinc function and has side lobes that cannot be disregarded and could be considered as leakage of energy [16], [33]. However, a Gaussian pulse in time domain is Gaussian in the frequency domain as well, and its energy is confined into a narrower band and can better fit the FCC mask limitations [1], [19]. The obtained signal can be represented by the following formula [34],

$$S_{TX}(t) = Ae^{-\pi(t/\tau)^2} cos(2\pi f_c t), \tag{1.1}$$

where A is the amplitude of pulse, τ represents the time duration of the pulse and f_c defines the center frequency of the spectrum frequency. In this case, using a raised-cosine [35], triangular [36] and trapezoidal envelope have been also used [37].

Another way of gaining a Gaussian-shape frequency response is to use a Gaussian pulse per se. A study shows that the 5^{th} derivative of a Gaussian pulse is the best order that can fit the FCC mask requirement [38], and could be determined recursively from equation 1.2, where superscript (n) denotes the n-th derivative and σ is the variance of the

Gaussian pulse.

$$S_{TX}(t) = x^{(n)}(t) = -\frac{n-1}{\sigma^2}.x^{(n-2)}(t) - \frac{t}{\sigma^2}x^{(n-1)}(t). \tag{1.2}$$

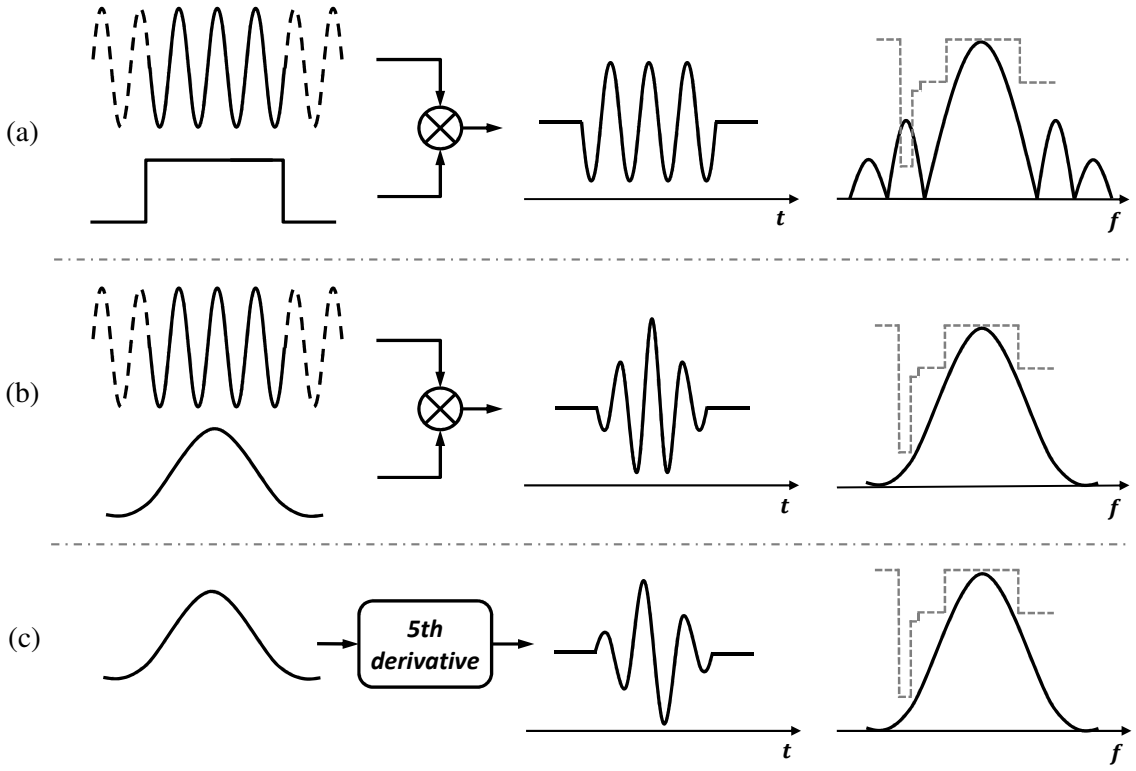


Figure 1.3: (a) Rectangular-shape envelope and its side lobes in frequency domain, (b) Gaussian-shape envelope and its Gaussian response in frequency domain, (c) 5th derivative of a Gaussian pulse and its Gaussian response in frequency domain. (Inspired from [1])

Typically, in the IR-UWB transmitters, most of the power is consumed in the pulse generator blocks. Thus, this block circuit should necessarily consume as less power as possible. In general, implementations of pulse generators can be categorized as:

- analogue or digital,
- mono-cycle or multi-cycle,
- single-band or multi-band, and/or multi-channel.

While a vast majority of pulse generators are analogue, digitally implemented ones are also available. They have relied on multiphase ring oscillators and/or a combination of different path delays [39], [40], [41], [42], [43], [44] (a.k.a. distributed waveform generators (DWG)) or time-interleaved architectures [45]. All-digital transceivers can take

the maximum advantage of CMOS technology scaling and be more easily programmable than their analog counterparts [46], [47].

Additionally, in terms of pulse shape, they can be mono-cycle or multi-cycle. Usually, the latter is preferable due to better spectral adjustment and work based on three different methods such as (1) time-interleaved architectures that generate positive and negative cycles with different amplitude and delays and ultimately add them up [48], [49], [50], [51]; (2) another method is to up-convert baseband pulses into a center frequency using mixers or oscillators [36], [52], [53], [54]; (3) filtered response of a very short input impulse [55], [56]. Besides, although most of the related work has focused on multi-cycle impulses, mono-cycle pulses can be too short so that they have wider spectrum but normally they need extra filtering [57]. Recently, on-chip self-calibration designs has been also presented [58].

Furthermore, UWB transmitters could be single-band for OOK, PAM, PPM and BPSK modulation [36], [40] or multi-band for FSK modulation [59] and multi-channel for serving multiple inputs [36], [60].

1.2.4 Signal coding schemes

The efforts to decrease the power consumption of sensor nodes do not exclude signal coding and analog-to-digital converter (ADC). To be real time, a typical digital SN needs to have an ADC with high enough sampling rate; while ADCs in turn are complex circuits, they can be considered as a critical building block in terms of power. Thus, a common inefficiency problem in novel Bluetooth and UWB systems is using ADC blocks inside a sensor node [61], [62], [63]. Performing part of the signal processing in the analog-domain provides more power efficiency [16] and has led to solutions that avoid ADCs at the sensor node [64], [65], [66]. Furthermore, another reason for avoiding ADC is a technological limitation. As the technology nodes shrink the voltage supply decreases and high precision quantizers are more and more difficult to implement making time encoding a new viable alternative to standard sampling techniques [61], [62], [67]. Therefore, a few teams has encoded data into time domain in transmitter while they have done the time to digital conversion (TDC) at the receiver. In other words, sending most of the circuit complexity of a WSN to the receiver has been of their interest, so that the sensor nodes, which are supposed to be produced in larger quantities, would enjoy the least complexity and power dissipation.

In this line of thought, a clockless pulse width modulation (PWM) technique has been proposed to modulate the input signal [65], which is then transmitted using FSK modulation. Yet, the transmitter uses complex and power hungry narrow-band methodologies.

Also in [66], a PWM technique is used to create impulses. It operates based on PPM communication technique, but here an IR-UWB transmitter is utilized for data transmission, which improves efficiency. Another option involves a time encoding method derived from an RC-based sensing interface [68]. It converts analog information to time intervals determined by the discharge time of an RC circuit, under the scheme of PPM technique, and again it uses UWB for transmission. Both last two solutions are power efficient, but, as presented, it does not allow for multiple-access sensor networks. In an effort to decrease the amount of data to be transmitted, which also favors efficiency, some authors have also proposed other alternative conversion mechanisms, such as the level-crossing ADCs which are claimed to be able to reduce significantly the data-rate when the signal is sparse [62], [69].

1.3 Proposed Idea

Processing information in the time domain, independent of signal magnitude, is a route that avoids the above-mentioned limitation. This dissertation changes the normal view of digital communication by encoding the amplitude information, of an arbitrary stimulus, to a series of time-encoded spikes. This technique is inspired by neuron operation, which are diverse in terms of functionality and behavior, and among different possible representations, the so called integrate-and-fire neuron (IFN) model is often used. It models the neuron to a first order fire-and-reset system [70]. In this model, the aggregated charge from external excitation raises the cell-membrane potential until it reaches a threshold. Then, the neuron generates a spike and the membrane potential resets to a reference value and again starts accepting inputs from neighbouring neurons. Basically, the membrane can be thought as a capacitor that relates the membrane potential (action potential) with the excitation current [70]. The resulting output pulse-density (firing rate) is related to the net input excitation. Particularly, this modulation technique is very convenient for IR-UWB communication, which naturally can radiate the action potentials generated by the IFN modulator. In fact, it modulates the analog input signal into distances (δ) between fixed- and short-duration spikes [71], as represented in Fig. 1.4. This technique, also known as pulse density modulation (PDM), not only shows potential to reduce the total power consumption in IR-UWB transceivers, almost more than ten times, but also benefits from a dynamic sample generating rate [70], [72] and relaxes the need for A/D converter at the sensor node, which normally is disregarded as a power-hungry component. Let us call such a system an impulse-radio integrate-and-fire (IRIF) transceiver. Comparing to the ordinary ADCs, integration-and-fire modulator (IFM) produces less amount of data

during conversion process while the input signal is still recoverable at the receiver with relatively high effective number of bits (ENOB), if a proper time resolution is defined. Overall, the contribution of the thesis has been summarized as follows:

- The main contribution of the thesis is to replace conventional A/D Converter by integrate-and-fire modulation and using it in UWB wireless communication. The proposed system is called IRIF transceiver.
- In a system-level study, the power efficiency of the IRIF transceiver is attested for a random Gaussian signal, and compared with the conventional A/D based systems. The results show 12 and 6 times less power consumption in comparison with BPSK and OOK modulations, respectively.
- A very low power LC-tank based pulse generator with 8.16 pJ/pulse power consumption is designed. It covers -10dB bandwidth of 4.8 GHz, and peak power of -42.8 dBm/MHz.
- The system is silicon proved and fully implemented on a single CMOS chip.

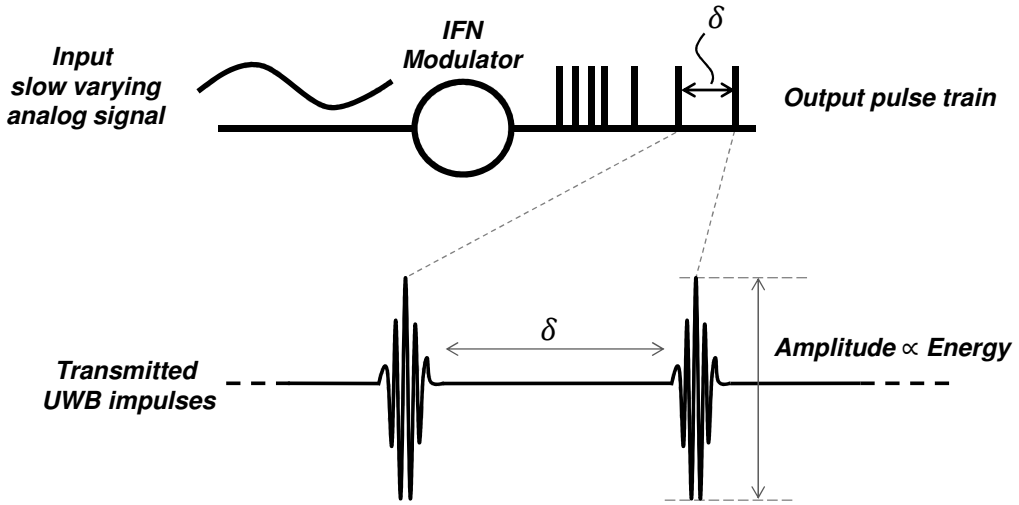


Figure 1.4: Function of integration-and-fire neuron as a modulator and representation of the transmission technique by radio impulses

1.4 Outline of the dissertation

The thesis is organized as follows: Chapter 2 discusses the integrate-and-fire modulation including its theory and reconstruction methods. It will end up with some more qualitative study, a performance estimation and a conclusion. Chapter 3 presents a system-level

analysis of the IRIF transceiver that takes into account channel model, link budget and quality of reception. CMOS implementation of the transmitter is discussed in chapter 4. Measurement results are all reflected in chapter 5. Finally, the thesis will be summarized and concluded in chapter 6.

Chapter 2

Integrate-and-Fire Modulation

Due to the ever decreasing of supply voltage in integrated circuits, high precision quantizers are more and more difficult to implement, which makes time encoding a viable alternative to classical sampling techniques. In general, there exists three types of time encoding machines (TEM), that can replace analog-to-digital converters in communication systems. These three techniques are pulse width modulation (PWM) [64], [66], pulse code modulation (PCM) that delta modulation is an example of it, and pulse density modulation (PDM) [70], [72]. They all represent analogue information as a sequence of time-encoded bit stream and/or spikes, either in a pulse shape (e.g. the output of a delta modulator) or in the form of spikes (e.g. the output of a PDM modulator). Integrate-and-fire modulation can be categorized as a PDM technique that converts amplitude information of an analog signal to a series of time-encoded spikes. Notably, it uses a dynamic/nonuniform sample rate. In this chapter the theory behind this type of modulation, along with its drawbacks and advantages will be discussed.

2.1 Sampling

So many signals around Plenty points to be found
Fortunate those who decode Where does the secret abode? [1]

Sampling is a fundamental operation in every signal analysis because a signal $x(t)$ cannot be recorded in its entirety. Thus, the the signal must be sampled at a sequence $\{t_n, n \in \mathbb{Z}\}$. Then, a critical question is how many samples must be stored so that the signal $x(t)$ can be reconstructed or at least well approximated. In practice, usually it

[1] Inspired by Hafez (one of the greatest Persian poets of 14th century), Goethe, the German poet wrote West-Eastern Divan (1814-1820)

is reasonable to assume that the signal is band-limited (i.e., $x(t) \in [-\Omega_N, \Omega_N]$) and the number of recorded samples are related to this bandwidth.

On one hand, if the samples are equally spaced by at least sampling time $T_s = \pi/\Omega_N$, then the famous sampling theorem enunciated by Nyquist and Shannon, at the beginning of the 20th century, tells us that the continuous-time function can be obtained from the samples using the equation 2.1, a minimum sampling rate is respected.

$$x(t) = \sum_{n=-\infty}^{\infty} x(nT_s) \frac{sin(\pi(t - nT_s)/T_s)}{\pi(t - nT_s)/T_s} \tag{2.1}$$

On the other hand, in case of irregular samples, where they are not equally spaced, reconstruction is more difficult and methods used in frame theory [73] and irregular sampling are necessary [72], [74]. From an engineering point of view, the modern theory of nonuniform (or irregular) sampling is originated from the work of Yen in 1956 [75]. Nonuniform sampling can be considered as the generalization of its uniform counterpart. Since any band-limited function is completely determined by its local averages, it can be reconstructed using them [72], [76].

2.1.1 Integrate-and-Fire Modulator (IFM)

Integrate-and-fire modulator (IFM) has been inspired from the behavior of biological neurons. Although, they are diverse in terms of functionality, among different possible representations, the so called integrate-and-fire neuron (IFN) model is often used. It models the neuron to a first order fire-and-reset system [70]. In this model, the aggregated charge from external excitation raises the cell-membrane potential until it reaches a threshold. Then, the neuron generates a spike and the membrane potential resets to a reference value and again starts accepting inputs from neighboring neurons. Basically, the membrane can be thought as a capacitor that relates the membrane potential (action potential) with the excitation current [70]. The resulting output pulse-density (firing rate) is related to the net input excitation. Mimicking this operation, the realization of an Integrate-and-fire modulator (IFM, a.k.a. IFN modulator), comprises an integrator and a comparator, as illustrated in Fig. 2.1. First, the input signal, $x(t)$, which might be superimposed by a DC value called b, is integrated in time and then compared with a reference value. As soon as the integration reaches the threshold (θ), the comparator activates the switch to reset the integrator. However, this happens after a certain amount of time τ_r, called refractory period needed to re-initiate the process, and thus, it inflicts some quantization on the signal conversion.

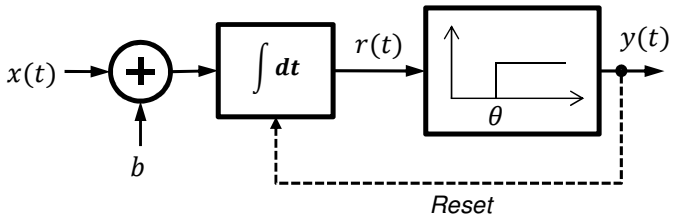


Figure 2.1: Modular view of an integrate-and-fire modulator

The basis of the amplitude/time to time encoding process is the above-mentioned PDM technique that converts the analog input signal to a series of time-encoded spikes. An IFN spike is then generated from equal time-integration areas of the input signal, resulting in a dynamic firing rate, which depends on the shape of the signal, and the resulting spike time-intervals may be either above or at Nyquist rate, while in conventional ADCs, the sampling rate is constant. This dynamic sample spike rate is inherently non-uniform leading to less produced data and lower power consumption [70], [72].

A non-uniformly sampled signal $x(t)$, includes sampling time set of $\{t_k, k \in \mathbb{Z}\}$ and can be represented by

$$x(t) = h^T c = \sum_{k=-\infty}^{\infty} c_k h(t - t_k), \tag{2.2}$$

where c_k represents the elements of vector c which corresponds to a set of weights and is multiplied by h^T, which is the transpose of a t_k-shifted impulse response of an ideal low-pass filter with bandwidth Ω_N shown in equation 2.3 [77].

$$h(t) = \frac{sin\Omega_N t}{\pi t} \tag{2.3}$$

Let us assume that $x(t)$ is a function band-limited in $[-\Omega_N, \Omega_N]$, and $s_k = (t_{k+1} + t_k)/2$ are the midpoints of each two consecutive samples, and $\delta = sup_{k\in\mathbb{Z}}(t_k - t_{k-1})$, $\omega_k = s_k - s_{k-1}$. A local average φ_k can be defined as $\varphi_k = \frac{1}{\omega_k}\int_{s_{k-1}}^{s_k} x(t)dx$, then x can be recovered by the following iteration algorithm, where n is the number of iterations [76].

$$x_0 = \sum_{k=-\infty}^{\infty} \varphi_k \omega_k \cdot h(t - s_k) \tag{2.4}$$

$$x_{n+1} = x_n + x_0 - \sum_{k=-\infty}^{\infty} \left(\int_{s_{k-1}}^{s_k} x(t)dx \right) \cdot h(t - s_k) \tag{2.5}$$

Then

$$x(t) = \lim_{n\to\infty} x_n \tag{2.6}$$

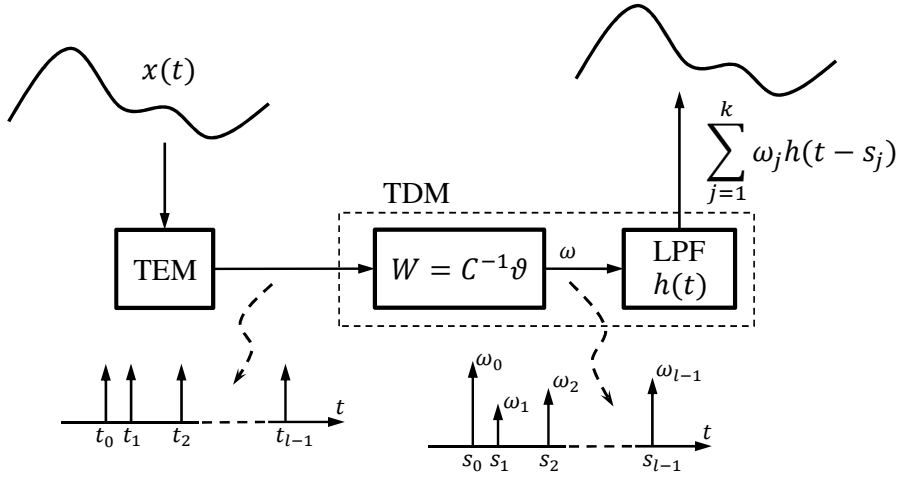


Figure 2.2: Modular view of an integrate-and-fire modulator and reconstruction method when it is seen as a time encoding machine (TEM) and time decoding machine (TDM)

and the error will be given by

$$||x - x_n|| \leq \left(\frac{\delta\Omega_N}{\pi}\right)^{k+1} ||x||. \tag{2.7}$$

2.1.2 Reconstruction

As stated above, an IFN spike is generated from equal time-integration areas of the input signal. Thus, the response for the IFN integrator can be represented as [71]:

$$\int_{t_i+\tau_r}^{t_i+1} x(t)\,dx = \theta, \quad \forall i \in \mathbb{Z} \tag{2.8}$$

where x(t) is the input signal band-limited to $[-\Omega_N, \Omega_N]$, t_i is a timing sequence and (τ_r) is called refractory time and represents the amount of time that the integrator needs to be reset. This formula can be seen as a TEM, converting an arbitrary input signal into a series of spikes, shown in Fig 2.2. The minimum sample rate in an IFN modulator is related to maximum adjacent interval $(\delta_{max} = sup(t_{i+1} - t_i))$. Obviously, the input signal can be recovered provided that the minimum sample rate is above Nyquist rate, or that is to say $\delta_{max} < 1/f_{Nyquist}$ [71], [78].

There are several approaches to reconstruct the original signal based on the received spikes, either in time-domain [71], [78], [79] or frequency-domain [80]. However, literature shows that frequency based methods have less ENOB compared to their time based counterparts. Here, the procedure represented in [78] is followed. It is known that any band-limited signal can be expressed as a low-pass filtered version of sum of delayed impulse functions which are appropriately weighted [72], [79]. Thus, for an Ω_N-bandlimited

signal x(t), which has k ($k \in \mathbb{Z}$) IFN spikes within length of l ($l \in \mathbb{Z}$), equation (2.9) can be used to decompose the signal into spike trains, basically following the procedure defined in last section for non-uniform sampling representation.

$$x(nT) = h(nT) * \sum_{j=1}^{k} \omega_j \delta(nT - s_j) = \sum_{j=1}^{k} \omega_j h(nT - s_j), \tag{2.9}$$

where T is the sampling time needed for digital computation and $n \in \mathbb{Z}$; $x(nT)$ is a vector with the length of l ($l \in \mathbb{Z}$), wherein k ($k \in \mathbb{Z}$) IFN spikes exist within this length, $s_j = (t_{j+1} + t_j)/2$, $\omega_j = x(s_j)$, '*' is the convolution operator, and $h(nT)$ is the impulse response of the ideal low-pass filter expressed as:

$$h(nT) = \frac{\sin(2\pi f_s nT)}{\pi nT}. \tag{2.10}$$

Let us denote the reconstructed signal, and the vector of weights, by q (having length of l) and W (with a length of k), respectively. W contains the ω_j values illustrated in Fig. 2.2. Then, equation (2.9) can be rewritten in a matrix form as follows,

$$q = H^T W, \tag{2.11}$$

where H^T is a transposed matrix, and each of its rows gives the vector of a s_j-shifted impulse response of the ideal low-pass filter $\big([\boldsymbol{H}]_{k,l} = [h(nT - s_j)]\big)$. The bandwidth of the filter is set slightly larger than $f_s/2$ for better reconstruction. Clearly, the signal can be reconstructed as long as the weights are given. Substituting (2.9) into (**??**) results in,

$$\theta_i = \sum_{j} \sum_{n=i}^{i+1} \omega_j h(nT - s_j) = \sum_{j} \omega_j C_{i,j} \quad , \tag{2.12}$$

where $C_{i,j}$ gives the values of integrals over (t_i, t_{i+1}) for each s_j-shifted $\mathrm{sinc}(\cdot)$ function; it can be calculated by the equation below,

$$C_{i,j} = \sum_{n=i}^{i+1} h(nT - s_j). \tag{2.13}$$

Therefore, the weight values are given by $\boldsymbol{W} = \boldsymbol{C}^{-1}\theta$. After all, substituting $\boldsymbol{W}$ into (2.11), the original signal will be recovered by the equation below:

$$q = H^T \boldsymbol{C}^{-1} \theta \tag{2.14}$$

This algorithm can be recognized as a time decoding machine (TDM), as illustrated in

Fig. 2.2. The practical solution, however, is challenging because $h(nT)$ needs to contain a finite number of samples, which causes boundary errors. In fact, only finite sets of the form $\{t_0, t_1,..., t_{l-1}\}$ and $\{\omega_0, \omega_1, ... , \omega_{k-1}\}$ are available for recovery. Thus, q and $\boldsymbol{W}$ have l and k elements, receptively; and H is a k-by-l matrix. Yet, for reasonably large l, and avoiding the boundary samples (at the beginning and end of the signal), a very good approximation can be achieved.

2.2 ENOB Calculation

Effective number of bits (ENOB) are normally defined as $ENOB = (SNR - 1.76)/6.02$ where SNR is the signal-to-noise ratio and may be replaced by SINAD (signal-to-noise and distortion ratio). However, in the IFN-related literature, the ENOB and SNR have been used in three different ways. Among these methods, only the third one is compatible with unanimous understanding from ENOB. Yet, the other two, cannot be ignored because they provide a way of comparison for non-sinusoidal signals. These methods are better described below.

Method I The first one is the signal-to-error power ratio, known as SER criterion [79]. It is presented in equation 2.15 where $P\{\cdot\}$ is the power operator, and $x(t)$ and $e(t)$ are the original and error signals, respectively. The error signal is defined as $e(t_k) = x(t_k) - \hat{x}(t_k)$ and $\hat{x}(t_k)$ is the reconstructed signal. This method is relatively conservative and care needs to be taken when measuring it. Specially phases between original and reconstructed signals should be aligned otherwise the ENOB will be affected. However, for non-sinusoidal input functions this method will be used.

$$SER = 10 \cdot log\left(\frac{P\{x(t)\}}{P\{e(t)\}}\right) \tag{2.15}$$

Method II The second method has been presented in [61] and still uses the same concept as in SER. Since, in the IFN modulator there is no access to the error at each sample, it expresses the error due to time quantizer as the difference in the estimating θ_i in the reconstruction formula, assuming that timing error is uniformly distributed in the interval of $[-T_{clk}/2, T_{clk}/2]$, where T_{clk} is the sampling period. This error is shown in 2.16.

$$e(t_k) = x(t_k) - \hat{x}(t_k) = \sum_i h_i(t_k)(\theta_i - \hat{\theta}_i) \tag{2.16}$$

Then, for the signal $x(t)$ with power of P_s it formulated the quantization signal-to-error ratio (SNR_{quant}) as equation 2.17. Besides, it assumed $|\theta_i| = \theta$, $\forall i$.

$$SNR_{quant} = 10 \cdot log\left(\frac{6\theta^2}{{T_{clk}}^2 P_s}\right) \tag{2.17}$$

Method III The third method, is the well-known SINAD calculation technique using power spectral density (PSD). It can be obtained by means of the equation 2.18, where P_s is the signal power, P_n is the noise power and P_d is the power of distortion in the signal.

$$SINAD = 10 \cdot log\left(\frac{P_s}{P_n + P_d}\right) \tag{2.18}$$

2.3 Modeling of the IFN Modulator in MATLAB

Here, the effect of sampling frequency and different types of noise are studied. Figure 2.3 shows the model of the IFN modulator implemented in MATLAB. The OTA converts the input signal to a current and charges C_{mem}, where the OTA transconductance is $G_m =$ 160 nS and C_{mem} is assumed to be 100 pF. The model also assumes an input referred noise $\eta_g(t)$. The comparator uses the clock of $\phi(2\pi f_s t + \eta_\phi(t))$ with sampling frequency of f_s including jitter, $\eta_\phi(t)$, with respect to T_{clk}. The reference voltage, $\theta(t)$, is set to the value of $\hat{\theta}$ with some amount of added noise, $\eta_\theta(t)$.

In practical applications the spike train will be synchronized to a sufficiently fast clock signal. It provides the system with time-compression capability and better spike detection at the receiver. However, this synchronization introduces time jitter to the arrival time of each spike and impairs the reconstruction quality and ENOB. Therefore, the clock speed can improve the performance. This issue has been studied for two different cases of input

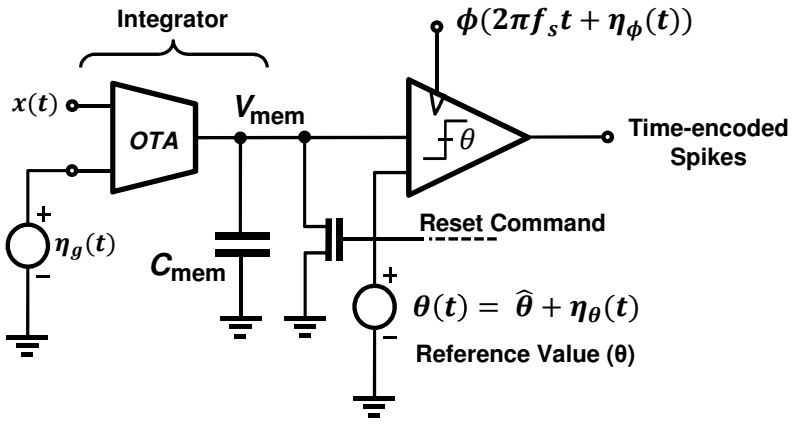


Figure 2.3: Integrate-and-fire neuron circuitry including noise and jitter

Table 2.1: SNR comparison between three methods of calculation. All values are in dB.

		SNR for each reconstruction method		
f_{clk}	SNR of input	I	II	III
1 MHz	83.63	53.9	120.47	38.66
10 MHz	104	67.98	140	62
100 MHz	122	78.93	160.5	80
1 000 MHz	143.8	97.84	179.9	89

signals. The first case is for a random Gaussian signal band-limited to 1 kHz, with SER criterion (Method I). The second case is for a sinusoidal input function with frequency of 1 kHz, and here the PSD criterion (Method III) is used. For both cases, the maximum amplitude of the signals are 100 mV, the signal is superimposed with a 0.6 V and the reference value, $\hat{\theta}$, is set to 100 mV. At this stage no kind of noise has been added.

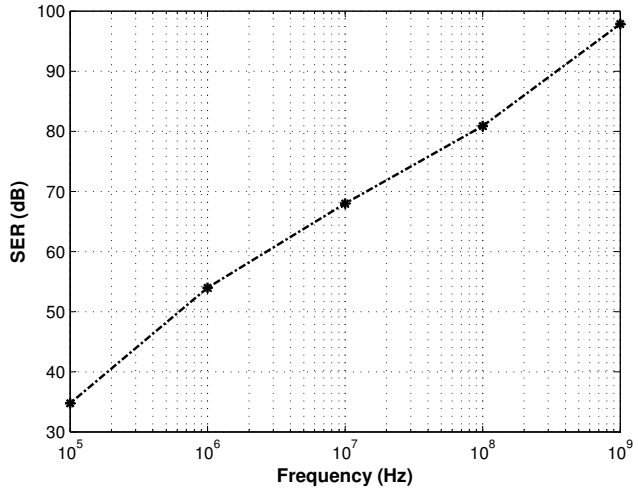


Figure 2.4: ENOB vs. sampling frequency for the case of random Gaussian signal while method I (SER) is used for ENOB calculation. For non-sinusoidal inputs this method should be used.

For the case of random Gaussian signal, the SER method is used to find the ENOB for different clock frequencies. Figure 2.4 shows that the SER characteristic will improve if the sampling rate increases. Similar conclusions have been reached in [78] and [79]. On the other hand, for the case of sinusoidal function, the PSD is calculated for different clock frequencies. The SNR results are summarized in TABLE 2.1. It also compares them to the SNR of the input signal that has been used interchangeably with its SINAD, which helps to infer the quality of the signal. All of the ENOB calculation methods, discussed in 2.2, show that the ENOB value improves if the clock frequency increases. Figure 2.5 shows the PSD graphs, confirming that the higher clock frequency, the larger ENOB will be obtained. It can be seen that after reconstruction process some amount of low-frequency components are added to the signal, which is the main degrading factor of

the ENOB. Whereas higher frequency is suppressed due to the fact that IFN conversion does perform an integration of the input signal within its band. Yet, by increasing the sampling rate this impairment can be compensated to some extent.

Furthermore, the effect of noise on reference value, θ, has been studied when the sampling clock is 10 MHz. It is shown that small amount of noise on reference value causes noticeable degradation in ENOB. This effect is illustrated in Fig. 2.6 and by comparing to Fig. 2.5-b, it is inferred that even 5% noise is enough to decrease the SNR by roughly 20 dB.

The effect of input noise is also verified for the sampling clock of 10 MHz and illustrated in Fig. 2.7, where the subplots on the left are PSD plots of the input signal for different percentage of input noise and the subplots on right are PSDs of the corresponding reconstructed signals. The input signal is contaminated by a white noise. Figures 2.7-(a,b) are input and reconstructed signals when no noise is added. It can be seen that due to reconstruction process low-frequency noise degrades the ENOB from 17 bits to 10 bits. This low-frequency noise remains almost in the same power level for different input noise. Figures 2.7-c,d represent the case when 5% noise is added. It can be inferred that due to integration process the IFN modulator can efficiently suppress high frequency noise and improve the ENOB from 5.8 bits to 9.7 bits. Figures 2.7-(e,f) show the input and reconstructed signals when the input is contaminated by 50% noise. These results show that the IFN modulator has an excellent robustness against the input noise above the defined bandwidth of the input signal $[-\Omega_N, \Omega_N]$.

The effect of clock jitter has also been studied and illustrated in Fig. 2.8, where the subplots on the left are PSD plots of the input signal for different percentage of jitter noise and the subplots on right are PSDs of the corresponding reconstructed signals. The frequency of clock is 10 MHz, which is contaminated by different jitter noise. Figures 2.8-(a,b) present the input and reconstructed signals when no jitter is added. It can be seen that due to the reconstruction process, low-frequency noise degrades the ENOB from 17 bits to 10 bits. This low-frequency noise remains almost in the same power level for different jitter noise. Figures 2.8-(c,d) are for the case when the clock is impaired with 5% jitter. Figures 2.8-(e,f) present the input and reconstructed signals when the clock is contaminated by 50% jitter noise. These graphs show that although the input signal degrades in terms of ENOB, the reconstructed signal sustain an ENOB of 10 bits. It can be inferred that because the sampling clock rate is very large, the IFN modulator is immune to jitter noise to a very good extent.

Moreover, simulations show that the noise at the frequencies lower than the fundamental tone is the major degrading factor in terms of ENOB and performance; moreover, the noise on the reference voltage will dramatically decrease this figure of merit.

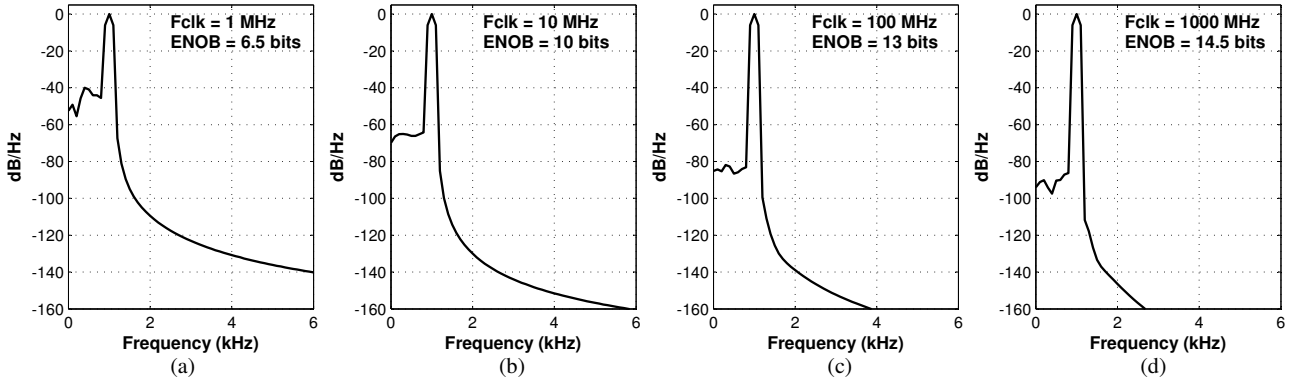


Figure 2.5: Effect of sampling rate on ENOB. The input sine wave has 1 kHz and the PSD method is used after removing the 0.6 V DC component. PSD is calculated using welch technique for 100 cycles of the signal. Hanning window is set and the window size is 10 periods of the signal. (a) Fclk = 1 MHz, ENOB = 6.5 bits, (b) Fclk = 10 MHz, ENOB = 10 bits, (c) Fclk = 100 MHz, ENOB = 13 bits, (d) Fclk = 1 000 MHz, ENOB = 14.5 bits.

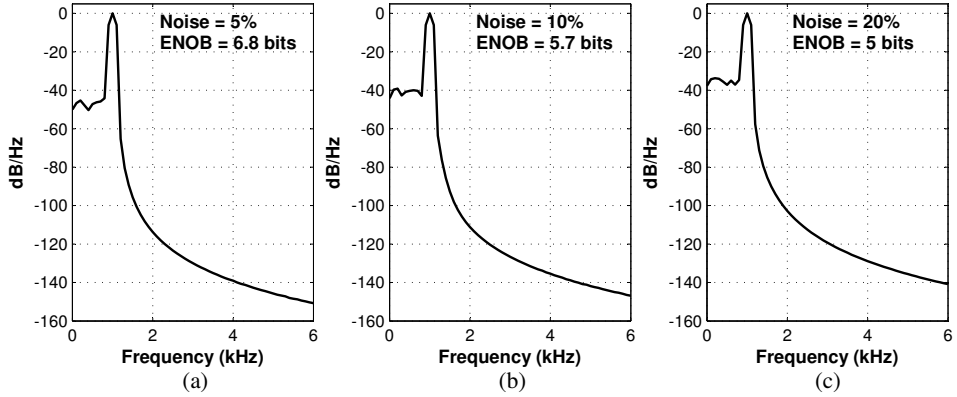


Figure 2.6: Effect of noise of the reference voltage on ENOB for the case of sinusoidal input function. The reference value is set to 100 mV. (a) Noise = 5 %, ENOB = 6.8 bits (b) Noise = 10 %, ENOB = 5.7 bits (b) Noise = 20 %, ENOB = 5 bits

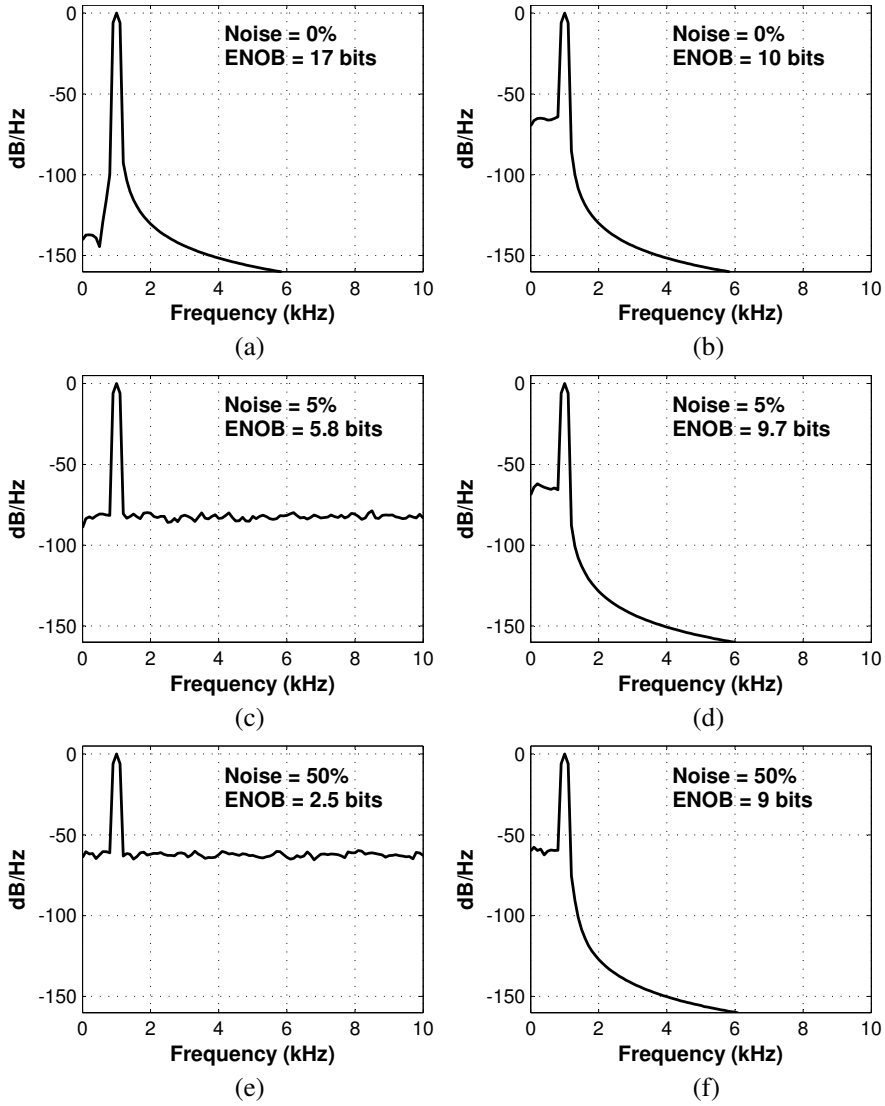


Figure 2.7: Effect of input noise on ENOB. The amplitude of the sinusoidal signal is 100 mV. (a) PSD of the input signal, Noise = 0%, ENOB = 17 bits; (b) PSD of Reconstructed signal when noise is 0%, ENOB = 10 bits; (c) PSD of the input signal, Noise = 5%, ENOB = 5.8 bits; (d) PSD of Reconstructed signal when noise is 5%, ENOB = 9.7 bits; (e) PSD of the input signal, Noise = 50%, ENOB = 2.5 bits; (f) PSD of Reconstructed signal when noise is 50%, ENOB = 9 bits.

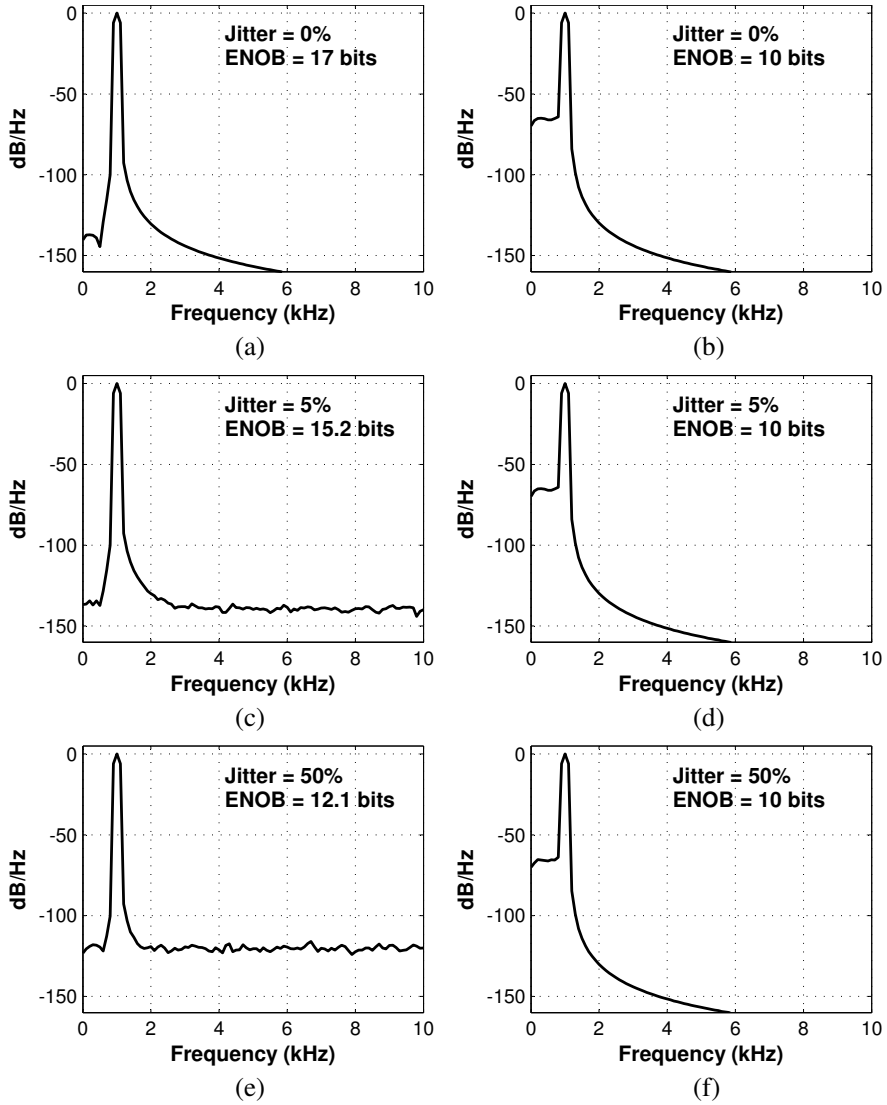


Figure 2.8: Effect of jitter noise on ENOB. The test has been done with clock frequency of 10 MHz for all cases. (a) PSD of the input signal, jitter = 0%, ENOB = 17 bits; (b) PSD of Reconstructed signal when jitter is 0%, ENOB = 10 bits; (c) PSD of the input signal, jitter = 5%, ENOB = 15.2 bits; (d) PSD of Reconstructed signal when jitter is 5%, ENOB = 10 bits; (e) PSD of the input signal, jitter = 50%, ENOB = 12.1 bits; (f) PSD of Reconstructed signal when jitter is 50%, ENOB = 10 bits.

2.4 How many spikes are required?

A critical question in IRIF transmitter is to find how much less data it generates comparing to typical digital transmission systems. To answer this question, it is required to find how many IFN pulses are needed to achieve a reasonable ENOB. In this section, two case studies will be done for input signals of a random Gaussian signal and a sinusoidal wave that can help to better understand the IFN modulator.

2.4.1 Input random Gaussian signal

Fig. 2.9-a shows a random Gaussian signal band-limited to $[-3000\pi, 3000\pi]$ used in the simulation experiment, and a clock samples the input by $f_s = 10\,\text{MHz}$. The integrate and fire/reset process is illustrated in Fig. 2.9-b when the threshold value is set to 100 mV. The IFN spike series are generated according to equation (2.8) and can be observed in Fig. 2.9-c. The reconstructed and error signals are shown in Fig. 2.9-d and -e, respectively. Figure 2.9 only shows one-third of a longer signal with time duration of 9 ms. In fact, due to limited length (non-ideality) of the sinc function, the reconstruction process is not perfect and boundary errors occur. This phenomenon is shown in Fig. 2.10 and can degrade the SER. Since, the input signal in this study is not a pure sinusoidal wave, the ordinary definitions of signal to quantization noise ratio and/or spurious free dynamic range is not applicable. Thus, the method I, namely SER, has been utilized for the performance measurement.

In Fig. 2.11, SERs are calculated for 3 ms duration of two reconstructed random Gaussian signals with input voltage amplitudes of 100 mV and 400 mV. The results are shown in terms of different reference voltages. The number next to each point indicates the number of required IFN spikes that results in the corresponding SER. As the reference value decreases, more number of spikes are generated and higher SERs are achievable. Also for both signals, successful reconstruction condition ($\delta_{max} < 1/f_{Nyquist}$) has been satisfied by roughly 15 or 16 IFN spikes in order for a reasonable SER to be obtained. Furthermore, with 18 spikes an SER = 62 dB is achieved for the input signal with amplitude of 100 mV and SER = 55 dB is obtained with 19 IFN action potentials for the case of the signal with 400 mV amplitude. This experiment also shows that, as the amplitude increases, the SER decreases. Definitely, the value of θ and the sampling rate needs to be adjusted according to the signal dynamics.

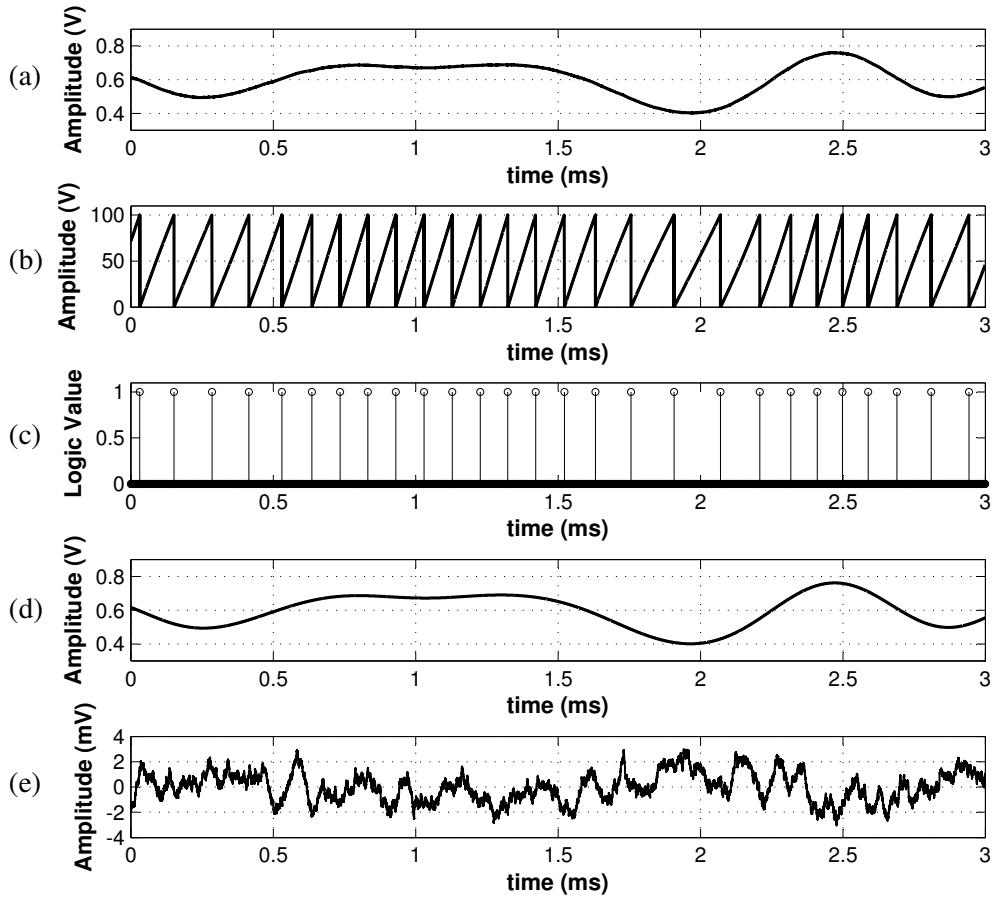


Figure 2.9: Modulation and reconstruction. (a) input signal, (b) integration signal, (c) the IFN pulse train for duration of 3 ms, (d) reconstructed signal, (e) the error between the input and reconstructed signals

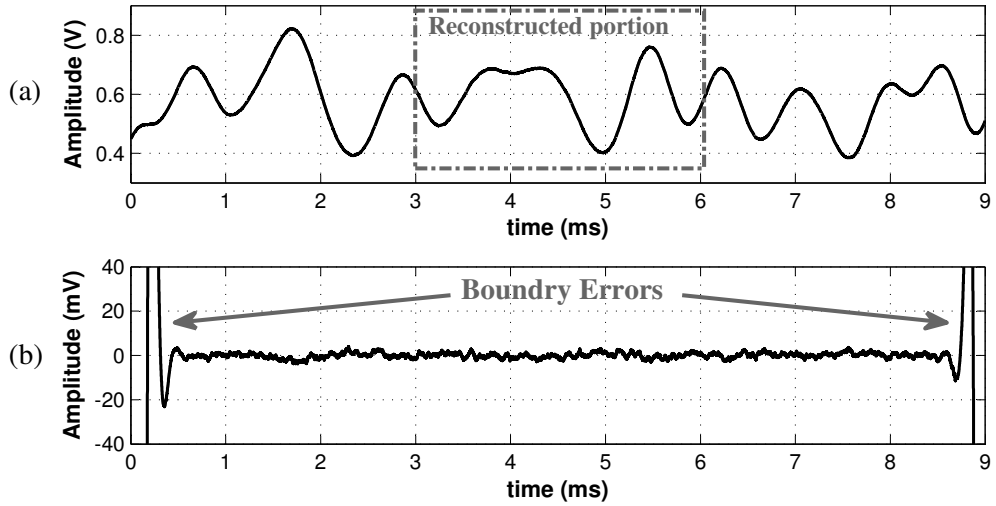


Figure 2.10: (a) Overall input signal, the red dashed rectangle is the section which was shown in Fig. 2.9-a (b) Error signal that shows large error value at the boundaries

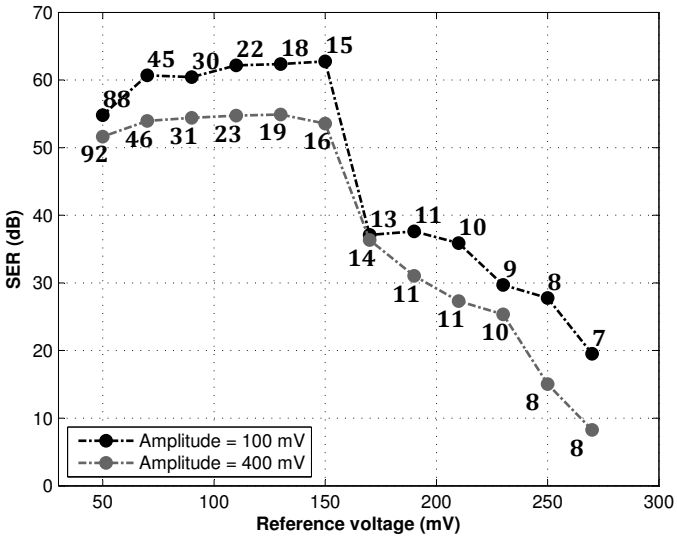


Figure 2.11: Reconstruction results: SER versus different reference voltages for two cases of different amplitudes of the random Gaussian noise. The number next to each point indicates the number of required IFN spikes that results in the corresponding SER value.

2.4.2 When the input is a sinusoidal function

Fig. 2.12-a shows the sinusoidal signal with frequency of 1 kHz and amplitude of 100 mV superimposed with a DC voltage of 0.6 V used in a simulation experiment, sampled with a clock of $f_s = 10$ MHz. The new integrate and fire/reset process is illustrated in Fig. 2.12-b when the threshold value is set to 100 mV. The IFN spike series are generated according to equation (2.8) and can be seen in Fig. 2.12-c. The reconstructed signal is shown in Fig. 2.12-d and clearly shows that the fidelity of this signal to the original one depends on the number of IFN spikes. In other words, enough IFN spikes are needed to get reasonable ENOB.

Using PSD method, ENOB calculation has been performed and the minimum required number of spikes are studied. In this experiment it is assumed that all blocks are ideal and no noise is injected. Figure 2.13 shows that even three IFN spikes are enough to reconstruct a sine wave with reasonable ENOB. For the clock frequency of 10 MHz, PSD of the input signal and reconstructed one recovered by only three IFN spikes are shown in Fig. 2.14-a and -b, respectively. It can be seen that due to reconstruction process low-frequency noise degrades the ENOB from 17 bits to 11 bits.

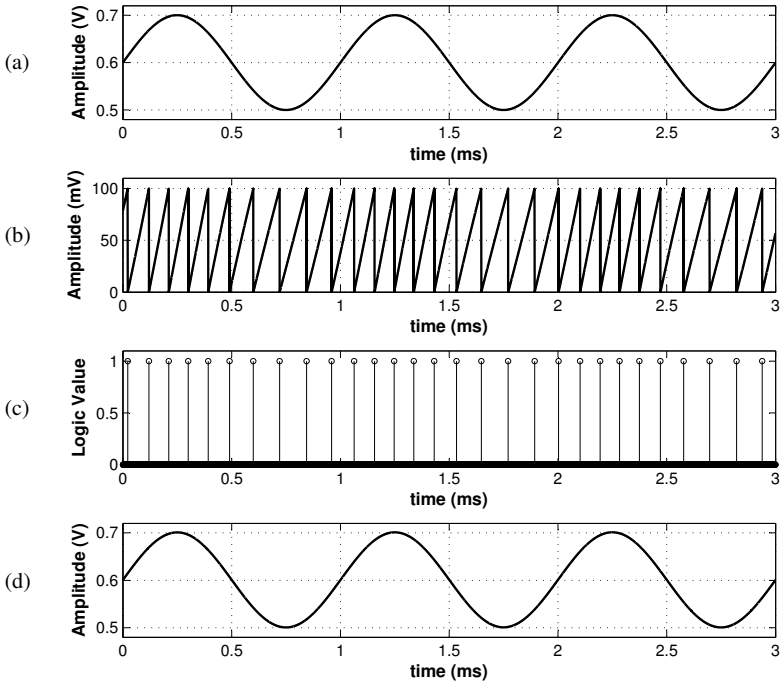


Figure 2.12: Modulation and reconstruction for duration of 3 ms of a sine wave. (a) input signal, (b) integration signal, (c) IFN pulse train, (d) reconstructed signal.

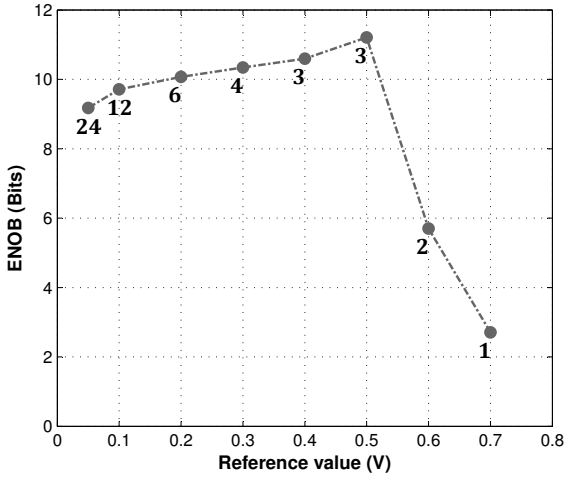
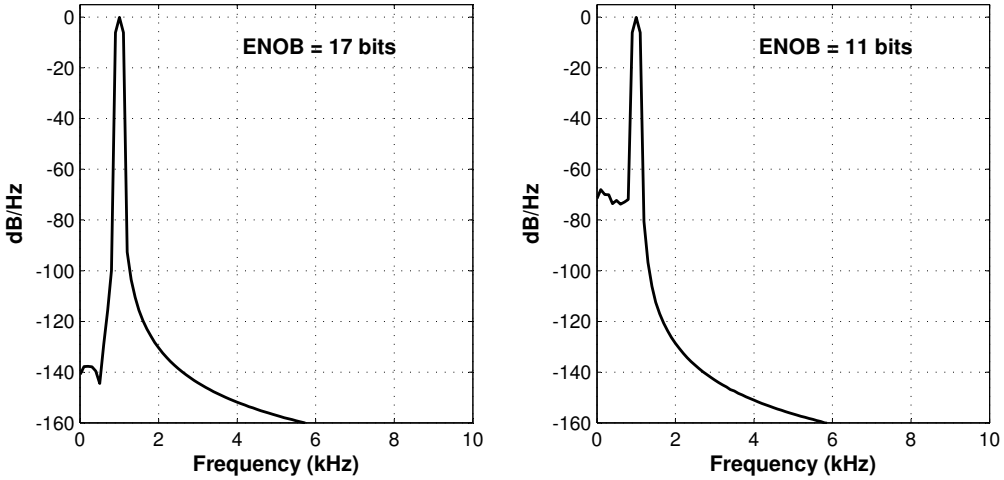


Figure 2.13: ENOB versus different reference voltages using PSD method. The number next to each point indicates the number of required IFN spikes that results in the corresponding ENOB.



(a) (b)

Figure 2.14: (a) PSD of the input sine function (b) PSD of the reconstructed signal using only three IFN spikes and after removing the DC component

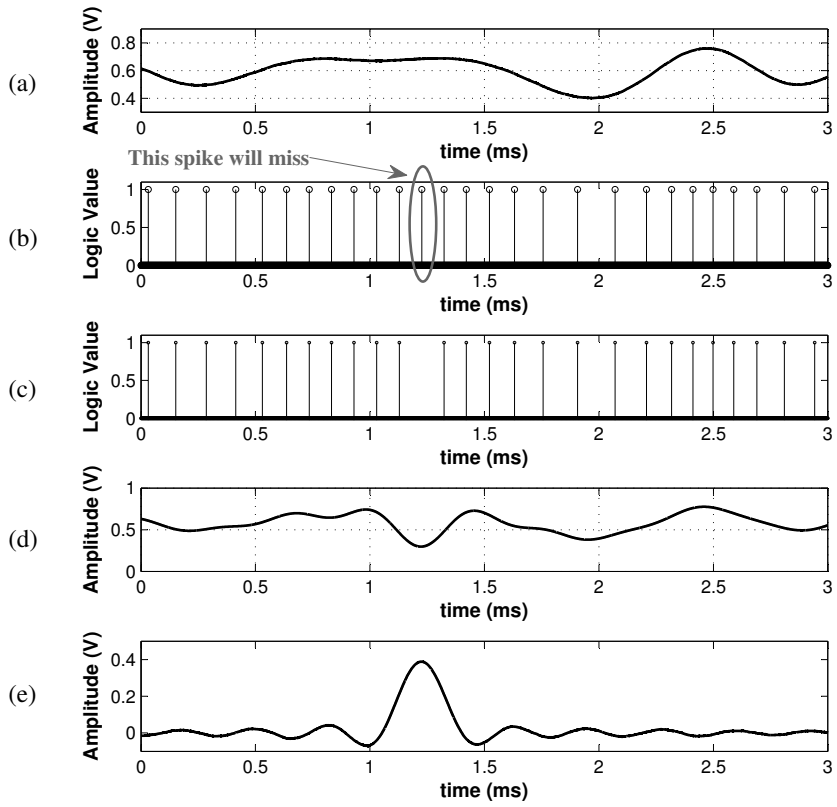


Figure 2.15: (a) input signal, (b) IFN spikes, (c) IFN spikes when one of the spikes are lost due to any disturbance in the channel, (d) failed reconstructed signal, (e) large error signal

2.4.3 What if one spike is missed?

One may ask what happens if one spike is missed. How much does it affect the SER? Let us consider the signal mentioned in subsection 2.4.1 where the modulator generated 20 spikes and after reconstruction SER is equal to 62. Since the distance between spikes are related to the integration process, losing one spike causes a regionally disturbance in reconstruction, and this experiment shows that SER may nosedive to less than 13.8 dB and the signal recovery will fail. This phenomenon is shown in Fig. 2.15.

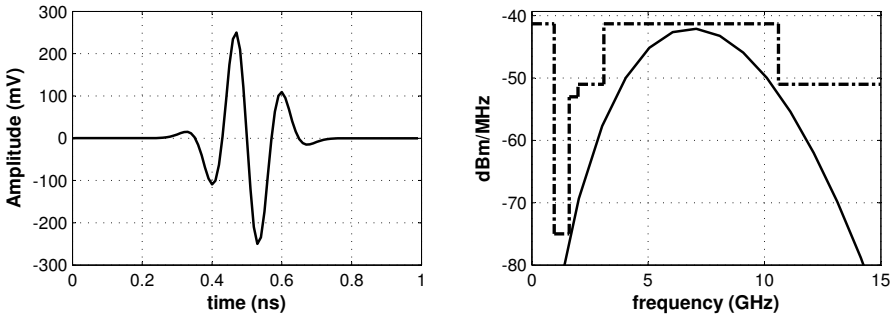
This experiment demonstrates that missing even a single spike easily causes the failure of the packet. Thus, it is absolutely necessary to implement some kind of checksum and error detection mechanism in the IRIF transceiver. This topic will be discussed more thoroughly in section 3.3.

2.5 Performance Estimation

The idea of IRIF transmitter is to generate a bit-stream of time-encoded spikes and then transmit them using an IR-UWB pulse generator. There exists two approaches for sending

the IFN spikes, either to send each spike by a single large-amplitude pulse or a bunch of low-amplitude UWB pulses sent consecutively such that they can deliver enough power to the antenna, fit the FCC mask and represent a one bit detectable by the receiver. Figure 2.16 demonstrates the former while Fig. 2.17 illustrates the latter. In order to meet the bandwidth requirement, the Gaussian UWB pulse has been used. A Gaussian pulse contains an inherent DC component and to avoid it, derivatives of the Gaussian function are then more often used. For the performance estimation analysis, the generated pulse is the 5th derivative of Gaussian function with pulse width of 1 ns and variance of 65 ps [38].

Figure 2.16-a shows a single UWB pulse with an amplitude of 500 mV. Using MATLAB, the PSD of this signal has been calculated for a 50 Ω load, showing that it can satisfy the FCC mask with the peak power of roughly -41.3 dBm/MHz, illustrated in Fig. 2.16-b. The power of this pulse will be detectable by a receiver up to a certain distance. Figure 2.17-a shows 10 consecutive UWB pulses with an amplitude of 260 mV each. Fig. 2.17-b shows the estimated PSD of this signal, which fits the FCC mask. Similarly, the power of these pulses will be detectable for a receiver until a certain distance. In order to maximize this distance, an effort should be made to provide the maximum transmitting power allowed by the mask. For performance estimation, let us assume that each IFN spike is to be represented by 10 consecutive UWB pulses.

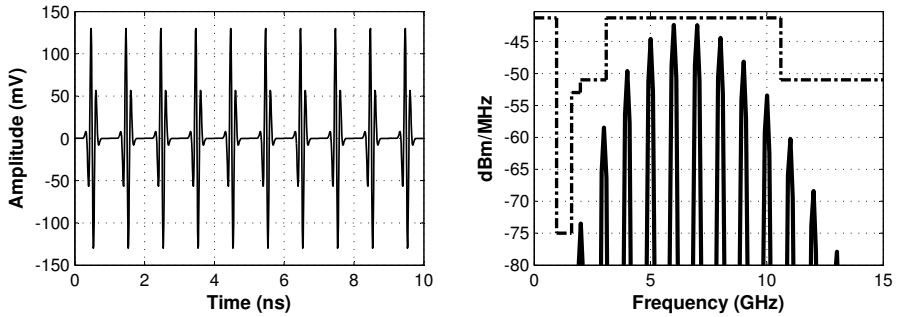


(a) (b)

Figure 2.16: (a) A single UWB pulse with amplitude of 0.5 V, (b) Power spectral density of the pulse compared with FCC mask.

In section 2.4, the number of spikes required for successful reconstruction of random Gaussian signal and sinusoidal wave was studied. In the present section, a comparison will be done for both random Gaussian and sinusoidal signals in order to estimate how much power will be saved by using IRIF transmitter comparing to a BPSK modulator.

According to the previous study (shown in Fig. 2.11), for 3 ms time span of a random Gaussian signal with 400 mV amplitude and band-limited to 1.5 kHz, roughly 20 IFN spikes are required in order to get approximately SER of 62 dB. As already discussed, in the IRIF transmitter this amount of data will be stored in a memory and sent using a



(a) (b)

Figure 2.17: (a) 10 UWB pulse with amplitude of 0.5 V, (b) power spectral density of the 10 consecutive UWB pulses compared with FCC mask.

relatively faster clock to time compress the full IFN signal. Therefore, the IRIF transmitter collects the time-encoded data of the input signal for a relatively long time duration and then transmits it in a much shorter time span, so that multiplexing and re-sending the packet (in case of a repeat request issued due to error), would be possible.

Figure 2.18 illustrates the quality of forming the transmitted signal. First, the slow varying function shown in Fig. 2.18-a is converted to IFN spikes of Fig. 2.18-b and then a single UWB pulse (illustrated in Fig. 2.18-c) is sent representing each IFN spike in the transmitted signal (Fig. 2.18-d). It also shows the 3 ms input random Gaussian wave compressed 10 times and then transmitted within a 300 µs. Since in UWB non-coherent receivers, energy detection circuits consisting of square law and integrator are used to detect the input signal over a certain time interval (timing window) [20], [28], the amount of energy in the UWB pulses can be viewed as a window of energy that is meaningful for the receiver. Let us assume that each window of 10 UWB pulses, called E_w, needs 10 pJ [1], [28], [29] to be built by a UWB pulse generator. Consequently, with 20 IFN spikes, 200 pJ energy per packet of data is required to transmit a 3 ms of the input signal.

As a comparison study, let us assume that the same input signal is applied to a Nyquist-rate ADC. Usually, their sampling rate is 3 to 20 times the input signal's bandwidth [81]. The very same signal is then assumed to be converted by an ADC, and applied to the UWB transmitter by the sampling rate of 6 times its bandwidth, which is 9 kHz and therefore 27 samples in 3 ms are taken. To reach the same SER value as the IRIF transmitter (62 dB), an ADC with roughly 9 bit resolution is needed. In fact, an experiment was made over the Gaussian signal using an ADC of 9 bits and the final SER was roughly equal to 62 dB, as expected. This means that for 3 ms of the signal 243 bits must be generated. If a BPSK digital transmitter stores data in a memory and then sends each bit using the same window of energy as IRIF transmitter (i.e., 10 pJ), then 2 430 pJ energy should be dissipated which is roughly 12 times higher than what IRIF transmitter dissipate. This power comparison

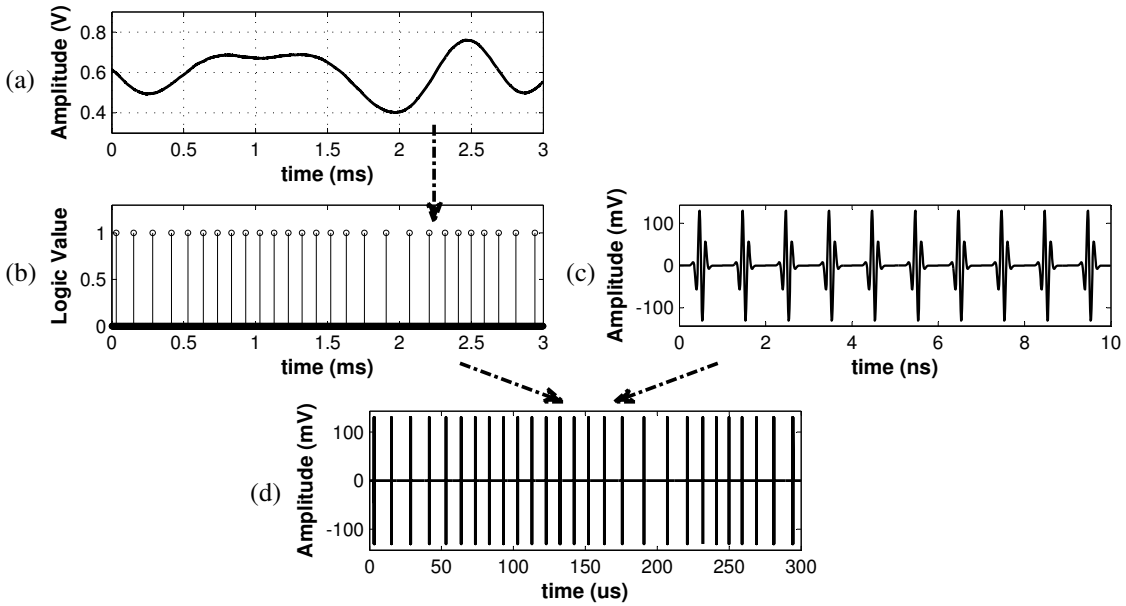


Figure 2.18: (a) 3 ms of the input signal, (b) IFN spikes after modulation, (c) The UWB pulse that is supposed to be sent representing one IFN spike and can be detectable as a window of energy at the receiver, (d) Transmitted signal after 10x compression in time

ratio will be equal to 13.5 for the case of input signal with 100 mV amplitude and ENOB of 10 bits (Fig. 2.11).

One may consider that in the above calculation the assumed Nyquist sampling rate (i.e., 6 times the bandwidth of the input signal), is chosen to make a relatively fair comparison. The above-mentioned energy per bit seems logical as a rule of thumb for comparison, because energy consumption of 0.64-to-250 pJ/bit has recently been reported [1], [28], [29], [51], [82], and is evaluated to be constant for a data-rate of 1 Mbps to 10 Gbps [25] and for energy detection receivers. The power saving mechanism of IRIF transmitter is not only due to the modulation technique but also because it relaxes the need of an ADC that also takes its power toll in transmitters.

For the case of an input sinusoidal wave (explained in subsection 2.4.2), let us say 30 IFN spikes for 10 cycles (3 spikes per cycle) are required to approximately obtain ENOB = 11 bits. Assuming the same amount of energy for E_w, then the overall amount of power consumption for 10 cycles of the sinusoidal wave will be 300 pJ. Now, let us assume that the same input signal is applied to a Nyquist-rate ADC and 60 samples for 10 cycles (6 points per cycle) are taken. With the same ENOB as IRIF transmitter (11 bits) this number of samples means 660 bits. If the preceding BPSK digital transmitter is used, for each bit 10 pJ will be dissipated. Overall, 6600 pJ energy will be consumed which is 22 times higher than IRIF transmitter. Indeed, the IRIF transmission promises a hefty ratio of power saving. All the above study consider BPSK because of simplicity

of comparison. However, OOK modulation could be considered as well. If it is assumed that the signal is applied to a full range ADC, and also the average energy of the signal, above and below the average, are equal, then after conversion the number of zeros and ones would be equal. Thus, it could be inferred that the amount of energy consumed for the case of OOK will be half of that of BPSK, which is still reasonably higher than what the IRIF transmitter dissipates.

2.6 Conclusion

This chapter addressed the theory behind the IFN modulator along with a reconstruction method and the non-ideal parameters that degrade recovery. Different techniques for ENOB calculation were discussed and compared. Effect of sampling frequency was also studied. Simulation shows that the noise on the reference voltage is the major factor that can degrade ENOB, while generally the modulator enjoys a good extent of tolerance against jitter and input noise. In order to reach a reasonable ENOB, the amount of spikes should not be less than a given value that depends on the dynamic of the signal. This issue was studied in this chapter for two cases of random Gaussian signal and a sinusoidal wave. Finally, the performance of IRIF transmitter was estimated and promising results, of power savings, obtained.

Chapter 3

Impulse-Radio Integrate-and-Fire (IRIF) Transceiver

In this chapter the proposed transmitter will be analyzed in a transceiver context and the performance of Tx/Rx is behaviorally studied. In fact, before completely delving into the circuitry of the transmitter, a system-level study has to be performed so as to better understand the bottlenecks and characteristics of such a system.

3.1 IR-UWB Integrate-and-Fire Transceiver

As presented in the previous chapter, and is shown again in Fig. 3.1 a possible architecture of an IFN modulator contains an integrator and a comparator. An operational transconductance amplifier (OTA) converts the input signal into a current that charges the capacitor, C_{mem}; the OTA and C_{mem} form an integrator that continuously do the integration of the input signal. However, synchronized with a clock (f_s), a comparator compares the output voltage of the integrator (V_{mem}) with a fixed reference value. Whenever the threshold is reached, the modulator outputs a high logic value considered as a bit/symbol "1", albeit it retains this value for no longer than a period of the sampling clock, $1/f_s$. During this time, the comparator output activates a switch that resets the integrator. On the contrary, if V_{mem} is less than the threshold, it holds an output low logic value (bit/symbol "0"). Thus, the modulator creates a bit stream of spikes.

Assuming $x(t)$ a band-limited input signal within $[-\Omega_N, \Omega_N]$ and t_i a timing sequence, equation 2.8 formally shows the key characteristic of the modulator, the equal time-integration defined by θ. The minimum spike-generating rate is related to maximum adjacent interval, i.e. $\delta_{max} = sup(t_{i+1} - t_i)$. Provided that the minimum sample rate is above Nyquist ($\delta_{max} < 1/f_{Nyquist}$), the input signal can be recovered [71, 78].

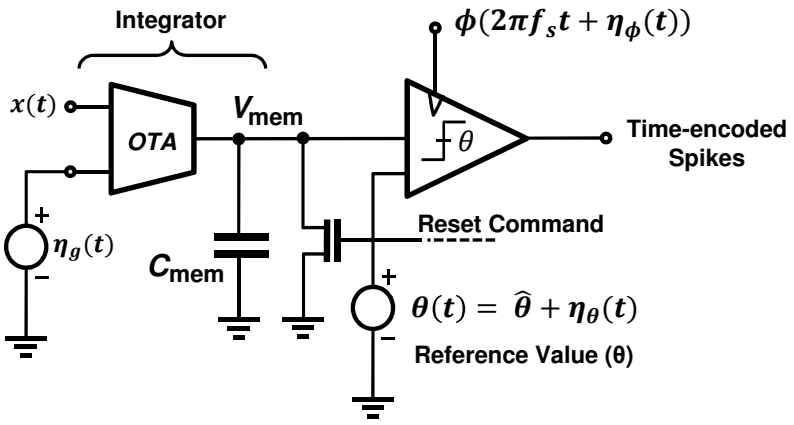


Figure 3.1: Integrate-and-fire neuron circuitry including noise and jitter

The IFN converter can serve as a baseband modulator in a UWB transmitter. To transmit each bit of "1" in the bit stream, a carrier-less UWB pulse generator (i.e. IR-UWB technique) is used, as discussed in previous chapter. The complete architecture of the IRIF transceiver is presented in Fig. 3.2. As mentioned in section 2.5, each spike can be sent by either a single high-amplitude UWB impulse or a burst of several low-amplitude consecutive impulses. In terms of architecture, there will be no difference between these two methods. The common requirement for both techniques is not to cross the FCC mask EIRP value (-41.3 dBm/MHz). In this system-level study the second method is chosen and every IFN spike will be transmitted by 10 consecutive UWB impulses. IRIF transmitter fundamentally comprises an IFN modulator, a digital controller and memory, and an impulse-radio generator. Because UWB pulses are short in time, the incoming signal can be compressed and then sent by a faster clock. Therefore, a digital controller circuit needs to be embedded in-between the modulator and the pulse generator in order to store data in a memory using the clock (f_s) while it reads the data by a faster clock (f_r) and feed the UWB pulse generator. This process is illustrated in Fig. 3.2-a. Moreover, the compression makes the transmitter capable of serving multiple inputs. Notably, the pulse generator is silent most of the time and only generates impulses whenever it receives a bit of "1" at the input; this will greatly improve the power efficiency. Shown in Fig. 3.2-b, a power detection architecture can be utilized at the receiver so as to detect the received burst of UWB pulses. In fact, whenever a UWB impulse is received, a symbol "1" will be stored and when no UWB impulse is to be detected, a symbol of "0" will be recorded in the memory. Afterwards, a digital processor reconstructs the original signal.

Recalling from Fig. 2.18-a, the signal is converted into time-encoded spikes (Fig. 2.18-b) by a clock frequency of $f_s = 10\,\text{MHz}$. In the transmitted signal, each IFN action potential is represented by 10 UWB impulses as shown in Fig. 2.18-c. They have nearly

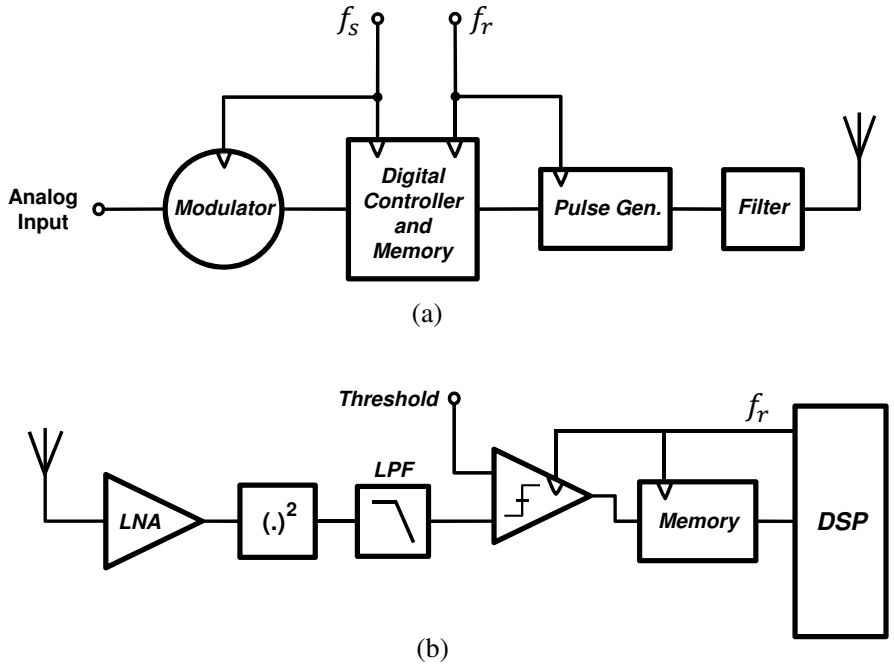


Figure 3.2: Block diagram of IRIF transceiver: (a) transmitter, (b) receiver

260 mV peak-to-peak amplitude and create a burst of pulses that signifies a bit of "1". The transmitted signal (shown in Fig. 2.18-d) is a compressed version of IFN bit stream; in fact 3 ms of the original input signal is sampled by a clock frequency of $f_s = 10\,\text{MHz}$ and is sent by a 10 times faster clock frequency of $f_r = 100\,\text{MHz}$. In other words, the original input signal will be ten times compressed in time and sent within 300 µs. Notably, every 3 ms portion of the input signal, along with start and end marks, and a checksum, forms a packet.

3.1.1 Channel Model

The transmitted signal will be greatly affected by noise and will face the path loss through the channel. Thus, an attenuated noisy signal will be sensed at the receiver. In this study, an AWGN channel with fading effect is considered. Multi-path effect is not considered because both the communication distance and pulse duration are short, any reflection is either faded or will add up with the pulse transmitted in line-of-sight. Other dispersion effects in the channel distorts the pulse. Nevertheless, the IRIF transceiver is an energy-detection system and signal distortion is not very important, as long as the total energy remains.

For a UWB waveform occupying the band $f_c - W/2$ to $f_c + W/2$, with flat power spectral density P_{ave}/W, and assuming perfect antennas with gains of 0 dBi at the trans-

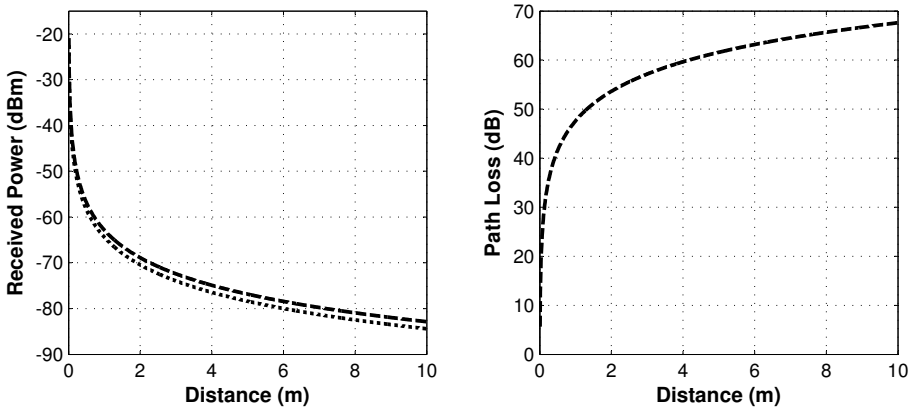
mitter and receiver, the total average received power at the output of the receiving antenna will be given by [83]:

$$P_{Rave} = P_{ave}^{NB}\left[\frac{1}{1-(W/2f_c)^2}\right], \tag{3.1}$$

where W is the signal bandwidth and f_c is the centre frequency. P_{ave}^{NB} is the well-known narrow-band path loss shown in equation (3.2) where c and d are the speed of light and the distance between transmitter and receiver, respectively.

$$P_{ave}^{NB} = \frac{P_{ave}\cdot c^2}{(4\pi d)^2\cdot f_c^2}, \tag{3.2}$$

Calculations show that the narrow-band model can be used to approximate the path loss for a UWB system. For the largest fractional bandwidth (3.1-10.6 GHz), P_{Rave} will differ from P_{ave}^{NB} by only 1.5 dB at d = 10 m [83], and this difference becomes smaller for smaller fractional bandwidths. This characteristic is shown in Fig. 3.3-a; it also shows how fast the signals will be attenuated through space. Figure 3.3-b illustrates the path loss which is calculated using the averaged PSD of the transmitted 10 UWB pulses which is equal to -11 dBm. Additionally, -90 dBm/MHz channel noise is considered and added. This means that if the received signal has less power than that of the channel noise, it will not be detected. Increasing the noise level eventually will prevent the signals to be well detected at a distance of one meter.

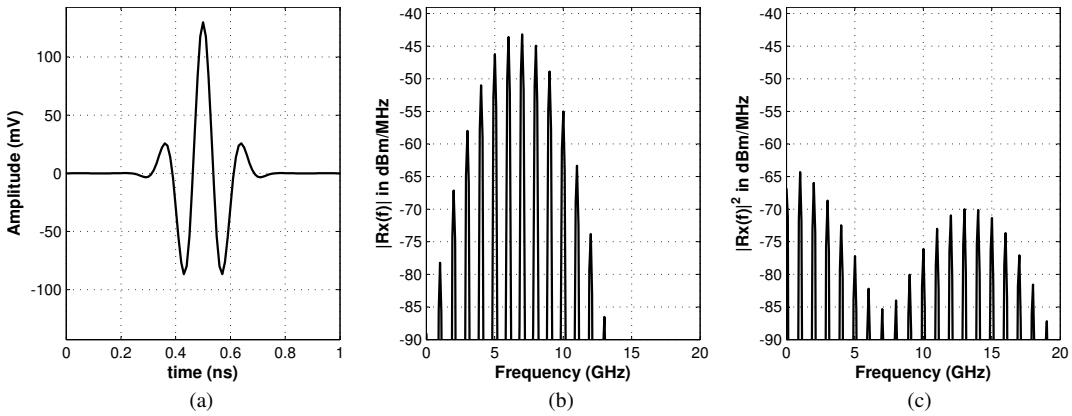


(a) (b)

Figure 3.3: (a) Received power for narrow-band and ultra wide-band as a function of distance, (b) Path loss vs. distance

3.1.2 Energy Detection Receiver

IRIF transceiver uses a non-coherent energy-detection (ED) receiver. It consists of a low-noise amplifier (LNA), which needs a certain sensitivity for the signal to be detected and it will be discussed later in 3.2. After the LNA, an energy detection circuit is used which performs squaring and integration followed by a comparator to detect the energy level, thus, the bits (Fig. 3.2-b). Afterwards, a digital processor is needed to reconstruct the original signal using embedded data within each packet. Since the transmitted UWB signal can be approximated by a Gaussian pulse modulating a carrier, it can be expressed by equation 1.1. Figure 3.4-a shows one of the ten Gaussian pulses representing one IFN spike in the transmitted signal that has been built with A = 0.125 V, τ = 0.2 ns and f_c = 6.7 GHz. At the receiver side, after the amplification by LNA, a squarer is used to multiply the signal by itself. In frequency domain, a received pulse train has a one-lobe PSD (Fig. 3.4-b) while squaring splits it into two parts shown in Fig. 3.4-c. The first fragment is down-conversion of the Gaussian envelope and the second one is the up-conversion of it centered at $2f_c$ [34]. The first part may be utilized to detect a received UWB signal. Since it has low frequency components, the energy detection can be done by a low-pass filter and a comparator, which leads to a simpler circuit architecture (Fig. 3.2-b).



(a) (b) (c)

Figure 3.4: (a) a Gaussian UWB impulse, (b) power of received signal, (c) Power of squared received signal

3.1.3 Signal Recovery at the Receiver

In this dissertation, the above-mentioned channel model and path loss have been used to ultimately calculate the received power at the receiver. Using the path loss at each distance and corresponding power of the received signal, an appropriate value for energy of a bit "1" (E_b) can be found and then the threshold in power detector (see Fig. 3.2-b) can be set. For that purpose, after squaring the signal a low-pass filter is realized by an integrator;

the output of the integrator is used to characterize the energy of a bit "1" which indicates the presence of an IFN spike. Clearly, if the transmitter-to-receiver distance increases, the path loss boosts and E_b/N_o will nosedive. The key point in UWB systems which are supposed to operate in IEEE standard 802.15.4 is the power limitation imposed by FCC rule that only allows small transmission power. Therefore, E_b/N_o is highly limited and so does the transmission range. Additionally, sensitivity improvements can be considered for power saving and/or improvement of the transmission range that will be discussed in section 3.2.

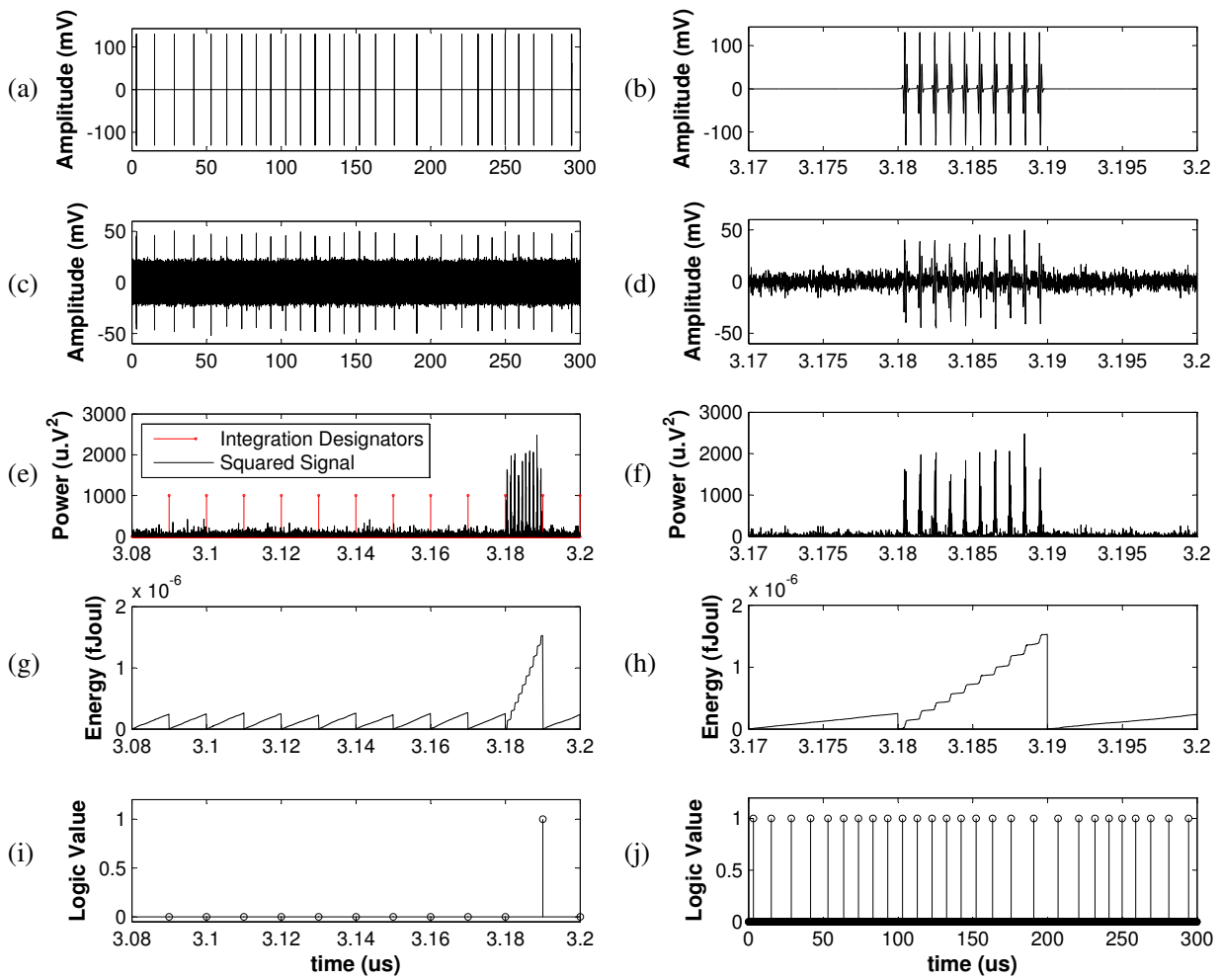


Figure 3.5: Reception quality when the distance between Tx and Rx is 1 meter (a) Transmitted signal, (b) A burst of pulses representing a bit "1" in the transmitted signal, (c) Received signal amplified by LNA, (d) A burst of pulses representing a bit "1" in the amplified received signal, (e) A portion of the squared signal, (f) A squared burst of pulses, (g) A portion of the filtered signal, (h) Integration result of a burst, (i) Recovery of an IFN spike, (j) Recovery of all IFN spikes

The quality of signal reception, when the transmitter and receiver are located at one meter distance, is shown in Fig. 3.5. According to Fig. 3.3-b the path loss at d equal to 1 m is 47 dB. The power gain of the LNA is assumed to be 10 dB [84], [85], [86], although a higher gain could be attained if LNA is terminated with a load larger that the standard 50 Ω. So, the transmitted signal (Fig. 3.5-a) is attenuated by 47 dB and then amplified by 10 dB, as shown in Fig 3.5-c. A burst of pulses which represents an IFN spike in the transmitted signal, and its amplified received version, are shown in Fig. 3.5-b and -d, respectively. As discussed above, passing the LNA, the signal will be squared; a small portion of the rectified waveform is shown in Fig. 3.5-e, including one burst of pulses which is illustrated individually in Fig. 3.5-f. An integrator has been utilized as an LPF to detect the energy of each bit, shown in Fig. 3.5-g and -h. In order to distinguish the energy of bits "0" and "1" a comparator shown in Fig. 3.2-b has been used and a threshold value of %90 of E_b has been set. Therefore, the IFN spikes can be recovered by finding the bursts as can be seen in Fig. 3.5-(i,j). Finally, time-encoded IFN spikes (identical to what was shown in Fig. 2.18-b) are obtained and the original signal can be recovered by the digital circuit afterwards as described earlier. Using the reconstruction method discussed in chapter 2, the signal is recovered with a SER nearly equal to 62 dB (which roughly corresponds to $ENOB = 9$ bits).

3.1.4 Bit Error Rate (BER) Calculation

According to signal-space analysis theory, at each transmitter to receiver distance, symbols "1" (presence of an IFN spike) and "0" have certain energy in the constellation diagram. As the physical distance increases, the difference between their energy will shrink, such that ultimately they cannot be distinguishable. Output bit-stream in IRIF transmitter has similarities with that of on-off keying (OOK) technique, thus a similar constellation diagram, as shown in Fig. 3.6, can be used for BER estimation. Since the distance between symbols *no IFN spike* ("0") and a *spike* ("1") is $\sqrt{E_b}$, equation (3.3) gives the error probability (P_e) plotted in Fig. 3.7. In equation (3.3), d is the Euclidean distance between the squared power of each symbol and $2N_o$ is the one-sided spectral noise power [87]. It shows that if the E_b/N_o raises, the BER of IFN detection decreases. In particular, the complementary error function (erfc) is a statistical expression and can be used for error probability regardless of how the energy is calculated. This result will be important in the next section where the link budget is addressed.

$$P_e = \frac{1}{2}\mathrm{erfc}\Big(\frac{d}{\sqrt{2N_o}}\Big) = \frac{1}{2}\mathrm{erfc}\Big(\sqrt{\frac{E_b}{2N_o}}\Big) = \frac{1}{2}\mathrm{erfc}\Big(\sqrt{SNR/2}\Big) \tag{3.3}$$

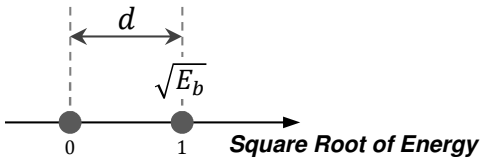


Figure 3.6: Constellation diagram. E_b is the energy of 10 consecutive impulses that defines a bit of '1'.

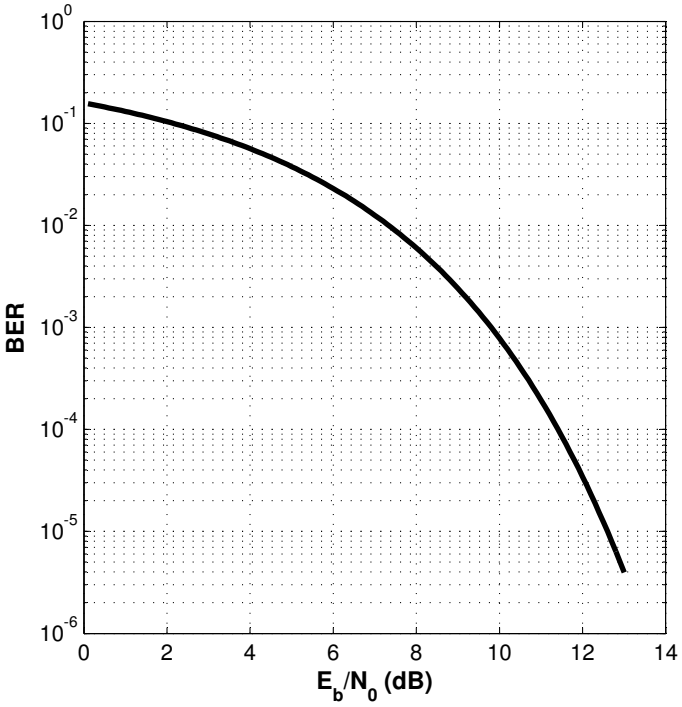


Figure 3.7: Bit error rate (BER) diagram

3.2 Link Budget

In non-coherent energy detection receivers, integration will increase the SNR since the signal is coherent and the noise is not. Thus, higher transmission range is achievable, although in UWB standard this range is expected to be relatively small compared to narrowband techniques. In order to approximate the transmission range of the IRIF transceiver a link budget has been studied. As shown in Fig. 3.8, the received power can be calculated using

$$P_R = P_T + G_T - PL(d) + G_R, \tag{3.4}$$

where P_T is the transmit power, $PL(d)$ is the path loss at distance d, G_T and G_R are the gains of transmitting and receiving antennas, respectively. Ideal antennas are assumed with gain of $G_R = G_T = 0\,\text{dBi}$. Path loss can be considered as a limit that degrade the transmit power and determines the minimum receivable power; on the other hand, sensitivity of the receiver is another constraint that defines the minimum detectable power. If the sensitivity power level (S_i) is not higher than the received power (P_R), the incoming signal is detectable. In other words, along with an up-limit (minimum receivable power, P_R), there exists a few constraints that form a bottom-limit called sensitivity. These constraints are physical thermal noise, noise figure (NF), and minimum required signal-to-noise ratio that all define the sensitivity of the LNA. Thermal noise power level is equal to KT_oB, where K is the Boltzmann's constant, T_o is the room temperature used here as a reference while in practice it is the temperature of the environment, and B is the desired bandwidth that is 7.5 GHz in the case of UWB range. Another constraint is NF, which is a circuit limitation and depends on the topology of the circuit and the bandwidth [84]. As a matter of fact, the huge bandwidth of UWB regime affects the reception in two ways; not only it increases the total power level of thermal noise (KT_oB) but also raises the noise figure of the electronic circuit, and they both degrade the receiver sensitivity. Therefore, the sensitivity can be defined as $S_i = 10 \cdot \log_{10}(KT_oB) + NF + SNR$.

According to Fig. 3.7 for a BER value of 8×10^{-4} the minimum required SNR is 10 dB, also let us assume the electronic noise figure is 3 dB [85]. Clearly the value of $10 \cdot \log_{10}(KT_oB)$ + 30 dB is equal to -75 dBm. Thus, the sensitivity of the designed receiver would be at least -62 dBm. Inferred from Fig. 3.3-a, for -62 dBm received power the transmission range is 1 m. These facts are illustrated in Fig. 3.8. In other words, if the LNA is designed with the sensitivity of -62 dBm, the received power (P_R) will have such power level when the transmitter and receiver are located at $d = 1\,\text{m}$ distance. This study shows that the IRIF transceiver is realizable inasmuch as low-sensitivity UWB LNAs are

available [85].

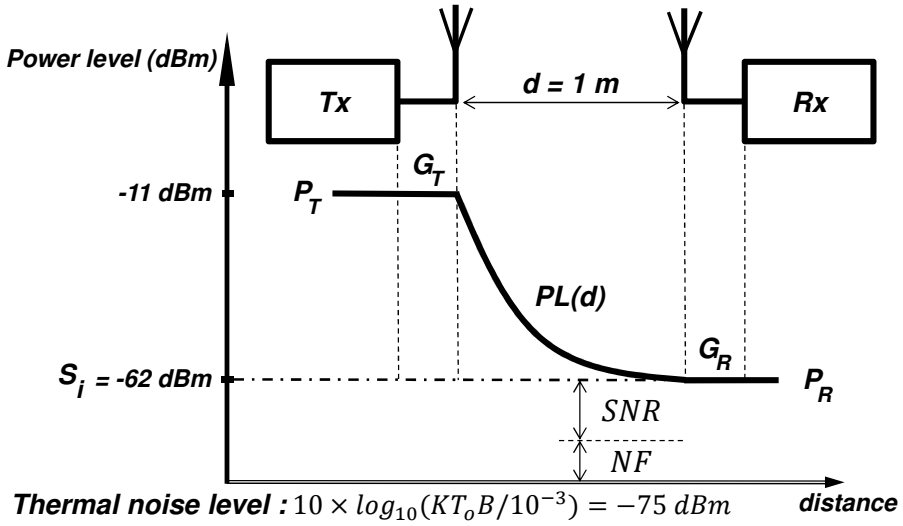


Figure 3.8: Link budget diagram

3.3 Packet Definition and Checksum

Obviously, a reliable transceiver system does require an error detection method and the transmitter must be able to treat a repetition request for a packet. Indeed, this capability will improve BER and transmission range. As discussed in section 2.4.3, the packets will be damaged if any of the IFN spikes is missed. Because of that, it is absolutely necessary to implement some kind of checksum and error detection mechanism in the IRIF transceiver. As mentioned above, an IFN spike can be sent either by a single large amplitude UWB impulse or a burst of several low-amplitude ones, e.g., ten impulses can represent one IFN spike. Yet, the latter will require ten times faster clock, i.e., 1 GHz. An oscillator with such a speed is practically a power hungry block. Thus, in practice the former (Fig. 2.16) will be used for CMOS implementation. Besides, the transmitted signal could be synchronized with slower clock rate, namely 100 MHz.

While only one UWB impulse represents an IFN spike, one possible approach to packetize the data is to build any of start, end and checksum symbols with ten consecutive UWB impulses having the same amplitude as those inside the packet. Since, during the modulation, occurrence of any two consecutive IFN spike will not be feasible, the receiver accepts ten consecutive UWB impulses as mark symbols so that the receiver can distinguish them from the data within the packet. The checksum itself can be a silent time between end symbol and a checksum-end symbol that represents the number of IFN spikes within the packet. In fact, number of zeros in the silent time will be counted by

the receiver and, in case an error occur, it sends back a repeat transfer request (RTR). Thereafter, the transmitter will able to detect it and repeat the packet.

3.3.1 Checksum Efficacy Verification

The efficacy of different error detection methods depends on the operating environment, the transferred data, the complexity of network, and the types of bit errors caused by noise and other sources. However, using MATLAB, a simple case study has been performed to verify the effectiveness of the proposed checksum.

The test has been done assuming that the transmitter and receiver are at 3 m distance. The threshold value on the power detector, at the receiver, is set to 90% of energy of a bit, E_b. The test has been done for 1000 random packets. If any packet was corrupted, the transmitter resend it whenever an RTR signal is sent back, however, it will be done for the maximum nine number of tries, because the silent time between two main packets does not allow for more than nine tries without any loss on a continuous sensing. If no checksum is used, 41% of the packets will be missed under the experiment conditions. Yet, by the aid of the proposed checksum, only 2 packets failed and could not be recovered even after nine tries.

3.4 Conclusion

In this chapter, integrate-and-fire modulator has been embedded in an impulse-UWB radio transceiver system and a new autonomous non-coherent architecture is proposed, the so-called IRIF transceiver. The architectural model is implemented in MATLAB and investigated. A simple AWGN channel model including fading effect is utilized and path loss is estimated. Power of transmitted and received signals are calculated and signal recovery at the receiver has been carried out. Additionally, a link budget shows that for a BER value of 8×10^{-4} the transmission range will be around 1 m. After all, a checksum is proposed in order to data recovery, in case error correction is needed.

Chapter 4

CMOS Implementation

As mentioned above, the IRIF transmitter comprises three main circuits or sub-systems, including the IFN modulator, a digital controller, and a UWB pulse generator. Given that the IRIF technique is proposed to reduce the power consumption of UWB transmitters, low-power design must be considered in all building blocks. In this section, the CMOS implementation of the whole system will be discussed. The transmitter has been fabricated using the CMOS process of a 0.13 µm technology node with 1.2 V supply voltage.

4.1 Integrate-and-Fire Modulator

As mentioned earlier, in chapter 2, the integrate-and-fire modulator simply consists of analog/mixed circuits, including an integrator, a track-and-latch (T/L) comparator, and a few logic gates. Here, let us describe every circuit that has been designed and utilized in the modulator.

4.1.1 Operational Transconductance Amplifier (OTA)

In theory, one possible integrator circuit could be an OTA with capacitive load that can be modeled as a single pole system. It is shown in Fig. 4.1. Assuming that all the high frequency poles are ignorable and that are much larger than the dominant pole, the transfer function of such a circuit can be simplified to equation 4.1, where $A_o = G_m R_O$ and $\tau = R_O C_m$. If $s\tau \ll 1$, the equation can be reduced to $V_O/V_{IN} = k/s$, where $k = A_o/\tau$. In such condition, the phase is equal to -90 degrees and gain drops by 20 dB/dec. The frequency of the dominant pole ($1/R_O C_m$) must be chosen based on the application. Overall, in this simplified model there are three parameters, namely R_O, C_m and G_m, that affect the frequency response of the integrator, as illustrated in Fig. 4.2. As shown in Fig. 4.2-a,

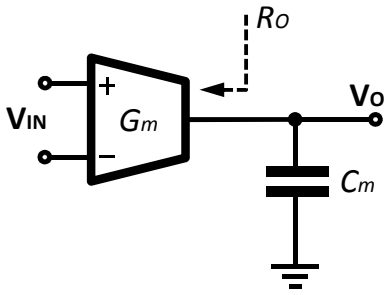


Figure 4.1: An OTA with capacitive load that can be modeled as a single pole integrator

if G_m increases, the gain will increase while the dominant pole remains unchanged. Figure 4.2-b illustrates that if C_m becomes larger the dominant pole will shrink and provides more bandwidth for the integration, while the gain will remain the same. In the architecture of the integrate-and-fire modulator, the name of C_m will change to C_{mem} which is the reminiscence of the functionality of the membrane in the integrate-and-fire neurons. Enlarging R_O increases the gain while pushes the dominant pole towards smaller frequencies (Fig. 4.2-c). In fact, the condition $s\tau \ll 1$ becomes a better approximation, making the transfer function of the one-pole system more similar to that of an ideal integrator, i.e., $V_O/V_{IN}(s) = k/s$.

$$\frac{V_O}{V_{IN}} = \frac{A_o}{1+s\tau} \tag{4.1}$$

Obviously, the OTA circuit is crucial to the linearity of the integrator and the quality of modulation. In fact the G_m value should not change for the whole range of the input signal amplitude. The input linear range must be typically large because the input signals might have large amplitude. Besides, given that the OTA is supposed to be utilized in a low-frequency integrator, it must show a very large time constant or equivalently a very small trans-conductance, in the range of nS. To achieve small trans-conductance, OTAs are usually designed in weak inversion operation region of MOSFETs, so that the power consumption of the circuit will noticeably decrease as well.

Designing OTAs in weak inversion is challenging. The high g_m/I ratio that MOSFETs present in this operation region limits the input linear-range. It corresponds to a technology parameter and equals $1/n\phi_t$, where n is the subthreshold swing factor and $\phi_t = kT/q$ is the thermal voltage [88]. As the size of transistors and supply voltage shrink, the input linear range decreases as well. However, for linearity improvement source degeneration technique have been utilized. To be used in the IFN modulator, a low-power current-mirror OTA, shown in Fig. 4.3, is designed using a simple source degeneration.

In the proposed OTA, M_3 and M_4 have the aspect ratio of $W/L = 0.65\mu m/47\mu m$, op-

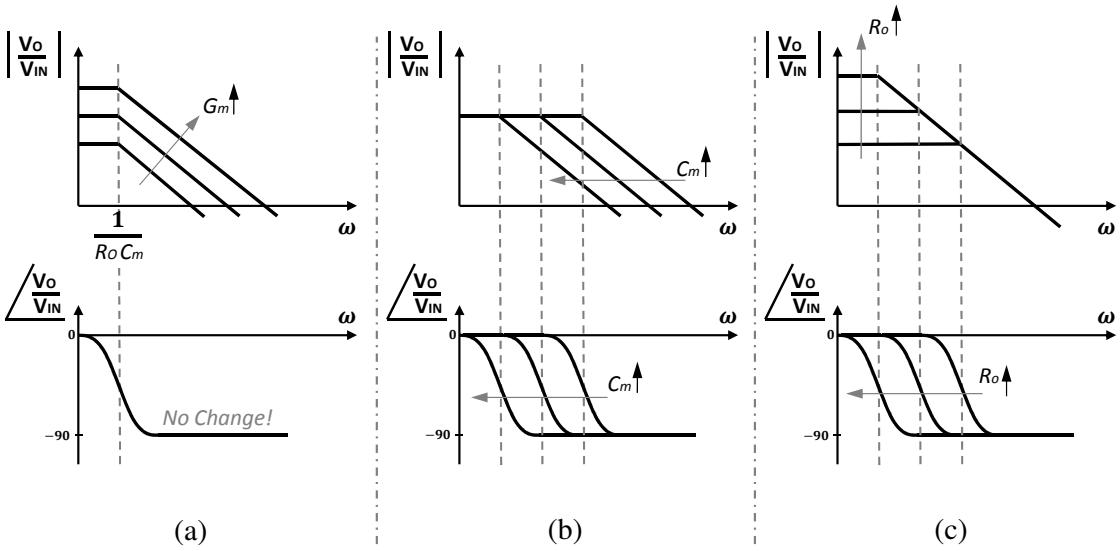


Figure 4.2: Effects of R_O, C_m and G_m on the frequency response of the integrator

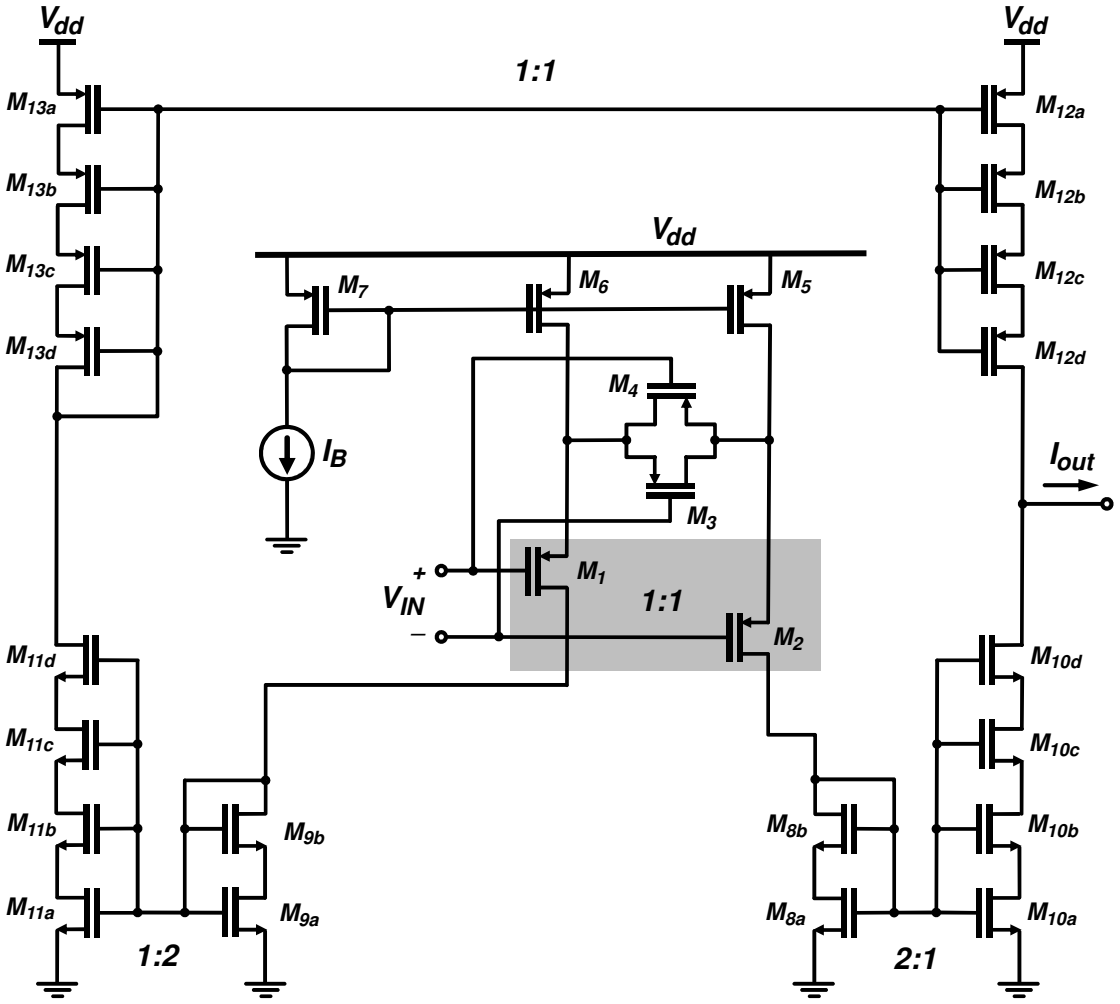
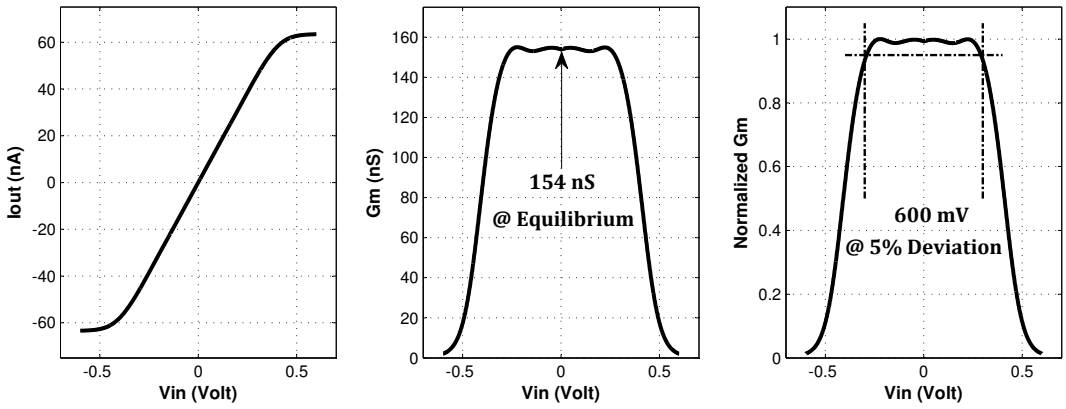
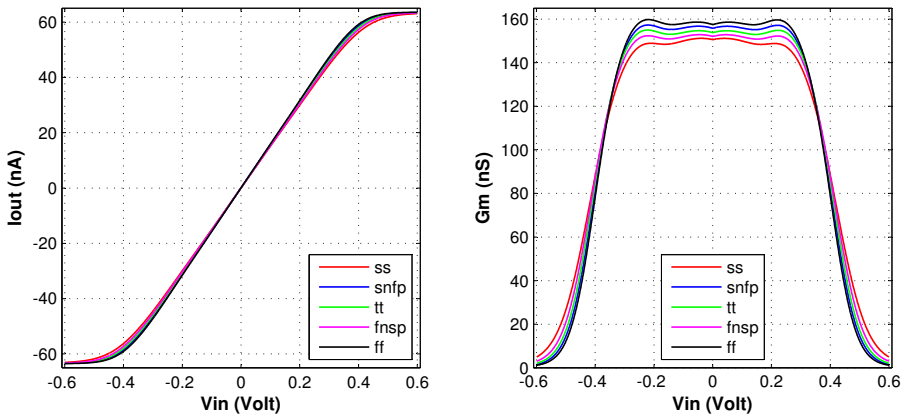


Figure 4.3: Circuitry of the OTA



(a) (b) (c)

Figure 4.4: Post layout simulation for DC analysis (a) Output current, (b) Transconductance G_m), (c) Normalized transconductance



(a) (b)

Figure 4.5: Results for DC corner analysis (a) Output current, (b) Transconductance (G_m)

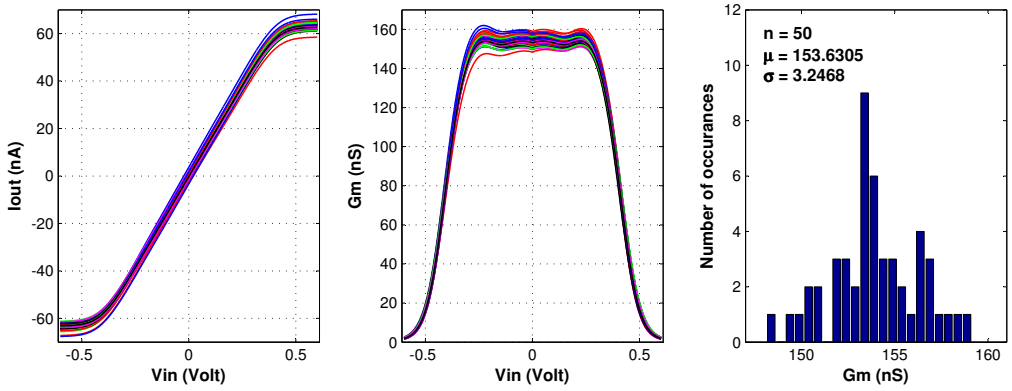


Figure 4.6: Monte-Carlo simulation for DC analysis (a) Output current, (b) Transconductance (G_m), (c) Monte-Carlo results for transconductance

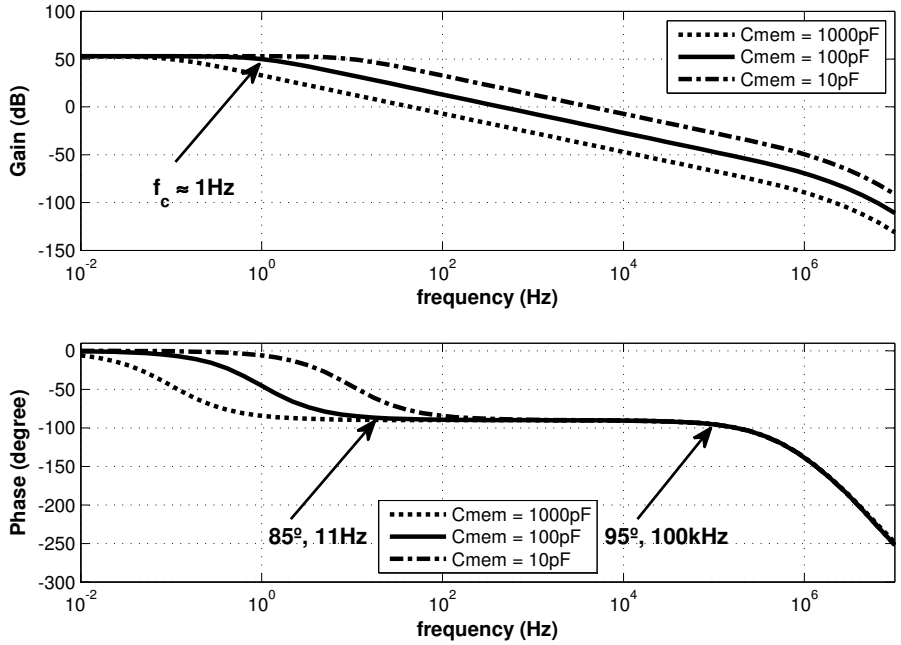


Figure 4.7: Results of AC analysis for different values of C_{mem}.

erate in triode region and together behave as a degenerating resistor. Transistors M_{5-7} are current mirrors for the input stage and are all equal in size ($W/L = 4\mu m/45\mu m$). M_1 and M_2 are the input differential stage with aspect ratio of $W/L = 1\mu m/10\mu m$. Series-parallel structures (M_{8-13}) containing equal size transistors ($W/L = 0.35\mu m/8\mu m$) are used for the active load stage. It acts as a combination of series transistors in current mirrors that can be treated as a long channel transistor [89]. It is a form of building equivalently longer transistors that saves area and improves matching and channel-length modulation [90], [91]. Thus, considering the above-mentioned sizes, a high resistance of 4 GΩ is expected seen from the output of the OTA [89]. The amplifier is biased by a current source of $I_B = 65$ nA. A post-layout analysis has been carried out and demonstrated in Fig. 4.4; the amplifier provides a transconductance value of 154 nS around the origin, while maintaining a linear input range of 600 mV with only 5% of deviation in G_m. Figures 4.5 and 4.6 demonstrate the corner analysis and Monte-Carlo simulations, respectively, considering inter-die mismatch and intra-die process variations.

In the integrate-and-fire technique, the offset of the OTA will not cause saturation because the integrator will reset after it reaches a certain threshold. Offset only adds/-subtracts an additional value to/from the integration voltage at the output of the OTA. Precisely speaking, the only impact of offset is a shifted-in-time firing, which may be critical in terms of final conversion SNR (as seen before). On the other hand, there are two degrees of freedom to cope with the offset. First, the reference voltage of the modulator ($\hat{\theta}$ in Fig. 3.1) is tunable. Second, the threshold value, θ, used in the reconstruction

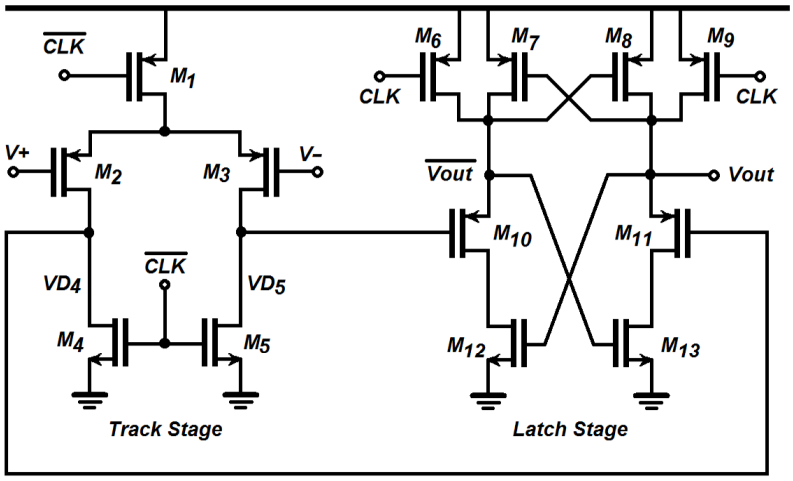


Figure 4.8: T/L Comparator

process (see equation 2.14), is also tunable. All in all, the modulator can be robust to any distortion caused by offset of the OTA, as long as these two parameters are used to compensate it in a tuning process.

Also in Fig. 4.7 the post-layout AC response of the integrator is plotted showing the capability of integration for a large frequency range of signals up to 100 kHz and as low as 0.1 Hz and 1 Hz if capacitors of 10 nF and 100 pF are applied as C_{mem}, respectively.

4.1.2 T/L Comparator

Latch-type or flip-flop based sense amplifiers, are a kind of track-and-latch (T/L) comparators widely used in memories, ADCs and on-chip transceivers [92]. They achieve fast decisions due to a strong positive feedback. There are different topologies of low-power T/L comparators that have no static current which have been widely used in low-power circuit designs [93], [94], [95], [96], [97], [98]. In this dissertation, and to demonstrate the concept of IRIF transmitter, one of them (i.e., [94]) has been utilized. It has no static current and therefore suitable for low power designs.

The comparator is composed of two stages, as shown in Fig. 4.8, namely a track and latch stages. The first stage tracks the difference between the input terminals, while the latch stage will store the comparison results. In detail, the comparator functions as follows. When the clock level is low, the channels of M_4 and M_5 are inverted so that the nodes VD_4 and VD_5 are grounded, holding logic "low"; meanwhile V_{out} and $\overline{V_{out}}$ have charged to logic "high", because M_6 and M_9 are on. In a rising clock edge current flows through M_1 and because M_4 and M_5 are off, this current charges the intrinsic capacitors of nodes VD_4 and VD_5. Depending on input voltages and their difference, one of the capacitors will charge faster than the other, turning on either M_{10} or M_{11}. As long as the

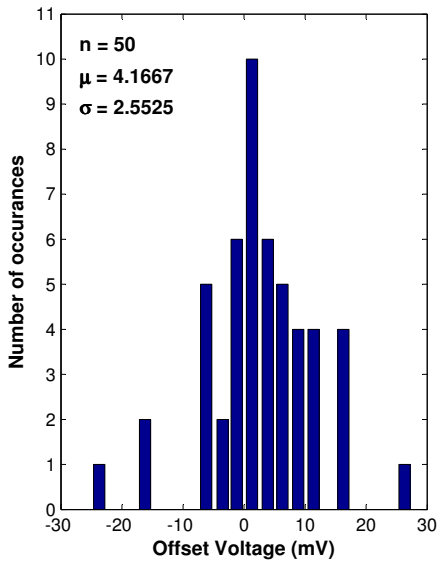


Figure 4.9: Mont-Carlo analysis for the offset of the comparator.

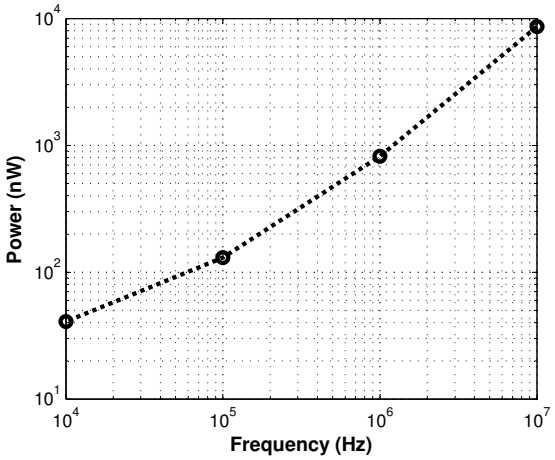


Figure 4.10: Power consumption of the comparator in terms of clock frequency.

clock is high the data is latched at the output. This means that the latch stage can hold the output data only for half a cycle of the clock. In the IFN modulator a clock signal with doubled frequency is used to precisely store the output value of the latch in a D-type flip-flop.

The offset of the comparator may inject jitter error to spike locations in the output bit-stream. Thus, large input transistors are chosen in order to average out the mismatch of the input differential pair. Monte-Carlo simulation for input offset including both inter-die mismatch and intra-die process variations is shown in Fig. 4.9.

Furthermore, as shown in Fig. 4.10, the comparator dissipates roughly 40 nW of power at clock frequency of 10 kHz while it increases as the frequency goes up. Its comparison delay time is 25 ps.

4.1.3 IFN Modulator

The designed IFN modulator along with the required off-chip auxiliary components is shown in Fig. 4.11. The integrator is formed by an OTA and an off-chip capacitor C_{mem}. As the OTA receives any analog signal within its input linear range, it converts it into a small flow of current (I_{out}). While this current is continuously charging C_{mem} the comparator periodically compares the voltage across it (V_{mem}) with the reference voltage (V_{REF}). Such system modulate the input signal, $v_{IN} = V_{IN} + v_{in}$, to a bit stream, where v_{in} represents the input signal (which is chosen to be a sine wave for testing purposes) superimposed by a DC value, V_{IN}. To distinguish the elements of the signal, different notations are chosen for DC and AC parts. V_{CM} is the common-mode voltage that is used to bias the OTA and is equal to half of the supply voltage.

Whenever the V_{mem} reaches the threshold V_{REF}, the output of the comparator jumps up at the next rise edge of the comparison clock. The comparator clock signal is called CLOCK_FS and will be applied by a digital interface circuit to be described later. Since the jump does not occur concurrently with the crossing point of the input signal and reference voltage, it creates jitter and inserts some quantization error to the system that degrades the SNR [61]. Obviously, by increasing the sampling frequency, f_s, the time resolution will improve and the error diminishes. Then, after a certain delay ($\tau_r = 1/f_s$), the switch, which is normally open, will become short and discharges/resets the capacitor C_{mem}. Afterwards, V_{mem} will become zero and in the next clock cycle, the output of the comparator goes back to zero and then again C_{mem} start being charged until the next time that V_{mem} reaches the threshold V_{REF} and another spike occurs. As mentioned earlier in subsection 4.1.2, the latch stage of the comparator can hold the latched data for half of its clock cycle. Therefore, in order to properly latch the output of the comparator, an

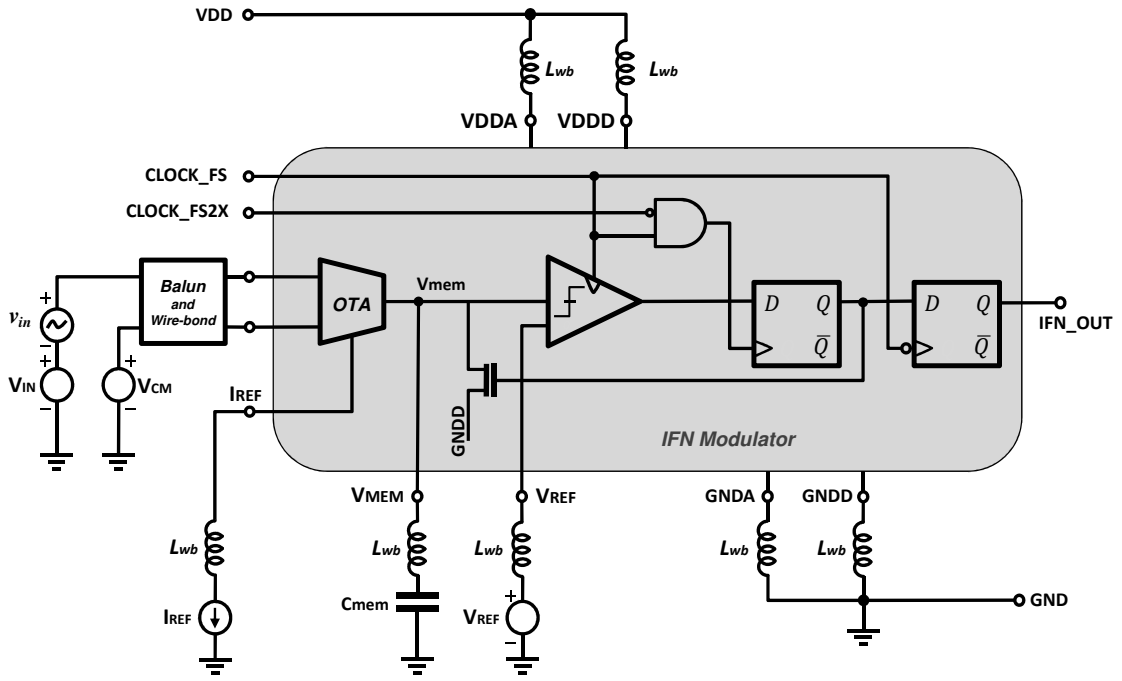


Figure 4.11: Circuitry of the integrate-and-fire modulator. L_{wb} is the wirebond inductance and the shaded rectangle is inside the chip.

auxiliary clock signal (e.g., CLOCK_FS2X) having twice the frequency of CLOCK_FS is used. Finally, using two latch stages, the output of the IFN modulator is provided.

Figure 4.12 illustrates the results for post-layout transient analysis. Applied is a sinusoid of $v_{IN} = 0.125 + 0.1 \times \sin(2\pi \times 3.3 \times 10^3\, t)$ shown in Fig. 4.12-a. It will be sampled by a clock frequency of 1 MHz while V_{REF} is set to 80 mV. Figure 4.12-b shows the V_{mem} voltage and the quality of integration. Figure 4.12-c and -d are the output bit stream of the modulator and the corresponding reconstructed signal after removing the DC component, respectively.

Calculations show that using the PSD method for ENOB estimation, the recovered sine wave exhibits ENOB value of 6.2 which is relatively less than the previously simulated result shown in Fig. 2.5 with the similar clock frequency. This SNR degradation is due to the jitter of the clock and the quantization error. The latter phenomenon is due to the fact that the comparator may compare the integration result after or before the actual analog data reaches the threshold. Post-layout simulation shows that the modulator is expected to consume roughly 8 µW power at 10 MHz clock frequency. Finally, Fig. 4.13 shows the layout of the modulator.

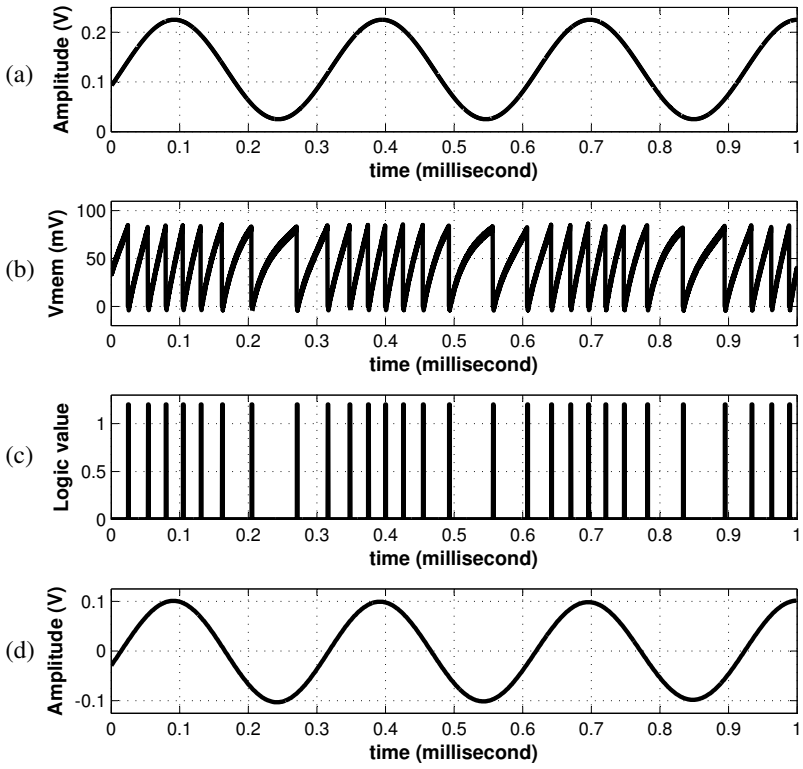


Figure 4.12: Results for Transient analysis, (a) Input sine wave $v_{IN} = 0.125 + 0.1 \times \sin(2\pi \times 3.3 \times 10^3\ t)$, (b) V_{mem}, (c) Time-encoded spikes at the output of the modulator. (d) Reconstructed sine wave after removing the DC component.

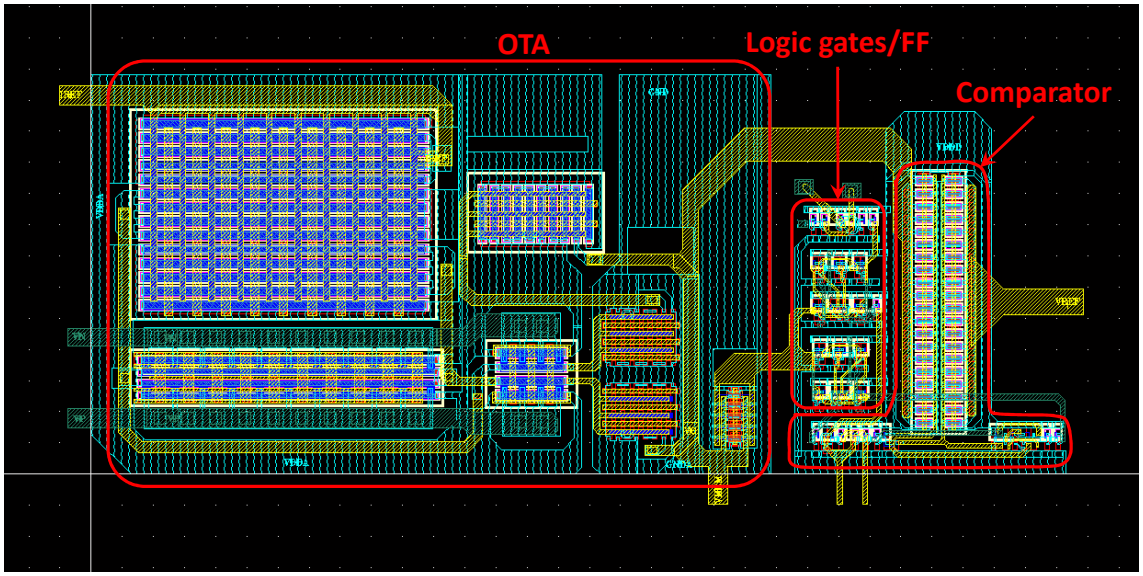


Figure 4.13: Layout of the integrate-and-fire modulator with separated analog and digital ground and supply tracks

4.2 Digital Interface

As discussed in chapters 2 and 3, it is the distance between each two consecutive IFN spikes that contains information. For that purpose, one possibility is to count the number of zeros in between them. In fact, the time-interval between spikes, arrived from the IFN modulator, must be stored in a memory. Then, using a faster clock, a command pulse must be generated such that it compresses the signal, forms a packet, and apply it to the next block of the architecture of the IRIF transmitter, which is a UWB pulse generator (PG). The created signal is encoded using the return-to-zero (RZ) coding scheme. This task will be done by a digital interface circuit that will be introduced in this subsection.

Precisely speaking, the digital interface circuit is responsible for storing the information of the received signal, into a memory for a certain time span and meanwhile reading data of the previous time span from a buffer memory. Finally, after reading data it provides the pulse generator with a command signal. The corresponding information of every time span will be packed by adding start and end marks, along with a checksum which is required in order to make sure that the received packet contains a proper number of spikes.

Figure 4.14 provides more details about the digital interface block. Furthermore, it gives a broader perspective of circuitry inside the chip and the quality that the blocks communicate with each other. Also, input/output pins are included and designated by white squares on the periphery, showing the connectivity of the chip to the outside world. The number written inside each white square is the number of wire-bonds used to connect that net to the off-chip test board. Further explanations are provided below.

One of the most important blocks of the digital interface in the *clock division unit* and the distribution of the generated clocks which are called CLOCK_FS, CLOCK_FS2X and clk100M. This unit is programmable by two control pins called COEF0 and COEF1. The selectable ratios for frequency division are summarized in TABLE 4.1. Notably, CLOCK_FS and CLOCK_FS2X are created based on a 100 MHz clock signal applied to the pin called CLK_IN. The divided signal of CLOCK_FS can be measured through a test pin called CLK_OUT (Fig. 4.14). Since, both CLOCK_FS and CLOCK_FS2X are synchronized with the main clock (clk100M), they must be carefully distributed in the chip.

The digital interface circuit utilizes a 15-bit counter so as to make time slots (T_{slot}) with duration of 3.3 ms. As shown in Fig. 4.14, the *slot counter* is triggered by the signal CLOCK_FS which is identical to f_s explained in system-level study in chapter 3. In fact, it was applied to the T/L comparator of the IFN modulator. Recalling from previous section, the comparator tracks the input data for half a cycle of the clock and latches the

Table 4.1: Provided frequencies by the clock division unit

Clock division ratio	COEF0	COEF1	CLOCK_FS
by 10	0	0	10 MHz
by 100	0	1	1 MHz
by 1000	1	0	100 kHz
by 2000	1	1	50 kHz

decided bit only during the next half. Therefore, in order to store the bit in a flip-flop another clock signal, e.g., CLOCK_FS2X, with twice the frequency of CLOCK_FS is generated and used. After all the output of the comparator is fed to the digital interface block through a couple of buffers.

The digital interface block receives a serial data either from the internal IFN modulator or an external one through the pin IFNSIG, depending on the state that the control pin, i.e., BUF_IFM_EN, holds. Basically, BUF_IFM_EN must set to "1" if the output of the internal IFN modulator is of interest, and on the other hand, when it is set to "0" IFNSIG pin is disconnected from the internal modulator and can be used as a port to apply the serial data generated by an off-chip modulator. The off-chip modulator, also, can use the CLOCK_FS signal through the CLK_OUT pin to be synchronized with the rest of the circuit.

A *write control unit* is supposed to count the number of zeros in between every two consecutive IFN spikes and save it in a memory called $Mem.\ A$. When the slot counter gives an overflow, three actions will happen immediately. First, the slot counter resets to zero; this means that it immediately starts the next time span. Second, another memory called $Mem.\ B$ begins to record the information of the next 3.3 ms time span. In fact the role of memories are swapped and the latter acts as a buffer in order not to lose any data (see Fig. 4.14). Third, the data stored in the $Mem.\ A$ will be read at the rate of the high speed clock, e.g., 100 MHz, which is identical to the clock f_r in Fig. 3.2.

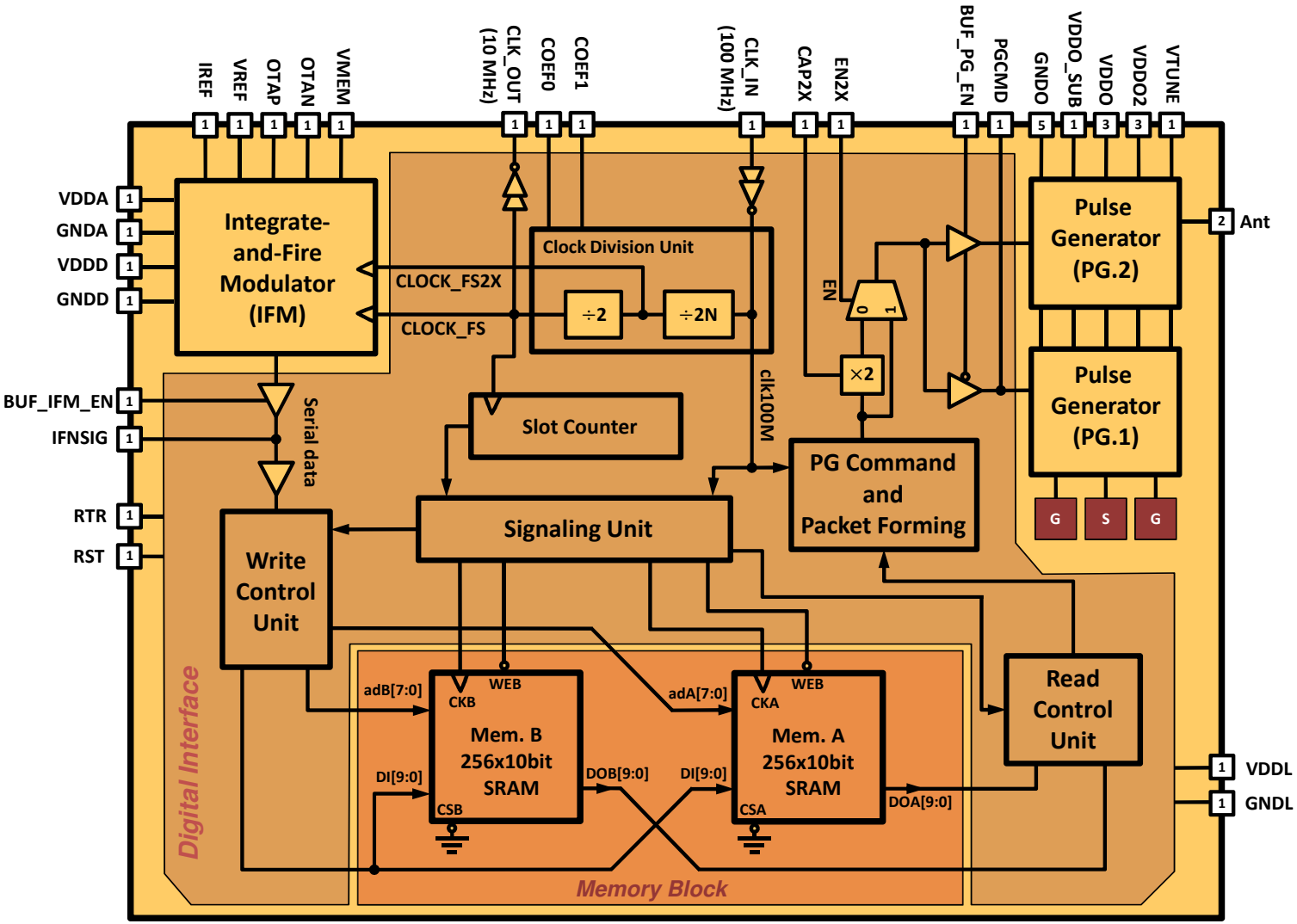


Figure 4.14: An overall view of the designed chip with concentration on details of digital interface circuit including all input and output pins. The numbers written on the input/output pins are the number of wire-bonds that connect the corresponding pin to the outside world.

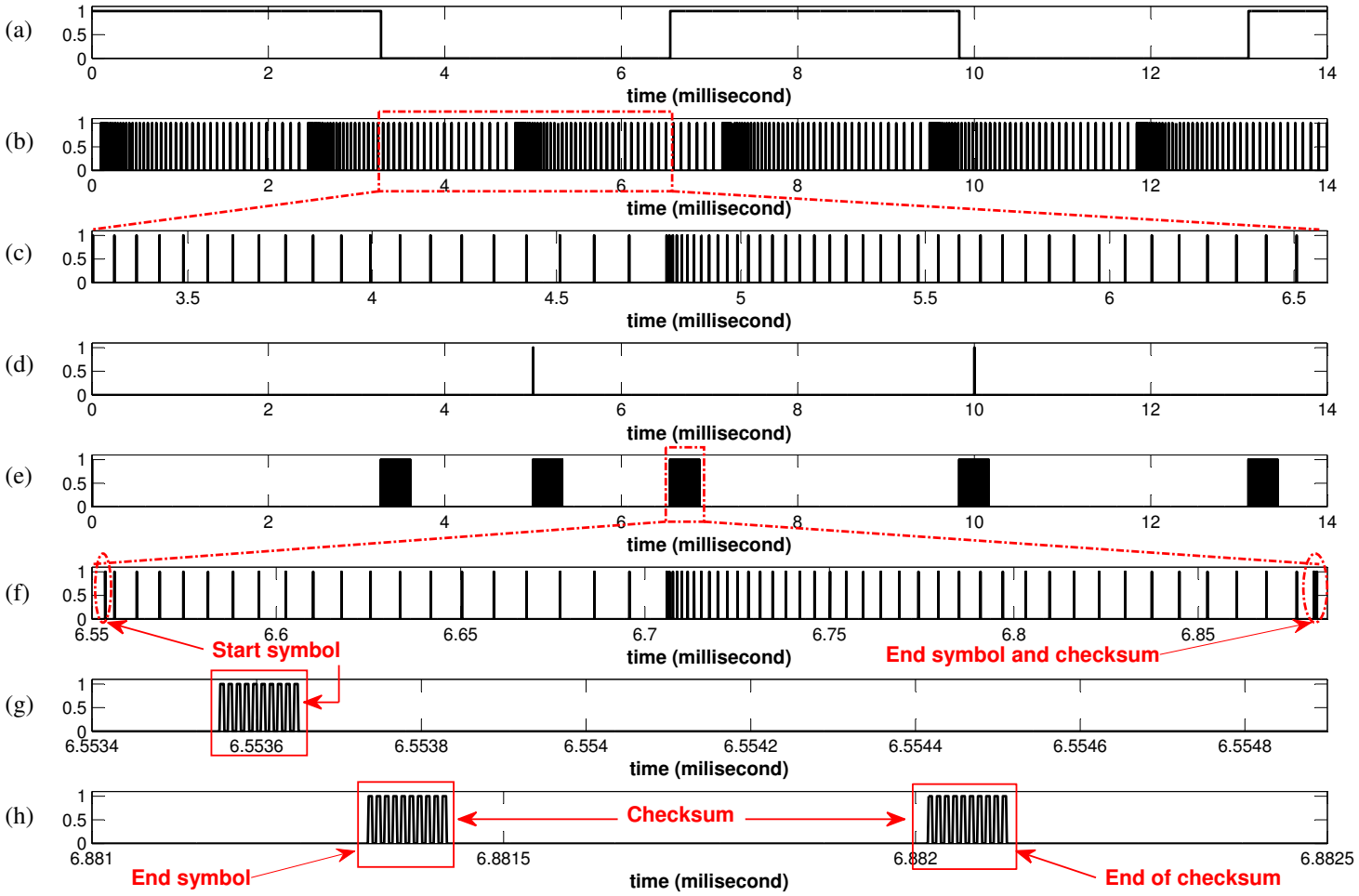


Figure 4.15: A few important signals of the digital controller. (a) command for memory selection, (b) a typical input serial data received from the IFN modulator, (c) a zoomed part of data in a time slot, (d) repeat transfer request (RTR), (e) output signal of the digital interface circuit which is the command for UWB pulse generator, (f) transmission of the portion of the data, shown in (c), while it is embedded in a packet form with start and end symbol and a checksum, (g) start-symbol is 10 consecutive pulses, (h) end-symbol and end-of-checksum are 10 consecutive pulses while the checksum is a silence distance between them.

Reading from the proper memory will be carried out by a *read control unit*. In fact, this unit synthesizes the bit stream and applies it to the next block, called *PG command and Packet Forming* which is responsible for packet forming. Actually, it adds start and end symbols, and a checksum to the raw data. Since the read operation is performed by a faster clock, this unit will compress data in time as well. As explained in section 3.3, start and end symbols consist of ten consecutive clock pulses synchronized with CLK_IN (100 MHz). The checksum is a silent time interval that comes after the end-symbol, representing the number of IFN spikes in the packet. The checksum itself ends up with a similar symbol as that of start and end packet. All the controlling clocks and settings for read and write on/from memory are generated by a *signaling unit* (Fig. 4.14). Furthermore, the digital interface circuit works synchronously with other blocks after receiving a reset signal which is created by a rise edge trigger at the pin RST [1]. That is to say, an external reset circuit is required on the test board.

Since within almost nine-tenth of T_{slot} no data will be transmitted, this interval can be reserved for any error request. The pin called RTR[2] is supposed to receive a rise edge trigger, in case any packet repetition is required. Also, this interval can be used to implement time division multiple access technique and serve other sources of sensors in case of a multiplexed system. Figure 4.15 shows a number of important signals of the digital interface circuit. It represents signaling information and the quality that the input serial data is stored, compressed and packed. Synchronized with the reference clocks, the signal shown in Fig. 4.15-a is a pulse that toggles every $T_{slot} = 3.3\,\text{ms}$, and is responsible to swap the read and write process in each memory. At every rising and falling edge of this signal, the stored data will be compressed and sent. Here, in order to perform a mixed-signal verification, an artificial signal (Fig. 4.15-b) is generated to represent the serial input data that comes from the IFN modulator. Figure 4.15-c is the magnified view of a part stored in $Mem.\ B$. This bunch of data will be sent at the end of the time slot and it can be repeated within the same time slot if an RTR request arrives. An example of an RTR signal is shown in Fig. 4.15-d; the first request happens in the free interval after sending the main packet, whereas the second one coincides with transmission of the main packet and has been rejected. Moreover, Fig. 4.15-e illustrates the output of the digital interface module. This signal is made by *PG command and Packet Forming* block after the bit stream data is embedded inside a packet. Figure 4.15-f is the compressed version of Fig. 4.15-c, while it is inserted in a packet that includes start and end markers and a checksum. Figure 4.15-(g,h) illustrate the start and end symbols along with the checksum and the symbol for end-of-checksum. The design compiler reports a power consumption

[1] Input reset signal

[2] repeat transfer request, it is more discussed in chapter 3.3.

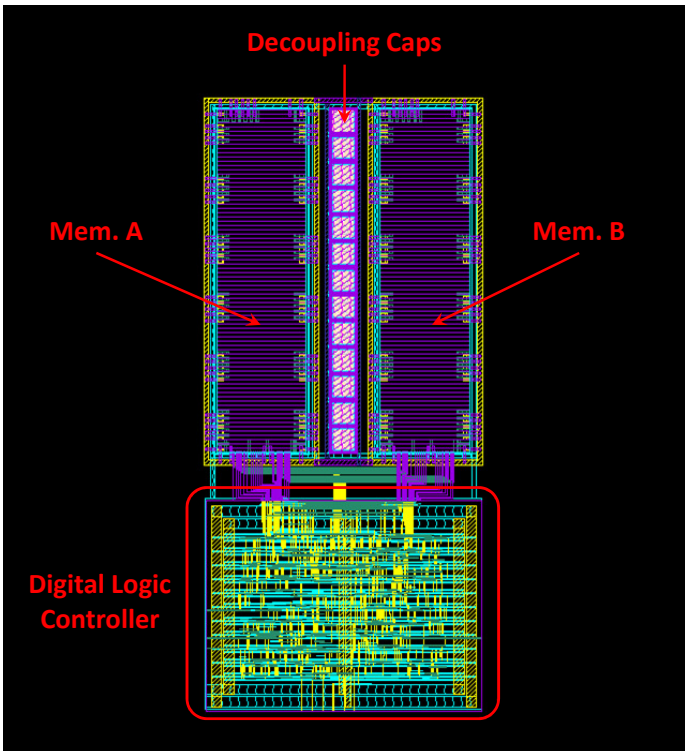


Figure 4.16: Layout of the digital interface circuit

of 3.3 µW for the digital circuits, excluding memories. Finally, Fig. 4.16 illustrates the layout of the digital controller.

4.3 UWB Pulse Generator (PG)

As demonstrated earlier in Fig. 4.14, the output signal of the digital interface block will be applied to a PG circuit. In fact, it creates a UWB pulse whenever it receives a rise edge of the command pulse. The rise edge will trigger a glitch generator circuit whereby the PG builds a UWB impulse which will be applied to an antenna.

As illustrated in Fig. 4.17, a lossy LC tank triggered by a current impulse shows a decaying oscillatory response. In fact, the resistance of the capacitor and the inductor converts into heat some of the energy that reciprocates between them. This concept can be used for designing a very low power PG, mainly because there are not that many active components in such a circuit. The UWB PG is supposed to drive a 50 Ω antenna, therefore in the RLC network the R_{Loss} can be replaced by $R_{Ant} = 50\Omega$. In the PSD of the output signal, the central frequency will be at $\omega_o = 1/\sqrt{LC}$, the bandwidth is determined by time duration that the oscillation decays. In fact, the faster decay, the wider bandwidth will be obtained.

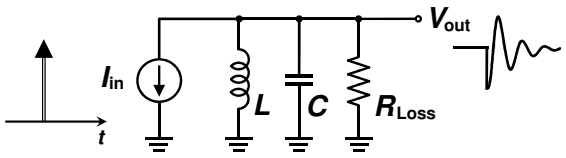


Figure 4.17: Decaying oscillatory behavior of a lossy LC tank triggered by a current impulse [2].

As can be seen in Fig. 4.14, two identical PG circuits are placed on the die. In fact, PG.1 which is illustrated in Fig. 4.18, will be used for probe testing and characterizing the design per se, and PG.2 shown in Fig. 4.19, will be connected to a printed circuit board (PCB) through wire-bonds and will provide the antenna with the actual transmitted signal. In PG circuits, an inductor of 1.68 nH and a capacitor of 250 fF are chosen for the LC tank. It is expected that due to parasitics, the central oscillation frequency shifts to the lower values. To run an accurate simulation, this issue must be taken into consideration, thus, comparatively smaller inductance and capacitance for L and C are opted. The main resonant frequency will be around 5.2 GHz. The LC tank will be triggered by a glitch signal applied to the gate of a MOSFET. When the transistor is "off" the LC tank is charged and when the glitch is applied to the MOSFET it becomes "on" and discharges the network. The glitch has a very short duration in the range of a few tens of pico second and within this short time the circuit draws 6.6 mA from the supply. Thus, the network generates fast oscillations at the output while it is charging back. Furthermore, choosing a proper width for the MOSFET is challenging. On one hand, the MOSFET must show a very small channel resistance, therefore a wise choice is to increase its width. On the other hand, widening the transistor, increases the parasitics. After all, the device is relatively large because small resistance of it is of high interest. This means that the glitch generator circuit must handle a large capacitive load. An obvious choice is to use an inverter chain, however, in order to decrease the occupied area on the die, a single circuit has been designed such that it can function as both glitch generator and inverter chain. In fact, the logic stage circuits in glitch generator are appropriately weighted and as a result they can drive a large capacitive load, i.e., the switching MOSFET. Also, the duration of the glitch is tunable, and to do so, a control knob called V_{Tune} in Fig. 4.18, is utilized in the inverter chain.

Additionally, a filter is required for the rejection of GPS and satellite band. For PG.1 circuit, the filter is implemented by an on-chip series LC network with an inductance of 1.51 nH and capacitance of 9.54 pF. Notably, an RF probe will act as an RLC load, thus its model must be included as long as time domain measurement is of interest and calibration is not possible. The width of glitches and peak current drawn from supply for various process corners are summarized in TABLE 4.2. Corner analysis results for

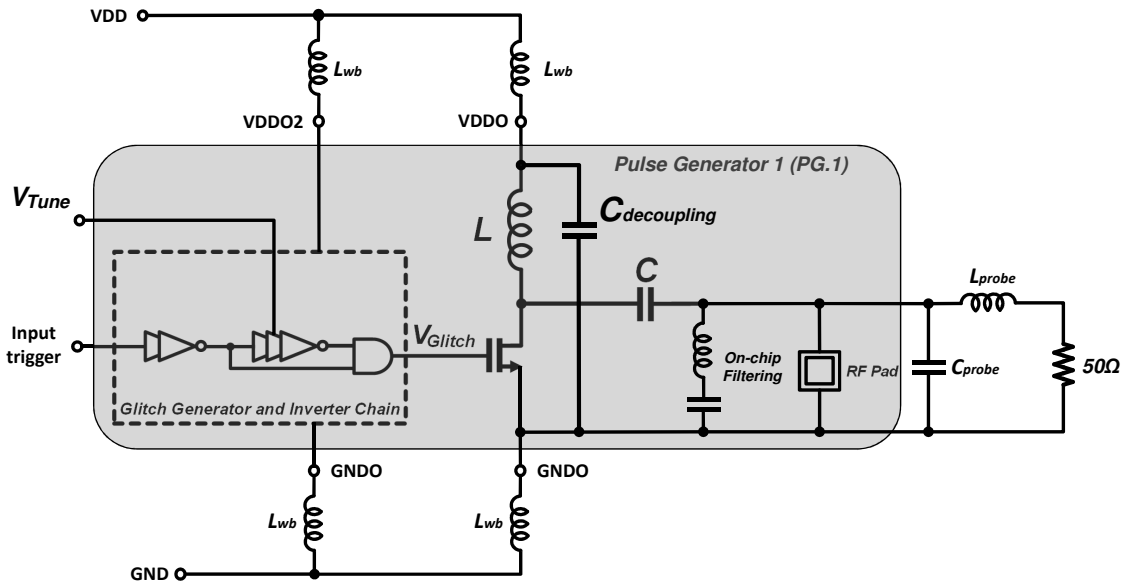


Figure 4.18: Pulse generator (PG) circuit for probe testing.

glitch, UWB output pulse and its PSD for the variations of the MOSFETs are shown in Fig. 4.20 and those of inductor and capacitors are illustrated in Fig. 4.21. The PG circuits build UWB impulses with amplitudes of up to 1.37 V within the duration of roughly 1 ns. Simulations show a -10 dB-bandwidth of approximately 4 GHz and power consumption of 5.64 pJ per pulse/bit. Layout of the designed PG circuit is also illustrated in Fig. 4.22.

As mentioned above, in order to connect the chip to an antenna, PG.2 circuit must be fed by the output signal of the digital interface circuit. As shown in Fig. 4.14, two three-state buffers, controlled by the pin BUF_PG_EN, determine which pulse generator circuit receives the command signal from the logic interface. In fact, if this pin is set to "0" the command signal will reach PG.1, while in case of "1", the upper buffer handles the command signal to PG.2 circuit. In other words, when PG.1 is triggered, PG.2 does not see any input pulse and vice versa. The output signal of PG.2 is reach a test PCB through two wire-bonds and thereafter it will face a transmission line. Besides, for PG.2 the band-rejection filter is off-chip due to lack of enough space on the die. Therefore, the output signal characteristics will be degraded or changed because of the loss related to all the components in the path to the antenna connector. All in all, the design of the transmission line must be done carefully, which will be discussed later in the section 4.4.

Table 4.2: Process corners results for glitch duration and peak current drawn from VDD

-	ff	fnsp	tt	snfp	ss
T_{Glitch}	48 ps	57 ps	60 ps	67 ps	83 ps
Idd_{peak}	6.5 mA	6.8 mA	6.6 mA	6.6 mA	7.2 mA

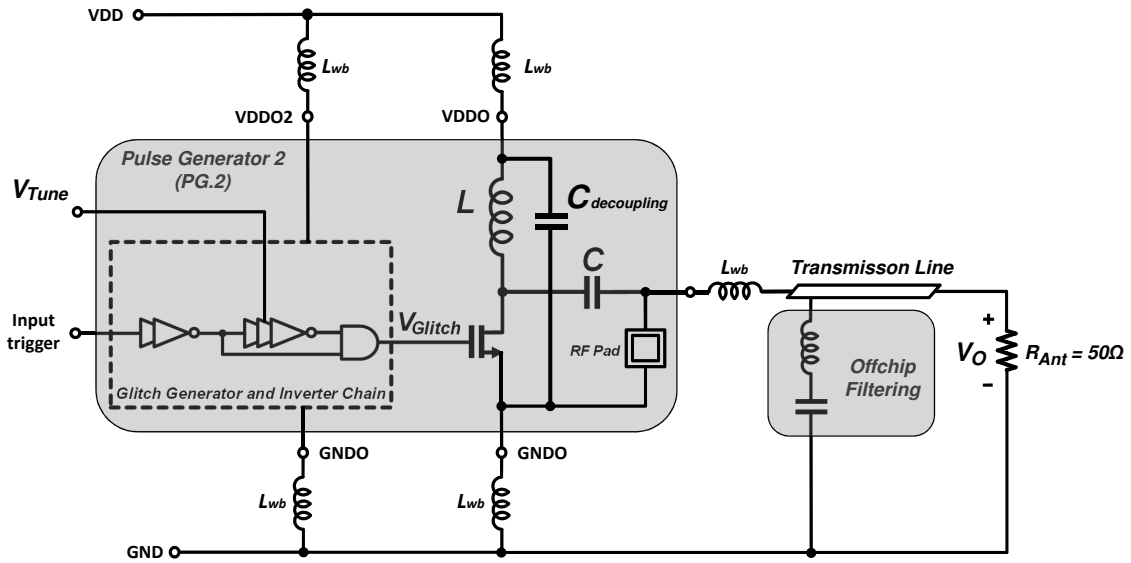


Figure 4.19: Pulse generator (PG) circuit to be connected to antenna.

The overall layout of the system is shown in Fig. 4.23. In order to avoid the substrate noise, analog, digital and RF blocks are shielded with guard rings connected to global ground. The grounds and power supplies for all three types of circuits (e.g., analog, digital and RF) are isolated by using different nets and tracks, which are connected to the PCB test board through different pins and wire-bonds. Each pin is protected by a simple diode-based electro-static discharge (ESD) circuit to provide some protection for the internal MOSFET gates. Also, circuits are placed far enough to decrease the impact of the interference noise. The critical tracks, which are supposed to carry high frequency signals or clocks, were carefully simulated and/or buffered. The 100 MHz clock is buffered right after it enters the chip and the associated track is shielded. Last but not the least, enough amount of decoupling capacitor are embedded inside the chip so as to make fixed and clean supplies for all the blocks.

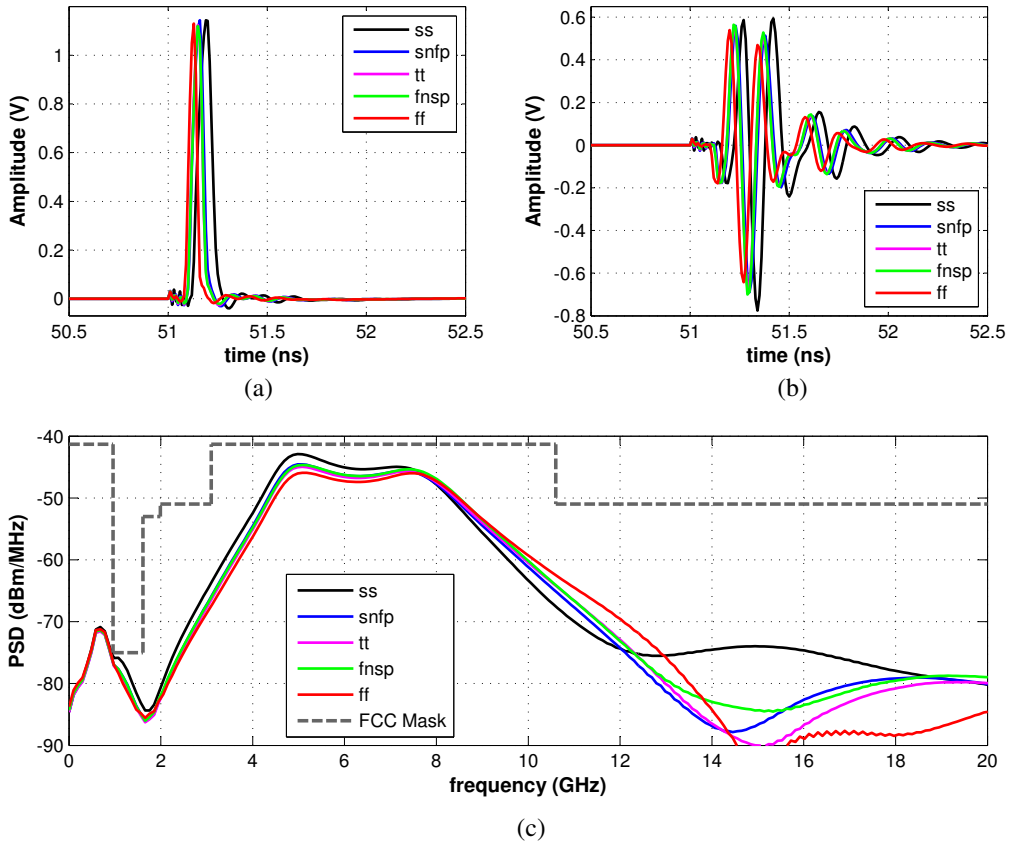


Figure 4.20: Corner analysis for MOSFETs in PG: (a) glitches (b) UWB impulses, (c) PSD corners

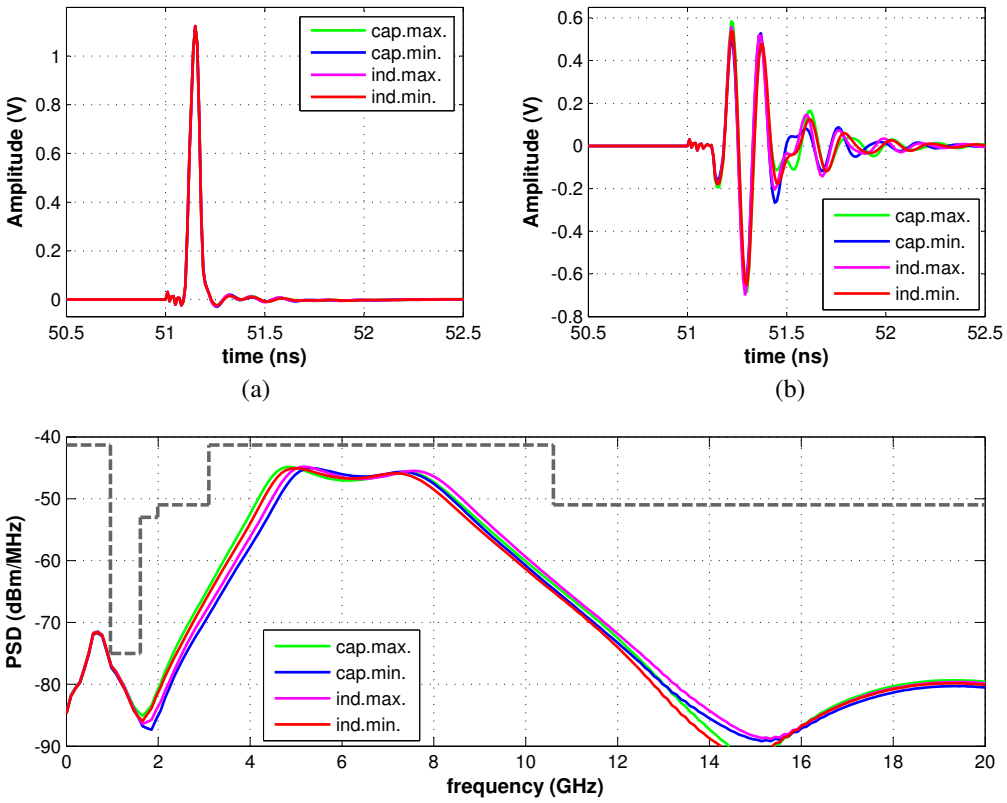


Figure 4.21: Corner analysis for inductors and capacitors in PG: (a) glitches (b) UWB impulses, (c) PSD corners

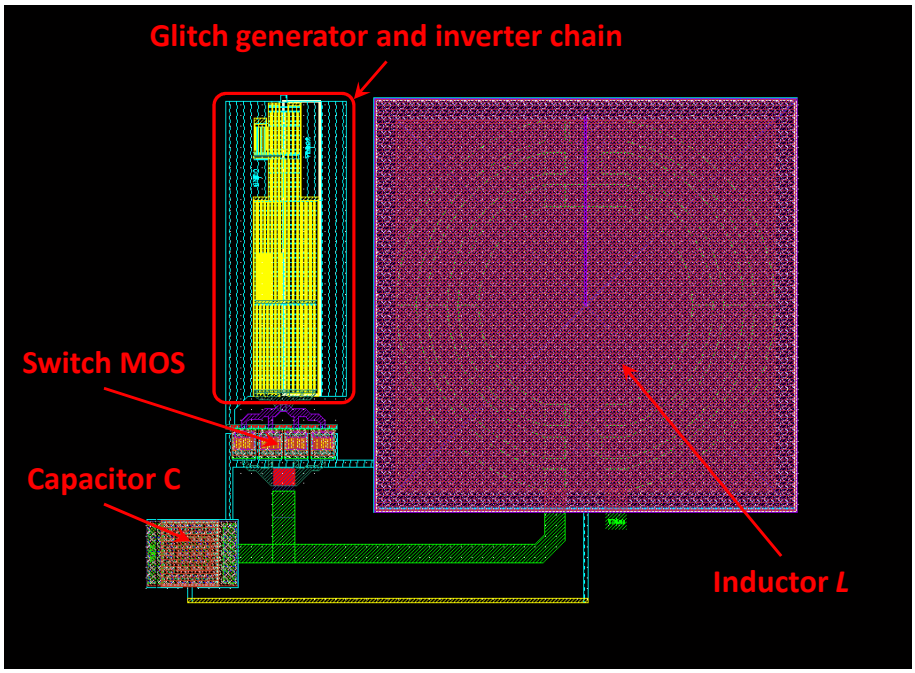


Figure 4.22: Layout of the pulse generator circuit

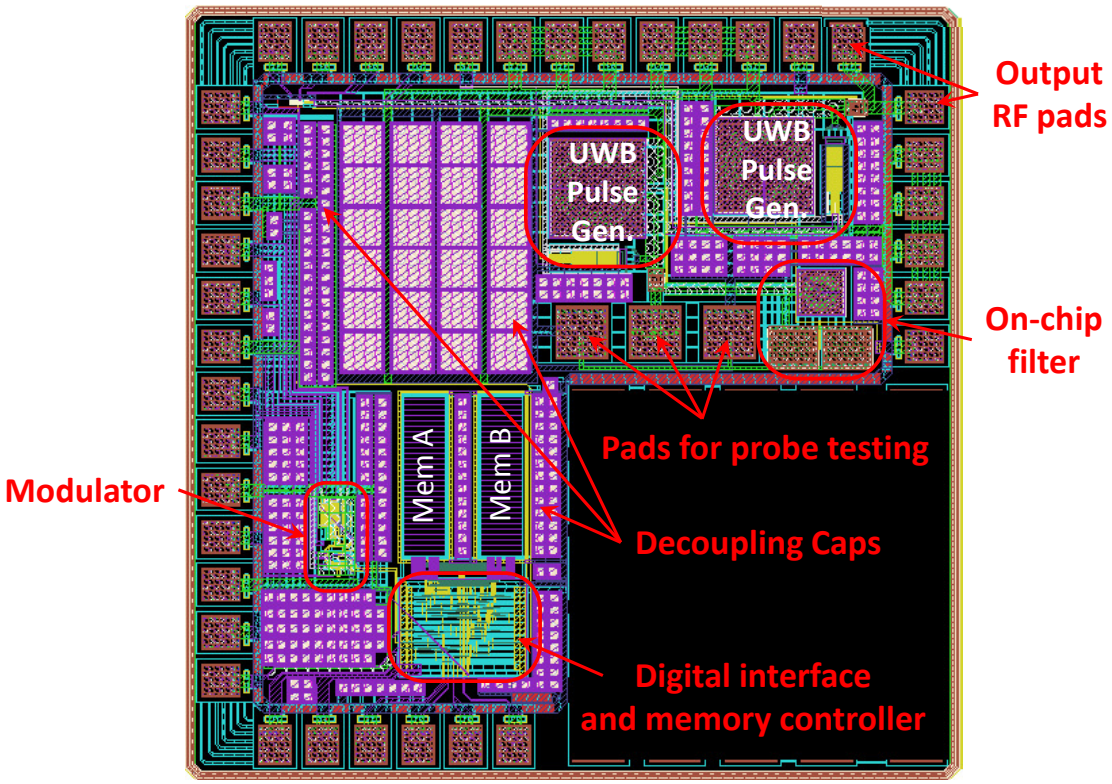


Figure 4.23: Layout of the full transmitter system

4.4 PCB Design for UWB Signal

As mentioned earlier, the output of PG.2 is connected through two wire-bonds to a PCB that is needed be designed for chip-on-board (CoB) measurement purposes. On the PCB, the track that is supposed to deliver the UWB impulses to the antenna must be considered as a transmission line (TL). Also, because of limited chip area available on the die, the GPS and satellite band-rejection filter has to be placed off-chip. Therefore, the transmission line on the PCB should be designed carefully such that the loss effects will be minimized.

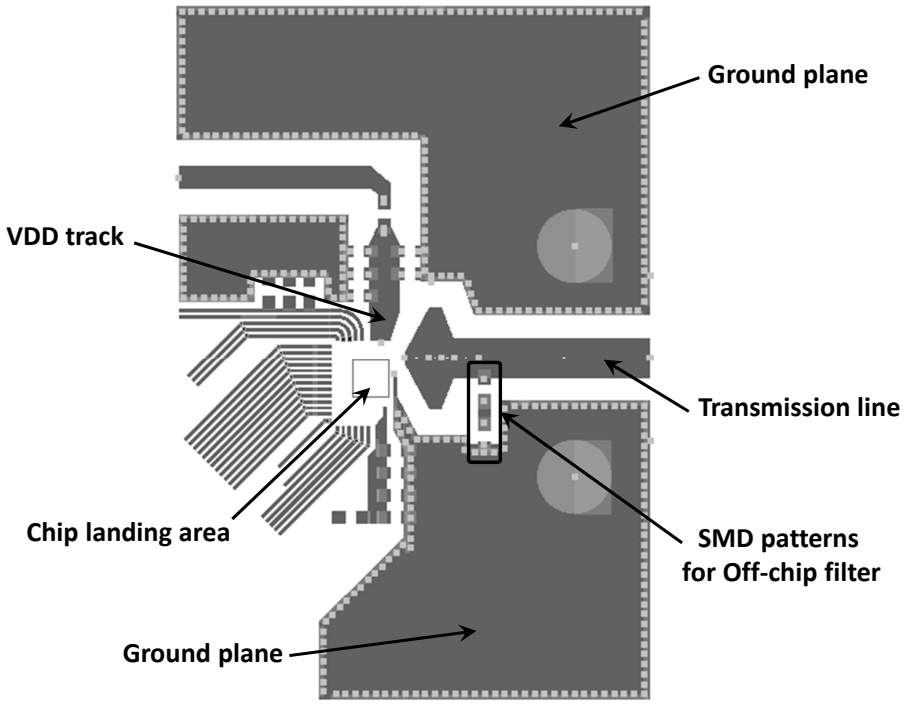


Figure 4.24: PCB of the RF section

The claimed TL is presented in Fig. 4.24. Momentum simulation in ADS [3] simulator shows that the TL provides a good matching for a wide range of UWB from 2.7 GHz to 8.4 GHz, which is illustrated in Fig. 4.25. Each wire-bond has been modeled by a π network including 1 nH inductance containing intrinsic resistance of 1 Ω along with two parasitic capacitances of 150 fF. The band-rejection LC filter is composed of a 8.2 nH inductor and a 1.5 pF capacitor and in the simulation their real models are included. A transient analysis using Cadence-ADS co-simulation is performed, while the Calibre-view of PG circuit and momentum results of the PCB are included. Illustrated in Fig. 4.26, co-simulation results show that the pulse amplitude at the end of TL is 900 mV and

[3] Advanced Design System

peak power -43.5 dBm/MHz at 5.3 GHz. The PSD in Fig. 4.26-b shows that the -10 dB bandwidth of 2 GHz. As mentioned above, due to the lack of space on the die, the band-rejection filter must be placed off-chip. This makes the design of the TL difficult. Thus, the TL is not optimized for the whole UWB range, though the transmitter still enjoys a 2 GHz bandwidth.

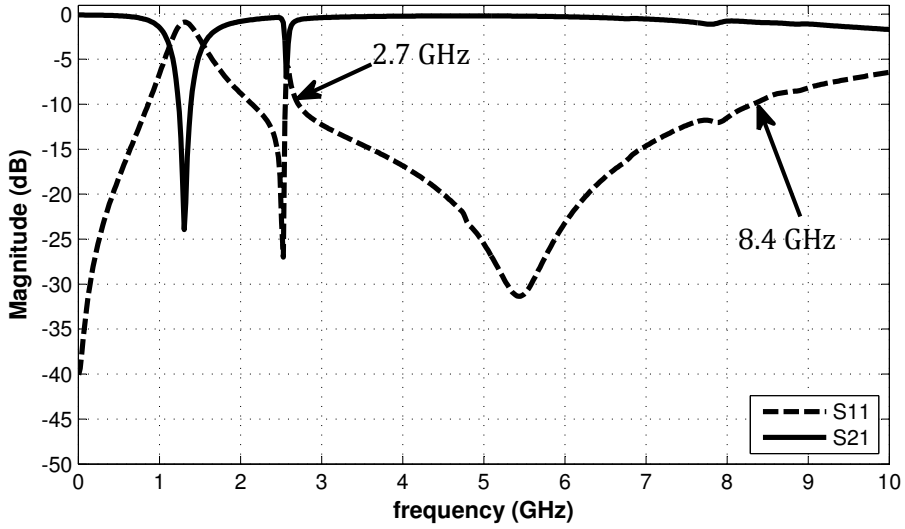
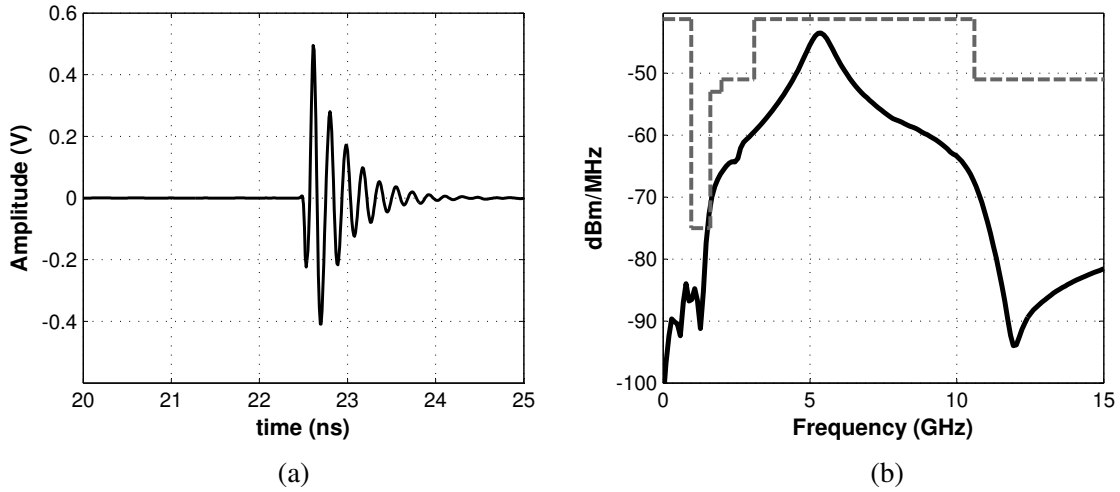


Figure 4.25: Momentum results for S parameters of the transmission line including LC network filter and wire bond model



(a) (b)

Figure 4.26: (a) Output signal at the end of transmission line when $V_{Tune} = 650\,\text{mV}$. (b) PSD of the output signal at PRF of 100 MHz.

4.5 Conclusion

CMOS implementation of the IRIF transmitter is explained in detail. The analogue and RF blocks, including the modulator and the pulse generator, are simulated by Spectre in Cadence; 130nm technology node and 1.2 V supply voltage have been used. The digital interface circuit is simulated using Verilog RTL coding, Synopsys' design compiler for synthesis and post-synthesis simulations, and it is implemented by Faraday's 130nm standard cells and memory IPs. Furthermore, SOC Encounter have been used for physical implementation. Analog simulations have been done carefully by including imposed parasitics models, e.g., PADs and ESD protection circuits and wire-bond models. After all, for the purpose of chip-on-board measurement, a PCB is designed and its high frequency response is investigated and characterized.

Chapter 5

Measurement Results and Discussion

5.1 Chip Measurements

The proposed transmitter is implemented in 0.13 µm CMOS process with 1.2 V supply voltage. The chip micro-photograph is shown in Fig. 5.1. A PCB is designed to set the bias and tunning voltages and currents, preparing the required input differential signals, and probing purposes; the board is presented in Fig. 5.2. Different circuits on the PCB are sectioned and isolated from each other. As explained in section 4.4, the RF part of the PCB is characterized by a Co-Sim technique using ADS and post-layout simulation results. The measurement setup is shown in Fig. 5.3. A sinusoidal function of $v_{IN} = 0.150 + 0.1 \times \sin(2\pi \times 1000\, t)$ is applied as the input low-frequency signal by a Tektronix AFG3021B function generator and can be seen in Fig. 5.4.

A clock signal with 100 MHz frequency is applied to the pin CLK_IN by a Keysight 33600A function generator. Inside the chip, this clock divided by ten and measured at the pin CLOCK_FS. The modulator works with this clock rate, e.g., 10 MHz. It can be observed that the time-slot (T_{slot}), the packet length, and the number of sinusoidal cycles within the packet has some formulated dependency on clock rate. These dependencies are more illustrated in TABLE 5.1 for various input clocks. Figure 5.5 shows the conversion

Table 5.1: Clock dependent parameters represented for the case of 1 kHz input sinusoidal function and clock division ratio of 10

CLK_IN	CLOCK_FS	Time-slot	Periods within a packet	Packet length
100 MHz	10 MHz	3.3 ms	3.3 cycles	0.33 ms
50 MHz	5 MHz	6.6 ms	6.6 cycles	0.66 ms
10 MHz	1 MHz	33 ms	33 cycles	3.3 ms
5 MHz	500 kHz	66 ms	66 cycles	6.6 ms
1 MHz	100 kHz	330 ms	330 cycles	33 ms

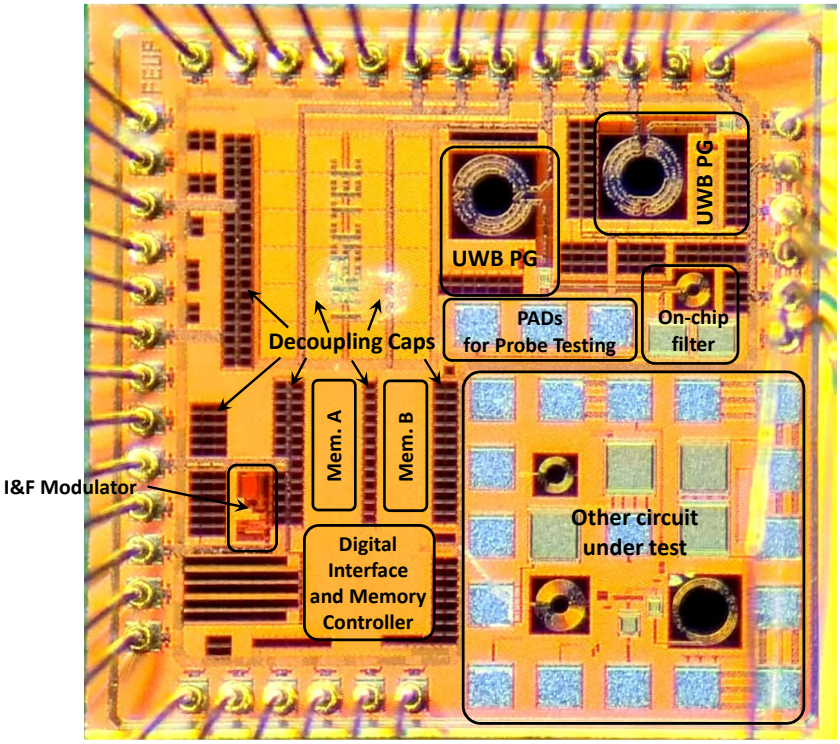


Figure 5.1: Micro-photograph of the die

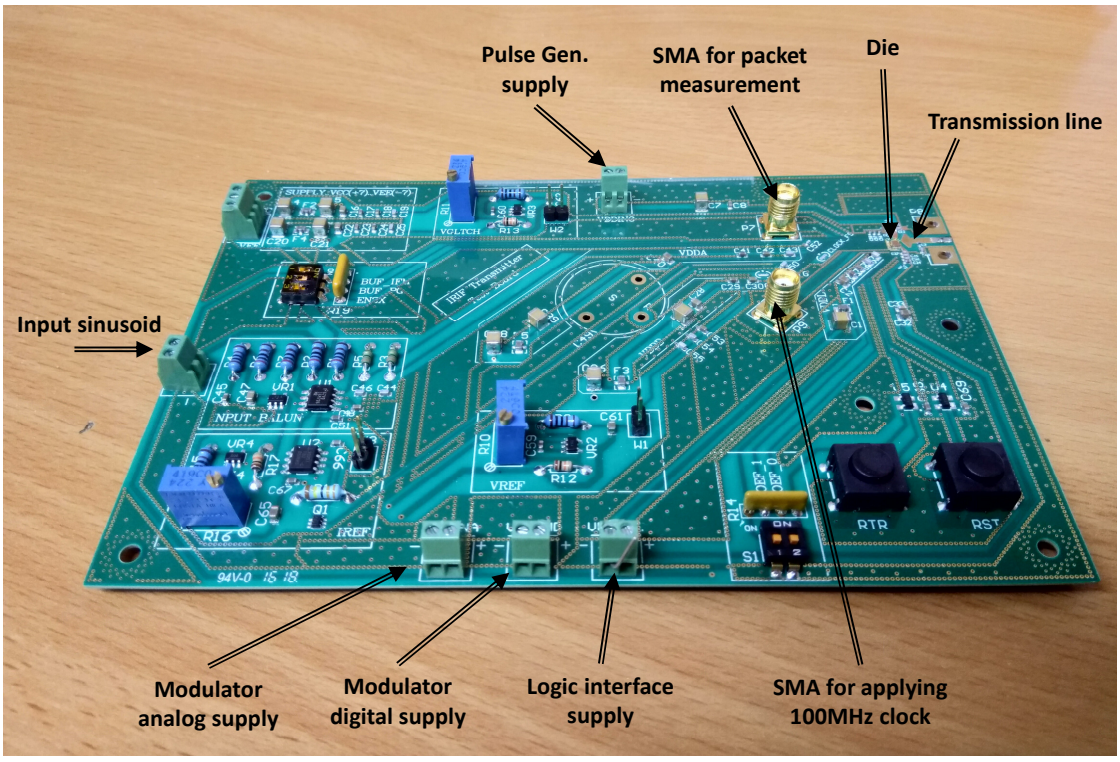


Figure 5.2: PCB for chip-on-board (CoB) measurement

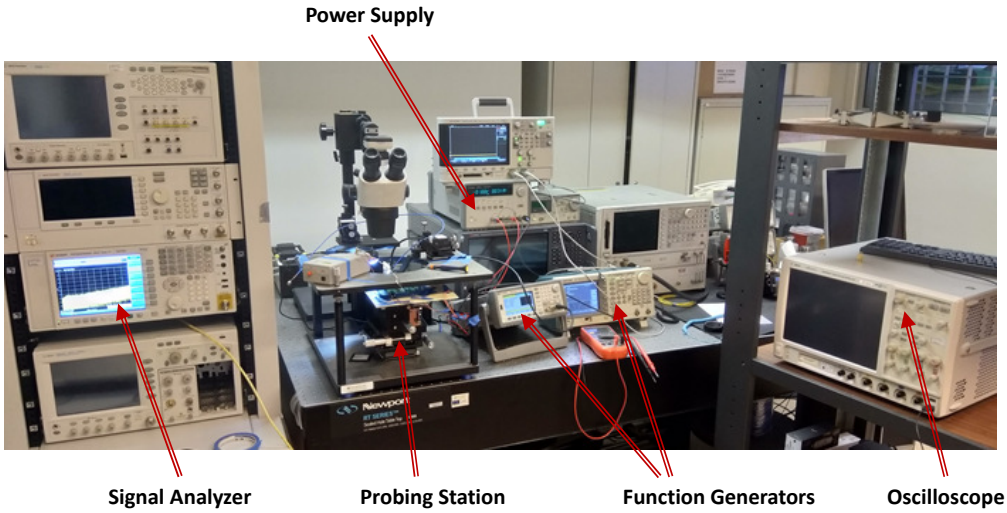


Figure 5.3: Measurement setup

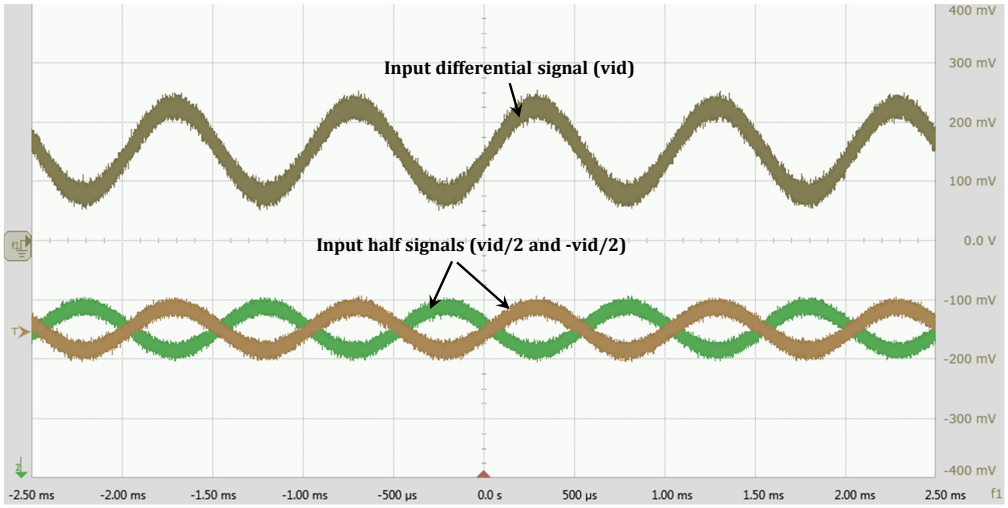


Figure 5.4: Input differential sinusoidal function

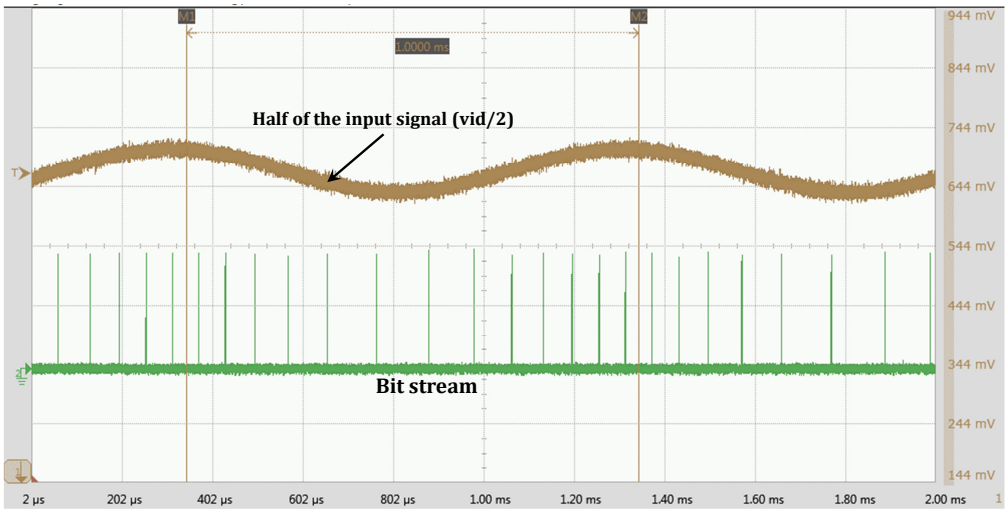


Figure 5.5: Conversion by the IFN modulator

quality of the input sine wave to a bitstream by the IFN modulator. Using 100 MHz clock, the recording time slot has the duration of 3.3 ms and after compression every packet will have 0.33 ms length.

Figure 5.6 shows packets of data measured at the pin called PGCMD which were already presented in Fig. 4.14 and explained in section 4.2. The reason of not having pulses with 1.2 V amplitude is the loading effect by the probe of the oscilloscope and lack of having a good driver inside the chip. It should be noted that due to this effect, for the input, end, and checksum symbols, the charge will accumulate more on the input capacitor of the probe. Thus, the amplitude of these markers is larger. Figure 5.7 illustrates a zoomed view of a packet.

Using a Keysight oscilloscope having 6 GHz cut-off frequency and 20 GS/s rate, the output UWB packets, generated by PG.2 (Fig. 4.14), are measured and shown in Fig. 5.8. The packets repeat periodically every 3.3 ms and have duration of 330 µs as expected from simulation results. Figure 5.9 shows only one packet of the transmitted data. It can be seen that roughly 3.3 cycles of the input sinusoid has been packed and transmitted. Due to utilization of two memories (one as a buffer) no data will be missed and it will be continued in the next packet. Figure 5.10 shows the peak-to-peak voltage amplitude of UWB impulse is around 400 mV; although the real amplitude is expected to be larger because of the small bandwidth of the measurement equipment. In fact, not all of the power of the transmitted pulse is measured and the oscilloscope filters the signal until 6 GHz. As mentioned earlier in section 3.3, only one UWB impulse represents a bit of "1" and then to build the mark symbols ten consecutive impulses are used and synchronized with the input clock. Furthermore, start and end symbols along with the checksum are demonstrated in Fig. 5.11 and 5.12, respectively.

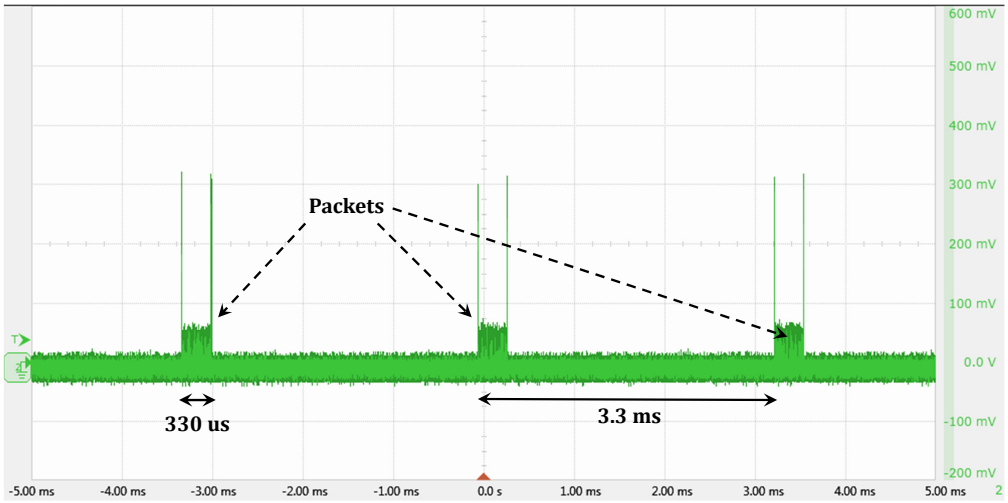


Figure 5.6: Output packet of the digital interface which is the command for pulse generator circuit

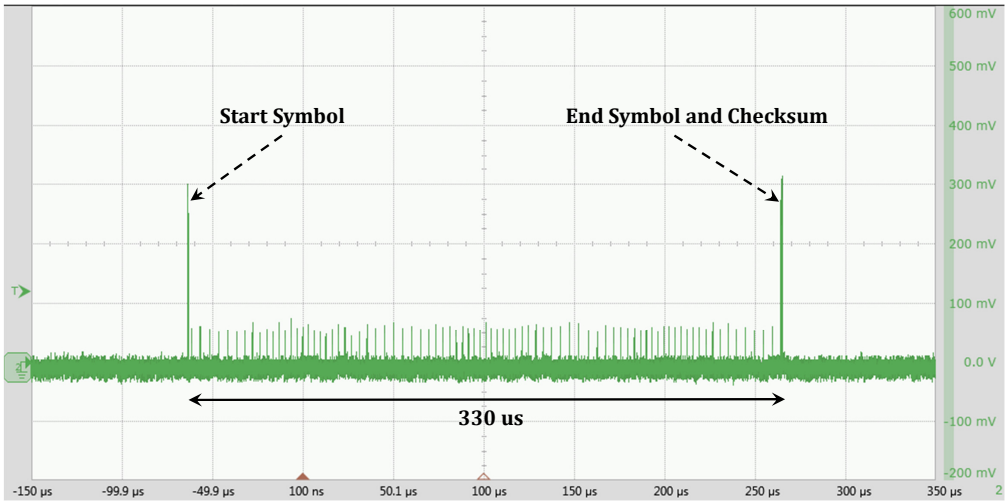


Figure 5.7: A cloder look to the output packet of the digital interface

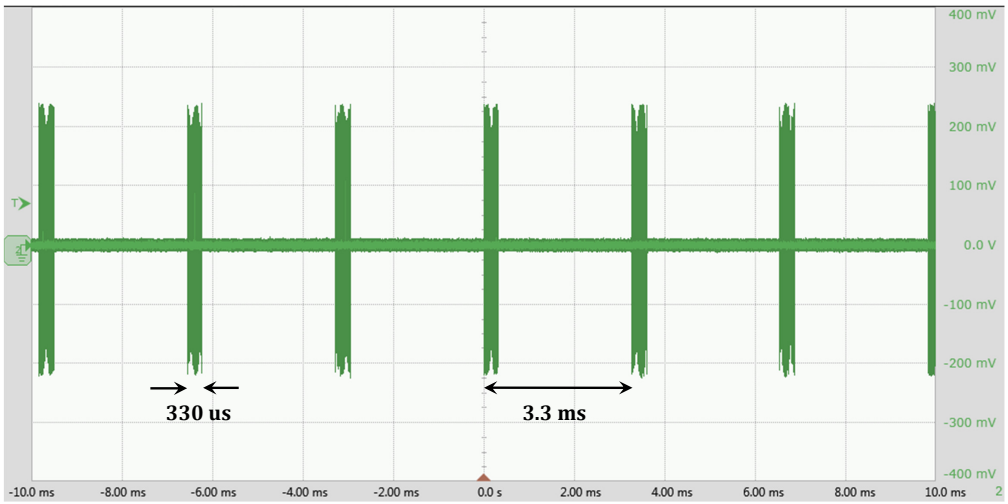


Figure 5.8: UWB packets

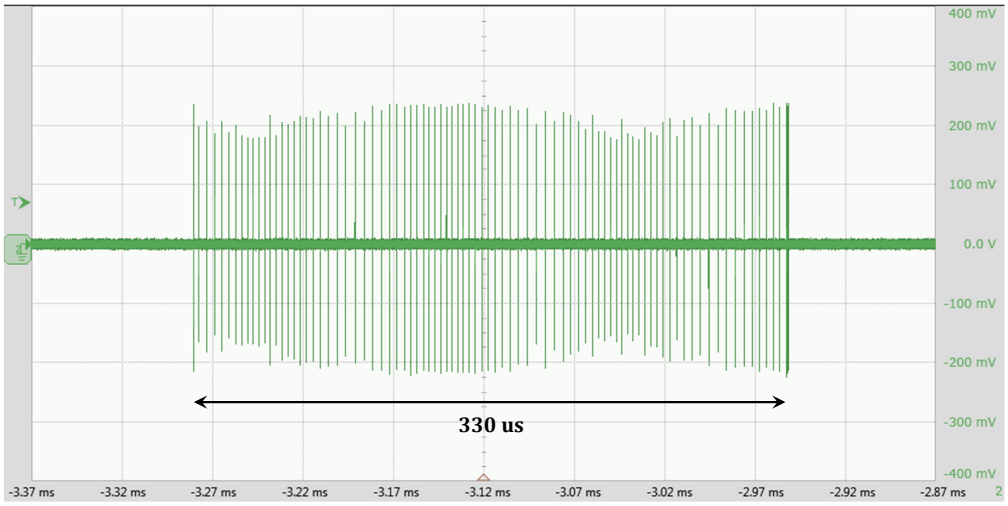


Figure 5.9: A single packet of data transmitted by UWB impulses

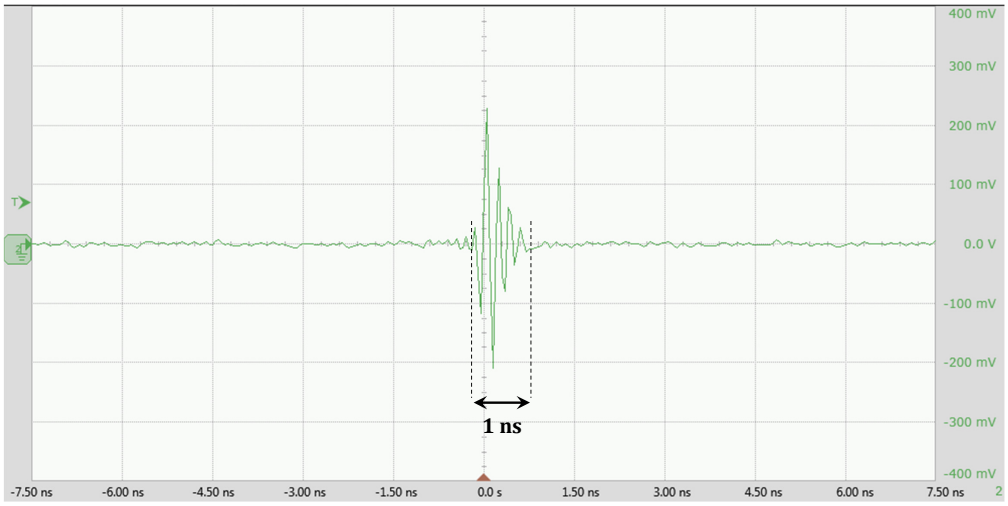


Figure 5.10: A UWB impulse in time domain

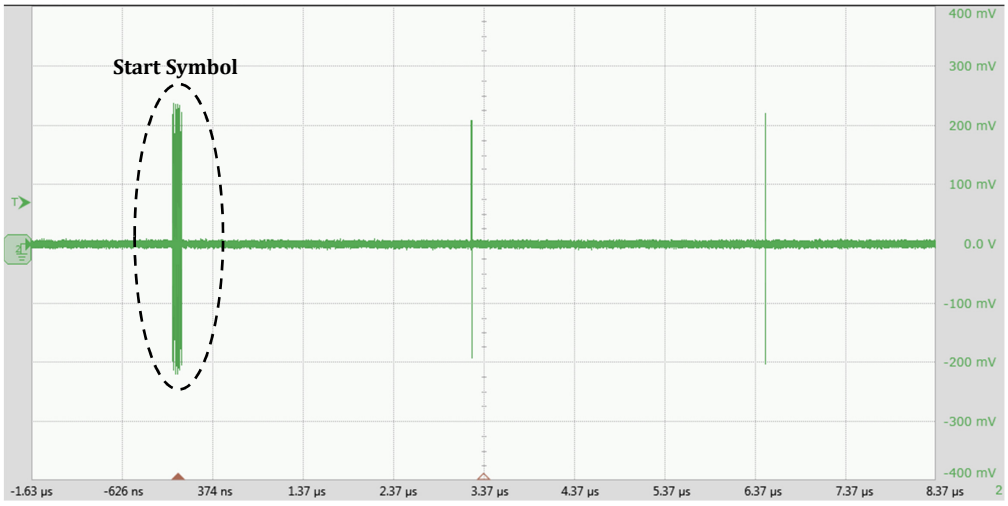


Figure 5.11: Start Symbol

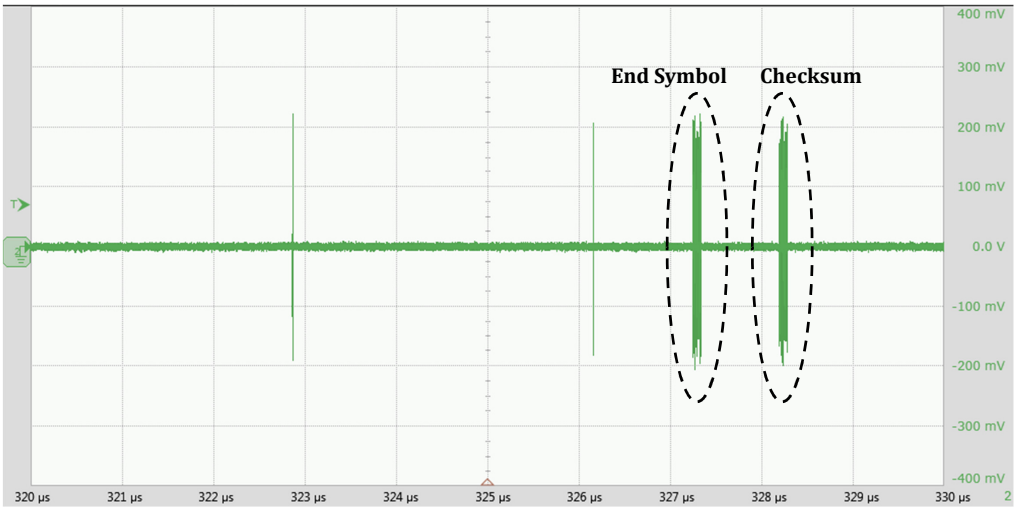


Figure 5.12: End Symbol and checksum

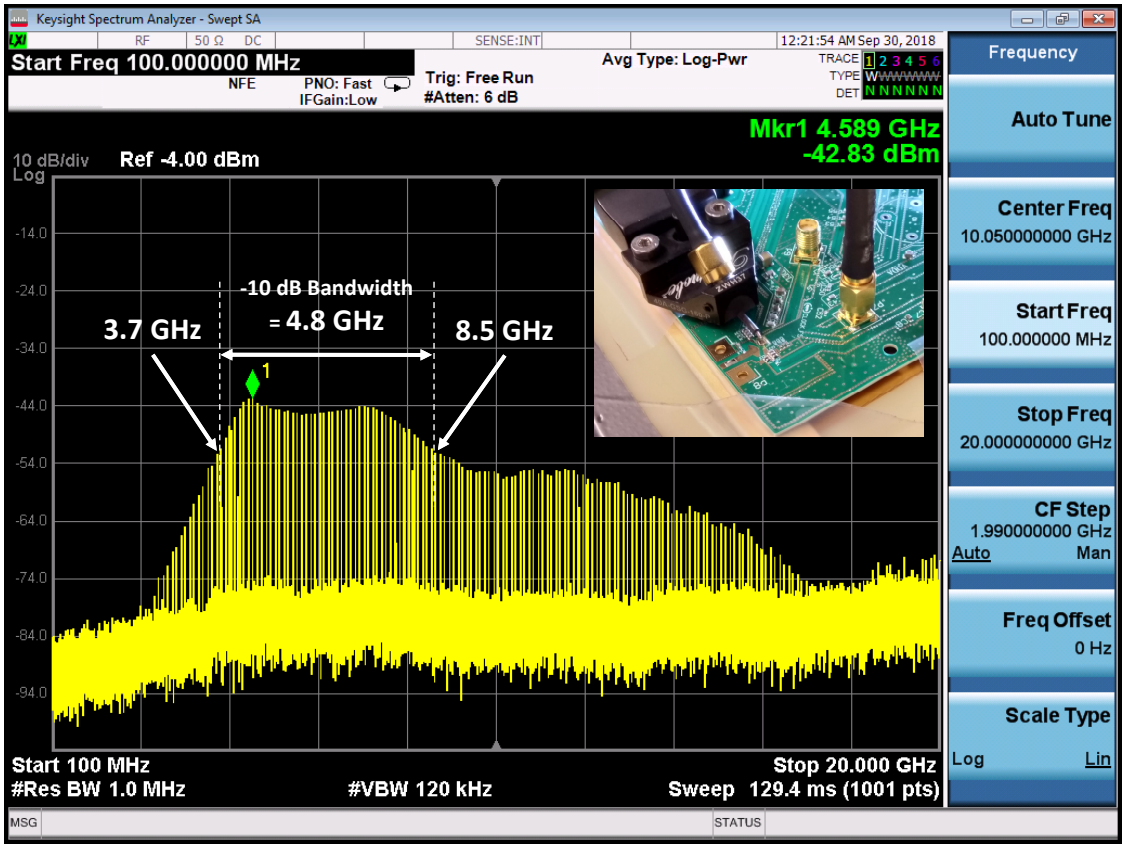


Figure 5.13: PSD of the output pulse train, PRF = 100 MHz

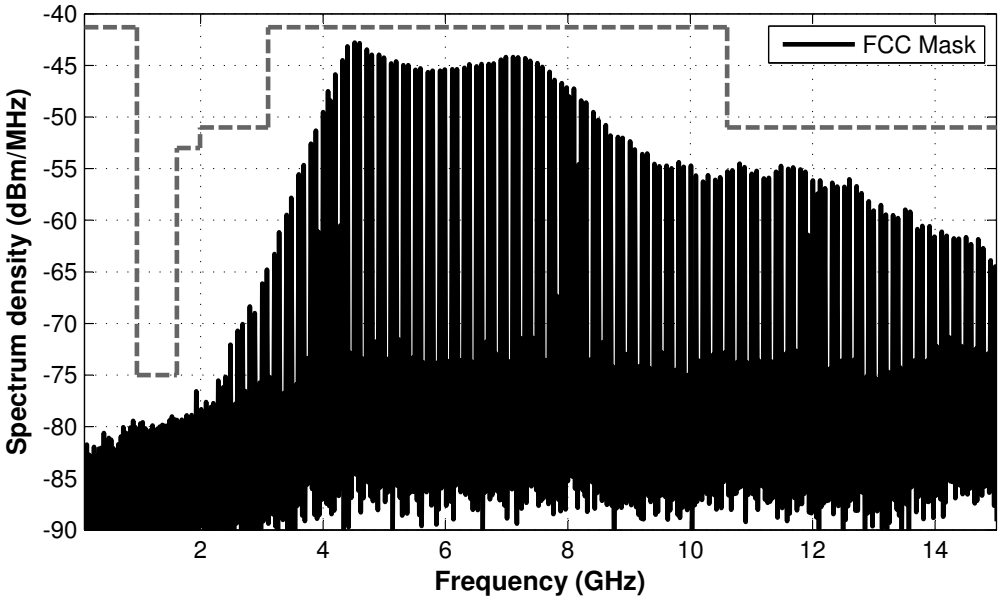


Figure 5.14: PSD of the output pulse train, PRF = 100 MHz compared to FCC mask

According to [18], in order to obtain true RMS average, three requirements should be met, (1) the resolution bandwidth of the analyzer must be set to 1 MHz, (2) the RMS detector should be selected and (3) a video integration time of 1ms or less could be used. Shown in Fig. 5.13, PSD of an impulse train applied to PG.1 circuit is measured by a Keysight N9030A signal analyzer. The pulse generator consume 0.68 mA at pulse repetition frequency (PRF) of 100 MHz, or equivalently 8.16 pJ/pulse/bit. The PSD has -10 dB bandwidth of 4.8 GHz spanned from 3.7 GHz to 8.5 GHz. It also has the peak power of -42.8 dBm/MHz and is compared to FCC mask in Fig. 5.14.

After all, the power of each block is measured and is depicted in Fig. 5.15. The OTA and the T/L comparator draw 200 nA and 8.6 µA, respectively. Overall, the IFN modulator consumes nearly 9 µW. Besides, the power of PG circuit depends on the number of IFN spikes within a packet. However, as an example, if 20 of them are to be sent, 123 nW will be dissipated. For digital block, it is not possible to report an accurate measured power consumption. Since the power supply of the digital interface was used for a few other circuits (e.g., reset circuit on the test PCB and ESD protection and buffers on the die) the measurement value does provide a correct estimation. The measured power at the corresponding connector called "logic interface supply" in Fig. 5.2 is 440 µW.

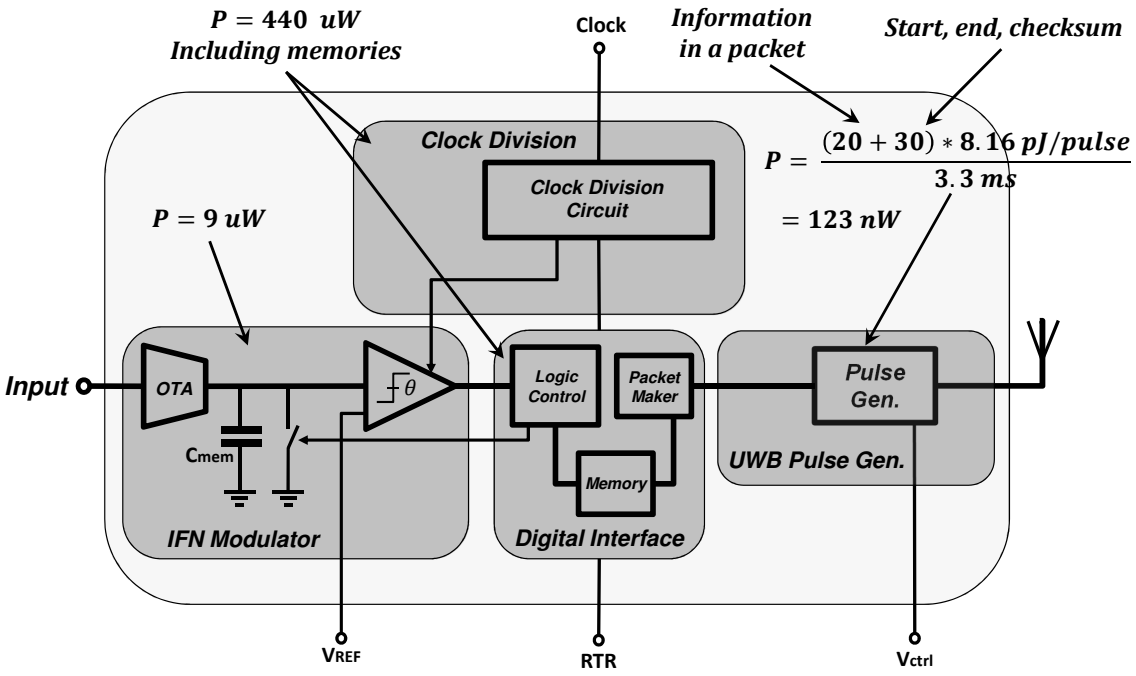


Figure 5.15: Power estimation for the full IRIF transmitter

5.2 Reconstruction Results

Bit stream data obtained from the measurement has been used to recover the original signal. The input 1 kHz sinusoid coming from the function generator is shown in Fig. 5.16-a. This signal is modulated when the V_{ref} voltage is set to 65 mV so that roughly 24 spikes per cycle are generated. The input signal is reconstructed using the measured IFN spikes shown in Fig. 5.16-b, and the recovery technique explained in section 2.1.2.

Reconstruction results in time-domain and frequency domain can be seen in Fig. 5.17

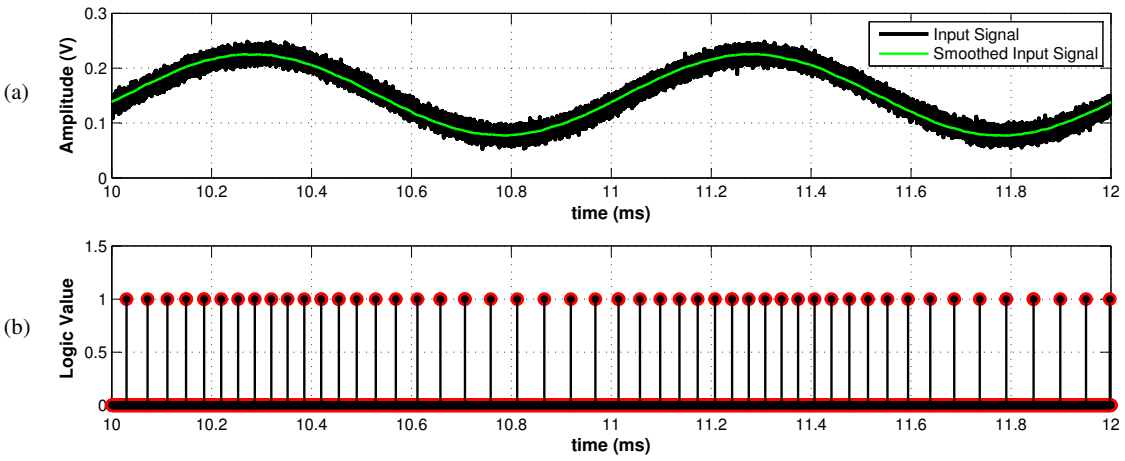


Figure 5.16: Input signal and IFN spikes

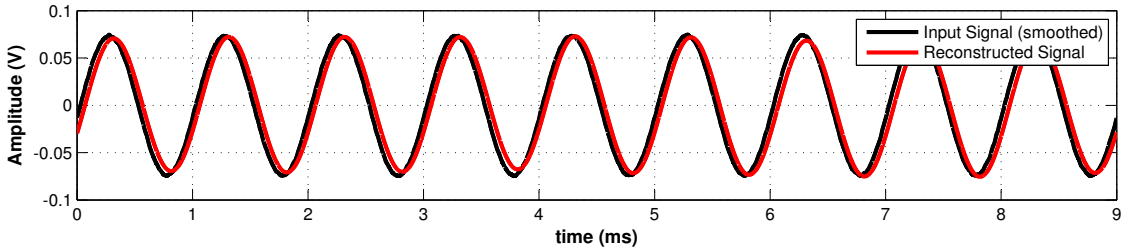


Figure 5.17: Smoothed input signal and reconstructed one

and 5.18, respectively. Figure 5.17, compares the input signal and the reconstructed one, while Fig. 5.18-a shows the PSD of the input noisy signal coming from the function generator and has ENOB of 6.56 bits, while Fig. 5.18-b represents the PSD of the reconstructed signal; it holds ENOB of 5.87. Various reasons can cause low ENOB. It is not only because of the low quality of the input signal, but also three other factors are responsible for degradation in reconstruction. First, inherent error due to reconstruction process that shows itself at lower frequencies. Second, the error related to removing the DC component of the signal, and third, measured 30 mV noise on the VREF pin, even though it is expected to be smaller inside the chip.

5.2.1 Transmission Range

Two horn antennas, with the average gain of 8 dB over the frequency range of 3.1 GHz to 10.6 GHz, have been used to measure the transmission range in a line-of-sight propagation. The receiver antenna is connected to the same oscilloscope described in previous section. Obviously, The SNR decreases as the distance increases. Under such circumstances, at 3 m distance the received SNR is still around 10 dB. Indeed short communication range is one of the inherent characteristics of the UWB systems. Besides, a proper

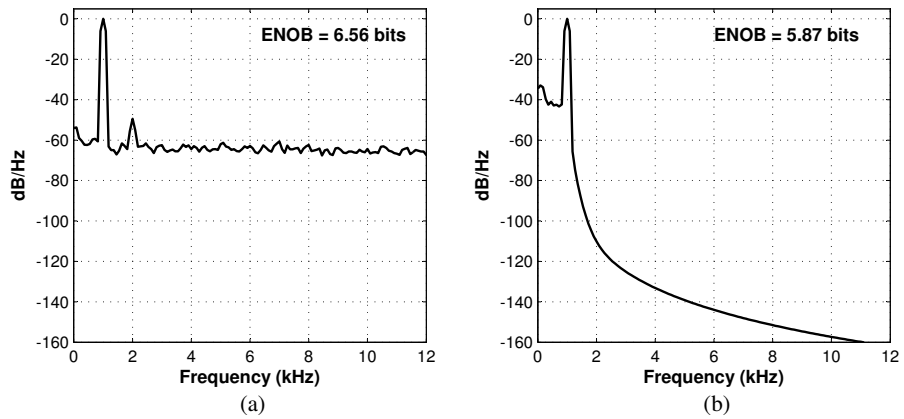


Figure 5.18: (a) PSD of the input signal (b) PSD of the reconstructed signal

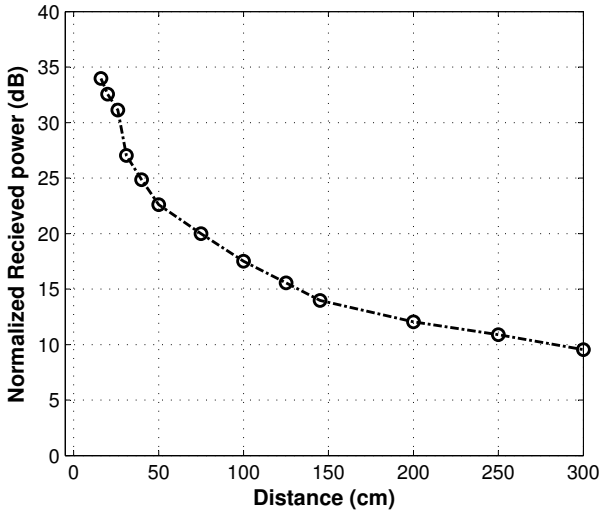


Figure 5.19: SNR of the received signal

antenna for such systems must be omni-directional so that after the sensors are deployed they will be able to communicate with the base node in any direction. Notably, all these measured results are relatively conservative, because the bandwidth of the oscilloscope is limited and also its input amplifier is not low-noise. On the other hand, since the power of the pulse is almost close to the FCC mask, having power amplifier at the output lets the transmitting power go above the mask; thus, it does not help increase of the transmission range.

5.3 Conclusion

In this chapter, the measurement results of the full transmitter chain are presented. Different blocks are measured and evaluated. To a large extent, the measurement results are compatible with those of simulations. The measured power consumption of the IFN modulator is 9 µW. The -10 dB bandwidth of the pulse generator is 4.8 GHz and the pulse shape is compliant with the FCC mask. Each UWB impulse dissipates 8.16 pJ energy per pulse/bit, which is measured at a pulse repetition rate of 100 MHz. Signal reconstruction is performed on a modulated sinusoidal function with frequency of 1 kHz and the PSD calculation represents ENOB of 5.87 bits while the input signal itself holds 6.56 ENOB.

Chapter 6

Conclusion and Future work

In this dissertation, a novel low-power transmitter for UWB and WSN applications has been designed, fabricated and tested. The transmitter is based on a modulation technique inspired from the behavior of neurons in the human body, the so-called integrate-and-fire neurons (IFN). Integrate-and-fire modulator has been embedded in an impulse-UWB radio transceiver system and a new autonomous non-coherent architecture is proposed, which is called IRIF transceiver. The architectural model is implemented in MATLAB and investigated. A simple AWGN channel model including fading effect is utilized and path loss is estimated. In system-level, the performance has been evaluated in terms of quality of modulation, transmission and reception, along with power saving, BER, link budget and checksum effectiveness. The transmitter has the capability of saving power by more than one order compared to typical BPSK transmitters; this is without considering the fact that the transmitter relaxes the need for A/D converters. To prove the claims the transmitter has been designed and fabricated.

All circuits and sub-systems are designed using 1.2 V supply voltage. Simulations have been done carefully by including imposed parasitics models, e.g., PADs, ESD protection circuits, wire-bonds, and RF probe models, and so on. The full transmitter chain has been fabricated in 0.13 µm CMOS technology. For the purpose of chip-on-board measurement, a PCB is designed and its high frequency response is investigated and characterized. Then the measurement results of the full transmitter chain were presented and discussed. To much extent, the measurement results are comparable with those of simulations. The -10 dB bandwidth of the pulse generator is 4.8 GHz and the pulse shape is complaint with FCC mask. Each UWB impulse dissipate 8.16 pJ energy which is measured at pulse repetition rate of 100 MHz. Signal reconstruction is performed on a modulated sinusoidal function with frequency of 1 kHz and the PSD calculation represent ENOB os 5.8 bits while the input signal itself holds 6.56 ENOB. The measured power consumption

Table 6.1: Comparison table

Parameters	Lee [65]	Bao [66]	Mao [68]	This work
Modulation	PWM	PPM	RC time-constant (PPM)	I&F
Radio technology	Narrow band	UWB	UWB	UWB
Tx band	915 MHz	3-8 GHz	3-5 GHz	3.5-8.5 GHz
Peak EIRP (dBm/MHz)	-	-60.4	-58	-42.8
Energy/pulse (pJ/pulse)	-	-	1.47	8.16
Sampling clock	21.48 kHz	300 kS/s	10 MHz	10 MHz
Power consumption	51.4 mW	41.5 µW	3.9 µW	9 µW(450 µW*)
ENOB	8.02 bits	7.3 bits	7.7 bits	5.87 bits
Packetizing and compression	No	No	No	Yes
Technology process	0.35 µm	0.18 µm	0.18 µm	0.13 µm
Year	2016	2018	2016	2019

* Including the digital interface part and general purpose memories

of the IFN modulator and the digital block are 9 µW and 440 µW, respectively. Besides, most part of the 440 µW dissipated power has come from the general purpose memories. Overall, the power consumption of the proposed transmitter is roughly 450 µW. Table 6.1, compares the measured results with other related publications.

Overall, the accomplishments of this work can be summarized as:

- The need for ADC is relaxed and the IFN modulator itself acts as a data converter so that less amount of data is produced and less power will be dissipated.
- A very low power pulse generator is designed with high peak power (EIRP) -42.8 dBm/MHz.
- A digital controller and memory circuit is embedded so that the compression in time and repetition of the packet is possible.

6.1 Future Work

In this transceiver, different building blocks are still missing and needed in order to reach a full ubiquitous system. An oscillator is needed to be designed. As discussed in chapter 2, as the sampling rate increases the better ENOB will be obtained. Thus, larger clock frequency could be considered if higher ENOB is of interest. One possible approach could be through low-power ring oscillators. Another one would be low-power synthesizing clock techniques usually done based on received RF signals. Harmonic injection locked divider (HILD) technique is an example of them. Also, an analog front-end module responsible for filtering, amplifying and making the input signal differential will be

required. Furthermore, a power-on-reset circuit is necessary for initialization. Above all, a receiver must be designed to detect the impulses and thereafter a digital processor to reconstruct the signal.

Besides, a few modifications could be done for improvement of the proposed system. A power management unit could be used for switching on/off the memories by means of power gating techniques for further power saving. In future updates of the system, the memories should be optimized for low power operation. In this design, cell memories are chosen from a standard process IPs (intellectual property); however, if low-leakage ones were possible, their power consumption could have been almost five times lower. Another solution to decrease the power is to use custom designed memory cells. Furthermore, as mentioned earlier, the noise on the reference voltage can degrade the conversion quality and therefore smaller ENOB will be obtained after reconstruction. Thus, minimizing the V_{ref} noise is crucial and an internal band-gap voltage can be designed to provide the reference. Another approach could be a system-level study on bi-phasic modulation that can generate positive and negative IFN spikes. Although, for transmission of such spikes two types of impulse-radios are required, they might alleviate the added low-frequency components after reconstruction. Yet, this technique will increase the power consumption of the pulse generator circuit and overall that of transmitter.

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