FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Design of an Ultra-Low Power RTC for the IoT

David Rosenberger Fernandes Ferrão

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Supervisor: Cândido Duarte

Co-Supervisor: Francisco Gonçalves

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Resumo

A infraestrutura da Internet das Coisas (IoT) está a crescer a um nível exponencial. O potencial de mercado aumenta consequentemente, pois as utilidades previsíveis das implementações possíveis são extremamente diversas, com imensos proveitos ainda por detectar. Por isso, uma crescente procura por componentes que tenham um consumo muito reduzido (ULP) está a ocorrer, pois estes cumprem os requisitos necessários para uma implementação numa rede IoT.

Um nó IoT é composto por uma unidade de gestão de potência, um receptor/emissor RF para comunicações externas, sensores, um processador e um relógio de tempo real (RTC). O RTC é um dos circuitos responsáveis pela gestão do modo de operação num nó IoT e, consequentemente, do seu consumo de potência pois este passa a maioria do seu tempo em "*sleep mode*" com o único circuito ligado sendo o RTC, que requer um design que tenha em atenção um consumo ULP. Realizar o design customizado do circuito e o layout físico deste torna-se um trabalho com imensos detalhes que necessitam de uma atenção considerável.

O trabalho desenvolvido apresenta o desenvolvimento de um RTC com consumos ULP, com componentes analógicos e digitais projetados de forma independente e depois interconectados. A componente analógica é responsável pela criação de uma estrutura que fornece uma independência de variações PVT ao Current-Starved Ring Oscillator com uma frequência de saída estável de 32.768 kHz, a consumos ULP, que subsequentemente é injetada no bloco digital. Diferentes componentes foram desenhados para a implementação analógica: referências de tensão, oscilador e regulador charge pump. Estes blocos individuais foram desenvolvidos com variações PVT reduzidas, operando com consumos ULP.

Isto produz um circuito com um valor de energia/ciclo de 25.7 pJ para um intervalo de temperatura que vai desde os -20 ° C até a 80 ° C, com um coeficient de temperatura de 291 ppm/°C com uma variação máxima de frequência em comparação com o objectivo de 1.74% a -20 ° C e uma mínima de 0.063% a 25 °C. Simulações Monte Carlo no corner TT do circuit extraído do layout atingem um consumo do bloco analógico de 841.97 nW para uma frequência de saída média de 32.698 kHz e um desvio padrão de 179.7 Hz.

Abstract

The emerging Internet of Things (IoT) infrastructure is growing at an exponential rate. Thus market potential for these technologies is huge, since the foreseeable applications are extremely diverse. Subsequently, there is an increasingly high demand for the development of ultra-low power (ULP) components that meet the performance requirements of this IoT network.

An IoT node is composed of a power management unit, a processor, an RF transceiver for external communications, sensor components and a real-time clock (RTC). The RTC is the circuit responsible for the management of the time in an IoT node, being an always-on circuit. This is intertwined with the node power consumption, as it stays most of its operational life in sleep mode with the only on circuit the RTC, which requires an ULP design of the RTC. Hence, designing the full-custom circuitry and physical layout of an RTC becomes a job that has a lot of details that need considerable attention.

The work displayed comprehends the development of an ULP mixed-signal RTC, with the analog and digital blocks developed independently and then interconnected. The analog component is responsible to guarantee an independent to the PVT conditions Current-Starved Ring Oscillator with a stable output frequency of 32.768 kHz, at ULP, which is then injected to the digital block. Different individual components were designed for the analog implementation such as: voltage references, regulated charge pumps and a oscillator. These individual blocks were developed with low PVT variations while operating in an ULP consumption mode.

This produces a circuit with an energy/cycle value of 25.7 pJ for a temperature range of -20 °C to 80 °C, a temperature coefficient of 291 ppm/°C, with a maximum absolute frequency variation relative to the proposed objective of 1.74% at -20 °C and a minimum of 0.063% at 40 °C. Monte Carlo simulations in the TT corner of the layout extracted circuit achieve an analog block power consumption of 841.97 nW for an average output frequency of 32.698 kHz with a standard deviation of 179.7 Hz.

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David Ferrão

"O burro nunca aprende,
o inteligente aprende com sua própria experiência
e o sábio aprende com a experiência dos outros"

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Abbreviations and Symbols

CMOS	Complementary Metal-Oxide Semiconductor
CSRO	Current Starved Ring Oscillator
CTAT	Complementary to Absolute Temperature
IC	Integrated Circuit
IoT	Internet of Things
LVT	Low Threshold Voltage
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PL	Perception Layer
PMU	Power Management Unit
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absoulute Temperature
PVT	Process, Voltage and Temperature
RF	Radio Frequency
RTC	Real-Time Clock
SQW	Square-Wave Output
T2T	Thing 2 Thing
TC	Temperature Coefficient
ULP	Ultra Low power
VLSI	Very Large Scale Integration
XOs	Crystal Oscillator
WSN	Wireless Sensor Networks

Chapter 1

Introduction

The **Internet of Things** is a concept that theorizes that, eventually, every single component in our work, at home and in the city will be interconnected through the Internet. This is a futuristic idea that is currently in development to be further researched and expanded. There are a number of different applications visualized for this technology and they all take into consideration the advantage of having a real-time monitoring and understanding of the surrounding environment, as seen in figure 1.1. [1].

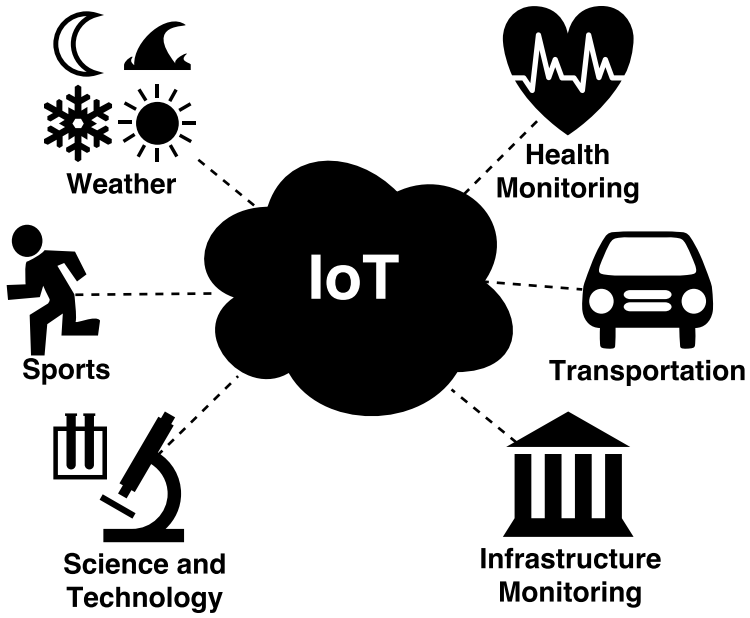


Figure 1.1: Some applications of the IoT

This interface creates a new dimension in the realm of digital information, allowing for the cooperated work between "things" on behalf of humans [2]. Thing to Thing (T2T) interaction is the main objective proposed for the IoT, establishing a new paradigm in our understanding of information, data analysis and transmission, as seen in figure 1.2.

The IoT architecture is composed of 4 main layers [3, 4]. These are described as follows:

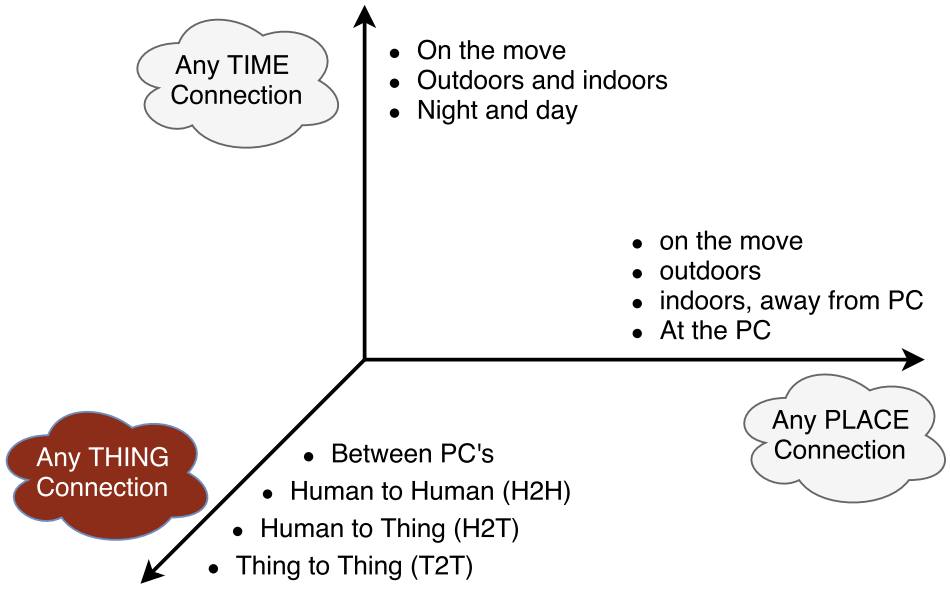


Figure 1.2: Conceiving a new dimension [2]

- **Perception/Sensing Layer** - first and most important layer one of the IoT network. The Perception Layer is integrated with existing hardware and controlling sensors that acquire information from the environment.
- **Network Communications Layer** - responsible for the transmission of data from the PL and the reception of control information. It provides basic networking interface support for wireless data transmission.
- **Middleware Layer** - provides services according to the user's needs and its main focus is to deliver an information processing system that takes actions in an autonomous way taking as reference received data.
- **Application Layer** - implements the real-life functionality of IoT operations according to end user requirements and other applications.

Data flows from the sensors in the **perception layer** through the **network layer**. The network processes and transfers the information through a wireless medium. The **middleware** processes the massive amount of incoming data and decides what is useful for the **application layer**. High level application uses this information and makes it available for further implementation according to the **final demands**. The control of the different layers arrives from the end user towards the lower layers [3, 4].

We can begin to visualize the IoT in our everyday lives through *smartphones*, *smart TV's* and other equipment connected to the Internet. These devices are a starting point, an initial concept of

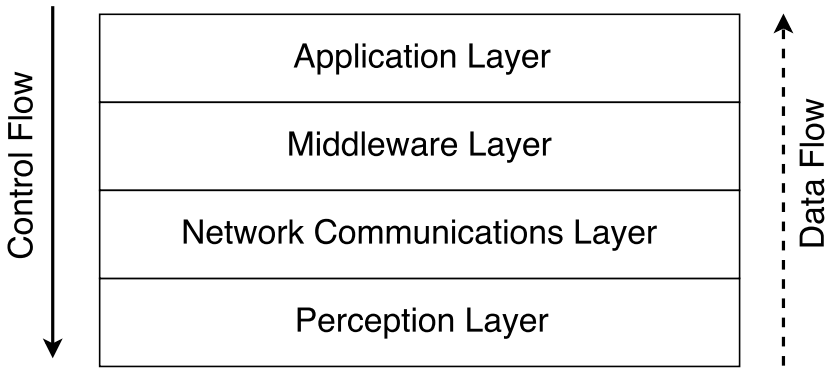


Figure 1.3: IoT Architecture

the IoT since it allows the user to be connected to the Internet anywhere. The building blocks of the IoT are these devices that are known as *smart objects* . Those apparatus are **heterogeneous** and the application layer of IoT allows for their inclusion in a **network of intelligent data**, regardless of their intrinsic characteristics [1].

The number of *smart objects* is growing exponentially and it is expected to reach around 20 to 30 billion devices interconnected in the entire world by 2020, according to predictions from different companies [5]. This is seen in figure 1.4, where the inception point represents the moment where the number of smart objects surpassed the human population.

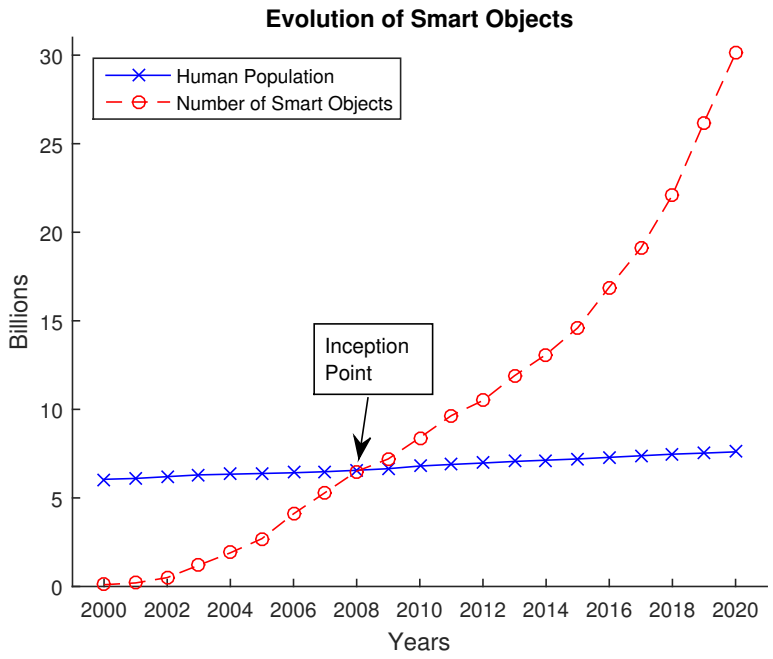


Figure 1.4: Ratio of Smart Objects vs Human Population

1.1 Wireless Sensor Networks

The rapid growth of the IoT caused an exponential increase on the number of interconnected devices. Because of the surge of wireless communication channels, a network is being developed to answer to these specifications known as **Wireless Sensor Networks** (WSN). It is composed of **sensor nodes** and **gateway nodes** (or master nodes) that acquire the data from the connected devices and sends it to the IoT data cloud according to specific application user demands [6].

The IoT data cloud can be specified as a space where the data acquired from the sensors is stored. It can be done in a local register base or through remote servers [2].

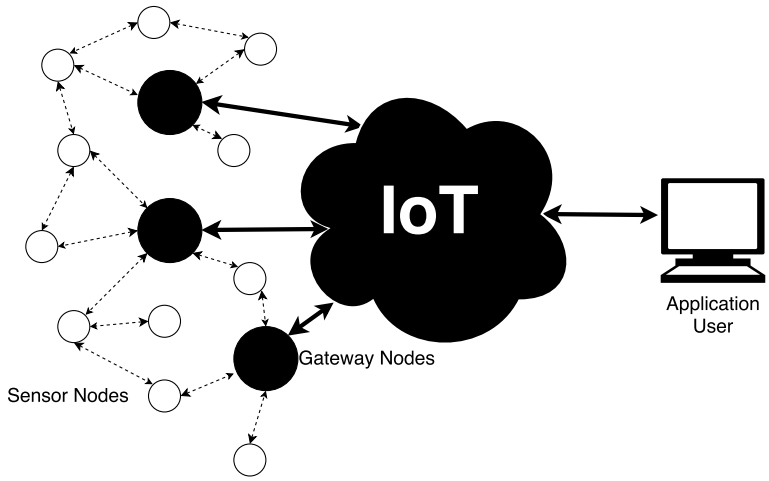


Figure 1.5: Concept of an WSN IoT

A typical **WSN IoT node** has a processing unit, one or multiple sensors, a transceiver, a RTC and a power management unit, as seen in figure 1.6 [7].

- **Processing Unit** is core unit of a sensor, processing the data acquired from the sensor and received from the radiofrequency transceiver. It also manages the general operation of the node.

- **RF Transceiver** is responsible for sending and receiving data from the outside environment. It is the component that has a higher power consumption, due to the inherent characteristics of a wireless transfer communication.

- **Power Management Unit** targets the administration of the total power supply of the unit, allowing for different states of consumption according to current state of processes in the node. It can have an internal power supply (e.g. battery) or an external source. For a WSN node, it is typical that internal batteries are used.

- **Sensors** are the main component of the WSN node. It acquires external data that is sent to the processing unit for internal handling and, consequently, through the RF transceiver to the IoT data cloud.

- **RTC** is the component of an IoT node that is extremely important for its correct behavior because it is responsible for the management, maintenance and verification of the time inside the device, allowing the node to synchronously communicate with the other nodes. For that, this component has a permanent working status, meaning that it will always keep on running regardless if the rest of the circuitry is engaged or not. It is also responsible for the interruptions that will tell the main system that it needs to *"wake up"* and perform some tasks.

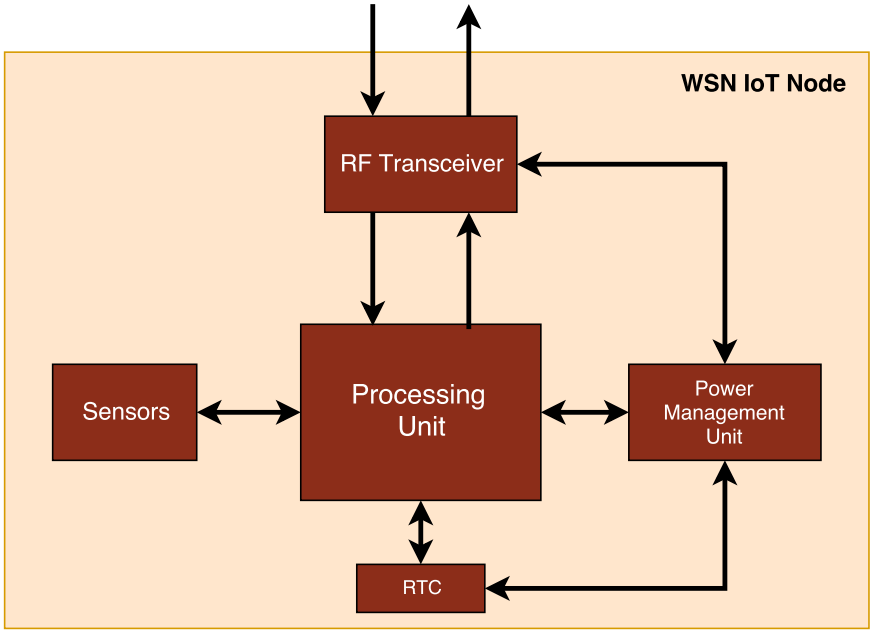


Figure 1.6: WSN IoT node main components

1.2 WSN Node Power Consumption

One of the main requirements of the current IoT implementation is an ultra-low power (ULP) consumption. It has an important impact on the design and development of the components in each node. The current peer-to-peer communication algorithms does not take into account power consumption restrictions of the devices, often leading to an early discharge of the main batteries and, consequently, to its early replacement. Since current software developments have been stagnating due to security issues with the implementation of an IoT network, more focus is being made regarding the hardware components of such IoT networks [4].

The operation in a WSN node is composed of three states with different power consumption, as seen in figure 1.7:

- **Idle mode** - representing the lowest power consumption, it occupies most of the time and is the main factor in the power budget.

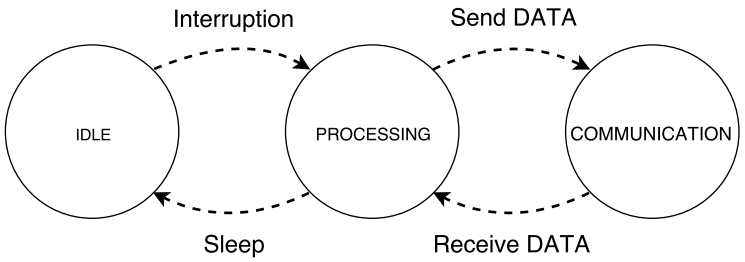


Figure 1.7: State Machine WSN node

- **Processing mode** - happens when the processor is activated, in this case, in order to prepare data to be transferred. It has a higher power consumption than idle mode, showing how important the RTC interrupts are in the power budget scenario.
- **Communication mode** - It happens on a short period of time and it is the highest power consumer in the operation.

The respective power consumption of these modes is demonstrated in figure 1.8. The node spends most of its time in idle mode, processing the data in a fixed interval of time and communicating in the most efficient way (i.e., in the least amount of time possible). This figure only shows the comparison between the different power consumption of the modes, since the processing mode and communication mode might only be active every second or every 5 minutes, according to different implementations [8].

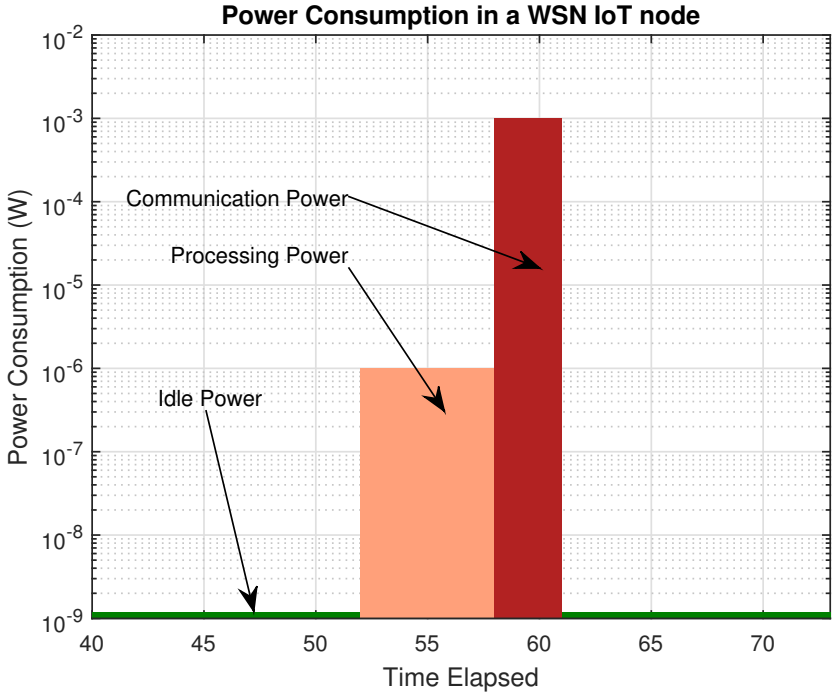


Figure 1.8: Power consumption in a typical IoT node [9]

The fact that the RTC component has a permanent working status means that the total power consumption of the system largely depends on the power consumption of this device. By lowering the necessary power for the correct operation of this device, total power consumption of the IoT node will also be reduced. This assumption is a practical problem to be solved in the IoT research domain, since most of the IoT components are meant to be self-reliable and require them to perform through long time periods (years).

1.3 Motivation

The Internet of Things is growing at an exponential rate. This new perception of reality is being researched even further nowadays because society is starting to develop an interest on these technologies. Market potential is increasing even further, since the foreseeable implementations are diverse and still to be detected. The future applications for the IoT are enthusiastic and they will increase the overall quality of life of the citizens of the world.

Developing a component that is crucial for the sustainability of this implementation is the task that truly motivates the intended work for this project. Designing the full-custom circuitry and physical layout of a Real Time Clock becomes a job that has a lot of minor details that need considerable attention. These technicalities truly tone the developers skill and knowledge of different design principles.

Besides, developing the solution using **ultra low power** CMOS techniques will put emphasis on different technological procedures. Producing devices that are heavily dependent on PVT variations, operational frequency and power consumption define this new task, that needs a stable approach to all these diverse figure of merits, even though they are all interconnected. The study and understanding of these different approaches allows for a more complex in depth grasp of this recent intriguing proceedings.

1.4 Problem Statement

The main purpose of this dissertation is to develop an analysis of the performance of an RTC component when applied to IoT nodes. As said before in the scope of this work, it is expected to design, implement and validate a Real-Time Clock circuit for use in an Internet of Things node, with power consumption being the major performance parameter to leverage in order to fit IoT requirements. Main expected features should also be added for the standard use of this component.

The main objectives of this dissertation are

- Design of an RTC to be used in an Internet of Things context;
- Ultra Low Power Consumption, in the order of sub-μW;
- CSRO with an output frequency of 32.768 kHz, with low PVT variation;

- Layout development with a focus on minimum area, sub-mm^2;
- Implement all the expected features in a typical RTC (time counting, interruptions, alarms...).

1.5 Document Outline

This document is constituted by the following chapters, besides the Introduction, as follows:

- **Chapter 2 - Subthreshold Operation Regime**

  Subthreshold operation regime is researched and analyzed. The main factors surrounding its behaviour are described and related to the work.

- **Chapter 3 - Real Time Clock Integrated Circuits**

  An extensive research will be performed regarding the current RTC ICs that the market offers. Through that, it will be possible to understand the different functional blocks that it requires to operate as well as different extra funcionalities that can be implemented. Besides, different oscillator implementations are studied and analyzed.

- **Chapter 4 - Proposed Architecture**

  The proposed architecture for the implementation of the work is shown. Both analog and digital design blocks are explained.

- **Chapter 5 - Power Management Unit**

  The Power Management Unit of the analog block is described and analyzed. Voltage references and regulated charge pump for this block are studied and the results from the layout extraction are shown.

- **Chapter 6 - Oscillator Design**

  The structure of the chosen oscillator topology is analyzed and shown. Besides, PVT compensation is explained and the results from the layout extraction are studied.

- **Chapter 7 - Integration**

  Power Management Unit and the Oscillator block are connected and the layout parasitic components are extracted. The results from this simulation are shown and analyzed.

- **Chapter 8 - Conclusions and Future Work**

  Some final considerations are done and the future work is presented.

Chapter 2

Subthreshold Operation Regime

Ultra low power micro systems are highly in demand in the IoT market. These micro systems target wireless nodes and battery-powered applications. For such systems, power consumption reduction becomes critical due to battery lifetime extension.

Complementary Metal-Oxide Semiconductor (CMOS) is still the main Very Large Scale Integration (VLSI) technology used in the design of current circuits due to its power characteristics. It consumes power when changing state and not in a steady state. Traditionally, CMOS technologies operate with a strongly inverted channel, meaning that the supply voltage V_{DD} is above threshold voltage, V_T [10].

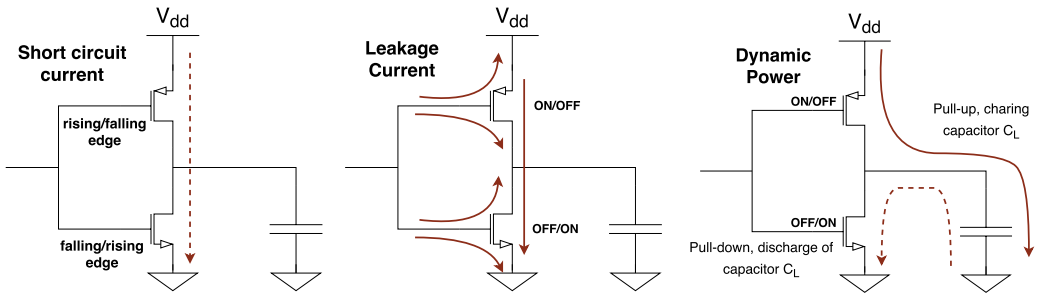
Lowering the supply voltage is the main path in order to reduce the power budget of an IoT node. However, this is not the only approach to decrease power consumption. In this dissertation, some of the transistors will be operating in the subthreshold (or weak inversion) region, since it also allows for low current values. This operation region is achieved when transistors are operating below or near V_T. Although the subthreshold regime is familiar in the field of circuit design since the 1970s , only now due to the rising popularity of ultra low power systems it is gaining more attention [11, 12].

This weak inversion region is considered a leak current in a strong inversion circuits. Since $V_{GS} < V_{TH}$, it is assumed that the device is turned off. This is not true due to the subthreshold current flowing even when the device is below threshold voltage. Total power consumption of the device is still dependent of this leakage, the **subthreshold current**. For ultra low power devices, this current proves to be an effective operation region for the intended objectives.

2.1 CMOS Power Consumption

As seen in figure 2.1 , in digital circuit CMOS design, power consumption is divided into three sections as described as follows [10]:

$$P_{total} = P_{dynamic} + P_{static} + P_{shortcircuit} \tag{2.1}$$



(a) Short Circuit current (b) Static/Leakage current (c) Dynamic current

Figure 2.1: The power components of a CMOS digital circuit [10]

2.1.1 Dynamic Power

Dynamic power, also known as switching power, comes from the output changing state. It is used to charge the load capacitance through the pMOS transistor with the high voltage level, usually V_{DD}. When the output changes to 0, it does not draw charge from the supply. However, the energy stored is dissipated through the nMOS pull-down transistor. The dynamic power consumption is described as [13] :

$$P_{dynamic} = \alpha_{0\to1} \cdot f_{clk} \cdot C_L \cdot V_{DD}^2 \tag{2.2}$$

Since most switching does not occur in the f_{clk} but at smaller speeds, $\alpha_{0\to1}$ describes the activity factor, $0 < \alpha_{0\to1} < 1$ (exceptions made regarding clock buffers). C_L stands for average load capacitance.

As seen in (2), dynamic power consumption is proportional to the clock frequency and the supply voltage squared. It is independent of the rise and fall times of the input gate signal [13].

2.1.2 Short Circuit Current

Short circuit power dissipation happens when both nMOS and pMOS devices are on, creating a direct path between V_{DD} and GND. This is significant when rise/fall time in the input gate is larger than the rise/fall time in the output since the short-circuit path will be opened for a longer period of time. Short circuit power dissipation is usually insignificant in the desing of a low power logic circuit [13].

2.1.3 Static Power Dissipation

Static/Leakage power dissipation occurs even when the device is in a stable logic state. This leakage is composed of 4 different types of currents, as shown in figure 2.2, that occur for different reasons as follows [10]:

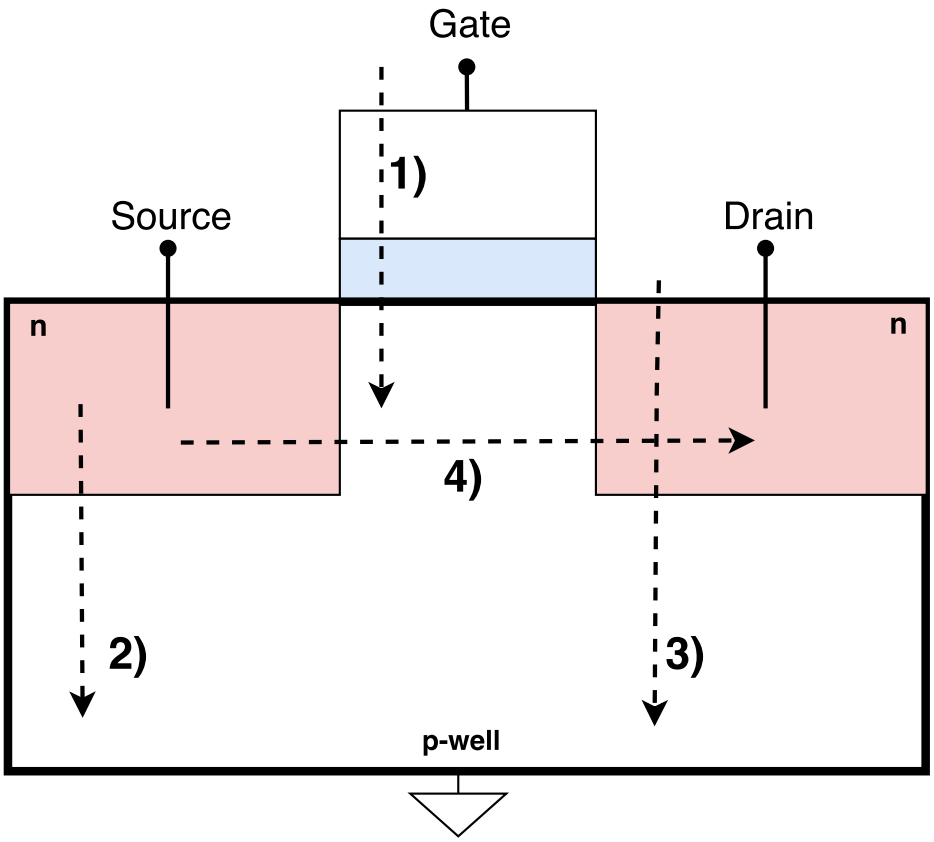


Figure 2.2: Components of Leakage Power [10]. The **gate-oxide leakage current** *(1)* flows from the gate supply towards the bulk through the oxide. **Reverse-biased diode leakage current** *(2)* flows from drain and source towards the bulk. **Gate induced drain leakage current** *(3)* flows from the drain interface with the oxide to the bulk. **Subthreshold leakage current** *(4)* flows from the source towards the drain when the device is "turned off", i.e., when $V_{GS} < V_T$

.

- **Gate-oxide tunneling** is a current I_{ox} that is flowing through the oxide layer in the gate. This layer is getting thinner with current developing technologies and can surpass other leakage currents as a dominant leakage mechanism in the future. As voltage supply is lowered, this tunneling effect decreases faster than subthreshold current, making it imperceptible.

- **Reverse-biased diode leakage** to drain and source to the bulk is composed of two components: electron-hole pair generation inside the depletion region of reverse-biased pn junction and the minority carrier diffusion and drift near the depletion region [14]. Process technologies create devices in a way that this leakage is small compared to subthreshold leakage [12].

- **Gate induced drain leakage (GIDL)** is due to the high electric field near the interface between the gate oxide and drain, making the silicon surface act like a p region. This current flows from the surface of the drain into the body of the transistor. For subthreshold

operation, low V_{DS} causes a reduction in the value of this leakage, making it negligible compared to subthreshold current [12].

- **Subthreshold leakage** Subthreshold operation regime occurs when V_{GS} is below threshold voltage. This region is also called *weak inversion* region. As seen in figure 2.3, an approximation is made regarding a relationship of drain current and gate to source voltage, with V_{DD} = 1.8V in 0.18 μm technology. In subthreshold, I_D varies exponentially with V_{GS}. Threshold voltage V_T is defined as the point where I_D starts to deviate from its original trajectory . The *subthreshold slope* of a transistor is defined as [12]:

$$S = nV_{th} \ln 10 \tag{2.3}$$

The ideal value of S in room temperature, i.e., T = 300K, is 60mV/dec and it occurs at the limit when n = 1. This parameter represents the effectiveness of the transistor in its ability to be turned off when V_{GS} is decreased below threshold voltage [14].

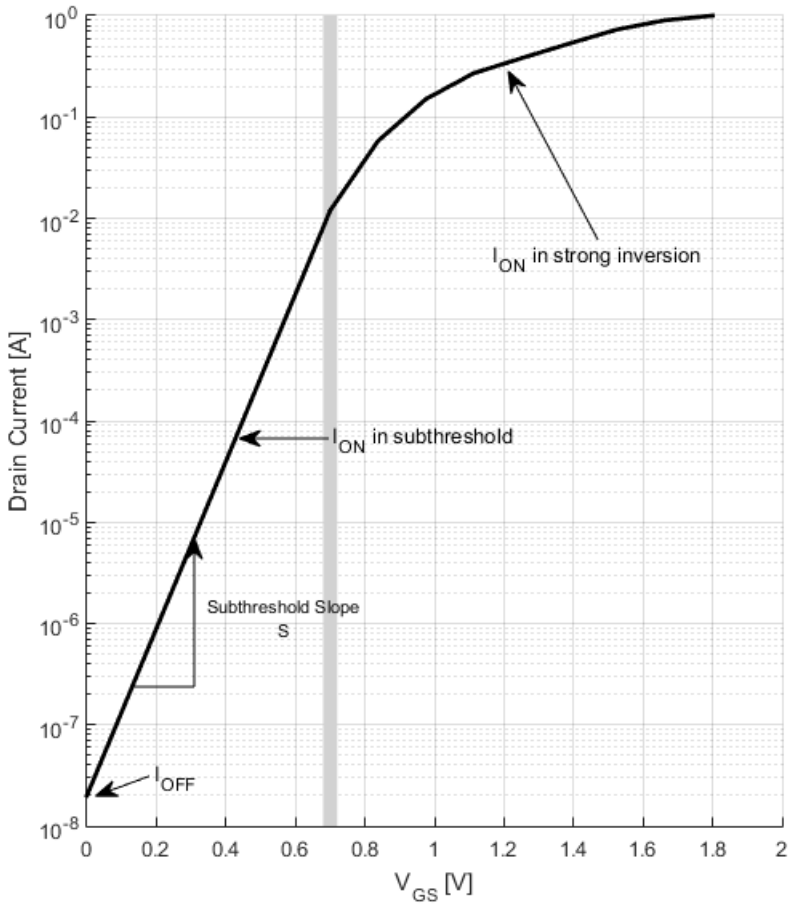


Figure 2.3: MOSFET Drain Current vs Gate to Source Voltage[12]

Another effect to consider in subthreshold leakage is the DIBL (Drain-induced barrier lowering) effect. It can affect the channel charge like V_G, prominent in short-channel devices [14]. In these devices, the proximity of the source and drain makes it so that drain voltage influences the depletion region beneath the channel. It is characterized as the reduction of V_{TH} due to high drain voltage [10].

These leakages tend to be negligible in comparison to subthreshold current. One case where this is not accurate is in a circuit operating at lower temperature. Since subthreshold current is exponentially related to temperature, gate leakage may become relevant again. Otherwise, for weak inversion operation, only subthreshold current is considered [12].

2.2 MOS EKV Model

The EKV analytical model for MOS transistors was first proposed in [15]. In [12, 16], the compact equation for all operation region current is described as:

$$I_D = I_{D0} e^{\frac{V_G}{nU_T}} \left(e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}} \right) \tag{2.4}$$

where

$$I_{D0} = I_{spec} e^{-\frac{V_{T0}}{nU_T}} \tag{2.5}$$

is the residual drain current in saturation for $V_G = V_S = 0$ or channel "leakage" current of CMOS digital circuits and I_{spec} is the *specific current* of the transistor, given as:

$$I_{spec} = 2n\beta V_T^2 \tag{2.6}$$

and β is the transfer parameter of the transistor:

$$\beta = \mu C_{OX} \frac{W}{L} \tag{2.7}$$

In these equations, these parameters are described as:

- V_T is the threshold voltage;
- n is the subthreshold slope factor which depends on process parameters (capacitive divider effect formed by C_{OX} and C_d) as well as biasing conditions, and is usually between 1 and 1,5 [14];
- U_T is the *thermodynamic voltage* described as:

$$U_T = \frac{kT}{q} \tag{2.8}$$

where k is the Boltzmann constant and q is the elementary charge. For T = 300 (27°C), U_T is 25,8 mV;

- C_{OX} is the gate oxide capacitance in *farads*;
- μ is the carrier mobility;

As seen in (2.3), drain current is exponentially proportional to gate, threshold, source and drain voltage. This means that lowering power supply will subsequently reduce power consumption of the device.

The exponential characteristics in the subthreshold EKV model makes it vulnerable to Process, Voltage and Temperature (PVT) variations [12] [17]. There are differences between analog and digital operations. For analog, it is important to have a better control over PVT, since the variations might undermine the overall operation.

2.2.1 Process

Process variations have an impact mainly in the model parameters V_{T0}, n and β, since transistors with equal structures in the layout do not have equal properties. This is seen in equation (2.3) and can be derived from random dopant fluctuations and small variations in the parameters of physical characteristics [18, 12].

2.2.2 Voltage

In ULP systems, voltage differences are due to variations in the external supply. Since I_{on} is orders of magnitude lower than in strong inversion operation regime, voltage drops across the on-chip supply distribution network are imperceptible. In battery powered systems, voltage supply is relatively constant. For batteryless devices, these suffer from much more pronounced power supply variations which are handled through voltage regulation circuits [18].

This means that, for an ULP system, the voltage regulation circuit has an important impact in the management of the power supply, since subthreshold devices have an exponential sensitivity to voltage variations.

2.2.3 Temperature

As seen in equations (2.1), (2.2) and (2.5), absolute temperature has an exponential impact on the drain current. In [19], it is shown that, due to its positive temperature dependence, subthreshold I_{ON} current increases exponentially with temperature while $\frac{I_{ON}}{I_{OFF}}$ ratio degrades due to the increase in leakage currents. Tolerable subthreshold circuit operation is placed at 25-75°C.

In figure 2.4, it is shown that in subthreshold operation, variations in temperature parameter have a greater impact the closer circuit operation reaches weak inversion. As operation decreases V_{GS}, temperature variation increases drain current very rapidly[14].

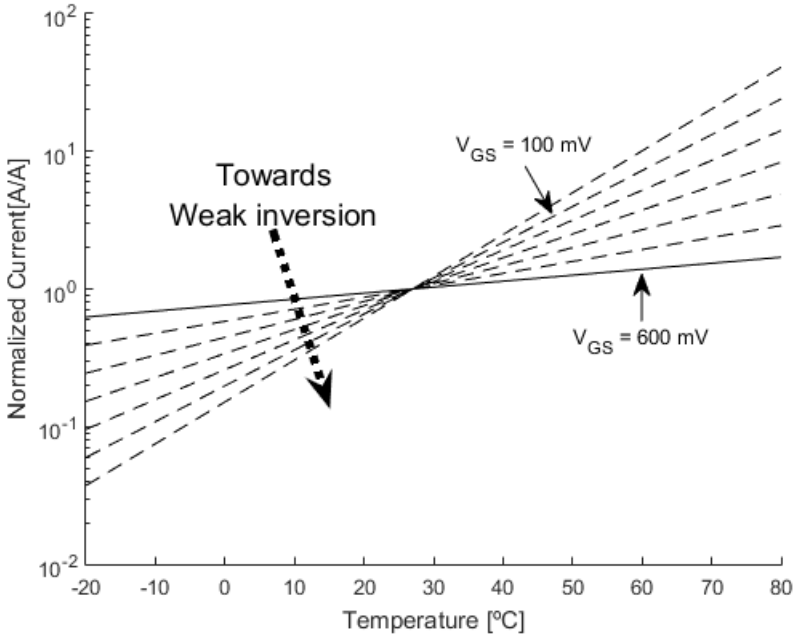


Figure 2.4: Bias current dependence on temperature variations. In this figure, the bias current is normalized to the nominal bias current at T = 27°C

2.2.4 Delay and Operational Frequency

This ultra low power consumption comes at a cost where lower drain current means that it will take longer to charge the output of a device. This latency will therefore affect the maximum operational frequency of a device.

In weak inversion operation, propagation delay for an inverter circuit with an output capacitance C_G is described as [12]:

$$t_d = \frac{KC_G V_{DD}}{I_{Dsub}} \tag{2.9}$$

where K is a delay fitting parameter. As seen in equation (2.2), since drain current has an exponential behavior this means that if it decreases, propagation delay will increase rapidly. With an increase of this delay, operational frequency will decrease consequently. Subthreshold devices are applied in situations where the frequency of the device is not an important factor.

Some situations are described in [8] where a city can check its waste containers levels to create a route and perform a service in a more efficient way [20] and in [21], where the human body is the target for health monitoring especially in cases like glucose level sensing and electrocardiogram monitoring. Some sensors only need to capture data in relatively great intervals of time (every second or every 5 minutes), allowing for a lower frequency operation of the device. This proves to be an effective solution to these situations, since lowering power consumption is the main objective of such implementations.

Observing subthreshold transistor behaviour, this "leakage current" can be perceived as a valid

operation region for ultra low power circuits. The main considerations to be taken are temperature dependence and the high propagation delays that are characteristic of the weak inversion region.

Since the main objective of the implementation of a WSN IoT node is to lower power consumption, operational frequency is a parameter that can be depreciated. PVT variation must be taken into consideration for a more balanced subthreshold circuit operation.

Chapter 3

Real Time Clock Integrated Circuits

The Real Time Clock (RTC) ICs all have the same functionality, *i.e.* they will keep track of time since a certain point that can be programmed and, if necessary, they can perform interrupts or output different signals. Most of those Integrated Circuits have the same core functional blocks and some of them (that are more expensive and complex) offer extra functionality. A research has been made regarding the Integrated Circuits (ICs) that are available in the actual market.

The main core functional blocks that are shared through all of the researched integrated circuits in the market are as shown in figure 3.1.

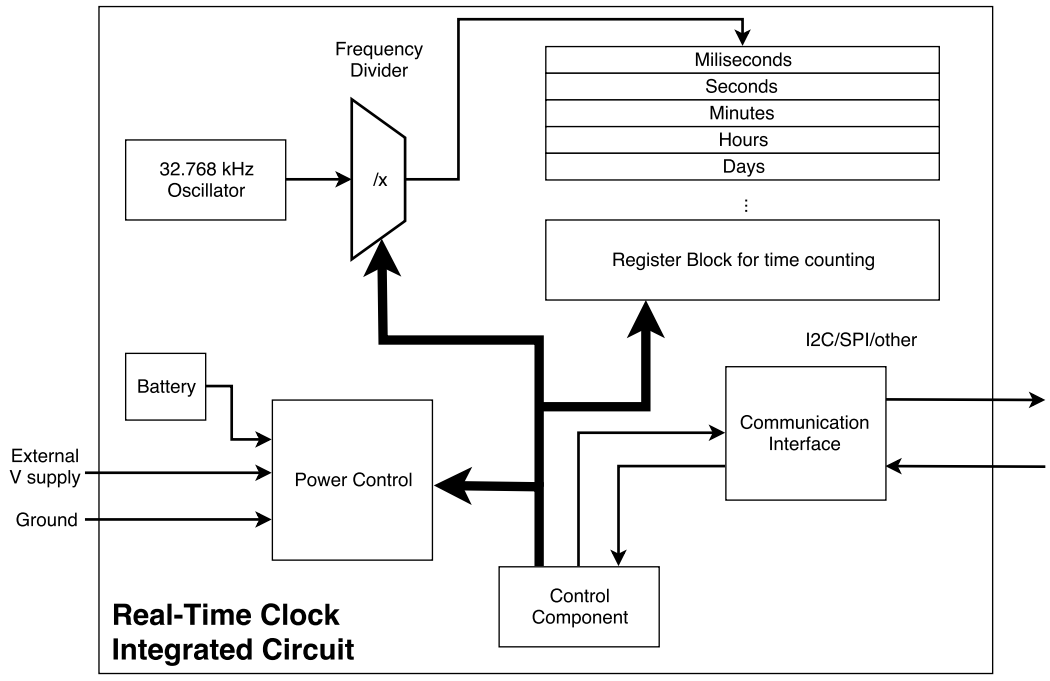


Figure 3.1: RTC IC main core functional blocks

- **Power Control** - This power control block will define where the supply power will come from. It can either originate from an external device, internal or external battery. This

is important because if the proposed RTC architecture has a low area size and an internal battery, this power supply will need to obey to a certain power characteristic and size limit

- **A Memory where it saves the elapsed time since boot** - The internal memory is divided in different registers that keep track of time in different time magnitudes, *i.e.*, seconds, minutes, hours, days, weeks, months, years and so on. Since most of the available ICs have leap year calculation integrated, it will automatically scale the registers so some of them can be reset when needed, accurately.

- **Communication Interface** - This communication interface is necessary so that external devices have the possibility to access the data inside the above mentioned memory. It can be implemented using different protocols (I2C, SPI, 3-wire topology...) and is selected in advance by the manufacturer.

- **IC component control** - This block is the main control of the integrated circuit. It analyses the signals that are being input by the user (trough the communication interface) and selects the data that will be output. It can also allow for different functionalities to be activated in some ICs (*alarms, interrupts, external signal generator, timer*...). It is also the functional block that keeps the time registers in the main memory updated. The time scale used for the updates is defined by the next component.

- **Oscillator frequency divider/scaler** - This block will simply select the frequency that the control component will base its calculation. As it performs with higher frequency, the time resolution will drop and the registers will keep track of time using a minor time magnitude. Some integrated circuits also allow for time resolution in the millisecond scale, allowing for more precise and accurate time keeping. In figure 3.2, is shown a brief resumed main interaction between the oscillator and the time registers. In this implementation, the prescaler (divider) defines a ticking 1 Hz clock that updates the second timer. Another counter (second counter) is being updated with the value from the second register and when it hits 60, it increases the minutes register and resets the value inside the second register to 0 and so on.

- **A RAM memory** - useful for intermediate calculations and simple arithmetic operations when operating through memory addresses and timer registers. In most cases, this RAM is limited and the number of bytes that it allows reaches a maximum of 512 bytes in the best option that the market allows.

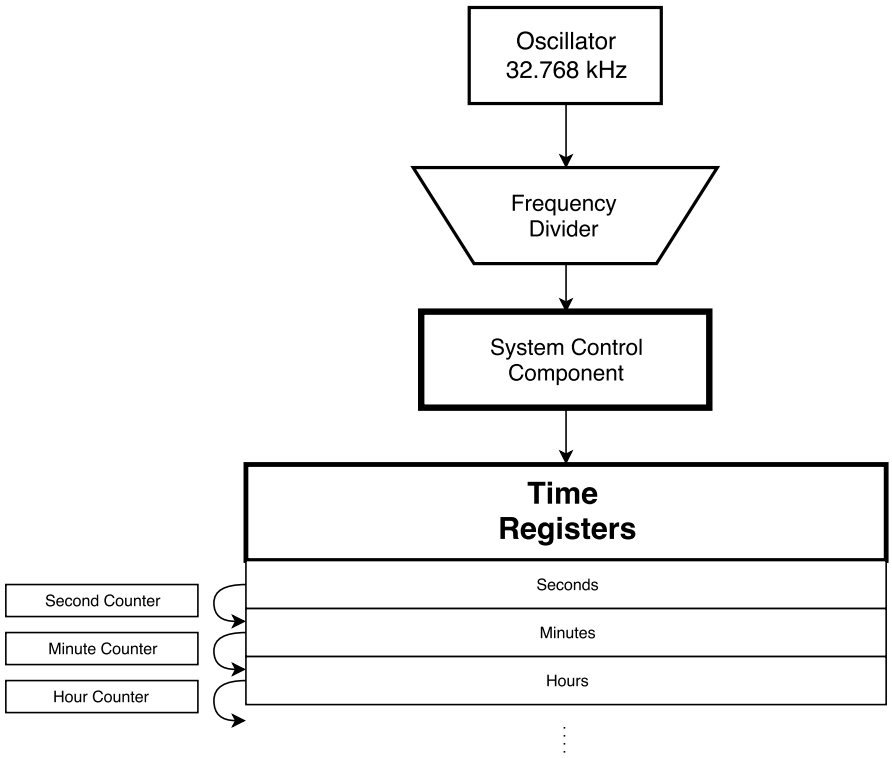


Figure 3.2: Time registers functionality

For some cases, the integrated circuits available in the market can also allow for an output (Square-Wave Output (***SQW***) or an analog sinusoidal oscillation) whose frequency can be selected through the prescaler or an internal multiplexer component. This scaling is done by the SQW prescaler register that has a defined number of bits to select different operation frequency. The signal output functionality will also need more power to operate, so in most cases, in order to lower the power consumption of the integrated circuit component, this will be turned off. In table 3.1, we can see, for the specific RV-1805-C3 RTC IC case, some frequencies that are enabled according to different SQW bit selections.

Additionally, some integrated circuits also allow for extra functionalities. Some of these utilities are only implemented if the user wants them to be activated. One has already been shown, the clock signal output. This one in specific consumes more power and should only be activated if needed. Aside from that, Real-Time Clock integrated circuits can also have:

- **Calendar functionality** that saves the actual date in a specific register. For this to work properly, the component should also have a leap-year calculation logic circuit that analyzes the year, month and day registers of the internal memory to process the days that the current year has.

- **12h/24h mode selection** allowing for flexibility regarding different global time measurements.

Table 3.1: SQW functionalities from the RV-1805-C3 RTC IC

SQW bit Selector					**Functionality**	**SQW bit Selector**					**Functionality**
0	0	0	0	0	1 century	0	1	1	0	1	4 Hz
0	0	0	0	1	32.768 kHz	0	1	1	1	0	2 Hz
0	0	0	1	0	8.192 kHz	0	1	1	1	1	1 Hz
0	0	0	1	1	4.096 kHz	1	0	0	0	0	1/2 Hz
0	0	1	0	0	2.048 kHz	1	0	0	0	1	1/4 Hz
0	0	1	0	1	1.024 kHz	1	0	0	1	0	1/8 Hz
0	0	1	1	0	512 Hz -default	1	0	0	1	1	1/16 Hz
0	0	1	1	1	256 Hz	1	0	1	0	0	1/32 Hz
0	1	0	0	0	128 Hz	1	0	1	0	1	1/60 Hz (1 minute)
0	1	0	0	1	64 Hz	1	0	1	1	0	16.384 kHz
0	1	0	1	0	32 Hz	1	0	1	1	1	100 Hz
0	1	0	1	1	16 Hz	1	1	0	0	0	1 hour
0	1	1	0	0	8 Hz	1	1	0	0	1	1 day

- **Interruptions** that activates a set output if a specific time has elapsed, allowing for low power consumption since most of the time, the component is in timekeeping mode. Some components have more than one interrupt output.
- **Alarms** that activate a set output if a specific date and hour has been reached.
- **Integrated XO Crystal** to allow for a more independent functionality.

In the next subsegment, an extensive research has been made regarding the Real-Time Clock integrated circuits that the current market has and the different functionalities that each one possesses.

3.1 Review of the RTC IC Market

In this subsection, an analysis will be performed regarding the main Real-Time Clock integrated circuits that the current market has available. A search has been made focusing on different microelectronics companies. In the scope of this work, only components that have low power or ultra low power consumption will appear in this examination.

A temperature range analysis will also be performed because ultra low power operation region is highly sensitive on absolute temperature. Voltage supply, current consumption and SQW/analog output will also be a figure of merit because the power consumption metrics are heavily influenced by these factors. Since this integrated circuits come in different packages, they only serve as a medium to compare what the market has to offer considering the projected work has different size objectives. This search is important to understand the main functional blocks and different functionalities that are expected from a Real-Time Clock component.

Voltage supply (V_{DD}) is represented as the minimum to maximum range while the communication protocol ($I2C, SPI$ or $3-wire$) is activated to make sure that there are no failures during this

operation. This voltage supply can be even lower when communication is not happening. Current consumption parameter shows the value that the component expends while there is no clock output and the communication protocol is disabled since, otherwise, the current expenditure would be greatly increased while the module is transferring data (around μA range).

In table 3.2, an analysis is performed regarding the main subthreshold Real-Time Clock integrated circuits that each manufacturer has for production and sale [22, 23, 24, 25, 26, 27].

Table 3.2: RTC IC in the current market

Component	Supply Voltage (V)	Current Consumption (nA)	Communication Protocol	RAM Bytes	SQW Output
Maxim Integrated [22]					
DS1339A	1.8 to 5.5	300	I2C	None	Yes
DS1308	1.8 / 3 / 3.3	250	I2C	56	Yes
DS1347	2 to 5.5	350	SPI	31	Yes
DS1344	1.8 / 3 / 5.5	250	3-Wire	96	Yes
DS1342	1.8 / 5	220	I2C	None	Yes
DS1341	1.8 / 5	400	I2C	None	Yes
DS1339	1.8 to 5.5	400	I2C	None	Yes
STMicroelectronics [23]					
M41T62	1.3 to 4.4	350	I2C	None	Yes
M41T65	1.3 to 4.4	350	I2C	None	No
M41T93	2.38 to 5.5	365	SPI	12	Yes
M41T82	2.38 to 5.5	365	I2C	12	No
M41T56	4.5 to 5.5	450	I2C	56	No
EM Microelectronics [24]					
V3020	1.2 to 5.5	390	1 bit serial	None	N/A
V3021	2 to 5.5	800	1 bit serial	None	N/A
A3024	2 to 5.5	1200	8 bit parallel	16	N/A
EM3027	1.3 to 5.5	600	I2C & SPI	8	N/A
Micro Crystal Switzerland [25]					
RV-8564-C3	1.8 to 5.5	250	I2C	512	No
RV-2123-C2	1.6 to 5.5	130	SPI	512	No
RV-8803-C7	1.5 to 5.5	240	I2C	512	No
RV-8523-C3	1.6 to 5.5	130	I2C	512	No
RV-2251-C3	1.8 to 5.5	270	I2C	512	Yes
RV-1805-C3	1.5 to 3.6	60	I2C	512	No
RV-8063-C7	1.8 to 5.5	180	3-Wire	512	Yes
NXP Semiconductors [26]					
PCF2123	1.8 to 5.5	100	SPI	None	Yes
PCF8523	1.6 to 5.5	150	I2C	None	Yes
PCF8564A	1.8 to 5.5	140	I2C	None	Yes
PCF85063A	1.8 to 5.5	122	I2C	None	Yes
Ambiq Micro [27]					
AM0805	1.7 to 3.6	14	I2C	256	Yes
AM0815	1.7 to 3.6	14	SPI	256	Yes

As shown in table 3.2, current consumption on the mentioned integrated circuits stands inside the *nA* magnitude. Besides what is shown, temperature range is almost always the same (-40°C to 80°C), showing that the manufacturing process takes into account this parameter in order to develop a standard temperature operation region. This is relevant due to the great fluctuation in subthreshold transistors intrinsic operation properties caused by temperature variance.

Though it must be taken into account that the power consumption shown in table 3.2 is achieved for some cases where the oscillator component is an external element, such as an XO. For example, in the AM0805 component, the value of 14 nA is obtained while using an internal RC oscillator, whose operating frequency is only 128 Hz.

Besides, most IC's use the same known **communication protocols** (I2C, SPI, SPI 3-wire or serial). RAM bytes are more relative, since some circuits do not have any bytes in the user RAM. Exception made for Micro Crystal Switzerland, that implements a memory register of 512 bytes, significantly higher than the remaining devices.

In figure 3.3, a comparison has been made taking into account minimum voltage supply and respective current consumption of the different devices researched in table 3.2. There is a region where researched market IC's are more concentrated. For the pretended circuit development, this is the intended region for implementation. The minimum supply voltage should be around 0.7-2V and current consumption should be lower than 850 nA.

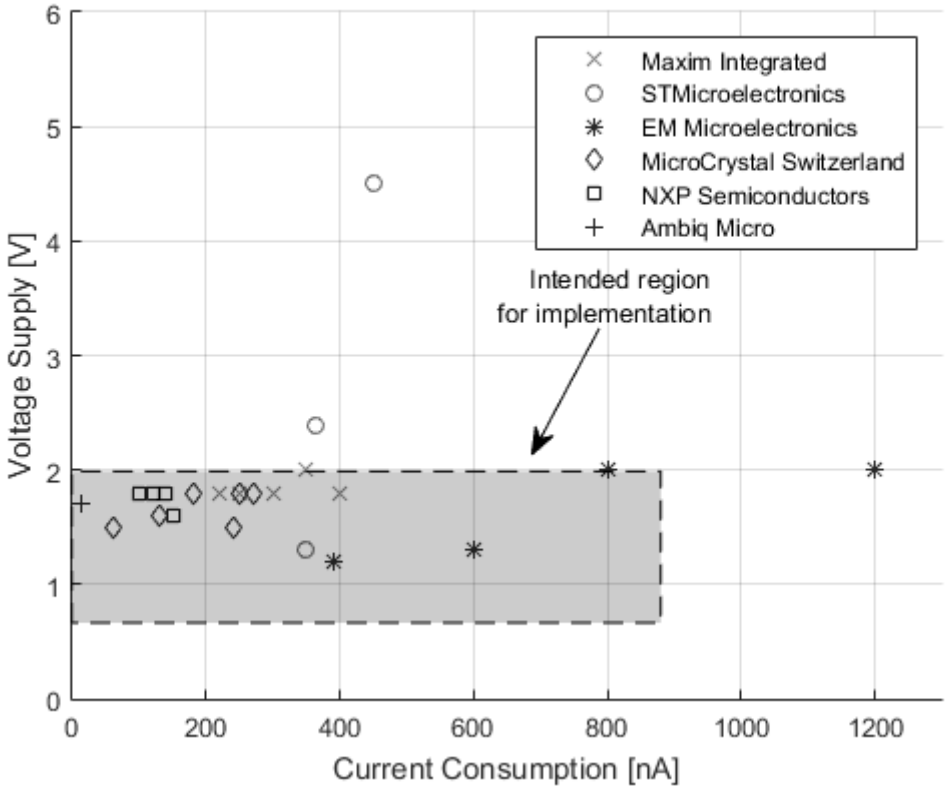


Figure 3.3: Minimum Voltage Supply vs Current Consumption in RTC ICs from table 3.2

3.2 Oscillators

Since most of the time the integrated circuit will be in timekeeping mode , most of its operation will be performed by the oscillator component. **Frequency change in ppm** (*parts per million*) is an important figure of merit since it describes how the oscillator deviates from the nominal value.

For the intended oscillator, the operational frequency should be **32.768 kHz**. This value is a power of 2 (2^{15}), and so the divider component can manage the intended frequency by manipulating only a 4 bit register. This lower frequency also allows for a lower power consumption of the oscillator component, further improving the expected results. This value is chosen for comparison reasons XO types of implemented RTC since this is the most used component in the oscillator industry due to its compromise between performance and cost [28].

3.2.1 Crystal Oscillators

Crystal oscillators (X0s) are exceptional frequency generators with low parameter variations in respect to supply voltage, process and temperature [29]. Another advantage is a low jitter noise compared to remaining oscillator architectures [30].

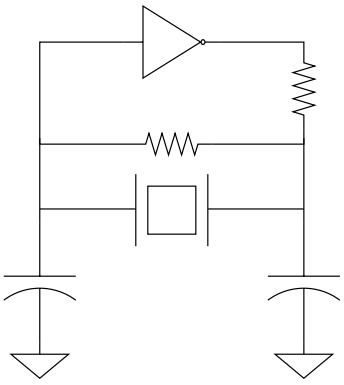


Figure 3.4: Conventional XO circuit [9]

As seen in figure 3.4, an inverter circuit in closed-loop amplifies the input noise to start the oscillation. Simultaneously, it provides a 180° phase shift and generates lost energy each period to maintain oscillation. The resistor forms a low-pass filter with the capacitor to avoid high overtone frequency oscillation. Also, a resistor is put in series at the output to control drive level and create a sinusoidal wave. This implementation, at low supply voltages, can not sustain oscillation due to loss of drive strength. It is a dependency since smaller oscillation leads to a smaller input signal.

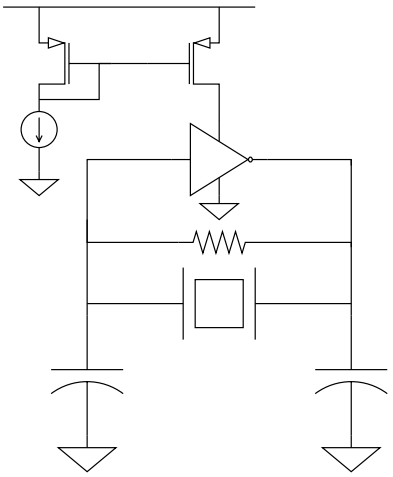


Figure 3.5: Widely used XO for low power circuits [9]

In figure 3.5, this is corrected using a circuit that controls the drive current through the source in the current mirror topology, reducing the amplitude of the oscillating signal. This also eliminates the need for a series resistor.

In [9], a circuit is proposed that implements a new XO architecture. This is developed using 180 nm CMOS technology, in an area of 0.3 mm^2. Voltage supply ranges from 0.94-1.82V and temperature variation is not a conditioning factor, since testing proved that frequency drift in ppm is not severely affected (-4.56 ppm to 133.3 ppm). Minimum power consumption is reported at **5.58 nW** at room temperature.

In [31], a self-charged XO (SCXO) is used to drastically lower power consumption, supply voltage and chip area. It is developed using 28 nm CMOS technology, implemented in an area of 0.03 mm^2. The SCXO itself only occupies 0.0028 mm^2 and the remaining space is used for the resitors and capacitors. Minimum power consumption is **1.89 nW** from a voltage supply of 0.15 V. Temperature deviation in ppm is reported as 48.8 ppm in a range of -20° to 80°C

In [32], an oscillator uses duty cycle to lower total power consumption from **2.1 nW** to **1.5 nW**, at the cost of an increased but negligible temperature deviation (1.87 ppm/°C in 0-80°C range, reaching -146 ppm at 80°C). With duty cycling, it reaches -150 ppm at 80°C). The circuit is implemented in 130 nm CMOS technology and occupies an area of 0,0625 mm^2.

Since our implementation requires a minimum sizing of less than a mm^2, a crystal will not be the best option to execute the work since it is bulky and expensive. A more compact alternative is necessary to create a low cost and low area solution to answer the current IoT nodes demands [33].

3.2.2 RC Oscillators

RC Oscillators and Relaxation oscillators operate in the same methodology. They function by charging a capacitor with a constant current and discharging it when it reaches a certain threshold voltage.

In [33], a RC Oscillator (RCO) is proposed, with a simple circuit that differs from a regular RCO (voltage mode) because it uses a current-mode architecture with a charge recycling integrator. Power dissipation is **54.2 nW** at room temperature with 0.85 V voltage supply. It is susceptible to temperature variation (99.5ppm/°C).

In [34], another RCO is proposed with a power consumption of **120 nW** on a voltage supply of 1V, with a small temperature variation in -40 to 90°C range (±2500 ppm). This is developed using 65 nm CMOS technology and the circuit occupies an area of 0,0032 mm^2.

In [35], an RCO is suggested that consists of an RC network, an inverting gain component from a resistor terminal to a capacitor point and another inverter gain element from the common resistor/capacitor terminal back to the resistor terminal. An advantage of this implementation is its ability to easily scale frequency. This was developed using 65 nm CMOS technology, occupying an area of 0,0015 mm^2 and achieving a power consumption of **190 nW**. Frequency stability is between ±1100 ppm and ±2100 ppm over the -20 to 90°C range.

3.2.3 Relaxation Oscillators

Another type of oscillators used in RTC applications are *relaxation oscillators*. These are favored against XOs because they do not require any external components and can be implemented in CMOS technology in a cheaper way. Besides, they draw less current than a XO oscillator, at the cost of a larger clock jitter. On the other hand, these are more susceptible to temperature variation [29].

In figure 3.6, the capacitor is charged with a current source (*Bias current* I_{REF}) and is reset periodically. A continuous comparator is used to trigger the reset signal, comparing the voltage in the capacitor terminal with a reference voltage (*VRef*). The inverter chain is responsible for the delay in the reset signal, allowing for a full discharge of the capacitor while reset is active. This produces a **sawtooth waveform** in the capacitor terminal and in the output of the comparator, with a output clock period of:

$$T_{period} = \frac{C_{INT} V_{REF}}{I_{REF}} + 2t_d \tag{3.1}$$

where t_d is comparator and inverter chain delay.

In [36], in order to address the temperature and supply dependency of the typical relaxation oscillator architecture, a constant charge subtraction circuit scheme has been developed. It achieves a power consumption of **5.58 nW** with a temperature stability of 45 ppm/°C, but operational frequency is limited to 11 Hz.

In [37], a typical relaxation oscillator is restructured in order to be area efficient. It achieves a power consumption of **271 nW**, in 1.1 to 1.3 voltage supply range. Temperature deviation is 135 ppm/°C. This circuit is developed using 65 nm technology and it occupies an area of 0,022 mm^2.

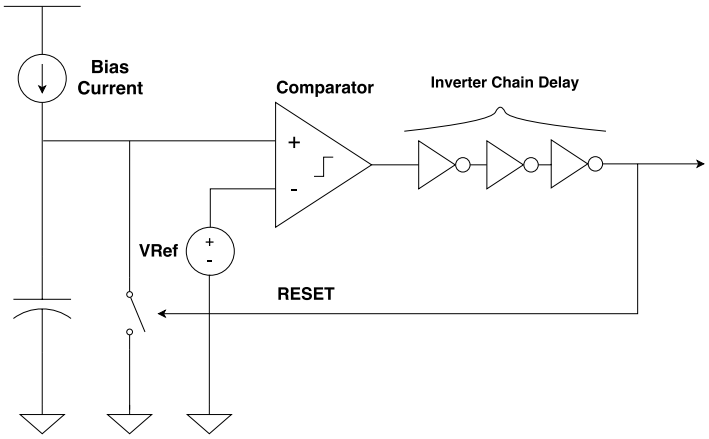


Figure 3.6: Relaxation Oscillator circuit [29]

In [38], a relaxation oscillator fully on-chip is implemented. At a supply voltage of 1 V, it achieves a power consumption of **472 nW** and an operational frequency of 32.55 kHz. This implementation adopts new compensation architecture to achieve a higher frequency output. It generates a stable oscillation clock pulse with a temperature deviation of 120ppm/°C.

3.2.4 Ring Oscillators

Another type of oscillators employed in real-time clock applications is the **ring oscillator** [39]. This topology is developed using an odd number of inverters in a closed feedback loop circuit. Although, at least 5 inverters should be used, an illustration of the typical implementation is shown in figure 3.7. In general, a ring with N inverters will oscillate with a frequency of:

$$fosc = \frac{1}{2Nt_p} \tag{3.2}$$

where t_p is the propagation delay of an inverters. This circuit also allows for a simple method of measuring the inherent propagation delay in an inverter circuit.

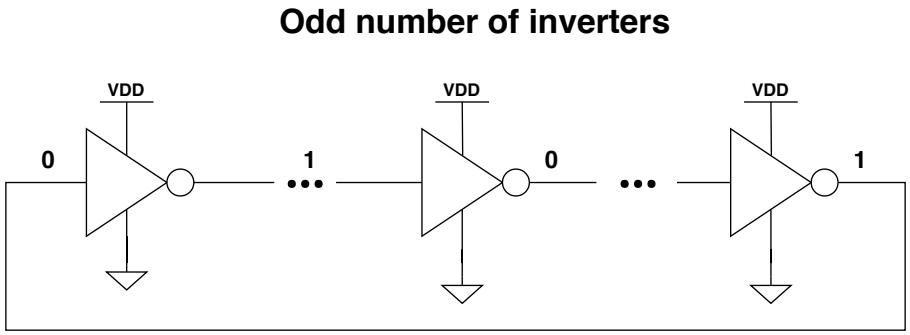


Figure 3.7: Ring Oscillator circuit [39]. The number of inverters should be around 7 or 11, or even higher.

In figure 3.8, a current starved ring oscillator (CSRO) solution is proposed. V_{CTRL} is assumed as:

$$V_{CTRL} = \sqrt{\frac{f_{OSC} \cdot N \cdot V_{DD} \cdot C_{TOT}}{0.5 \cdot \mu_N \cdot C_{OX} \cdot \frac{W}{L}}} + V_{TH} \tag{3.3}$$

where f_{OSC} is the oscillation frequency, N is the number of inverters in the closed chain, V_{DD} is the supply voltage, C_{TOT} is the total load capacitor. The mobility carrier μ_N and threshold voltage V_{TH} are dependent on temperature then, consequently, V_{CTRL} is also dependent on temperature as follows:

$$V_{CTRL} = aT + b \tag{3.4}$$

where a and b are coefficients. These types of ring oscillators are widely used due to their stability in voltage and temperature variations.

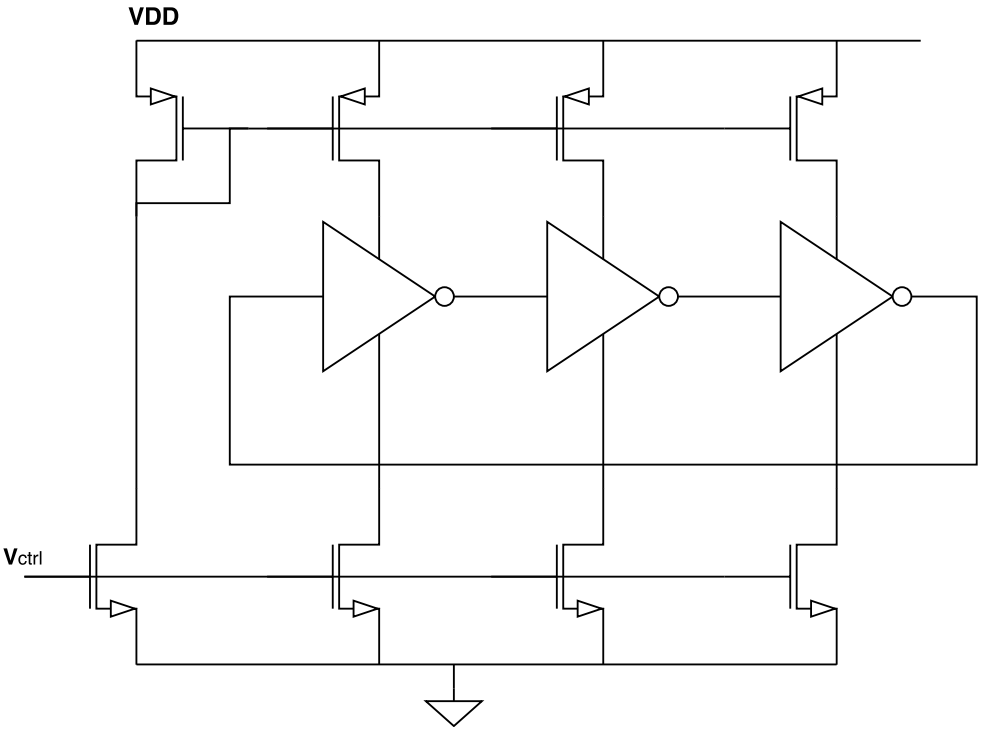


Figure 3.8: Current Starved Ring Oscillator circuit [40]

In [41], an ultra low power voltage controlled ring oscillator (*VCRO*) for a passive RFID application is given. The VCRO occupies an area of 500 μm^2 and has a power consumption of **3,6 nW** at a voltage supply of 140 mV. This implementation uses quasi-floating gate (QFG) techniques, allowing for an oscillation with a low supply voltage.

In [42], the inverters are substituted by a delay cell, with a biasing network and an output buffer. Altough power consumption is **2.01 mW** at a supply voltage of 1 V, this device is used for Bluetooth applications, with an operating frequency of 4.9 GHz. As demonstrated earlier, power consumption can be lowered with a smaller frequency.

In [43], a temperature sensor using a current starved ring oscillator for IoT applications is presented. It works with a voltage supply of 0.2V with an overall power consumption of **3.75 pW**. This sensor is composed of 3 parts that converts the temperature signal to a digital code.

In [44], a current start VCRO is presented, with a topology that improves the output signal symmetry. It achieves a frequency range of 1.75 kHz to 10 MHz with a power consumption of **1 nW to 3.6 μW**, respectively.

For this implementation, the current starved ring oscillator is chosen because:

- Crystal oscillators are too big to be integrated in a small chip and have increased costs.
- LC oscillators are circuits used primarily in RF technologies and the implementation of an inductor component with a small area is extremely difficult. Besides, the oscillation frequency is obtained using:
$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.5}$$
showing that it is dependent of the capacitance and inductor value.
- RC and Relaxation Oscillators obtain their oscillation frequencies through a time constant generated by the values of a resistance and a capacitor.
- Current starved ring oscillators are VCO's that generate a constant frequency by manipulating a current. It also has a great integration capability since it is dependent on the propagation delay of CMOS transistors. Compared to the remaining topologies, it also allows for a more fine tuned oscillation frequency that can be easily trimmed for process corners by changing the current source CTAT and PTAT value.

Chapter 4

Proposed Architecture

Taking into account the different theoretical considerations regarding the intended work to be done, the implementation of the Real-Time Clock will be performed using the topology as seen in figure 4.1. This modular methodology increases the independence of each component and makes it so that each part can be used for different purposes. The final integration of the whole project is specified in chapter 7.

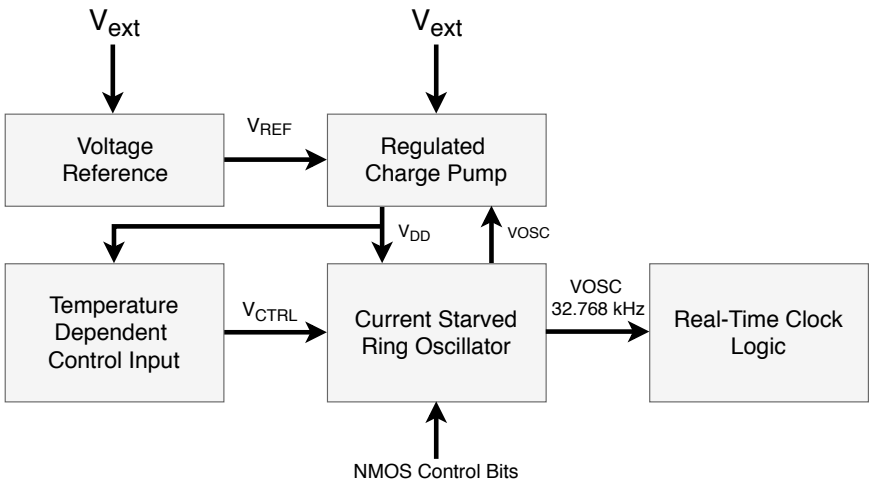


Figure 4.1: Overall schematic block of the final circuit implemented

The circuits will be described independently throughout the following sections, showcasing the different methodologies for the intended implementation. They can be divided in two different domains:

- **Analog design** that is responsible for the development of the Voltage References necessary for the functionality of the circuit, the regulated charge pump for a voltage supply stability, the voltage control for temperature compensation and the oscillator, that provides a stable signal output with a specific frequency as a digital input for the intended logic;

- **Digital design** that handles the input frequency clock and generates the Real-Time Clock functionalities (time counting, alarms and interrupts), mainly done developing a verilog circuit;

Digital power consumption is inherently low power since the clock signal will be provided by the implemented current starved ring oscillator. As seen in (2.2), dynamic power consumption is proportional to clock frequency. By using a value such as the objective (32.768 kHz), low power digital circuitry is achieved. Since the main objective of this work is to develop an ULP circuit, the analog component of the system is the main endeavor of the implementation. Transistors operating with low current values have an increased sensitivity towards PVT variations.

- **Process variation** derives from the different corner processes that describe different speeds for NMOS and PMOS devices, resulting in different current values and different threshold voltages.
- **Voltage variation** comes from the supply voltage. The current available for each transistor varies if the supply voltage also changes, since an external battery value deteriorates over time.
- **Temperature variation** occurs because of the inherent properties of each device. Transistor parameters (threshold voltage V_{TH}, carrier mobility μc and thermal voltage U_T) display a deviation with temperature changes. This is further escalated when low current values are used for implementation.

An oscillator operating in this region is a challenging task to stabilize for different temperatures, voltage supply variation and process variability.

4.1 Analog Topology

The analog circuit in this work can be described in two parts, as seen in figure 4.2:

- **Power Management Unit** that is responsible to feed the oscillator a stable voltage supply V_{DD} that is independent of the V_{EXT}, the external voltage supply. This circuit must be able to achieve the same supply voltage for the internal circuit even when the external battery starts to deteriorate over time.
- **Temperature and Process Block** that overcomes the oscillating frequency deviation according to a signal V_{CTRL} that is designed to compensate the temperature variation. The process homogeneity is achieved through a trimming section inside the oscillator's schematic;

The main objective of the final analog design is to develop a structure that allows for a stable oscillating frequency that is independent of all process, temperature and voltage variations.

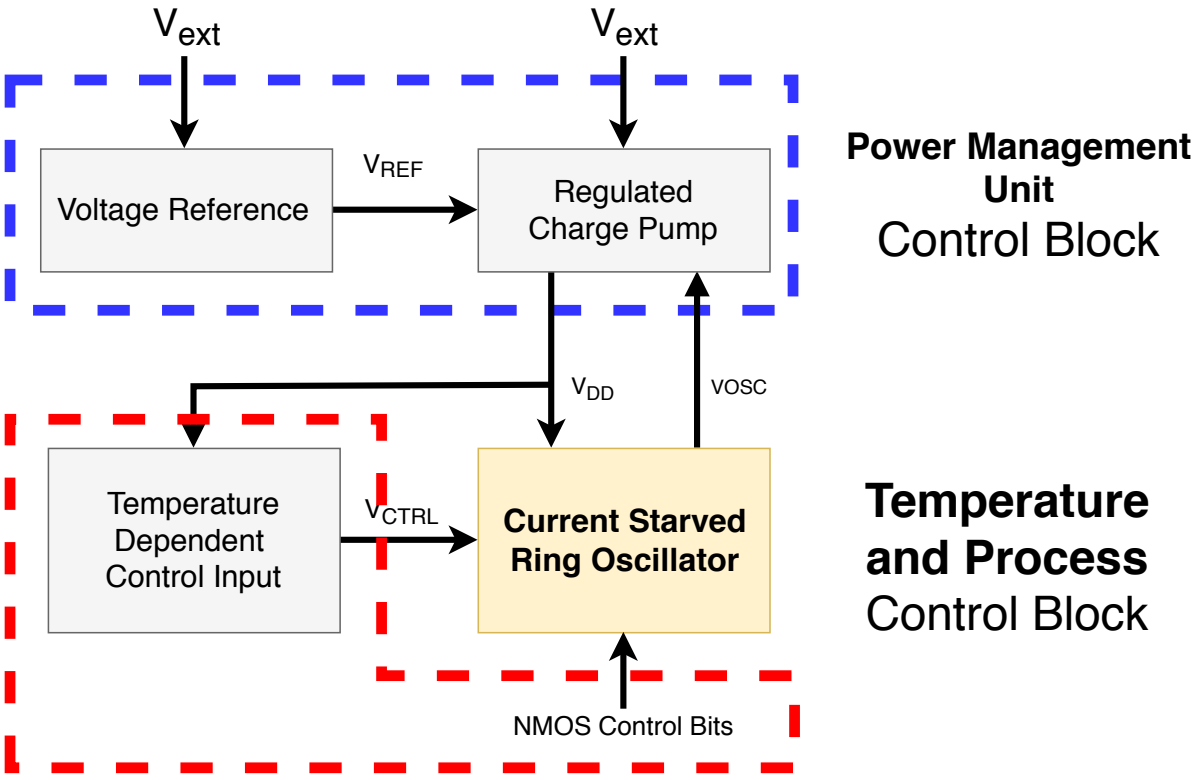


Figure 4.2: Analog blocks for implementation

4.2 Digital Implementation

For the digital design, a simple Real-Time Clock was developed using Verilog code. The main components of the developed work can be seen in figure 4.3. The main clock signal is provided by the current starved ring oscillator and this implementation has some extra functionalities besides time counting like alarms (that output a *high* value when time has reached a set value) and interruptions (periodic alarms, outputs a *high* value every pre defined time period). The implemented design also accounts for leap years and counts the time according to this parameter.

The digital implementation has a structure to count time from a set value that can be changed. It also has a set of auxiliary registers for specific alarm values and interrupt intervals of time that can be specified from the user as suited for the intended application. This is achieved through a setup input that has 2 bits. In table 4.1, the operating modes of the RTC are described.

Table 4.1: RTC Operation Modes

Setup Input	Operation Mode
00	*Normal*
01	*Setup Time*
10	*Setup Interruption*
11	*Setup Alarm*

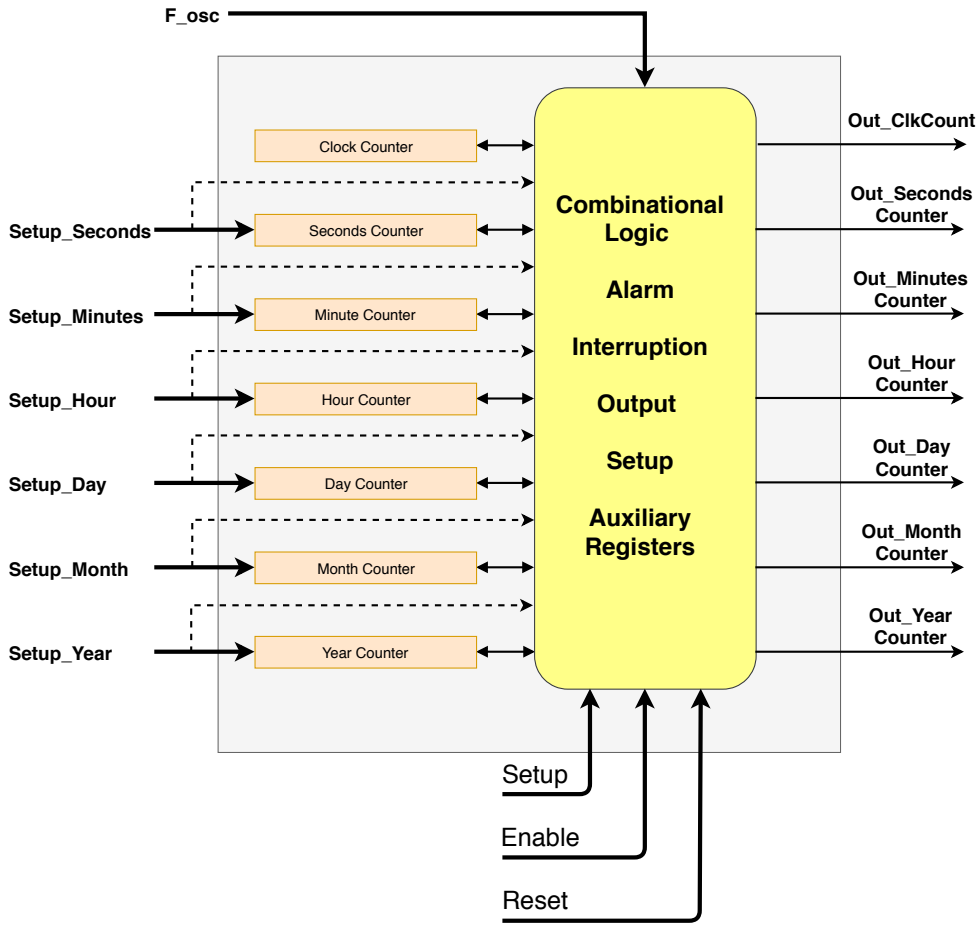


Figure 4.3: RTC digital blocks

- *Normal* - In this mode, the RTC keeps its normal functions. It keeps track of time spent and, if interrupt or alarm flags are activated, it checks for these situations to output corresponding values if needed.

- *Setup Time* - When the RTC has this set value in setup input it stops counting time and changes the actual value from all counter registers to the values from the time setup inputs. These time setup inputs are seen in figure 4.3 (setup_seconds, setup_minutes...) and all are connected to the registers from the counters.

- *Setup Interruption* - This state updates the auxiliary register values inside the RTC dedicated to the interruption functionality with the value from the time setup inputs. This also activates the interruption flag, enabling the interrupt output to be set to high when the specified values are reached. The circuit is still in time keeping mode.

- *Setup Alarm* - In this mode, the auxiliary register values dedicated to the alarm process are updated with the value from the time setup inputs. This also activates the alarm functionality by setting the alarm flag to high. The circuit is still in time keeping mode.

When the reset input is set to high, the seconds, minutes, hours and year counters plus the interrupt, alarm flags and their auxiliary registers are set to 0, while the day and month register are set to 1. The *startup* and output year registers are set to 1990. The *startup* year register is a value that allows for a lower input number of bits to specify the desired year, specifically 7 bits. So, the output year is described as the sum of the start-up year register plus the year counter. In a more specific example, if the intended year is 2018, the value of *setup_year* must be 38. The maximum year available in this topology is 1990 + 128 = 2118.

Both the reset and the setup modes can be seen in figure 4.4. As seen in this transient analysis, timekeeping mode only is enabled when the input *enable* bit is 1 and the setup is different from the Time Setup mode. In this regime, the counter values from the setup are updated to the values in the setup inputs. For interrupt and alarm setup, timekeeping is still kept on.

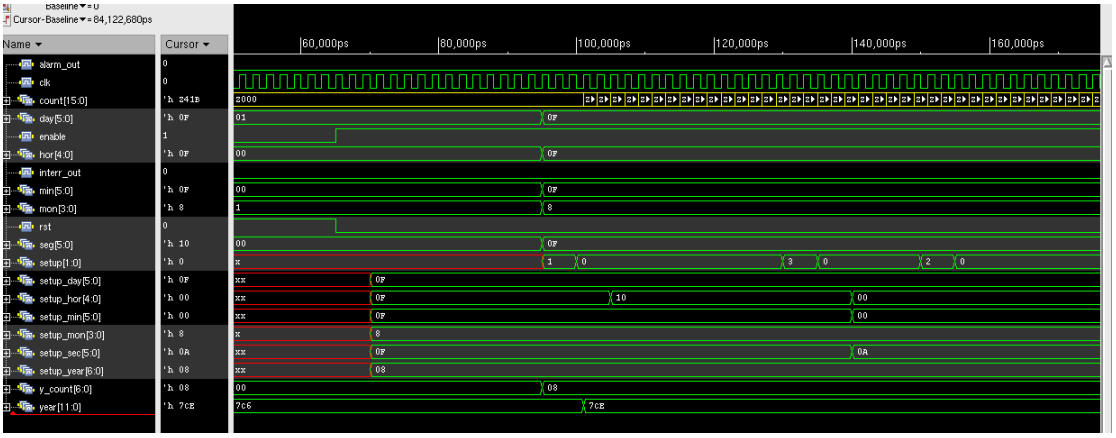


Figure 4.4: Setup and Reset verification

For the remaining functionality, each time there is a reset of the system or the year counter is increased, the circuit performs a set of functions to check if the year that it is currently on is a leap year or not. In this way, it specifies that when the counter reaches the end of month 2 (February), the final day is 28 or 27, depending if current year is a leap year or not (defined by the activation of the flag *leap_year*.

The input clock of the system is the frequency generated by the analog component of the overall system F_{OSC}, defined as 32.768 kHz. The clock counter register increases each time that this input is set to high and when it overflows (since clock counter is a register with 15 bits, the maximum available value to be represented is 32767) it increases the second counter and goes back to 0. After that, the same procedure is applied for the seconds and minutes counter (only when any of these two reach the value 60, the following counter is incremented) and the hour counter value is limited to 24. As per day values, they have to be calculated according to the current month and if the current year is a leap year or not.

For the interrupt functionality, an extra register is used to specify the needed interval of time in the seconds domain. The user defines an interval through the setup functionality, the circuit

transcribes to the seconds domain (*inter_value* and a counter *inter_aux* is initiated parallel to the seconds counter. When *inter_aux* is equal to *inter_value*, the system sets *inter_out* high and restarts the *inter_aux* for further time interruptions.

In figure 4.5, the test bench for this digital validation is set to input an interrupt value of 10 seconds. As such, the test bench first needs to place the values desired in the setup inputs array and then activate the corresponding mode. The auxiliary registers of the interrupt function are updated. And so, the circuit calculates, with the help from an auxiliary register, the amount of time elapsed and compares it to the set value. This is seen in the figure and makes it so that even if the remaining counters are changed, the interrupt interval is kept the same, as seen in figure 4.6.

The alarm functionality, when enabled, will set an output *alarm_out* high when the set time has been reached. After that, the alarm flag is set off and the system does not check for further alarms. This is seen in figure 4.6, where the test bench sets an alarm for a set hour, minute and second into its pre-defined alarm registers. This stored registers are then compared to the actual timekeeping and when they are equal, the RTC sets its alarm output to 1.

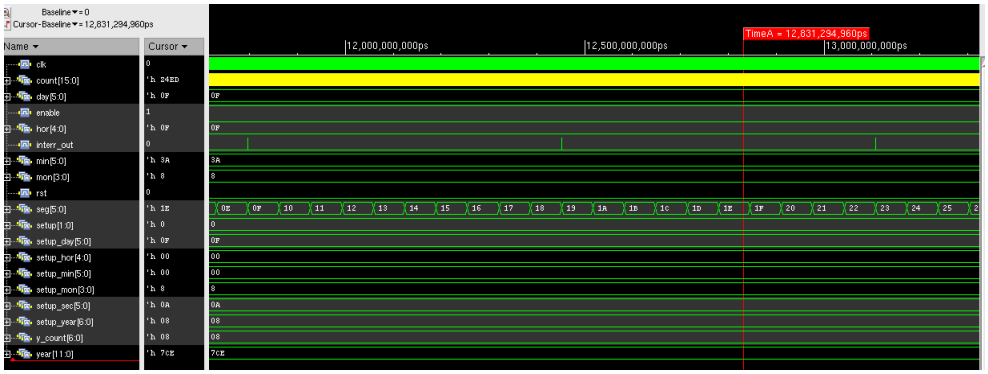


Figure 4.5: Interrupt Validation

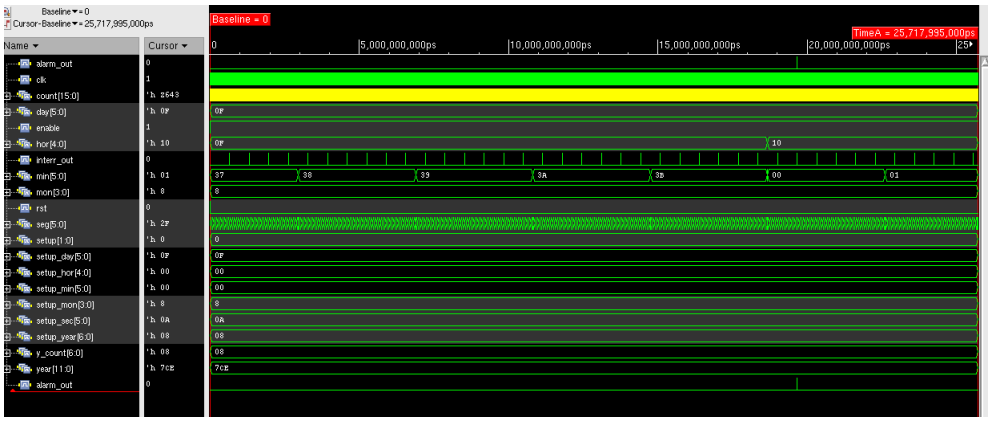


Figure 4.6: Interrupt and Alarm Validation

Chapter 5

Power Management Unit

The Power Management Unit is responsible to feed into the oscillation structure a constant voltage supply. Taking as its input an external supply voltage (such as a battery), it eliminates voltage supply variations (such as battery lifetime voltage depreciation) that may have been input into the oscillation system. In the design of this circuit, different parameters must be analyzed and described in order to achieve good performance for a specific operation point (PVT variations). The overall structure of the system is displayed in figure 5.1.

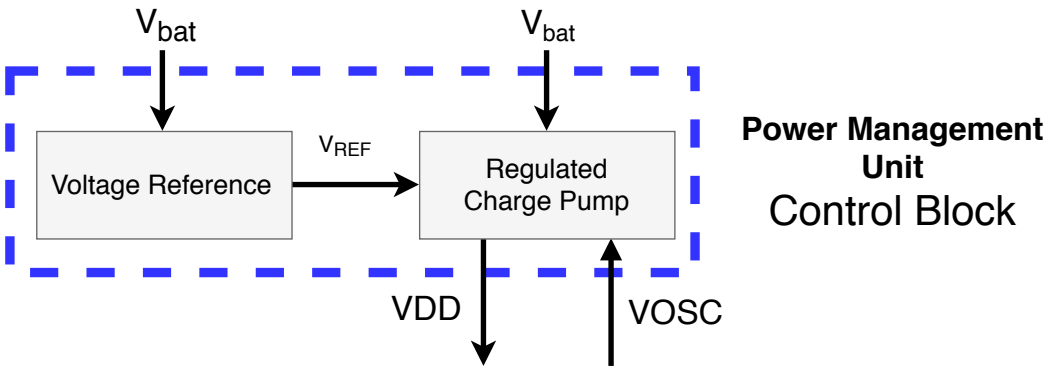


Figure 5.1: Power Management Unit diagram block

In the following sections, each sub-component (*Voltage Reference* and *Regulated Charge Pump*) of this block is described and analyzed. Different voltage references are used, each with a different purpose in the final implementation. The design considerations, simulation values and layout extraction simulations will be presented. Final verification of the overall power management unit is also displayed in the last section.

5.1 Voltage Reference

The Voltage Reference is a circuit that outputs a stable voltage value that in theory is independent of the input voltage supply and temperature [45]. For the performance analysis of a voltage reference, there is a need to measure its temperature coefficient, line regulation, power supply rejection ratio and power consumption.

Temperature coefficient describes the variation of the output voltage according to temperature. It is obtained using the *box method*, checking for the highest and lowest values of the output voltage reference as follows [46]:

$$TC(ppm/^{\circ}C) = 10^6 \left(\frac{V_{REF_{MAX}} - V_{REF_{MIN}}}{V_{REF_{@25^{\circ}C}}} \right) \left(\frac{1}{T_{MAX} - T_{MIN}} \right) \tag{5.1}$$

Line regulation is set as a function of the variation of the output voltage with the input voltage and is described as follows [46]:

$$Line\_Regulation = 10^6 \left(\frac{V_{REF@VIN_{MAX}} - V_{REF@VIN_{MIN}}}{V_{REF@VIN_{MIN}}} \right) \left(\frac{1}{VIN_{MAX} - VIN_{MIN}} \right) \tag{5.2}$$

The extension towards frequency variation of the line regulation figure of merit is the **Power Supply Rejection Ratio** (PSRR) that describes how much the output voltage varies if there is noise within the input voltage. It is calculated as follows [47]:

$$PSRR(dB) = 20 \left[\log \left(\frac{\Delta V_{IN}}{\Delta V_{OUT}} \right) \right] \tag{5.3}$$

Power consumption is calculated as follows:

$$Pcons(W) = V_{bat} I_{sub} \tag{5.4}$$

where the V_{bat} is the supply voltage derived from the external battery unit and I_{sub} is the subthreshold current flowing through the circuit. This is the main parameter to be optimized without compromising the values of temperature coefficient, line regulation and power supply rejection ratio.

In the following subsections, the proposed voltage references architectures are displayed and explained. Layout of each modular block is shown and its area is measured. Schematic analysis are performed and compared to layout parasitic extractions performances of the final circuit.

5.1.1 2T Voltage Reference

For this work, a subthreshold circuit has been implemented [45]. This implementation takes into account that the circuit is extremely simple (only 2 transistors are necessary, as seen in figure 6.2) and so its final area is decreased. Since it is operating in a subthreshold region, it allows for an ultra lower power consumption.

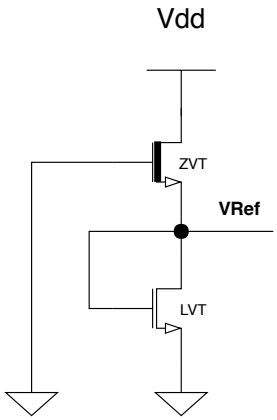


Figure 5.2: 2T voltage reference [45]

As seen in figure 6.2, this circuit uses two different types of NMOS: a near-zero V_{TH} transistor and a low V_{TH} transistor. Both of the transistors bulks are connected to the lowest voltage level in the circuit. The current flowing through both of them can be described using the known subthreshold equation from the EKV model and setting them equal as follows:

$$I_D = \mu C_{ox} \frac{W}{L}(m-1)e^{\frac{V_{GS}-V_{TH}}{nU_T}}(1-e^{-\frac{V_{DS}}{U_T}}) \tag{5.5}$$

$$I_{D1} = \mu_1 C_{ox1} \frac{W_1}{L_1}(m_1-1)e^{\frac{V_{GS1}-V_{TH1}}{nU_T}}(1-e^{-\frac{V_{DS1}}{U_T}}) \tag{5.6}$$

$$I_{D2} = \mu_2 C_{ox2} \frac{W_2}{L_2}(m_2-1)e^{\frac{V_{GS2}-V_{TH2}}{nU_T}}(1-e^{-\frac{V_{DS2}}{U_T}}) \tag{5.7}$$

substituting inside 6.6 and 6.7 with

$$m = 1 + \frac{C_d}{C_{ox}} \tag{5.8}$$

and equaling both equations we get

$$V_{REF} = \frac{m_1 m_2}{m_1 + m_2}\left[\ln\left(\frac{\mu_1 C_{d1} W_1 L_2}{\mu_2 C_{d2} W_2 L_1}\right)U_T + \frac{V_{TH2}}{m_2} - \frac{V_{TH1}}{m_1}\right] \tag{5.9}$$

This equation holds since the parameter $\left(1-e^{\frac{V_{DS}}{U_T}}\right)$ can be neglected for an error of less than 1% when V_{DS} is 5 ou 6 times higher than U_T for both transistors [45].

As shown in (5.9), the voltage output value is defined by the difference between both of the threshold voltages of the transistors. The temperature variation comes mainly from the logarithmic factor and the deviations of V_{TH}, since threshold voltage decreases as temperature increases. For the acquisition of the values, an extensive simulated-based research has been performed to address low values of temperature coefficient, line regulation and power consumption. According

to equation (5.9), setting $L_1 = L_2$, implies there is an optimal ratio value between W1 and W2 that equals the lowest temperature variation possible. And for lower power consumption purposes, the values of L_1 and L_2 are the highest available for this technology, i.e., $L_1 = L_2 = 50\mu m$.

This is shown in figure 5.3, for different values of V_{DD}. In this case, W1 was set as 10 μm to calculate different temperature coefficients according to different ratios with the equation in (5.9). This value was selected for a compromise between line regulation and power consumption. As we increase the value of W1, line regulation is slightly improved, but power consumption is also increased.

For the external input voltage supply, the assumed voltage level is set as 1.5V and as can be seen, significant voltage variations do not have a great impact on temperature coefficient. So for this values, this circuit achieves good line regulation values for a lower power consumption. As such, the chosen values for the transitor sizes are described in table 5.1.

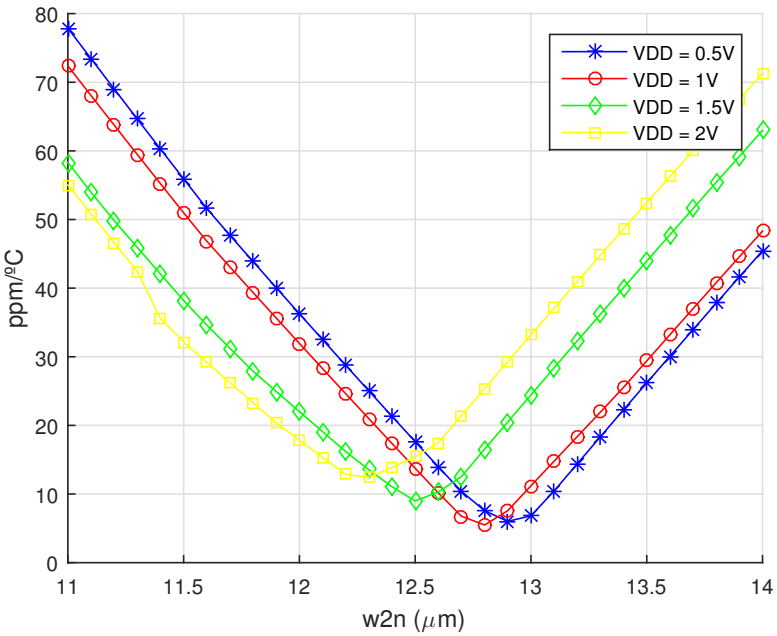


Figure 5.3: TC variation with W1/W2 ratio for 2T BGR

Table 5.1: 2T Voltage Reference Parameters values

Transistor Parameter	**Value** (μm)
W1	*10*
L1	*50*
W2	*12.5*
L2	*50*

For PSRR compensation, in figure 5.4, it is shown that as the output capacitance increases there is an improvement in the PSRR. After an analysis of the PSRR variations described in figure 5.4, a capacitor was added to the output, for the implementation of this work, with a value of 1 pF for a better input noise rejection. This value was chosen considering the improvements it gives towards a better PSRR, without occupying a larger area of the final layout. For layout considerations, a Metal-Insulator-Metal capacitor (MIM_CAP) was used because of its high capacitance density that allows for a reduction in fabrication costs and a more compact circuit [48].

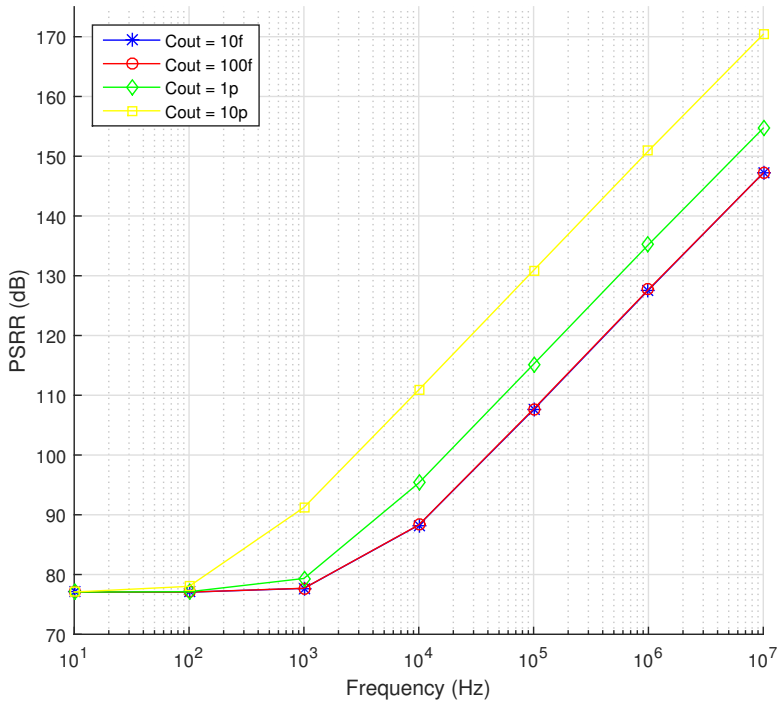


Figure 5.4: PSRR with different output capacitances

As such, the layout of the schematic is performed, the capacities of the nodes and resistances extracted. The layout is seen in figure 5.10. Total occupation area is 3684,7 μm^2. Results of this extraction are represented and compared with the simulated results and it is shown that the final layout circuit is validated, with similar results to the ones expected.

The simulation results versus the layout extracted values can be seen in figures 5.5, 5.6, 5.7, 5.8 and 5.9. The output voltage reference is measured according to supply voltage, temperature variations and different process corners. Power consumption is also analyzed for these parameters. The values for specific operating points are also shown in tables 5.2, 5.3 and 5.4.

This allows for a comparison of the values obtained through simulation and the values obtained with final parasitic extraction of the layout. This layout extracted values are represented as a dotted line with the same color of the corresponding parameter in a schematic simulation.

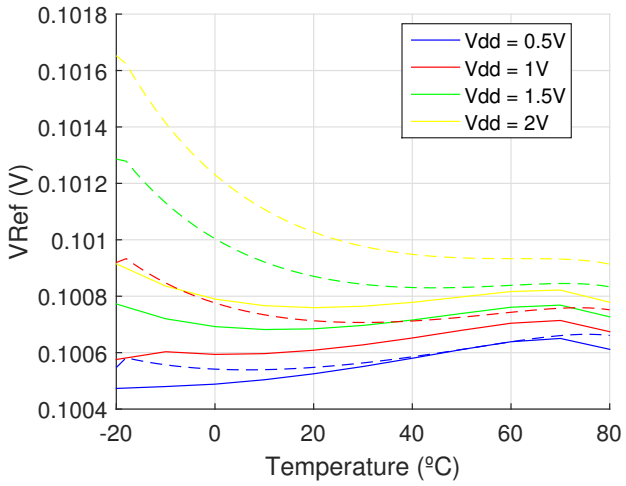


Figure 5.5: Output Voltage Reference versus Temperature

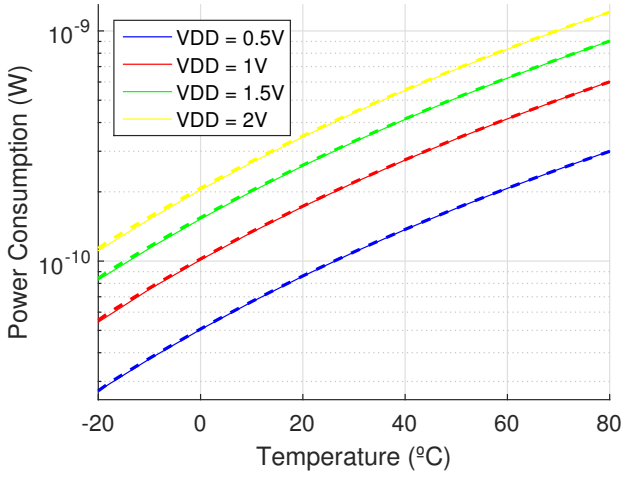


Figure 5.6: Power Consumption versus Temperature

Table 5.2: TC and Power Consumption comparison with Temperature

Supply Voltage (V)	**0.5**	**1**	**1.5**	**2**
TC (ppm/° C)				
Simulation	*17.63*	*13.75*	*8.991*	*15.4*
Layout	*12.53*	*22.46*	*45.24*	*73.15*
Power Consumption (pW) @ 25° C				
Simulation	*97.65*	*195.78*	*249.3*	*393.25*
Layout	*97.41*	*195.7*	*249.84*	*394.82*

As seen in table 5.2, the simulation obtains good temperature coefficient. As we increase the supply voltage, the temperature coefficient also increases. This schematic achieves a power consumption of 97.41 pW at the minimum supply voltage of 0.5V and 25°C, as is also seen in figure 5.5.

Analyzing the variation of power consumption as the supply voltage is increased, the exponential relationship between this parameters and I_{sub} is visualized, since for a fixed amount of ΔV_{bat}, the power consumption calculated with the equation in (5.4) is also dependent on I_{sub} that is responsible for this exponential increase. This can be visualized in figure 5.6, where the graphic displays a logarithmic scale for power consumption as temperature increases.

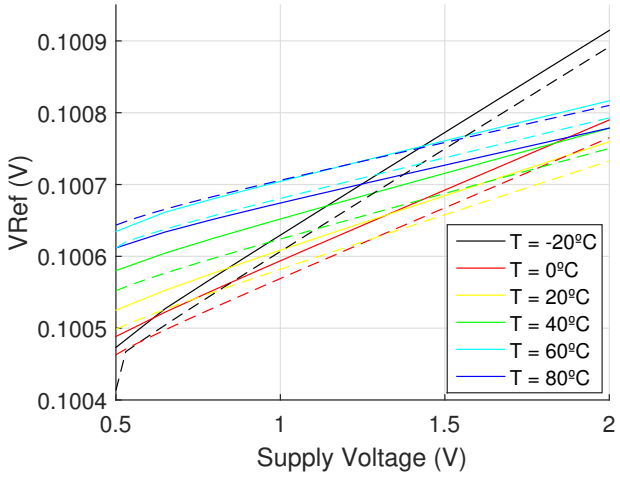


Figure 5.7: Output Voltage Reference versus Supply Voltage

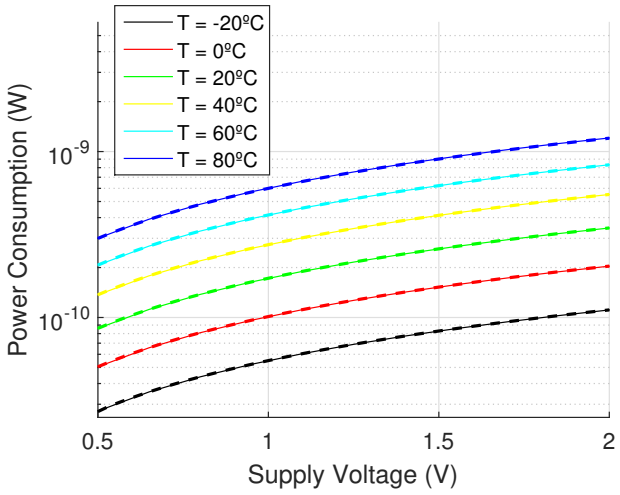


Figure 5.8: Power Consumption versus Supply Voltage

Table 5.3: Line Regulation and Power Consumption Comparison with Supply voltage

Temperature (° C)	**-20**	**0**	**20**	**40**	**60**	**80**
Line Regulation (%)						
Simulation	*0.293*	*0.2*	*0.155*	*0.131*	*0.121*	*0.111*
Layout	*0.318*	*0.201*	*0.156*	*0.131*	*0.12*	*0.11*
Power Consumption @ 1.5V (pW)						
Simulation	*82.88*	*152.45*	*259.14*	*412.77*	*632.32*	*904.64*
Layout	*82.9*	*152.48*	*259.2*	*412.8*	*632.17*	*901.42*

As seen in table 5.3 and figure 5.8, the exponential growth of the current with temperature is seen since power consumption increases drastically with a small increase in temperature. A variation in temperature between -20 °C and 80°C displays an increase higher than 100x the value achieved at the lower temperature.This sensibility is a a great challenge in the design of subthreshold circuits and careful considerations must be taken when designing for devices that require wide temperature ranges of operation.

Line regulation decreases as temperature increases and the values extracted from the layout simulation show a similar behaviour to the ones achieved with schematic simulation. For lower temperatures as -20 °C, the line regulation is higher and this can be visualized in figure 5.7, where the increase of the output voltage reference as the supply voltage is increased is significantly higher than other temperature values.

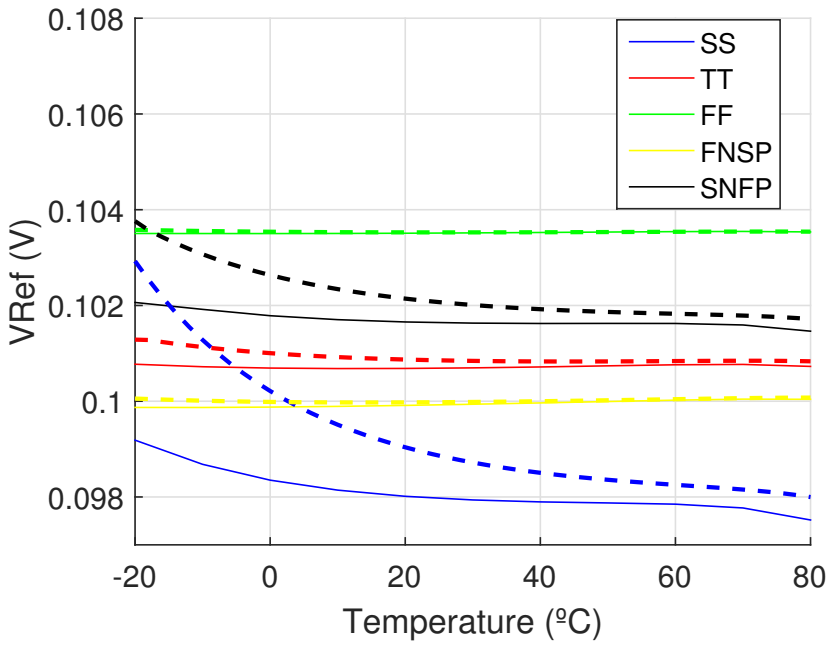


Figure 5.9: 2T - Output Voltage Reference versus Process Corners

Table 5.4: Process Corner results

Process Corners	**SS**	**TT**	**FF**	**FNSP**	**SNFP**
Temperature Coefficient @ 1.5V (ppm/°C)					
Simulation	*170.2*	*8.991*	*4.336*	*17.46*	*59*
Layout	*496.5*	*45.25*	*5.106*	*10.18*	*200.4*
Line Regulation @ 25 °C (%)					
Simulation	*0.433*	*0.148*	*0.096*	*0.109*	*0.245*
Layout	*1.154*	*0.294*	*0.126*	*0.173*	*0.589*
Power Consumption @ 1.5V and 25 °C (pW)					
Simulation	*61.55*	*294.3*	*1380*	*696.9*	*122.5*
Layout	*63.07*	*294.84*	*1378*	*696.5*	*123.7*

Process corners are a main factor of variation in the performance of the voltage reference. As seen in figure 5.9, there are higher output voltage variations in specific corners, SNFP and SS. This shows that the circuit has worse temperature coefficient and line regulation when its NMOS transistors are slower. In table 5.4, the values described show that for faster NMOS devices, in corners FNSP and SS, the values of line regulation and temperature coefficient are improved, at the cost of an increase in power consumption.

As seen in the analysis performed, this schematic is extremely reliable and insensible to temperature and voltage variations, even when operating in subthreshold regime. This shows that this circuit is a great voltage reference for an implementation for any IoT device.

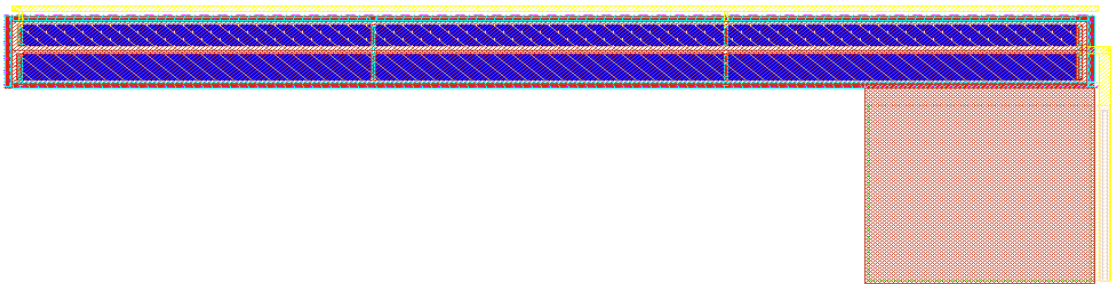


Figure 5.10: Layout of the 2T Bandgap Voltage Reference

5.1.2 6 Stages Voltage Reference

Since in our implementation we need a voltage reference for the regulated charge pump with an output supply voltage of 1.2V, the output voltage value of this component must be increased. This is achieved by increasing the number of stages as shown in figure 5.11. This methodology requires another circuit optimization and increases the minimum voltage supply for correct operation.

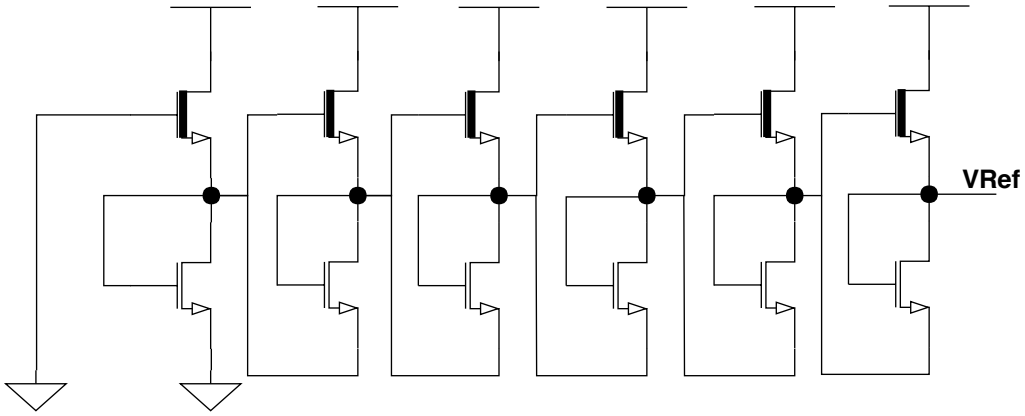


Figure 5.11: Voltage Reference with 6 stages

The same methodology as before was followed to estimate the values for the widths of the transistors. In this case, the current flowing through the transistors is increasing for each added stage, i.e., the current flowing through the transistor in the first stage is the sum of all the currents from the downstream stages and so on, as seen in figure 5.12.

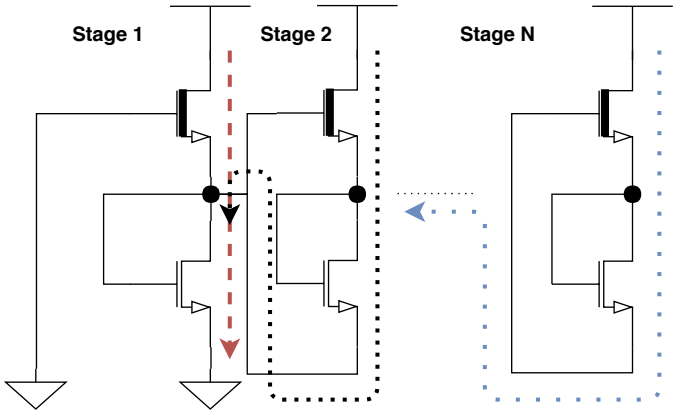


Figure 5.12: Current flow in the Voltage Reference with N stages

This requires that the width value is increased and the length decreased, to handle this current. Since they are operating in subthreshold region, the values for transistor sizing were obtained through an iterative simulation procedure, tweaking the values of L and W in order to obtain the best results for temperature coefficient, line regulation and power consumption.

For this case, the values of L for all the transistors in this circuit was set as $3\mu m$, to stabilize the current flowing through each stage. This means that the transistors are not long channel devices, as such, an analysis was made to achieve the best temperature coefficient for all process corners because it now has a greater impact on the output voltage temperature sensitivity. As seen in figure 5.13, for a set value of W1 = $25\mu m$, the lowest overall temperature coefficient value for all process corner is achieved with W2 = $83\mu m$. The sizes of this transistors are much higher compared to the 2T schematic solution proposed in the previous section

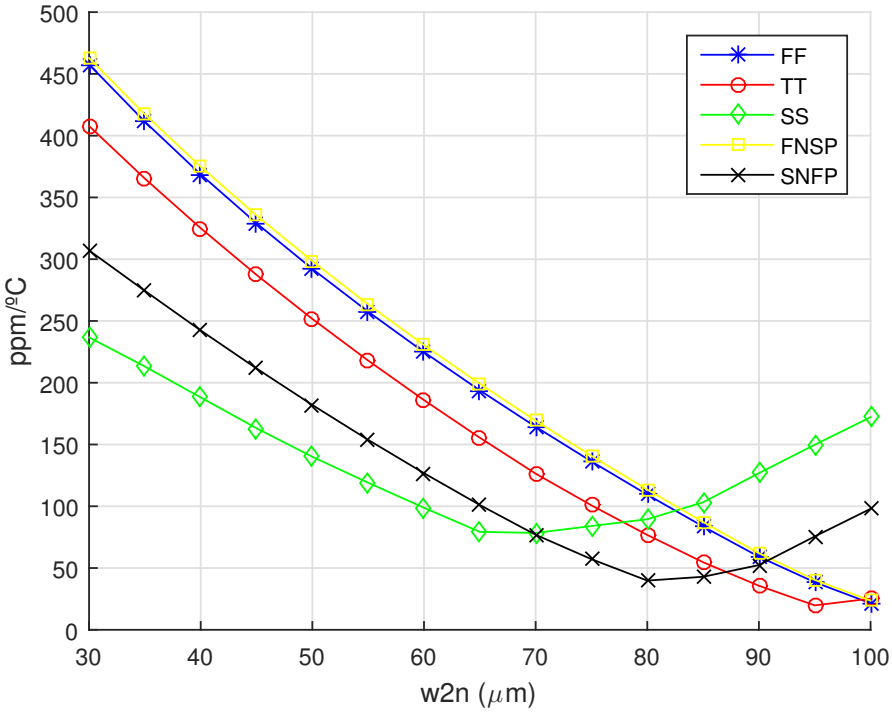


Figure 5.13: TC variation with W1/W2 ratio for 6 stages BGR

PSRR also was analyzed for this circuit, as seen in figure 5.14. As output capacitance increases, better PSRR values are achieved. Since the circuit transistors will occupy a bigger area, a value of Cout = 1pF is selected to improve circuit stability frequency wise without compromising overall area occupancy. The output capacitance used is the same as the one selected for the 2T reference voltage design.

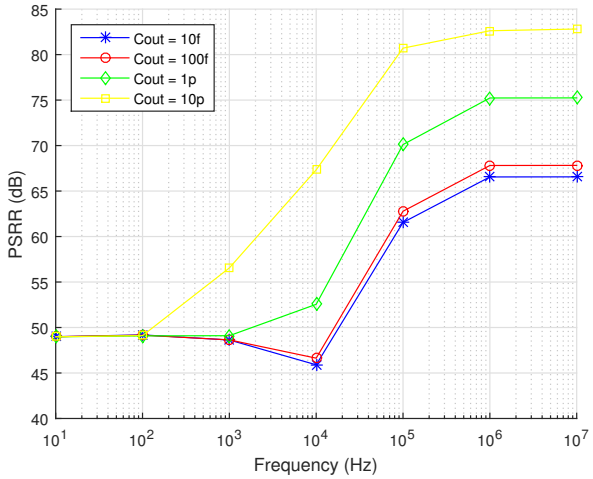
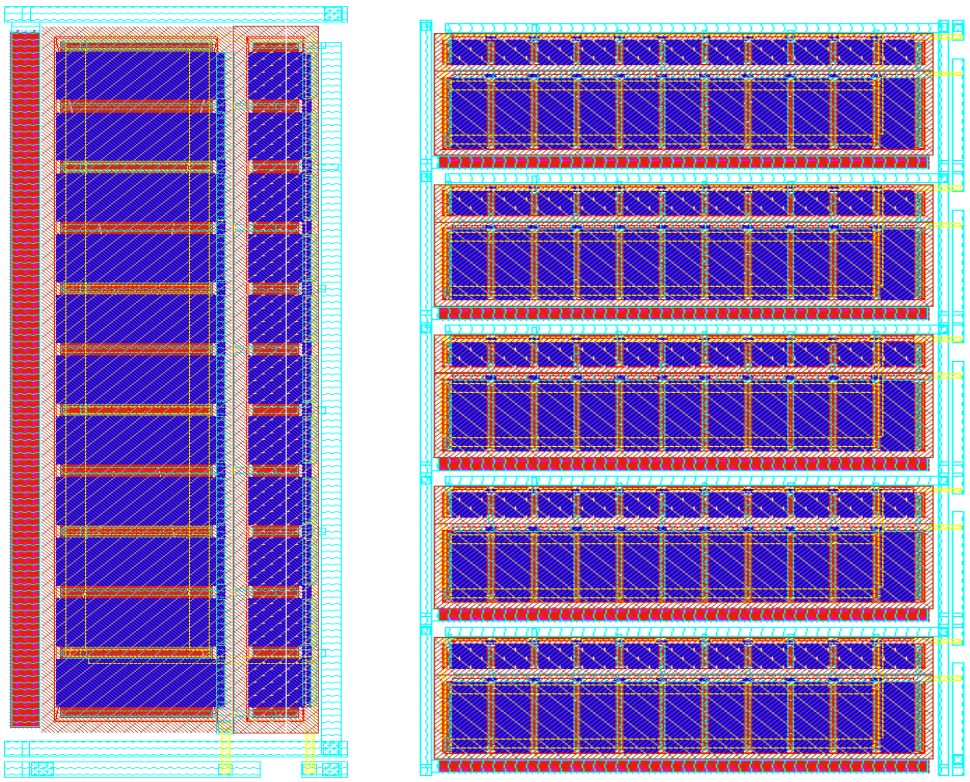


Figure 5.14: PSRR - Voltage Reference with 6 stages

In layout terms, a modular approach was used. Some steps were taken to improve transistor matching and layout symmetry. The different layout phases can be seen in figures 5.15 and the final layout version with the output capacitor is depicted in figure 5.16. Final layout area occupied by the circuit is 6299,7 μm^2.



(a) Single stage (b) 5 stages stacked

Figure 5.15: 6S Voltage Reference Layout stages

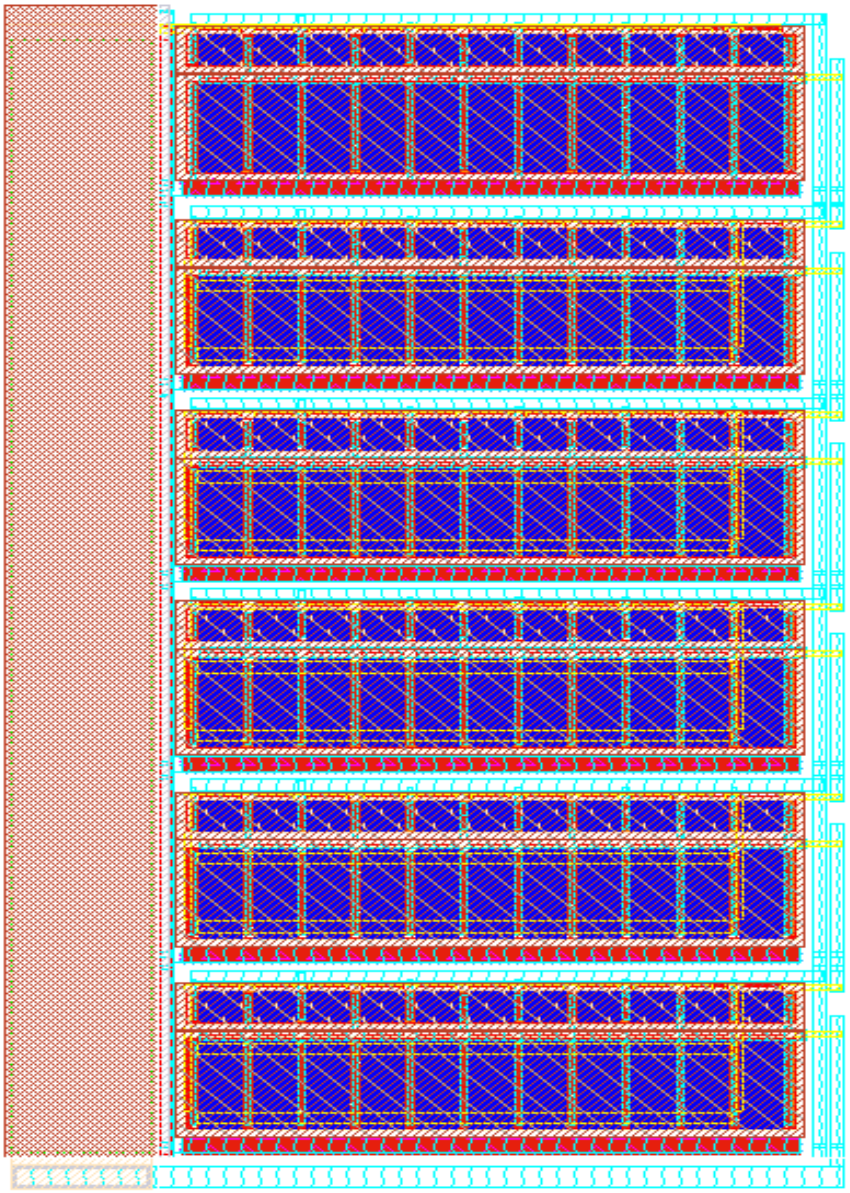


Figure 5.16: 6S BGR Final layout with C_{out}

For different values of input supply voltage (1V, 1.5V and 2V), a comparison is made between results achieved with simulated circuit and the circuit extracted with parasitic components from the final layout in tables 5.5, 5.6 and 5.7. Graphical view is also available for different supply voltages variation with process corner and temperature in figures 5.17, 5.18 and 5.19.

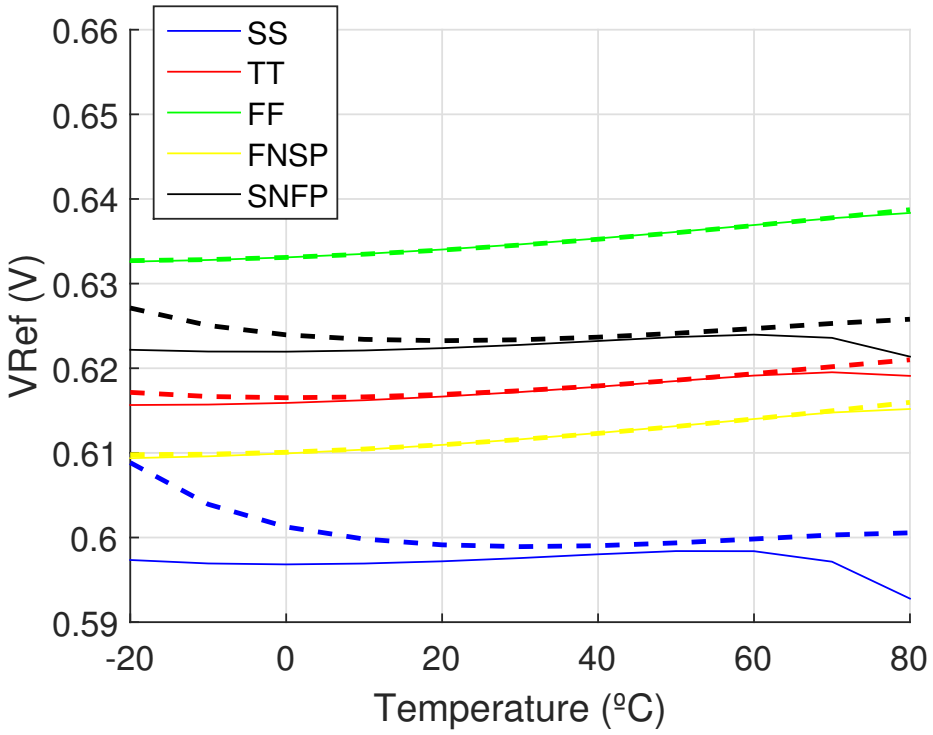


Figure 5.17: VRef vs Temperature @ VDD = 1V for different process corners

Table 5.5: Process Corner results @ VDD = 1V

Process Corners	**SS**	**TT**	**FF**	**FNSP**	**SNFP**
Temperature Coefficient (ppm/°C)					
Simulation	*93.97*	*62.75*	*90.67*	*95.03*	*41.74*
Layout	*165.7*	*72.67*	*94.88*	*101.1*	*61.97*
Power Consumption @ 25 °C (nW)					
Simulation	*3.963*	*19.77*	*95.18*	*48.03*	*7.961*
Layout	*3.974*	*19.78*	*95.2*	*48.05*	*7.972*

As seen in figure 5.17, for an input supply voltage of VDD = 1V, the values for the output voltage varies between 590 mV and 640 mV, for an overall process consideration. Minimum temperature coefficient is achieved for a TT process corner with a value of 72.67 ppm/°C. Corners SNFP and SS show an increase in output voltage levels at lower temperatures, contributing to the higher temperature coefficient values.

Considering power consumption values in table 5.5, the lowest values are achieved in the SS process corner (3.974 nW) but at the cost of an increase in temperature coefficient values (165.7 ppm/°C).

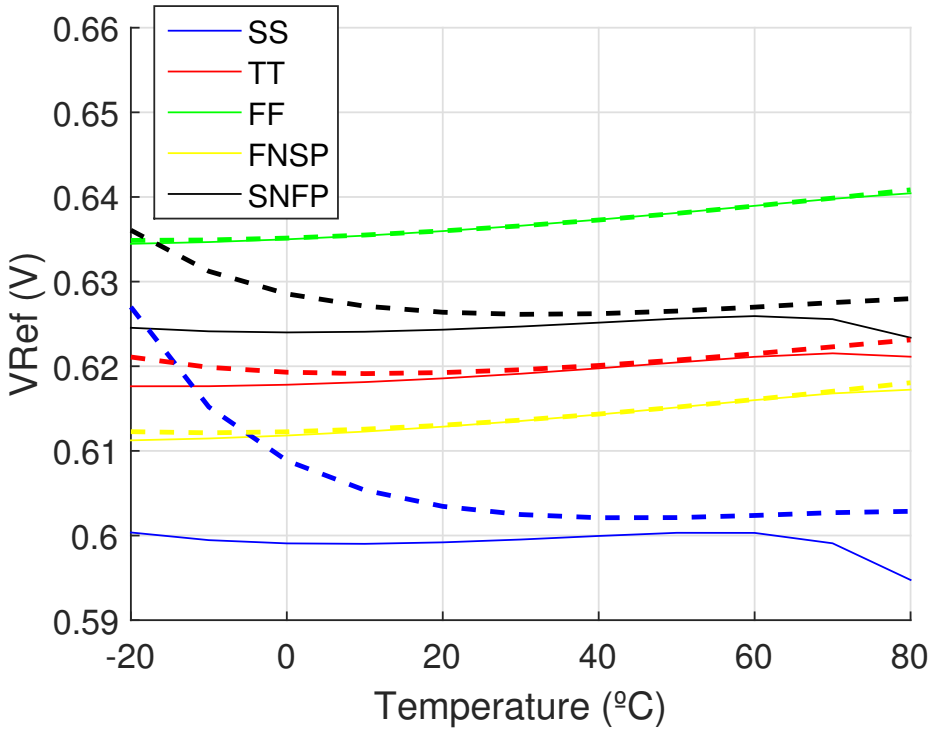


Figure 5.18: VRef vs Temperature @ VDD = 1.5V for different process corners

Table 5.6: Process Corner results @ VDD = 1.5V

Process Corners	**SS**	**TT**	**FF**	**FNSP**	**SNFP**
Temperature Coefficient @ 1.5V (ppm/°C)					
Simulation	*93.62*	*62.91*	*93.82*	*97.62*	*40.86*
Layout	*412.9*	*64.36*	*93.89*	*96.5*	*158.7*
Power Consumption @ 1.5V and 25 °C (nW)					
Simulation	*5.993*	*29.9*	*144*	*97.62*	*12.04*
Layout	*6.02*	*29.93*	*144*	*87.4*	*12.07*

As we increase the supply voltage value, SNFP and SS corners show an increase in the output voltage value, contributing to an increment in temperature coefficient when compared to the previous values achieved with a V_{DD} of 1V. The best temperature coefficient is achieved in a TT process corner 64.36 (ppm/°C) for a power consumption of 29.93 nW.

The lowest values of power consumption are again achieved with the SS and SNFP corners (6.02 nW and 12.07 nW respectively) at the cost of an increased value in temperature coefficient values (412.9 ppm/°C and 158.7 ppm/°C respectively). Compared to the power consumption with V_{DD} = 1V, an increase is expected for all process corners.

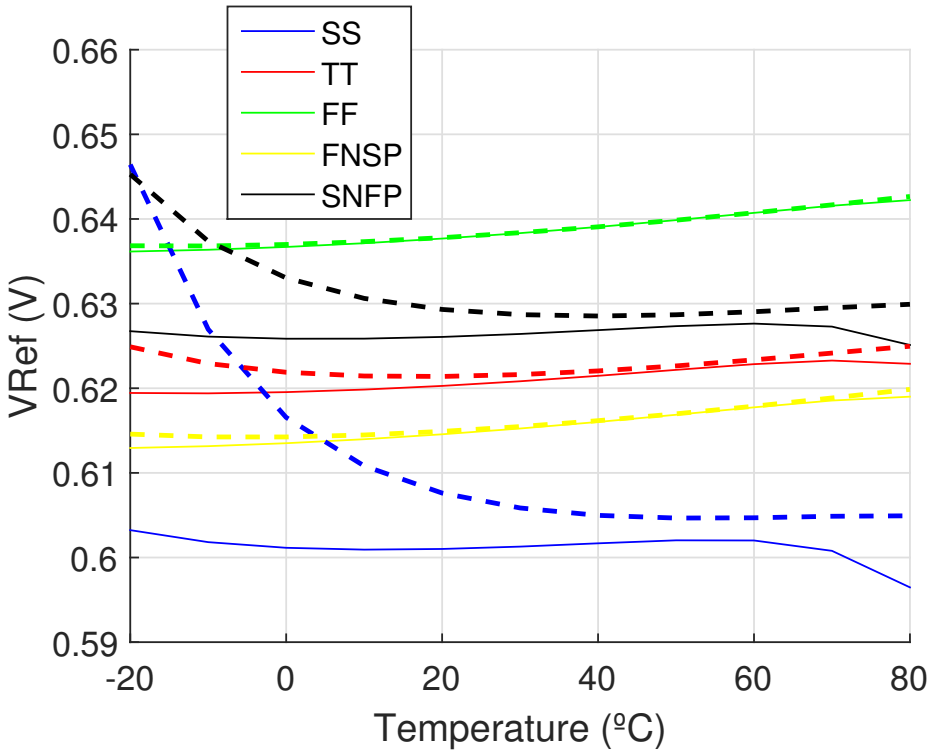


Figure 5.19: VRef vs Temperature @ VDD = 2V for different process corners

Table 5.7: Process Corner results @ VDD = 2V

Process Corners	**SS**	**TT**	**FF**	**FNSP**	**SNFP**
Temperature Coefficient (ppm/°C)					
Simulation	*112.5*	*62.45*	*95.27*	*98.6*	*40.33*
Layout	*688.3*	*57.43*	*91.64*	*91.4*	*266.1*
Power Consumption @ 25 °C (nW)					
Simulation	*8.052*	*40.18*	*193.5*	*97.3*	*16.18*
Layout	*8.101*	*40.23*	*193.5*	*97.67*	*16.27*

For a V_{DD} of 2V, higher voltage outputs are achieved, for the cost of an overall increase in power consumption. TT process corner power consumption at this supply voltage is 40.23 nW and when we compared it to the values achieved with V_{DD} = 1V (19.78 nW) we see a slight increase in this values. Temperature coefficient for the same TT case analysis is improved, reducing its value from 72.67 ppm/°C to 57.43 ppm/°C.

Lowest power consumption is again achieved with process corners SS and SNFP but a substantial increase is seen with temperature coefficient, showcasing the exponential relationship between supply voltage and temperature variation.

Comparing the results, the layout extraction has similar values to the simulated ones and the overall circuit shows good temperature coefficient for different supply voltages and different process corners. Some extreme values are found for SS and SNFP corners, the values where the NMOS devices are slower. Power consumption is also in the nW range, making it a viable voltage reference for an IoT device. This 6 stage voltage reference will be used as the reference voltage for the positive input of the operational amplifier inside the regulated charge pump component, delivering a temperature and supply voltage independent reference for the implementation of the device and correct operation.

5.2 Regulated Charge Pump

For the voltage input independence of the current starved ring oscillator, a typical charge pump topology is used to achieve a constant voltage supply. This schematic is seen in figure 5.20 and it is composed of an input external voltage source V_{DD}, 5 switches, a transfer capacity known as the *flying capacitor* C_F, an output capacitor known as the *reservoir capacitor* C_R, a voltage divider for the negative input of the operational amplifier and an input clock that will be supplied by the own implemented current starved ring oscillator [49].

This voltage converter was selected due to its low cost, simplicity and low power. This topology also does not need inductors to operate, lowering the overall area occupation and compared to low dropout regulators, its power consumption and output current value is lower.

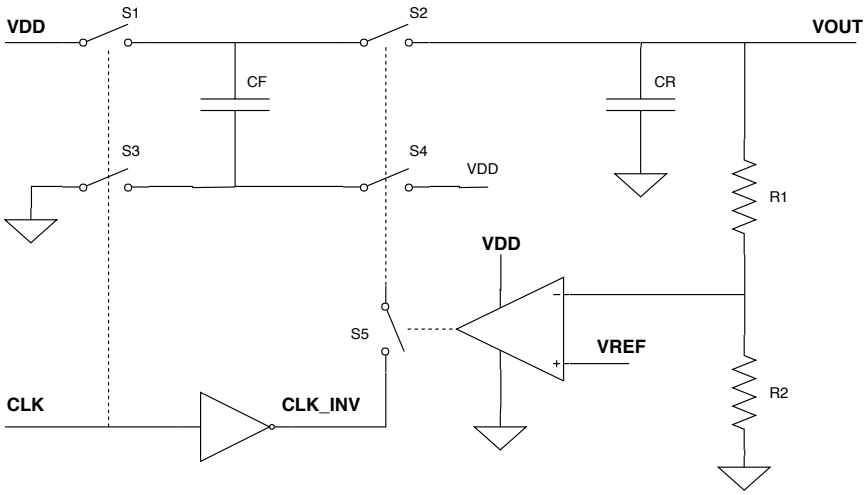


Figure 5.20: Regulated Charge Pump

This regulated charge pump has 2 operating points, *charging phase* and the *discharge phase*.

- **Charging phase** - occurs when the clock input signal is 1. S1 and S3 switches are closed, S2 and S4 are opened. The input supply voltage charges the flying capacitor to its value.
- **Discharging phase** - happens when the clock input signal is 0. S1 and S3 switches are opened, S2 and S4 are closed, depending on the value that the operational amplifier outputs, since it controls S5. If $V^- < V_{REF}$, then the S5 switch is closed, closing S2 and S4 and allowing for the flying capacitor C_F to transfer energy to the reservoir capacitor and the load, increasing the voltage value. If $V^- > V_{REF}$, S5 is kept open and the reservoir capacitor supplies the load with current and a voltage level. By defining R1 = R2, V_{OUT} will be $2 \times V_{REF}$ since:

$$V_{OUT} = V_{REF}(1 + \frac{R2}{R1}) \tag{5.10}$$

and so the desired output voltage is acquired.

Since the clock frequency output is 32.768 kHz, this will require larger capacitor values to account for this higher period increase, since the capacitor must have a sufficient value to hold the voltage level steady and not fully discharge in one cycle. This is seen in the following equation [50]:

$$\Delta V_{OUT} = \frac{I_{pump}}{C_L f} \tag{5.11}$$

where ΔV_{OUT} is the ripple voltage, I_{pump} is the pumping current from the flying capacitor, C_L is the load capacitor and f is the frequency switch between the charging and the discharging phase. To achieve a lower ripple voltage, a higher load capacitor is required for a small frequency. The flying capacitor value should be large enough to transfer enough energy to charge the load capacitor.

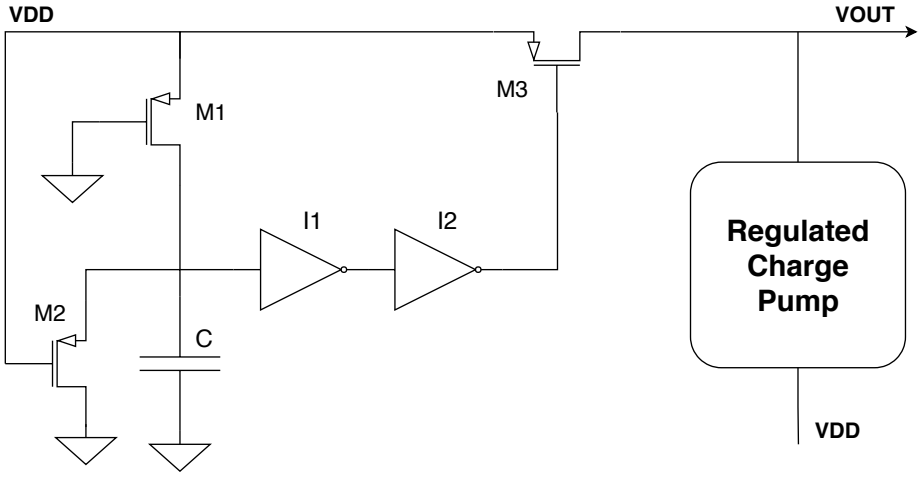


Figure 5.21: Startup Circuit of the Regulated Charge Pump

This self-biased schematic needs a circuit to start up the overall implementation. Since this charge pump requires that the oscillator is already working for the correct operation point, a bypass of V_{DD} is needed to achieve a start up oscillation that, in turn, will start the regulated charge pump, as seen in figure 5.21. When the circuit starts, M1 is always on and this current charges the capacitor C. The voltage value in C is 0 and I1/I2 place a 0 on the gate of M3. The inverters assure a stable turning point for the M3, not depending on the capacitor voltage value but on the voltage transfer characteristic of the inverters. Meanwhile, V_{DD} is bypassed to V_{OUT} and is the supply voltage of the oscillator component, starting the circuit. As C charges up, the voltage level in its terminal rises until the value is recognized by I1 as a *high* voltage level and M3 is turned off for the remaining of the operation. Since the oscillation in the CSRO has already started, the charge pump will dominate and regulate the V_{OUT} from that point. When the system turns down, to reset the capacitance value of C, it is discharged through the M2 transistor. In figure 6.22, the output signal of V_{OUT} is seen. As the voltage level reaches the required value, the charge pump takes over control of this circuit and establishes a regular voltage output.

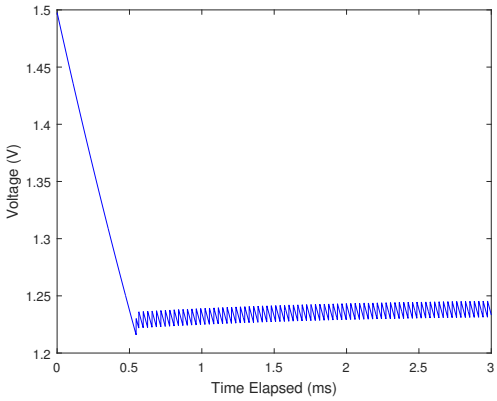


Figure 5.22: Startup of the Charge Pump

The switches are defined as transmission gates. The transistors inside the transmission gates in the charge pump and the startup circuit have the minimum size available for this technology.

The reservoir capacitor C_R is implemented as a MOSFET transistor operating as a MOS capacitor. The gate is connected to the output point, while the bulk, drain and source of the transistor are connected to the ground level. The layout of the circuit is seen in figure 5.23 and the total occupation area is 71971 μm^2.

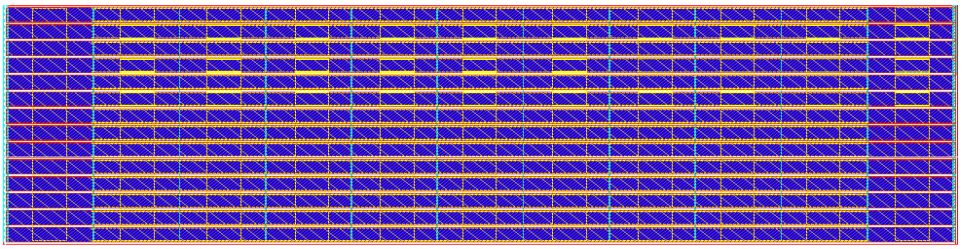


Figure 5.23: MOSCAP Layout

In figure 5.24, the layout of the voltage divider resistors is seen. The implemented resistors are interleaved so that any foundry defects affect both of the resistors and the overall functionality is not compromised. Since the values of R1 and R2 need to be higher than the output resistance seen by the charge pump, high resistance sheet is used. The total occupation area is 34216 μm^2.

The final layout of the charge pump is seen in figure 5.26. As shown, the majority of the area is occupied by the MOSCAP device and the resistors that implement the voltage divider. The 6 stages voltage reference is also seen. The output voltage is extracted from the layout circuit and is exhibited in figure 5.26. Ripple voltage is estimated to be around 14 mV, making this circuit a stable supply voltage source for the current starved ring oscillator that is going to be implemented.

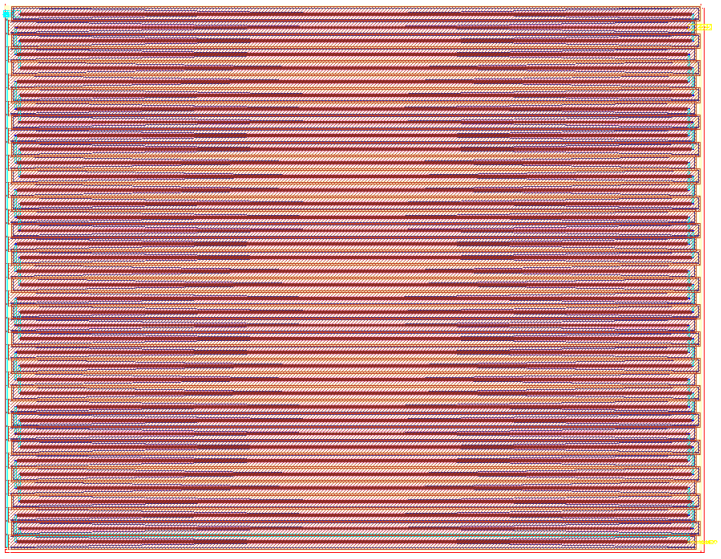


Figure 5.24: Resistors in the Voltage Divider Layout

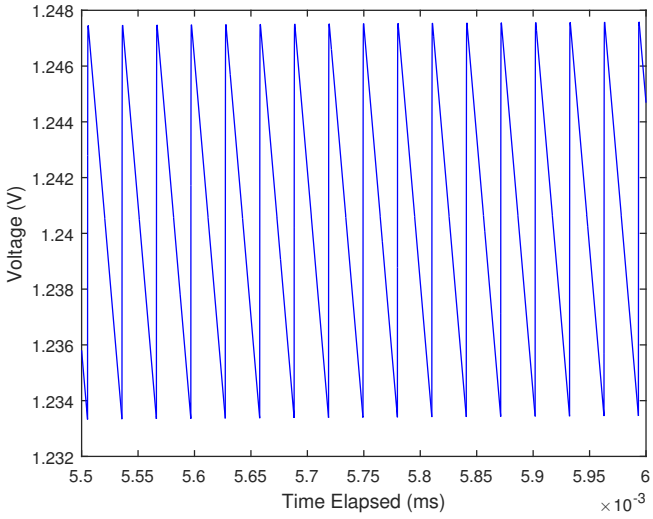


Figure 5.25: Output of the Charge Pump

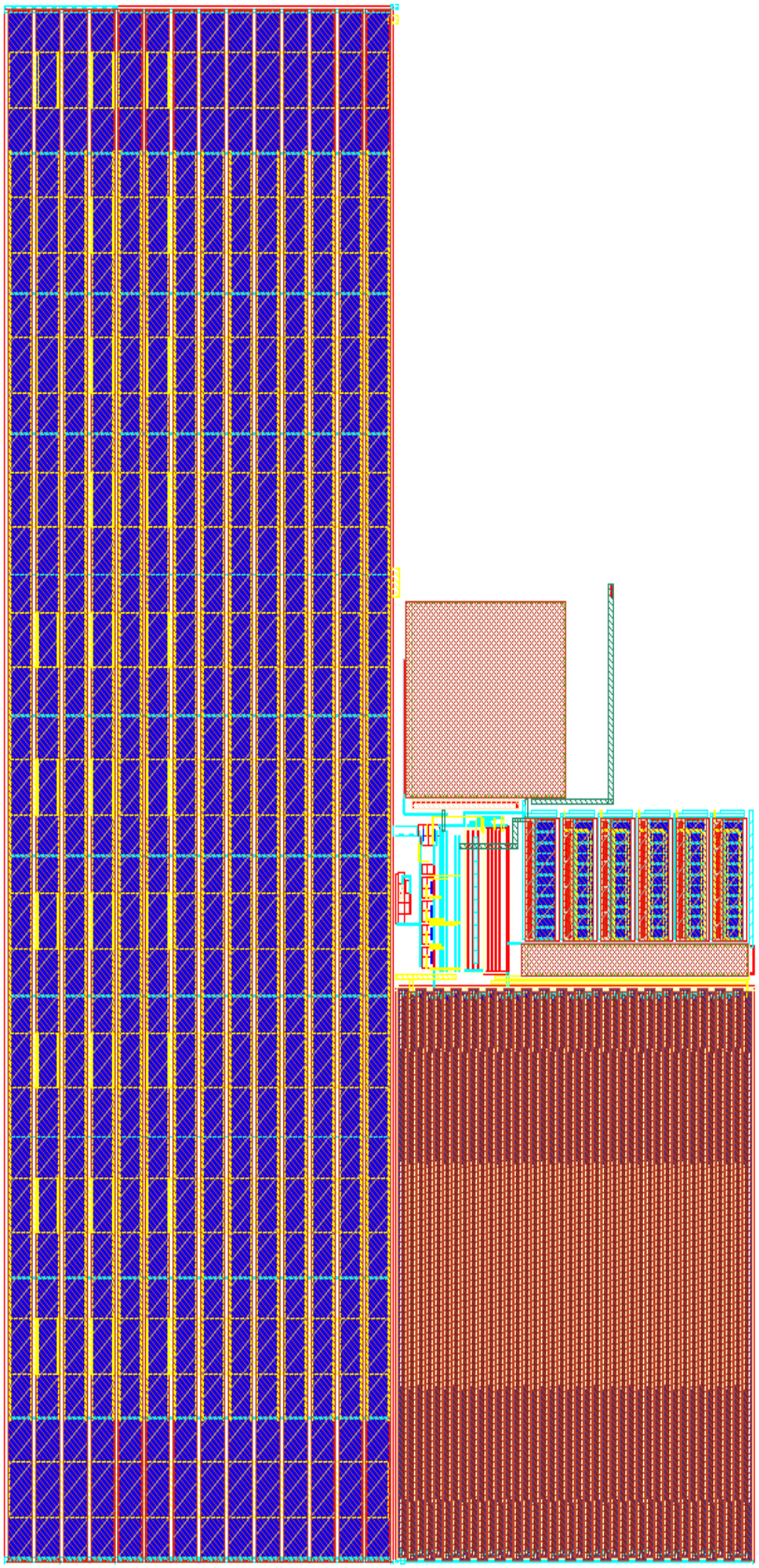


Figure 5.26: Final Charge Pump Layout

Chapter 6

Oscillator Design

As depicted in figure 6.1, this proposed oscillator design takes as its input a temperature and external supply voltage independent V_{DD}. The oscillator suffers from PVT variations and this is accentuated by the fact that the objective of this work is to achieve low power consumption. So, to achieve a stable oscillation frequency and not dependent on process, voltage and temperature variations, it must be compensated.

The temperature compensation is done through a temperature dependent V_{CTRL} that compensates for the PTAT variation of the output oscillating frequency. Process compensation is achieved through trimming with external control bits that activate or deactivate certain transistors to lower or increase the oscillation frequency as it will be explained further in this chapter.

All this structure surrounding the oscillator proposes to achieve a stable output frequency of 32.768 kHz, independent of supply voltage, temperature and process variation. The adopted design methodology also took into consideration ultra low power consumption for further integration of proposed circuit into an IoT device.

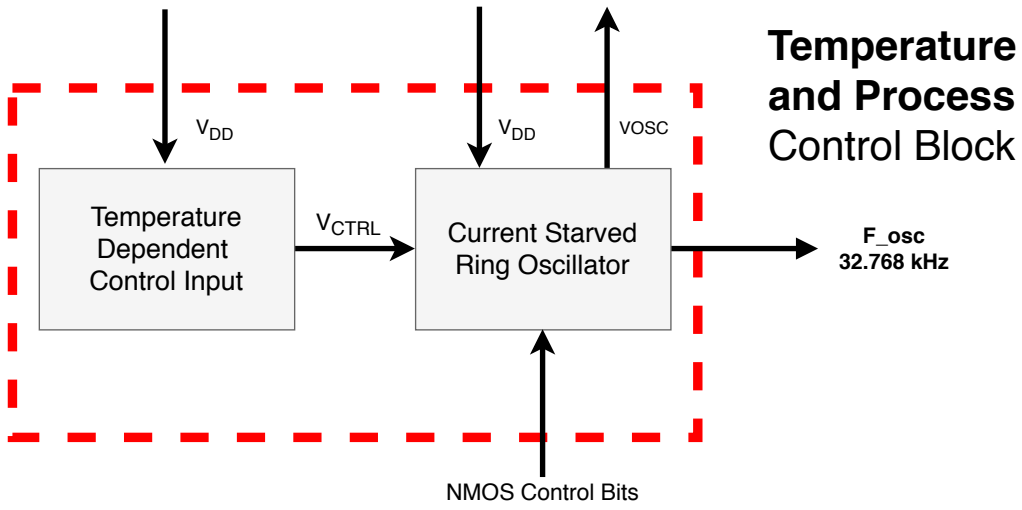


Figure 6.1: Oscillator block diagram

6.1 Current Starved Ring Oscillator

The oscillator topology that was chosen for the implementation of the proposed work is a typical Current-Starved Ring Oscillator, modified from [40] since the control voltage, in this case, is applied to the gates of the PMOS current source structure and the current flowing through each stage is mirrored from M_{N1} through the NMOS current sink structure [51].

$$f_{OSC} = \frac{1}{2Nt_p} \tag{6.1}$$

As seen in (6.1), the oscillation frequency is obtained by a propagation delay time t_p. This t_p is described as the propagation delay of a single stage and can be written as:

$$t_p = \Delta V \frac{C_{out}}{I_{starved}} \tag{6.2}$$

and substituting in (6.1) we get that

$$f_{OSC} = \frac{I_{starved}}{2N\Delta V \times C_{out}} \tag{6.3}$$

By setting a fixed value for C_{out} as an integrated capacitor with a value C, as seen in figure 6.1, and deploying a temperature and external voltage supply independent ΔV (in this case, VDD) through a regulated charge pump, we can see for a fixed number of stages (in this situation, N=3), the oscillation frequency is only dependent on the current available for each stage. The driver and signal restoration component takes as its input the oscillating signal from the delay stages and outputs a square wave with the same frequency value.

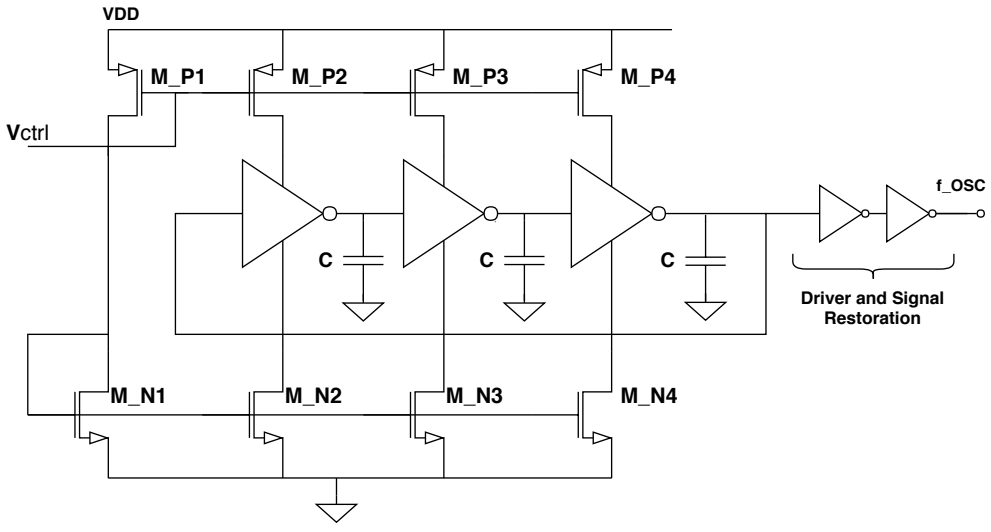


Figure 6.2: Proposed Current Starved Ring Oscillator circuit

This current $I_{starved}$ is the main parameter to be characterized in order to obtain a stable oscillation frequency. The current is defined by the first stage transistors M_{P1} and mirrored with M_{N1} through each stage. This value will be manipulated in order to eliminate the PTAT current value to obtain a stable oscillation frequency through a V_{ctrl} and to eliminate CTAT process variation through trimming in the M_{N1} transistor.

Analyzing figure 6.3, it is clear that frequency increases as temperature increases. This also means that by checking equation (6.3), it means that the parameter that is responsible for this increase is the current flowing, since remaining factors (N, ΔV_{DD} and C_{out}) are fixed values. So, to compensate for this increase in current, V_{ctrl} will also increase to lower the current flowing through each stage.

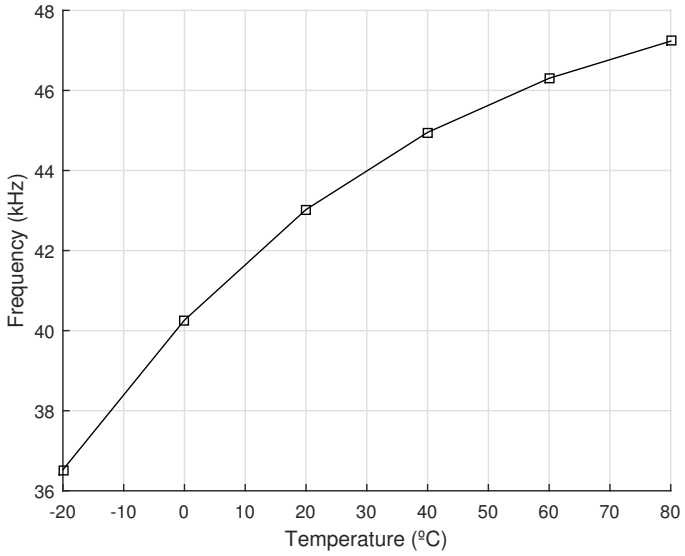


Figure 6.3: Frequency variation with temperature in the CSRO

6.2 Temperature Variation

To stabilize this current as temperature increases, a 2T voltage reference as described in figure 5.2 is used, with a specific ppm/°C parameter to compensate the increase in current by increasing the M_{Px} gate voltage input and, therefor, decreasing the current flowing through each stage, as can be seen in figure 6.4.

Since the voltage reference is operating in subthreshold regime, it requires an extensive research to achieve the desired ppm/°C parameter by changing the values of W and L of both transistors. In turn, this will also change the CTAT value of such reference voltage, i.e., as we increase the variation rate with temperature of the skewed bandgap voltage reference, the output voltage is increased. There is an optimal point determined for a typical process corner *TT*, calculated

through graphical analysis of the output frequency as we change the voltage applied in the gates of the current source PMOS structure.

By changing the ration between W1, W2, L1 and L2, we can achieve the desired skewed transistor [45]. In this specific case, the output oscillation frequency is seen in figure 6.4. The value is compared in figure 6.5 to a situation where ppm/°C is near zero, i.e., the V_{ctrl} value increases with temperature in a way that counteracts the increase in current with temperature.

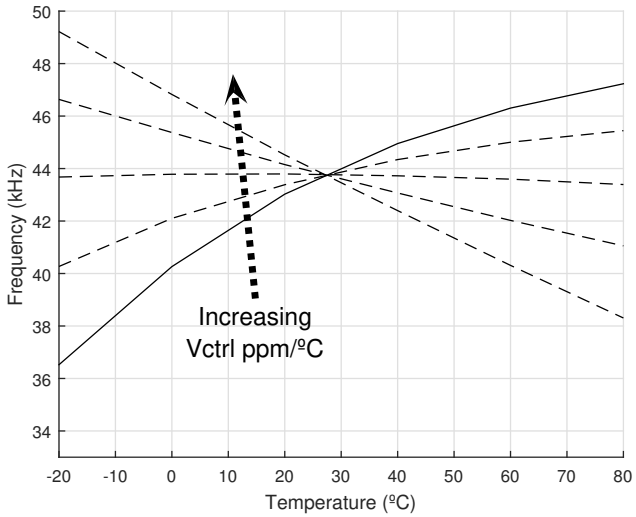


Figure 6.4: Frequency variation with temperature in the CSRO. Different values of ppm/°C into the gate input will change the PTAT variation of the oscillation frequency

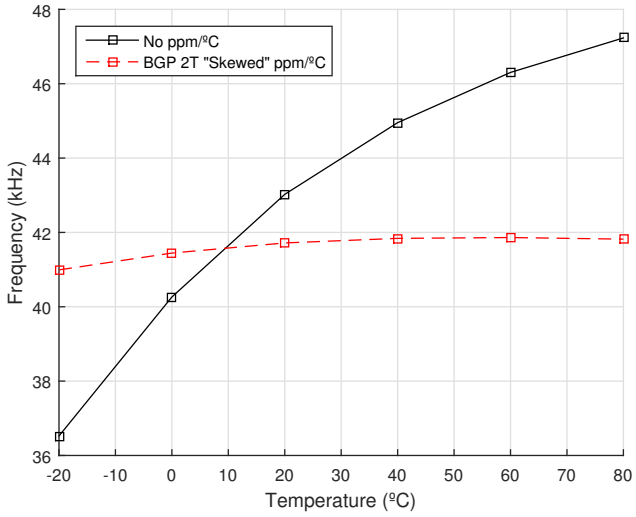


Figure 6.5: Output oscillation frequency of the CSRO with a skewed 2T Voltage Reference

For our implementation, the size values for the 2T schematics are described in table 6.1. The maximum available size for the width of a near-zero threshold voltage for this technology is 100 μm. To achieve this value of 160 μm, two transistors where connected in a parallel topology, each with 80 μm as its width.

Table 6.1: 2T BGR Parameters values

Transistor Parameter	**Value** (μm)
W1	*160*
L1	*0.5*
W2	*0.8*
L2	*50*

The final layout of the 2T skewed voltage reference can be seen in figure 6.6. As seen, the M1 transistors are surrounding M2 to achieve a better symmetrical layout. The final area occupied by this circuit is 888,06 μm^2.

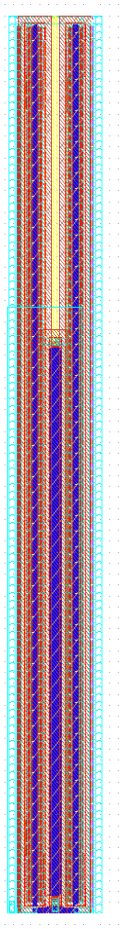


Figure 6.6: 2T Skewed Reference Voltage Layout

6.3 Process Variation

For process variation, the M_{N1} transistor was replaced by a set of parallel NMOS devices that can be turned on/off as needed to decrease/increase the current value mirrored towards the remaining NMOS current sink transistors. This trimming action is performed by inserting a transmission gate 2-to-1 multiplexer schematic to pass the gate input if it is turned on by a set control value C_X or connected to the ground level to send the transistor into cut-off state ($V_{GS} = 0$). This topology is seen in figure 6.7 and was selected because a simple transmission gate always requires a path to the lowest voltage level in the circuit when it is turned off, achieved with an output capacitor and a resistance [39]. To eliminate the need for these components, another transmission gate with the input connected to ground is inserted, turning off the output transistor and creating a path to ground for this circuit. This topology produces a 2:1 multiplexer that passes the value of VG_{PMOS} when the control bit C_n is high and grounds the gate of the transistor when the control bit is 0, creating a condition where, for that specific transistor, V_{GS} = 0.

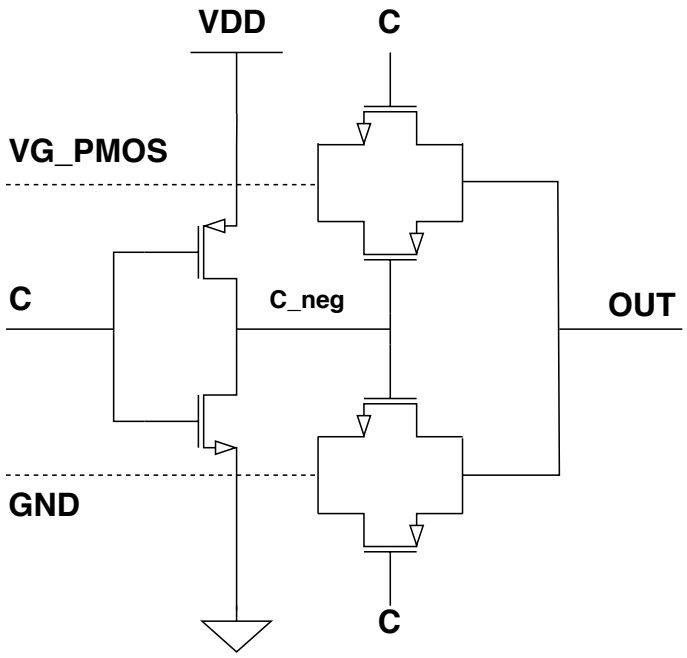


Figure 6.7: 2-to-1 Transmission gate Multiplexer

The layout of the implemented multiplexer can be seen in figure 6.8. This has a total area occupied of 83.62 μm^2 which is extremely smaller compared to remaining components of the circuit. This is also possible by using the smallest values for W and L of the used technology. Since the transmission gate only has to pass a small value to the output (in the orders of hundreds of mV) , the main component in the output resistance R_{OUT} is the value of the resistance of the NMOS device, that is a great component to pass near-zero values, i.e., low values of R_{OUT}.

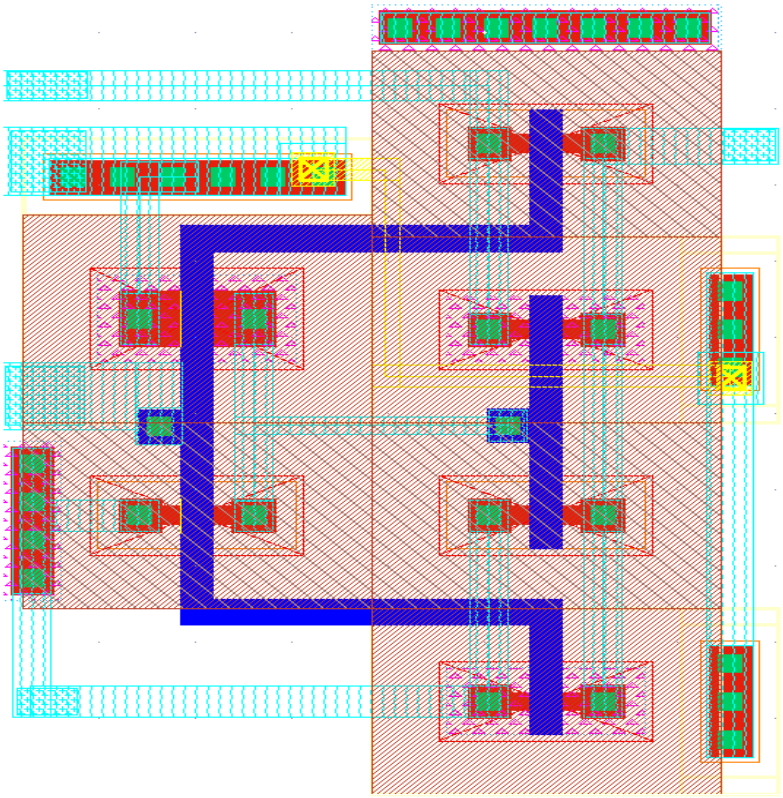


Figure 6.8: 2-to-1 Transmission gate Multiplexer - Layout

The number of parallel NMOS devices was defined in order to compensate for wide range of input voltage VDD and all process corners. The scaling of the W values for each transistor is an increase by the power of 2, creating a binary word with a minimum resolution defined by the size of the smallest NMOS transistor, as seen in figure 6.9. For our implementation, the minimum size of the M_{N1} parallel structure is $250nm$.

For the NMOS devices in the current sink, the size estimation depends on the maximum frequency output desired and the granularity of the intended trimming. As seen in figure 6.10, the current I1 is mirrored into the transistors M_NX. For design symmetry and circuit stability, the values of M_NX are defined as equal for each stage.

The value of W_{M_NX} defines the maximum available current for each stage and its resolution as follows:

$$\frac{I2}{I1} = \frac{W_{M\_NX}}{W_{M\_N1}} \tag{6.4}$$

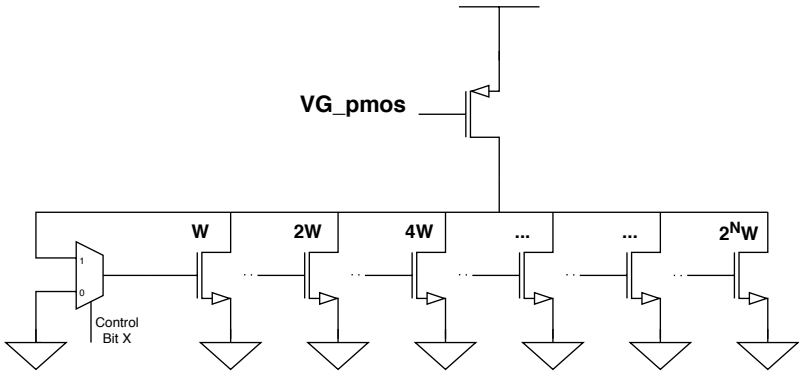


Figure 6.9: Schematic for the implementation of the parallel NMOS devices

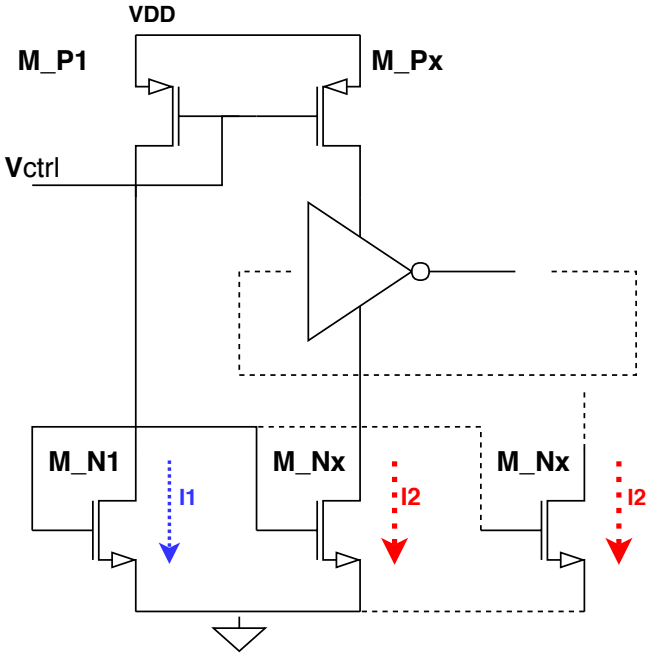


Figure 6.10: Current mirror analysis

The maximum current is obtained when W_{M_N1} transistor array is minimum size, i.e., $250nm$. The resolution of this implementation is defined as follows:

$$\left(\frac{I2}{I1}\right)_{min} = \frac{W_{M\_NX}}{(W_{M\_N1})_{max}} \tag{6.5}$$

By choosing a value for W_{M_NX}, the maximum ratio $\frac{I2}{I1}$ is defined and the resolution of the current selection is specified. In this implementation, the chosen value for W_{M_NX} is $4\mu m$ for a maximum ratio $\frac{I2}{I1}$ of 16 and a resolution of 0.5. This allows for a well established and linear current ratio, for a reasonable resolution, as seen in figure 6.11 . The frequency variation CTAT values with minimum size variation, measured at 25 °C, is approximately 700 Hz.

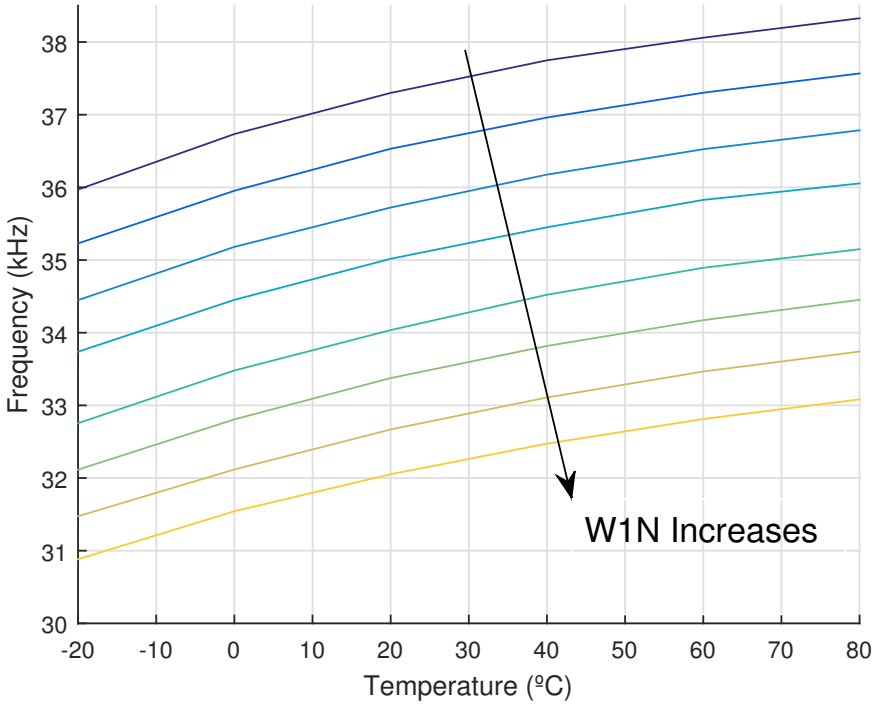


Figure 6.11: CSRO frequency variation with W_{M_N1}

Global lenght L_x parameter of all transistors in the CSRO is 40 μm to achieve ultra low power consumption values and the desired current flowing through the circuit for the intended oscillation frequency. The current flowing through M_N1 is defined by the PMOS transistor M_P1. This value is already temperature compensated with an input V_{ctrl} in its gate as described previously. The value of the current flowing through each stage is dependent on the transistor W_{M_N1} value, that is mirrored to the remaining current sink NMOS.

For the intended design, process and supply voltage variations must be considered, since the NMOS current sink must be able to achieve the desired current for each stage to output the expected frequency. For this case, the process corners behaviour for the worst supply voltage values (VDD = 1.3V) was analyzed with the full NMOS M_N1 current sink structure activated (achieving the lowest possible value of $\frac{I2}{I1}$) and the results are seen in figure 6.12. The value selected for W_{M_P1} is $7\mu m$ since in this case, for the worst possible case, it is possible to reach the desired output frequency . This shows another advantage since temperature variation is also decreased with lower values of W_{M_P1} and the process corner variations are lower.

The inverter sizing was defined to output a frequency with the duty cycle as close as possible to 50% and to match the rising time with the falling time of the output signal. As such, the value for W_{P_I} is $3\mu m$ while W_{N_I} is $1\mu m$ to compensate for the difference in mobility of the holes in the PMOS device and the mobility of the electrons in the NMOS device.

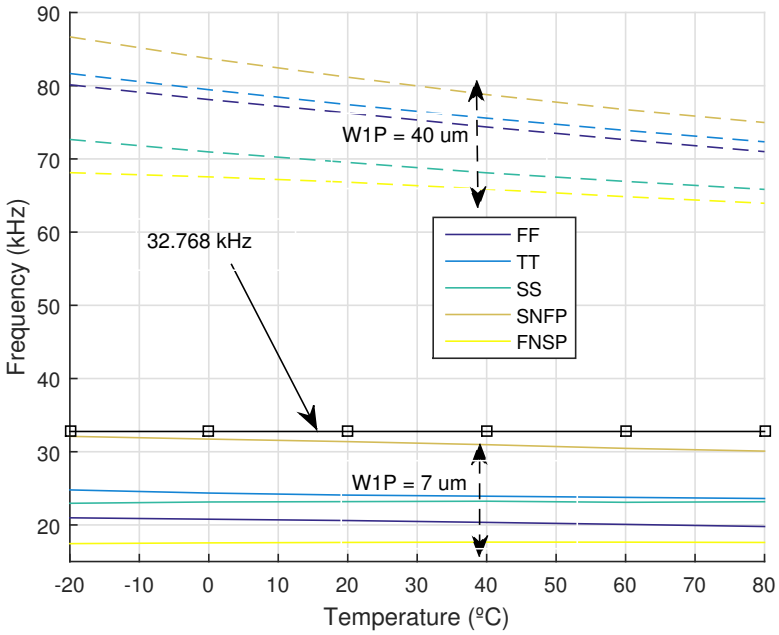


Figure 6.12: CSRO frequency variation with W_{P_N1}

As seen in equation (6.3), the capacitor value is inversely proportional to the output frequency. So, for the same frequency value, if the value of C_{out} is lower, the current $I_{starved}$ must also decrease its value to achieve the same results. As such, the value of C_{out} is defined as the lowest possible for this technology (2,022fF) , to achieve a lower current flowing through the stages and decrease power consumption. The values for all devices in the system are described in table 6.2. The L value is the same for all transistors in the schematic. Taking figure 6.2 as reference point, M_P1 is matched with M_P2, M_P3 and M_P4 while M_N2 is matched with M_N3 and M_N4. The capacitor values are the same for all 3 while the driver and signal restoration inverter sizes are the minimum available for this technology.

Table 6.2: Transistor Sizes of the CSRO

Transistor Parameter	**Value** (μm)
L	*40*
W1P	*7*
W1N	*4*
WIP	*3*
WIN	1

The layout for the CSRO is seen in figure 6.13. The 3 stages are seen as 3 identical structures on the middle of the layout. Each stage was designed to achieve maximum symmetry of the circuit, with 3 transmission gates on each side of the NMOS current sink M_N1 structure. Global signal rails are available for each side of the design. The capacitor area occupation is almost negligible

compared to the overall circuit. The 2T skewed voltage reference can be seen on the top right side of the figure 6.13. Total area occupied by the CSRO and the skewed voltage reference is 22829 μm.

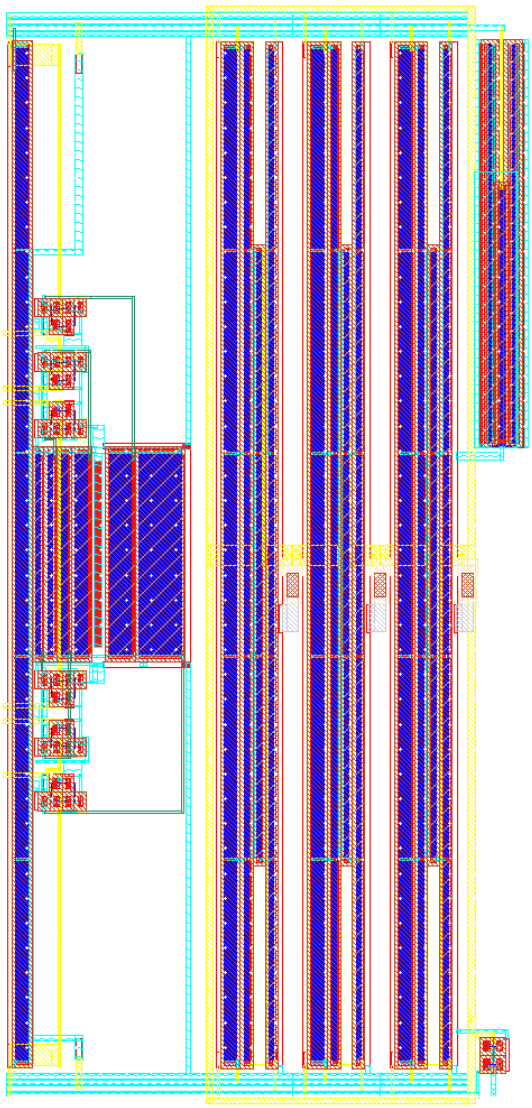
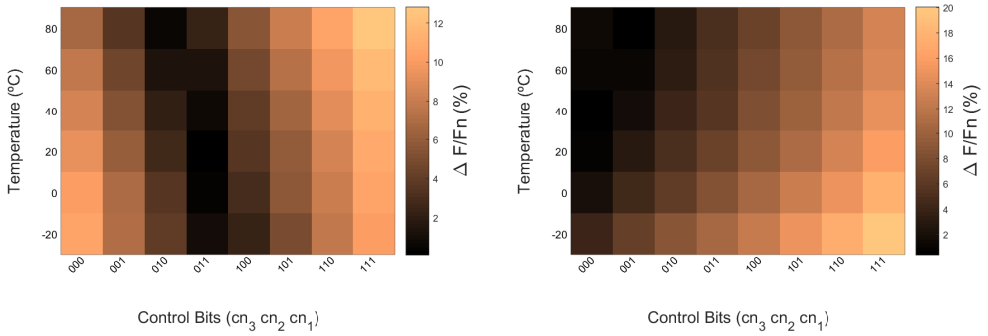


Figure 6.13: CSRO layout

The whole Process and Temperature control block (including the current starved ring oscillator) is simulated and the values are presented in a heat map for specific control bits that achieve the desired output frequency for each process corner and different temperature values. The value presented is calculated as the temperature point deviation from the 32.768 kHz objective for each temperature point as follows:

$$\Delta F/Fn(\%) = abs\left(\frac{F_{res} - F_{obj}}{F_{obj}}\right) \times 100 \tag{6.6}$$

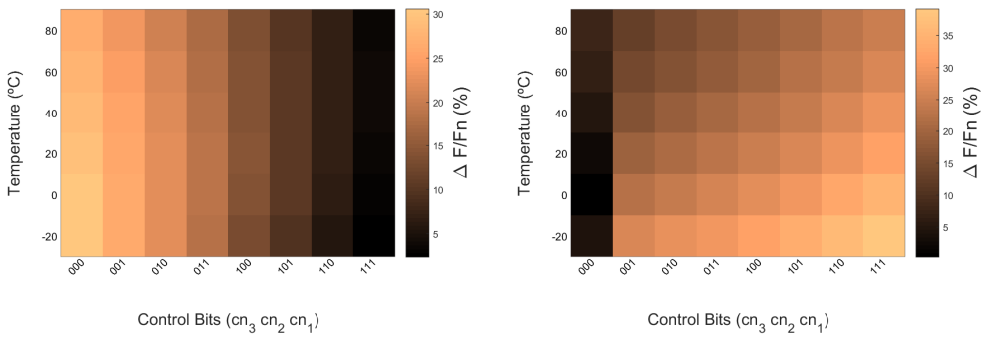
where F_{res} is the acquired frequency and F_{obj} is the 32.678 kHz value. This is shown in figures 6.14, 6.15, 6.16, 6.17 and 6.18 where the darkest color spots of each heat map represent the lowest values obtained with (6.6). The gradient is shown in each figure and the brightest colors attend for the worst cases in each simulation of the extracted circuit. Power consumption is shown for the best scenario at each voltage supply level.



(a) VDD = 1.3V @ $Cn_6Cn_5Cn_4 = 010$ (b) VDD = 1.2V @ $Cn_6Cn_5Cn_4 = 000$

Figure 6.14: CSRO - Layout results for FF process corner

For the FF corner, the power consumption achieved for the best control bit setup is 138,4 nW @ V_{DD} = 1.2V and 271,29 nW @ V_{DD} = 1.3V. The resulting differences of the percentage blocks derive from the higher temperature coefficient values that this process corner has. For the *010011* control bit setup V_{DD} = 1.3V, the maximum frequency deviation percentage is 2,35% at 80 °C and the lowest achieved is at 20 °C with a value of 0.0879%.

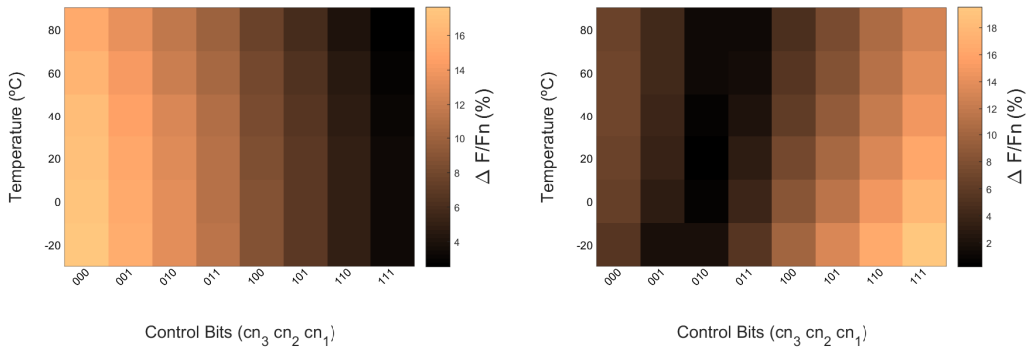


(a) VDD = 1.3V @ $Cn_6Cn_5Cn_4 = 001$ (b) VDD = 1.2V @ $Cn_6Cn_5Cn_4 = 000$

Figure 6.15: CSRO - Layout results for FNSP process corner

In the FNSP process corner, a more linear increment is seen. This translates to a better temperature coefficient of the circuit. Power consumption achieved for the best control bit setup is 97.79 @ V_{DD} = 1.2V and 212.57 nW @ V_{DD} = 1.3V. This lower power consumption @ V_{DD} = 1.2V is achieved when all NMOS current sink transistors are turned off, meaning that only a small leakage current is mirrored to each oscillator stage. For the *001111* control bit setup V_{DD} = 1.3V,

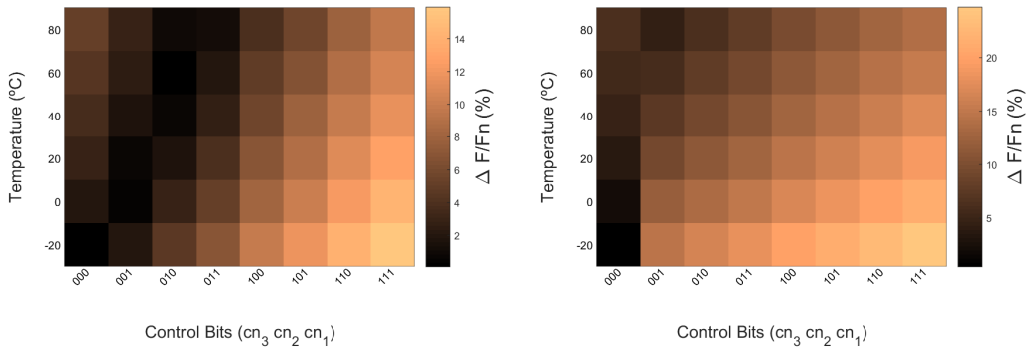
the maximum frequency deviation percentage is 3.66% and the lowest achieved is at -20 °C with a value of 2.33%.



(a) VDD = 1.3V @ $Cn_6Cn_5Cn_4 = 011$ (b) VDD = 1.2V @ $Cn_6Cn_5Cn_4 = 001$

Figure 6.16: CSRO - Layout results for SNFP process corner

In the SNFP process corner, the temperature coefficient is low for a voltage supply of 1.3V but it increases with a drop to 1.2V., as seen in figure 6.16 with the best control bit setup $Cn_3Cn_2Cn_1$ for -20 °C being *001* and the best control bit setup for 80 °C is *011*. Power consumption achieved for the best control bit setup is 197.66 @ V_{DD} = 1.2V and 340.13 nW @ V_{DD} = 1.3V. For the *001010* control bit setup @ V_{DD} = 1.2V, the maximum frequency deviation percentage is 1.89% at 80 °C and the lowest achieved is at 20 °C with a value of 0.22%. This is an improvement compared to the values obtained in the FNSP process corner.

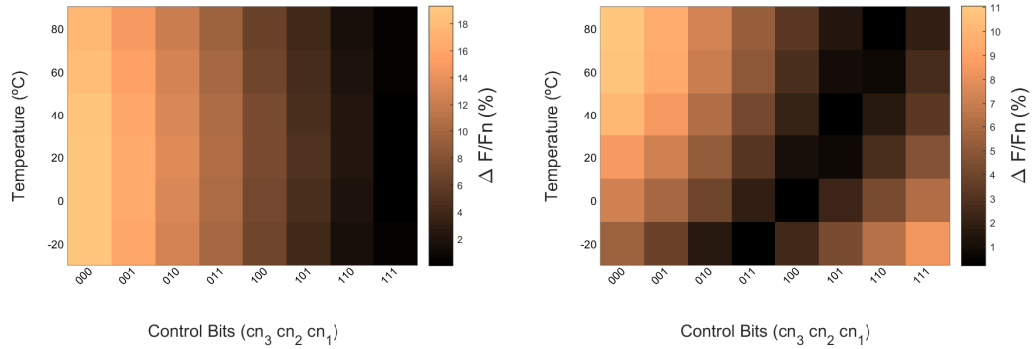


(a) VDD = 1.3V @ $Cn_6Cn_5Cn_4 = 010$ (b) VDD = 1.2V @ $Cn_6Cn_5Cn_4 = 000$

Figure 6.17: CSRO - Layout results for SS process corner

In the SS process corner, the highest temperature coefficient is achieved @ V_{DD} = 1.3V, as seen in figure 6.17. The darkest spot fluctuates for each temperature point is constant regarding the control bit setup and it is increased as temperature rises. In the case where V_{DD} = 1.2V, the lowest percentage achieved is achieved when all NMOS current sink transistors are turned off, mirroring a leak current to each stage. The power consumption for the SS process corner @ V_{DD}

= 1.3V is 229.36 nW. For the V_{DD} = 1.2V case, power consumption is 133.67 nW. The SS process corner also displays the worst results regarding percentage deviation from the objective since for the *000000* bit control the maximum deviation is achieved at 80 °C with 6.14% and the lowest achieved deviation is at -20 ° with 0.44%.

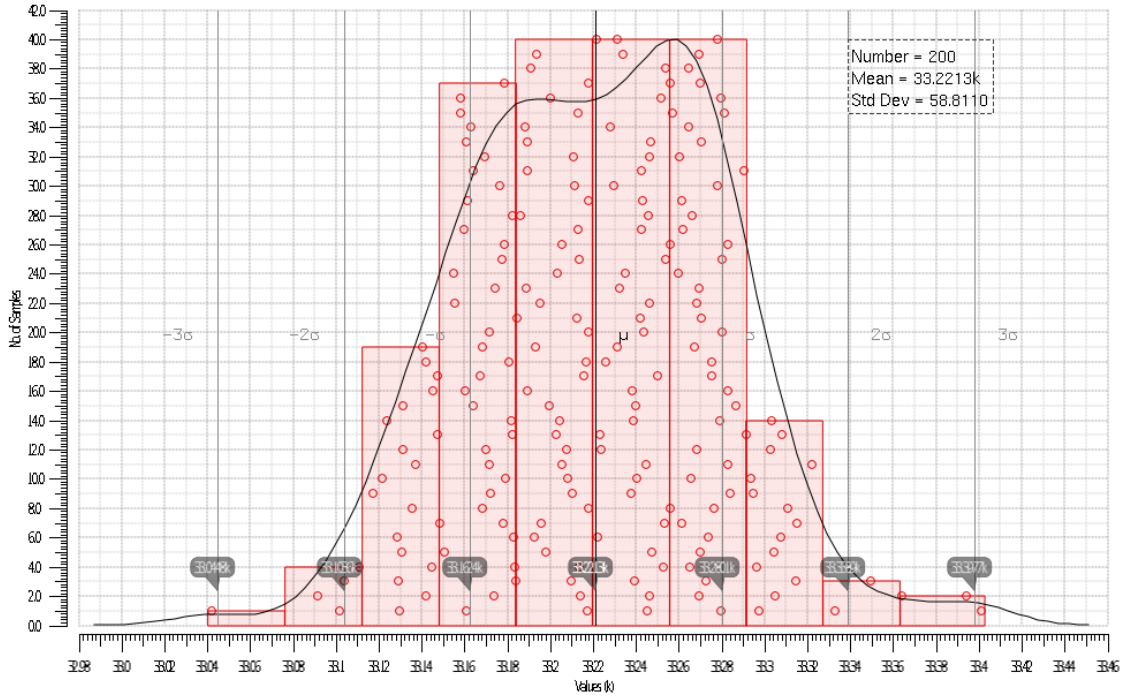


(a) VDD = 1.3V @ $Cn_6Cn_5Cn_4$ = 010 (b) VDD = 1.2V @ $Cn_6Cn_5Cn_4$ = 000

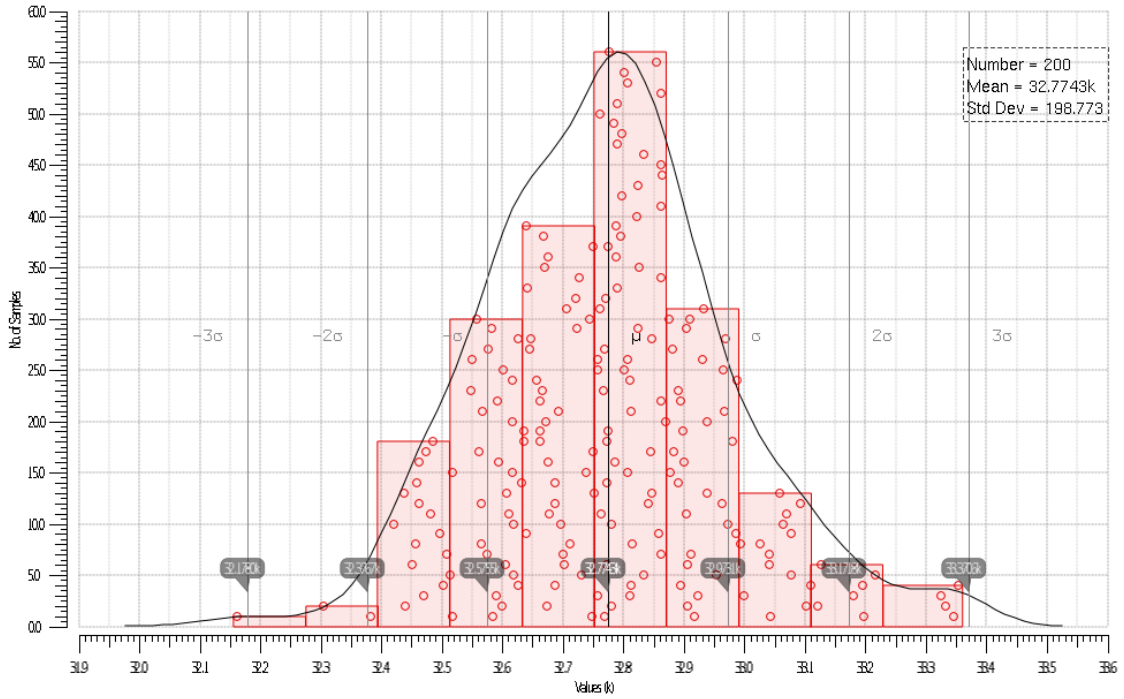
Figure 6.18: CSRO - Layout results for TT process corner

For the TT process corner, the circuit shows better temperature coefficient @ V_{DD} = 1.3V, as seen in figure 7.18. The worse temperature coefficient is seen in the case where supply voltage is 1.2V, since the lowest values of percentage deviation from the objective increase almost linearly with temperature. The power consumption for the case where V_{DD} = 1.3V is 272.77 nW and when V_{DD} = 1.2V, the value obtained is 151.98 nW. For the case where V_{DD} = 1.2V and the control bit setup is *000101*, the lowest value of percentage deviation is obtained when temperature is 40 °C at the value of 0.26% and the highest at -20 °C, with the value of 4.34 %.

After an individual process corner assessment, the circuit extracted from the layout implementation is subjected to Monte Carlo simulations in the TT process corner. The number of runs for the Monte Carlo simulation is set as 200 and a standard deviation of 3 to account for the worst case scenarios. This achieves the complete analysis of the overall circuit behaviour in all process corner possible values. This Monte Carlo simulation is done with temperature at 25 °C and for the best control bit setup achieved after the analysis performed in figure 6.18, for the two extreme values of supply voltage V_{DD} = 1.2V and V_{DD} = 1.3V. The tested parameters are the output frequency of the current starved ring oscillator (figure 6.19), its power consumption (figure 6.20) and its duty cycle (figure 6.21). Process sensibility is described with the mean value μ and standard deviation σ.

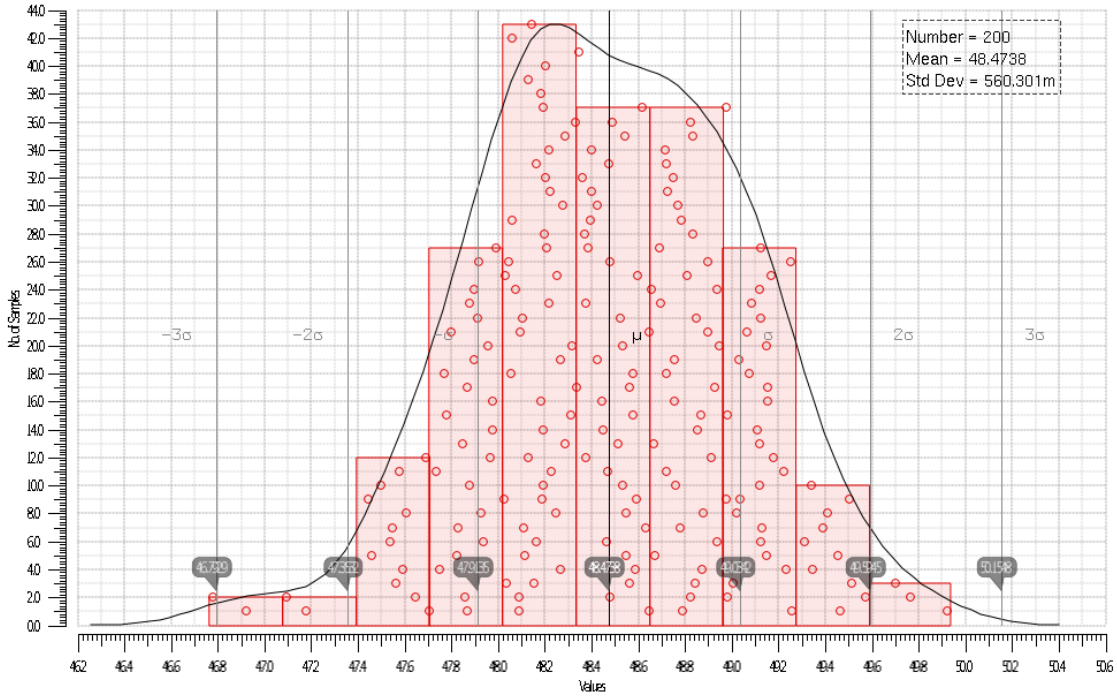


(a) VDD = 1.2V

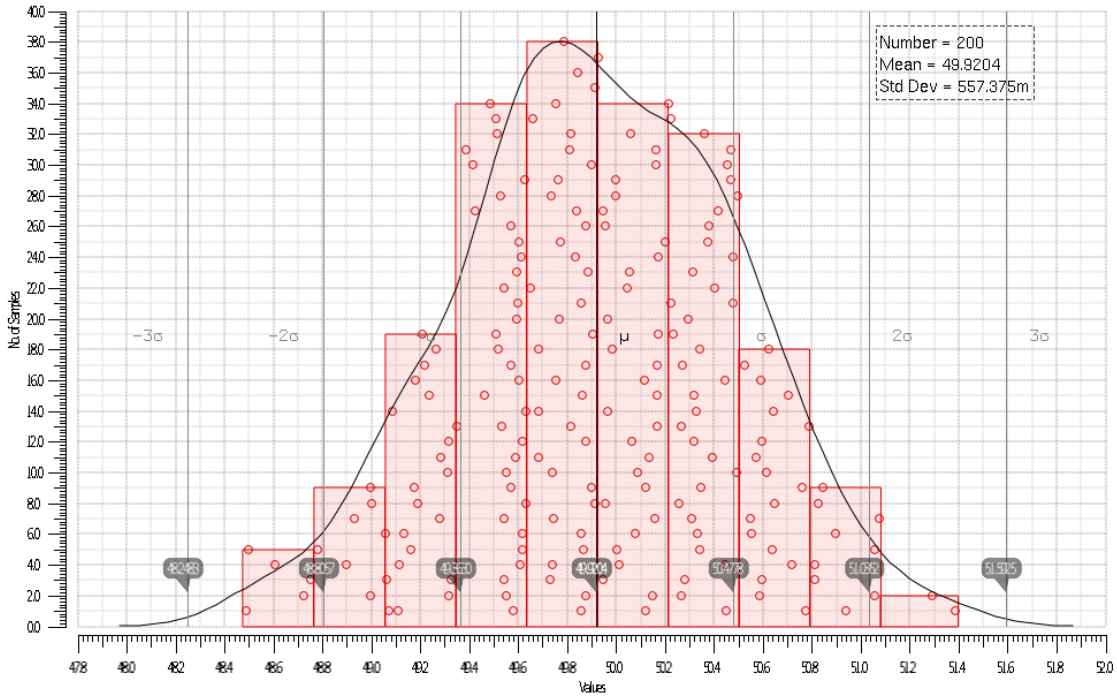


(b) VDD = 1.3V

Figure 6.19: CSRO - Monte Carlo Simulation for the TT process corner - Output Frequency

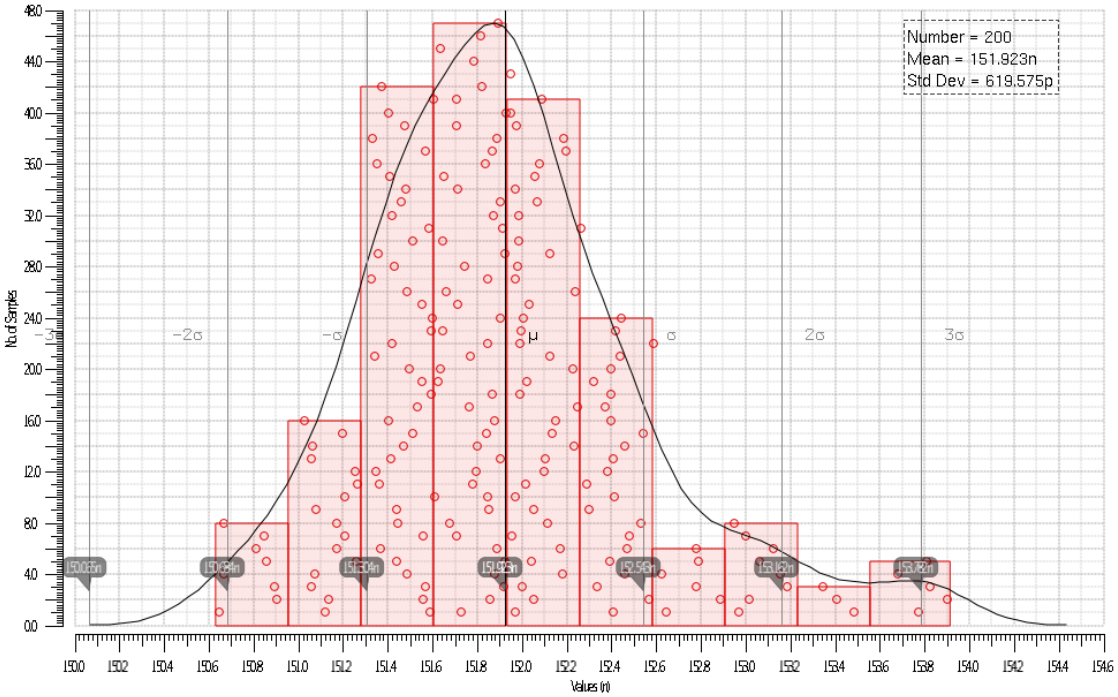


(a) VDD = 1.2V

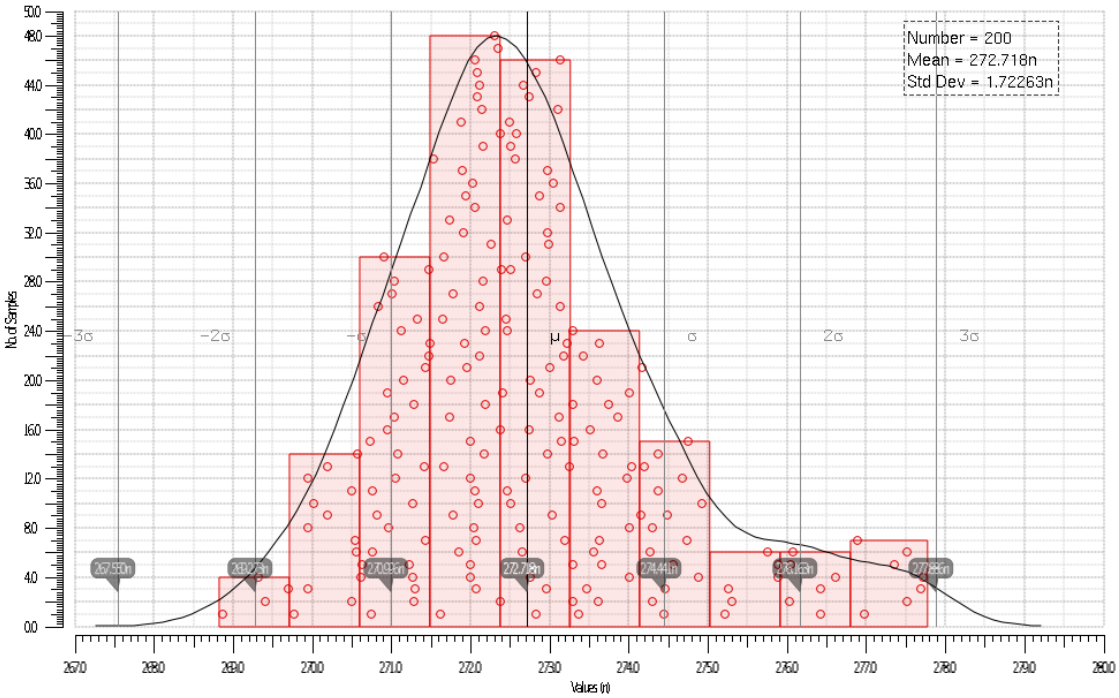


(b) VDD = 1.3V

Figure 6.20: CSRO - Monte Carlo Simulation for the TT process corner - Duty Cycle



(a) VDD = 1.2V



(b) VDD = 1.3V

Figure 6.21: CSRO - Monte Carlo Simulation for the TT process corner - Power Consumption

Monte Carlo simulations of the CSRO shown in figures 6.19, 6.20 and 6.21 display the variation of the performance of the final circuit according to small discrepancies in terms of process and mismatch of transistors around the TT corner. This provides a clear picture of the most likely output of the implemented circuit. Process corner case analysis is also studied to achieve a full view of all possible outcomes. This analysis is studied for 3 different performance variables, with 2 different supply voltage values (1.2V and 1.3V):

- **Output Frequency** is described in figure 6.19 and it is extremely close to the proposed objective. The run obtained with a supply voltage V_{DD} = 1.2V has a tighter distribution than the values obtained with V_{DD} = 1.3V but the frequency output achieved with V_{DD} = 1.3V (32.774 kHz) for a temperature of 25 °C is better than the one obtained with V_{DD} = 1.2V (33.221 kHz)
- **Duty Cycle** is shown in figure 6.20 and, as proposed, the values are near 50%, achieving a stable and viable output frequency.
- **Power Consumption** analysis in figure 6.21 makes this circuit suitable for ultra low power implementations. The value is increased as the supply voltage increases, but for the best output frequency at V_{DD} = 1.3V and a temperature of 25 °C, the resulting power consumption is 272.72 nW.

After analyzing all the individual components, the next step in the realization of the overall circuit is the integration. In the next chapter, all blocks will be interconnected. A performance analysis of the circuit will be performed and the resulting necessary changes to the initial circuit are shown. For a final consideration, figure 6.22 shows the output signal for the best case scenario at V_{DD} = 1.3V with a frequency of 32.774 kHz.

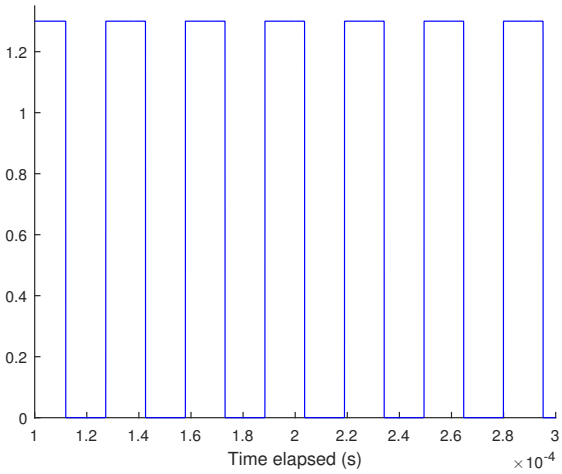


Figure 6.22: CSRO Output Signal

Chapter 7

Integration

In this chapter, the individual power management unit control block and temperature/process control block will be connected and the performance of the circuit will be analyzed. In the study of each block, some parameters like supply voltage for the CSRO and oscillation frequency for the regulated charge pump were taken as an ideal factor. This is not the case, since the values for each one of them will change according to different variables of the system (PVT variations).

- **Power Management Unit** - the input clock for the control of the switches is given by the CSRO. This will affect the behaviour of the system and change the output voltage that, in turn, will also change the output frequency and so on. Stability of the system is the main objective.
- **Temperature and Process Control Block** - temperature variation of the system is compensated through the V_{ctrl} block, assuming a constant value of V_{DD}. The whole system must be checked to assure a low temperature coefficient of the output frequency and therefor a stable frequency input for the regulated charge pump.

The layout of the implemented integration is seen in figure 7.1. The area occupied by the system is 146255 μm^2 (0.1463 mm^2). As expected, the majority of the space is occupied by the reservoir capacitor C_R and the voltage divider for the operational amplifier regulation input. The parasitic extraction is executed and tests are performed on the final circuit. The input voltage is defined as 1.5 V and temperature variation is seen in the range of -20 °C to 80 °C. Process corner analysis is realized. The control bits for each process corner is shown, as well as power consumption, the duty cycle at 25 °C, the *startup time* that is defined that the interval of time until the circuit stabilizes and the output signal can be used, the temperature coefficient and the output frequency at 25 °C. The analysis of the circuit is shown in figures 7.2, 7.3 and 7.4. All of them are taken from the results extracted from the layout circuit simulation.

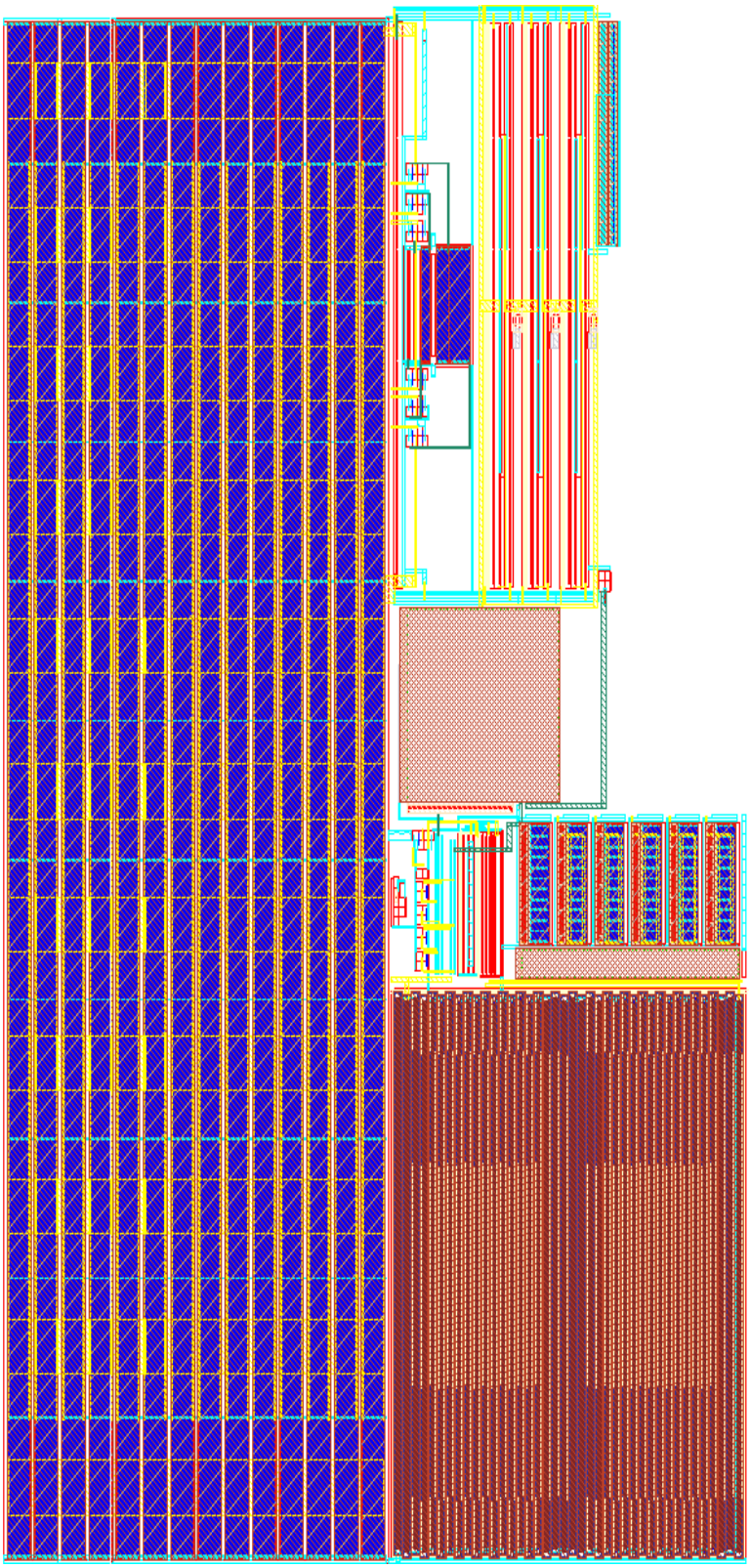


Figure 7.1: Final layout of the proposed circuit

In figure 7.2, the signals for the supply voltage of the CSRO and the output frequency are shown. As can be seen, the startup circuit initiates the oscillation and after a set interval of time, the regulated charge pump takes over and assumes control of the supply voltage. The blue line shows the output voltage supply from the regulated charge pump while the red values show the output from the oscillator component. This representation is also used for the following figures 7.3 and 7.4.

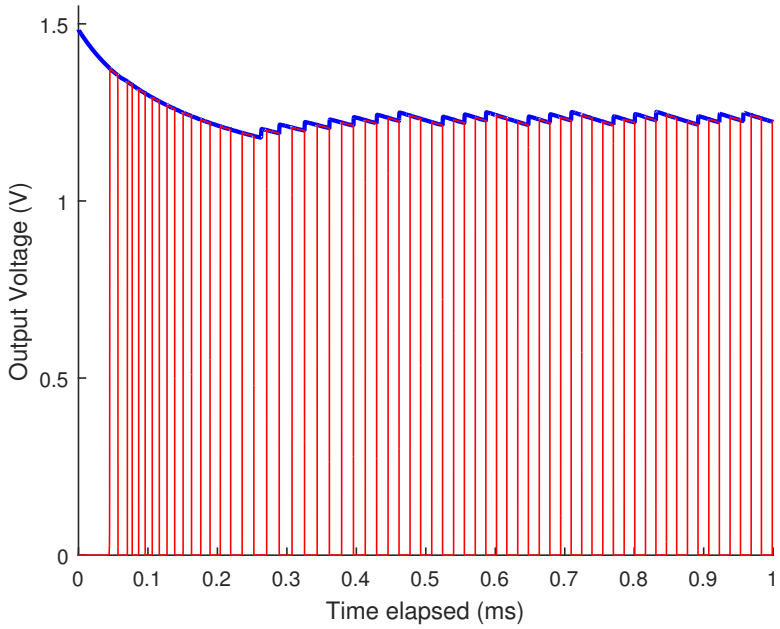


Figure 7.2: Startup Circuit of Final Integration

In figure 7.3, a wider picture of the output signal is seen. The circuit stabilizes after a set interval of time. The oscillation frequency remains the same even when small variations of supply voltage are inserted through the regulated charge pump. This is the output signal fed to the digital block of the overall implementation and into the regulated charge pump and used as the clock signal for the internal switching between the *charging phase* and the *discharging phase*.

In figure 7.4, a closer look is taken to view the output oscillating signal. It is shown that the maximum value is limited by the supply voltage coming from the regulated charge pump. The ripple voltage from the regulated charge pump does not have a major impact on the frequency variation of the output signal. This signal also has a well defined "*high*" and "*low*" value for the digital input. This shows that this output signal can be used for the intended implementation, since the digital circuit can do an easy recognition of this values for its counter.

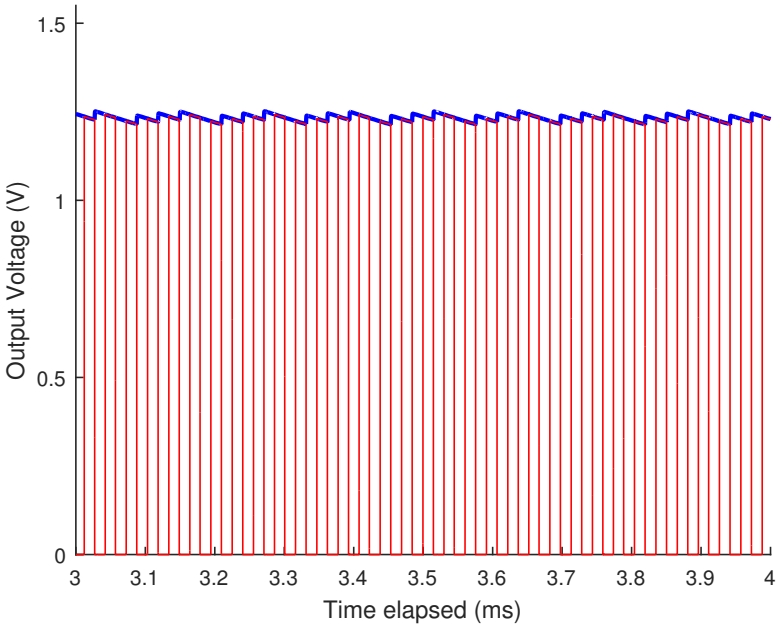


Figure 7.3: Output Signal

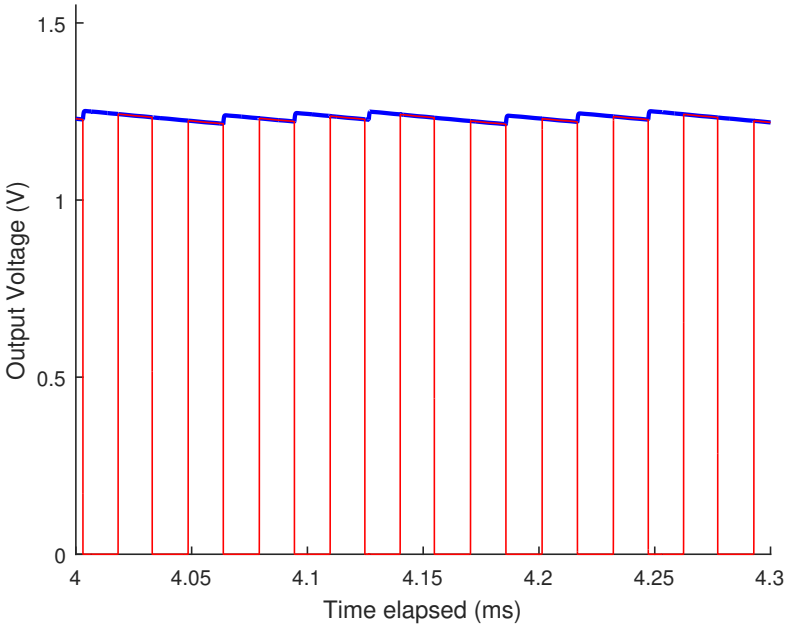


Figure 7.4: Output Signal - Closeup view

In table 7.1, the results are shown for specific performance points. Different control bits are necessary to achieve the desired frequency output. The selected values are the ones where temperature coefficient and overall deviation with temperature from the goal frequency is minimum. This in turn explains the difference at 25°, so that the overall achieved result is better. The power

Table 7.1: Process Corner performance results

Parameter	TT	SS	FF	FNSP	SNFP
Power Consumption at 25 °C (nW)	841.3	*274.6*	*1396*	*517*	*1038*
Output Frequency at 25 °C (kHz)	*32.789*	*31.304*	*34.076*	*32.734*	*33.248*
Energy per Cycle at 25 °C (pJ/Hz)	*25.7*	*8.8*	*41*	*15.8*	*31.2*
Duty Cycle (%)	*49.19*	*48.26*	*49.17*	*48.4*	*49.18*
Startup Time (μs)	347.91	*449.31*	*329.79*	*447.61*	*1213*
TC (%/°C)	*0.0291*	*0.2485*	*0.1459*	*0.1336*	*0.1515*

consumption is higher in the FF and SNFP corners (around 1.038 μW for the SNFP corner) and the lowest values are achieved for SS and FNSP corner points (with the value of 274.6 nW for the SS corner). Duty cycle is similar to all process corners and extremely close to the desired 50%. The temperature coefficient is calculated for a percentage value, where the worst case scenario is presented in the FF corner, with the value of 0.1583%. For the typical corner case TT, the values presented show extremely good power consumption, with an energy per cycle value of 25.7 pJ/Hz and a temperature coefficient of only 0.0291%/°C, that shows that the circuit is compensated for temperature variations.

Using the equation (6.6), output frequency deviation from the desired frequency is presented as a heat map for different process corners in figure 7.5. As can be seen, for the typical TT process corner, the frequency deviation is low, with a maximum value of 1.74% at -20°C and a minimum value of 0.063% at 25°C.

The frequency versus temperature graphic for different process corners is displayed in figure 7.5. The best temperature coefficient is achieved for the TT process corner and it is also the corner where the frequency output most closely achieves the desired value.

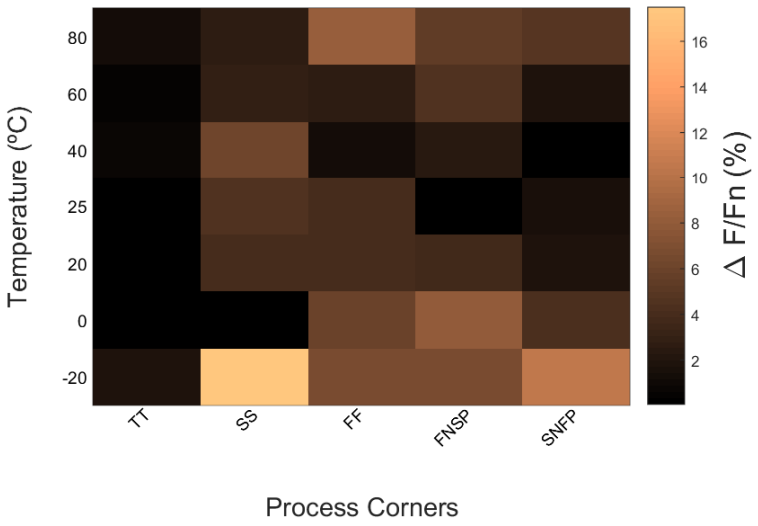


Figure 7.5: Frequency Deviation for each process corner at different temperatures

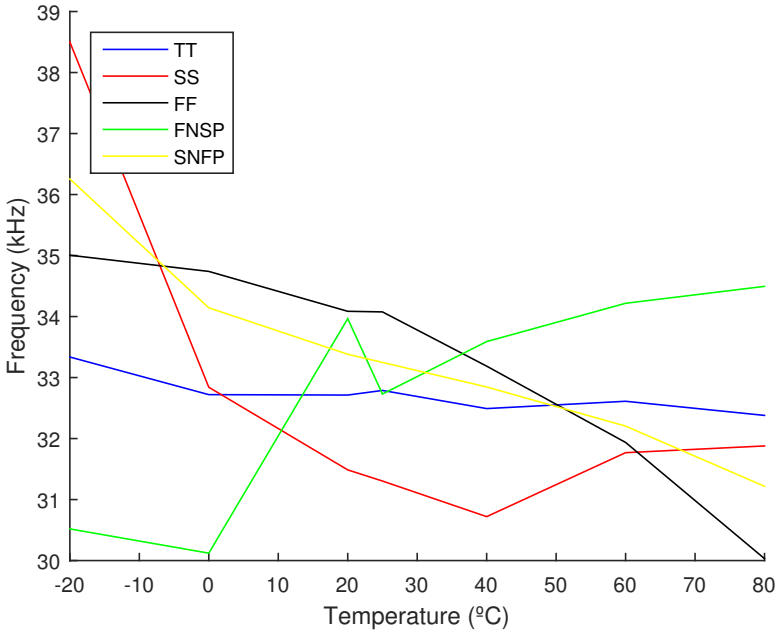


Figure 7.6: Output Frequency for each process corner at different temperatures

In figure 7.6, the different process corner frequency variations are displayed. The great temperature coefficient achieved with the TT process corner is shown in this figure, since output frequency almost does not change with temperature.

Monte Carlo simulation on the TT corner is performed to achieve full overview of the most likely performance ratings of the system. The Monte Carlo simulation is run 200 times at 25 °C for analysis of 3 parameters of performance: output frequency (figure 7.7), duty cycle of the output signal (figure 7.8) and power consumption of the overall system (figure 7.9).

The mean value for the output frequency is 32.698 kHz for a standard deviation of 179.7 Hz. This shows that around the TT process corner, small variations in process and mismatch of the transistors in the circuit do not have such a great impact on the most likely output frequency. Mean duty cycle achieved is 49.15 % for a power consumption of 841.97 nW, for an energy per cycle metric of 25.7 pJ. This in turn shows that is circuit is a great alternative for an implementation in an IoT node.

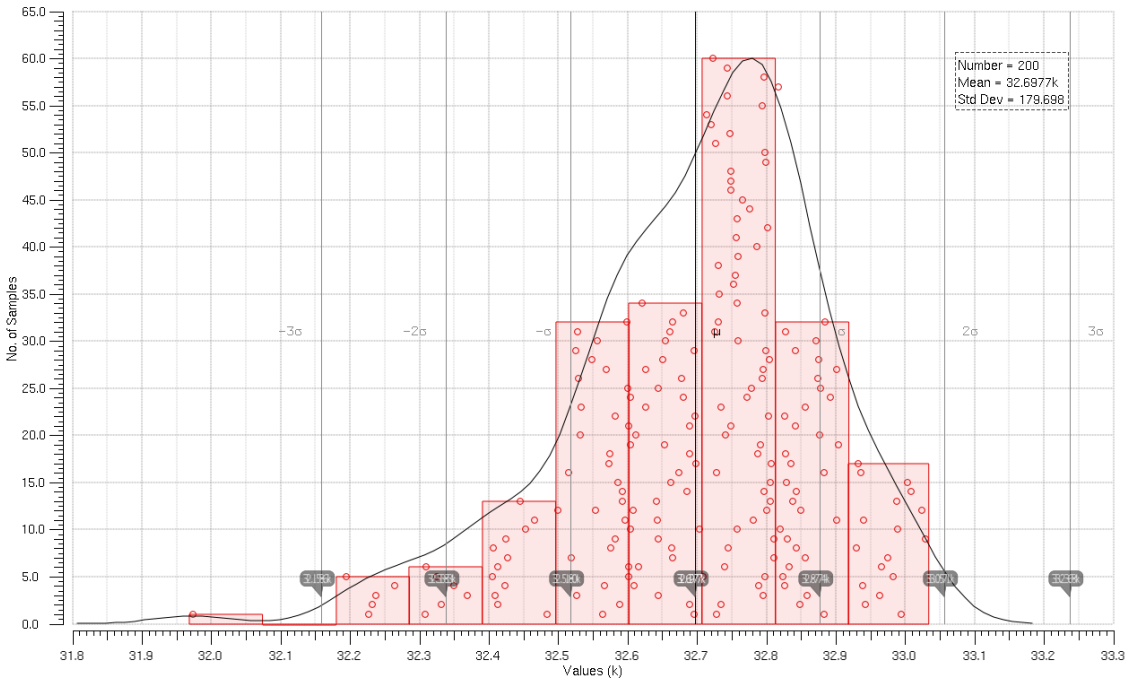


Figure 7.7: Monte Carlo Simulation TT corner - Final Layout - Output Frequency

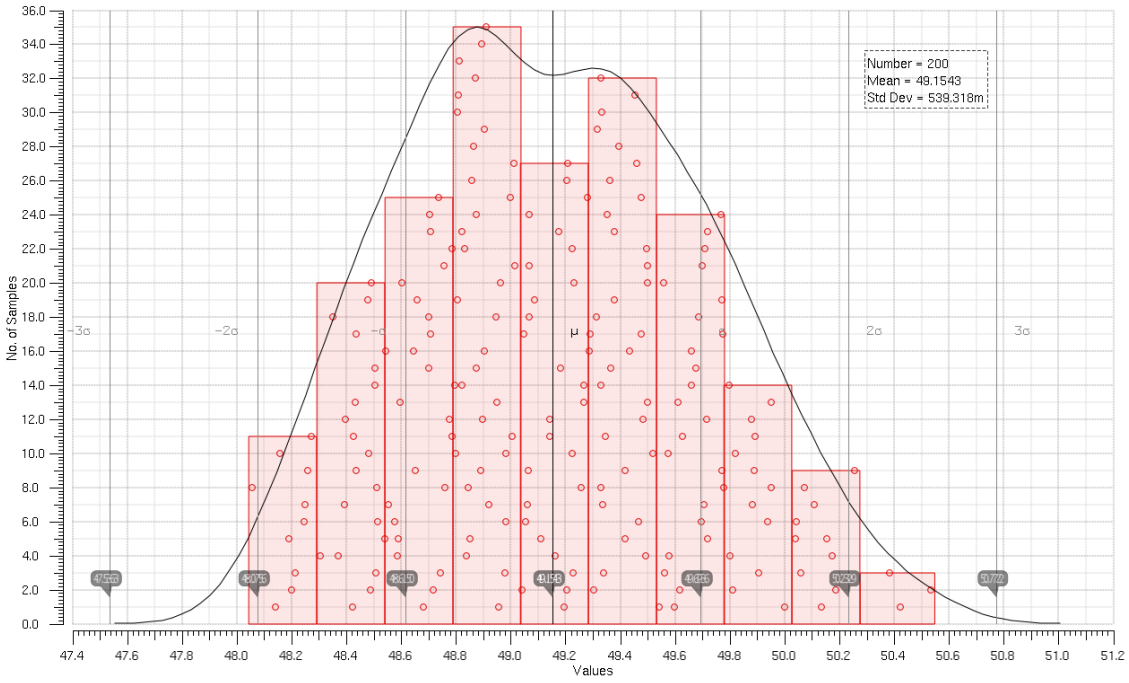


Figure 7.8: Monte Carlo Simulation TT corner - Final Layout - Duty Cycle

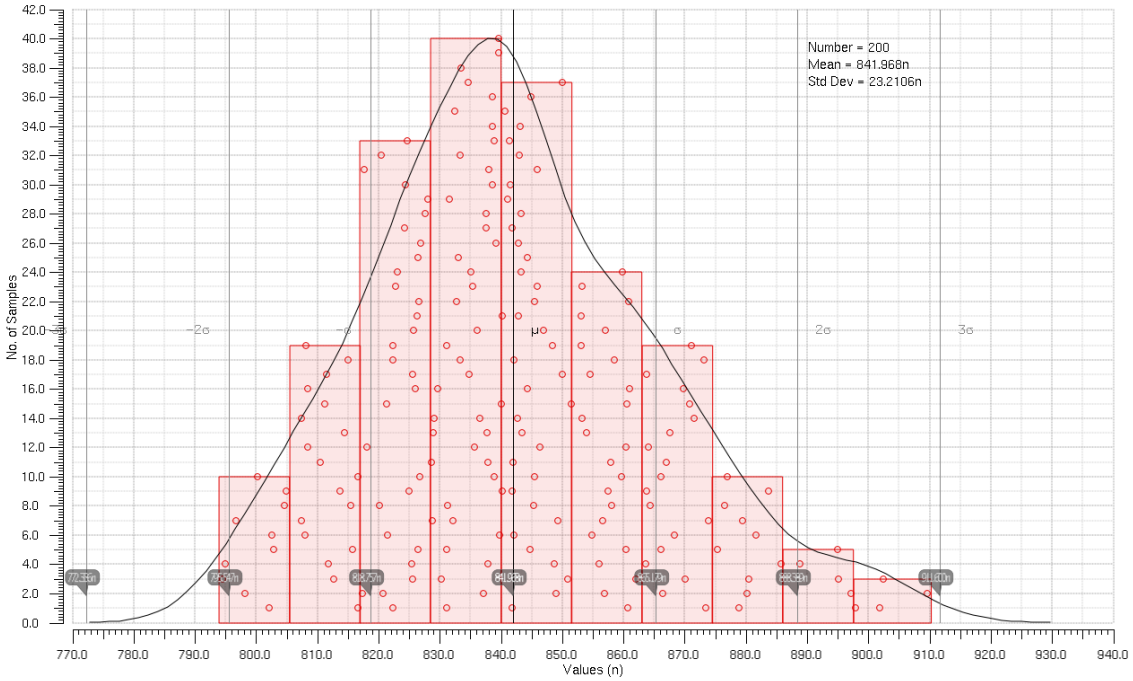


Figure 7.9: Monte Carlo Simulation TT corner - Final Layout - Power Consumption

Chapter 8

Conclusions and Future Work

The design of an RTC to be used for the IoT was done. Mixed signal circuitry was executed in this dissertation. PVT variations are taken into consideration and the results display a circuit that can be used in an IoT network due to its ULP characteristics.

More focus was put into the design of the analog component, since this block is what will be the major power consumer. In turn, different analog devices were developed such as voltage references, regulated charge pumps and an oscillator, all with a main objective: ultra low power consumption with a low PVT variation.

The circuit operates in the temperature range of -20°C to 80°C, for a supply voltage of 1.5V. Monte Carlo simulations display a value of 32.698 kHz operational frequency that has a low temperature coefficient of 0.029% and an ULP consumption of 842 nW, where the energy per cycle value exhibited is 25.7 pJ. The total area occupied by the analog component is 0.146 mm^2, well below the proposed objective. This is all done using 0.18 μm UMC technology.

The presented work is compared to other RTC and oscillator architectures in table 8.1. The analog component is compared to literature oscillator topologies as in [52, 53, 54, 9, 55, 27]. The comparison between the results obtained and an RTC available in the market (Ambiq AM08X5) does not take into account the power consumption of the digital part that still needs to be developed. The results were retrieved from the respective datasheet of the IC [27].

Table 8.1: Results Comparison

Parameters	**This Work**	**[52]**	**[53]**	**[54]**	**[9]**	**[55]**	**[27]**
Technology (*nm*)	*180*	*180*	*350*	*180*	*180*	*180*	*90*
Type	*CSRO*	*CSRO*	*CSRO*	*MEMS*	*XO*	*SR*	*RC*
Area (mm^2)	*0.146*	*0.032*	*N/A*	*1.14*	*0.3*	*0.1125*	*N/A*
Energy/Cycle (pJ)	*25.7*	*4050*	*69.1*	*74.1*	*0.17*	*97.6*	*109.4*
Temperature Range (°C)	*[-20;80]*	*[-25;80]*	*N/A*	*[-40;85]*	*[-20;80]*	*[0;50]*	*[-40;85]*
Temperature Coefficient (ppm/°C)	*291*	*10000*	*N/A*	*4*	*4.56*	*10*	*1500*

8.1 Future Work

More focus should be made towards the digital implementation. As it is, this topology requires a lot of pins in the fabricated pad. To lower this value, a serial input methodology should be adopted, with a MISO and MOSI pin for all setup values and an external clock to handle this commmunication, creating two different clock domains that are independent of each other. The digital layout should be made and the whole system should be tested together. IC fabrication and respective testing should also be done.

For the analog layout, if the circuit is to be taped out, dummy transistors, resistors and capacitors should be added to compensate for different boundary conditions on the transitors that are on the borders of each layout.

Lower power consumption can be achieved if the frequency value is lowered. Tests should be made in order to lower the operational frequency and verify it it is possible to obtain the same or lower energy per cycle and PVT variation metrics. This in turn will also change a major design concept of this dissertation, where the focus was to achieve a 32.768 kHz oscillation frequency.

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