Two-stage S-Band LNA Development Using Non-Simultaneous Conjugate Match Technique

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Abstract. This paper presents the development of a two-stage low noise amplifier (LNA) operating at the S-band frequency that is implemented using the non-simultaneous conjugate match (NSCM) technique. The motivation of this work was to solve the issue of the gain of LNAs designed using the most commonly used technique, i.e. simultaneous conjugate match (SCM), which often produce an increase of other parameter values, i.e. noise figure and voltage standing wave ratio (VSWR). Prior to hardware implementation, the circuit simulation software Advanced Design System (ADS) was applied to design the two-stage S-band LNA and to determine the desired trade-off between its parameters. The proposed two-stage S-band LNA was deployed on an Arlon DiClad527 using a bipolar junction transistor (BJT), type BFP420. Meanwhile, to achieve impedances that match the two-stage S-band LNA circuit, microstrip lines were employed at the input port, the interstage, and the output port. Experimental characterization showed that the realized two-stage S-band LNA produced a gain of 22.77 dB and a noise figure of 3.58 dB at a frequency of 3 GHz. These results were 6.1 dB lower than the simulated gain and 0.76 dB higher than the simulated noise figure respectively.

Keywords: *bipolar junction transistor (BJT); impedance matching network; microstrip line; non SCM technique; S-band frequency; two-stage low noise amplifier (LNA).*

1 Introduction

The growth of communication technology especially in wireless communication systems has stimulated the development of supporting components as well as devices. Numerous devices that support this technology, such as antennas, radio frequency (RF) amplifiers and power combiners/splitters, have been investigated, including a number of front-end amplifiers that were realized using various techniques [1,2]. It is well known that the front-end amplifier,

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sometimes referred to as low noise amplifier (LNA), is one of most critical devices in the receiver of a communication system. This is because the LNA is responsible for recovering data from the signal received from the transmitter. Since the signal that arrives at the antenna can be weak and is almost always accompanied by noise as well as interference, an LNA with high performance capability is necessary to provide sufficient power gain and a low noise figure [2,3]. The LNA should have good enough impedance matching within the required operational frequency bands to suppress the reflected signals or dissipated power. Due to the wide application area of receivers in communication systems, the LNA should also meet several requirements related to non-technical aspects such as physical size, production cost, and ease of fabrication.

Numerous design techniques for constructing LNAs have been investigated in recent times. In [4-6], some of the requirements in the construction of LNAs were satisfied by using a CMOS integrated circuit and a single bipolar transistor. To obtain good impedance matching as well as better isolation at the input and output ports, some amplifiers were cascaded instead of constructed in a single-stage amplifier [7-9]. Some essential parameters should be considered in the design of an LNA, i.e. noise figure, gain, and impedance matching [2,3]. The LNA should also provide low noise behavior not only at one frequency but over all frequencies in the desired working bandwidth [9,10]. The stability of the LNA is another important parameter that should be taken into account. There are some techniques that can be used to attain the desired stability as well as the maintenance stability that could be involved in the design of an LNA, including positive feedback, balanced circuits, resistive matching, and network compensation [7-9].

In most cases, the main goal of an LNA design is to achieve simultaneous noise and input impedance matching at any given amount of power dissipation. Hence, the design of LNAs is most commonly carried out by employing the simultaneous conjugate match (SCM) technique [2,3,11,12]. Moreover, in SCM-based LNA designs, in particular for bilateral and unilateral RF amplifiers, due to the influence of reflected waves it is sometimes very hard to achieve a gain level with maximum transducer power gain. As a result, the determination of the desired trade-off value between gain and VSWR is hard to do and easily affected. To overcome this, using a NSCM technique could be an alternative design approach [13]. In this case, the LNA is designed under mismatch condition to achieve the desired value of gain and VSWR. In this study, a two-stage LNA was developed by using a NSCM technique and cascading 2 BFP420 type RF transistors working at the S-band frequency, i.e. 2-4 GHz. In comparison to a one-stage LNA, the use of a two-stage LNA has a number of advantages, for instance in gain performance. However, at the same

time it also increases the noise figure [14,15]. The LNA was numerically characterized through the ADS software and deployed on an Arlon DiClad527 dielectric substrate. A method of network compensation was employed to compensate impedance mismatch by using microstrip lines at the input and output ports as well as at the interstage between the transistors. To achieve impedance matching, the dimensions of the microstrip lines were determined. After hardware realization some measurement results were analyzed and compared with the design results.

2 Overview of Two-stage S-band LNA Design

2.1 Circuit Topology and Design Technique

There are various circuit topologies for designing LNAs. One of them is the common emitter topology, which was adopted in this study for the design of the two-stage S-band LNA. This topology was chosen to achieve high gain and low noise with good impedance matching and VSWR at the S-band frequency. Figure 1 shows a block diagram of the two-stage S-band LNA, which consists of 2 cascaded type BFP420 BJTs and impedance matching circuits at the input port of the first stage transistor, the interstage between the transistors, and the output port of the second stage transistor.

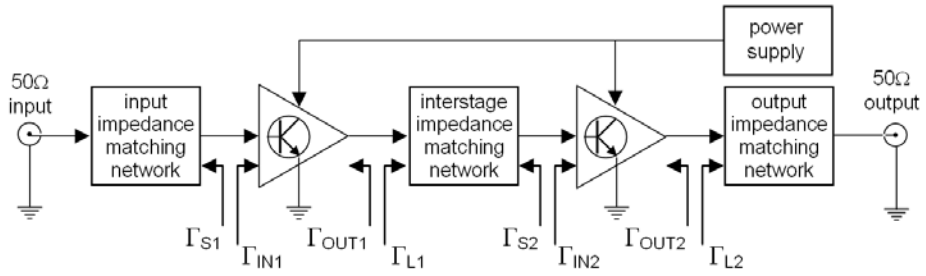

Figure 1 Block diagram of the two-stage S-band LNA.

The reflection coefficients at the input port (Γ_{IN}) and the output port (Γ_{OUT}) of each transistor as a function of scattering parameters are expressed in Eqs. (1) and (2), where Γ_S and Γ_L denote the reflection coefficient of source and load, respectively [3]. Based on the SCM technique, to achieve maximum gain at the first stage transistor the condition $\Gamma_{S1} = \Gamma_{IN1}^*$ and $\Gamma_{L1} = \Gamma_{OUT1}^*$ must be satisfied. This also applies for the second stage transistor, i.e. $\Gamma_{S2} = \Gamma_{IN2}^*$ and $\Gamma_{L2} = \Gamma_{OUT2}^*$. However, as the values of Γ_{L1} and Γ_{L2} are influenced by Γ_{OUT1} and Γ_{OUT2}, respectively, it is sometimes difficult to achieve the above condition.

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{1}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2}$$

Furthermore, in the NSCM technique, the values of Γ_{IN1} and Γ_{OUT1} for the first stage transistor as well as Γ_{IN2} and Γ_{OUT2} for the second stage transistor do not need to be calculated since the two-stage S-band LNA was designed under mismatch condition. Therefore, using this technique simplifies the mathematical calculations for the gain at a given value of the source impedance (Z_S) and the load impedance (Z_L). Since the proposed two-stage S-band LNA was designed under mismatch condition, the impedance mismatch factor (M) for each stage transistor, i.e. M_1 and M_2 for the first and second stage transistor respectively, is given in Eq. (3) [3]. It should be noted that the value of M is between 1 and 0, where a value of 1 means that the impedance is perfectly matched, while a value of 0 means that the impedance is fully mismatched. By determining the impedance mismatch factor, the value of VSWR can be theoretically obtained using Eq. (4) [3].

$$\mathrm{M} = \frac{\left(1 - |\Gamma_S|^2\right) \cdot \left(1 - |\Gamma_{IN}|^2\right)}{|1 - \Gamma_{IN}\Gamma_S|^2} \tag{3}$$

$$\mathrm{VSWR} = \frac{1 + \sqrt{1 - \mathrm{M}}}{1 - \sqrt{1 - \mathrm{M}}} \tag{4}$$

From Eqs. (3) and (4), if the value of M equals 1, it means that the value of VSWR is 1, or, in other words, the RF power signal from the source is fully transferred by the transistor. If the impedance is mismatched, mathematically expressed by a value of VSWR larger than 1 or a value of M smaller than 1, it means that some of the RF signal is reflected to the source, which is important in designing an impedance matching network. Furthermore, to calculate the transducer power gain (G_T), which indicates the gain capability of the two-stage S-band LNA, the relationship between the operating power gain (G_P) and the impedance mismatch factor (M), as expressed in Eq. (5), can be applied, where the value of G_P is given by Eq. (6) [3].

$$\mathrm{G_T} = \mathrm{G_P} \cdot \mathrm{M} \tag{5}$$

$$\mathrm{G_P} = \frac{\left(1 - |\Gamma_L|^2\right) \cdot |S_{21}|^2}{\left(1 - |\Gamma_{IN}|^2\right) \cdot |1 - S_{22}\Gamma_L|^2} \tag{6}$$

2.2 Circuit Design of Two-stage S-band LNA

After obtaining the required parameter values for the LNA design using the NSCM technique, the circuit design of the proposed two-stage S-band LNA was simulated by applying the ADS circuit simulation software. Figure 2 shows the circuit design of the two-stage S-band LNA equipped with DC biases as well as DC current blocks at the input and output ports. The value of each component for lumped elements is tabulated in Table 1.

It is noted that the component values of R_1, R_2, and R_3 can be obtained by applying a DC analysis to the first stage transistor with the desired gain and quiescent point [16]. The same procedure also applies to the component values of R_3, R_4, and R_5 for the second stage transistor. It shows that some radio frequency choke (RFC) components of L_1, L_2, L_3 and L_4 are connected to the transistor to avoid RF signal intrusion from the power supply into the circuit or vice versa. The component values of L_1, L_2, L_3 and L_4 can be calculated by taking into account the frequency of the power supply allowable to disturb the RF signal. Furthermore, C_1 and C_{13} are used to block the DC current in the circuit at the input and output ports. These component values are obtainable by determining the input or output port impedance of the circuit in correlation with the frequency of the RF signal. This procedure also applies to determining the component value of C_4. However, the use of DC current blocks often affects the increase of the base transistor current. Meanwhile, the remaining capacitors, i.e. C_2, C_3, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, and C_{12}, which are applied for smoothing the DC power supply and avoiding noise from the AC signal, can be determined by taking into account the frequency of RF signals allowable to interfere the DC power supply.

As shown in Figure 2, each stage of the LNA powered by a BFP420 type BJT was designed to produce a gain of around 15dB at a frequency of 3 GHz with values of VSWR and noise figure below 2 and 2.8 dB, respectively. To acquire the desired gain, the quiescent point of each transistor was chosen at I_c = 10 mA, β = 100, V_{be} = 0.7 Volt, V_{ce} = 2 Volt and V_{cc} = 5 Volt. One of methods to bias the transistors is by using a double-transistor method to provide a temperature-stable current source as implemented in [17]. However, this DC biasing circuit is too complicated since it needs an inductance emitter as negative feedback to increase the stability, which causes a decrease of overall gain. Hence, complicated DC biasing and negative feedback were avoided to prune the complexity of the design.

Based on the scattering parameter data of the transistor that are provided in the data sheet [18], the ADS circuit simulation software confirmed that the transistor had good stability operation at a frequency of 3 GHz with a value for

S_{11} of (0.54∠162.904°) dB, S_{12} of (0.075∠48.295°) dB, S_{21} of (4.24∠63.908°) dB, and S_{22} of (0.151∠-137.164°) dB. Furthermore, the values of Z_S and Z_L for each transistor could also be determined. They were (23.95-j6.65) Ω and (36.55-j10.7) Ω, respectively. From the result of Z_S and Z_L, as the input and output ports of the two-stage S-band LNA were set to 50 Ω, the impedance matching networks were required to compensate the impedance mismatch that occurs in each stage.

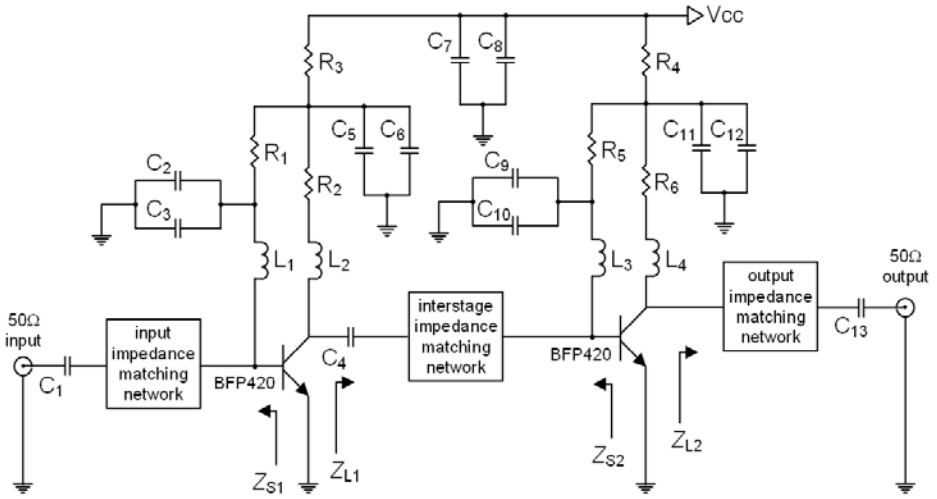

Figure 2 Circuit design of two-stage S-band LNA.

Table 1 Value of each component for lumped elements.

Resistors		Inductors		Capacitors	
R_1	30k1Ω	L_1	18nH	C_1	47pF
R_2	18 Ω	L_2	10nH	C_2	0.1μF
R_3	100 Ω	L_3	18nH	C_3	15pF
R_4	100 Ω	L_4	10nH	C_4	47pF
R_5	30k1 Ω	-	-	C_5	0.1μF
R_6	182 Ω	-	-	C_6	15pF
-	-	-	-	C_7	1nF
-	-	-	-	C_8	1nF
-	-	-	-	C_9	0.1μF
-	-	-	-	C_{10}	15pF
-	-	-	-	C_{11}	0.1μF
-	-	-	-	C_{12}	15pF
-	-	-	-	C_{13}	47pF

2.3 Determination of Impedance Matching Network

To determine the value of the impedance matching networks at the input and output ports, a graphical method using a Smith chart was applied. The input matching impedance network is required to fit the 50 Ω input impedance to the source impedance of the first stage transistor (Z_{S1}) of (23.95-j6.65) Ω. The Smith chart in Figure 3 shows the method to determine the input matching impedance network. As shown in Figure 4, the input matching impedance network was realized using an open parallel stub of 0.109λ (l_{s1}) connected to a microstrip line of 0.067 λ (l_{m1}), where λ denotes the wavelength at a frequency of 3 GHz on the dielectric substrate used for deployment. Here, the use of microstrip lines for the input matching impedance network was also done to minimize parasitic effects, which may cause oscillation in the two-stage LNA. The microstrip line was also implemented as the impedance matching network at the output port as well as at the interstage between transistors.

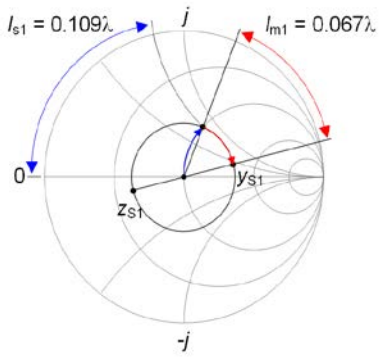

Figure 3 Determination of input matching impedance network using Smith chart.

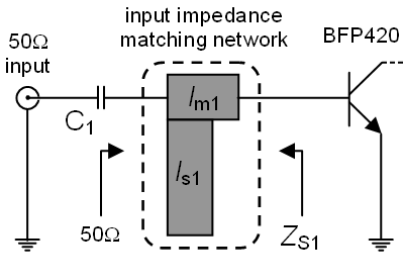

Figure 4 Realization of input matching impedance network using a microstrip line.

By using the graphical method using a Smith chart, the output matching impedance network was determined to match the load impedance of the second stage transistor (Z_{L2}) of (36.55-j10.7) Ω to the 50 Ω output impedance. Figure 5 illustrates the method to obtain the output matching impedance network, which was realized using an open parallel stub of 0.06λ (l_{s2}) connected to a microstrip line of 0.202λ (l_{m2}), as shown in Figure 6. Moreover, the interstage impedance matching network was required to match the load impedance of the first stage transistor (Z_{L1}) of (36.55-j10.7) Ω to the source impedance of the second stage transistor (Z_{S2}) of (23.95-j6.65) Ω. The method to determine the interstage impedance matching network using a Smith chart is illustrated in Figure 7, where the realization uses a microstrip line of 0.147λ (l_{is}), as shown in Figure 8.

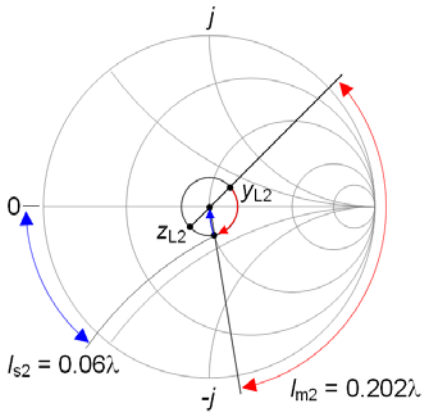

Figure 5 Determination of output matching impedance network using a Smith chart.

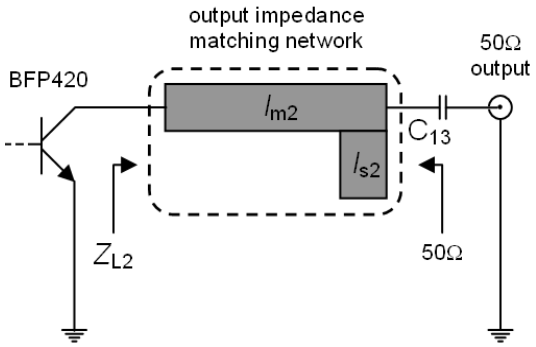

Figure 6 Realization of output matching impedance network using a microstrip line.

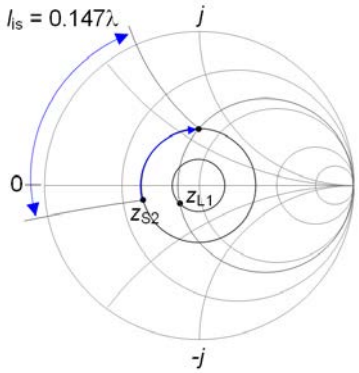

Figure 7 Determination of interstage matching impedance network using a Smith chart.

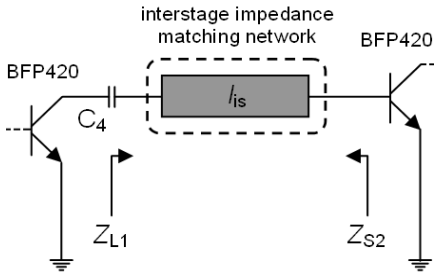

Figure 8 Realization of output matching impedance network using a microstrip line.

Since the proposed two-stage S-band LNA was deployed on an Arlon DiClad527 dielectric substrate with a thickness of 1.02 mm and a relative permittivity of 2.5, by using equations from [19] the physical length of the microstrip lines could be calculated. Table 2 summarizes the electrical length of the microstrip lines determined using a Smith chart and the physical length obtained from the calculation. It should be noted that the width of each microstrip line was 2.95 mm, which corresponds to an impedance line of 50 Ω.

Table 2 Electrical and physical lengths of microstrip lines.

Microstrip line	Electrical length (λ)	Physical length (mm)
l_{s1}	0.109	7.56
l_{m1}	0.067	4.65
l_{is}	0.147	10.2
l_{s2}	0.06	4.2
l_{m2}	0.202	14.02

Prior to hardware realization, the final design of the two-stage S-band LNA was numerically characterized through the ADS software. Figure 9 plots the simulated results of noise figure and overall gain, while the simulated results of $VSWR_{IN}$ and $VSWR_{OUT}$ are depicted in Figure 10. It can be seen that the overall gain of LNA was almost flat for frequencies lower than 3 GHz and decreased significantly for the rest frequency.

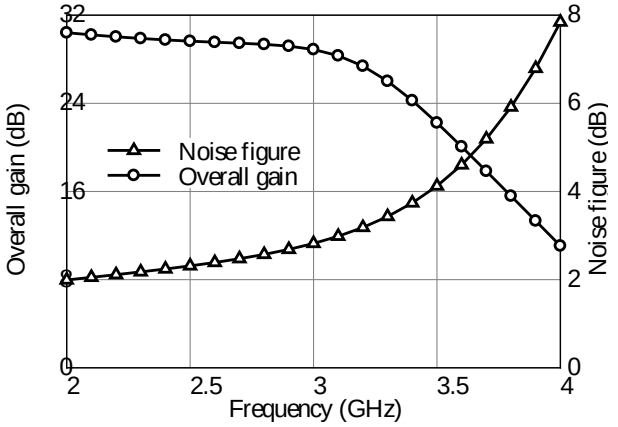

Figure 9 Simulated results of noise figure and overall gain.

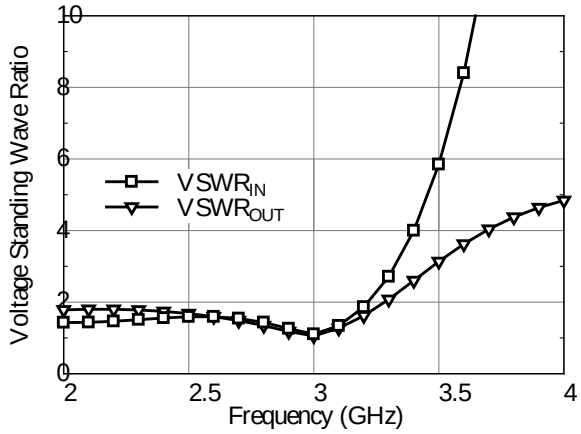

Figure 10 Simulated results of $VSWR_{IN}$ and $VSWR_{OUT}$.

A similar tendency but in the opposite direction was shown by the noise figure. This is probably evoked by the used transistors, which have appropriate gain and noise figure for frequencies lower than 3 GHz. It is noted that the gain and noise figure at a frequency of 3 GHz, i.e. 28.88 dB and 2.82 dB respectively,

were slightly outside of the specification but both values are still acceptable. Meanwhile, from the VSWR results it seems that the phenomena found in the gain and noise figure also occurred. The circuit has good impedance matching as the prediction for the frequency was less than 3 GHz. However, for the rest frequency the value of VSWR for both the input and output ports increased remarkably, which was caused by the impedance mismatch at the input of the first stage transistor and the output of the second stage transistor. The result demonstrates that the value of VSWR at the input port ($VSWR_{IN}$) was 1.11 at a frequency of 3 GHz, while at the output port ($VSWR_{OUT}$) it was 1.05.

3 Hardware Realization and Measurement

According to the final circuit design explained in the previous section, a prototype of the two-stage S-band LNA was realized and experimentally characterized. Figure 11 shows a picture of the printed circuit board (PCB) for deploying the two-stage S-band LNA on an Arlon DiClad527 dielectric substrate. Meanwhile, Figure 12 shows a picture of the realized two-stage S-band LNA prototype with SMD (surface-mount device) components for resistors, inductors and capacitors.

To avoid signal interference from the outside or vice versa, the prototype was placed inside a metal (aluminum) box. Two SMA connector types were soldered at the input/output ports of the prototype for the experimental characterization. The measurement results are shown in Figures 13-16 for noise figure, overall gain, $VSWR_{IN}$, and $VSWR_{OUT}$, respectively. For comparison, the simulated results for each respected parameter were also plotted together. Due to the unavailability of an instrument for noise figure characterization, the measured noise figure shown in Figure 13 was obtained from the correlation of the measured gain of the prototype instead of by direct measurement.

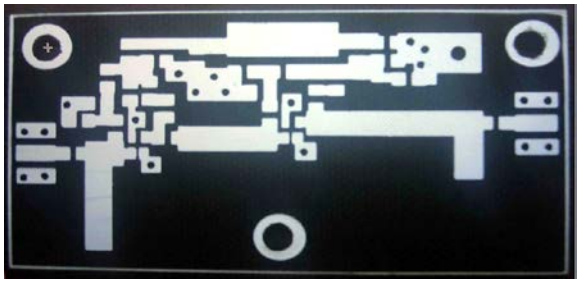

Figure 11 Image of the printed circuit board S for deployment of the two-stage S-band LNA.

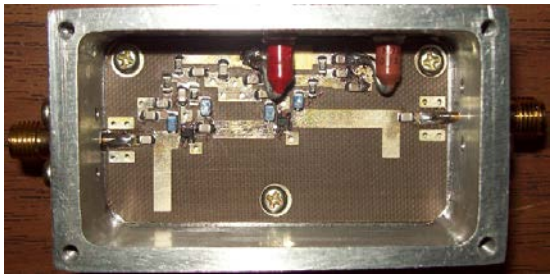

Figure 12 Picture of the two-stage S-band LNA prototype inside the metal box.

From Figure 13 it can be seen that the measured noise figure coincided with the simulated one for frequencies higher than 3.5 GHz. Meanwhile, in the rest frequency, the measured noise figure was higher than the simulated result and tended to increase for the frequency range of 2.5-3 GHz. The same was the case for the measured gain plotted in Figure 14 but in the opposite manner. From the results, the noise figure and gain of the two-stage S-band LNA prototype at a frequency of 3 GHz were 3.58 dB and 22.77 dB, respectively, i.e. worse than the simulated values at the same frequency, with a gain of 28.88 dB and a noise figure of 2.82 dB. The discrepancy between the measured results and the simulated ones was possibly caused by a different parameter value in the Arlon DiClad527 dielectric substrate, i.e. dielectric loss, used for realizing the prototype, which had a higher dielectric loss value than in the simulation. When the value of the dielectric loss is higher, some amount of energy from the input port that should actually be transmitted to the output port is absorbed by the dielectric substrate, causing a decrease of measured gain.

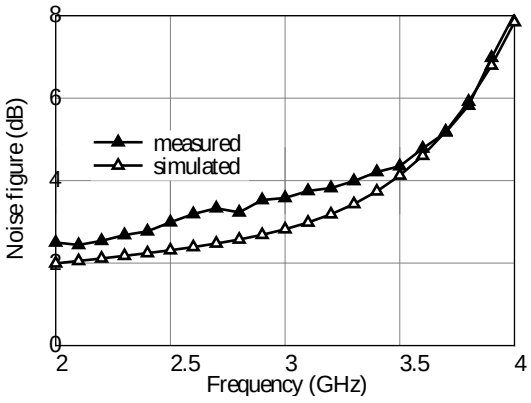

Figure 13 Measured noise figure of the realized LNA with simulated result for comparison.

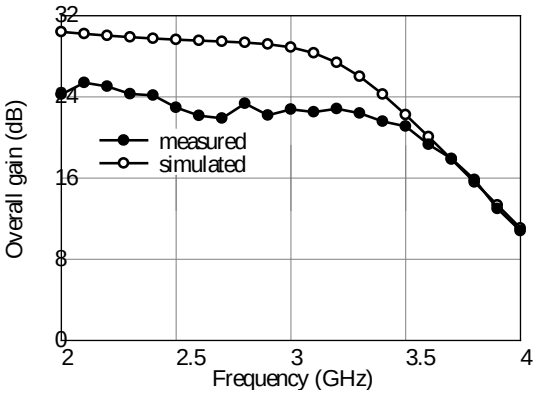

Figure 14 Measured gain of the realized LNA with simulated result for comparison.

Different measurement results were also found for the values of VSWR at the input and output ports as plotted in Figures 15 and 16, respectively. Generally, both VSWR values were shifted to a higher frequency range. The measured $VSWR_{IN}$ and $VSWR_{OUT}$ at a frequency of 3 GHz were 5.49 and 3.44, respectively, while the simulated values were 1.11 and 1.05, respectively. The difference in measured results of VSWR was probably evoked by the different value of relative permittivity of the dielectric substrate used in the realization.

From the results it can be inferred that the actual value of relative permittivity seemed to be lower than in the simulation. If the actual relative permittivity is lower, then the value of the impedance matching networks, i.e. the microstrip lines, becomes larger, causing an increase of the VSWR value.

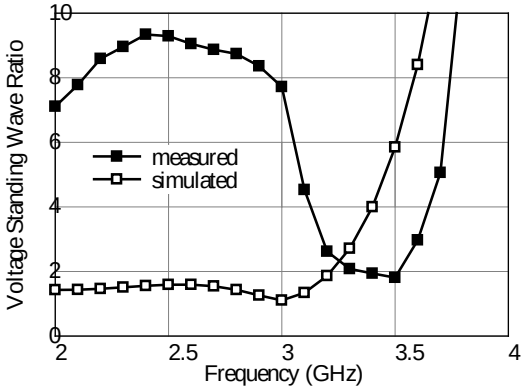

Figure 15 Measured $VSWR_{IN}$ of the realized LNA with simulated result for comparison.

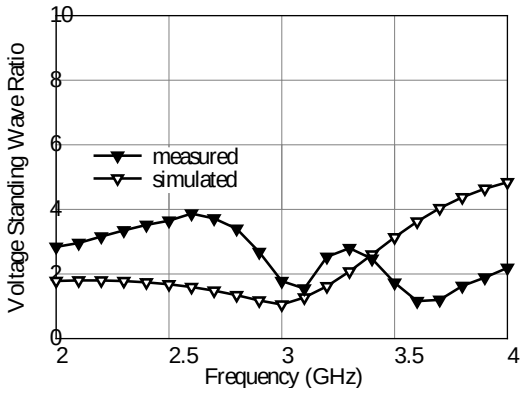

Figure 16 Measured $VSWR_{OUT}$ of the realized LNA with simulated result for comparison.

4 Conclusion

A two-stage LNA working at the S-band frequency was developed by using of the non-simultaneous conjugate match technique and was realized on an Arlon DiClad527 dielectric substrate for experimental characterization. It was shown that using the NSCM technique could reduce unnecessary calculation of the values of Γ_{IN} and Γ_{OUT} for determining the impedance matching network. The characterization results demonstrated that the realized two-stage S-band LNA produced a gain of 22.77 dB at a frequency of 3 GHz with values for $VSWR_{IN}$ and $VSWR_{OUT}$ of 5.49 and 3.4, respectively. The experimental characterization results were worse in some frequency ranges than the design results, which indicates the need of improvement. However, in general, the prototype of the two-stage S-band LNA showed acceptable performance and the same tendencies as the simulated ones.

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