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Solution-Processed Perovskite Field-Effect Transistor Artificial Synapses

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Metal halide perovskites are distinctive semiconductors that exhibit both ionic and electronic transport and are promising for artificial synapses. However, developing a 3-terminal transistor artificial synapse with the perovskite channel remains elusive due to the lack of a proper technique to regulate mobile ions in a non-volatile manner. Here, a solution-processed perovskite transistor is reported for artificial synapses through the implementation of a ferroelectric gate. The ferroelectric polarization provides a non-volatile electric field on the perovskite, leading to fixation of the mobile ions and hence modulation of the electronic conductance of the channel. Multi-state channel conductance is realized by partial ferroelectric polarization. The ferroelectric-gated perovskite transistor is successfully used as an artificial synapse that emulates basic synaptic functions such as long-term plasticity with excellent linearity, short-term as well as spike-timing-dependent plasticity. The strategy to regulate ion dynamics in the perovskites using the ferroelectric gate suggests a generic route to employ perovskites for synaptic electronics.

1. Introduction

Emulation of memory/computing functions of the brain is promising for overcoming the limitations of traditional computing systems in the analysis and perception of real-world

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and unstructured data.[1,2] In a brain, information is stored in a synapse where a cleft connects two nerve cells (neurons). In response to input stimuli arriving on a pre-neuron, neurotransmitters are secreted from the pre-neuron, bind to receptors on a post-neuron, and regulate ion transport channels (**Figure 1**a).[3] The ion's dynamic through the channel plays a crucial role in strengthening/weakening synaptic weight by activating/deactivating the formation of ion-permeable channels (i.e., conductance update).[3] Depending on the pre-synaptic stimuli, the synaptic weight is maintained temporally or lasts for minutes, hours, or even longer and can act as a memory state. Development of an artificial synapse in which the conductance is updated by ion-like dynamics would closely mimic the behavior of the biological synapse and could eventually emulate a variety of biological neural operations.

Drift memristors have succeeded in mimicking conductance updates with long-term potentiation (LTP) and long-term depression (LTD) characteristics but are intrinsically stochastic[4] and require additional diffusive components to mimic ion dynamics.[5] A 3-terminal device structure, such as a transistor, allows for regulating ions and is, therefore, a promising candidate for artificial synapses.[6–13] An electrolyte-gated transistor enables control of the ions without additional circuitry.[6,7] However, achieving long-term plasticity has been challenging in electrolyte-gated transistors, mainly because of device instability arising from, for instance, parasitic electrochemical reactions at the contacts.[6–8] A ferroelectric field-effect transistor (FeFET) provides an excellent device architecture to control the synaptic weight by programming/erasing non-volatile multi-conductance states through control over polarization of the ferroelectric gate.[9] Ferroelectric gates have been used for adjusting the conductance of FeFETs that employ various semiconductors as the channel material ranging from indium gallium zinc oxide (IGZO),[9–11] to 2-dimensional materials,[12,13] and polymers.[42] However, the emulation of the ionic dynamics with semiconducting materials that lack ions is hardly achievable. Therefore, a channel material capable of conducting ions that can maintain its electronic structure is needed.

Metal halide perovskite semiconductors are promising materials for artificial synapses due to their unique ionic-electronic mixed conduction characteristics.[14–16] Remarkable electronic conduction properties such as high mobility, large diffusion length, and long lifetime of charge carriers make
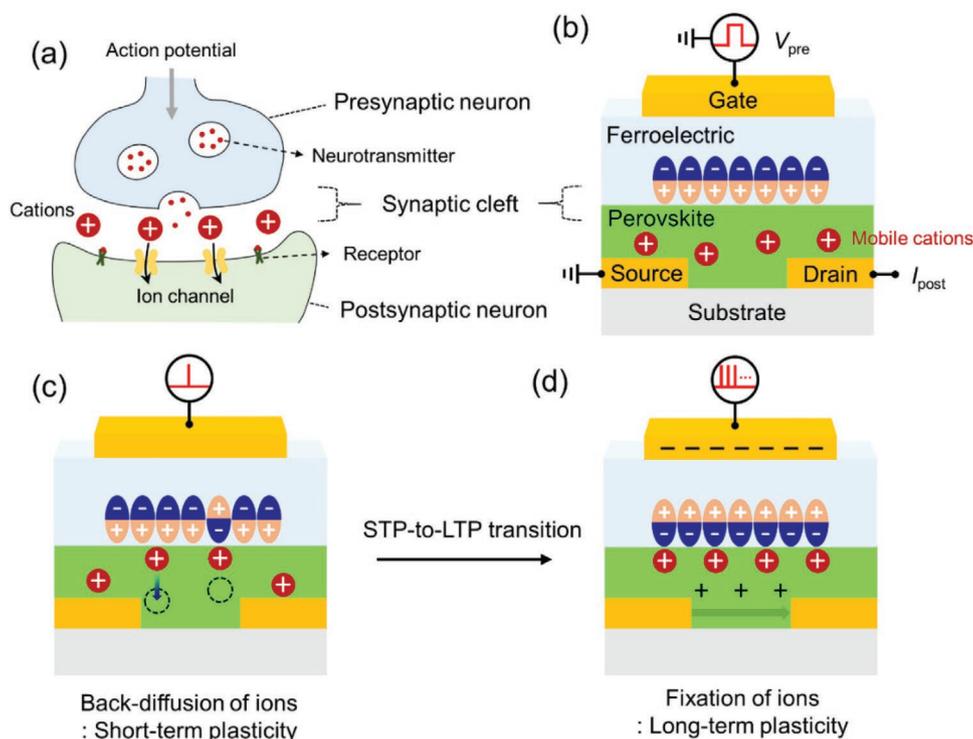
Figure 1. Schematics for perovskite transistor artificial synapse (PeTAS) working principles. a) A biological synapse wherein an action potential on a pre-synaptic neuron secretes neurotransmitters, which bind to receptors on a post-synaptic neuron and activate the ion channel to be permeable to cations. Dynamic balance of an ion concentration across a membrane of the post-synaptic neuron regulates the conductance of the synapse. b) The PeTAS employs an architecture of a perovskite transistor comprising of a top gate electrode, a ferroelectric gate insulator, perovskite channel, source, and drain electrodes, respectively. The ferroelectric-perovskite interface emulates the synaptic cleft where the electronic conductance is modulated. Pre-synaptic spike (V_{pre}) is applied on the gate, and post-synaptic current (I_{post}) is read at the drain to probe conductance states. As a low conductance state, the direction of the ferroelectric polarization points downward. Hypothetic mobile cations (red circle) are distributed inside the bulk, disturbing an electronic transport in the perovskite channel. c) When a single short negative pulse is applied, the mobile cations are attracted but back-diffused due to the dominant downward ferroelectric polarization, emulating short-term plasticity. d) When a long train of negative pulses is applied, the ferroelectric polarization is fully reversed upward and stabilized by the ionic charges from the mobile cations. The perovskite channel shows a high electronic conductance, exhibiting long-term plasticity.

the perovskites highly promising for application in synaptic devices.[17] Excellent optoelectronic properties such as high absorption coefficient, high photon-to-electron conversion efficiency, and facile bandgap tunability are further advantageous for realizing photonic synapses.[18–22] Moreover, ion transport behavior in perovskite, frequently observed as hysteresis in current-voltage loops, can endow memory states at various timescales for artificial synaptic memory.[16–18] Furthermore, perovskites are responsive to various stimuli such as light, pressure,[23] or chemical species,[24] which are potentially useful for artificial sensory synapses. Therefore, perovskites hold great promise for the implementation of artificial synapses.

Previous perovskite artificial synapses have mainly focused on 2-terminal resistive devices based on electrochemical metallization or vacancy-driven ion migration.[25–29] The 2-terminal devices have the merits of the simple device structure and scalability. However, the electrochemical process is an intrinsically destructive weight update that results in stochasticity, significant noise and involves power- and time-consuming filament-forming processes. The ion migration mechanism exhibits poor long-term plasticity because ions diffuse back to their equilibrium position in the absence of an external electric field. Moreover, due to the intrinsic electronic conductivity of perovskites,

a sizeable parasitic leakage current is usually observed in 2-terminal devices, potentially limiting the number of achievable conductance states. A 3-terminal transistor architecture advantageously allows for non-destructive operation as programming and reading processes are decoupled. Functional expandability, reduced sneak paths, and improved controllability of synaptic characteristics are further advantages of a transistor geometry for perovskite-based synapses. However, 3-terminal perovskite transistor artificial synapses remain undeveloped due to the lack of proper techniques that enable reproducible regulation of the ion transport in the perovskite channel. Perovskites have only been used as an auxiliary component for instances as photo-induced charge trapping centers.[30–32] So far, little attention has been paid to the unique semiconducting-ionic properties of the perovskites and their potential for application as the active semiconducting material in a FET channel for neuromorphic device applications.

In this work, we develop a perovskite transistor artificial synapse (PeTAS) wherein a ferroelectric gate modulates ion transport in the perovskite channel. The ferroelectric gate provides a programmable non-volatile electric field that can regulate mobile ions and the electronic conductance of the perovskite channel. The PeTAS emulates a biological synapse, as shown

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in Figure 1b–d. The ferroelectric-perovskite interface mimics the synaptic cleft, as depicted in Figure 1a,b. The gate and drain electrodes mimic the pre-neuron and post-neuron, where pre-synaptic voltage (V_{pre}) and post-synaptic current (I_{post}) are applied and measured, respectively. The conductance of the perovskite channel represents the synaptic weight. When the ferroelectric layer has a downward remanent polarization, the electronic conductance of the perovskite channel is significantly suppressed because the mobile cations disturb the hole charge transport (Figure 1b).

When a negative bias is applied to the gate to reverse the polarization, the mobile cations are attracted and fixated by the upward ferroelectric polarization. The channel conductance is increased with the depletion of the mobile cations. When a short pulse of the negative bias is applied, the ferroelectric layer cannot fully polarize, and most of the cations diffuse back due to a sizeable repulsive force from the dominant downward polarization (Figure 1c). The channel conductance is temporarily maintained but quickly decays, emulating short-term plasticity. When a long train of pulses is applied that can fully reverse the ferroelectric polarization, the positive ionic charges of the mobile cations stabilize the upward ferroelectric polarization (Figure 1d). As the mobile cations are depleted, the perovskite channel exhibits a high conductance. Short-term plasticity transitions to long-term plasticity. The PeTAS functions as a long-term memory. It is shown here that PeTAS exhibits excellent electronic memory functionalities with a high ON/OFF current ratio, stable data retention, and good cycle endurance. Different states of the perovskite channel's conductance are achieved by the partial remanent polarization of the ferroelectric gate. Essential synaptic functions such as long-term potentiation (LTP) and long-term depression (LTD) characteristics with excellent linearity and spike-timing-dependent plasticity (STDP) learning rules are successfully demonstrated. Our results show that PeTAS offers a generic and straightforward route to regulate the ionic and electronic transport in perovskites and mimics the behavior of biological synapses.

2. Results and Discussion

The PeTAS consists of the perovskite channel and a ferroelectric gate dielectric with a top-gate bottom-contact configuration (Figure 1b). As the perovskite layer, $CsPbBr_3$ is used, which is known as a p-type semiconductor in which cations are dominant mobile ionic species.[33,34] Solution-processed polycrystalline $CsPbBr_3$ is an electronic and ionic conductor with an ionic surface charge density that reaches up to 1 μC cm^{-2}.[33–35] Polymer poly(vinylidene fluoride-co-trifluoroethylene) [P(VDF-TrFE)] is used as the ferroelectric layer. P(VDF-TrFE) can provide a non-volatile surface charge density of ±7–8 μC cm^{-2}, which is comparable to that of the ionic surface charge density in the $CsPbBr_3$ channel. The choice of the $CsPbBr_3$ perovskite channel is motivated by its ambient stability and resistance to the solvent (methylethylketone, MEK) from which the P(VDF-TrFE) is processed.[36]

The thin $CsPbBr_3$ film for the FET channel is fabricated by anti-solvent quenching (see the Experimental section for detail). An atomic force microscopy (AFM) height image, given

in **Figure 2**a, shows the surface morphology of the $CsPbBr_3$ film. The film is highly uniform and compact with a pinhole-free polycrystalline morphology over a large area with an average grain size of ≈172 ± 55 nm. The thickness of the film is ≈55 ± 5 nm. Figure 2b shows a high-resolution X-ray diffraction (HR-XRD) pattern of the $CsPbBr_3$ film. A typical orthorhombic crystal structure is observed without any impurity peaks.[37] The UV-vis absorbance spectrum shows that the optical property of the $CsPbBr_3$ film is in line with the typical polycrystalline $CsPbBr_3$ film, as shown in Figure 2c. The $CsPbBr_3$ film is not damaged by MEK, which is used as the solvent for spin-coating of the atop P(VDF-TrFE) film. We note that additives, typically used for improving crystallinity and electrical properties of the perovskite, are not introduced during the film processing to simplify the analysis of the device behavior.

Figure 3a shows the electrical characteristics of the $CsPbBr_3$ transistor where the P(VDF-TrFE) gate modulates the conductance in the $CsPbBr_3$ channel and provides binary memory states. The p-type transfer characteristic is exhibited with a modulated hole current, as shown in Figure 3a. The charge carrier mobility and the threshold voltage of the perovskite transistor are 2.1×10^{-4} cm^2 V^{-1} s^{-1} (± 9.9×10^{-5} cm^2 V^{-1} s^{-1}) and −28.5 V (±4.10 V) for the backward direction (positive-to-negative gate bias), and 9.2×10^{-5} cm^2 V^{-1} s^{-1} (±5.1×10^{-5} cm^2 V^{-1} s^{-1}) and 1.80 V (±9.12 V) for the forward direction (negative-to-positive), respectively (Figure 3b,c). For all cases, a clockwise hysteresis in the I_D–V_G transfer curve with a large ON/OFF current ratio of about 1.9×10^3 is observed, as shown in Figure 3d. The ferroelectric switching occurs at $V_G = −42$ V and $V_G = +33$ V as confirmed by the displacement peaks in the gate current, which appears at the expected coercive voltages for a 700 nm-thick P(VDF-TrFE) film. When the P(VDF-TrFE) gate is swept to negative gate voltages, mobile cations are attracted to the top surface and stabilize the upward ferroelectric polarization. Counter-anions in the opposite sites act as acceptor-type defects that can provide additional free hole charge carriers to the channel.[33,34] As the P(VDF-TrFE) gate bias is reversely swept to positive gate voltages, cations are pushed back to the bulk. Counter-anions compensate for the downward ferroelectric polarization. However, the drain current is significantly reduced because the $CsPbBr_3$ perovskite is a p-type semiconductor and lacks electrons. In stark contrast, the perovskite transistor with a non-ferroelectric gate dielectric of polytrifluoroethylene (PTrFE), instead of P(VDF-TrFE), does not respond to gate bias (Figure S1, Supporting Information), indicating that the transistor function with the memory effect is mainly originated from the ferroelectric polarization.

For the ferroelectric-gated perovskite FETs, the dominant hysteresis process is due to the ferroelectric polarization, as clearly shown by the gate displacement current, Figure 3a, where the switching of the source-drain current from a low to a high current coincides with the appearance of the polarization switching peak in the gate displacement current.[42] We note that hysteretic transfer characteristics in perovskite FETs have been observed previously for bottom-contact bottom-gate device layout with a non-ferroelectric SiO_2 gate and attributed to charge trapping at the interface between the dielectric and the perovskite layer.[43] For a p-type channel FET, trap-related transfer curves show a counter-clockwise hysteretic loop,
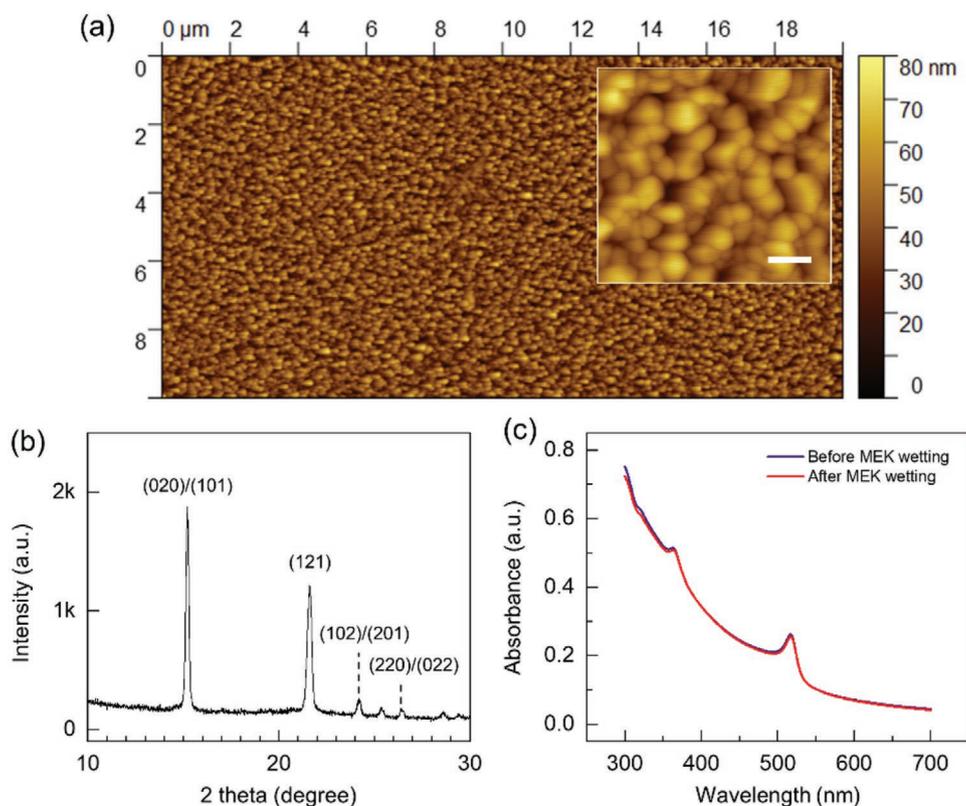
Figure 2. Characterization of the solution-processed $CsPbBr_3$ film used as a channel in the perovskite transistor. a) Tapping mode AFM height image of the surface of the $CsPbBr_3$ film. The inset shows a magnified image. The scale bar is 200 nm. b) HR-XRD pattern of the $CsPbBr_3$ film. The crystallographic planes of an orthorhombic crystal structure of polycrystalline $CsPbBr_3$ are indexed. c) UV-vis absorbance spectra of the $CsPbBr_3$ film. The UV-vis absorbance spectrum of the $CsPbBr_3$ film wet (immersed) by MEK solvent is compared.
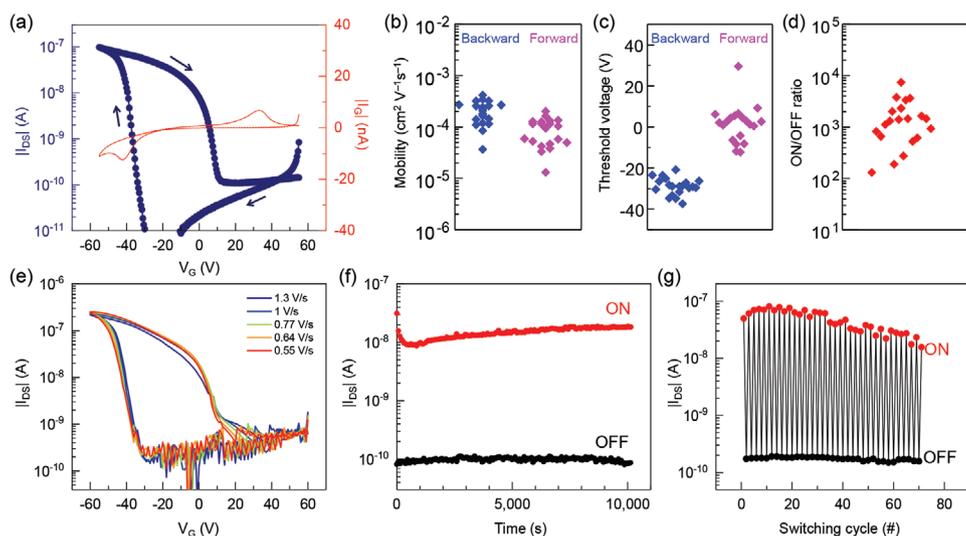

Figure 3. Electrical characteristics of the $CsPbBr_3$ transistor used for the perovskite transistor artificial synapse (PeTAS). a) Transfer I_{DS}–V_G characteristic. The arrows indicate the sweeping direction. Gate current (I_G) is also provided to show the occurrence of ferroelectric switching. V_D is −5 V. Statistics of b) charge carrier mobility, c) threshold voltage, and d) ON/OFF ratio (read at $V_G = 0$ V) of the $CsPbBr_3$ transistor. The charge carrier mobility and the threshold voltage are extracted from both the backward and forward sweep directions. More than 20 devices have been tested. e) Scan-rate-dependent transfer characteristics. The scan rate is controlled from 0.55 V s^{-1} to 1.3 V s^{-1}. f) Data retention with time and g) switching cycle endurance. A high conductance is programmed by sweeping the gate from $V_G = 0$ to $V_G = -50$ V (represented by "ON"), whereas a low conductance state is achieved by sweeping to $V_G = +50$ V (represented by "OFF"). The drain current (I_{DS}) is read at $V_G = 0$ V and $V_D = -5$ V.
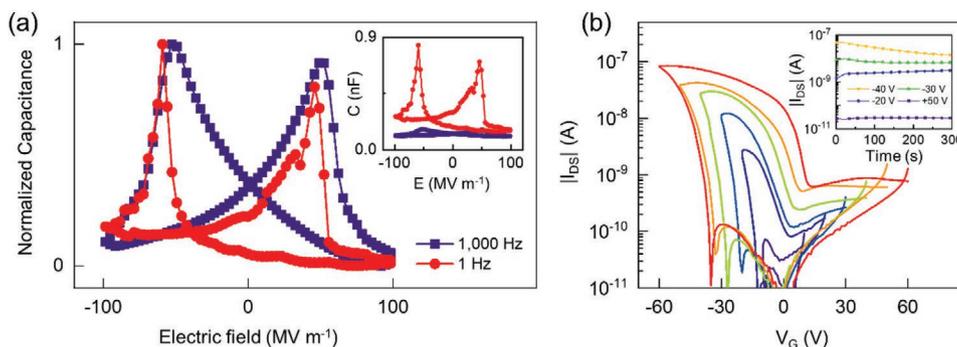
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Figure 4. a) C–E characteristics of the MFS diode with a stack of top Au/P(VDF-TrFE)/CsPbBr$_3$/bottom Au measured at a frequency of 1 Hz and 1000 Hz. The voltage is applied to the top Au electrode. The bottom Au is grounded. The capacitance is normalized to show the symmetry of the loops explicitly. The inset shows the C–E loops before normalization. b) Transfer characteristics of the CsPbBr$_3$ transistor swept with a V_G range of ±10, ±20, ±30, ±40, ±50, and ±60 V, respectively. The inset shows data retention swept to V_G = +50, −20, −30, −40 V.

where the current for the backward transfer sweep is always lower than the forward sweep current because the trapped charges screen the gate field. The situation is reversed with a ferroelectric gated p-type channel FET, i.e., the transfer characteristic shows a clockwise hysteresis loop where the current for the backward gate sweep is always higher than the forward sweep because of the (partial) polarization of the ferroelectric and formation of a charge accumulation layer in the channel. Observation of a clockwise hysteresis direction even for partially polarized PeTAS, as demonstrated in **Figure 4**b, indicates that the ferroelectric polarization overwhelms charge trapping and is the prevailing hysteretic mechanism in PeTAS. Furthermore, Figure 3e shows that the ferroelectric hysteretic behavior is not affected by changing a gate bias scan rate from 0.55 V s^{-1} to 1.3 V s^{-1}. The CsPbBr$_3$ transistor exhibits bistable conductance states at V_G = 0. The data retention of the static ON- and OFF-states and their cycle endurance are presented in Figures 3f,g. The high and low conductance states are programmed upon sweeping the gate to V_G = −50 V and V_G = +50 V, respectively. The channel conductance is probed by measuring the drain current at V_G = 0 V and a low drain bias. The drain current for the high and low conductance states remains constant at 10^{-8} A and 10^{-10} A in time (measured up to 10^4 s), respectively, as shown in Figure 3f. The current ratio remains larger than 10^2 after repetitive switching over 70 times, as shown in Figure 3g.

Field-effect mobility crucially depends on the roughness between the gate dielectric and the semiconductor. A rough interface (even for root-mean-square, rms, roughness below 1 nm)[44] has a severe negative influence on the field-effect mobility. In a top-gated device, as in the case of PeTAS, the roughness of the semiconductor is the limiting factor for achieving high field-effect mobilities. The film formation process is optimized to achieve a very smooth film, and the rms roughness amounts to only 5 nm, which is a factor of 10 larger than the typical roughness of thermally grown SiO$_2$ that is typically used for the fabrication of the perovskite transistors.[43] Hence, obtaining the low field-effect mobility is more due to the roughness of the perovskite layer, rather than the perovskite material itself.

The depletion of the mobile cations in the CsPbBr$_3$ channel by the ferroelectric polarization is supported by measuring the capacitance-electric field (C–E) characteristics of the metal-ferroelectric-semiconductor (MFS) diodes. Figure 4a shows normalized C–E characteristics of an MFS diode with Au/P(VDF-TrFE)/CsPbBr$_3$/Au stack. At a sufficiently high frequency of 1 kHz, ions do not follow the change in the electric field. Therefore, the MFS diode exhibits a symmetric butterfly C–E loop with the peaks at a coercive field of E_C = ±50 MV m^{-1} without a notable sign of the mobile ions. However, the movement of the ions is strongly activated at a low frequency of 1 Hz.[34,35] A strong asymmetry in the C–E loop at 1 Hz is observed with a negatively shifted ferroelectric switching, implying the presence of the mobile cations. The mobile cations partly screen the applied negative gate bias. Therefore, a much stronger bias is needed to fully polarize the ferroelectric. The mobile cations can be quantitatively regulated through partial polarizations with different poling voltage sweeps. The CsPbBr$_3$ transistor swept at different ranges of V_G = ±10, ±20, ±30, ±40, ±50, and ±60 V, respectively, exhibits multiple loops with discrete conductance states at V_G = 0 V with stable retention in time, as shown in Figure 4b. The programmable conductance with multi-states allows for the emulation of a synapse and analog adjustment of the synaptic weight in response to electrical stimulation, and therefore CsPbBr$_3$ transistor can be used as an artificial synapse.

The conductance of the PeTAS can be updated with discrete multi-states upon consecutive pulses. The LTP and LTD characteristics exhibit excellent linearity, as shown in **Figure 5**a. LTP is achieved by pulsing 50 times with an amplitude of V_{pre} = −30 V and a width of 20 ms, whereas LTD is realized with the same condition as the LTP, however, at a lower bias of V_{pre} = +15 V. The lower amplitude of the pulse for LTD is necessary because of a strong repulsive electrostatic force between the accumulated cations and the depolarization of the ferroelectric. The amplitude of V_{pre} = +30 V and +20 V for LTD leads to the earlier transition from high to low conductance state, while +10 V cannot fully reverse the state, as shown in Figure 5b. The width of the pulse is essential in achieving high linearity. A short pulse width of 5 ms cannot fully reverse the polarization, possibly due to the remaining cations at the ferroelectric surface, whereas a pulse width longer than 100 ms yields fast saturation of the potentiation and earlier depression, as shown in Figure 5c. The LTP and LTD withstand

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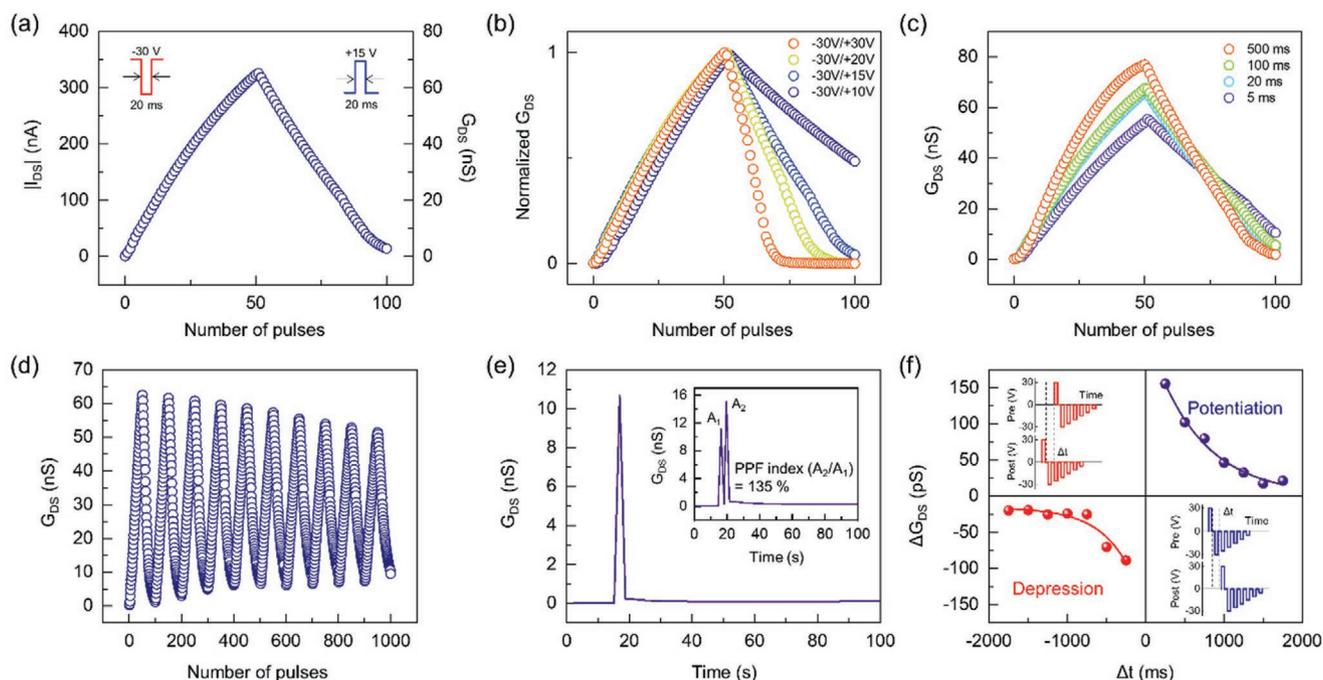
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Figure 5. Synaptic behaviors of the perovskite transistor artificial synapse (PeTAS). a) Long-term potentiation (LTP) and long-term depression (LTD) characteristic of the PeTAS of which the channel conductance is updated by multiple pulses up to 50 times for LTP and LTD, respectively. The amplitude and width of the pulse used for LTP (−30 V, 20 ms) and LTD (+15 V, 20 ms) are represented in the inset. b) LTP and LTD characteristics dependent on the pulse amplitude of LTD. The width is fixed to 20 ms. c) LTP and LTD characteristics dependent on the pulse width. The amplitude is set to −30 V for LTP and +15 V for LTD. d) Multiple cycles of the conductance updates by LTP and LTD. e) Short-term plasticity with a conductance update by a single pulse (−30 V for 20 ms). The inset shows a PPF characteristic with time. f) Demonstration of spike-timing-dependent plasticity (STDP). Spikes of the waveform represented in the inset are applied on a gate and a drain with a delay of Δt. A conductance change from a preset high conductance is probed for depression, whereas a conductance change from a preset low conductance is probed for potentiation.

repetitive switching up to 1000 times, as shown in Figure 5d. We note that the cycle endurance slightly degrades upon prolonged cycles (Figure 5d and Figure 2g), possibly due to the fatigue of the P(VDF-TrFE).[38] We believe that fatigue-resistant ferroelectrics like nylons or δ-PVDF can improve the cycle endurance.[39,40]

The LTP behavior indicates that a single pulse width of 20 ms does not switch the polarization of the P(VDF-TrFE), but cumulative pulses gradually reverse the polarization. The single pulse, therefore, can be used to emulate volatile characteristics for short-term plasticity. The conductance is slightly increased by a single pulse and exhibits paired-pulse facilitation (PPF) behavior with the PPF index of 135%, as shown in Figure 5e. The updated conductance with the single or paired-pulse quickly decays to the original state due to the back-diffusion of the cations, exhibiting short-term plasticity.

The conductance can be updated by applying the pre- and post-neuron spikes on a gate (V_{pre}) and on a drain (V_{post}) with a close timing of Δt, as shown in Figure 5f. The spike is designed as the waveform to transitorily exceed a coercive voltage of the ferroelectric gate when the V_{pre} and V_{post} spikes overlap.[41] The conductance increases when V_{post} follows V_{pre} ($\Delta G > 0$, synapse strengthening) whereas the conductance decreases when V_{pre} follows V_{post} ($\Delta G < 0$, synapse weakening). Closely overlapped spikes primarily change the conductance, whereas long delays only produce a marginal conductance change, demonstrating the STDP learning rule.

3. Conclusion

We have developed a 3-terminal artificial synapse based on a perovskite transistor. A ferroelectric gate is utilized to regulate mobile ions in the perovskite channel. The electronic conductance of the perovskite is successfully modulated because the non-volatile electric field from the remanent polarization of the ferroelectric fixates the mobile ions in the perovskite. Partial remanent polarization of the ferroelectric gate enables the realization of the multi-state conductances. The perovskite transistor exhibits synaptic functions such as LTP and LTD behaviors with excellent linearity, short-term plasticity, and STDP. Our strategy to regulate the mobile ions and emulate synaptic plasticity using the ferroelectric gate is a generic route and potentially applicable to various ionic-electronic mixed conductors for realizing hardware for future artificial intelligence.

4. Experimental Section

Materials: P(VDF-TrFE) copolymer (VDF:TrFE = 75:25) and PTrFE were purchased from Solvay. CsBr (99.9%), PbBr$_2$ (99.999%), DMSO, chlorobenzene and MEK were purchased from Sigma-Aldrich.

Device Fabrication: The CsPbBr$_3$ transistor was fabricated on the glass substrate cleaned by detergent, distilled water, acetone, and 2-propanol. For the source/drain electrodes, Cr (1 nm) and Au (50 nm) were sequentially deposited on the cleaned glass substrate by thermal evaporation with a pre-defined shadow mask with the channel length

and width of 25 and 5000 μm, respectively. The source/drain substrate was treated by UV-oxygen plasma for 20 min before spin-coating the perovskite precursor solution. The precursor powders were dissolved in DMSO (200 mg ml^{-1}, CsBr:PbBr$_2$ = 1:1 in a molar ratio) by vigorous stirring at room temperature, filtered through porous nylon filter (pore size = 1 μm), and spin-coated at 3000 rpm for 60 s. The as-spun precursor film was immediately immersed in the preheated anti-solvent bath at 70 °C and quickly taken out after 5 s. Chlorobenzene was used as the anti-solvent because of its excellent miscibility with DMSO but insolubility to the CsPbBr$_3$ perovskite. The film was dried at 70 °C for 5 min to remove residual anti-solvent. For the ferroelectric gate insulator, a P(VDF-TrFE) solution (dissolved in MEK at 70 mg ml^{-1}) was spin-coated on top of the CsPbBr$_3$ film, followed by thermal treatment at 100 °C for 30 min. The thickness of the CsPbBr$_3$ and P(VDF-TrFE) films was around 55 nm and 700 nm, respectively. The transistor fabrication was finished with the thermal evaporation of the top Au gate electrode (50 nm). For the MFS diode, a crossbar array with an area of 0.0016 cm^2 was fabricated with the top Au (50 nm) and bottom Cr (1 nm)/Au (50 nm) electrodes.

Characterization and Electrical Measurements: The surface morphology of the CsPbBr$_3$ film was examined by tapping mode AFM (Nanoscope Dimension 3100 Bruker). The X-ray diffraction pattern was acquired using a Rigaku SmartLab HR-XRD equipment at a scan rate of 1° min^{-1}. The UV–vis spectra were obtained from a PerkinElmer Lamda 25 instrument. The *C–E* characteristics were measured using a Novocontrol broadband impedance analyzer. Electrical measurements of the perovskite transistor were carried out using a Keithley 4200-SCS instrument. All the electrical measurements were performed in a vacuum of 10^{-5} mbar.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

[1] G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. L. Gallo, K. Moon, J. Woo, H. Hwang, Y. Leblebici, *Adv. Phys.: X* **2017**, *2*, 89.

[2] J. Zhu, T. Zhang, Y. Yang, R. Huang, *Appl. Phys. Rev.* **2020**, *7*, 011312.

[3] A. Citri, R. Malenka, *Neuropsychopharmacology* **2008**, *33*, 18.

[4] J. Tang, F. Yuan, X. Shen, Z. Wang, M. Rao, Y. He, Y. Sun, X. Li, W. Zhang, Y. Li, B. Gao, H. Qian, G. Bi, S. Song, J. J. Yang, H. Wu, *Adv. Mater.* **2019**, *31*, 1902761.

[5] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.

[6] H. Ling, D. A. Koutsouras, S. Kazemzadeh, Y. van de Burgt, F. Yan, P. Gkoupidenis, *Appl. Phys. Rev.* **2020**, *7*, 011307.

[7] Y. Lee, T.-W. Lee, *Acc. Chem. Res.* **2019**, *52*, 964.

[8] T.-F. Yu, H.-Y. Chen, M.-Y. Liao, H.-C. Tien, T.-T. Chang, C.-C. Chueh, W.-Y. Lee, *ACS Appl. Mater. Interfaces* **2020**, *12*, 33968.

[9] a) M.-K. Kim, J.-S. Lee, *Nano Lett.* **2019**, *19*, 2044; b) M. Hassanpour Amiri, J. Heidler, K. Müllen, P. Gkoupidenis, K. Asadi, *Adv. Funct. Mater.* **2020**, *30*, 2003085; c) A. K. Tripathi, J. J. M. van Breemen, J. Shen, Q. Gao, M. G. Ivan, K. Reimann, E. R. Meinders, G. H. Gelinck, *Adv. Mater.* **2011**, *23*, 4146.

[10] M.-K. Kim, J.-S. Lee, *Adv. Mater.* **2020**, *32*, 1907826.

[11] G. Zhong, M. Zi, C. Ren, Q. Xiao, M. Tang, L. Wei, F. An, S. Xie, J. Wang, X. Zhong, M. Huang, J. Li, *Appl. Phys. Lett.* **2020**, *117*, 092903.

[12] B. Tian, L. Liu, M. Yan, J. Wang, Q. Zhao, N. Zhong, P. Xiang, L. Sun, H. Peng, H. Shen, T. Lin, B. Dkhil, X. Meng, J. Chu, X. Tang, C. Duan, *Adv. Electron. Mater.* **2019**, *5*, 1800600.

[13] a) Z.-D. Luo, X. Xia, M.-M. Yang, N. R. Wilson, A. Gruverman, M. Alexe, *ACS Nano* **2020**, *14*, 746; b) M. Hassanpour Amiri, J. Heidler, K. Müllen, K. Asadi, *ACS Appl. Electron. Mater.* **2019**, *2*, 2.

[14] C. Eames, J. M. Frost, P. R. F. Barnes, B. C. O'Regan, A. Walsh, M. S. Islam, *Nat. Commun.* **2015**, *6*, 7497.

[15] D. Moia, J. Maier, *ACS Energy Lett.* **2021**, *6*, 1566.

[16] Y. Tuchman, T. N. Mangoma, P. Gkoupidenis, Y. van de Burgt, R. A. John, N. Mathews, S. E. Shaheen, R. Daly, G. G. Malliaras, A. Salleo, *MRS Bull.* **2020**, *45*, 619.

[17] J. S. Manser, J. A. Christians, P. V. Kamat, *Chem. Rev.* **2016**, *116*, 12956.

[18] P. C. Harikesh, B. Febriansyah, R. A. John, N. Mathews, *MRS Bull.* **2020**, *45*, 641.

[19] Y. Sun, L. Qian, D. Xie, Y. Lin, M. Sun, W. Li, L. Ding, T. Ren, T. Palacios, *Adv. Funct. Mater.* **2019**, *29*, 1902538.

[20] S. Ham, S. Choi, H. Cho, S.-I. Na, G. Wang, *Adv. Funct. Mater.* **2019**, *29*, 1806646.

[21] F. Ma, Y. Zhu, Z. Xu, Y. Liu, X. Zheng, S. Ju, Q. Li, Z. Ni, H. Hu, Y. Chai, C. Wu, T. W. Kim, F. Li, *Adv. Funct. Mater.* **2020**, *30*, 1908901.

[22] L. Yang, M. Singh, S.-W. Shen, K.-Y. Chih, S.-W. Liu, C.-I. Wu, C.-W. Chu, H.-W. Lin, *Adv. Funct. Mater.* **2021**, *31*, 2008259.

[23] Z. Ma, Z. Liu, S. Lu, L. Wang, X. Feng, D. Yang, K. Wang, G. Xiao, L. Zhang, S. A. T. Redfern, B. Zou, *Nat. Commun.* **2018**, *9*, 4506.

[24] M.-A. Stoecke, M. Gobbi, S. Bonacchi, F. Liscio, L. Ferlauto, E. Orgiu, P. Samorì, *Adv. Mater.* **2017**, *29*, 1702469.

[25] W. Xu, H. Cho, Y.-H. Kim, Y.-T. Kim, C. Wolf, C.-G. Park, T.-W. Lee, *Adv. Mater.* **2016**, *28*, 5916.

[26] H. Tian, L. Zhao, X. Wang, Y.-W. Yeh, N. Yao, B. P. Rand, T.-L. Ren, *ACS Nano* **2017**, *11*, 12247.

[27] R. A. John, N. Yantara, Y. F. Ng, G. Narasimman, E. Mosconi, D. Meggiolaro, M. R. Kulkarni, P. K. Gopalakrishnan, C. A. Nguyen, F. D. Angelis, S. G. Mhaisalkar, A. Basu, N. Mathews, *Adv. Mater.* **2018**, *30*, 1805454.

[28] S. G. Kim, Q. V. Le, J. S. Han, H. Kim, M.-J. Choi, S. A. Lee, T. L. Kim, S. B. Kim, S. Y. Kim, H. W. Jang, *Adv. Funct. Mater.* **2019**, *29*, 1906686.

[29] S.-I. Kim, Y. Lee, M.-H. Park, G.-T. Go, Y.-H. Kim, W. Xu, H.-D. Lee, H. Kim, D.-G. Seo, W. Lee, T.-W. Lee, *Adv. Electron. Mater.* **2019**, *5*, 1900008.

[30] Y. Wang, Z. Lv, J. Chen, Z. Wang, Y. Zhou, L. Zhou, X. Chen, S.-T. Han, *Adv. Mater.* **2018**, *30*, 1802883.

[31] S. Hong, S. H. Choi, J. Park, H. Yoo, J. Y. Oh, E. Hwang, D. H. Yoon, S. Kim, *ACS Nano* **2020**, *14*, 9796.

[32] B. Pradhan, S. Das, J. Li, F. Chowdhury, J. Cherusseri, D. Pandey, D. Dev, A. Krishnaprasad, E. Barrios, A. Towers, A. Gesquiere, L. Tetard, T. Roy, J. Thomas, *Sci. Adv.* **2020**, *6*, eaay5225.

[33] B. Zhang, F. Wang, H. Zhang, B. Xiao, Q. Sun, J. Guo, A. B. Hafsia, A. Shao, Y. Xu, J. Zhou, *Appl. Phys. Lett.* **2020**, *116*, 063505.

[34] B. Jeong, L. Veith, T. J. A. Smolders, M. J. Wolf, K. Asadi, *Adv. Mater.* **2021**, *33*, 2100486.

[35] M. S. Alvar, P. W. M. Blom, G. A. H. Wetzelaer, *Adv. Electron. Mater.* **2019**, *6*, 1900935.

[36] B. Jeong, H. Han, H. H. Kim, W. K. Choi, Y. J. Park, C. Park, *ACS Nano* **2020**, *14*, 1645.

[37] Y. Rakita, N. Kedem, S. Gupta, A. Sadhanala, V. Kalchenko, M. L. Böhm, M. Kulbak, R. H. Friend, D. Cahen, G. Hodes, *Cryst. Growth Des.* **2016**, *16*, 5717.

[38] D. Zhao, I. Katsouras, K. Li, K. Asadi, J. Tsurumi, G. Glasser, J. Takeya, P. W. M. Blom, D. M. de Leeuw, *Sci. Rep.* **2014**, *4*, 5075.

[39] S. Anwar, B. Jeong, M. M. Abolhasani, W. Zajaczkowski, M. H. Amiri, K. Asadi, *J. Mater. Chem. C* **2020**, *8*, 5535.

[40] M. Li, H. J. Wondergem, M. Spijkman, K. Asadi, I. Katsouras, P. W. M. Blom, D. M. de Leeuw, *Nat. Mater.* **2013**, *12*, 433.

[41] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, *Nat. Commun.* **2017**, *8*, 14736.

[42] K. Asadi, P. W. M. Blom, D. M. de Leeuw, *Appl. Phys. Lett.* **2011**, *99*, 053306.

[43] W. Yu, F. Li, L. Yu, M. R. Niazi, Y. Zou, D. Corzo, A. Basu, C. Ma, S. Dey, M. L. Tietze1, U. Buttner, X. Wang, Z. Wang, M. N. Hedhili, C. Guo, T. Wu, A. Amassian, *Nat. Commun.* **2018**, *9*, 5354.

[44] M. Li, F. Hinkel, K. Müllen, W. Pisula, *Nanoscale* **2016**, *8*, 9211.