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Room-Temperature Halide Perovskite Field-Effect Transistors by Ion Transport Mitigation

Beomjin Jeong, Lothar Veith, Thijs J. A. M. Smolders, Matthew J. Wolf, and Kamal Asadi**

Solution-processed halide perovskites have emerged as excellent optoelectronic materials for applications in photovoltaic solar cells and light-emitting diodes. However, the presence of mobile ions in the material hinders the development of perovskite field-effect transistors (FETs) due to screening of the gate potential in the nearby perovskite channel, and the resulting impediment to achieving gate modulation of an electronic current at room temperature. Here, room-temperature operation is demonstrated in cesium lead tribromide ($CsPbBr_3$) perovskite-based FETs using an auxiliary ferroelectric gate of poly(vinylidenefluoride-*co*-trifluoroethylene) [P(VDF-TrFE)], to electrostatically fixate the mobile ions. The large interfacial polarization of the ferroelectric gate attracts the mobile ions away from the main nonferroelectric gate interface, thereby enabling modulation of the electronic current through the channel by the main gate. This strategy allows for realization of the p-type $CsPbBr_3$ channel and revealing the thermally activated nature of the hole charge transport. The proposed strategy is generic and can be applied for regulating ions in a variety of ionic–electronic mixed semiconductors.

1. Introduction

An excellent combination of physical properties, such as solution-processability, high carrier mobility, and large carrier diffusion length,[1] makes halide perovskites highly promising semiconducting materials for application in field-effect transistors (FETs), which are the building blocks of integrated circuits. In an FET, modulation of the electrical conductivity of the channel is achieved through capacitive coupling and the application of an appropriate bias to the gate electrode. However, current modulation at room temperature, and at low frequencies (in particular DC operation) has is challenging for halide perovskite in a conventional FET architecture primarily due to the mixed ionic–electronic characteristics of the perovskite layer.[2] Solution-processed FETs typically operate in accumulation mode, in contrast to conventional Si-based transistors that operate in inversion mode, where a depletion layer isolates the conducting channel from the semiconductor bulk. To achieve gate modulation of the current, and a large ON–OFF current ratio under accumulation mode, a perovskite layer with a low concentration of ions is required. At high ionic concentration, as in **Figure 1**a, an accumulation channel cannot be formed because the gate field is screened by mobile ions, as shown in Figure 1b. The field-effect current is observed only when the gate bias is sufficiently large such that ions are unable to fully screen the gate field. Consequently, an accumulation layer is formed, as depicted in Figure 1c.

The concentration of mobile ions in solution-processed perovskites is estimated to be of the order of 10^{25} m^{-3},[3,4] leading to surface charge densities of a few μC cm^{-2}, e.g., methylammonium lead halide exhibits a surface ion density of 5 μC cm^{-2}.[3] Such a large density would necessitate the application of gate voltages greater than 300 V in order to induce an accumulation channel when using a typical SiO_2 gate dielectric (relative permittivity, $k = 3.9$) with 200 nm thickness, which is impractical since it would cause dielectric break down. Consequently, current modulation in perovskite FETs has been demonstrated mostly at cryogenic temperatures, where ionic conductivity is significantly reduced, or at high-frequencies using pulsed mode operation where ions cannot respond to the rapid changes in the electric field.[5] Operating at low temperature or high frequency severely limits practical applications of the perovskite FET. To address these issues, material modifications such as synthesis of single-crystal microplates,[6] quasi-2D nanosheets,[7] or multicomponent perovskites[8,9] have been attempted. However, these approaches may compromise high-throughput fabrication, reproducibility, or efficient charge transport. Therefore, mitigation or compensation of ion mobility is crucial for the realization of practical perovskite-based FETs.

Here, we propose the usage of dielectric materials with the ability to induce a large surface charge density, such as

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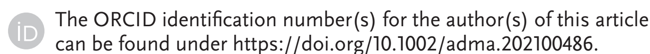
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adma.202100486.

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DOI: 10.1002/adma.202100486

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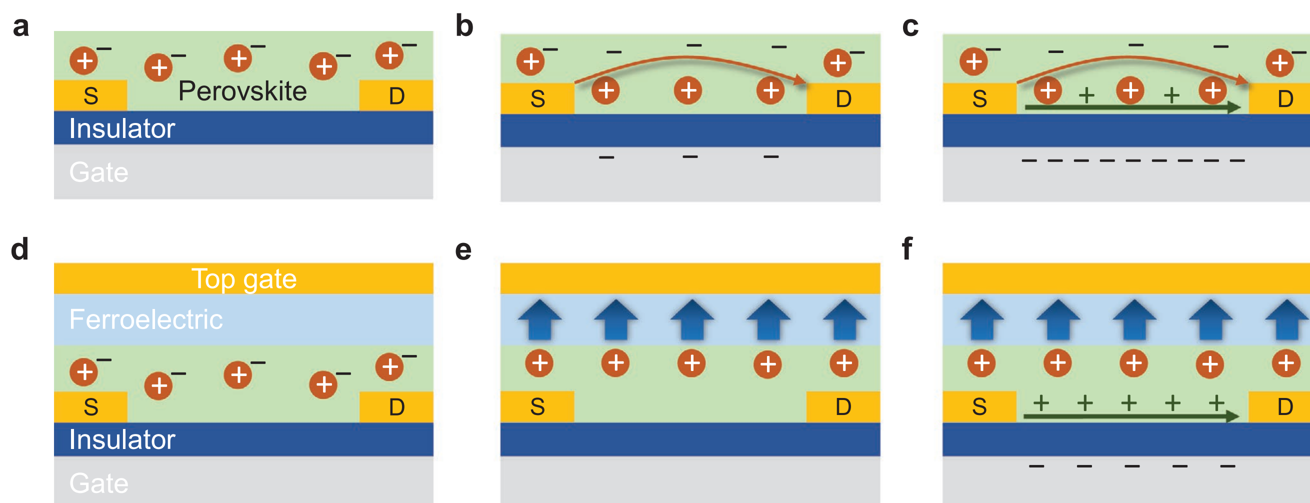

Figure 1. Ion mitigation in perovskite FETs. a) A conventional perovskite FET with a bottom-gate bottom-contact architecture. The S and D denote source and drain electrode, respectively. Mobile cations are represented as "+" signs in red circles, while "–" signs in the perovskite layer represent counter-anions. b) Device operation of the perovskite FET at a negative gate voltage with a negative drain voltage (source is grounded). c) Operation of the perovskite FET at a high negative gate voltage much larger than the breakdown voltage of the gate dielectric. The "+" signs denote hole charge carriers. Note that cations and holes are both accumulated on the insulator. d) A perovskite FET with an auxiliary ferroelectric gate on top of the perovskite layer, and e) with the negative ferroelectric polarization (upward direction). f) Device operation with the negative polarization of the auxiliary ferroelectric gate at low gate voltages. Mobile cations are accumulated at the interface with the ferroelectric and holes are accumulated at the interface with the insulator to make a charge-transporting channel.

ferroelectrics, to electrostatically fixate the mobile ions and thereby overcome the practical limits on FET operation described above. We demonstrate perovskite FETs that operate at room temperature in DC mode. A schematic of the proposed perovskite FET is given in Figure 1d, where a ferroelectric layer is deposited onto the perovskite semiconductor, in this case solution-processed polycrystalline cesium lead tribromide ($CsPbBr_3$). Depending on the material, the ferroelectric layer in its polarized state can provide a surface charge density ranging from several to tens of μC cm^{-2}. Here, poly(vinylidenefluoride-*co*-trifluoroethylene) [P(VDF-TrFE)] is employed as the ferroelectric layer, which offers a surface charge density of 7–8 μC cm^{-2}. Such a high surface charge density is equivalent to applying 450 V to a 200 nm SiO_2 dielectric gate dielectric, which is far larger than the minimum voltage required to achieve an accumulation channel. Polarization of the ferroelectric layer can be stabilized by the compensating charge carriers or by the mobile ions that are provided by the semiconductor.[10–12] For the FET shown in Figure 1d, the ferroelectric polarization attracts mobile ions in the channel to the ferroelectric gate interface, Figure 1e, and depletes the interface at the opposite non-ferroelectric gate, yielding an ion-depleted channel which enables gate modulation of the electronic current and the realization of conventional FET operation, as depicted in Figure 1f.

2. Results and Discussion

Dual-gate perovskite-based FETs were fabricated using a solvent-quenched $CsPbBr_3$ film on top of a heavily doped Si wafer, with a 200 nm thick thermally grown SiO_2 layer. Among the halide perovskites, all-inorganic $CsPbBr_3$ is used due to its stability under ambient conditions[13] and its insolubility in solvent 2-butanone from which P(VDF-TrFE) is processed. Details of the solvent-quenching process[14] for the $CsPbBr_3$ film are given in the Supporting Information (Note S1 and Figure S1). The P(VDF-TrFE) film was then spin-coated on top of the $CsPbBr_3$ layer, annealed and then capped with Au. Subsequently, P(VDF-TrFE) is negatively poled by applying −55 V to the top-gate electrode while grounding both source and drain electrodes; a poling voltage of −55 V was chosen because it is greater than the coercive voltage of –43 V for the 650 nm thick P(VDF-TrFE) top-gate layer used in our device.

The transfer characteristics of the $CsPbBr_3$ FET (linear regime) at room temperature following negative poling of the top P(VDF-TrFE) layer is shown in **Figure 2**a. The FET exhibits a typical p-type behavior with an ON–OFF switching ratio of 10^3. The current for the back-sweep direction (from $-V_{GS}$ to $+V_{GS}$) is lower than that of the forward-sweep direction (from $+V_{GS}$ to $-V_{GS}$). The observed hysteresis is a signature of charge trapping in the semiconductor.[15] The effect of traps in the $CsPbBr_3$ layer on charge transport will be discussed in more detail in the next section. The hole field-effect mobility (μ_{lin}) is 10^{-5} cm^2 V^{-1} s^{-1} (extracted from the positive-to-negative sweep direction). To test the reproducibility of our fabrication strategy, 25 different FET devices were fabricated and their mobilities were measured; as shown in Figure S2 in the Supporting Information, there is a small variation from device to device. The output I_{DS}–V_{DS} characteristic, Figure 2b, clearly exhibits a linear behavior without hysteresis. The $CsPbBr_3$ FET endures multiple operations (over 100 times) without significant degradation (Figure S3, Supporting Information). A marginal decrease in the ON current is observed, most likely due to bias stress, or less likely due to the degradation of the ferroelectric polarization of P(VDF-TrFE), which could be improved by using alternative ferroelectrics such as nylons[16] or δ-PVDF.[17]

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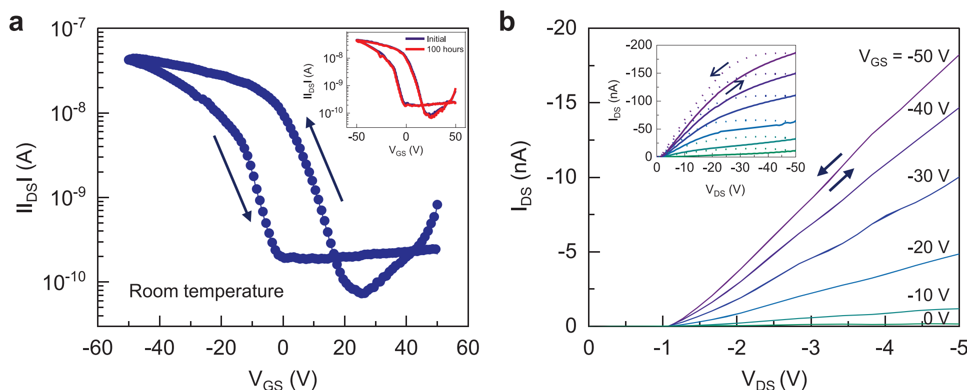

Figure 2. Solution-processed $CsPbBr_3$ perovskite FET. a) Transfer and b) output characteristic of the $CsPbBr_3$ perovskite FET measured at room temperature. The V_{DS} is biased at −5 V while V_{GS} is swept. Inset in (a): comparison of transfer characteristics of a fresh $CsPbBr_3$ perovskite FET and the same after 100 h. Inset in (b): an output characteristic swept to V_{DS} = −50 V.

Comparison between $CsPbBr_3$ FETs with a poled and a nonpoled top P(VDF-TrFE) layer suggests that poling significantly improves FET operation (Figure S4, Supporting Information). Observation of a gate-modulated current without poling of the P(VDF-TrFE) layer could be due to the fact that the P(VDF-TrFE) is composed of polar nanoscopic domains. Although the macroscopic polarization of the layer before poling is zero, at the nanoscale, such polar domains could still attract mobile ions, thereby allowing for the gate modulation of the current even without poling. The operation of the $CsPbBr_3$ FET is weakly dependent on the thickness of P(VDF-TrFE) if poled with a sufficiently higher voltage than the coercive voltage (Figure S5, Supporting Information). In comparison, the $CsPbBr_3$ FET without the top P(VDF-TrFE) layer shows no response to the gate bias, as expected (Figure S6, Supporting Information).

To unambiguously demonstrate the role of the high surface charges of the ferroelectric layer in the operation of the bottom-gated SiO_2 channel, FETs are fabricated wherein polytrifluoroethylene (PTrFE, $k \approx 8$) is used as the top gate dielectric. PTrFE has a similar molecular structure to P(VDF-TrFE) but it is not ferroelectric. FETs are also fabricated with a poly(methyl methacrylate) (PMMA, $k \approx 3.5$) top gate dielectric. PMMA is a non-fluorinated polymer, which is considered to rule out effects of the high electronegativity of the fluorine atom. The bottom $CsPbBr_3$ FET channel is examined while a fixed continuous negative bias is applied to the top gate electrode. The transfer characteristics of both transistors are given in Figure S7 in the Supporting Information. The bottom $CsPbBr_3$ FET channel becomes conductive upon application of a negative bias to the top non-ferroelectric gate. However, a large nonvolatile negative surface charge on the dielectric is needed to fixate mobile cations, to render the bottom $CsPbBr_3$ FET fully operational. PMMA and PTrFE are unable to withstand the biases that are needed to create such surface charges, which can be as large as several hundred volts. Moreover, the surface charge of the non-ferroelectric top gates is volatile, and disappears if the gate bias is removed. In contrast, P(VDF-TrFE) can readily provide a sufficient surface charge at relatively low biases. Furthermore, the density of mobile ions fixated by the top P(VDF-TrFE) layer can be quantitatively controlled by partial polarization of P(VDF-TrFE).[18] The operation of the $CsPbBr_3$ FET is examined as a function of the surface charge density induced on the top P(VDF-TrFE) layer poled at the voltages of −25, −35, −45, and −55 V (Figure S8, Supporting Information). The ON current and the threshold voltage of the $CsPbBr_3$ FET increase linearly with the surface charge density on the top P(VDF-TrFE) layer (Figure S8, Supporting Information).

To probe the mobile ions more directly, we have measured the low-frequency capacitance–voltage (C–V) behavior of the $CsPbBr_3$/P(VDF-TrFE) stacks using a metal/ferroelectric/semiconductor (MFS) diode structure. The C–V behavior of this structure is compared with that of a metal/ferroelectric/metal or MFM capacitor in which the $CsPbBr_3$ layer is absent. For both device structures, Au is used for the contacting electrodes. First, the capacitance response in the devices at zero bias is examined. The impedance spectra of the real and loss permittivity of the MFS diode with a pristine nonpoled P(VDF-TrFE), **Figure 3**a, show huge ionic conduction at frequencies below 100 Hz. In contrast, the low-frequency ionic contribution is absent in the MFM capacitor (greatly suppressed loss permittivity below 100 Hz in comparison to the MFS diode). Next, C–V measurements are performed at 1 Hz to capture the influence of mobile ions in the MFS diode. The MFM capacitor shows the conventional symmetric butterfly loop, which is a signature of ferroelectric materials with switchable polarization. The peaks of the butterfly occur approximately at the coercive voltage V_C, viz., ±21 V (corresponding to a coercive field E_C of ±65 MV m^{-1}), Figure 3b. The full butterfly loop indicates that both polarization states are stabilized by the compensation charges provided by the top and bottom Au electrodes.[19,20] In sharp contrast, the MFS diode containing a $CsPbBr_3$ layer shows an asymmetric C–V loop. The peak in capacitance for the positive biases occurs at a $+|V_C|$ value of +26 V ($+|E_C|$ of +67.5 MV m^{-1}), whereas the $-|V_C|$ value is significantly shifted to −37 V ($-|E_C|$ of −98 MV m^{-1}). The asymmetry is attributed to the ionic displacement at low frequencies, because the C–V loops measured at high frequencies, 1 kHz, Figure 3b, shows perfect symmetry for the $CsPbBr_3$/P(VDF-TrFE) MFS diode, comparable to that of P(VDF-TrFE) MFM capacitor. It should be noted that halide perovskites are ionic–electronic semiconductors. Ions can also compensate the ferroelectric polarization. Therefore, the C–V loop of the perovskite MFS diode also shows stability of both polarization states. This is in contrast with typical MFS diodes

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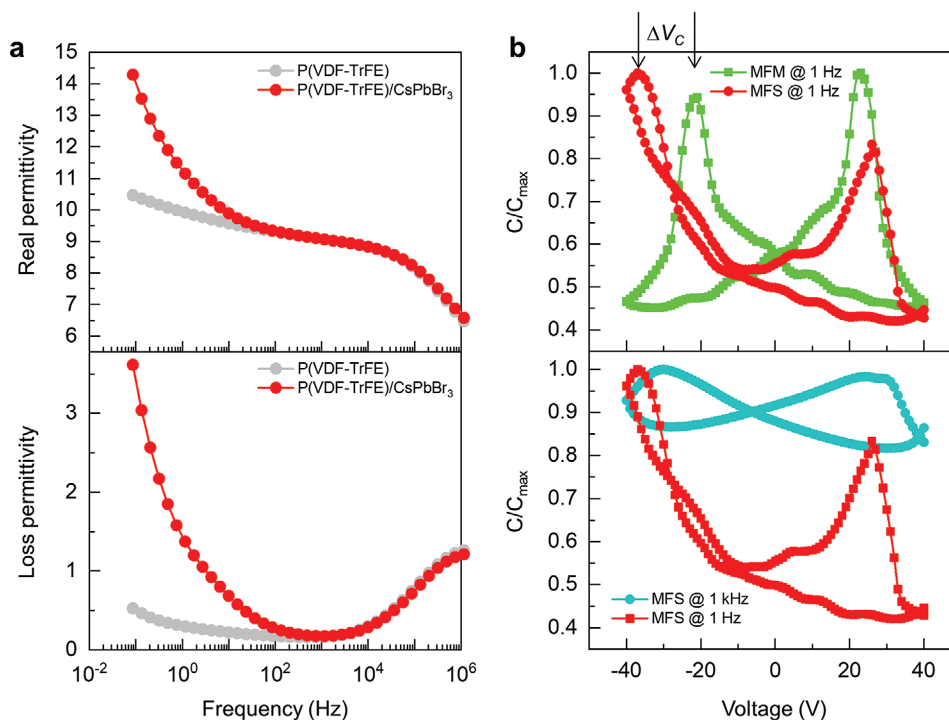

Figure 3. Impedance and capacitance characteristics of the $CsPbBr_3$/P(VDF-TrFE) capacitor. a) Frequency-dependence of real (top) and loss (bottom) permittivity of the MFM capacitor of Au/P(VDF-TrFE)/Au (gray) and the MFS diode of Au/P(VDF-TrFE)/$CsPbBr_3$/Au (red), respectively. The P(VDF-TrFE) layer in both devices is a nonpoled pristine state. b) Top: *C*–*V* characteristics of the MFM capacitor with Au/P(VDF-TrFE)/Au (green) and the MFS diode with Au/P(VDF-TrFE)/$CsPbBr_3$/Au (red) measured at 1 Hz. Bottom: *C*–*V* characteristics of the MFS diode with Au/P(VDF-TrFE)/$CsPbBr_3$/Au measured at 1 Hz (red) and 1 kHz (cyan). The capacitances are normalized by dividing measured capacitance (C) to the maximum one (C_{max}).

based on unipolar non-ionic organic semiconductors, where only one ferroelectric polarization is stabilized.[20,21]

The negative shift in $-|V_C|$ compared to $+|V_C|$ indicates that the mobile ions in $CsPbBr_3$ have positive charges that screen the negative bias, and therefore a significantly greater negative bias is needed to pole the P(VDF-TrFE) layer. From the shift of the coercive voltage in the MFS diode, the surface density of the cations ($\Delta n'$) can be estimated through the relation $\Delta n' = C'|\Delta V_C|/q$, where C', $|\Delta V_C|$, and q are the areal capacitance of the P(VDF-TrFE) layer, the shift in the coercive voltage, and electronic charge respectively. Taking a relative permittivity of 10 for the P(VDF-TrFE), we arrive at a surface cation concentration of 1.82×10^{12} cm^{-2}. In order to determine the identity of the charged species accumulated on the P(VDF-TrFE) layer, we have analyzed the ionic distributions using time-of-flight secondary ion mass spectroscopy (ToF-SIMS). The depth profiling is performed for the Au/P(VDF-TrFE)/$CsPbBr_3$/Au layer stack. While we found that signals from Pb or Br were insensitive to the ferroelectric polarization state of the P(VDF-TrFE) layer (data not presented), the depth profile of the Cs depends on the direction of the P(VDF-TrFE) polarization, as shown in Figure S9 in the Supporting Information. When P(VDF-TrFE) is positively poled, the Cs profile has a relatively symmetric distribution over the volume of the $CsPbBr_3$ film. In contrast, when P(VDF-TrFE) is negatively poled, the Cs profile is notably asymmetric with larger accumulation at the P(VDF-TrFE)/$CsPbBr_3$ interface. Therefore, our elemental analysis indicates that Cs^+ ions are the dominant mobile species attracted by the negative polarization of the P(VDF-TrFE) layer. However, it should be noted that the migration mechanism of Cs^+ ions is undetermined at this stage; in particular, Cs vacancy-mediated migration is unlikely since such defects would be negatively charged with respect to the lattice. Furthermore, the role of other mobile species such as positively charged halide vacancies,[22–26] also needs to be investigated.

The impedance spectra of the MFS diode poled in negative and positive polarization states further reveal the accumulation of the mobile cations at the interface of the $CsPbBr_3$ and P(VDF-TrFE) layer (Figure S10, Supporting Information). For as long as the ferroelectric polarization is compensated with the mobile cations, the transfer characteristic of the bottom-gate transistor should not change. Figure 2a (inset) shows that the transfer characteristic of the transistor right after the polarization of the top P(VDF-TrFE) layer and after 100 h is similar. This is expected, due to the long-term stability of ferroelectric polarization when compensation charges are present.[21] Therefore, P(VDF-TrFE) is not depolarized, and the cation movement remains suppressed.

The observed hysteretic behavior of the transfer characteristic in Figure 2a is attributed to charge trapping. When the mobile cations are attracted and fixated by the negative remanent polarization of P(VDF-TrFE), counter-anions are left behind that can act as charge trapping centers due to their Coulombic attraction with hole carriers. To elucidate the influence of charge traps on the transport mechanism, transfer characteristics of the FETs with negatively poled P(VDF-TrFE) are measured at

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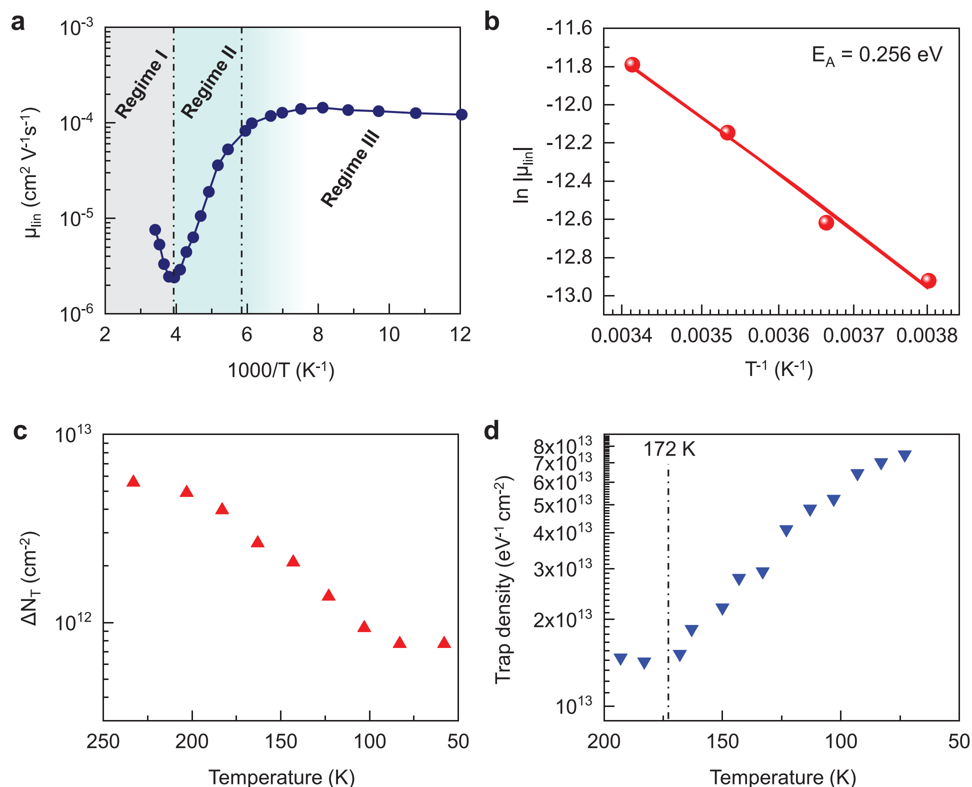

Figure 4. Low-temperature measurement of the ion-transport-mitigated $CsPbBr_3$ perovskite FET. a) A plot of linear field effect mobility (μ_{lin}) versus inverse temperaturef for the $CsPbBr_3$ perovskite FET. Each regime of I, II, and III is marked by the gray, cyan, and cyan-shaded area, respectively. For clarity, each regime is divided by a dashed line at 256 and 172 K. b) The Arrhenius plot in the regime I. The line shows the linear fit for extracting activation energy. c) The number of trapped hole carriers (ΔN_T) calculated from the hysteresis gap of the transfer curves at each temperature (Figure S11, Supporting Information) in the regime II and III. d) The maximum number of trap density extracted from the subthreshold swing at each temperature in the regime III. The dashed line marks a temperature of 172 K to specify the start point of the regime III.

different temperatures, and the resulting field-effect mobility (μ_{lin}) of the $CsPbBr_3$ as a function of temperature (T) is shown in **Figure** 4a. The corresponding transfer characteristics are given in Figure S11 in the Supporting Information. The μ_{lin}–T plot exhibits three distinct regimes: I) decreasing mobility from room temperature to 256 K, II) increasing mobility from 256 to 172 K, and III) nearly constant mobility for temperatures below 172 K. The presence of residual mobile cations is unlikely because, in this case, the mobility should increase and the hysteresis gap should decrease with temperature as the ions are immobilized.[5] However, the opposite trend is observed in our experiment for regime I; the mobility decreases. Regime I features thermally activated charge transport with an Arrhenius behavior: $\mu = \mu \exp(-E_A/kT)$, where μ_0 is the free carrier mobility (which is temperature dependent in general, although here we neglect it since the exponential function dominates), and k, and T are the Boltzmann constant, and the temperature, respectively. An activation energy of $E_A = 0.256$ eV is extracted for the charge trapping regime I, as shown in Figure 4b. With decreasing temperature, from 293 K, the p-type conductance (i.e., ON-current at $V_{GS} = -50$ V), and therefore the mobility, decreases. The activation energy is attributed to the thermal ionization of acceptor-like defects, which results in a decrease in free hole concentration as temperature lowers. The experimentally measured activation energy matches well with density functional theory calculations where similar values have been reported for the thermodynamic charge transition levels of a number of acceptor defects.[22,27,28] These include Cs and Pb vacancies, Br interstitials, Br_{Cs}, Br_{Pb}, and Cs_{Pb} substitutions, and even impurities such as HBr. In principle, which of these are likely to be most abundant can be estimated from the defect formation energies,[22,27,28] though we note that in practice the abundances are likely to depend on the experimental growth conditions and therefore we leave their determination for a subsequent study.

In regime II, 256 K < T < 172 K, the mobility exponentially increases by more than one order of magnitude. In this regime, thermal ionization is severely limited and as a result, hysteresis in the transfer curves due to trapping is substantially reduced. In this regime, phonon scattering is the limiting factor for charge transport similar to conventional inorganic crystalline semiconductors.[29,30] In regime III, characterized scattering from ionized (shallow trap) defects in $CsPbBr_3$ shows weak temperature dependence because all the (deep trap) counteranions are compensated through trapped holes. Nevertheless, the mobility slightly decreases. The trap density, ΔN_T, estimated from the transfer curves is plotted in Figure 4c. The N_T has been calculated from the hysteresis window through $N_T = C'_{ox}\Delta V_{Hys}/q$, where C'_{ox} is the areal capacitance of SiO_2 (17.3 nF cm^{-2} for 200 nm thick SiO_2), ΔV_{Hys} is the difference

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in onset voltages of forward and reverse direction at each temperature. The maximum trap density (N_t) calculated from the subthreshold swing (SS) rapidly increases in the regime III, as shown in Figure 4d. The SS is a simple indicative of the deep trap density (Note S2, Supporting Information).[31] We note that the previous report on temperature-dependent photoluminescence that studied charge trapping in $CsPbBr_3$ indicates the presence of deep level defects below 172 K,[28] which supports our finding.

3. Conclusion

We have demonstrated the operation of solution-processed perovskite FETs based on $CsPbBr_3$ that show current modulation at room temperature through mitigation of ion transport. It is shown that mobile ions, including but not limited to Cs^+, can be successfully fixated with the negative remanent polarization of the ferroelectric P(VDF-TrFE); the resulting depletion of mobile ions from the $CsPbBr_3$–SiO_2 interface facilitates gate-modulation of the electronic conduction in the channel with large current modulation with an ON–OFF ratio of 10^3 at room temperature.

Furthermore, the electrostatic fixation of ions allows for the investigation of the intrinsic electrical properties of the perovskite layer in a transistor structure, which are crucially needed but have rarely been attempted because of the lack of a proper strategy to mitigate the effects of mobile ions; here, it is shown that p-type mobility of the $CsPbBr_3$ channel at room temperature is governed by traps with an activation energy of 0.256 eV. Further work to identify the defects responsible for trapping will enable strategies to control trap densities to be developed and device characteristics to be further improved.

Finally, we note that the proposed strategy for suppressing ion transport is potentially applicable to various solution-processed halide perovskite semiconductors regardless of compositions and dimensions, and therefore facilitates application of solution-processed perovskites in emerging FET-based devices such as light-emitting transistors, phototransistors, or neuromorphic transistors, and also to various ionic–electronic mixed semiconductors beyond halide perovskites.

4. Experimental Section

Materials Preparation: CsBr (99.9%), $PbBr_2$ (99.999%), and all the chemical solvents were purchased from Sigma-Aldrich. P(VDF-TrFE) with 75 mol% VDF and 25 mol% TrFE (M_w = 350 mol kg^{-1}) was purchased from Solvay.

$CsPbBr_3$ Thin Film Preparation: CsBr and $PbBr_2$ precursor powders were dissolved in anhydrous dimethyl sulfoxide (DMSO) at the concentration of 200 mg mL^{-1} with 1:1 molar ratio. The solution was vigorously stirred for 3 h at room temperature, and filtered through a porous nylon filter (pore size = 1 µm). The solution was spin-coated on the UV-treated silicon or glass substrates at 3000 rpm for 60 s. For rapid extraction of DMSO from the as-spun film by solvent-quenching, the film was immediately immersed in hot chlorobenzene (70 °C) for 5 s, and subsequently dried on a hot plate at 70 °C for 5 min. All the processes were performed in an inert condition (less than 1 ppm H_2O and O_2).

Film Characterization: UV–vis absorbance spectrum of $CsPbBr_3$ thin films deposited on glass substrates was obtained from a PerkinElmer Lamda 25 instrument. Tapping-mode atomic force microscopy (NanoScope Dimension 3100, Bruker) was utilized to acquire the surface morphology of the films. X-ray diffraction patterns were recorded using a Rigaku SmartLab HR-XRD equipment at a scan rate of 1° min^{-1}. The thickness of the films was measured with a Dektak surface profilometer. The depth profile of Cs^+ was obtained through ToF-SIMS instrument (IONTOF TOF.SIMS5 NCS). Analyses of the samples were acquired using Bi_3^+ ions at 30 keV energy on the sputtering area of 100 µm^2.

Capacitor Fabrication: The MFS capacitors were fabricated on a glass substrate on which Au bottom electrodes with a Cr adhesion layer were thermally evaporated using a shadow mask. The thickness of Au and Cr was 50 and 1 nm, respectively. The glass substrates with Au/Cr bottom electrodes were treated by UV to render surface hydrophilic, followed by deposition of $CsPbBr_3$ films as described. P(VDF-TrFE) (60 mg mL^{-1}) dissolved in 2-butanone was subsequently spin-coated on top of $CsPbBr_3$ at 1500 rpm for 60 s. The polymer-$CsPbBr_3$ bilayer films were annealed at 100 °C for 30 min. Finally, Au top electrodes (50 nm) were thermally evaporated using a shadow mask to form a crossbar array with the area of 0.0016 cm^2.

FET Fabrication: The perovskite transistor was fabricated with a configuration of highly doped Si, SiO_2, interdigitated Au electrodes, and the $CsPbBr_3$ film for functioning as a gate electrode, a dielectric, source–drain electrodes, and a semiconductor channel, respectively. The Au source/drain electrodes (W = 10 000 µm, L = 10 µm) with an adhesion layer of Ti were patterned using conventional photolithography. Before the deposition of $CsPbBr_3$, the substrate with patterned source/drain electrodes was cleaned by ultrasonication in acetone and 2-propanol for 10 min each, and dried in a nitrogen flow. After UV-treatment for 20 min to render the substrate hydrophilic, the $CsPbBr_3$ thin film was deposited by solvent-quenching as described above. P(VDF-TrFE) dissolved in 2-butanone at 60 mg mL^{-1} was subsequently spin-coated on top of $CsPbBr_3$ at 1500 rpm for 60 s, and thermally annealed at 100 °C for 30 min. The thickness of the P(VDF-TrFE) was 650 nm. For electrical poling of P(VDF-TrFE), a 50 nm thick top Au electrode was thermally evaporated using a shadow mask.

Electrical Measurement: Capacitance–voltage characteristics at various frequencies were measured using a Novocontrol analyzer. Electrical measurements of the transistors were carried out with a Keithley 4200-SCS instrument under continuous mode. To induce a negative remanent polarization of P(VDF-TrFE) on top of the perovskite FET, the P(VDF-TrFE) film was swept from 0 to −55 V. The bias of −55 V was sufficiently larger than the coercive voltage of the 650 nm thick P(VDF-TrFE). For temperature-dependent electrical measurements, the device was positioned on a metal plate in a Janis probe station connected to a cryostat and cooled with liquid N_2. To ensure thermal contact, heat-conducting glue was pasted between the plate and the substrate. The temperature was monitored using thermocouples. All the electrical measurements were carried out in a vacuum of 10^{-5} mbar.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors thank Christian Bauer and Frank Keller for technical support. B.J. and K.A. thank the Alexander von Humboldt Foundation for their financial support. The authors thank Prof. Paul W. M. Blom from the Max Planck Institute for Polymer Research and Prof. Alison B. Walker from the University of Bath for fruitful discussions.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

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Data Availability Statement

Research data are not shared.

Keywords

ferroelectric polarization, ion transport, lead halide perovskites, perovskite transistors, thin films

Received: January 19, 2021
Revised: April 26, 2021
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