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Abstract— This paper presents the design of an active inductor based wideband LNA using current reuse topology,which is designed and simulated in 0.18um CMOS technology. The low noise amplifier is considered to be the key block in an RF receiver. It plays a critical role in determining the noise figure of a receiver. The main function of an LNA is to provide sufficient gain to reduce the noise of subsequent stages while adding as little noise as possible. To achieve a good impedance matching over a desire bandwidth (0.05GHz to1.5GHz) active inductor is implemented based on gyrator structure and its noise is improved by employing a feed-forward path (FFP). The simulations show a maximum power gain of 17.32dB, minimum noise figure (NF) of 0.87dB with a 3db bandwidth of 1.0GHz over 0.05-1.5 GHz range. The total power consumption is 6.38mW with 1.8V power supply.

Keywords- *Low Noise Amplifier (LNA),Active Inductor, Noise Figure (NF),Current reuse technique.*

I. INTRODUCTION

The common objectives in design of a low noise amplifier(LNA) are to provide high gain, to achieve as minimum noise figure (NF) as possible, to minimize the nonlinearities and finally to have good input and output impedance matching as this will ensure maximum power transfer and optimized gain and noise performances. In radio receivers, the LNA, as the first input block, is to be matched with the antenna's characteristic impedance (generally 50 Ω)[2].For this purpose a matching network is needed to ensures optimum noise performance as well as stability and also power matching between the antenna and LNA[3]. Shunt feedback amplifier suggests yet a solution for achieving the required matching at the input port. However, this method suffers from a relatively high NF due to the thermal noise of shunt resistor[4]. The inductive source degenerated cascode LNA topology can provide excellent impedance matching and noise figure[5].Traditional LNA designs[1] is their heavy reliance on large passive inductors to achieve various performance requirements. Where as passive inductor takes up the majority of the chip area and on the other hand has limited quality factor(Q).

Active inductors have been advocated for a long time as area efficient replacements for passive inductors. The inductance value of the active inductors can be easily changed either in a continuous manner or in discrete steps, which provides flexibility in the tuning of matching circuits. Higher accuracy, easier layout floor-planning, small area, and absence of magnetic coupling are other advantages of active inductors compared to their passive counterparts[1].Several active inductor topologies[6],[7],[8] have been designed and discussed, most of which utilize a capacitor-gyrator(C-G) structure to duplicate the required inductive properties. However, due to poor noise and linearity performance of active inductors, their applications are limited in RF receiver. In recent year input matching circuit is implemented by a low noise, good linearity active inductor[1],which is fully on chip and occupies a small die area, but tends to suffer from larger power dissipation to achieve high center frequency.

In this paper, a inductive source degenerated cascode LNA topology is presented for which input matching circuit is implemented using an active inductor. In addition to that current reuse technique is adopted to achieve low power consumption. The proposed circuit is designed and simulated using TSMC 0.18-μm CMOS Technology.

This paper is organized as follows. In section II, a low noise tunable Active inductor is presented. In section III Cascode Low Noise Amplifier and small signal analysis of that LNA is presented. It also describes the design of Cascode LNA using Active Inductor and current reuse topology .In section IV measurement results are reported and finally, section V provides conclusion.

II. ACTIVE INDUCTOR

The gyrator-c structure is a well known circuit topology to synthesis active inductors. It consists of two back to back connected trans-conductors, one that has a negative transconductance, another that has a positive transconductance and an external shunt capacitor c[9]. The input impedance of the circuit is inductive and can be written as,

$$Z_{in} = \frac{sC}{G_{m1}G_{m2}} \qquad (1)$$

The conventional circuit realization of the gyrator concept (G_{m1} and G_{m2})[10] is shown in Fig. 2.1(b), for which the input impedance is inductive with

potentially high quality factor(Q) and high self-resonant frequency(f_r) . The parasitic capacitances and the input/output resistances of the transconductance amplifiers degrade the quality factor and reduce the self-resonant frequency of the active inductor.

Using the hybrid- small signal model for the transistors and assuming ideal current sources, the components of the equivalent circuit of Fig. 2.1(c) can be calculated as[10],

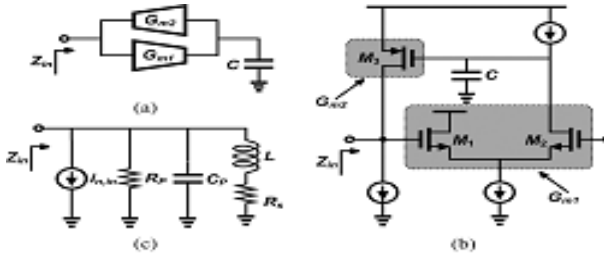

Fig. 2.1 Active inductor. (a) General structure. (b) Typical implementation. (c)Equivalent RLC model.

$$L = \frac{2C}{g_{m1}g_{m2}} \qquad 2(a)$$

$$C = \frac{1}{2}C_{gs1} + C_{gd1} + C_{gd3} + C_{db3} \qquad 2(b)$$

$$R_S \cong \frac{2}{g_{m1}g_{m2}r_{02}}, \quad R_P = r_{03} \qquad 2(c)$$

$$\overline{i^2_{n,in}} = 4kT\gamma\left[\frac{2}{g_{m2}(L\omega)^2} + g_{m3}\right] \qquad 2(d)$$

Where M_1 and are assumed to be identical, C is the total capacitance seen at the gate ofM_3;$C_{gs,}$ C_{gd}, and C_{db} are the transistors' capacitors, g_m and r_o are the transistors' transconductance and output resistance, respectively. The flicker noise is neglected at high frequencies and the channel thermal noise is assumed to be $i^2_d = 4kT\gamma g_m$ where γ is the channel excess noise factor. In order to improve the noise performance of the differential stage, a feed-forward path (FFP) is added to the basic differential pair consisting of transistors and, as shown in Fig 2.2[1].

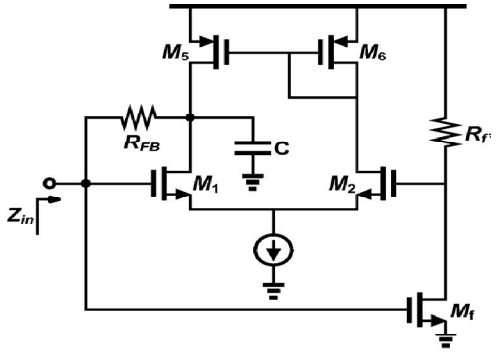

Fig. 2.2 Low noise active inductor

The active inductor can be placed at the input of LNA to provide impedance matching at the input. The active inductor resonates with the amplifier's input capacitance C_{in}, at the resonant frequency and leaves the equivalent resistance of the active inductor as the input impedance. The typical value of capacitances and the transistors' output resistance, is often larger than the antenna's characteristic impedance. Also, being connected to the input node, the matching inductor has to be low noise for a low noise figure of the overall LNA. Therefore, to design a low noise active inductor with reduced equivalent resistance, as shown in Fig.2.2[1] the following changes is applied to the conventional gyrator-based active inductor circuit. For low-noise performance, it uses the modified differential pair with the FFP to realize the transconductance G_{m1}. The current mirror (M_5 and M_6) is used to cancel the effect of the common mode noise generators such as that of the tail current source.

III. DESIGN OF LNA

The general topology of an LNA can be broken down into three stages: an input matching network, the amplifier core, and the output matching network [3]. In fig 3.1, the LNA and the matching network are characterized by the S-parameters. There are four S-parameters, S11, S12, S21, and S22, where

S11 is the input impedance,

S12 is the reverse transmission factor,

S21 is the forward gain, and

S22 is the output impedance.

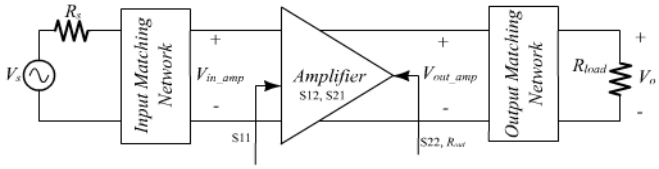

Fig 3.1 Generalized LNA topology

To address these challenges in the design of a wideband LNA, several topologies and circuit techniques have been proposed. In this paper the inductive source degenerated cascode LNA topology, shown in Fig.3.2, has demonstrated the potential for excellent impedance matching, noise figure, and power dissipation as well as decreases the Miller effect compared to other topology[2].

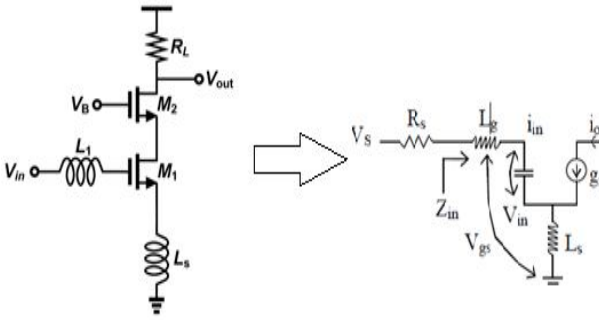

Fig3.2(a)Cascode LNA, (b)Small-signal equivalent schematic

The design and analysis of the amplifier in all aspects, such as input match, gain and noise, are discussed as follows.

- Part a: From this model,

$$V_{in} = i_{in}\left(j\omega L_g + j\omega L_s\right) + i_{in}\left(\frac{1}{j\omega C}\right) + I_0 j\omega L_s \qquad (3.1(a))$$

$$i_0 = g_m V_{gs} = g_m i_{in}\left(\frac{1}{j\omega C_{gs}}\right) \qquad (3.1(b))$$

Substitute 3.1(b) in 3.1(a).

$$V_{in} = i_{in}\left[j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}\right] \qquad (3.1(c))$$

Input impedance,

$$Z_{in} = \frac{V_{in}}{i_{in}} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \qquad (3.2)$$

For matching $L_g + L_s$ are cancelled out by C_{gs}. So at frequency of interest

$$\omega_0\left(L_g + L_s\right) = \frac{1}{\omega_0 C_{gs}}$$

$$\omega_0^{\,2} = \frac{1}{\left(L_g + L_s\right)C_{gs}} \qquad (3.3)$$

$$\text{source resistance, } R_s = 50\Omega = \frac{g_m L_s}{C_{gs}} \qquad (3.4)$$

In the design, *Ls* is chosen such that
Real(Z_{in}) = ωTL_s = 50 Ω.
L_g is chosen according to (3.2).so that *imaginary* (Z_{in}) = 0 at ω_0.
NOTE:
1) L_s is typically small and may be realized by the bond wire for source.
2) L_g can be implemented by spiral/external inductor.

- Part b:For series RLC Circuit[12]

$$\left[Q_s = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{\omega_0 L}{RC}, \text{ and } V.C = Q_s V_{in}\right]$$

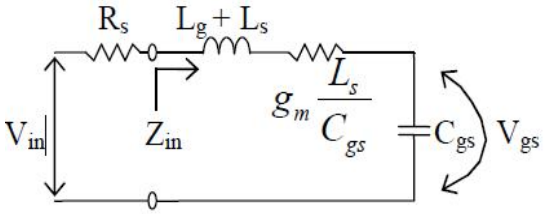

Fig.3.3 Series RLC Circuit with Lg and Ls

Quality factor of circuit (fig 3.3) can be calculated as follows,

$$Q_{in} = \frac{\omega_0\left(L_g + L_s\right)}{R_s + \frac{g_m L_s}{C_{gs}}} = \frac{\omega_0\left(L_g + L_s\right)}{R_s + \omega_T L_s} \qquad (3.5)$$

$$Q_{in} = \frac{1}{\omega_0\left(R_s + \frac{g_m L_s}{C_{gs}}\right)C_{gs}} \qquad (3.6)$$

$$\text{for match load, } R_s = \frac{g_m L_s}{C_{gs}} \qquad (3.7)$$

$$Q_{in} = \frac{1}{2\omega_0 R_s C_{gs}} \qquad (3.8)$$

- Gain:

$$V_{gs} = Q_{in}\, V_{in} \qquad (3.9)$$

Transistor transconductance is given by,

$$g_{m[12]} g_m = \frac{I_{out}}{V_{gs}} \qquad (3.10)$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{V_{gs} g_m}{V_{in}} = Q_{in} g_m \qquad (3.11)$$

$$gain = \frac{V_{out}}{V_{in}} = -G_m R_L \qquad (3.12)$$

From (3.12) it is clear that, the gain is proportional to *RL* which can be made large: a few hundred to over a thousand Ohm and also transconductance of amplifier.

- Noise Figure:

For calculation of the noise factor of the LNA, only the classical channel noise of M1 and the thermal noise of RL are considered as indicated in Fig. 4.3. The noise contribution of M2 and other parasitic noise sources are ignored. The derivation was based on the quasi static approximation and the influence of the cascode pole, the Miller-effect and other parasitic are neglected. Noise figure is given as ratio of total noise power at the output to total noise power at the output due to input source. For this calculation channel noise is ignored[12].

$$F = \frac{\overline{V^2_{n0,R_s}} + \overline{V^2_{n0,d}}}{\overline{V^2_{n0,R_s}}} = 1 + \frac{\overline{V^2_{n0,d}}}{\overline{V^2_{n0,R_s}}} \qquad (3.13)$$

Noise contribution of transistor is defined as,

$$\overline{V^2_{n0,d}} = \overline{i^2_{n,d}} R_L^2$$

$$\text{where } \overline{i^2_{n,d}} = 4kT\gamma g_m \Delta f \qquad (3.14)$$

From above expression (3.14) it is cleared that noise figure decrease with square of Q-factor, where as Q-value depends upon L_g+L_s, L_s is usually small. So Q-value mainly depends on L_g. But as L_g can be implemented by spiral/external inductor it will occupy larger area. So in order to reduce area the proposed active inductor [8] can be placed at the input of LNA. It also provide noise reduction as well as good impedance matching at the input.

A. PROPOSED LNA

This fig3.4 shows the proposed LNA which is applicable for noise reduction. For most broadband amplifiers there is a severe trade-off between input-impedance match and NF because for minimum NF, high input impedance *Zin* of the amplifier is required whereas for maximum power transfer, *Zin* needs to be matched with 50ohm as it mentioned. Because of this trade off, most of the CMOS WB LNAs show NF above 3dBwhen matched to 50ohm. The cascoded stage provides a reasonably low (about 3dB) noise figure as derived previously. If the body effect is absent then the width of the cascoding transistor M2, should be chosen three times less than that of the input transistor M1.

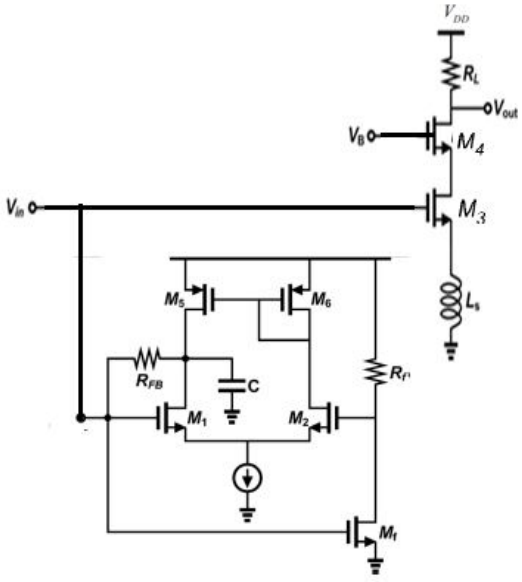

Fig.3.4 Proposed Cascode LNA with Active Inductor

Figure 3.5[14] illustrates the LNA with a current reuse topology. For the low power consumption requirement, the two-stage amplifier is folded into a single stage. It means that it is cascode for DC and cascade for RF signals. The two cascading common source amplifiers share the same supply current to reduce power consumption. Hence,with the same gain performance, this circuit only consumes about half the power of the two-stage amplifier. $C_{coupling}$ is a coupling capacitor, L1 is an RF choke and C_{pass} is a capacitor providing AC ground. In this topology, the Miller effect is more serious than in a cascade amplifier, since the first common source amplifier has a large voltage gain. This effect can be reduced by inserting an inductor before the gate of the second stage. The input impedance of the LNA is matched to 50Ω since the band pass filter (BPF) required in most conventional receiver architectures is in a 50 Ω system. The source degeneration method for input matching is employed.

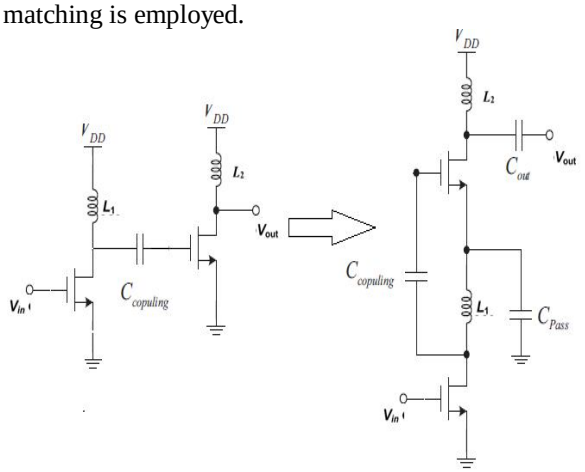

Fig.3.5 CMOS LNA with a current-reuse topology

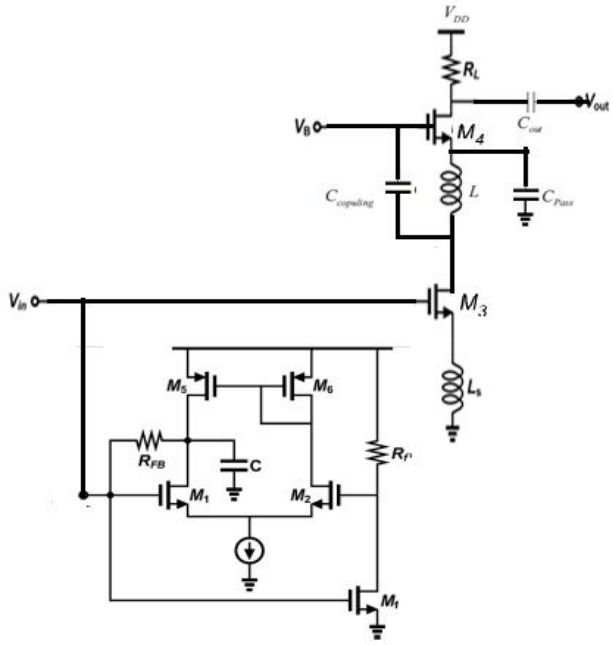

Fig.3.6 Proposed Cascode LNA with Current reuse

B. LNA using CURRENT REUSE TOPOLOGY

Figure.3.6 shows the LNA with active inductor using current reuse topology.The Active inductor with source degeneration method is employed for input impedance matching.

IV. SIMULATION RESULT

In this section, the simulation results of Active inductor based wideband LNA using current reuse topology which is designed in TSMC 0.18µm CMOS process is presented.

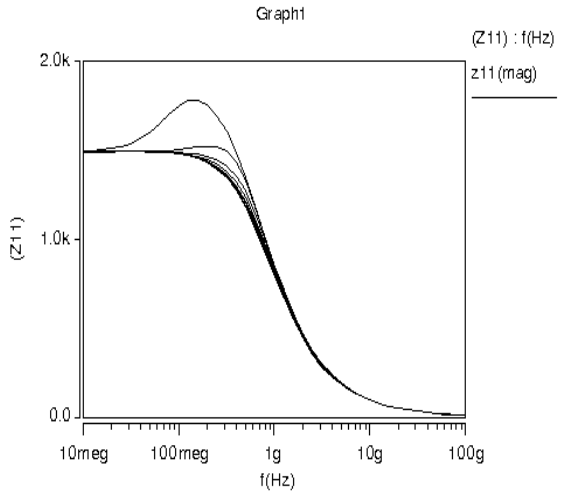

Fig4.1.Input Impedance of Active Inductor

Fig 4.1 shows the input impedance of Active Inductor which is inductive in nature from 10MHz to 1.5GHz. The measurement results are described in Fig.4.2-Fig.4.5.The gain shown in Fig. 4.1 has peak value 17.32dB at 0.31GHz.In Figure4.2, the input matching has S_{11} low than -10dB and the output matching has S_{22} lower than -14 dB. The reverse isolation S_{12} is maintained well below -40 dB throughout the frequency of 0.05GHz to 1.5GHz, which is shown in Figure 4.4.

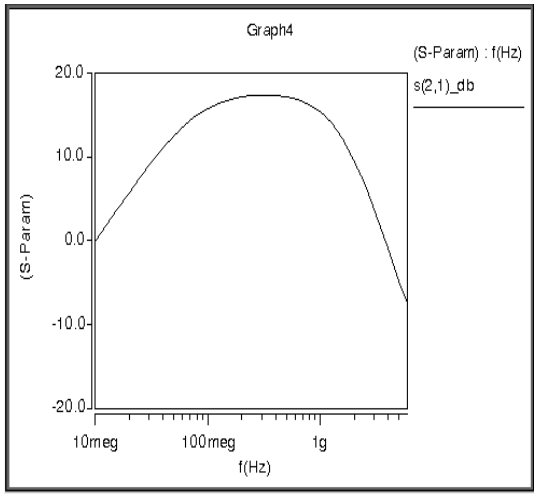

Fig 4.2 Gain of LNA (S_{21})

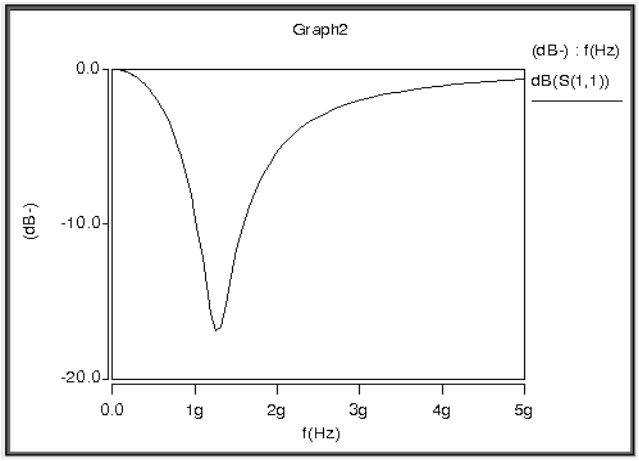

Fig 4.3 S_{11}

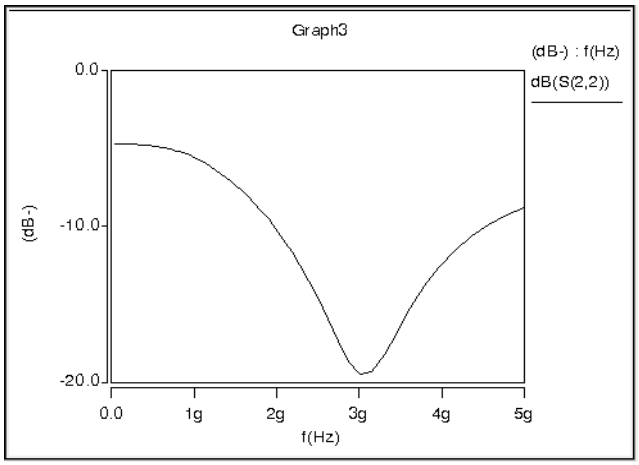

Fig.4.4 S_{22}

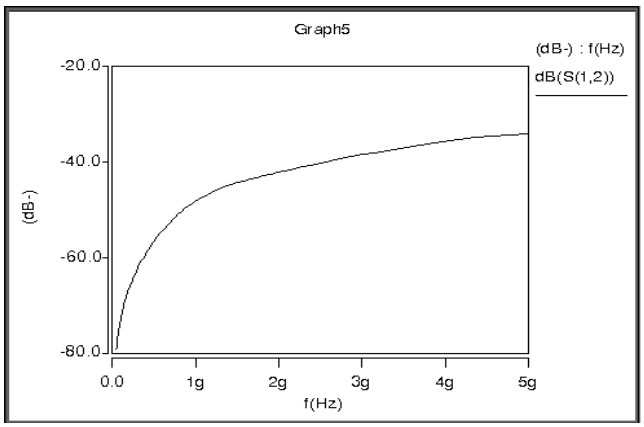

Fig.4.5 S_{12}

The noise figure depicted in Fig.4.5 has minimum value of 0.87dB at 0.58GHz,noise voltage of $3.75nV^2/Hz$ and it maintained well below 3.5dB over the range of frequency below 2.5GHz.

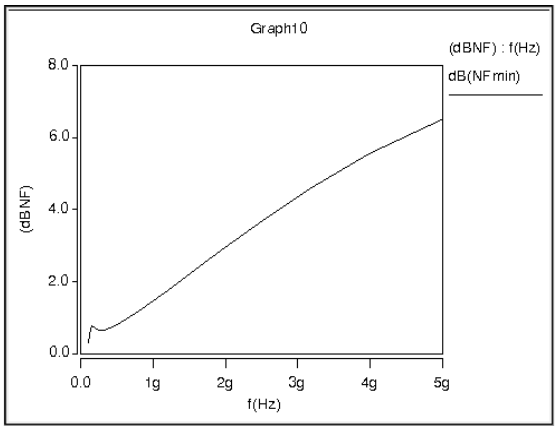

Fig.4.6 Noise figure of LNA

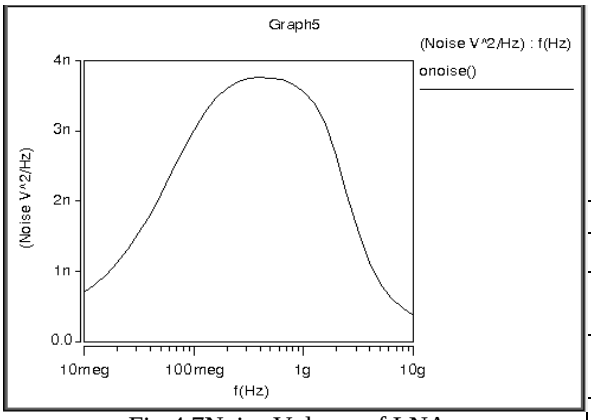

Fig.4.7Noise Voltage of LNA

Linearity refers to ability of amplifier to produce signals that are accurate copies of input. Linearity can be improve by exploiting a noise or distortion cancellation technique. Although there are many ways to evaluate the linearity of the LNA, to measure the third-order intercept point (IP3) is the most commonly used method. The IIP3 is obtained graphically by plotting the output power versus the input power both on logarithmic scales. As in Fig.4.8 the input third-order intercept point (IIP_3) can attain -10.42dBm.

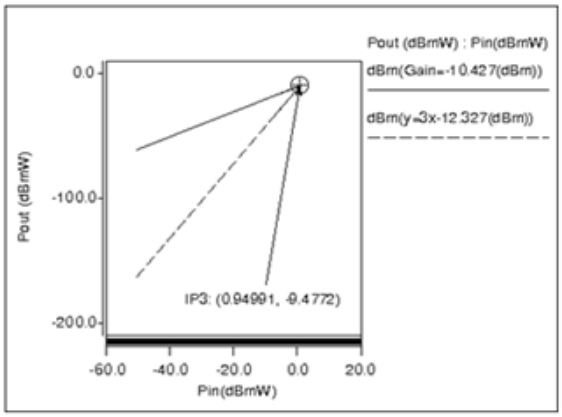

Fig.4.8 IIP3 Analysis

TABLE I summarizes and compares the performance with Active inductor based LNA using Current reuse and without current reuse topology. Comparison of the proposed work with other published works is summarized in TABLE II.

TABLE I. Comparison of results

Parameters	Proposed LNA	Proposed LNA using Current reuse
S_{11}(dB)	<-12	<-10
S_{12}(dB)	<-46.3	<-32
S_{21} Gain(dB)	17.13	17.32
S_{22}(dB)	<-19.3	<-14.3
Noise figure(dB)	1.2	0.87
Noise Voltage(nV^2/Hz)	4.2	3.75
IIP_3(dBm)	-10.96	-10.42
V_{DD}(V)	1.8	1.8
DC Power(mW)	7.8	6.32

TABLE II. Comparison of the proposed circuit with the existing work

Parameters	Ref [1]	Ref [8]	Ref[14]	This work
Technology	0.18µ	0.13µ	0.18µ	0.18µ
Freq(GHz)	1.2-11.9	2–6	0.4-10	0.05-1.5
GainS21(dB)	18-23.5	14.18	12.4	13.1-17.32
Noise figure	2.2-2.7	2.78-2.4	2.6-3.9	0.87-1.3
IIP3 (dBm)	-1	_	-3	-10.42
V_{DD}(V)	1.8	1.2	1.2	1.8
Power(mW)	15.3	10.36	12	6.32

V. CONCLUSION

In this paper, a current reuse active inductor based wideband LNA has been presented. The circuit is designed with TSMC 0.18µm CMOS technology. The wideband LNA exhibits maximum gain of 17.32dB, minimum noise figure of 0.87dB over the frequency range of 0.05-1.5GHz with a 3db bandwidth of 1.0GHz while consuming a DC power of 6.32mW from 1.8V supply. Thus by using the current reuse technique, the proposed paper achieves an optimum power and minimum noise figure compared to other existing work.

REFERENCES

[1] MohsenMoezzi, Member, *IEEE*, and M. Sharif Bakhtiar "Wideband LNA Using Active Inductor With Multiple Feed-Forward Noise Reduction Paths": *IEEE Transaction On Microwave Theory and Techniques, VOL. 60, NO. 4, APRIL 2012.(*Base Paper)

[2] B. Razavi, "Design Considerations for Direct-Conversion Receivers,"IEEE Transactions on

Circuits and Systems-II: Analog and DigitalSignal Processing. Vol. 44, pp. 428 -435,1997.6

[3]VLSI for WIRELESS COMMUNICATION by BoscoLeung:Prentice Hall Electronics and VLSI series Charles G.Sodini,Series Editor.

[4]B. Perumana, J.-H. Zhan, S. Taylor, B. Carlton, and J. Laskar,"Resistive-feedback CMOS low-noise amplifiers for multiband applications,"*IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1218–1225, May2008.

[5]A. Nieuwoudt, T. Ragheb, H. Nejati, Y. Massoud, Increasing Manufacturing Yield for Wideband RF CMOS LNAs in the Presence of Process Variations, 8th International Symposium on Quality Electronic Design, 2007,IEEE, p.801-806

[6]M. Reja, I. Filanovsky, and K. Moez, "A CMOS 2.0–11.2 GHz UWB LNA using active inductor circuit," in *IEEE Int. Symp. Circuits Syst.(ISCAS)*, May 2008, pp. 2266–2269.

[7]M. Nair, Y. Zheng, and Y. Lian, "1 V, 0.18 m-area and power efficient UWB LNA utilising active inductors," *Electron.Lett.*, vol. 44, no. 19, pp. 1127–1129, Nov. 2008.

[8] K Suray Kumar Department of ECE, NIT Calicut, India," Compact WIMAX Low Noise Amplifier using Active Inductor" *2011 IEEE.*

[9] A. Thanachayanont and A. Payne, "VHF CMOS integrated active inductor,"*Electron. Let.*, vol. 32, no. 11, pp. 999–1000, May 1996.

[10] D. DiClemente and F. Yuan, "Current-mode phase-locked loops—A new architecture," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54,no. 4, pp. 303–307, Apr. 2007

[11] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier,"*IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May1997.

[12] Tutorial-1,Low Noise Amplifier (LNA) Design,*Spring 2011: Radio Frequency Integrated Circuits (TSEK03).*

[13] 2. H. Fouad, K. Sharaf, E. El-Diwany and H. El-Hennawy, "An RF CMOS Cascode LNA with Current-reuse and Inductance Source degeneration," Radio Science Nineteenth National Conference Proceedings NRSC 2002, pp. 450–457.

[14] Chang-Hsi Wu* and Kuan-Lin Liu and Wei-Chen Department of Electronic Engineering Lunghwa University of Science and Technology" Design of a Low-Noise Complementary and Current-Reused Technology":*2012 IEEE*

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