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Abstract: - Radio Frequency Identification (RFID) UHF Tag based on RCEAT technique is proposed in this paper. RCEAT means Reliable and Cost Effective Anti-collision technique. The proposed system is designed with the help of Verilog HDL. The System is simulated using Modelsim SE 6.3f and it synthesized using XST. The RCEAT system is classified into two subsystems. One is Pre and another one is Post . By using Pre we have to detect the errors from incoming messages. And using Post we identify the tag.

Key words*: Verilog HDL,CRC remover, Fast-search look up table,Xlinx ise.*

1. INTRODUCTION

A significant advantage of RFID devices over the others identification devices is that the RFID device does not need to be positioned precisely relative to the scanner. As credit cards and ATM cards must be swiped through a special reader. In contrast, RFID devices will work within a few feet (up to 20 feet for high-frequency devices) of the scanner. But the problem associated with this technique is the collision of tags. So inorder to avoid coliision of tags a technique has been proposed which is both reliable and also cost effective. And so call this technique as Reliable and Cost Effective Anti-Collision Technique(RECEAT). This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power.

Some common problems with RFID are reader collision and tag collision. Reader collision occurs when the signals from two or more readers overlap. The tag is unable to respond to simultaneous queries. Systems must be carefully set up to avoid this problem. Tag collision occurs when many tags are present in a small area; but since the read time is very fast, it is easier for vendors to develop systems that ensure that tags respond one at a time.

The tag collision can be eliminated using different techniques.They are mainly of two types: a)Tree Based Algorithms and ALOHA based algorithms. where Tree based algoritms consists of Binary tree algorithms and Query tree. Whereas the ALOHA based algorithms are classified into ALOHA,Slotted ALOHA and Frame Slotted ALOHA. Some hardwares also desigened for this purpose. Here in this paper Tree algorithms has been considered with Fast Search Algorithm.

2. ARCHITECTURE :

The architecture consists of two parts:Pre RECEAT and Post RECEAT. The first part,the PRE RECEAT ensures that the incoming messages are errorless using a CRC-remover. In the CRC-remover the incoming messages are divided into two;the received ID and CRC. These two are sent to CRC checker for verification process where the received CRC is being checked with the recalcalucated CRC of the received message. If both are equal means no error and this is indicated by status bit which is set to zero. Otherwise the status bit is set to two. And then the status bit is updated and sent to status checker. If no errors are present then it is sent to the next part;the Post RECEAT part.

In PostRCEAT, the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process. The PostRCEAT reads all the ID bits at once regardless of its length. This is performed by using the word-by word multiplexing. During the identification process, the Fast-search module identifies the four tag's IDs simultaneously in one Read cycle. The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves.

To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves. The reader selects these IDs using the proposed Fast-search Lookup table, and then the selected ID will be identified. The four IDs will be identified from the smallest value to the largest one in one Read cycle. Then the tag that has successfully identified will be acknowledged by sending the Kill-tag.

Once the tags are identified the most significant bit is represented by 1,which specifies that the tags are identified. So we use Cyclic Redundant Check for getting errorless incoming messages and then those are checked with the recalculated one and then goes

to the Post part where using fast search algorithm four tags are considered at once then arranged into ascending order ,then comes out one by one using a parallel to serial converter. Which will be the final output which is both reliable and cost effective.

The whole process can be represented simply by using a block diagram as:

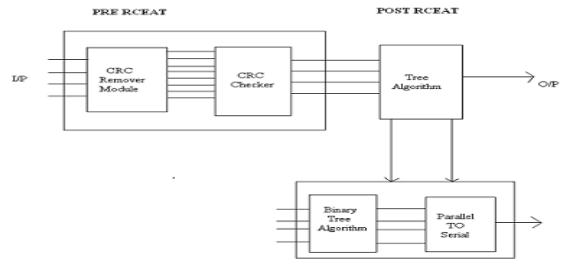
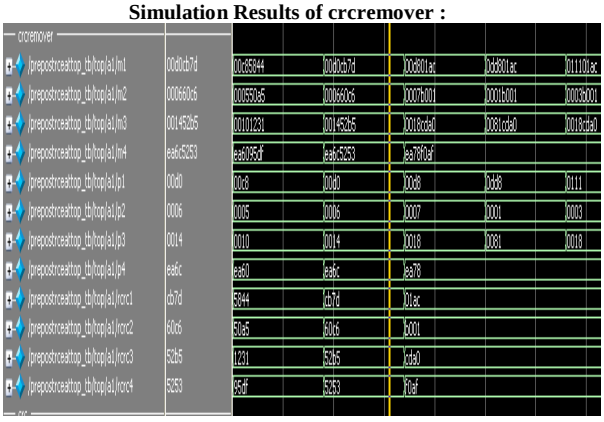


Fig:simple block diagram representation

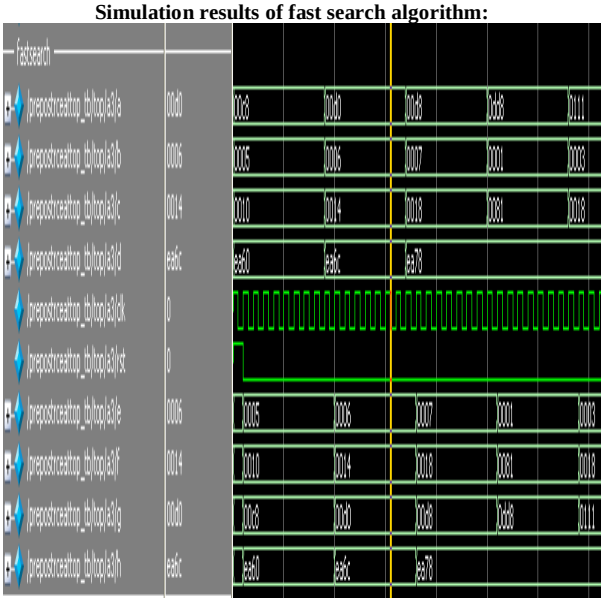
3. SIMULATION RESULTS:

The proposed technique has been simulated and verified using Modelsim and synthesized usisg Xlinx ISE and obtained the results. The obtained results are also shown:

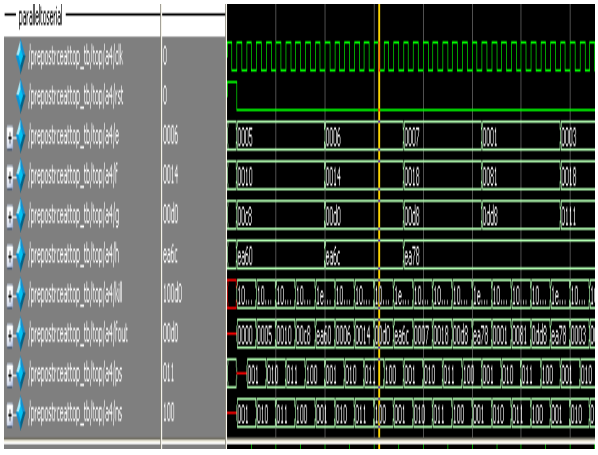
Simulation Results of crcremover :



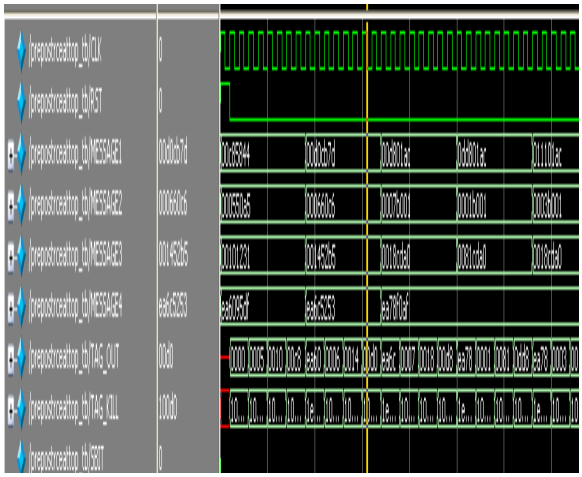
Simulation results of fast search algorithm:



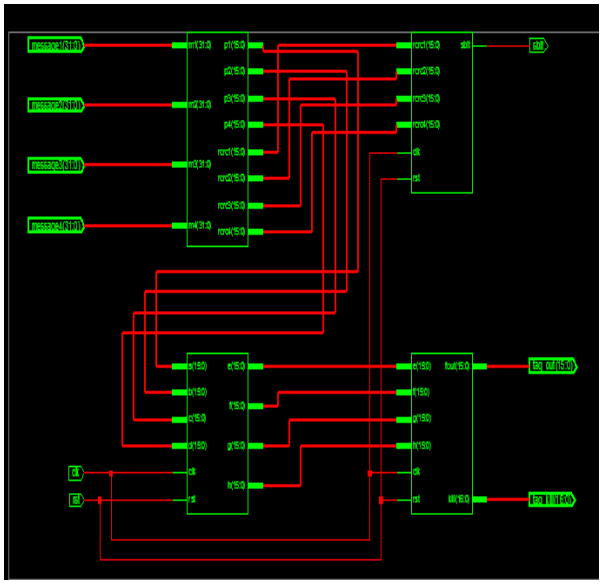
Simulation results of parallel to serial conversion:



Simulation result of prepostrceat module:



RTL Schematic:



4. DEVICE SUMMARY:

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	89	9,312	1%
Number of 4 input LUTs	430	9,312	4%
Logic Distribution			
Number of occupied Slices	222	4,656	4%
Number of Slices containing only related logic	222	222	100%
Number of Slices containing unrelated logic	0	222	0%
Total Number of 4 input LUTs	430	9,312	4%
Number of bonded IOBs	100	232	43%
Number of BUFGMUXs	1	24	4%

5. CONCLUSION

A proposed Reliable and Cost Effective Anti-collision technique (RCEAT) is designed to achieve a reliable and cost effective identification technique of the tag. The RCEAT architecture consists of two main subsystems; PreRCEAT checks error in the incoming packets using the CRC scheme. PostRCEAT identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinx Synthesis Technology (XST), Simulated using MODELSIM.

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