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CMOS Logic Design with FINFETS Using 32nm TECHNOLOGY

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ABSTRACT:- In this paper we propose double gate transistor i.e. FINFETS circuits. It is the substitute of bulk CMOS that mean without any compromise in fabrication process except one or two changes. Actually bulk CMOS suffers high power consumption and high leakage currents .so we implement a various novel circuits i.e FINFETS logic design style in 32nm technology and analyzing various parameters like power dissipation, delay, frequency are observed in this paper. In here we notice that less power consumption in FINFETS when compared to ordinary bulk CMOS. We also check the other submicron technology compared to that this submicron technology got less power consumption.

Keyword: Finfets, IG, LP, Hybrid, SG, CMOS,Nand

1.Introduction:-

Since the fabrication of MOSFET, the minimum channel length has been shrinking continuously. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. The sustained scaling of conventional bulk device requires innovations to circumvent the barriers of fundamental physics constraining the conventional MOSFET device structure. The limits most often cited are control of the density and location of dopants providing high I on /I off ratio and finite subthreshold slope and quantum-mechanical tunneling of carriers through thin gate from drain to source and from drain to body. The channel depletion width must scale with the channel length to contain the off-state leakage I off. This leads to high doping concentration, which degrade the carrier mobility and causes junction edge leakage due to tunneling. Furthermore, the dopant profile control, in terms of depth and steepness, becomes much more difficult. The gate oxide thickness tox must also scale with the channel length to maintain gate control, proper threshold voltage V_T and performance. The thinning of the gate dielectric results in gate tunneling leakage, degrading the circuit performance, power and noise margin.

. At the current pace of scaling, the industry predicts that planar transistors will reach feasible limits of miniaturization by 2010, concurrent with the widespread adoption of 32 nm technologies. At such sizes, planar transistors are expected to suffer from undesirable short channel effect, especially "off-state" leakage current, which increases the idle power required by the device. In a DG device, the channel is surrounded by two gates on surfaces, allowing more effective suppression of "off-state" leakage current. DG gates also allow enhanced current in the "on" state, also known as drive current. These advantages translate to lower power consumption and enhanced device performance Its main advantage is that better control of short channel effects, lower leakages and better yield in aggressively scaled CMOS process, will required to overcome these obstacles to scaling. .

2. FINFET (DG) Technology:-

Double gate MOSFETs (DG-FET) is a MOSFET that has two gates to control the channel. Its schematic is shown in Fig. 1. Its main advantage is that of improved short channel effects. Now a day FINFETS very usually using because of short channel effects, better in driving current, more compactable that other device.FINFETS are substitutes for bulk CMOS. The two gates for FINFETs provide effective control of the short-channel effects without aggressively scaling down the gate-oxide thickness and increasing the channel doping density. The separate biasing in DG device easily provides multiple threshold voltages. It

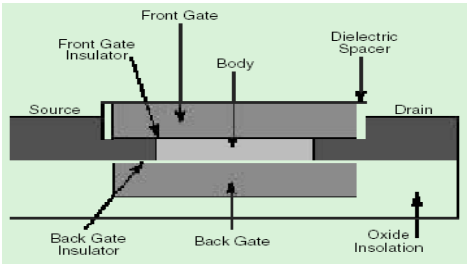


FIG1: DG transistor structure(FINFET)

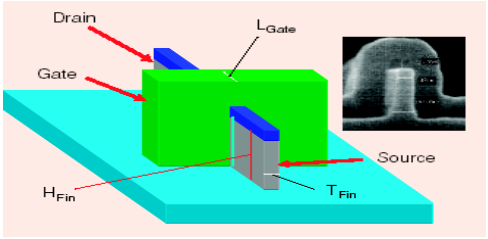


FIG2: FINFET structure

can also be exploited to reduce the number of transistors for implementing logic functions. In this paper we scale down upto 32nm .in here power consumption of FINFETS will be less compared to bulk CMOS.

$$\text{Effective channel length } L_{eff} = L_{gate} + 2\times L_{ext} \quad (1)$$
$$\text{Effective channel width } W = T_{fin} + 2\times H_{fin}$$

Where Hfin and Tfin are the fin height and thickness respectively, Lgate is length of the gate, Lext is extended source or drain region see in fig2.The main features of FINFETs are – Ultra thin Si fin for suppression of short channel effects, raised source/drain to reduce parasitic resistance and improve current drive. FINFETs are designed to use multiple fins to achieve larger widths. FINFETS provide much lower sub-threshold leakage currents than bulk CMOS at the same gate length

3. FINFETs Logic Design Styles:-

In this paper, comparison of various parameters between an ordinary two-input CMOS NAND and four FINFETs logic design styles for two-input NAND are presented.

3.1 CMOS NAND Gate:-

A two-input CMOS NAND gate is implemented by placing two NMOS in series and two PMOS in parallel with inputs (A, B) and output (Out). The output is low when the two inputs are high, else high which can be viewed from Table I. Here the channel is controlled by a single gate which is input to FET.

3.2 Short Gate (SG) Mode:-

The shorted-gate (SG) mode FINFETs style implemented by tying both gates, achieves high current drive and eventually decrease transistor delay by applying high voltage to both gates of N-FINFETs and can have low leakage current with increase in threshold voltage of the front gate by back gate when both transistors are grounded. The SG – mode NAND gate can be obtained by directly translating the CMOS NAND design to FINFETs, while retaining the same size.

3.3 Independent gate (IG) mode:-

In this mode independent signals are used to drive the two device gates, the back gate can be used independently as an input to reduce the number of transistors needed to implement numerous logic functions. This can be designed to have asymmetric rise and fall delays because only one transistor gate is used to pull-up but this can lead to large disparities under conditions of greater load.

3.4 Low-power (LP) mode:-

In this mode back-gate is tied to a reverse-bias voltage to reduce leakage power and the drive strength of every FINFET is reduced equally.

3.5 Hybrid (IG/LP) mode:-

This mode is a modification of the IG design, the parallel transistors, i.e. the pull –up for NAND is merged. Unlike the IG design, delays are balanced by reducing the strength of the complimentary series structure, this can be achieved by tying the back gates of FINFETs in series to a strong reverse bias .The circuit diagrams of ordinary CMOS two-input NAND and different FINFETs-based two-input NAND gate styles are shown from Fig. 3 - Fig. 8.

INPUT1	INPUT2	OUTPUT
0	0	1
0	1	1
1	0	1
1	0	0

Table I- Truth table of 2-input NAND gate

FINFETS Circuit Diagram:-

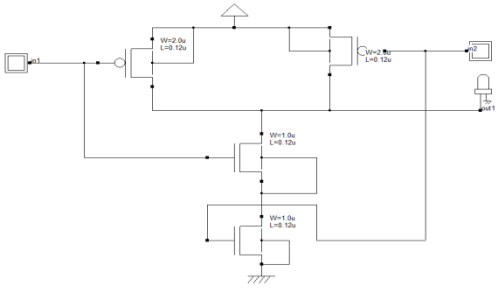


FIG3. Finfet Cmos Nand

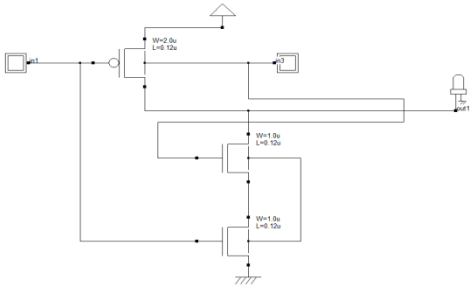


FIG4.IG/LP mode Nand

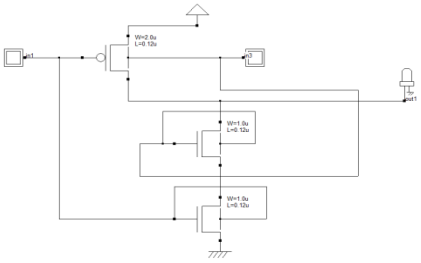


FIG5.IG mode Nand

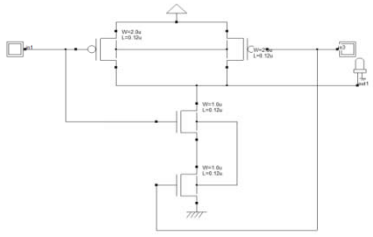


FIG 4: LP Mode Nand

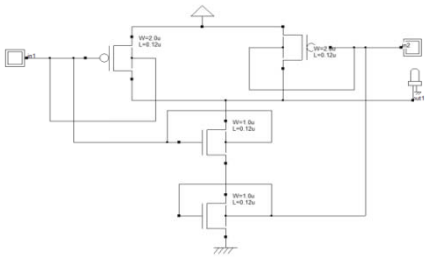


FIG7. SG mode Nand

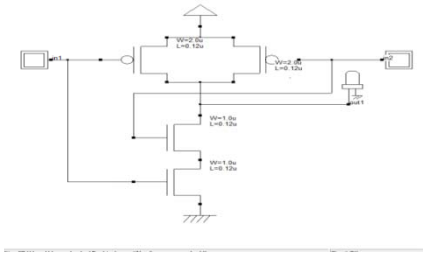


FIG8.Ordiary Cmos Nand

Results and Discussion:-

The six mode of circuits and layout of two input five FINFETS Nand gate and one ordinary Nand gate (bulk CMOS) are doing the work in microwind tool3.1 with 32nm foundry .using this tool we constructed device , implemented and simulated the results. In here we first design the circuit and checking the logic using truth table see the Fig3 to Fig8 and Table I .After that we convert the circuit into layout design see Fig9 to Fig14 .Next the design rule must be checked before applying the inputs. The design rule which is used in simulation is lambda based design rule. From the table II we show the various powers applying the input and get the output of various Finfet circuits and ordinary CMOS gate. From the Table II we also compare the power dissipation of ordinary CMOS and Finfet circuits. The output of the power results are shown in Table II its corresponding graph is shown Graph I. Using microwind tool we also analyzed the some more parameter they are delay, capacitance, inductance, resistance and frequency. These parameter results are show in GraphII to GraphIV.when compare to other FINFETS device IG mode Nand gate has less power dissipation. We also check at 65nm IG has more leakages when compared to others. In this paper using 32nm technology we decrease those leakages in 65nm as possible as.LP, SP, CMOS FINFET Nand when compare to IG and Hybrid, it will gets less leakages.

Finfet Layout Diagram:-

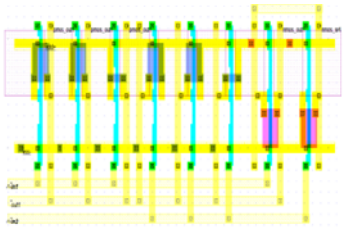


FIG9.Finfet Cmos Nand

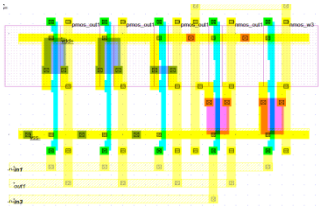


FIG10.IG/LP Mode Nand

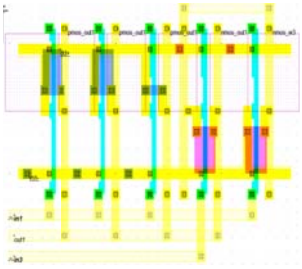


FIG11.IG Mode Nand

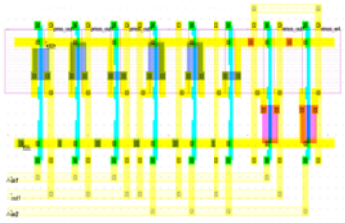


FIG12.LP Mode nand

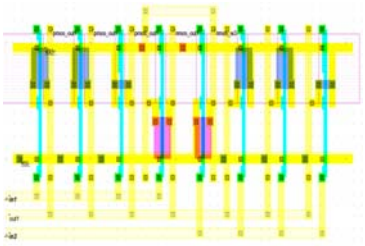


FIG13.SG Mode Nand

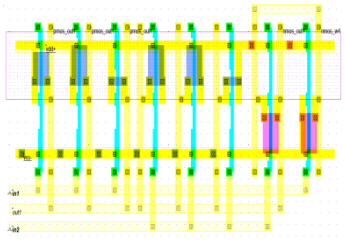
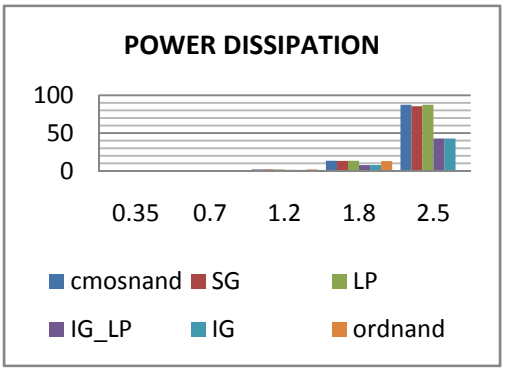


FIG14.Ordinary Cmos Nand

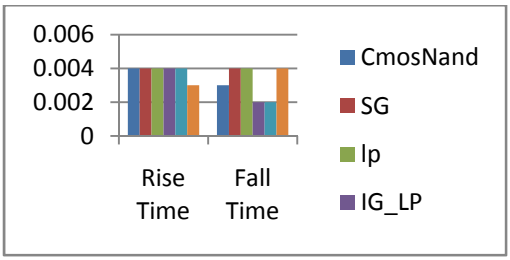
Various parameters Table and Graphs:-

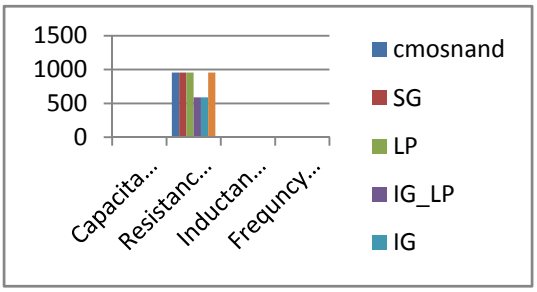
SUPPLY VOLTAGE	POWER DISSIPPATION					
	CMOS NAND	SG	LP	IG_LP	IG	Ordinary Nand
0.35	0.065	0.065	0.065	0.043	0.043	0.066
0.7	0.318	0.313	0.319	0.215	0.211	0.322
1.2	1.958	1.927	1.960	1.382	1.350	1.921
1.8	13.357	13.095	13.360	7.631	7.368	12.985
2.5	87.478	85.634	87.489	42.852	40.750	87.990

Table I: comparisons of ordinary Nand and Diff. Finfet Nand



GraphI:Power DIssipation





Graph III: Finfet Nand Gate outputs Delay(ns)

GraphII:various parameter

Conclusion:-

In this paper we discussed various circuits for various parameters like power consumption, delay, frequency, o/p capacitance/p resistance/p inductance. Among all circuits IG gets less power consumption and resistance compared to other FINFETS devices. Hybrid IG/LP mode gate get the less capacitance output compared to other FINFETS device and bulk CMOS. Compared to the bulk CMOS Nand gate, FINFETS device gets less power dissipation.

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