Graduate Research in Engineering and Technology (GRET)

Volume 1 | Issue 1 Article 6

July 2013

AN EFFECTIVE APPROACH OF BILATERAL FILTER IMPLEMENTATION IN SPARTAN-3 FIELD PROGRAMMABLE GATE ARRAY

P. KARTHIKEYAN
ECE Department, Velammal College of Engineering and Technology, Madurai, India.,
Kpkarthi2001@gmail.com

M. GAUTHAM
ECE Department, Velammal College of Engineering and Technology, Madurai, India.,
megauthamm@gmail.com

R. RAMAKRISHNAN
ECE Department, Velammal College of Engineering and Technology, Madurai, India.,
ramakrishnan7210@gmail.com

A. MOOKKAIYA
ECE Department, Velammal College of Engineering and Technology, Madurai, India.,
mookkaiya.a@gmail.com

Recommended Citation

KARTHIKEYAN, P.; GAUTHAM, M.; RAMAKRISHNAN, R.; and MOOKKAIYA, A. (2013) "AN EFFECTIVE APPROACH OF BILATERAL FILTER IMPLEMENTATION IN SPARTAN-3 FIELD PROGRAMMABLE GATE ARRAY," *Graduate Research in Engineering and Technology (GRET)*: Vol. 1 : Iss. 1 , Article 6.
DOI: 10.47893/GRET.2013.1005
Available at: https://www.interscience.in/gret/vol1/iss1/6

AN EFFECTIVE APPROACH OF BILATERAL FILTER IMPLEMENTATION IN SPARTAN-3 FIELD PROGRAMMABLE GATE ARRAY

P.KARTHIKEYAN[1], M.GAUTHAM[2], R.RAMAKRISHNAN[3] & A.MOOKKAIYA[4]

[1,2,3&4]Assistant Professor, ECE Department, Velammal College of Engineering and Technology, Madurai, India.
E-mail: Kpkarthi2001@gmail.com, megauthamm@gmail.com, ramakrishnan7210@gmail.com, mookkaiya.a@gmail.com

Abstract- This paper presents the Field Programmable Gate Array (FPGA) implementation of Bilateral Filter, in order to achieve high performance and low power consumption. Bilateral filtering is a technique to smooth images while preserving edges by means of a nonlinear combination of nearby image values. This method is nonlinear, local, and simple. We give an idea that bilateral filtering can be accelerated by bilateral grid scheme that enables fast edge-aware image processing. Nowadays, most of the applications require real time hardware systems with large computing potentiality for which fast and dedicated Very Large Scale Integration (VLSI) architecture appears to be the best possible solution. While it ensures high resource utilization, that too in cost effective platforms like FPGA, designing such architecture does offers some flexibilities like speeding up the computation by adapting more pipelined structures and parallel processing possibilities of reduced memory consumptions. Here we have developed an effective approach of bilateral filter implementation in Spartan-3 FPGA.

Keywords- *FPGA, Bilateral filter, image denoising, VLSI, Bilateral grid*

I. INTRODUCTION

Image processing is a method to convert an image into digital form and perform some operations on it, in order to get an enhanced image or to extract some useful information from it. Basically images are corrupted by noise in random manner during image acquisition and transmission. The various types of noise include gaussian noise, impulse noise, salt and pepper noise. The overall noise characteristics in an image depend on many factors like sensor type, pixel dimensions, temperature, exposure time, and ISO speed. Removing noise from the original image is still a challenging problem for researchers. Image denoising is used to the recovery the digital image that has been contaminated by noise. Many denoising methods have been developed over the years; among these methods, bilateral filter is the most popular approach [1]. In addition to image denoising, bilateral filter has also been used in some other applications like image enhancement, tone mapping and volumetric denoising [4].The bilateral filter is a powerful filter:

- One application of it gives the effect of numerous iterations using traditional local filters,
- Can work with any reasonable distances d_R and d_S definitions,
- Easily extended to higher dimension signals, e.g. Images, video, etc.
- Easily extended to vectored-signals, e.g. Color images, etc.

Various Implementation schemes have been analyzed and bilateral grid is observed as the effective - implementation scheme. An important issue with the application of the bilateral filter is the selection of the filter parameters, which affect the results significantly and another research interest of bilateral filter is the acceleration of computation speed. Digital image processing is an ever expanding area with various applications such as medicine, space exploration, surveillance and many more areas. Implementing such applications on a general purpose computer is easier, but time consuming due to additional constraints on memory and other peripheral devices. Application specific hardware implementation offers much greater speed than a software implementation. Nowadays, most of the applications require real-time hardware systems with large computing potentiality for which fast and dedicated Very large scale integration (VLSI) architecture appears to be the best possible solution. With advances in the VLSI technology hardware implementation has become an attractive alternative. There are two types of technologies available for hardware design. Full custom hardware design also called as Application Specific Integrated Circuits (ASIC) and semi custom hardware device, which are programmable devices like Digital signal processors (DSPs) and Field Programmable Gate Arrays (FPGA's). A fixed hardware approach using an ASIC would have flexibility limitations making FPGA a better choice. An FPGA consists of a matrix of logic blocks that are connected by a switching network. Both the logic blocks and the switching network are reprogrammable allowing application specific hardware to be constructed. This paper describes an approach to the implementation of bilateral filter algorithms on FPGAs.

The paper is organized as follows
SECTION II: BILATERAL FILTER
SECTION III: FPGA IMPLEMENTATION
SECTION IV: RESULT AND DISCUSSION
SECTION V: CONCLUSION

II. BILATERAL FILTER

Bilateral Filter was first introduced by Smith and Brady under the name "SUSAN" [6] and was later referred as "Bilateral Filter" by Tomasi and Manduchi [1]. The bilateral filter is a heuristic tool for removing noise from images [1]. This filter is merely a weighted average of the local neighborhood samples, where the weights are computed based on temporal (or spatial in case on images) and radiometric distances between the center sample and the neighboring samples. This filter is also locally adaptive, and it was shown to give similar and possibly better results to those obtained by the previously mentioned iterative approaches. The bilateral filter is technique to smooth images while preserving edges [Fig. 1, 2]. Bilateral filter is a nonlinear filter which combines domain and range filtering. The key idea of the bilateral filter is that for a pixel to influence another pixel, it should not only occupy a nearby location but also have a similar value.

Figure-1 Input Image

Figure-2 Smoothed version of the image

The bilateral filter has several qualities:

- Its formulation is simple: each pixel is replaced by a weighted average of its neighbors.
- It depends only on two parameters that indicate the size and contrast of the features to preserve.
- It can be used in a non-iterative manner.
- It can be computed at interactive speed even on large images.

The bilateral filter takes a weighted sum of the pixels in a local neighborhood; the weights depend on both the spatial distance and the intensity distance. In this way, edges are preserved well while noise is averaged out. Mathematically, at a pixel location, the output of the bilateral filter is calculated as follows:

$$\bar{I}(x) = \frac{1}{C} \sum_{y \in N(x)} e^{-\frac{1\|y-x\|^2}{2\sigma_s^2}} e^{\frac{-I(y)-I(x)^2}{2\sigma_r^2}} I(y)$$

where σ_s and σ_r are parameters controlling the fall-off of the weights in spatial and intensity domains, respectively, σ_s is a spatial neighborhood and C is the normalization constant

$$C = \sum_{y \in N(x)} e^{\frac{-\|y-x\|^2}{2\sigma_s^2}} e^{\frac{-I(y)-I(x)^2}{2\sigma_r^2}}$$

A. *Parameters*

The bilateral filter is controlled by two parameters: σ_s and σ_r. Here the term I denotes the image, and I_p denotes the image at pixel position P. BF [I] designates the output of a bilateral filter F applied to the image I. We will consider the set S of all possible image locations as spatial domain, and the set R of all possible pixel values as range domain. $||\mathbf{p} - \mathbf{q}||$ is the Euclidean distance between pixel locations **p** and **q**.

The Algorithm for direct implementation of bilateral filter is given below,

For each pixel **p** in *S*

(1) Initialization:

(2) For each pixel **q** in *S* $BF[I]_p = 0, W_p = 0$

a. $BF[I]_p^+ = wI_q$
b. $w = G_{\sigma_s}(\|p - q\|)\, G_{\sigma_r}(|I_p - I_q|)$
c. $W_p^+ = w$

(2) Normalization: $BF[I]_p = I_p / W_p$

Here W_p is the normalization factor, $G\sigma_s$ is the spatial Gaussian weight, $G\sigma_r$ is the range Gaussian. The Computation of weights for one pixel near an edge is illustrated in the Fig. 3.

III. FPGA IMPLEMENTATION

There are several approaches for the implementation of Bilateral Filter. It includes Brute Force, Separable Kernel of Pham [7], Local Histograms of Weiss [8] and Bilateral Grid [10, 9].

The brute force implementation is efficient for small spatial kernels but become quickly prohibitive for

large kernels because of the quadratic dependence in σ_s. The separable kernel approach yields significantly faster running times but the performance still degrades linearly with the kernel size. Although it is satisfying for uniform areas and straight edges, it forms a poor match to more complex features such as textured regions. Local Histogram approach is able to handle any kernel size in short times but the iterations are complex.

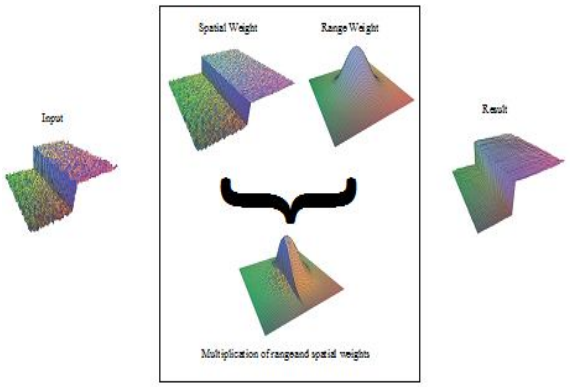

Figure-3 Illustration on how the weights are computed for one pixel near an edge

Bilateral Grid method can be used when Graphics hardware is available because it achieves high-quality outputs and real-time performances even on high-resolution images and videos. To process color images, the bilateral grid provides a satisfying solution, especially with large kernels. Hence Bilateral Grid approach is used in the implementation of bilateral filter in Spartan 3 FPGA.

The hardware used to support the bilateral filter implementation is the Xilinx Spartan-3 FPGA. Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications. It has certain features like 74,880 logic cells, 633 I/O pins , Double Data Rate (DDR) support, Abundant logic cells with shift register capability, Wide and fast multiplexers, Fast look-ahead carry logic, Dedicated 18 x 18 multipliers. Using System Generator, the FPGA design and simulation is carried out using Xilinx blocks. After the successful simulation, the synthesizable VHDL code is automatically generated from the models for final FPGA implementation.

A relatively low-level data flow approach at the register transfer level (RTL) was taken since this makes explicit the distortion correction and interpolation pipelines. The Summary of Spartan-3 FPGA Attributes is shown in Table I.

The device used is XC3S400. It has 400K system gates, 8064 logic cells, 896 Configurable Logic Blocks, 16 dedicated multipliers, Maximum of 264 I/O ports and 116 Maximum differential I/O pairs.

IV. RESULTS AND DISCUSSIONS

On applying various numbers of iterations in the implementation of bilateral filter, it is observed that the resource usage is minimum. The device used is XC3S400. The results are as follows. The total number of system gates used is 20% of the total system gates available. Only 25% of logic cells were used and hence the resource usage is low. Out of 896 Configurable Logic Blocks only 20% is used. It is observed that only 30% of the multipliers are used. The results are summarized in Table II.

TABLE-I SUMMARY OF SPARTAN - 3 FPGA ATTRIBUTES

Device	System gates	Logic cells	Total CLBs	Dedicated multipliers	Maximum User I/O	Maximum Differential I/O pairs
XC3S400	400K	8,064	896	16	264	116

TABLE-II RESULTS

Device	System gates	Logic cells	Total CLBs	Dedicated multipliers	Maximum User I/O	Maximum Differential I/O pairs
XC3S400	80K	2016	179	5	53	24

V. CONCLUSION

In this paper, the FPGA implementation of bilateral filter is performed. A number of iterations are performed using bilateral grid approach to determine the resource usage. It is determined that the bilateral filter is a powerful alternative to the iteration-based filters for noise removal. The use of bilateral filter results in Low resource usage. Since there is low resource usage the power consumption is low. As a result the computational speed is high.

REFERENCES

[1] C. Tomasi and R. Manduchi, “Bilateral filtering for gray and color images,” Proc. Int. Conf. Computer Vision, 1998, pp. 839–846.

[2] M. Elad, “On the origin of the bilateral filter and ways to improve it,” *IEEE Trans. Image Process.*, vol. 11, no. 10, pp. 1141–1151, Oct. 2002.D. Barash, “A fundamental relationship between bilateral filtering, adaptive smoothing, and the nonlinear diffusion equation,” *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 24, no. 6, pp. 844–847, Jun.2002.

[3] Ming Zhang and Bahadir K.Gunturk, “ Multiresolution Bilateral Filtering for Image denoising ,“ *IEEE Trans. Image Process.*, vol. 17, no. 12, pp. 2324–2333, Dec. 2008.

[4] Michael M.Bronstein, “Lazy sliding window Implementation of the Bilateral filter on parallel Architectures,“ *IEEE Trans. Image Process.*, vol. 20, no. 6, pp. 1751–1756, Jun. 2011.

[5] Smith, S.M., Brady, J.M.,” SUSAN – a new approach to low level image processing,”International Journal of Computer vision 23,pp.45-78,1997.

[6] T. Q. Pham and L. J. van Vliet, "Separable bilateral filtering for fast video preprocessing," in *Proceedings of the IEEE International Conference on Multimedia and Expo*, 2005.

[7] Computational Intelligence in Scheduling (SCIS 07), IEEE Press, Dec. 2007, pp. 57-64, doi:10.1109/SCIS.2007.357670.

[8] B.Weiss, "Fast median and bilateral filtering," *ACM Transactions on Graphics*, vol. 25, no. 3, pp. 519–526, Proceedings of the ACM SIGGRAPH conference,2006.

[9] S. Paris and F. Durand, "A fast approximation of the bilateral filter using a signal processing approach," *International Journal of Computer Vision*, vol. 81, no. 1, pp. 24–52, 2009.

[10] J. Chen, S. Paris, and F. Durand, "Real-time edge-aware image processing with the bilateral grid," *ACM Transactions on Graphics*, vol. 26, no. 3, p. 103, Proceedings of the ACM SIGGRAPH conference, 2007.

[11] Sylvain Paris, Pierre Kornprobst, Jack Tumblin and Fr´edo Durand, "Bilateral Filtering: Theory and Applications "Foundations and Trends in Computer Graphics and Vision Vol. 4, No. 1 (2008) 1–73.

[12] www.xilinx.com/support/documentation/data_sheets/ds099.pdf