Convolutional Coding Using Booth Algorithm For Application in Wireless Communication

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Abstract— Convolutional codes are preferred types of error control codes which can achieve low BERs at signal to noise ratio (SNR) very close to Shannon limit. Here, a new method of convolutional encoding is proposed using the general Booth algorithm for multiplication. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. It can be a useful technique for use in chip design as it provides significant improvements. In this work, the performance of conventional convolutional coding with Viterbi decoding in AWGN channel, is studied and the results show the effectiveness of the work described here.

I. INTRODUCTION

To control or to mitigate distortion during data transmission in digital communication systems, error control coding is frequently used in various communication systems. The primary function of an error control encoder-decoder pair (codec) is to enhance the reliability of message during transmission of information carrying symbols through a communication channel. In all types of communication, the channel introduces noise and interference to corrupt the transmitted signal. At the receiver, the channel corrupted transmitted signal is recovered. Bit errors may result during transmission and the number of bit errors depends on the amount of noise and interference in the communication channel [1].

Among the existing error control codes, Convolutional codes are the most widely used channel codes in practical communication systems. These codes are developed with a separate strong mathematical structure and are primarily used for real time error correction. Convolutional codes convert the entire data stream into one single codeword and those encoded bits depend not only on the current k input bits but also on past input bits of the sequence. The main decoding strategy for convolutional codes is based on the widely used Viterbi algorithm [3]. Convolutional coding with Viterbi decoding has been the predominant Forward error correction technique used in space communication, particularly in geostationary satellite communication networks. In this work, the design and implementation Of Booth Encoder for

Convolutional Coding of digital signals in AWGN Channel is carried out. The description is related to the design of a Booth encoder for implementation of convolutional codes for certain digitally modulated waveforms so as to generate Bit Error Rate (BER) plots with varying Signal to Noise Ratio (SNR)s as a measure of performance in wireless channels.

II. THEORETICAL BACKGROUND

A. Convolutional Encoding

Convolutional codes are commonly described using two parameters: the code rate and the constraint length. The code rate, k/n, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter, K, denotes the "length" of the convolutional encoder, i.e. how many k-bit stages are available to feed the combinatorial logic that produces the output symbols [4]. A simple convolutional encoder is shown in Fig (1). The information bits are fed in small groups of k-bits at a time to a shift register. The output encoded bits are obtained by modulo-2 addition (EX-OR operation) of the input information bits and the contents of the shift registers which are a few previous information bits [5]. The shift register of the encoder is initialized to all zero state before encoding operation starts. A binary convolutional code is generated by passing the information sequence to be transmitted through a linear finite state shift register. For a (n,1,K)

convolution code, the shift register consists of K stages and n linear modulo-2 function generators. The input data is shifted into and along the shift register a single bit at a time producing a n-tuples output for each shift. The input
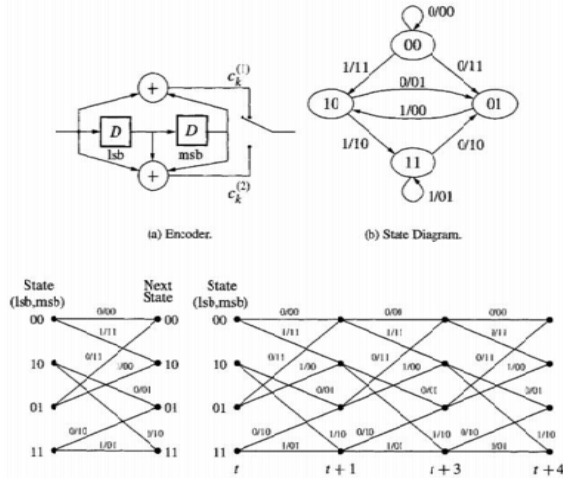

Figure 1: Encoder, state diagram, and trellis for $G(x) = [l + x^2; 1 + x + x^2]$
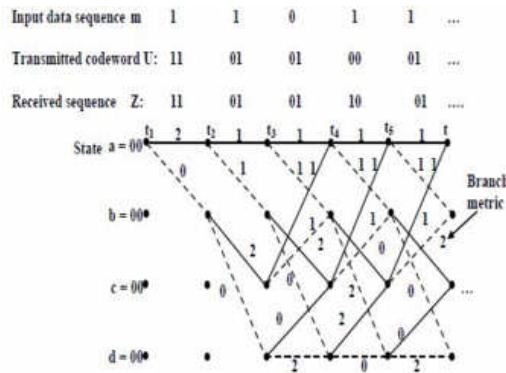

Figure 2. Trellis diagram, used in the decoder corresponding to the encoder in figure 1.

stream m_k passes through two filters (sharing memory elements) producing two output streams

$$C_{k1} = m_k + m_{k-2} \quad and \quad C_{k2} = m_k + m_{k-1} + m_{k-2} \quad (1)$$

These two streams are interleaved together to produce the coded stream C_k. A rate $R = k/n$ convolutional code has associated with it an encoder, a $k \times n$ matrix transfer function $G(x)$ called the transfer function matrix. For the rate $R = 1/2$

code of this example, $G_{a(x)} = [1 + x^2 \ 1 + x + x^2]$. The trellis diagram, which describes the operation of the encoder, is very convenient for describing the behavior of the corresponding decoder, especially when the famous "Viterbi Algorithm (VA)" is followed [3] [7]. Viterbi algorithm is a maximum likelihood sequence estimator (MLSE) computing the maximum likelihood code sequence given the received data. Figure (2) shows the trellis diagram for the encoder in Figure (1).

TABLE I: BASIC OPERATIONS TO BE DONE IN BOOTH ALGORITHM

b_i	B_{i-1}	operation
0	0	Do nothing
0	1	Add a
1	0	Subtract a
1	1	Do nothing

B. Booth Algorithm

Booth's algorithm is a well-known method for 2's complement multiplication. It speeds up the process by analyzing multiple bits of multiplier at a time. This widely used scheme for two's complement multiplication was designed by Andrew D. Booth in 1951. Booth algorithm is an elegant way for this type of multiplication which treats both positive and negative operands uniformly. It allows n-bit multiplication to be done using fewer than n additions or subtractions, thereby making possible faster multiplication. It operates on the principle that strings of 1s in the multiplier require no addition but just shifting and a string of 1s in the multiplier from bit weight 2^k to weight 2^m can be treated as 2^{k+1} to 2^m[8]. This algorithm involves examination of the multiplier bits, and shifting of the partial product. Prior to the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged according to the following rules:

- The multiplicand is subtracted from the partial product upon encountering the first least significant 1 in a string of 1's in the multiplier.
- The multiplicand is added to the partial product upon encountering the first 0 (provided there was a previous in a string of 0's in the multiplier.

- The partial product does not change when the multiplier bit is identical to the previous multiplier bits. The following table explains in detail (Table:I)

III. EXPERIMENTAL DETAILS AND DISCUSSION

Our main motivation for the work is to devise an efficient convolutional encoder designed with the help of the Booth algorithm which is a fast method multiplication. It is designed to obtain the convolutionaly encoded data bits in a high speed manner, by reducing the no. of partial products in the multiplication operation. The design is basically based on an architecture which is energy and area efficient than a conventional multiplier at the

performance level. Figure 3 shows the block diagram of the hardware realization of Booth multiplier. Using this architecture, the design of Booth multiplier is carried out, which is shown in Figure 5. Next, a Convolutional encoder is designed to show the effectiveness of using this fast multiplier in the performance of error correction. The position of the Booth multiplier is shown in the Convolutional encoder design in figure 5. Booth multiplication algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. Convolutional encoding involves a lot of 2's complement calculations and hence the Booth Algorithm designed to deal with such arithmetic is ideally suited to

Figure 5: Block diagram of the propose Convolution encoder using Booth multiplier.

Figure 3: Block diagram of the Booth multiplier.

Figure 4: The complete circuit of Booth multiplier.

Figure 6: Simulation results of data transmission using Convolution encoder using the Booth multiplier.

generate faster computation. This is useful for applications with communication system design primarily for wireless and mobile segments [9]. The performance of the newly designed encoder is shown in figure 6. The simulation of the encoder is carried out for code rate of ½ and constraint length k=7 for QPSK baseband modulation scheme.

The decoding scheme used here is Viterbi algorithm with hard decision technique. The error correction capabilities of convolutional encoding with the union bound performance estimates is depicted clearly as shown in figure 6. The simulation process involves first to generate a random sequence of binary data, next convolutional encoding and transmission through a wireless channel. The channel is considered to be showing AWGN and multipath fading characteristics. This figure shows different stages of the binary symbols which are sent through the Booth encoder. The Booth multiplier is used to encode the information symbols. The encoded symbol rate is twice the information symbol rate. The in-phase and quadrature components of the noiseless QPSK signal are plotted in the figure 6. in one plot. Then the demodulated and the decoded symbols are found to be identical to the transmitted signal which is depicted in the last part of the figure 10. In the decoding part, hard decision decoding technique with continuous decoding option is used.
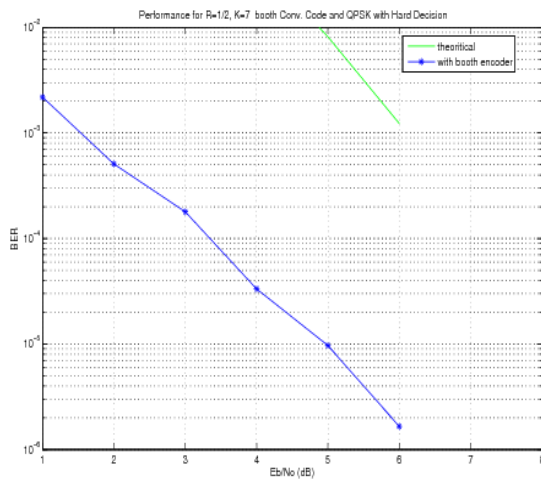

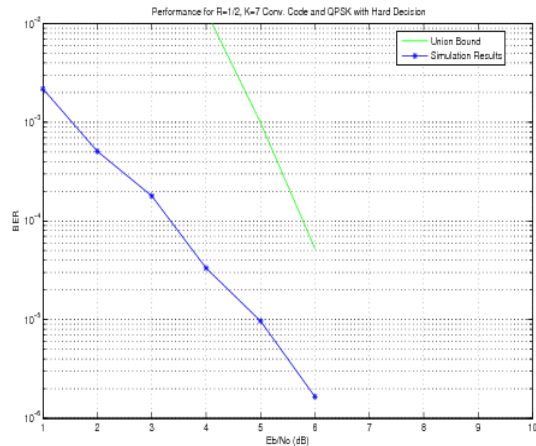Figure 7:BER performance using Convolution encoder using Booth multiplier for QPSK

Figure 8:BER performance using conventional Convolution encoder for QPSK.

This option causes a delay in the decoded stream of 10 symbols (traceback length = 10). Therefore the decoded data plot is shifted by 10 symbols to compensate for the decoder delay. In the final plot, the original message and the decoded output of the message transmitted through the channel are compared and it shows the effectiveness of coding technique being used.

IV. RESULTS

Results of BER performance for BPSK and QPSK modulation schemes over AWGN channel using the designed convolutional encoder are given in Figures 7 to 10.
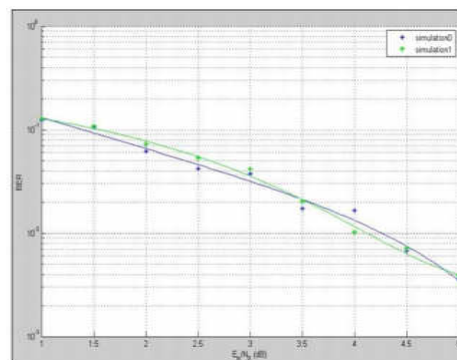

Figure 9: Comparative plot of the BER performance using conventional Convolution encoder and using Booth multiplier for QPSK
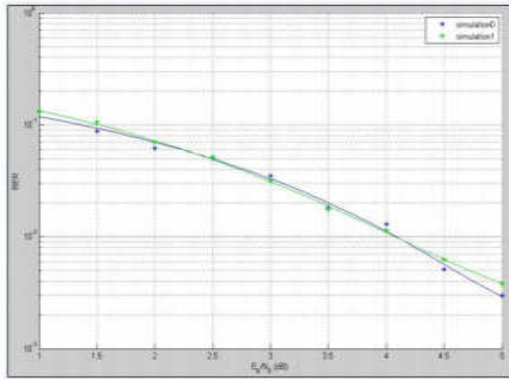
Figure 10: Comparative study of the BER performance using conventional Convolution encoder and using Booth multiplier for BPSK.

The systems are simulated by varying the value of bit energy to noise ratio (EbNo) from 1dB to 10dB. Figures 7 and 8 show the BER vs E_bN_o graph obtained for the designed encoder and the conventional convolutional encoder respectively. The individual BER plots are obtained to find the graph for the encoded data and the theoretical or un-coded data respectively for the two encoders. The BER vs SNR plots show that the BER value decreases for a specific SNR value in the coded model as compared to the un-coded one. This means, it gives a lower bit error rate for the same value of signal to noise ratio used in uncoded schemes. Thus, to achieve the same bit error rate the convolutional code will require a lower SNR. A lower SNR means a lower transmitter power. Figures 9 and 10 show the comparison of the error performance of the two different encoders in two different baseband modulation schemes, BPSK and QPSK. These BER vs EbNo graphs show similar type of error correction capabilities of the two encoders. Compared to a conventional encoder the Booth multipler based convolutional encoder generates on an average 10 to 15% time improvements. It thus necessitates the Booth algorithm based convolutional code encoder which proves effective in a range of wireless channels.

V. CONCLUSION

In this paper simulation results are presented on the performance of convolutional codes which are the widely used forward error correcting codes. The studies are made by appropriately modeling different systems for the two PSK modulation schemes and studying the performance of Convolutional Codes with respect to SNR noting the BERs for the cases when the encoder is a conventional one or a Booth multiplier based one. The work offers an insight into the development of a method for generating convolutional codes with faster multiplication and proves effective in arrange of wireless channels. The Booth encoder not only offers a fast multiplication, it also reduces the transmitter power and a less BER value is obtained at a specified SNR compared to the conventional process. A fast and energy-efficient encoder is such an important element which contributes substantially to the total power consumption of the system. On VLSI level, the area also becomes quite important as it is related to packing density and system cost. The Booth multiplication based convolutional encoder is thus designed keeping in mind these aspects.

REFERENCES

[1] B. Sklar: Digital Communication - Fundamental And Application, Second ed., Pearson Publication, 2005.

[2] C. E. Shannon, ``A Mathematical Theory of Communication'', *The Bell System Technical Journal*, pp- 379 - 427, 623-656,1948.

[3] A. J. Viterbi: ``Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm'', *IEEE Transactions on Information Theory*, Vol.IT-13, pp. 260-269, April, 1967.

[4] S. Haykin: Communication System. Fourth ed., Wiley Publication, 2008.

[5] J. G. Proakis: Digital Communication, McGraw-Hill Series, 2001.

[6] T. K. Moon: ``Error Correction Coding, Mathematical Methods And Algorithms'', Utah State University.

[7] T. S. Rappaport: Wireless Communication: Principle and Practice, Pearson Educational International, 2nd ed., 2002

[8] J. W. Mark and Weihua Zhuang: Wireless Communications and Networking, Prentice-Hall India, 2005.

[9] M. M. Mano: Digital Logic And Computer Design, Pearson Prentice Hall, 2005.

[10] S. T. Karris: Digital Circuit Analysis And Design With Simulink Modeling.

[11] M. M. Mano: Computer System Architecture, Third ed., Pearson Prentice hall, 2006.