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DESIGN & FPGA IMPLEMENTATION OF EFFICIENT MULTIBAND OFDM USING DWT/DUC/DDC

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Abstract - To increase data rate of wireless medium with higher performance, OFDM (orthogonal frequency division multiplexing) is used. Here DWT (Discrete wavelet transforms) is adopted in place of FFT (Fast Fourier transform) for frequency translation. Modulation schemes such as 16-QAM (Quadrature amplitude modulation) have been used in the development of OFDM system using DWT. In this paper, I propose a DWT-IDWT based OFDM transmitter and receiver .It has been proven that all the wavelet families better over the IFFT-FFT implementation.. The wavelet filter used in the project is Bi-orthogonal (9,7) with N=2. The Project also include implementation of Digital Up Converter and Digital Down Converter at the transmitter and receiver part respectively. The project is implemented on FPGA by designing using Verilog HDL and System Generator.

Key words : QAM,DWT/IDWT,Digital Up Converter, Digital Down Converter, FPGA.

I. INTRODUCTION

An Orthogonal Frequency Division Multiplexing (OFDM) system is a multi-carrier system which utilises a parallel processing technique allowing the simultaneous transmission of data on many closely spaced, orthogonal sub-carriers. Inverse fast Fourier transform (IFFT) and fast Fourier transform (FFT) in a conventional OFDM system are used to multiplex the signals together and decode the signal at the receiver respectively. The system adds cyclic prefixes (CP) before transmitting the signal. The purpose of this is to increase the delay spread of the channel so that it becomes longer than the channel impulse response. The purpose of this is to minimize inter-symbol interference (ISI). However, the CP has the disadvantage of reducing the spectral containment of the channels. multimedia systems, medical imaging, pay-TV & military communication .By using the transform, the spectral containment of the channels is better since it does not use CP [1], [2], [4], [5]. Digital Up Converters (DUC) and Digital Down Converters (DDC) are key components of RF systems in communications, sensing, and imaging.

II. WAVELET-BASED OFDM (DWT-OFDM):

One type of wavelet transform is namely as Discrete Wavelet Transform OFDM (DWT-OFDM). It employs Low Pass Filter (LPF) and High Pass Filter(HPF) operating as Quadrature Mirror Filters satisfying perfect reconstruction and orthonormal bases properties. The transform uses filter coefficients as approximate and detail in LPF and HPF respectively. The approximated coefficients is sometimes referred to as scaling coefficients, whereas, the detailed is referred to wavelet coefficients [3]. Sometimes these two filters can be

called sub-band coding since the signals are divided into sub-signals of low and high frequencies respectively.

The transceiver of DWT-OFDM is shown in Figure. 1. In the top part, the transmitter first uses a digital modulator (i.e 16-QAM) which maps the serial bits into symbols converting dk into X_m , within N parallel data stream $X_m(i)$ where $X_m(i)j0 \cdot i \cdot N ; 1$.

The main task of the transmitter is to perform the discrete wavelet modulation by constructing ortho-normal wavelets. Each X_{mi} is first converted to serial representation having a vector XX which will next be transposed into CA . This mean that CA not only its imaginary part have inverting signs but also its form is changed to a parallel matrix. Then, the signal is up-sampled and filtered by the LPF coefficients or namely as approximated coefficients. Since our aim is to have low frequency signals, the modulated signals XX perform circular convolution with LPF filter whereas the HPF filter also perform the convolution with zeroes padding signals CD respectively. Note that the HPF filter contains detailed coefficients or wavelet coefficients. Different wavelet families have different filter length and values of approximated and detailed coefficients.

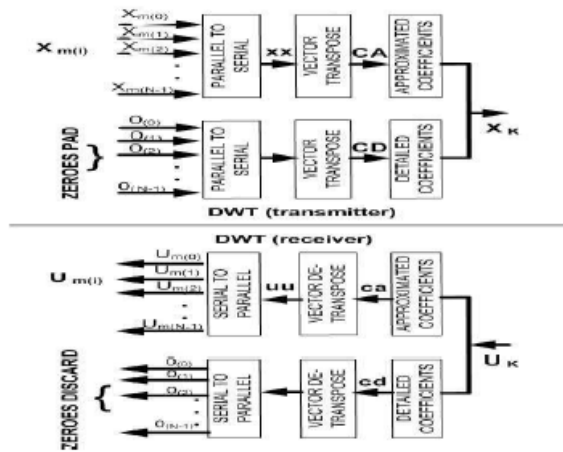


Figure 1: The proposed model of DWT-OFDM for substituting into the Inverse and Forward Transforms.

III. LIFTING BASED DWT ARCHITECTURE:

Lifting scheme is used for the development of architecture. Here N=2 means, we will be having two stages of lifting scheme i.e predict1, update1 and in second stage predict2, update2. The main feature of the lifting-based wavelet transform is to break-up the high pass and the low pass wavelet filters into a sequence of smaller filters. The lifting scheme requires fewer computations so the computational complexity is reduced. The lifting-based wavelet transform basically consists of three steps, which are called split, lifting, and scaling, respectively, as shown in Figure 2. The basic idea of lifting scheme is first to compute a trivial wavelet (or lazy wavelet transform) by splitting the original 1-D signal into odd and even indexed sub sequences, and then modifying these values using alternating prediction and updating steps.

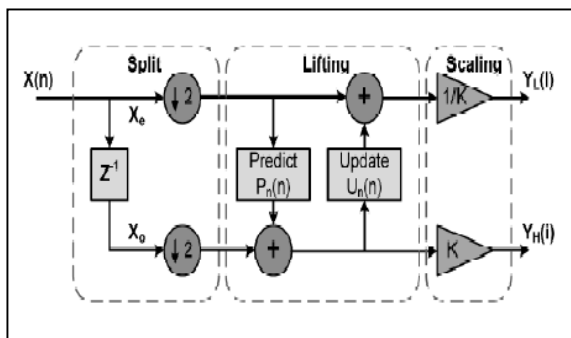


Figure 2: The lifting scheme implementation of 1D-DWT .

The lifting scheme algorithm can be described as follow:

- i. Split step: The original signal, $X(n)$, is split into odd and even samples (lazy wavelet transforms).
- ii. Lifting step: This step is executed as N sub-steps (depending on the type of the filter), where the odd and even samples are filtered by the prediction and update filters, $P_n(n)$ and $U_n(n)$.

- iii. Normalization or Scaling step: After N lifting steps, a scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass band ($Y_L(i)$), and the high-pass sub-band ($Y_H(i)$). Figure. 7 illustrates how the lifting scheme can be implemented using these steps. The diagram shows the lifting scheme for Daubechies (9, 7) bi-orthogonal filter.

The lifting scheme algorithm to the (9, 7) filter is applied as:

i. Split step

$$X_e = X(2i) \text{ Even Samples } \text{-----}(1)$$

$$X_o = X(2i+1) \text{ Odd Samples } \text{----}(2)$$

ii. Lifting Steps

For (9, 7) filter, $N=2$

$$\text{Predict P1: } D(i) = X_o(i) + a [X_e(i) + X_e(i+1)] \text{ ...}(3)$$

$$\text{Update U1: } S(i) = X_e(i) + b [D(i-1) + D(i)] \text{ } (4)$$

$$\text{Predict P2: } Y_H(i) = D(i) + c [S(i) + S(i+1)] \text{}(5)$$

$$\text{Update U2: } Y_L(i) = S(i) + d [Y_H(i-1) + Y_H(i)] \text{}(6)$$

iii. Scaling Step

$$Y_H(i) = K Y_H(i) \text{ -----}(7)$$

$$Y_L(i) = 1/K Y_L(i) \text{-----}(8)$$

Where $a=-1.586134342$, $b=-0.0529801185$, $c=0.882911076$, $d=-0.443506852$, and

$K=1.149604398$. These fractional values are multiplied by a factor of 128 to convert them

to decimal values.

Just reverse operation of this with corresponding sign change is carried out to compute IDWT.

IV. DIGITAL UP CONVERTERS AND DIGITAL DOWN CONVERTERS:

Digital Up Converters (DUC) and Digital Down Converters (DDC) are widely used in communication systems for scaling the sample rate of signals. Digital up conversion is required when a signal is translated from baseband to intermediate frequency (IF) band. Digital down conversion happens when a signal is converted from intermediate frequency band to baseband. DUCs and DDCs typically include frequency shifting using mixers, in addition to sampling rate conversion. The structure of a DUC or DDC depends mainly on the conversion ratio that is required.

Digital up converter (DUC) translates the base band signal to a higher frequency band. This is done by first up-sampling the base band signal to the required sampling frequency and then mixing it with a high-frequency carrier.

A functional block diagram of the DUC is given in Figure 3.

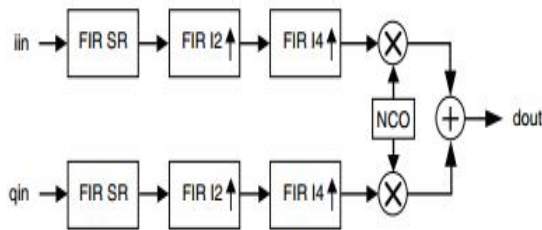


Figure 3: Functional block diagram of the DUC

The DUC has two identical paths, one for the I-input and the other for the Q-input. For this reason, it is also referred to as a complex DUC. The base band signal is first up-sampled to the IF frequency of 89.6 Msps before mixing with an NCO output to produce the spectrum centered around the desired modulation frequency. The sampling rate of the input signal is assumed to be 11.2 Msps. This signal has to be up-sampled by a factor of 8 to achieve a sampling rate of 89.6 Msps. This up-sampling can be done in many different ways. For example, there can be a single interpolation filter that performs up-sampling by 8 or there can be three interpolation filters connected in cascade, each performing an up-sampling by a factor of 2. For a FPGA implementation, smaller resource utilization is achieved by appropriately factoring the interpolation filters to more than one stage.

The digital down converter (DDC) performs the reverse function of that of a DUC. It converts a signal from the IF band to the base band. The DDC is built using a structure similar to the DUC, but it uses decimation filters instead of interpolation filters and they are connected in the reverse order of the DUC.

A functional block diagram of the DDC is shown in Figure 4.

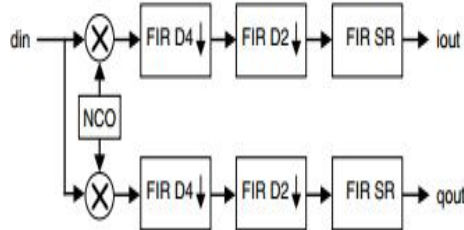


Figure 4: Functional Block Diagram of the DDC

As shown in Figure 8, the input signal is first mixed with the IF frequency sine and cosine outputs from the NCO.

This creates multiply replicated base band frequency response spectrum. The filter chain that follows the mixer reduces the sampling rate and performs low pass filtering to remove the spectral replications and to yield the correct base band spectrum. In Figure 8, the notations D4, D2 and SR are used to denote decimation by 4, decimation by 2

and single rate filters, respectively. The first filter in the chain is a decimation by 4 FIR filter (FIR D4) which reduces the sampling rate by 4 and performs low pass filtering. The pass band to stop band transition is not sharp for this filter. The second stage is a decimation by 2 FIR filter (FIR D2) with a moderate transition band.

V. SYSTEM DESIGN

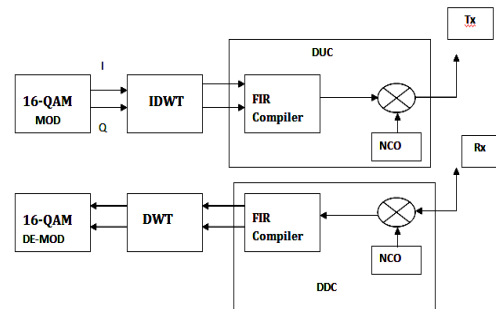


Figure 5 : Overview of the design

Figure 5 shows the design overview where the input given to QAM modulator which generate the I and Q values for the Inverse dwt, later sending it to the digital upconverter. To bring back the baseband signal at the receiver end, signal is down converted and passed to DWT ,later to Demodulator of QAM.

Here QAM Modulator/Demodulator, IDWT/DWT is written using the verilog HDL ,the digital down converter and Up converter by using the system generator Modeling. The overall design is as shown in Figure 6, whereas the QAM and DWT Hdl are included in black box.

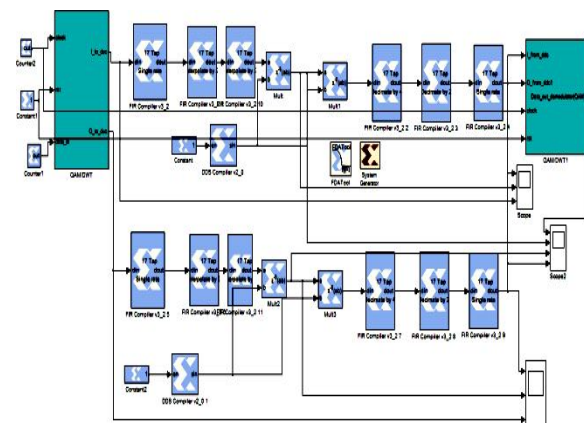


Figure 6: system implementation using system generator.

VI. RESULTS:

The Design for the DWT based OFDM is simulated and verified using ModelSim Simulator and implemented using Virtex II Pro FPGA board. The outputs is almost accurate that of the input at receiver end. The Hardware utilization for the design is as shown in the Table 1.

BUFGs	8 out of 32	25%
DSP48Es	240 out of 640	38%
LUT-Flip Flop pairs	9173 out of 58880	15%
Flip Flops	6006 out of 58880	10%
External IOBs	132 out of 640	20%

Table 1 : Device Utilization Summary.

VII. CONCLUSION

In this design of OFDM using DWT/DUC/DDC, it is clear that the usage of cyclic prefix can be avoided and the bandwidth efficiency can be improved, the baseband signal can be upconverted and down converted and is implementable on FPGA.



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