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# NOVEL GROUND BOUNCE NOISE REDUCTION WITH ENHANCED POWER AND AREA EFFICIENCY FOR LOW POWER PORTABLE APPLICATION

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**Abstract:** As technology scales into the nanometer regime ground bounce noise and heat dissipation immunity are becoming important metric of comparable importance to leakage current, active power, delay and area for the analysis and design of complex arithmetic logic circuits. In this paper, low leakage 1bit PFAL full adder cells are proposed for mobile applications with low ground bounce noise and heat dissipation in the circuits using adiabatic logic. The simulations are done using DSCH &MicrowindSoftware.

## INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call).

When an electronic device such as a mobile phone is in standby mode, certain portions of thecircuitry within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de-activated. Even if the leakage current is much smaller than the normal operating current of the circuit. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest. To summarize, some performance criteria are considered in the design and evaluation of adder cells, such as leakage power, active power, ground bounce noise, area, noise margin and robustness with respect to voltage and transistor scaling as well as varying process and compatibility with surrounding circuitries.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30xincrease in gate leakage. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity.

The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further peak of ground bounce noise is possible with proposed novel technique with improved staggered phase damping technique.

## PREVIOUS OPTIMIZATION TECHNIQUES

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches

to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level. Each transistor in series has a lower voltage at its output than at its input. If several devices are chained in series in a logic path, a conventionally-constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic always switches transistors to the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

## ALTERNATIVE APPROACH

Power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed novel technique. Modified sizings are shown in following figures respectively.

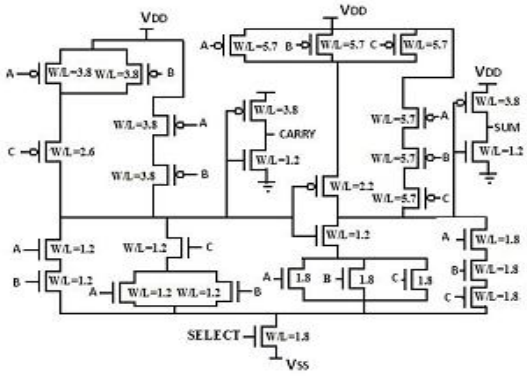



**Fig.1: full adder (Design1) circuit with sleep transistor.**

Each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because subthreshold current is directly propotional to the Width/Length ratio of transistor. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost. Modified adder circuit i.e Design2 shown figure, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby leakage power. Further compared to the Base case and Design1 and ground bounce noise produced when a circuit is connected to sleep transistor. However, there will be a slight variation on the noise margin levels and is almost equal to the Base case.

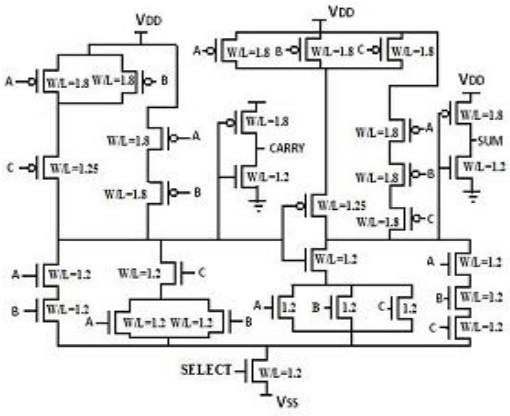



**Fig.2: 1 bit full adder (Design2) circuit with sleep Transistor**

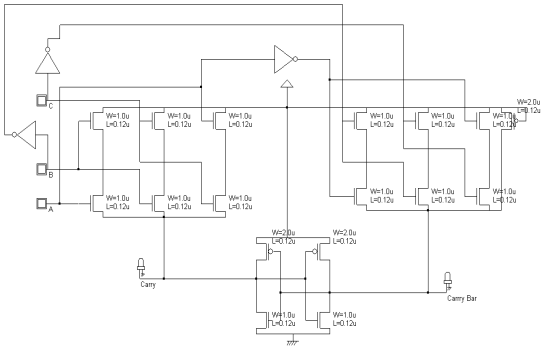



**Fig. 3: Proposed PFAL Adder Carry Circuit**

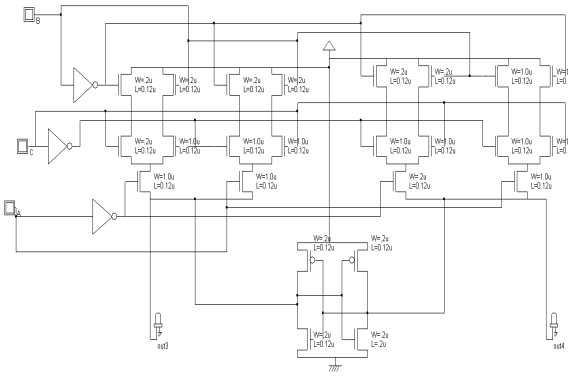
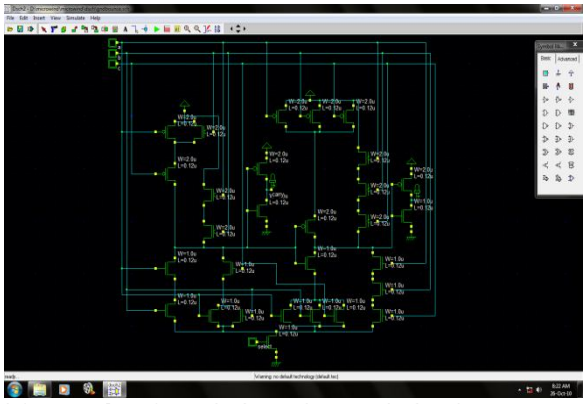


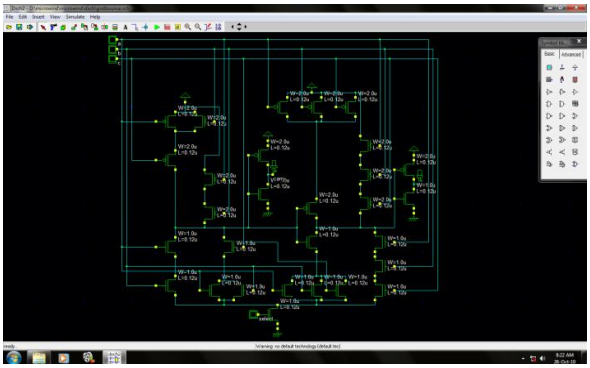
**Fig. 4: Proposed PFAL Adder SUM Circuit**

## SIMULATION RESULTS

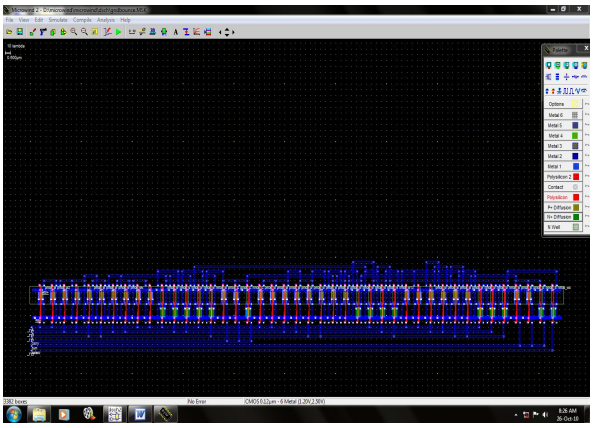
### SCHEMATIC DESIGN FOR CIRCUIT 1



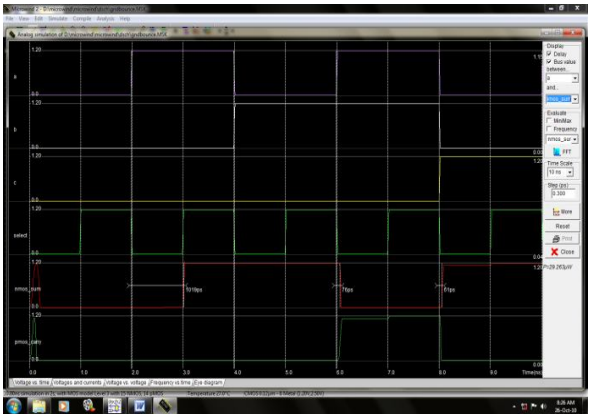
### SCHEMATIC DESIGN FOR DESIGN 2



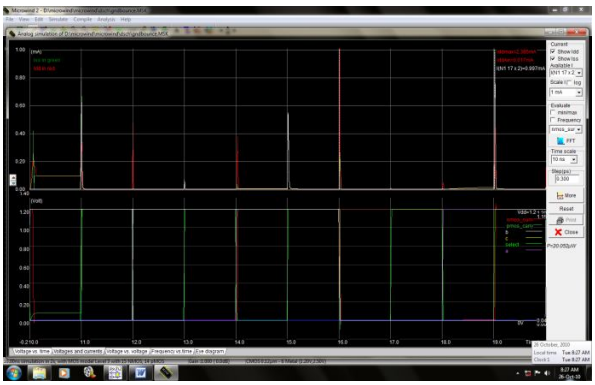
### 6.4. LAYOUT IN MICROWIND



### 6.5 ANALYSIS FOR VOLTAGE VS CURRENT



### 6.6. ANALYSIS FOR FREQUENCY VS TIME



## CONCLUSION

In this paper, low leakage 1 bit PFAL full adder cells are proposed for mobile applications.Which will enhance the battery power by reducing the heat leakage power using PFAL Logic. By using this Adiabatic logic circuit we are reducing the power by nearly 25% than the adders of Ground Bounce techniques shown in the paper the simulations are done using DSCH &Microwind Software.

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